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Modulation-Doped Heterovalent Structures for High-Speed Electronic Device Applications

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14. ABSTRACT
Optimized conditions for growing III-V, II-VI, and IV-VI materials in a single chamber were investigated, including experimenting with different growth modes, substrate temperatures, flux ratios, and interface termination.

15. SUBJECT TERMS
modulation doping, heterovalent structure, monolithic integration

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Final Report

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Executive Summary

This research program focused on the demonstration of modulation-doped heterovalent structures and their feasibility for novel high-speed electronic device applications using our recently proposed II-VI (BeMgZnCd)(SeTe) and III-V (InGaAl)(AsPSbBi) semiconductor systems lattice-matched to 6.1-Å GaSb, 5.65-Å GaAs, and other virtual substrates. These semiconductor binary and alloy materials have direct band gaps covering the entire energy spectrum from far-IR (~0 eV) to near-UV (~3.4 eV), with very high electron and hole mobilities, and similar thermal expansion coefficients.

The activities during the first year of the project mostly involved the growth and characterization of II-VI/III-V heterostructures based on GaAs, GaSb and InSb substrates: i) ZnTe virtual substrates were grown on lattice-matched GaSb substrates, and optimization of highly conductive InAsSb channel layers grown on ZnTe is ongoing; ii) High quality CdTe/MgCdTe HEMTs were grown on InSb substrates; and iii) Optimum conditions for ZnSe growth on GaAs substrates were explored.

The project activities during the second year included: 1) Optical and structural characterization of ZnSe/GaAs heterostructures grown in the dual-chamber MBE system; and 2) Growth of II-VI/III-V heterostructures and superlattice in a novel single-chamber MBE system

using GaAs, GaSb, InAs and InSb substrates. The combinations grown included ZnTe/GaSb, ZnSe/GaAs, CdSe/InAs, and CdTe/InSb heterostructures and superlattice.

The project activities during the third year included: 1) Optical and structural characterization of InSb/CdTe heterostructures grown in the dual-chamber MBE system; 2) Growth and development of Pb-containing IV-VI rock-salt crystals and the integration of these materials with lattice-matched zincblende heterostructures on InSb or GaSb substrates; 3) Optimized conditions for growing III-V, II-VI, and IV-VI materials in the single chamber were further investigated, including experimenting with different growth modes, substrate temperatures, flux ratios, and interface termination.

X-ray diffraction (XRD), transmission electron microscopy (TEM), and photoluminescence (PL) measurements were utilized continuously throughout these investigations to determine material characteristics and assess interface quality.

Research Results

A. Heterostructures grown with dual-chamber MBE system

1. Development of 6.1-Å materials system lattice-matched to GaSb substrates

The 6.1-Å materials system is an ideal platform for the integration of optoelectronics and high-speed electronics due to the wide range of materials that have this particular lattice constant. For example, ZnTe can be grown on widely available GaSb to form insulating virtual substrates, which would allow for vertical integration of multiple semiconductor devices on the same wafer. Notable materials with this approximate lattice constant include: GaSb (0.73 eV), AlGaSb (0.73 – 1.62 eV), AlAsSb (1.70 eV), InAsSb (0.26 eV), ZnTe (2.26 eV), CdSeTe (1.55 eV), and MgSeTe (3.13 eV). In addition, GaSb and InAsSb have ideal hole and electron mobilities (respectively), which are both required for high-speed and low-power CMOS devices. Development of high quality insulating layers could improve the gate leakage problem for III-V CMOS devices and allow for thinner barriers and smaller scaling. Such flexibility with the material parameters makes this system ideal for integrating CMOS technologies with optoelectronic devices that operate at nearly any wavelength.

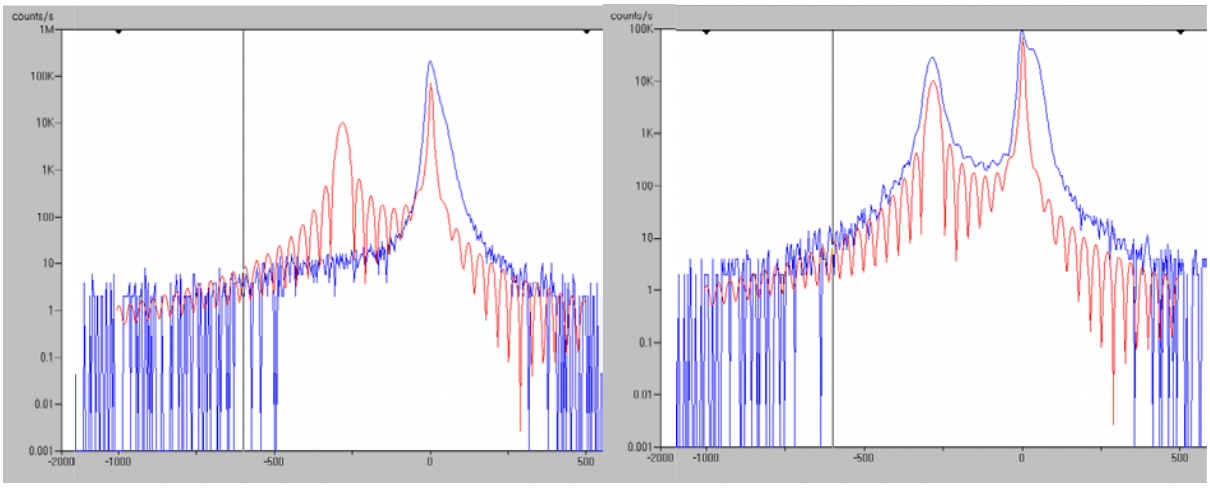
ZnTe/III-V heterostructures

High quality, insulating ZnTe virtual substrates have been successfully grown on lattice-matched GaSb substrates, and the optimization of highly-conductive InAsSb channel layers grown on ZnTe was also investigated. The optimum growth temperature of InAsSb is approximately 70 °C higher than the temperature at which Zn desorbs from the ZnTe surface. This requires a reduced growth temperature to retain the ZnTe buffer quality and to avoid poisoning the III-V chamber with Zn. RHEED surface reconstructions suggest that 3D material growth occurs at the InAsSb channel layer, most likely because of the reduced growth temperature required to suppress Zn outgassing from the ZnTe film. XRD diffraction curves show a deviation in the crystal structure with addition of the InAsSb QW layer. To better optimize the growth conditions, a Zn overpressure is needed at temperatures above 380°C to maintain stoichiometry in the ZnTe layer before the InAsSb layer growth is initiated. Meeting this requirement became possible with the single-chamber MBE system growth chamber, which was developed and completed later in the program.

Thermal property	GaSb	ZnTe	InAs
Optimal growth temperature	500 °C	320 °C	450 °C
Desorption temperature	400 °C (Sb)	380 °C (Zn)	430 °C (As)
Thermal expansion coefficient	7.75×10^{-6} °C^{-1}	8.0×10^{-6} °C^{-1}	4.52×10^{-6} °C^{-1}

Table 1. Key thermal coefficients for 6.1-Å materials

Photoluminescence (PL), X-ray diffraction (XRD), and transmission electron microscopy (TEM) data were collected for these 6.1-Å structures. From the XRD diffraction, we can demonstrate the importance of the interface bonding between two heterovalent materials and its effect on the interfacial cohesion and crystal structure of the epilayer for the specific case of ZnTe grown on GaSb substrates. ZnTe layers require suppression of Ga-Te bonding at the heterovalent interface, which displaces Sb from the surface and tends to reduce the ZnTe crystal quality. Therefore, a Zn-Sb interface termination is likely to be required for high quality heterovalent epitaxial growth due to its ability to retain the cubic zincblende structure under non-octet bonding instead of forming a charge-compensated compound as with the Ga-Te terminated interface. The XRD patterns shown in Fig. 1 for two identical structures, one with 10 seconds of Zn pre-growth overpressure, and the other with 10 seconds of Te overpressure before the deposition of 500 nm ZnTe on GaSb, clearly indicate the dependence on the interface termination for growth of the ZnTe/GaSb heterostructures. Extrapolating this result, ZnTe layers must be prepared with a Zn surface termination if III-V layers with ideal carrier properties are to be achieved. Efforts to develop a consistent method for preparing Zn-terminated virtual substrates to be grown at the relatively high temperatures required for high quality III-V growth are ongoing.



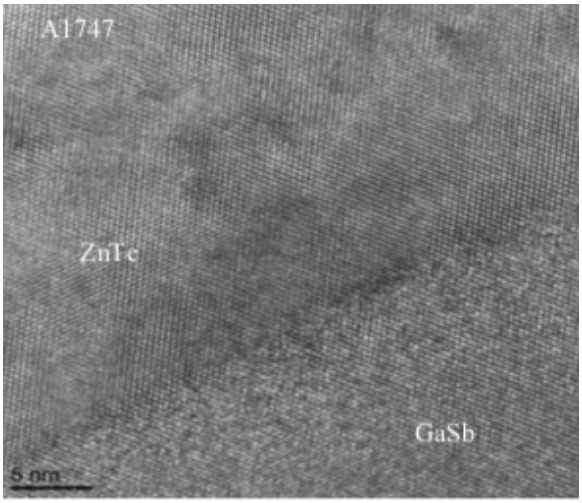


Figure 1. XRD patterns for 500-nm ZnTe layers grown on GaSb. Growth of the ZnTe film was preceded with 10 seconds of Zn flux for Sample A1747 (left), and 10 seconds of Te flux for Sample A1748 (right). The red curves show simulated patterns for monocrystalline ZnTe on GaSb.

Figure 2. High-resolution electron microscope image showing cross-section view of the coherent ZnTe/GaSb interface of Sample A 1747.

2. Exploration of 6.5-Å materials II-VI semiconductors lattice-matched to InSb

Although the 6.5-Å materials system lacks the versatility of the 6.1 Å system, this area is still of interest because it contains the semiconductor with the highest known electron mobility (InSb) and the best material for infrared detectors (HgCdTe), among others. Development of a relatively low-cost insulating substrate could therefore benefit the national defense, energy, and commercial microelectronics sectors. Mg can also be added to CdTe to increase the band gap (up to 3.46 eV) to create effective carrier blocking barriers with only a small effect on the lattice constant, as indicated in Figure 3. Because this material system represents the common semiconductors with the largest lattice constants, the choice of materials and their alloys is reduced compared with the other two systems. InSb is the only III-V semiconductor with a lattice constant greater than 6.2 Å which makes InSb-based electronics nearly impossible due to the lack of lattice-matched insulating layers. MgCdTe could potentially be utilized as an efficient lattice-matched barrier layer for InSb electronics, but a systematic study of the electrical properties at this interface is required to assess the feasibility of this idea.

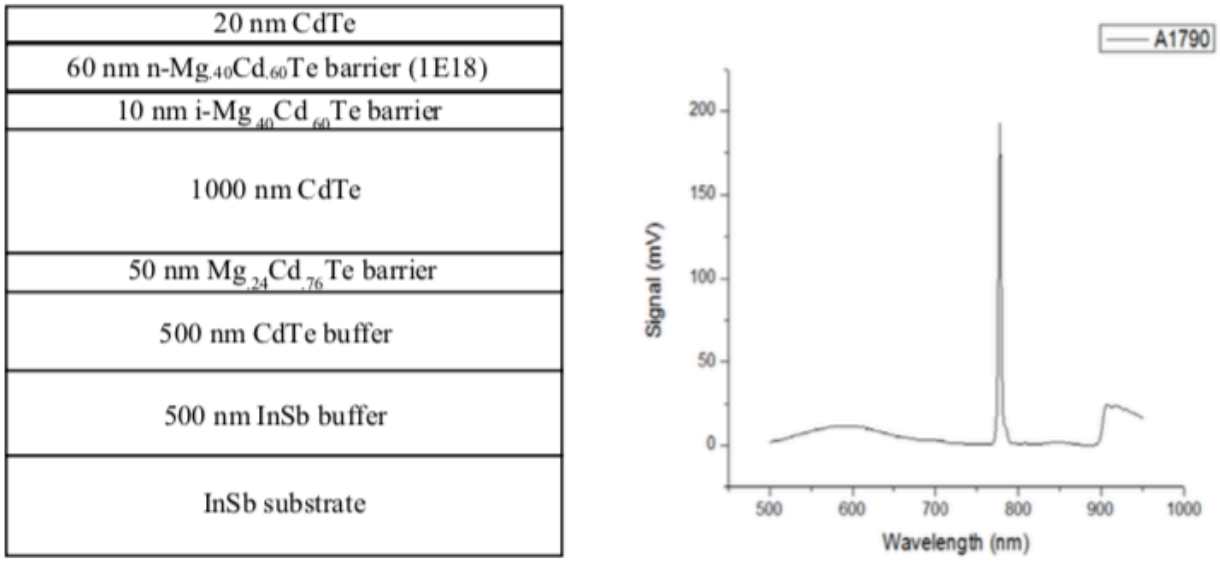


Figure 3. Left: Structure of Sample A1790: Right: PL spectrum (12 K) of sample A1790 CdTe/MgCdTe HEMT. showing very sharp peak at approximately 785 nm.

Very similar structure like this has also been used to demonstrate CdTe/MgCdTe double heterostructure solar cells with record Voc and efficiency. The results are published in the prestigious journal Nature Energy, May 2016. The paper has attracted a lot of attention from the solar cell community. The following paragraphs are some highlights from this paper.

---------- start of Nature paper highlights

To achieve long carrier lifetimes, we leverage high-quality CdTe epitaxially grown on InSb (001) substrates using molecular beam epitaxy (MBE) and CdTe/$Mg_xCd_{1-x}Te$ double-heterostructure (DH) designs. The complete desorption of the oxide layer on InSb substrates under a Sb flux and the near-perfect lattice match between InSb and both CdTe (0.03% mismatch) and MgTe (0.9% mismatch) enable extremely low defect density, and thus very good structural and optical properties. The DH designs offer optimal confinement for minority carriers and excellent passivation of the surfaces of the CdTe absorber layer.

To reduce the Interface Recombination Velocity (IRV), we employ a DH in which a CdTe absorber layer is sandwiched between two $Mg_xCd_{1-x}Te$ barrier layers. These wide- bandgap barriers effectively confine the minority carriers to the narrower-bandgap CdTe absorber. Furthermore, the CdTe/$Mg_xCd_{1-x}Te$ interfaces themselves are close to perfect, eliminating recombination-active defects at the absorber interfaces. Figure 1a shows time- resolved photoluminescence (TRPL) data for a set of four CdTe/$Mg_xCd_{1-x}Te$ DH samples, each consisting of two 30-nm-thick intrinsic $Mg_{0.46}Cd_{0.54}Te$ barriers and a CdTe middle layer with n-type background doping of the order of 10^{14} cm^{-3} and a thickness between 220nm and 541 nm. All samples exhibit effective carrier lifetimes determined by fitting single exponentials to the TRPL decay tails exceeding 2 µs, which attests to the high quality of the CdTe layers and the CdTe/$Mg_xCd_{1-x}Te$ heterointerfaces. Figure 1b plots the inverse nonradiative lifetime versus the inverse CdTe layer thickness for the four samples shown in Fig. 1a, which have 30-nm thick $Mg_{0.46}Cd_{0.54}Te$ barriers, and another set of four samples with identical layer structure and alloy composition but with 22-nm thick barriers. Weighted fittings of the data using the error bars yield effective IRVs of 1.2 ± 0.7 $cm.s^{-1}$ and 1.4 ± 0.6 $cm.s^{-1}$, which are comparable to or better than the best values reported for GaAs/$Al_{0.5}Ga_{0.5}As$ (18 $cm.s^{-1}$) and GaAs/$Ga_{0.5}In_{0.5}P$ (1.5 $cm.s^{-1}$).

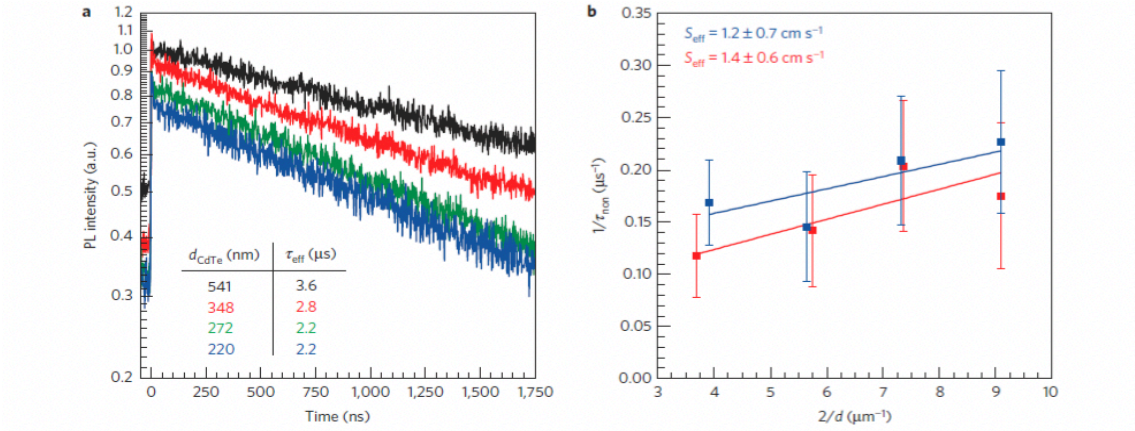


Figure 1 | CdTe double-heterostructure photoluminescence decay and interface recombination velocity. a, Normalized room-temperature time-resolved photoluminescence decay for a set of four DH samples, each consisting of two 30 nm $Mg_{0.46}Cd_{0.54}Te$ barriers and a CdTe layer with a thickness between 220 nm and 541 nm. The curves have been shifted along the *y*-axis for clarity. The fitted lifetimes are shown in the inset table. **b**, Inverse non-radiative recombination lifetime $1/\tau_{nr}$ versus inverse CdTe layer thickness $2/d$. The effective interface recombination velocities were extracted by fitting these data. The error bars of $1/\tau_{non}$ were determined by considering the uncertainty of the estimated radiative lifetimes due to the estimation of doping densities.

The studied device structure shown in Fig. 2a affords new opportunities with respect to addressing the challenge of p-type doping in CdTe: with interface passivation provided by the $Mg_xCd_{1-x}Te$ barrier layers, the contact layers can be defective. This structure maintains the voltage of the solar cell by preventing the contact layers from compromising the absorber quality, as the minority

carriers in the CdTe absorber will be confined by the barriers. That is, heterostructure barriers offer an alternative way to construct a junction in CdTe solar cells that circumvents the major challenge of p-type doping and opens the door to many novel device structure designs – a similar approach is used in HIT solar cells.

We used a 5- to 15-nm-thick heavily doped p-type amorphous silicon (a-Si:H, estimated doping level of 10^{18} cm^{-3}) or amorphous silicon carbide (a-SiC_y:H, y ~ 6%) layer as the p-type contact. These layers were deposited by plasma-enhanced chemical vapor deposition on the front $Mg_xCd_{1-x}Te$ barrier, followed by an indium tin oxide (ITO) electrode deposited by sputtering (Fig. 2a). The schematic band diagrams are shown in equilibrium in Fig. 2b and at open circuit in Fig. 2c. The intent of the design is that the barrier/contact stacks block the transport of minority carriers to the contacts while permitting majority carriers to flow unimpeded – minority carriers referring to the minority carrier type of each respective contact layer, not the absorber.

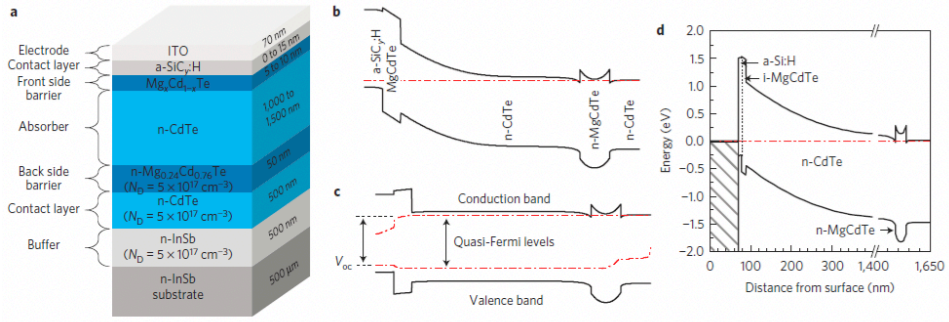


Figure 2 | Device design and band diagram. a, Layer structure of the CdTe/$Mg_xCd_{1-x}Te$ DH solar cell with an a-SiC_y:H (y = 0–6%) hole-contact layer. **b–d**, Schematic band diagrams at equilibrium (**b**) and open circuit (**c**) and an equilibrium band diagram drawn to scale for the hero cell (**d**). The band diagrams shown in **b** and **c** represent several different structure designs and are thus not drawn to scale with respect to energy and length. The parameters used for the calculation are given in Table 1.

The best tested device had a V_{oc} of 1.036V, a J_{sc} of 22.3 $mA.cm^{-2}$, a FF of 73.6%, and a power conversion efficiency of 17.0%, as shown in Fig. 5a. The measured reflectance loss and External Quantum Efficiency (EQE), and the corresponding calculated values are shown in Fig. 5b and 5c. The efficiency of 17.0% is the highest ever reported for monocrystalline CdTe solar cells and the V_{oc} of over 1 V is also significant to the CdTe solar cell community.

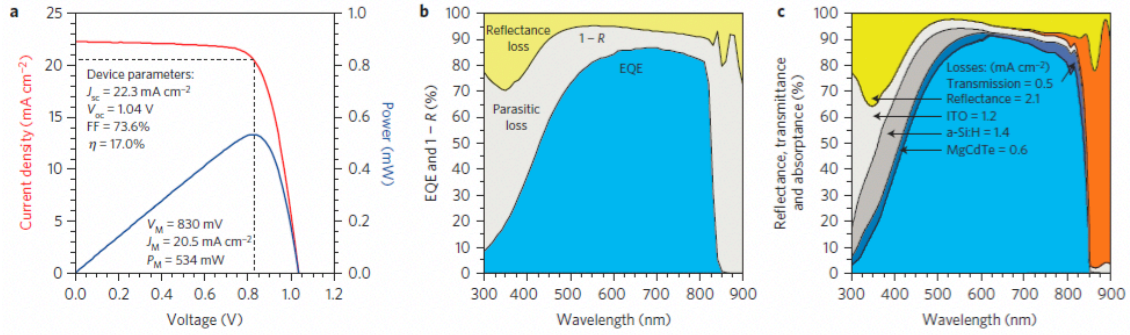


Figure 5 | Optimum device performance. a, Measured *J–V* curve and associated device parameters. **b**, Measured EQE and 1 — reflectance (1 — *R*) with a calculated photo-current of 22.3 mA cm^2. **c**, Simulated absorptance spectrum for the highest-performing CdTe solar cell device with a calculated photo-current of 23 mA cm^2. The device under test (Design B) has a 10-nm-thick $Mg_{0.30}Cd_{0.70}Te$ barrier layer, an 8-nm-thick a-Si:H hole-contact layer and an area of 0.03 cm^2.

---------- end of Nature paper highlights

3. Investigation of 5.65-Å materials lattice-matched to GaAs substrates

ZnSe/GaAs quantum well and double heterostructure samples were grown using a dual-chamber V80 system, which is equipped with separate II-VI and III-V growth chambers. Zn-As bonds were promoted at the interface by ramping down the GaAs growth with an As overpressure, and applying a Zn flux for 10s before and after the ZnSe growth. The first sample grown was a GaAs/ZnSe double heterostructure, with 500-nm GaAs confined by 200-nm ZnSe barriers. The ZnSe layer was grown at approximately 280°C after a 10-nm buffer grown at 240°C with a Zn/Se flux ratio of approximately 1. The RHEED showed streaky 2x1 surface reconstruction throughout growth suggesting high-quality ZnSe, while TEM images showed very little defect formation in the ZnSe and GaAs epilayers. The 500-nm GaAs layer was initiated at a substrate thermocouple temperature of 285°C and was gradually ramped to 500°C (460°C actual pyrometer temperature) at a rate of approximately 15°C/min. A sharp 2x4 RHEED surface reconstruction was apparent at 150 nm into the growth and this remained until the end of the GaAs layer growth. A 200-nm ZnSe cap was deposited on the GaAs layer using the same growth conditions as for the first ZnSe layer, and the RHEED pattern showed the same 2x1 surface reconstruction. TEM images (Fig. 4) and XRD (Fig. 5) confirmed the high epilayer quality, and the interfaces had virtually no defects that propagated between layers. Two distinct PL peaks from the double heterostructure are visible at 11 K (Fig. 6). The main GaAs emission peak of 870 nm is not apparent at 298 K and only appears below 200 K. A significant below-bandgap impurity peak is prominent at 10 K, but is not visible at higher temperatures.

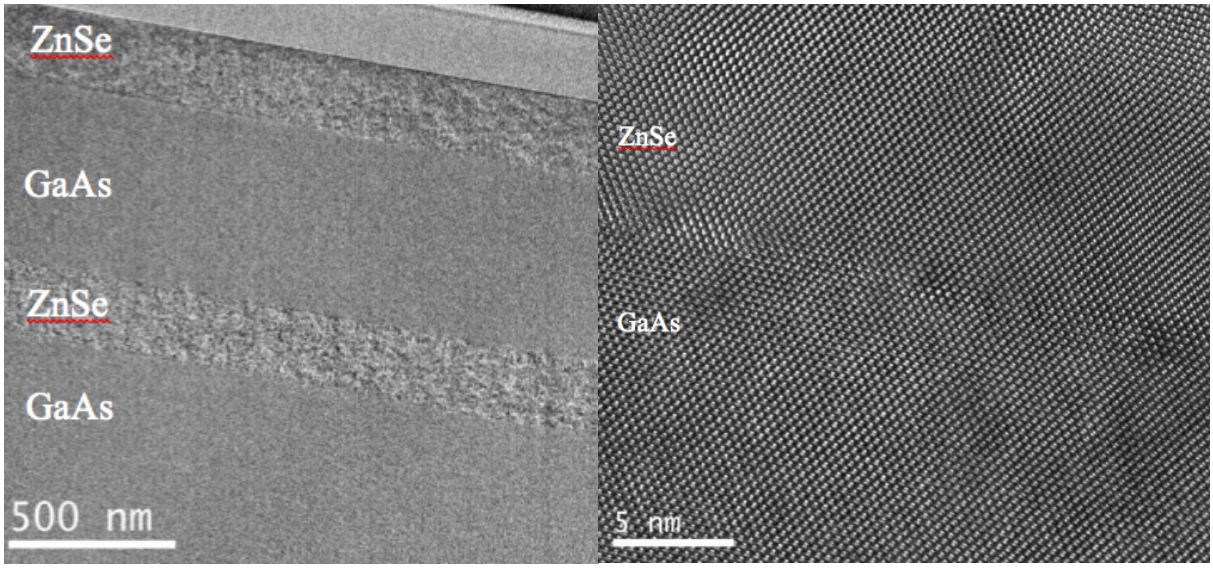


Fig. 4: TEM images showing cross sections of the GaAs/ZnSe double heterostructure grown in two-chamber MBE system.

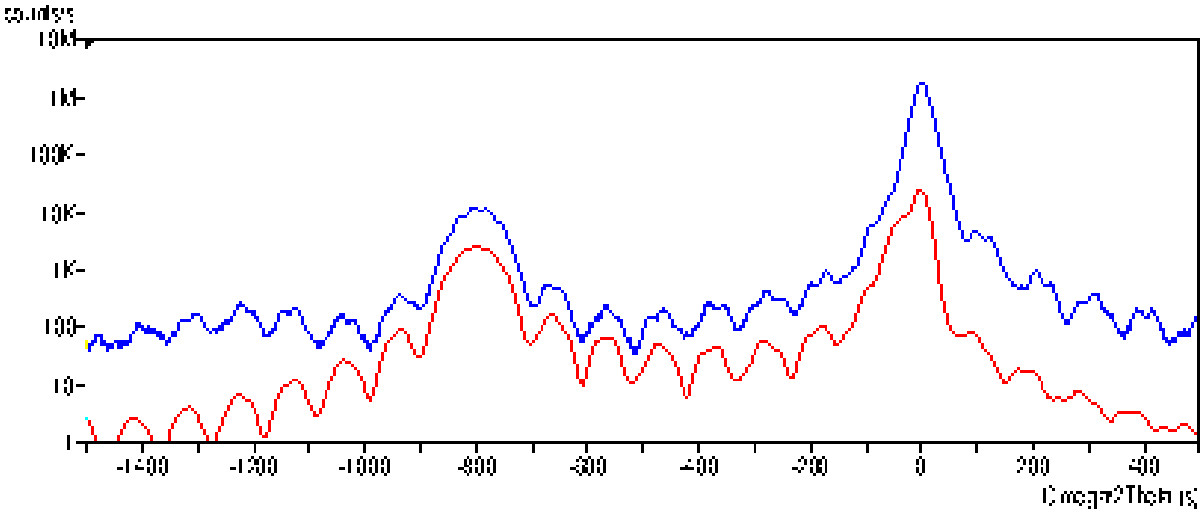


Fig. 5 (above): XRD pattern of the GaAs/ZnSe double heterostructure. The left peak is due to the ZnSe barrier layers.

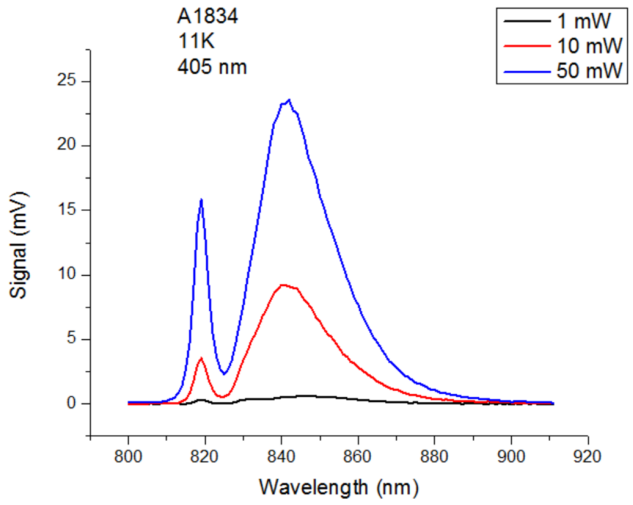
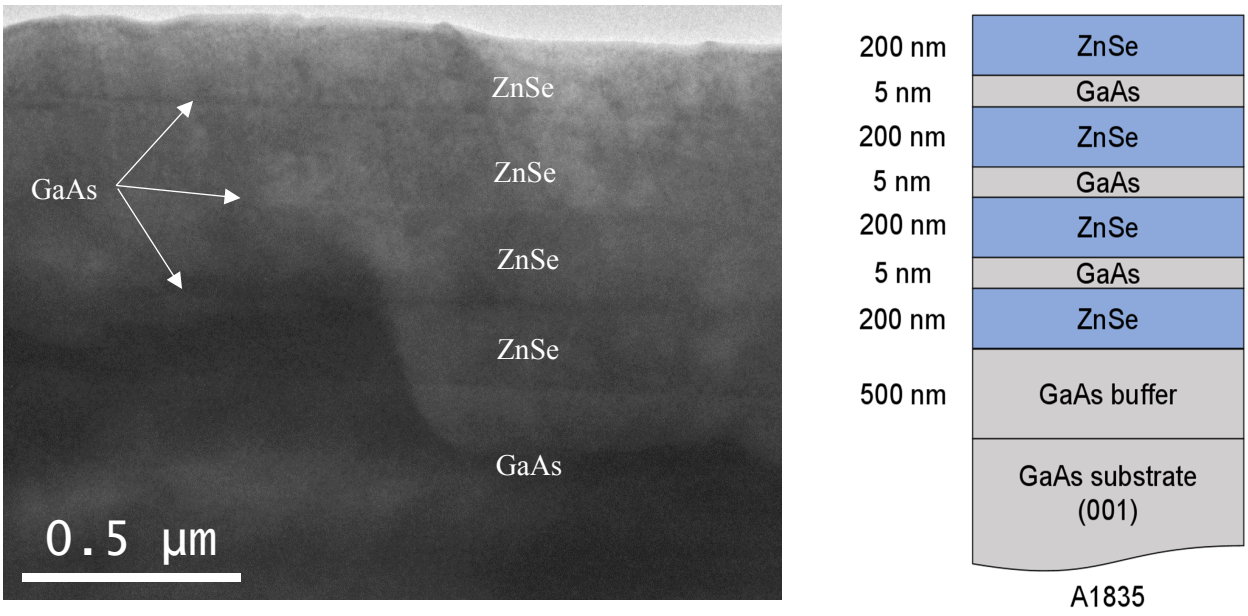
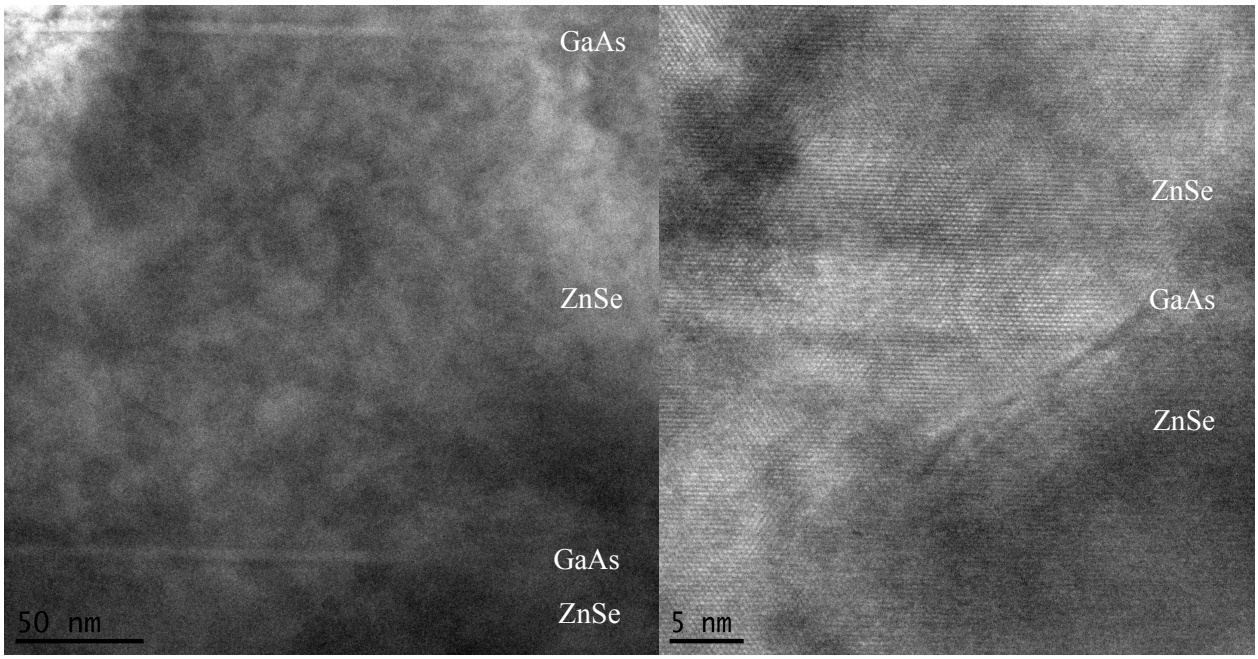


Fig. 6 (left): Temperature-dependent PL spectrum of the GaAs/ZnSe double heterostructure.

For the GaAs/ZnSe quantum well structure, 5-nm GaAs wells were confined by 200-nm ZnSe barriers (see Fig. 7). A similar approach of applying Zn/As over-pressure was used between the ZnSe and GaAs layers to promote high quality interface. The ZnSe barriers were grown using the same growth conditions as the first structure, but the GaAs quantum wells were grown at a substrate thermocouple temperature of 250°C. TEM images showed flat and abrupt interfaces between the ZnSe and GaAs layers, but some occasional stacking faults propagated upwards from the interfaces and their density multiplied as the number of wells increased. These may be due to some Ga-Se bonds forming at the interface due insufficient As pre-deposition before the GaAs growth. No photoluminescence was detected from the GaAs wells, even at low temperature, due to the reduced interface quality at the GaAs/ZnSe heterojunction, which drastically increased the interface recombination velocity and hence the parasitic non-radiative recombination in the GaAs wells.





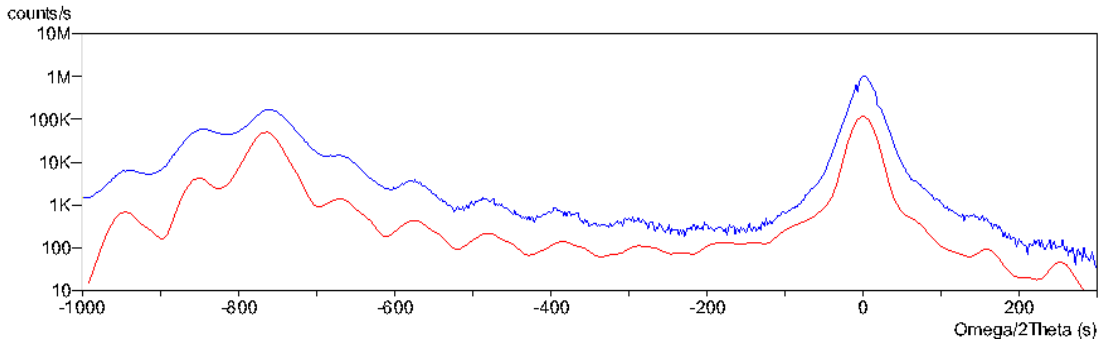


Fig. 7: TEM images and XRD profile of multiple 5-nm GaAs quantum wells confined by 200-nm ZnSe layers. Stacking faults propagate from the boundary, no PL signal observed from the wells.

2. Heterostructure growth with single-chamber MBE system

The new single-chamber MBE system is specifically designed for investigating heterovalent heterostructures, and it contains effusion cells with inter-changeable crucibles compatible with a wide variety of source materials. The system is currently equipped with Zn, Cd, Ga, In, As, Sb, Se, and Te cells to exploit all of the conventional lattice-matched heterovalent compounds (ZnSe/GaAs, ZnTe/GaSb, CdSe/InAs, and CdTe/InSb). Since the chamber is equipped with both II-VI and III-V materials, the interfaces between these compound semiconductors can be extensively studied by applying different elemental overpressures after growth of each layer to adjust the interface terminations. Our previous experiments have demonstrated the importance of avoiding III-VI bonds at the interface to minimize defects that propagate from the interface. With the new chamber, it was possible to go from applying a group V elemental over-pressure while ramping down the temperature from III-V growth to a group II over-pressure before the temperature becomes low enough for the group V atoms to form more than a single monolayer.

ZnSe/GaAs interface studies

The ZnSe/GaAs experiments have mainly focused on improving the growth conditions for depositing GaAs on ZnSe and controlling the interface structure to minimize defects in the epilayers. Unlike the dual-chamber system described above, elemental over-pressures can be applied at any time and with any substrate temperature. For example, a Zn flux can be applied to a ZnSe surface while the substrate temperature is ramping to the As deposition temperature to promote a Zn-As terminated interface. The surface reconstructions were monitored by RHEED to determine when the Zn-terminated surface - c(2x2) - was lost due to Zn desorption. At around 530°C thermocouple temperature and with Zn overpressure, the RHEED changed to a (1x1) reconstruction which suggested that the GaAs layer must be started before this temperature to retain the structural benefits of the Zn-As interface. At temperatures above 450°C, the RHEED pattern changed from a streaky 2x1 with As overpressure to a spotty pattern immediately after opening the Ga shutter, suggesting that the epilayer quality was destroyed by the interface bonds and not the low temperature. The surface reconstruction may shift back to a streaky RHEED pattern after a couple hundred nanometers of GaAs growth if the substrate temperature is low enough to retain a stable ZnSe layer, but quantum well structures require more precise control of the interface to minimize the surface recombination velocity. Even with a few monolayers of GaAs deposited on ZnSe, the GaAs layer needs to be started at or below 450°C to avoid intermixing between the GaAs and ZnSe which completely destroys the material. Structures such as GaAs quantum wells on ZnSe therefore cannot be grown above these temperatures: otherwise, the GaAs and ZnSe layers exchange atoms and form a high defect density in the intermixed layer. Studies are ongoing to determine the optimum substrate temperature for GaAs growth on ZnSe. Other growth conditions, including As deposition temperature and the initial GaAs growth temperature, are currently being investigated to improve the quality of the GaAs epilayer and the ZnSe/GaAs interface.

GaAs/ZnSe quantum wells

GaAs quantum wells confined by ZnSe were grown in the heterovalent MBE chamber under various growth conditions (see Fig. 8). Two main problems exist when growing thin GaAs layers on ZnSe, the first of which is the inability to grow GaAs at the preferred growth temperature since the quantum well layers are too thin to prevent the ZnSe layer from thermally decomposing. The second issue is prevalent for all GaAs/ZnSe heterostructures, since As-terminated surfaces cannot be retained on ZnSe near the ZnSe growth temperature. This causes Ga-Se bonds that destroy the interface quality of the GaAs layer and any subsequent epilayers. Therefore, the substrate must be ramped to lower temperature before As will stick on the ZnSe surface. Thin, high quality GaAs layers on ZnSe were achieved by reducing the substrate temperature to around 125 °C on the thermocouple readout before applying 30 seconds of As flux. This is followed by two monolayers of Ga on top of the As layer, which results in a low-quality film that can be annealed at 400°C under As overpressure to regain a streaky surface reconstruction. Once the GaAs surface reconstruction is obtained, growth of a thin, high quality GaAs layer can be achieved at a substrate temperature of around 440°C.

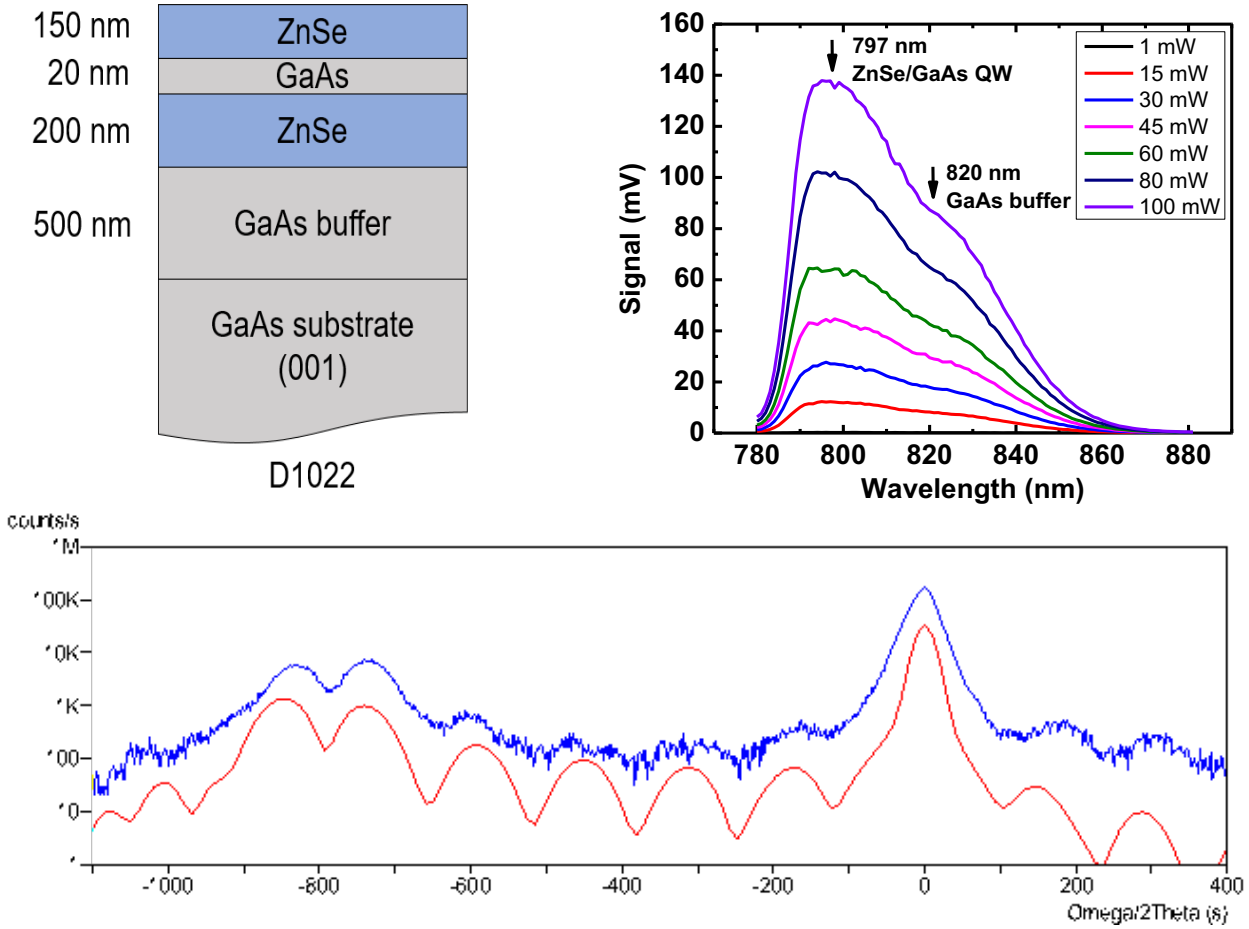


Fig. 8: Growth structure, XRD diffraction pattern, and PL spectrum for GaAs/ZnSe quantum well sample

GaSb/ZnTe quantum wells

GaSb/ZnTe quantum well structures have been grown in our single-chamber MBE system (see Fig. 9). A 20-nm GaSb well was grown between 60-nm ZnTe barriers with a growth temperature of 325°C for the entire structure. The Zn and Te fluxes were calibrated for a flux ratio near unity and the ZnTe barrier layers showed a streaky 2×1 RHEED surface reconstruction. After the first ZnTe layer, a Zn-terminated interface was promoted by leaving the Zn shutter open for 10 seconds after closing the Te valve. Sb was then deposited on the ZnTe surface for 30 seconds before initiating the GaSb growth. The surface reconstruction of the GaSb layer showed a streaky 3×1 pattern about 5 nm into the layer growth. The reverse process was used after the GaSb layer to promote a high quality ZnTe/GaSb interface.

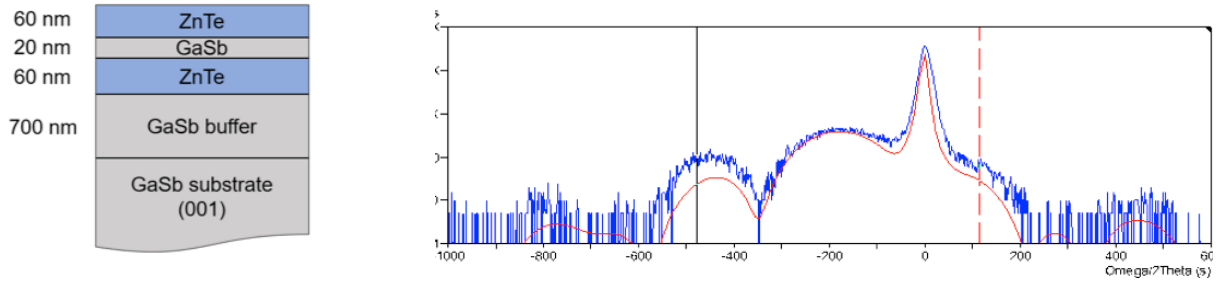


Fig. 9. Growth structure and XRD pattern of GaSb/ZnTe quantum well sample.

Heterovalent superlattices

GaSb/ZnTe and GaAs/ZnSe superlattices have been grown with the single-chamber MBE system and optimization of these structures is in progress. A 5-nm/5-nm GaSb/ZnTe superlattice with 50 periods was grown using similar growth conditions as the quantum well sample (see Fig. 10). For the superlattice, the Sb deposition time was changed to 30 seconds. The substrate temperature was 325 °C for both the GaSb and ZnTe layers throughout the superlattice growth.

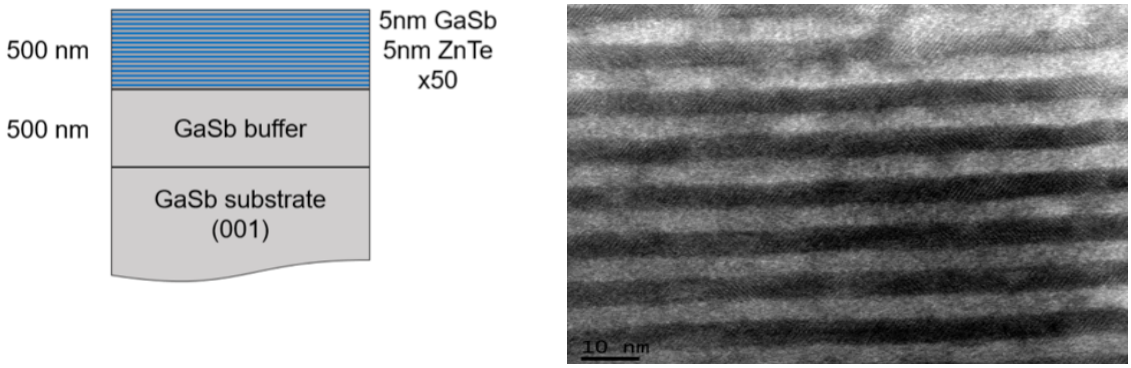


Fig. 10. Growth structure and TEM image of GaSb/ZnTe superlattice. Interfaces are flat but some defects are present due to low growth temperature and sub-optimal growth conditions.

For the GaAs/ZnSe superlattice, the substrate temperature was not ramped down for the As deposition in the preliminary studies. A 4-nm/4-nm GaAs/ZnSe superlattice with 50 periods was grown at a substrate temperature of approximately 280°C for both the GaAs and the ZnSe layers (see Fig. 11). Both the As and the Se cracker cell valves were left open for the duration of the growth since the chamber does not yet have automated valve controllers. The ZnSe layers were initiated with 10 seconds of Zn flux before opening the Se shutter to initiate the ZnSe growth. The surface reconstruction of the ZnSe layers showed a streaky 2x1 up until the 50th layer. For the GaAs layers, As was deposited on the Zn-terminated ZnSe surface for 10 seconds before opening the Ga shutter to initiate the GaAs growth. The surface reconstruction of the GaAs layers turned spotty immediately and never recovered, suggesting that not enough As was present on the ZnSe surface before the Ga flux was introduced. This could be mitigated by using the low temperature anneal process used for the GaAs/ZnSe quantum well structures, but this would significantly increase the superlattice growth time and more calibrations would need to be completed before an automated growth program could be devised. No PL signal from this preliminary superlattice sample was observed, most likely due to the interface conditions of the GaAs/ZnSe heterojunction. Efforts to improve the interface focused on increasing the As sticking coefficient on the ZnSe surface.

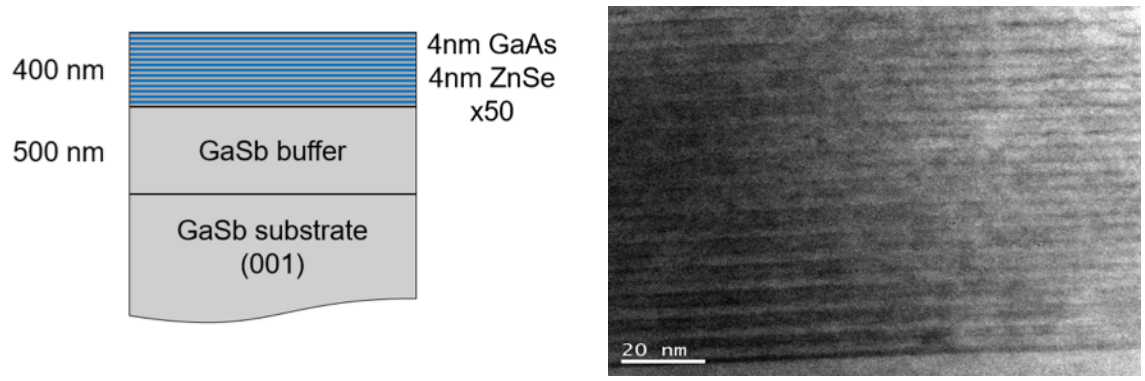
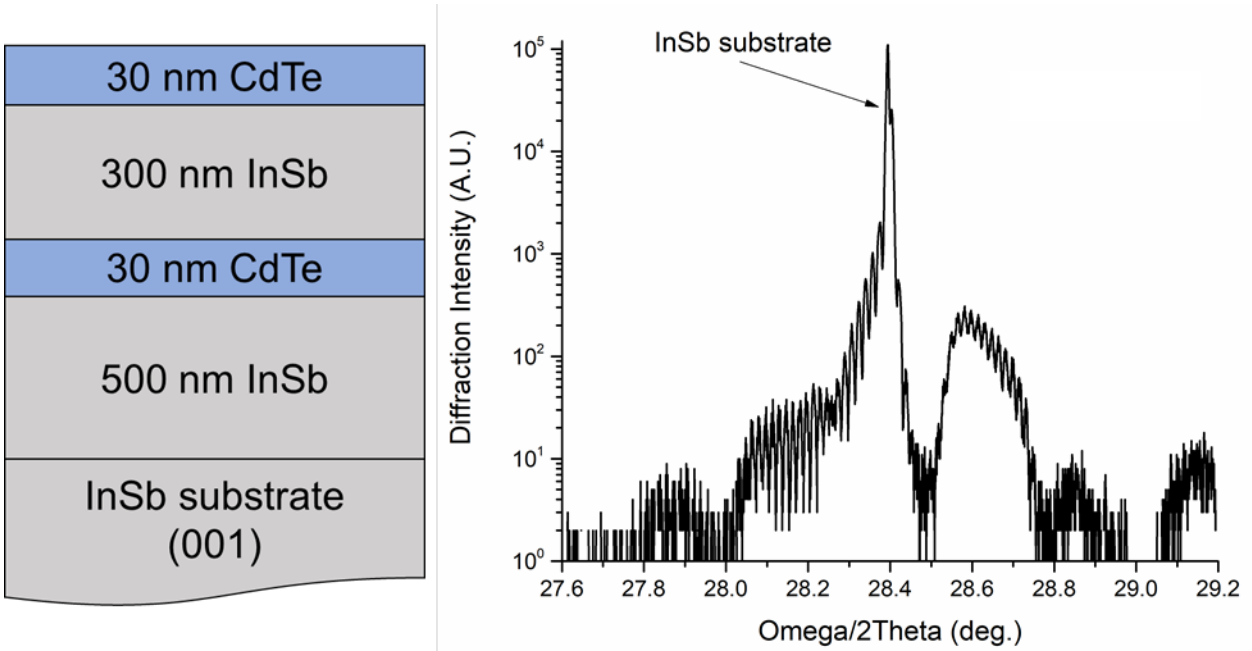


Fig. 11: Growth structure and TEM image of GaAs/ZnSe superlattice. Interfaces are straight but the uniformity still needed to be improved.

InSb/CdTe heterostructures

While CdTe and InSb have dramatically different optical and electrical characteristics, such as the energy band gap, refractive index, and electrical conductivity, the crystal structures are almost perfectly lattice matched, with only a 0.046 % mismatch between the two lattice constants. Additionally, unlike the previous cases of GaSb/ZnTe and GaAs/ZnSe, the optimal growth temperatures of the two materials are relatively close, which simplifies the growth of InSb on CdTe. Unfortunately, this material combination also has its drawbacks, such as unwanted doping due to the high amount of In diffusion into the CdTe layers. Various growth conditions were tested to achieve sharp interfaces and optical emission from the InSb layers. Double heterostructures, quantum wells, and superlattices were grown on nonpolar (100) and polar (211) oriented InSb substrates to investigate the effect of the interface bonding on the heterostructure characteristics. As was done previously for the other heterovalent material combinations, II-V bonding was promoted by applying elemental fluxes of Cd or Sb between the CdTe and InSb layers to achieve coherent epilayers and avoid interfacial compounds caused by III-VI bonding at the interface. Initially, an InSb/CdTe double heterostructure was grown to determine the optimal InSb growth conditions without causing significant interdiffusion between the CdTe and InSb layers. A growth temperature ramp from 280 to 300 °C was found to be sufficient to achieve high-quality InSb epilayers on CdTe without causing significant diffusion between the two materials. The growth structure and XRD pattern are shown in Figure 12, it is evident from the Pendellösung fringes in the diffraction pattern that the interfaces between the CdTe and InSb layers are sharp and well-



defined.

Fig. 12: Growth schematic and XRD pattern of the InSb/CdTe double heterostructure.

In addition to the double heterostructure growths, InSb/CdTe quantum wells and superlattices were also grown using similar growth conditions to the optimized double heterostructure conditions. For the thin InSb layers, migration-enhanced epitaxy was used to improve the adatom diffusion length at lower temperatures without a temperature ramp. Instead of the typical (3x1) surface reconstruction for InSb, the superlattice layers showed a (4x1) reconstruction during growth as determined by RHEED. XRD measurements, seen in figure 13, show that the interfaces of the quantum wells and superlattices are not as well-defined as the double heterostructure interfaces, most likely due to the reduced growth temperature and the interface flux conditions. Different growth temperatures, flux conditions, interface termination, and layer thickness were tested to examine how they affect the structural quality, the peak emission energy of the heterostructures. Strong photoluminescence signals were observed from many of the superlattice samples, with emission peaks blueshifted with respect to the bulk InSb band gap energy. Figure 14 shows power-dependent PL measurements of an InSb/CdTe superlattice sample, which confirm that the high energy peaks in the superlattices are not due to band filling in the InSb due to unintentional doping, as the peak energy shows no shift as the pump power is varied over two orders of magnitude. Optical emission from one superlattice sample, shown in Figure 15, is observed up to temperatures of 130 K, with a peak energy shift of approximately 20 meV over a temperature range of 100 K. Continuing improvements to the superlattice growth conditions have significantly enhanced the PL emission strength, but the physical origin of the high energy emission has not been completely determined yet.

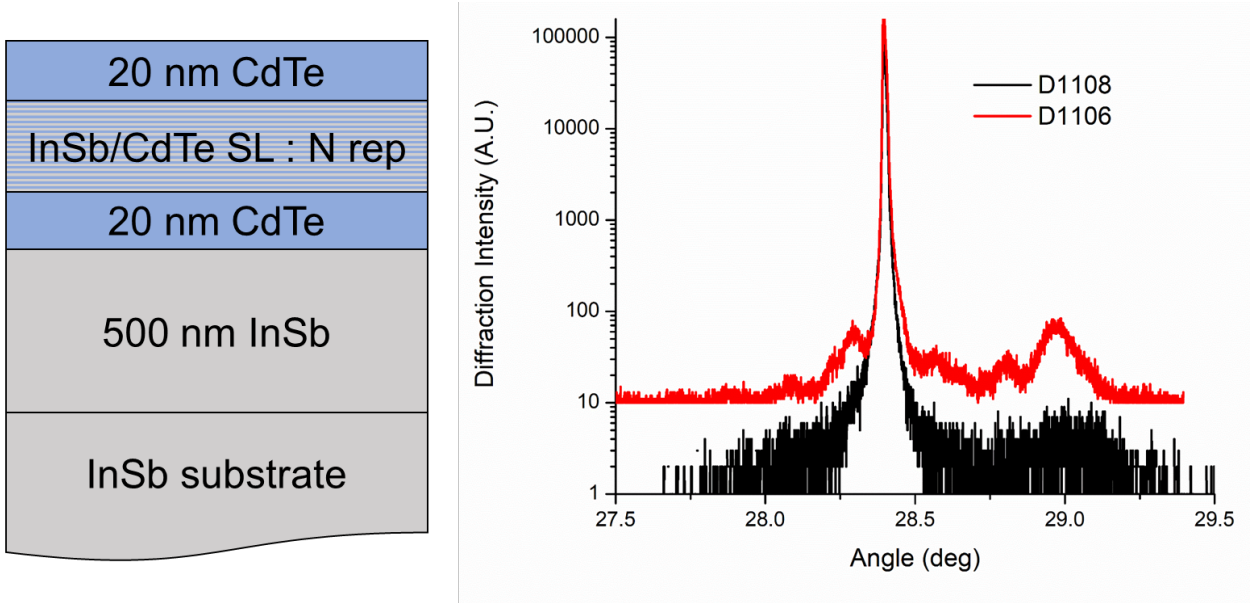


Fig. 13: Growth schematic and XRD pattern of the InSb/CdTe superlattice samples. The sample with the red curve (D1106) has 15 alternating periods of 1.2 nm InSb and 3 nm CdTe, while the sample with the black curve (D1108) has 10 alternating periods of 1.8 nm InSb and 3 nm CdTe.

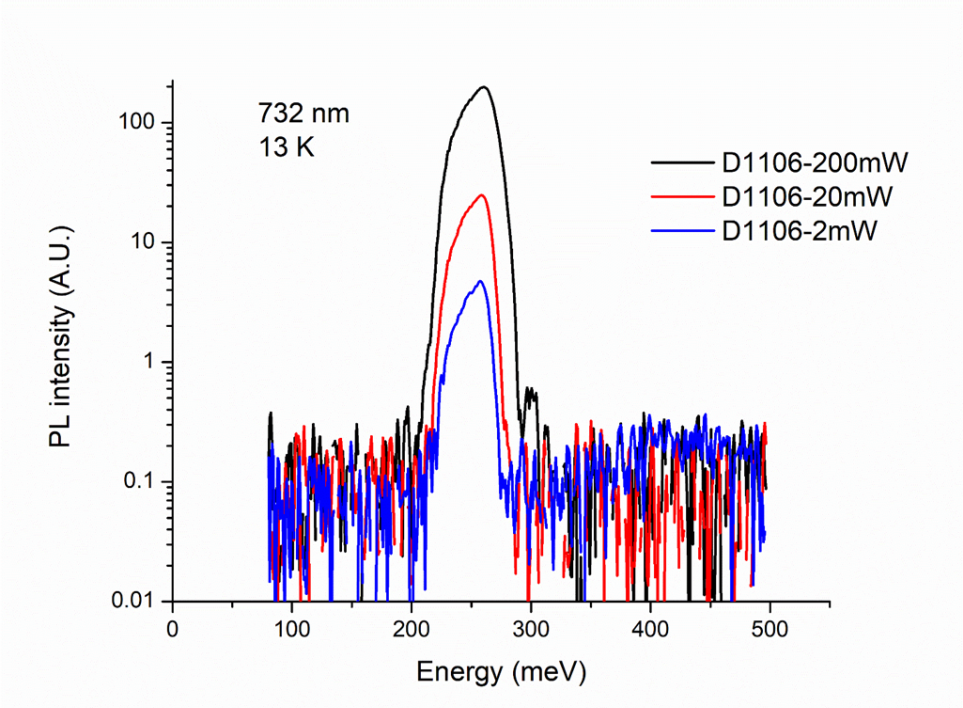


Fig. 14: Power dependent PL measurements for an InSb/CdTe superlattice showing a constant emission peak, which suggests that the high energy peak is not caused by band filling due to high doping levels in the InSb.

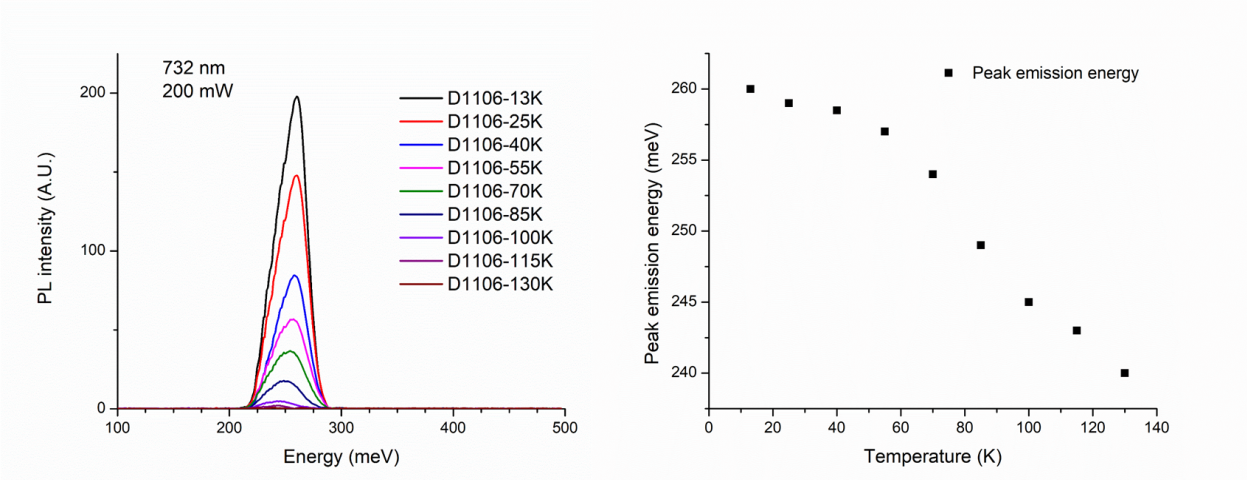


Fig. 15: Temperature dependent PL measurements show that as the temperature increases past about 40 K, the peak emission energy drops at a rate of approximately 0.2 meV/K.

3. Integration of IV-VI materials with lattice-matched III-V/II-VI heterostructures

Although Pb-containing IV-VI materials typically form rock salt crystals, they can still be integrated into heterostructures with lattice-matched zinc blende materials such as InSb or GaSb. These rock salt materials are of interest for several reasons, including their infrared band gap that can be tuned depending on the material stoichiometry which can help in expanding the available material properties available for a given lattice constant. Additionally, the IV-VI materials have significantly lower Auger coefficients than the III-V or II-VI materials, which could be utilized to enhance infrared laser technology. The IV-VI materials, when integrated with the more established zinc blende compound semiconductors, can add additional degrees of freedom for the selection of material parameters for a given lattice constant. PbSe and PbTe were grown on GaSb and InSb substrates, respectively.

The structural quality of the IV-VI crystals was significantly impacted by the material on which it is deposited, and therefore buffer layers consisting of different lattice-matched III-V and II-VI materials were tested. Growth of these materials were investigated on both polar and nonpolar substrates to examine the interface bonding structure and the crystal structure shift for the various surface orientations. Buffer layers consisting of II-VI materials consistently showed higher quality IV-VI crystals compared to III-V buffer layers, most likely due to the presence of a common group-VI atom at the interface between the IV-VI and II-VI materials. The surface reconstruction during PbTe growth on the (100)-oriented CdTe buffers became slightly spotty and remained as so throughout the growth of the entire layer, but during the growth of the CdTe cap layer the reconstruction shifted to a streaky (1x1) pattern instead of the expected c(2x2) or (2x1) pattern commonly exhibited during CdTe growth. For growth on (211)-oriented substrates, the surface reconstruction shifts from inclined streaks to a streaky (3x1) pattern for a short period, which suggests a shift in the growth mode near the interface. This pattern lasts for only a few nanometers of PbTe growth before shifting to a pattern similar to that seen in the (100) PbTe growth. Although the IV-VI crystals have a significantly higher thermal expansion coefficient than their lattice-matched zinc blende counterparts, no propagating defects due to the thermal mismatch were observed in the IV-VI layers, as seen in Figure 16. While the growth of the IV-VI materials on II-VI buffer layers was relatively robust, determining the optimal conditions for high-quality II-VI capping layers on the IV-VI crystals requires careful tuning of the interface configurations. Preliminary TEM images show that while the first II-VI buffer layer and the subsequent IV-VI layer are nearly defect-free, the top II-VI layer is riddled with defects propagating from the interface. The reduced cap quality significantly increases the parasitic recombination, and further enhancements to the growth of II-VI layers on IV-VI materials is required before any in-depth PL studies can be completed.

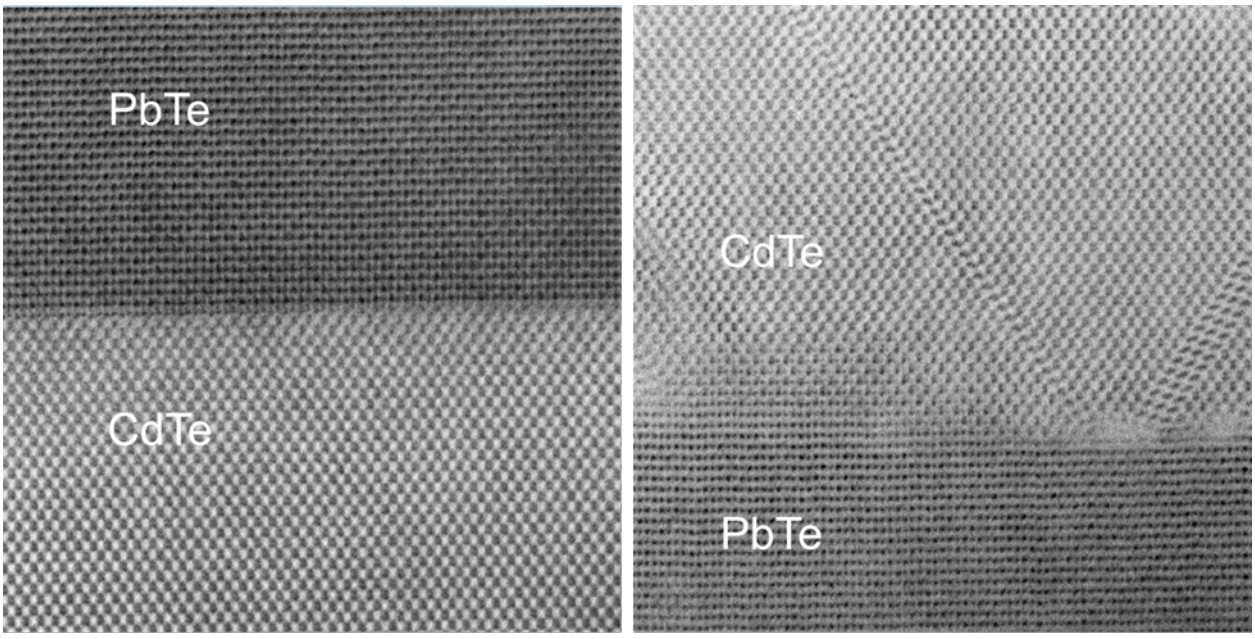


Fig. 16: TEM images from a single PbTe/CdTe double heterostructure sample showing the sharp, defect-free bottom PbTe/CdTe interface (left), and the top CdTe cap with defects propagating from the uneven CdTe/PbTe interface.

XRD patterns of the IV-VI heterostructures vary significantly depending on the type of buffer layer material. For the case of PbTe on InSb substrates, a thin CdTe film appears to be an adequate buffer layer for the transition from zinc blende to the IV-VI rock salt crystal structure, whereas PbTe grown directly on InSb shows no evidence of forming a single crystal layer. Since PbTe and CdTe share a common Te atom in their lattices, Te-terminated PbTe/CdTe interfaces were first tested by applying an elemental Te overpressure between the deposition of the CdTe and PbTe layers. This results in a high quality PbTe layer on CdTe, but the Te-terminated interface destroys the CdTe cap layer grown on the PbTe. In addition to the interface termination, the substrate orientation and growth temperature will also play a role in the epilayer quality, and a comprehensive study of the interface conditions between PbTe and CdTe is underway.

PbSe layers were grown on GaSb substrates with a variety of different buffer layers and growth conditions. The lattice constant of GaSb enables both ZnTe and CdSe to be used as nearly lattice-matched buffer layers, but the quality of the PbSe grown on these two materials differs significantly, as demonstrated in figure 17. Although ZnTe is more closely lattice matched to PbSe, the quality of the PbSe layers grown on ZnTe buffers are much more difficult to grow due to the lack of common atoms at the interface. The surface reconstruction during PbSe growth became diffuse with rings, which suggests the loss of coherent crystal growth. For the PbSe/CdSe growth, the reconstruction showed a characteristic shift from a streaky zinc blende reconstruction to a slightly spotty pattern commonly seen during growth of rock salt materials on (100)-oriented substrates. The pattern shifted back to a streaky pattern during the growth of the CdSe cap layer,

suggesting a coherent zinc blende/rock salt heterostructure. XRD measurements of PbSe/ZnTe quantum wells on GaSb substrates only show a slight shoulder and weak peripheral fringes, whereas the structures with CdSe buffer layers show clear PbSe features in the diffraction pattern, and some samples even have faint Pendellösung fringes indicative of sharp, high-quality interfaces. Similar to the PbTe growths, no PL signal has been observed yet from the PbSe structures.

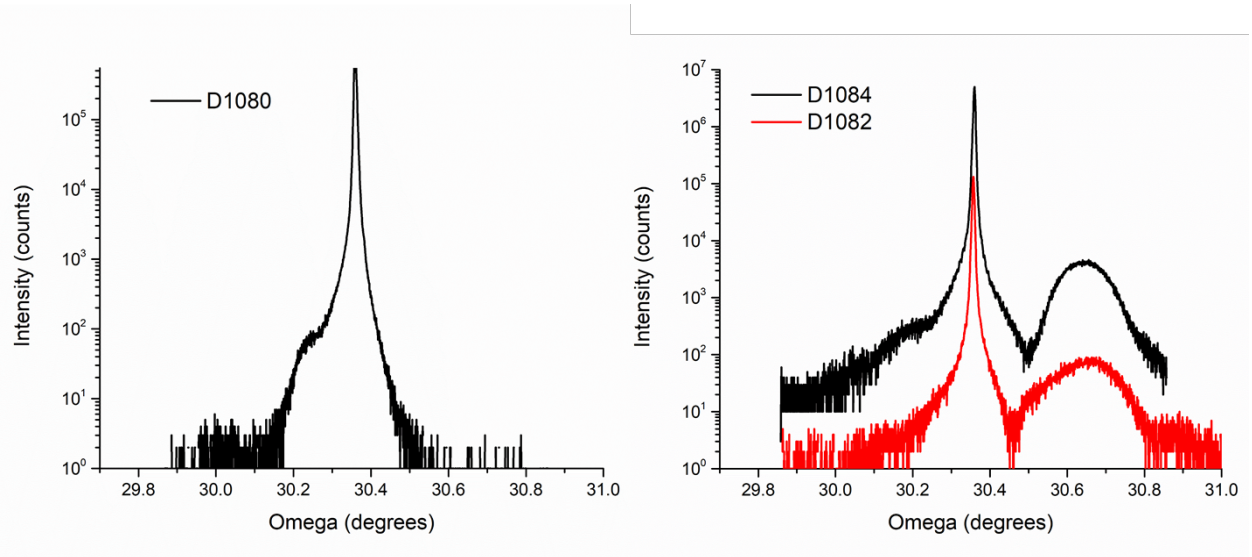


Fig. 17: XRD patterns for PbSe grown on GaSb substrates with a ZnTe buffer layer (left), and a CdSe buffer layer (right).

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2. Xin-Hao Zhao, Shi Liu, Calli M. Campbell, Maxwell B. Lassise, Yuan Zhao, Ying-Shen Kuo, and Yong-Hang Zhang, "CdTe/MgCdTe Double Heterostructures with Very Long Minority Carrier Lifetime and Low Interface Recombination Velocity", US II-VI Workshop 2015.
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24. M. B. Lassise, T. T. McCarthy, B. D. Tracy, D. J. Smith, and Y.-H. Zhang, 14th International Conference on Mid-IR Optoelectronics: Materials and Devices, Flagstaff, Oct. 2018.
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Degrees awarded:

Ph.D.: Brian D. Tracy, "Investigating Optoelectronic and Electronic Materials for Next Generation Semiconductor Devices", December 2017.

Ph.D.: Maxwell B. Lassise, "Monolithic Heterovalent Integration of Compound Semiconductors and Their Applications", May 2019.