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**TECHNICAL REPORT**

# **Radiation Effects in III-V MOSFETs for sub-10 nm CMOS**

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## REPORT DOCUMENTATION PAGE

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**Subaward PI: Ronald D. Schrimpf**

**Final Report**

**March 20, 2020**

## **Objectives**

This research program aims to study radiation effects in InGaAs- and InGaSb-based MOSFETs for future CMOS technology insertion and to investigate appropriate parametric sensitivity that will be useful in the event that mitigation strategies are required in the future. The goal is to develop basic understanding of the physical phenomena involved by building appropriately tailored test structures and devices and testing them under a variety of radiation conditions that include X-rays, protons, heavy ions, and alpha particles. Emphasis will be given to dielectrics and semiconductor structures and geometries of relevance to sub-10 nm CMOS nodes, namely Tri-gate designs.

The program has three major thrusts:

1. Device prototyping of InGaAs-based n-channel and InGaSb p-channel MOSFETs
2. Radiation studies on III-V MOSFETs and test structures
3. Device modeling

## **Accomplishments**

We report our accomplishments along the three major thrusts of this program and by year:

### 1. Device prototyping of InGaAs-based n-channel and InGaSb p-channel MOSFETs

#### **2015**

In this period of performance we fabricated deeply scaled self-aligned InGaAs planar MOSFETs and carried out several fundamental device physics experiments of relevance to this program.

On the one hand, we studied the excess off-state leakage current observed in self-aligned InGaAs MOSFETs fabricated by a tight pitch process. We identified band-to-band tunneling (BTBT) as the triggering mechanism for this excess current but we also found that this current is amplified many times over by a parasitic floating-base bipolar transistor formed by the source-body-drain structure of the device. This is relevant to this program because the identified amplification mechanism should also be in action during radiation events enhancing the magnitude of the upset and lengthening the recovery of the device.

We have also carried out a detailed gate length and channel thickness scaling study of InGaAs MOSFETs in terms of transport and short-channel effects. We find classic MOSFET scaling behavior that indicates that InGaAs MOSFET structures are at the limit of scaling at a gate length of ~50 nm. This is important

for this program because it strongly suggests that future sub-10 nm III-V MOSFET structures will be of a multigate (trigate or nanowire) architecture.

We have started efforts to demonstrate InGaAs FinFET and Trigate MOSFETs as well as planar InGaSb MOSFETs and test structures. We have succeeded in fabricating InGaAs FinFETs with sub-10 nm fin widths but not Trigate MOSFETs. At the same time, we have succeeded in fabricating InGaSb planar MOSFETs and FinFETs but they suffer from excessive buffer leakage. Efforts will continue along these two fronts so that we can soon deliver working devices to the Vanderbilt group.

In this period of performance, the MIT team as sent several sets of planar InGaAs MOSFETs with different design and geometries to Vanderbilt for radiation testing.

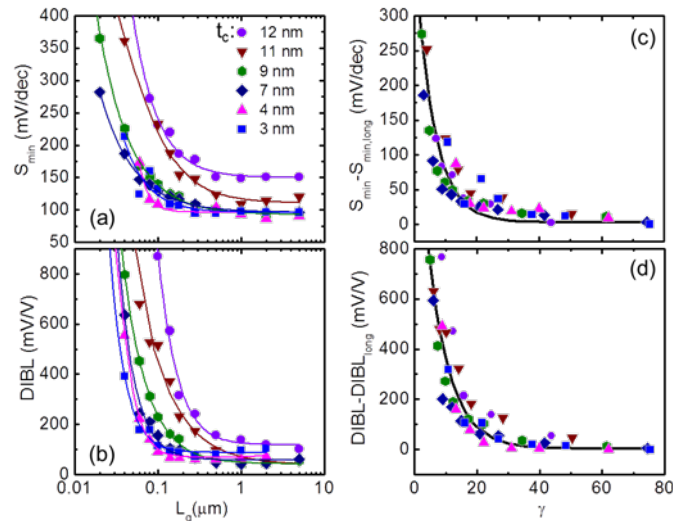


Figure 1: (a, b) Experimental  $S_{min}$  and DIBL as a function of gate length for  $t_c = 3$  nm to 12 nm channel thickness InGaAs planar MOSFETs. (c, d)  $S_{min} - S_{min, long}$  and  $DIBL - DIBL_{long}$  as a function of “natural channel length”.

## 2016

In this period of performance, there was very significant progress in the prototyping of InGaAs-based n-channel planar quantum-well MOSFETs and FinFETs, as well as InGaSb p-channel FinFETs.

In planar InGaAs QW-MOSFETs, we carried out a channel thickness and gate length scaling study that has indicated the limits of scaling of these devices. While worthwhile for the purpose of understanding physics, these devices do not scale to the required dimensions and are not contenders for deployment. In addition, a scaling study of the ohmic contacts has also been carried out. This work has shown that while Mo contacts offer for the moment leading performance on n+-InGaAs, the contact resistivity is still too high and further progress is required. Our device physics insights, particularly the role of the extrinsic source and drain, has resulted in a new device design that has delivered a record transconductance among all InGaAs FETs of any kind. Some of these devices have been delivered to Vanderbilt for radiation experiments.

We have also demonstrated the first sub-10 nm fin-width InGaAs double-gate FinFETs with a channel aspect ratio in excess of 5. This has been accomplished through precision dry etching and digital etch. Our devices exhibit a record transconductance when normalized by the fin width, as is relevant for density. In addition, we have carried out a sensitivity study of the threshold voltage of InGaAs double-

gate FinFETs to the fin width. We find that VT becomes very sensitive to Wf in the sub-10 fin width range. This is due to prominent quantum effects as a result of the low effective mass of electrons in InGaAs. Some of these devices have been delivered to Vanderbilt for radiation experiments.

We have also demonstrated the first InGaSb p-type FinFETs. For this, we developed Si-compatible ohmic contacts and precision dry etching. Fins with aspect ratio as high as 10 with low interface state density were demonstrated. FinFETs with gate lengths as short as 100 nm were obtained.

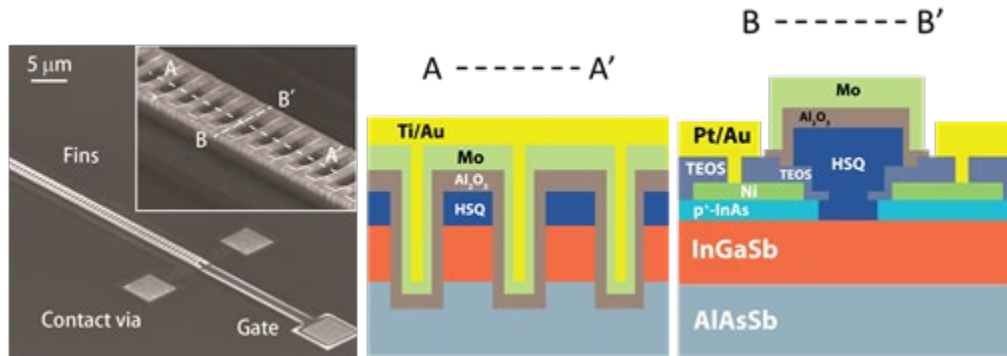


Figure 2: (a) SEM image of an InGaSb FinFET before final pad deposition. Inset: zoom-in of the gate region. Device cross-sectional structure along (b) A-A' and (c) B-B' directions.

## 2017

In this period of performance, there was significant progress in the prototyping of InGaAs-based n-channel planar quantum-well MOSFETs and FinFETs, as well as InGaSb p-channel FinFETs.

We have reported, for the first time, a prominent but fully reversible enhancement in transconductance after applying positive gate stress to self-aligned InGaAs MOSFETs. We attribute this to electric-field-induced migration of fluorine ions (F-) introduced during the RIE gate recess process. F- is known to passivate Si donors in InAlAs. In our device structure, an n-InAlAs ledge facilitates the link from the contacts to the intrinsic device. We use secondary ion mass spectroscopy (SIMS) to independently confirm that our process leads to F pile up at the n-InAlAs layer. Transmission line model (TLM) structures confirm F--induced donor passivation. The understanding derived has led us to redesign our InGaAs MOSFETs by eliminating n-InAlAs layers and instead use an n-InP ledge. The new device design not only exhibits greatly improved electrical stability but also record performance.

We have studied the scaling properties of self-aligned InGaAs FinFETs with sub-10-nm fin widths fabricated through a CMOS compatible front-end process. Working devices with fins as narrow as 7 nm, fin aspect ratios in excess of 5, and gate lengths as short as 20 nm have been fabricated using precision dry etching and digital etch. The devices feature self-aligned metal contacts that are 20–30 nm away from the edge of the gate. FinFETs with  $L_g = 30$  nm,  $W_f = 7$  nm, and channel height of 40 nm exhibit a transconductance of  $900 \mu\text{S}/\mu\text{m}$  at  $V_{DS} = 0.5$  V. When normalized to  $W_f$ , this is a record value among all III–V FinFETs, indicating that our device architecture makes efficient use of conduction along the fin sidewalls.

We have also developed a second generation InGaSb p-channel FinFETs featuring fin width as narrow as 18 nm and gate lengths down to 20 nm with record electrical performance. A device with 18 nm fin width and 20 nm gate length shows well saturated characteristics with a peak transconductance of 186

$\mu\text{S}/\mu\text{m}$  at  $V_{\text{DS}} = -0.5\text{ V}$  and a minimum subthreshold swing of  $370\text{ mV}/\text{dec}$  at  $V_{\text{DS}} = -50\text{ mV}$ . Our best device exhibits a peak transconductance of  $338\text{ }\mu\text{S}/\mu\text{m}$ . This is a record among GaSb or InGaSb p-channel planar or fin MOSFETs, and nearly triples the previous record. We also observe the presence of leakage paths in the device, such as undesired conduction within the fin buffer and at the buffer surface. This prevents effective transistor turn off and remains one of the major challenges in InGaSb FinFET fabrication.

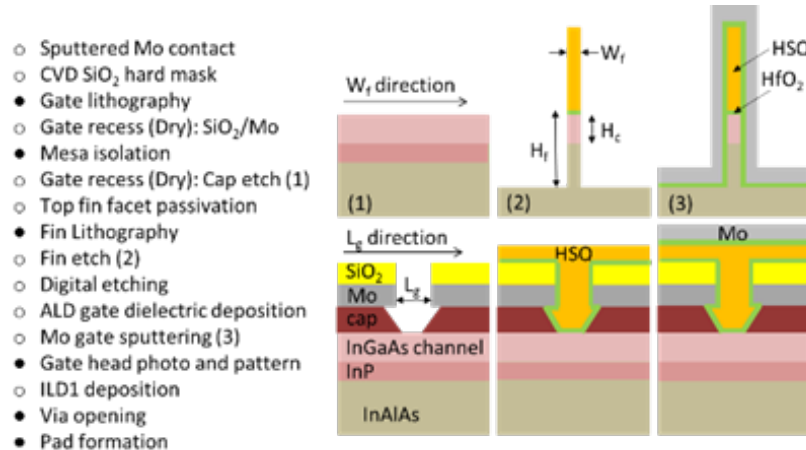


Figure 3: Sketch or process flow for sub-10 nm InGaAs FinFET fabrication.

## 2018

In this period of performance, there was significant progress in the prototyping of InGaAs-based n-channel FinFETs, as well as InGaSb p-channel FinFETs. Key developments are summarized next.

We have developed a scalable gate-last process to fabricate self-aligned InGaAs FinFETs that relies on extensive use of dry etch. The process involves F-based dry etching of refractory metal ohmic contacts that are formed early in the process. The fins are etched in a novel inductive coupled plasma process using  $\text{BCl}_3/\text{SiCl}_4/\text{Ar}$ . High aspect ratio fins with smooth sidewalls are obtained. To further improve the quality of the sidewalls and shrink the fin width, digital etch is used. Through this process flow, we have demonstrated FinFETs with  $L_g=20\text{ nm}$  and fin width as narrow as  $7\text{ nm}$  with high yield. Good electrostatic characteristics are obtained in a wide range of device dimensions. In devices with  $7\text{ nm}$  fin width, record channel aspect ratio, and transconductance per unit footprint are obtained.

We have further demonstrated self-aligned InGaAs FinFETs with fin widths down to  $5\text{ nm}$  fabricated through an improved CMOS compatible front-end process. Precision dry etching of the recess cap results in metal contacts that are about  $5\text{ nm}$  away from the intrinsic portion of the fin. The new process has allowed us to fabricate devices with undoped fins and compare them with delta-doped fins. We find that in highly scaled transistors, undoped fin devices show better OFF-state and a tighter VT distribution but similar ON-state characteristics, as compared with  $\delta$ -doped-fin transistors. 2D Poisson-Schrodinger simulations reveal undoped fins making more effective use of the fin height.

We have carried out a detailed study of the off-state leakage current in scaled self-aligned InGaAs FinFETs. In long-channel devices, band-to-band tunneling at the drain-end of the channel is shown to be the root cause of excessive off-state current. This conclusion emerges from its characteristic electric field and temperature behavior and the absence of gate length and fin width dependencies. In short-channel devices, off-state current is significantly larger and it increases as the gate length shortens or

the fin widens. We attribute this behavior to current multiplication through the gain of a floating-base parasitic bipolar transistor that is present inside the MOSFET. We extract the bipolar current gain which in short-channel devices is found to increase as the gate length shortens and decrease as the fin width narrows. In long channel devices, the current gain drops exponentially due to base recombination. This understanding has allowed us to extract the diffusion length of electrons in the body of the transistor.

We have also fabricated self-aligned InGaSb p-channel FinFETs using a novel antimonide-compatible digital etch. This is the first demonstration of digital etch on InGaSb-based transistors of any kind. It has enabled the first fabricated InGaSb FinFETs featuring fin widths down to 10 nm and gate lengths of 20 nm. Single fin transistors with  $W_f = 10$  nm and channel height of 23 nm (fin aspect ratio of 2.3) have achieved a record transconductance of  $160 \mu\text{S}/\mu\text{m}$  at  $V_{\text{DS}} = 0.5$  V. When normalized to device footprint, the devices deliver a record high  $g_m = 704 \mu\text{S}/\mu\text{m}$ . Digital etch has been shown to effectively improve the turn-off characteristics of the devices.

Our latest InGaSb FinFET results have been enabled by a novel alcohol-based digital etch technique for III-V FinFET and nanowire MOSFET fabrication that we have developed. The new technique addresses the limitations of the conventional water-based approach in realizing structures with sub-10-nm 3-D features. Using the same oxidation step, the new technique shows an etch rate of 1 nm/cycle, identical to the conventional approach. Sub-10 nm fins and nanowires with a high mechanical yield have been achieved. InGaAs nanowires with a diameter of 5 nm and an aspect ratio greater than 40 have been demonstrated. The new technique has also been successfully applied to InGaSb-based heterostructures, the first demonstration of digital etch in this material system. Vertical InGaAs nanowire gate-all-around MOSFETs with a subthreshold swing of 70 mV/decade at  $V_{\text{DS}} = 50$  mV have been obtained at a nanowire diameter of 40 nm, demonstrating the good interfacial quality that the new technique provides.

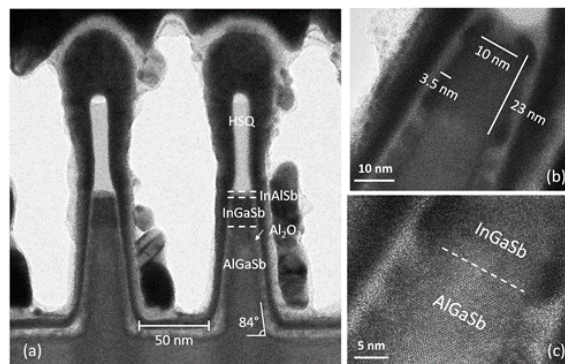


Figure 4: HR-TEM images of finished InGaSb FinFET with fin width of 10 nm, fin aspect ratio of 2.3, and 3.5 nm Al<sub>2</sub>O<sub>3</sub> gate dielectric.

## 2019

In this period of performance, there was significant progress in the prototyping of InGaAs-based n-channel FinFETs and in the understanding of the role of oxide trapping in device behavior. Key developments are summarized next.

For the first time, thermal atomic layer etching (ALE) on InGaAs-based III-V heterostructures is demonstrated. Also, we report the first transistors fabricated by the thermal ALE technique in any semiconductor system. We further highlight one unique advantage of thermal ALE: its integration with atomic layer deposition (ALD) in a single vacuum chamber. Using in situ ALE-ALD, we have fabricated the

most aggressively scaled self-aligned In<sub>0.53</sub>Ga<sub>0.47</sub>As n-channel FinFETs to date, featuring sub-5 nm fin widths. The narrowest FinFET with  $W_f = 2.5$  nm and  $L_g = 60$  nm shows  $g_m = 0.85$  mS/ $\mu$ m at  $V_{ds} = 0.5$  V. Devices with  $W_f = 18$  nm and  $L_g = 60$  nm demonstrate  $g_m = 1.9$  mS/ $\mu$ m at  $V_{ds} = 0.5$  V. Subthreshold swings averaging  $S_{lin} = 70$  mV/dec and  $S_{sat} = 74$  mV/dec across the entire range of  $W_f$ , at minimum  $L_g = 60$  nm have been obtained. These are all record results. The transistors demonstrated here show an average 60%  $g_m$  improvement over devices fabricated through conventional techniques. These results suggest a very high-quality MOS interface obtained by the in situ ALE-ALD process.

We have also studied the performance degradation of InGaAs FinFETs as they scale to sub-10 nm fin width. This is often attributed to degradation in intrinsic transport parameters. High frequency measurements, however, indicate increasingly severe oxide trapping as the fin width narrows. This is confirmed by pulsed-IV measurements. A new mobility extraction method using concurrent S-parameter and DC-IV measurements avoids the impact of oxide trapping and reveals promising mobility in thin-channel InGaAs planar MOSFETs and narrow-width FinFETs. Our study suggests that performance degradation of InGaAs FinFETs is largely an extrinsic phenomenon that can be engineered around and that the potential performance of deeply-scaled InGaAs FinFETs is significantly underestimated.

We have studied the impact of fin-width scaling on transport in highly doped InGaAs fins and the effect of digital etch (DE). Our experiments suggest the existence of a 10-nm-wide “deadzone” on each side of the fin that does not contribute to transport. The extent of the deadzone cannot be mitigated by DE nor sidewall passivation. Simulations suggest that the Fermi-level pinning and its associated subsurface depletion region alone cannot explain the relatively wide deadzone that is measured. We propose an explanation based on the combination of Fermi-level pinning and mobility degradation as the fin width scales down. This leads to an apparent wider deadzone than accounted by the Fermi-level pinning alone.

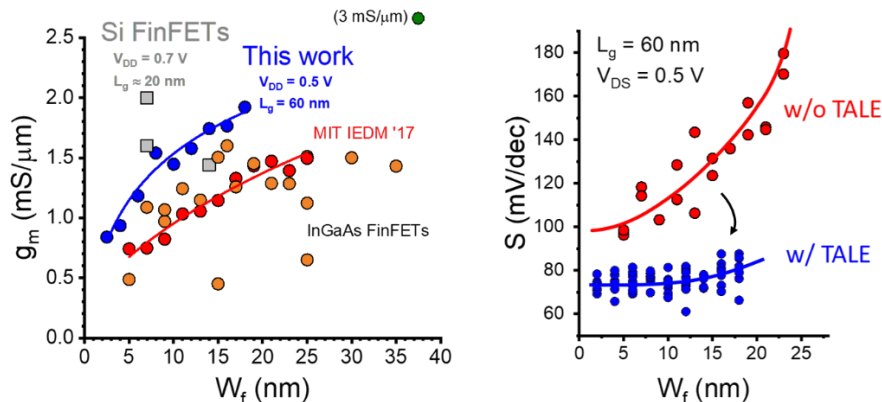


Figure 5: Transconductance (left) and subthreshold swing (right) of InGaAs FinFETs fabricated by conventional technique (red) and the new integrated ALE-ALD technique. A remarkable enhancement in ON- and OFF-state characteristics is demonstrated.

## 2. Radiation studies on III-V MOSFETs and test structures

### 2015

Radiation testing was performed using 10 keV x-ray exposure for TID studies, and laser and heavy ion (10 MeV oxygen) exposures for single event transient studies all using radiation sources at Vanderbilt. The experimental details, results, and analyses of mechanism are detailed in the presentations and publications listed for the 2014 and 2015 IEEE NSREC and associated IEEE TNS papers (one published and another to be submitted in early July prior to the 2015 IEEE NSREC). 2D device TCAD studies are included

as part of the single event analyses. Additional heavy-ion experiments were carried out in June 2015 at LBNL. Two devices were tested using four different ions: Ne, Ar, Kr, and Xe. The data are currently being processed for subsequent analyses and presentation.

Presently, we are constructing 3D device models to use in Monte Carlo energy deposition (MRED) simulations and TCAD device simulations to better understand the observed single-event response, particularly the long temporal tail in the response. The baseline MRED model is 95% done and is based upon the device layout and structural information from MIT. The solid model definition is complete, materials models are incorporated, and key properties (density, band gaps and mean ionization energies) have been estimated. The appropriate physics models have been set up, and the post processing software is complete. Initial simulations are underway using the 10 MeV oxygen ions for which we have experimental data. Results from the MRED simulations will inform the device response TCAD simulations, which combined will provide single event cross sections for the device.

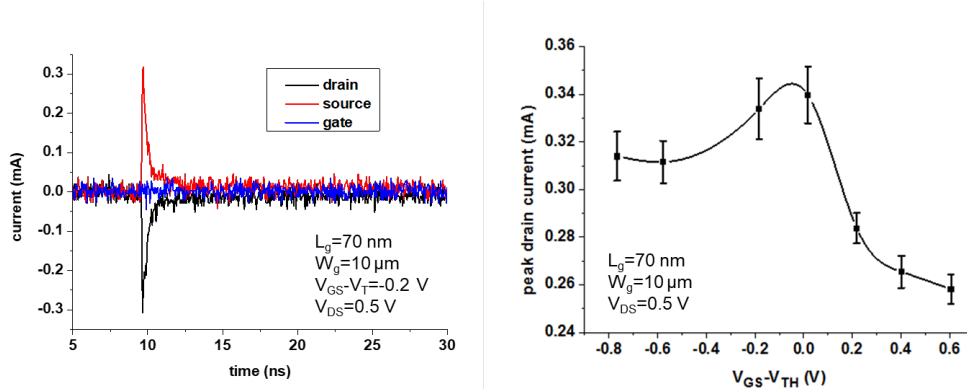


Figure 6: 14.3 MeV oxygen ion response of planar InGaAs MOSFET: temporal response (left); peak drain current response vs. gate bias (right).

## 2016

Radiation testing was performed under 10 keV x-ray irradiation to study TID effect in planar InGaAs quantum-well MOSFETs. Experimental results show that irradiation and electrical stress effects are additive or compensatory to each other, depending on the gate bias applied during irradiation. The electrical stress induced electron trapping compensates radiation induced hole trapping during positive gate biased irradiation. For negative gate biased irradiation, however, the stress induced hole trapping adds together with radiation induced hole trapping. It is further shown that the radiation induced hole trapping is higher under positive gate bias than negative gate bias. Geometry dependence study shows that the radiation induced hole trapping is larger for larger gate length device.

Tunable wavelength laser irradiation has been applied to study single event transients and charge collection mechanisms in InGaAs double-gate FinFETs. A high bandwidth oscilloscope with time resolution of 12.5 ps has been used to capture the ultrafast transients, which enables us to resolve the fast signals, for example, rising edge of transients, which we are not capable of before. Tunable wavelength laser allows us to study the device response to charge injection in a specific region in the device. With these tools, new insights can be obtained. In addition, 3D TCAD model has been built and used to study the charge collection process in the device. From the study, it is shown that there is significant charge enhancement effect due to additional channel current. This is caused by shunting effect and the parasitic bipolar effect due to temporal perturbation in the local potential in the device.

We have also studied the charge sharing between adjacent planar InGaAs quantum-well MOSFETs through pulsed laser irradiation. 3D TCAD model has also been built to study the process in detail. The result shows that the distance, 30  $\mu\text{m}$ , is large enough so that the adjacent devices are well isolated, even in the high injection regime. In the future, devices with shorter and more relevant distance will be studied.

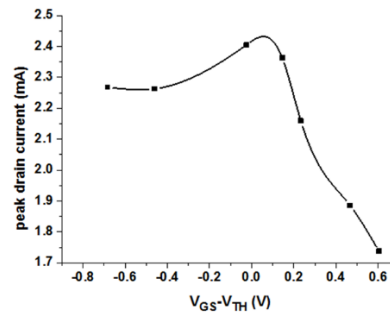


Figure 7: Response of planar InGaAs MOSFET to 1.26  $\mu\text{m}$  laser wavelength exposure. Bias dependence is consistent with heavy ion data.

## 2017

A tunable wavelength laser system and high-resolution transient capture system were developed and applied to characterize transients in high mobility MOSFETs. The experimental configuration enables resolution of fast transient signals and new understanding of charge collection mechanisms. In particular, the system was applied to InGaAs FinFETs. It was found that the channel layer is critical in the charge collection process for these devices. The transient current mainly comes from the channel current, due to shunt effects and parasitic bipolar effects, instead of the junction collection. The charge amplification factor is found to be as high as 14, which makes this technology relatively sensitive to transient radiation. The peak current is inversely proportional to the device gate length. Simulations show that the parasitic bipolar effect is due to source-to-channel barrier lowering caused by hole accumulation in the source and channel. Charge deposited in the channel causes prompt current, while charge deposited below the channel causes delayed and slow current.

The effects of total-ionizing-dose irradiation were investigated in HfO<sub>2</sub>/InGaAs quantum-well MOSFETs. It was found that radiation-induced hole trapping is higher for irradiation under positive gate bias than under negative gate bias. Electrical stress-induced electron trapping compensates radiation-induced hole trapping during positive gate-bias irradiation. Stress-induced hole trapping adds to the effects of radiation-induced hole trapping under negative gate bias. Radiation-induced charge trapping increases with the channel length.

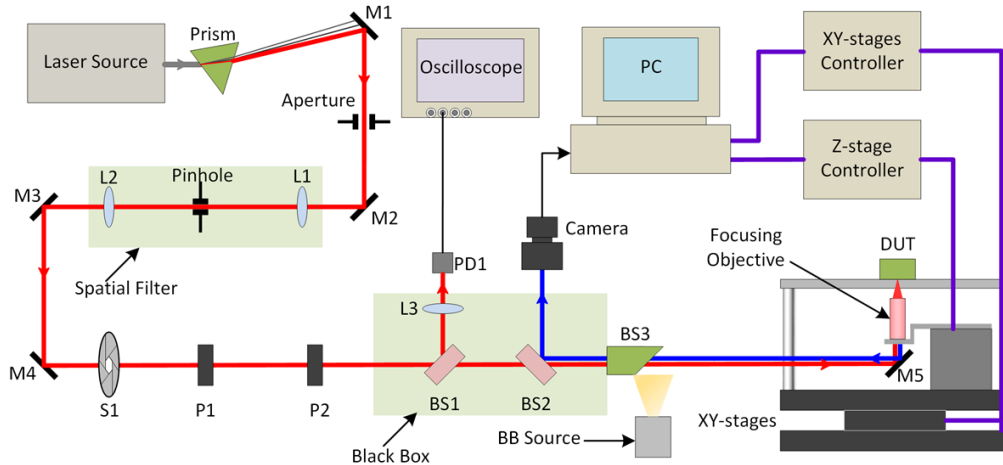


Figure 8: Pulsed tunable wavelength laser system for single-event research at Vanderbilt.

## 2018

We have performed pulsed-laser irradiation of MIT's InGaAs FinFETs at Vanderbilt University. In addition, we have carried out single-event effects simulation of these devices with TCAD. Further, we have also performed optical simulations using Lumerical.

We have investigated the parasitic bipolar amplification effect in the single-event transient (SET) study. In addition, we have explored plasmonic effects in the FinFET structures as well as the SET sensitive area of III-V FinFETs.

We have found that charge collection and SET cross-section in InGaAs FinFETs scale with fin width. 3D TCAD simulations suggest that the enhanced charge collection of wider fin devices is mainly due to larger geometric volumes. Charge accumulated underneath the channel functions as back gate, which also produces stronger channel modulation effects for wider fin devices. Optical simulations show that the optical field is enhanced inside the fin due to the confinement of light associated with the metal-dielectric interface. A tunable pulsed-laser system was used to investigate charge collection mechanisms in quantum-well structures.

We have demonstrated that a high-speed variable wavelength pulsed-laser system is an efficient way to investigate SETs for future CMOS technologies. TCAD simulations were used to understand the charge collection mechanisms. Plasmonic effects were shown to be important for pulsed-laser experiments for most advanced CMOS technologies.

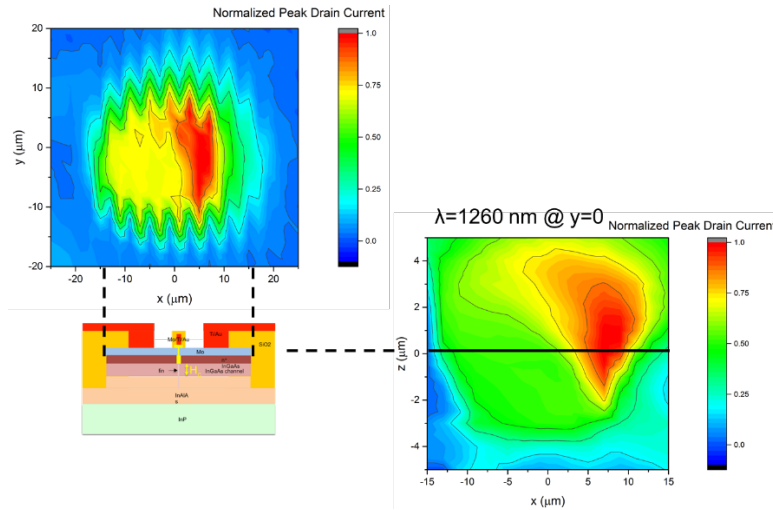


Figure 9: Sensitive volume exploration of InGaAs FinFETs using Vanderbilt's laser system with wavelength of 1260 nm.

2019

In order to further understand single-event charge collection mechanisms and the implications of device scaling, single-photon and two-photon pulsed-laser-induced single-event transient (SET) characterization was performed as a function of fin width and strike location for InGaAs FinFETs. Single- vs. two-photon measurements allow results to be compared for charge generation in the active fins only ( $\lambda = 2200$  nm) with that for charge generated in the entire device structure ( $\lambda = 1260$  nm), with the latter producing  $> 10X$  peak currents. Variation of the incident beam location produce SET pulses with  $\sim 3X$  increase in peak drain current, and  $1.5X-4X$  increase in collected charge, for strikes to the center of the channel compared to source and drain regions.

TCAD simulations indicate that for the case of charge generation throughout the structure, charge builds up under the channel and alters the conduction, including inducing parasitic bipolar enhancement. Comparison of the response across fin widths from 40 nm down to 5 nm show higher peak current response for the wider fins, consistent with larger collection volumes. Overall, the peak SET response was found to be determined by an initial "shunt" from source to drain; the total collected charge, including the tail of the SET pulse, is determined by the parasitic bipolar gain.

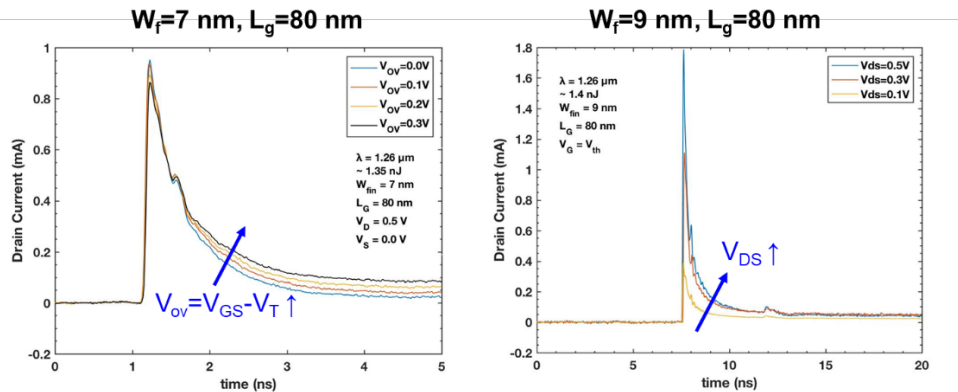


Figure 10: Bias response of photon-induced current in InGaAs FinFETs.

### 3. Device modeling

2015

An improved Virtual Source (VS) model, called MVS-2, was developed that builds upon the original MIT Virtual Source (MVS) model but now uses self-consistent solution of Poisson-Fermi Dirac equations and is therefore surface-potential-based and incorporates the effects of (i) carrier degeneracy on thermal velocity and mean free path of carriers, (ii) drain-bias dependence of gate capacitance and virtual-source charge, and (iii) non-linear channel-access resistance on gm-degradation at high drain currents in the channel. This model has been tested successfully against existing data from InGaAs QW HEMTs. For MOSFETs a significant role in determining the mobile charge at the VS point is played by the spectrum of trap states at or near the interface between the dielectric and the semiconductor. This aspect is not yet included in MVS-2 and is the subject of this project.

It is well known that both the thermal velocity and the mean free path of carriers increase with increase in carrier concentration. While the basic MVS model required an abnormally low effective carrier mass to match the measured drain currents in InGaAs HEMTs, the MVS 2.0 model allows for the virtual source injection velocity of carriers to increase with  $V_{gs}$ , permitting a higher and now realistic effective mass of carriers. Also, in the original MVS model, the VS charge is not influenced by non-equilibrium transport conditions in the channel, and essentially the gate capacitance of the device is assumed independent of the drain bias. This assumption is too simplistic for quasi-ballistic devices where the negative momenta of the VS charge distribution are primarily supplied by the drain contact in near-equilibrium transport ( $V_{ds} \approx 0V$ ) and are missing in non-equilibrium transport (high  $V_{ds}$ ). The VS charge model in MVS 2.0 is improved to capture the effect of non-equilibrium transport. The charge model also includes the quantum-mechanical correction to the gate-channel capacitance due to the finite separation of the charge centroid from the semiconductor-insulator interface. Finally, the non-linearity of channel-access resistances that is responsible for the reduction in the transconductance of the III-V HEMTs for high drain currents has been included in MVS 2.0 by modeling the source and the drain channel-access resistances as non-linear voltage-dependent resistances. Even though the original MVS model has fewer fitting parameters and can also fit the experimental data well, MVS 2.0 captures more completely the essential physics of the nanotransistor in presence of non-equilibrium transport, carrier degeneracy, and access-region non-linearity, and therefore it is superior in this respect.

MVS 2.0 will be released via the NSF-supported NanoHub/NEEDS website later this year, and a manuscript describing the physics of the model and the model verification with III-V HEMTs and Si ETSOI devices has been submitted to IEEE Transaction on Electron Devices.

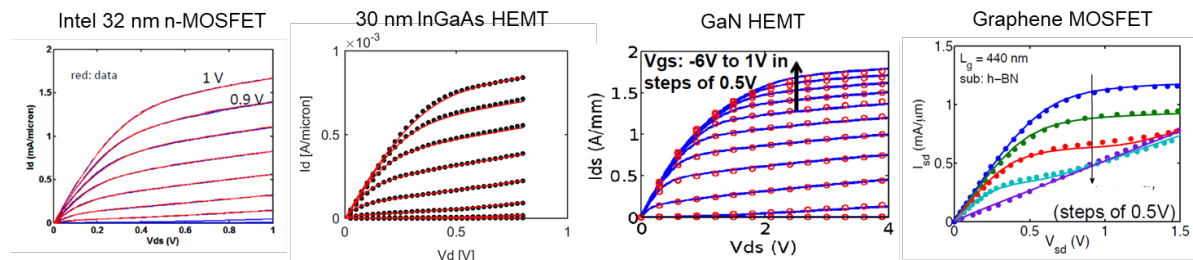


Figure 11: Modeling capabilities of MIT Compact Virtual Source model of (from left to right) planar Si MOSFET, planar InGaAs HEMT, GaN HEMT and Graphene MOSFET.

2016

Our planar InGaAs QW-MOSFETs have been instrumental in carrying out a detailed theoretical and experimental study of ballistic transport in the linear regime. This is important because device characterization in the linear regime is used to extract critical device parameters such as the external resistance. This is also an essential element for a holistic modeling of the device. Our study involves a systematic analysis of external resistance, ballistic resistance, and channel mobility in InGaAs QW-MOSFETs under near-equilibrium conditions. Our analysis includes the effect of carrier degeneracy in the quantum well. We have shown that unless ballistic transport and carrier degeneracy are properly accounted for, the external resistance is grossly overestimated as it incorporates the so-called ballistic resistance. Furthermore, taking advantage of the wide range of ballistics of the devices studied in this work, we demonstrate a methodology to self-consistently extract scattering-dependent effective mobility, mean-free-path length and ballistic mobility.

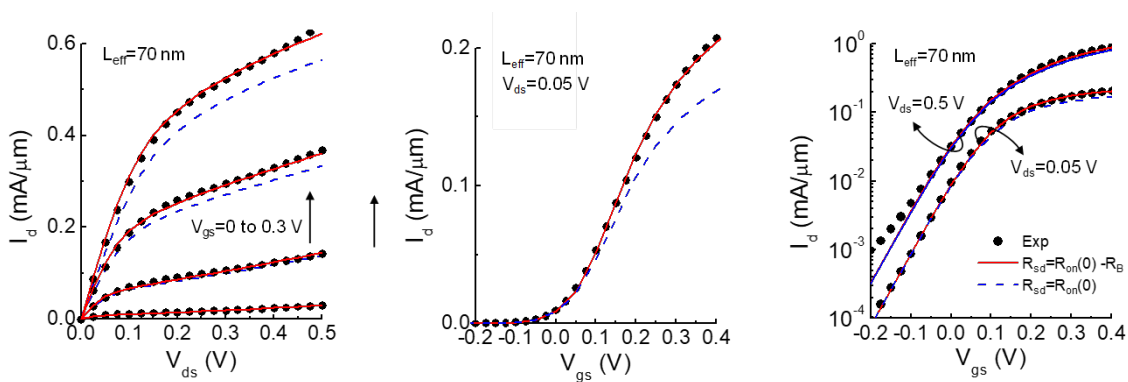


Figure 12: Modeling of planar InGaAs MOSFET. From left to right: output characteristics, transfer characteristics, subthreshold characteristics. Dashed blue line: conventional model. Red line: new mode that accounts for ballistics.

2017

Physics-based transistor models are important for technology projections and circuit simulations. To date, there has been little discussion on the incorporation of ballistic effects in transistor models. Recent experimental studies have revealed the significance of ballistic transport in the electrical characteristics of nanometer-scale InGaAs MOSFETs with ultra-low external resistance. Without proper accounting for the ballistic resistance and its gate voltage dependence, the access resistance to the intrinsic device cannot be accurately determined, and any physics-based transistor modeling is bound to fail. In this research, we have shown that the MIT Virtual Source model, which natively captures ballistic transport physics, correctly incorporates the impact of ballistic resistance. As a result, it accurately models the electrical characteristics of self-aligned nanoscale InGaAs MOSFETs, an excellent model system for near ballistic transistors, over a broad operational range. We also show that the success of the model development effort crucially relies on the correct extraction of the external source and drain resistance,  $R_{sd}$ , from experimental measurements.

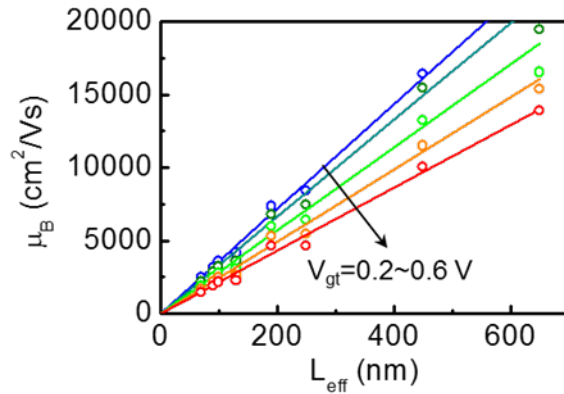


Figure 13: Ballistic mobility vs. effective gate length at varying gate overdrive as measured in planar InGaAs MOSFETs. The linear fits cross the origin.

## 2018

InGaAs FinFETs are challenged by relatively high leakage current in the OFF state. This originates from band-to-band tunneling (BTBT) at the drain end of the channel that is amplified by a parasitic bipolar effect (PBE) as a result of its floating body. We have developed an analytical model of the PBE in InGaAs FinFETs which captures the key gate length and fin width dependences. Our model accounts for surface recombination at the sidewalls of the fin as well as bulk recombination at the heavily doped source. When compared with experimental results, our model suggests that fin sidewall recombination dominates in long gate length transistors and leads to an exponential gate length dependence of the current gain on the parasitic bipolar junction transistor (BJT). The model enables the extraction of the carrier diffusion length which exhibits the predicted fin width dependence. For short gate length transistors, source recombination is shown to dominate and the parasitic bipolar gain scales with the inverse of the gate length.

A scaling study of excess OFF-state current in planar InGaAs quantum-well MOSFETs has also been carried out. We find that pure band-to-band tunneling (BTBT) dominates the drain OFF-state current in devices with channel length above  $\sim 1 \mu\text{m}$ . In this regime, the drain-gate voltage sets the rate of BTBT. In devices with channel lengths below  $1 \mu\text{m}$ , a parasitic bipolar transistor effect becomes relevant. The bipolar current gain is found to scale inversely with the effective channel length for  $L_g$  between  $70 \text{ nm}$  and  $1 \mu\text{m}$ , as expected from simple bipolar transistor theory. For  $L_g$  below  $\sim 70 \text{ nm}$ , the OFF-state current increases rapidly due to an enhancement in bipolar current gain as a result of strong short-channel effects and punchthrough. Current gains in excess of 104 have been observed. A reduction in channel thickness decreases both BTBT and the bipolar gain effect.

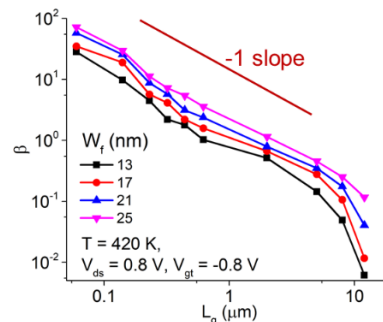


Figure 14: Current gain of parasitic bipolar transistor of InGaAs FinFETs as a function of gate length and fin width.

2019

Models for the performance of InGaAs MOSFETs and FinFETs predict values that are significantly larger than what is experimentally observed. This is particularly the case for thin-body planar MOSFETs and thin-fin FinFETs. An explanation for this discrepancy has been offered that relies in a reduction of mobility with body or fin thickness, similar to what has been observed in very thin body Silicon-on-Insulator MOSFETs. In our research on this important topic, we have found that in the presence of prominent gate oxide trapping, the conventional technique for channel mobility extraction based on IV-CV measurements becomes inadequate. This is the consequence of two different effects associated with oxide traps: gate voltage stretch-out and electron trapping and detrapping in the oxide at the MHz-range frequencies that are commonly utilized. In thin-channel planar InGaAs MOSFETs, both effects are observed and found to result in a severe overestimation of mobile charge and subsequently an underestimation of mobility using IV-CV. To address this issue, we demonstrate a new mobility extraction technique (RF-ID) based on concurrent IV and S-parameter measurement in the GHz regime that is largely immune to oxide trapping. Excellent agreement with Hall measurements as well as with theoretical predictions from Poisson-Schrodinger simulations give confidence to the new technique. Importantly, the new technique is not limited to InGaAs planar MOSFETs, but applies to any device geometry and any material system. Our new technique reveals that the channel mobility does degrade with channel thickness and fin width, however, the degradation is much less than conventionally believed. In fact, a promising mobility of  $\sim 1100 \text{ cm}^2/\text{V}\cdot\text{s}$  is found in quantum-well planar InGaAs MOSFETs with 4 nm-thick channel.

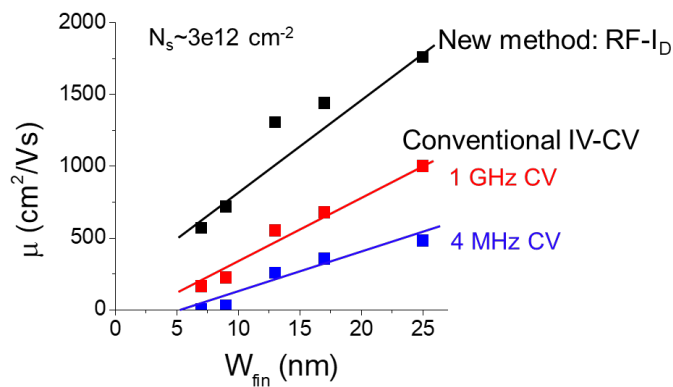


Figure 15: Channel mobility in InGaAs FinFETs as a function of fin width as extracted in three different ways: (blue) conventional IV-CV technique using C-V measurements at 4 MHz, (red) IV-CV technique using CV measurements at 1 GHz, (black) new technique.

### Publications and conference presentations emerging from this program

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