DIRECT DIGITAL SYNTHESIS: A FLEXIBLE ARCHITECTURE FOR ADVANCED SIGNALS RESEARCH FOR FUTURE SATELLITE NAVIGATION PAYLOADS

DISSERTATION

Pranav R. Patel, Civilian

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DEPARTMENT OF THE AIR FORCE
AIR UNIVERSITY

AIR FORCE INSTITUTE OF TECHNOLOGY

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Pranav R. Patel, BSCE, MSEE

Civilian

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Pranav R. Patel, BSCE, MSEE
Civilian

Committee Membership:

Richard K. Martin, PhD
Chairman

Robert F. Mills, PhD
Member

Michael R. Grimaila, PhD, CISM, CISSP
Member

Timothy W. Albrecht, PhD
Dean's Representative

ADEDJI B. BADIRU, PhD
Dean, Graduate School of Engineering and Management

AFIT-ENG-DS-20-S-014

Abstract

In legacy Global Positioning System (GPS) Satellite Navigation (SatNav) payloads, the architecture does not provide the flexibility to adapt to changing circumstances and environments. GPS SatNav payloads have largely remained unchanged since the system became fully operational in April 1995. Since then, the use of GPS has become ubiquitous in our day-to-day lives. GPS availability is now a basic assumption for distributed infrastructure; it has become inextricably tied to our national power grids, cellular networks, and global financial systems. Emerging advancements of easy to use radio technologies, such as software-defined radios (SDRs), have greatly lowered the difficulty of discovery and exploitation of vulnerabilities to these systems. The promise of a Direct Digital Synthesis (DDS) architecture provides the flexibility of incorporating countermeasures to emerging threats while maintaining backward capability with existing GPS signals.

The objective of the proposed research is to determine if DDS architecture is a viable replacement for legacy GPS SatNav payloads. The overall performance of several architectures is analyzed and evaluated. The architecture with the best performance is chosen and implemented onto a programmable logic device, and GPS signals are generated. The advantages and disadvantages of using the DDS model are discussed and an end-to-end numerical and mathematical models are developed. The end-to-end mathematical model analyzes the quantization effects of the DDS architecture, and it predicts the location and power levels of the desired signal and spurious content present in the spectrum. The spurious content may potentially cause intermodulation distortion to the desired signal. The appropriate DDS architecture and resources are selected by the information gained from the mathematical model.

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Pranav R. Patel

Table of Contents

Page

Page

List of Figures

List of Tables

List of Abbreviations

ADC analog-to-digital converter

AFB Air Force Base

AFIT Air Force Institute of Technology

AFRL Air Force Research Laboratory

AGT Advanced GPS Technologies

APL Applied Physics Laboratory

ARNS Aeronautical Radio Navigation Service

ASIC Application-Specific Integrated Circuits

BPSK Binary Phase Shift Keying

C/A Coarse/Acquisition

CDMA Code Division Multiple Access

Chimera Chips-Message Robust Authentication

CLB configurable logic block

COTS commercial off-the-shelf

CW continuous wave

DAC digital-to-analog converter

DDS Direct Digital Synthesis

DNSS Defense Navigation Satellite System

DoD Department of Defense

DSP Digital Signal Processing

DSSS direct-sequence spread spectrum

EGNOS European Geostationary Navigation Overlay Service

EU European Union

EW Electronic Warfare

FHSS Frequency-Hopping Spread Spectrum

FOC Full Operational Capability

FPGA Field Programmable Gate Array

GNSSTA Global Navigation Satellite System Test Architecture

GOTS government off-the-shelf

GPS Global Positioning System

GNSS Global Navigation Satellite System

GSPS GigaSamples Per Second

GWPP GNSS Waveform Prototyping Platform

HDL Hardware Description Language

HPA high-power amplifier

HYB Hybrid RF switches

IOC Initial Operational Capability

IPA intermediate-power amplifier

JPO Joint Program Office

LFSR Linear Feedback Shift Registers

LSBs Least Significant Bits

LUT look-up table

M Military

MACC multiply accumulate

MEO medium Earth orbit

MMCM Mixed-Mode Clock Managers

MSB Most Significant Bit

MSPS MegaSamples Per Second

NASA National Aeronautics and Space Administration

NCO Numerically Controlled Oscillator

NIMS Navy Ionospheric Monitoring System

NNSS Navy Navigation Satellite System

NRL Navy Research Laboratory

NTS-I Navigation Technology Satellite I

NTS-II Navigation Technology Satellite II

NTS-III Navigation Technology Satellite III

ORDWG On-Orbit Reprogrammable Digital Waveform Generator

P Precise

PLL Phase Lock Loop

POCET Phase Optimized Constant Envelope Transmission

PRN pseudorandom noise

PRNSA Pseudo Random Noise Subsystem Assembly

RAM Random Access Memory

RF radio frequency

ROM Read Only Memory

SA Selective Availability

SAMSO Space and Missile Organization

SatNav Satellite Navigation

SDR software-defined radio

SoL safety-of-life

SPS Standard Positioning Service

STR Side Tone Ranging

SV satellite vehicle

TIMATION TIMe/navigATION

uC microcontroller

USAF United States Air Force

VCO Voltage Controlled Oscillator

VHDL VHSIC Hardware Description Language

VHSIC Very High Speed Integrated Circuit

ZOH Zero-Order-Hold

DIRECT DIGITAL SYNTHESIS: A FLEXIBLE ARCHITECTURE FOR ADVANCED SIGNALS RESEARCH FOR FUTURE SATELLITE NAVIGATION PAYLOADS

I. Motivation

It has been almost 20 years since the U.S. Government decided to discontinue the use of Selective Availability (SA) on Global Positioning System (GPS) Standard Positioning Service (SPS). Before the discontinuation of SA, civilian GPS service only had a position accuracy of GPS within 100 meters. After the discontinuation of SA, the position accuracy improved to within 20 meters [1]. This allowed for the use of GPS technology to flourish and it has since become the de facto standard for worldwide precise navigation, timing, and time transfer. However, the current civilian GPS service does not provide resiliency against threats such as intentional or unintentional interference. Current Satellite Navigation (SatNav) payloads are unable to incorporate any kind of resiliencies from emerging threats because it lacks a reconfigurable architecture.

The Air Force Research Laboratory's (AFRL's) Advanced GPS Technologies (AGT) program researches and develops advanced techniques to detect and mitigate existing and potential threats, thus increasing SatNav system resiliency for military and civilian users. The DDS architecture is being considered for implementation on an On-Orbit Reprogrammable Digital Waveform Generator (ORDWG) [2]. Using the DDS method with a high-speed digital-to-analog converter (DAC) may provide the required flexibility for future-proof payloads. Direct Digital Synthesis (DDS) allows for digital control of frequency and phase in subnano-hertz and subnano-degrees,

respectively. Even though DDS allows for precise control, analog components may introduce variations to the generated signal, such as frequency drift. Due to analog component aging, system calibration is needed to compensate for these variations. The DDS architecture reduces the number of analog components used. When used as a quadrature synthesizer, DDS eliminates the delays between the in-phase and quadrature (I/Q) channels. Finally, the entire DDS can be controlled digitally thus giving software-defined capability to the system. The ability to dynamically update signals in orbit using a DDS architecture may drastically reduce modernization costs and development time. Particularly, as new threats to GPS emerge, a DDS architecture will allow engineers and operators to mitigate those threats rapidly and efficiently on existing systems.

Implementing a DDS architecture in a test system determines the viability of the architecture as a SatNav payload. The GPS constellation is located in medium Earth orbit (MEO), and the test system shall emulate the Doppler effects of a dynamic satellite constellation. Also, the DDS architecture generates in-band spurious content. It is critical to know the reasons, location, and power levels of the spurious content to prevent intermodulation interference. The research in this document covers the above topics.

The rest of this document is organized as follows. Chapter II begins with background information followed by a standard notation set. Afterward, various DDS architectures, such as Wheatley Random Jittering, pulse output, fractional divider, triangle output, sine output, and phase interpolation, are discussed and evaluated. Next, the section of the origins of GPS discusses the entire history of GPS from the launch of Sputnik I to the Full Operational Capability (FOC) of the entire system. In addition, the chapter discusses the GPS payload and signal structure. Finally, hardware information used to conduct the research is discussed.

In Chapter III, a viable DDS architecture is selected and implemented on hardware with a high-speed DAC and GPS L1 Coarse/Acquisition (C/A) signals with navigation messages are generated; existing commercial off-the-shelf (COTS) and government off-the-shelf (GOTS) GPS receivers will be used to evaluate the generated signal. The implementation includes Doppler shifts to mimic a dynamic satellite constellation. The chapter discusses a synchronization technique used to generate multiple signals in parallel at lower speeds to match the sampling rate requirements of the DAC. This allows the DDS architecture to be used in programmable logic devices that aren't able to operate at the same sampling rate as the DAC.

Chapter IV covers mathematical analysis and numerical evaluation of the close-in phase noise and quantization effects of DDS architecture. Global Navigation Satellite System (GNSS) is very sensitive to any kind of excessive phase noise. The phase noise directly impacts the navigation solution generated by GPS receivers. Also, the quantization error is a disadvantage of using a DDS architecture, because it generates in-band spurious content. The chapter discusses the end-to-end numerical and mathematical modeling of the DDS architecture. With a given set of design parameters, an analytical solution determines the locations and power levels of the in-band spurious content.

Chapter V concludes the dissertation with a summary of the three contributions and discusses thoughts on future work for the research.

II. Background

This chapter outlines background information about DDS architectures, origins of GPS, GPS payload design, GPS L1 C/A signal structure, high-speed DAC, reconstruction filer, and the Field Programmable Gate Array (FPGA) overview. First, an overview of various DDS architectures is given, followed by notation definitions. Next, the implementation of a selected DDS architecture for a GPS application is examined. Furthermore, details of the origins of GPS, GPS payload and L1 C/A signal structure are discussed. Finally, an overview of the hardware used for this research is discussed. This includes information of the high-speed DAC, reconstruction filer, and the FPGA device.

DDS architectures provides greater flexibility in signal generation than traditional analog or mixed signal architectures. It offers all-digital control over the signal generation process. Digital control offers total software-defined capability, with subnano degree and voltage precision, over the phase and amplitude of the signal. Unlike analog architectures, digital architectures provide a future-proof capability for signal generation.

Current GPS SatNav payloads use a direct modulation architecture for signal generation. Upon inspection of the L-band system block diagram [3], the architecture relies heavily on analog components because of the lack of an analog-to-digital converter (ADC) in the signal path. However, the architecture of the C/A code generator is comprised of digital components such as shift registers [3]. Since the L-band systems have fixed analog frequency synthesizers and modulators, the system is unequipped to make any changes to the synthesized frequency or the modulation. The goal of the DDS architecture is to reduce obsolescence by providing the flexibility to make changes to the signal structure. The aim of this work is to use the DDS architecture and determine viability as a potential alternative SatNav solution.

2.1 Notation

To analyze various DDS systems, some notation is needed to describe the architecture.

Table 1. Variables

Variable	Description
f_s	Sampling Frequency
f_c	Carrier Frequency
f_{clk}	Clock Frequency
K	Step Size for Frequency Requested
n	Time Sample Index
T	Sample Period
N	Number of Total Bits
R	Result of Accumulator
C/N_0	Carrier-to-Noise Ratio

2.2 DDS Overview

Various types of DDS architectures have been researched. The performance of each architecture differs in spectral purity. Lack of spectral purity would cause the desired signal to degrade in total power, the generation of in-band spurious content, and an increase in phase noise. Additional loss of total power of an already weak GPS signal would cause acquisition problems for the receiver. The generation of in-band spurious content would cause correlation problems with the receiver because the spurs would be within the GPS bandwidth. Phase jitter on the signal would cause the phase noise to increase. This would cause the noise floor to increase and drown out weaker signals, and the receiver would see the jitter as motion. To generate an

ideal GPS signal, maximizing spectral purity of the signal is critical.

There are six major types of DDS architectures: Pulse Output, Fractional Divider, Triangle Output, Sine Output, Phase Interpolation, and Wheatley Random Jittering Injection. The performance of each architecture varies and this will impact the spectral purity of the signal.

2.2.1 Pulse Output DDS.

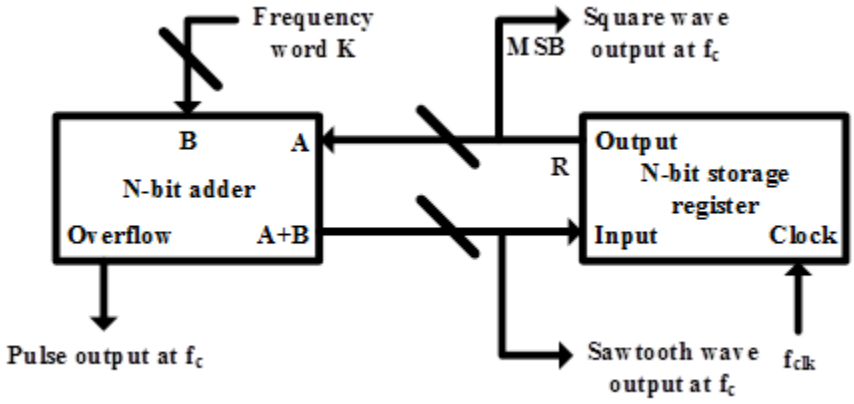

Figure 1. Pulse Output DDS Architecture [4]

The Pulse Output architecture, as shown in Figure 1, is the simplest of the six DDS architectures [4] and the most versatile in generating different kinds of waves at a specific carrier frequency (f_c). It consists of an accumulator with N-bits of resolution. For every clock frequency (f_{clk}), K is added onto the previous value. The Pulse Output architecture produces pulses, square, and sawtooth waves at f_c and is described as

$$f_c = \frac{K}{2^N} \cdot f_{clk} \tag{1}$$

The square wave is generated by the Most Significant Bit (MSB) of the output of the storage register. The sawtooth wave is generated by the resulting value of the

accumulator. The accumulator is expressed by

$$R(n) = mod(K \cdot n, 2^N) \tag{2}$$

The pulses are generated by the overflow flag from the adder in the accumulator. The overflow flag is set when the value of the accumulator exceeds N-bits. Since there is an abrupt change in energy, high frequency content is generated thus causing large in-band spurious emissions to be generated [5]. Out of all six architectures, the Pulse Output architecture has the most in-band spurious content and phase jitter [4].

2.2.2 Fractional Divider DDS.

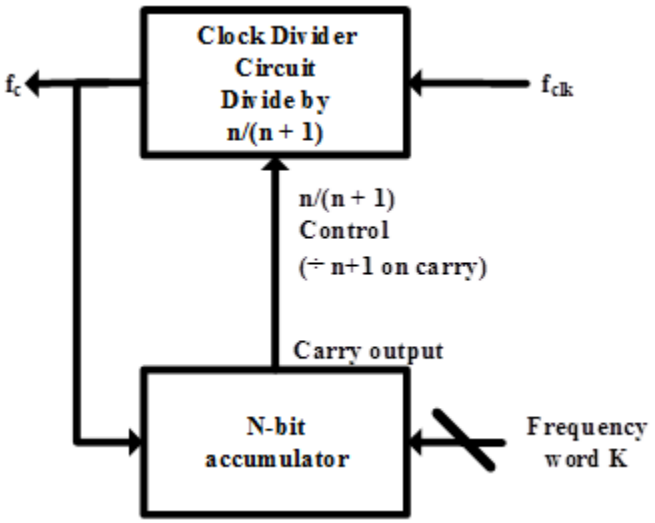

Figure 2. Fractional Divider DDS Architecture [4]

The Fractional Divider architecture, as shown in Figure 2, is a modified version of the Pulse Output architecture. The clock of the accumulator is controlled by a clock divider circuit. The clock divider circuit regulates the clock to determine when the accumulator will perform its addition process. The Fractional Divider architecture produces pulses at f_c and is described as

$$f_c = \frac{f_{clk}}{n + (\frac{K}{2^N})} \tag{3}$$

Pulses are generated with this architecture. As a result, the amount of in-band spurious content is equivalent to the Pulse Output architecture, but the phase jitter is less due to being able have fractional control over the accumulator [4].

2.2.3 Triangle Output DDS.

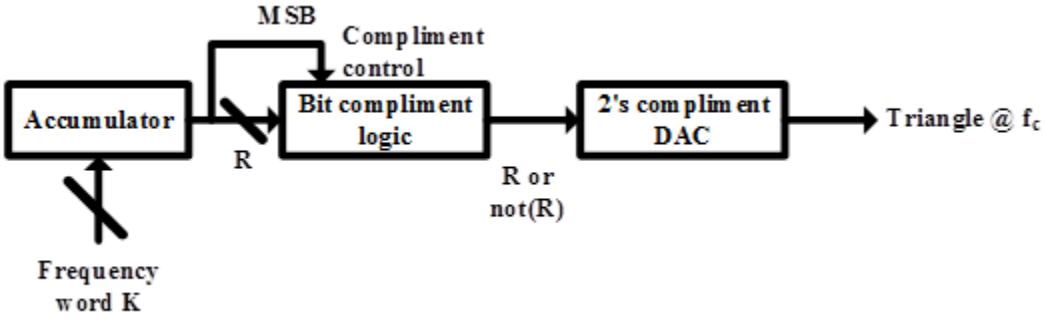

Figure 3. Triangle Output DDS Architecture [4]

The Triangle Output architecture, as shown in Figure 3, produces a triangle wave. Unlike the pulsed architectures, the Triangle Output architecture requires a DAC to convert digital values into an analog representation form. Like the prior architectures, the accumulator is used to calculate phase of the signal. The MSB of the phase is stripped from the resulting value and used to determine if the remaining bits should be complimented. As a result, the values will gradually increase and decrease over time. The Triangle Output architecture produces a triangle wave at f_c where

$$f_c = \frac{K}{2^N} \cdot f_{clk} \tag{4}$$

Unlike the Pulse Output architecture, there is a gradual change in value. As a result, the in-band spurious emissions are less in magnitude, but the amount of phase jitter

is the same as the Pulse Output architecture.

2.2.4 Sine Output DDS.

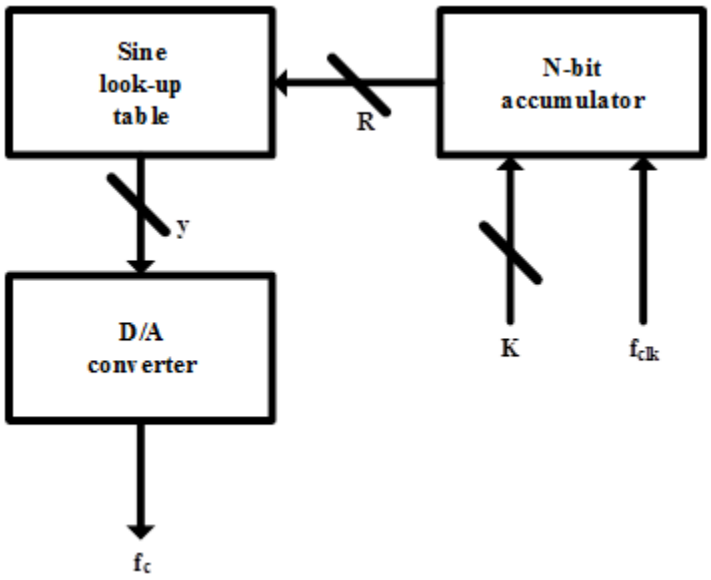

Figure 4. Sine Output DDS Architecture [4]

The Sine Output architecture, as shown in Figure 4, produces a sinusoidal wave. The phase of the signal is produced from the accumulator and is described as

$$f_c = \frac{K}{2^N} \cdot f_{clk} \tag{5}$$

$$R(n) = mod(K \cdot n, 2^N) \tag{6}$$

The phase is used as an address for the sine look-up table (LUT). The quantized form of a sinusoidal wave is stored in the LUT. As a result, a signal is produced which resembles the ideal form of a sinusoidal wave and described by the following equation

$$y(n) = sin\left(\frac{2 \cdot \pi \cdot R(n)}{2^N}\right) \tag{7}$$

Any quantization effects are caused by the bit resolution of the accumulator and the stored sinusoidal wave in the LUT. The quantization effects will vary the magnitude of the in-band spurious emissions, but the amount of phase jitter is the same as the Pulse Output and Triangle Output architectures.

2.2.5 Phase Interpolation DDS.

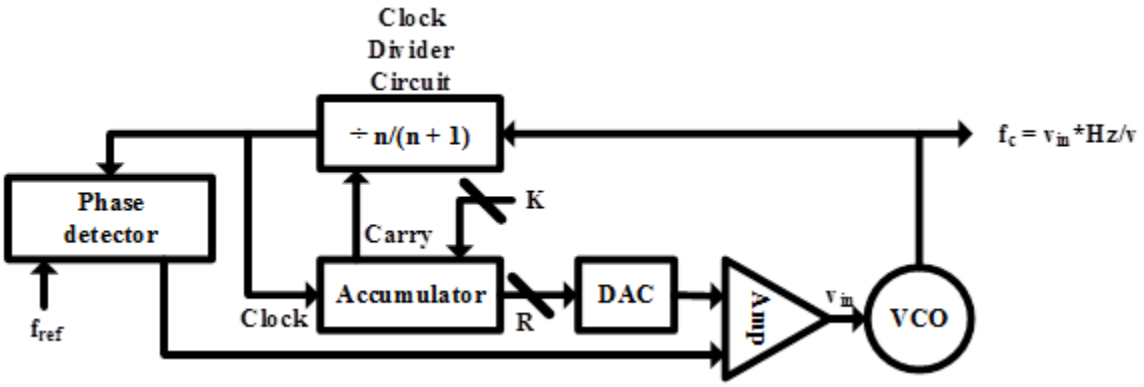

Figure 5. Phase Interpolation DDS Architecture [4]

The Phase Interpolation architecture, as shown in Figure 5, uses external analog components such as Voltage Controlled Oscillator (VCO) and a Phase Detector. The VCO is used as a Phase Lock Loop (PLL) to provide feedback to the divider loop, which controls the clock to the accumulator. The Phase Detector allows for greater reduction in phase jitter and in-band spurious emissions compared to other architectures.

2.2.6 Wheatley Random Jittering Injection DDS.

The Wheatley Random Jittering Injection architecture, as shown in Figure 6, uses dithering techniques to reduce the amount of in-band spurious content. The dithering technique injects uniformly distributed values from 0 to K-1 into the signal causing the periodicity of the phase deviation patterns to be destroyed. Since noise is being injected into the signal, the overall noise floor and phase jitter is increased.

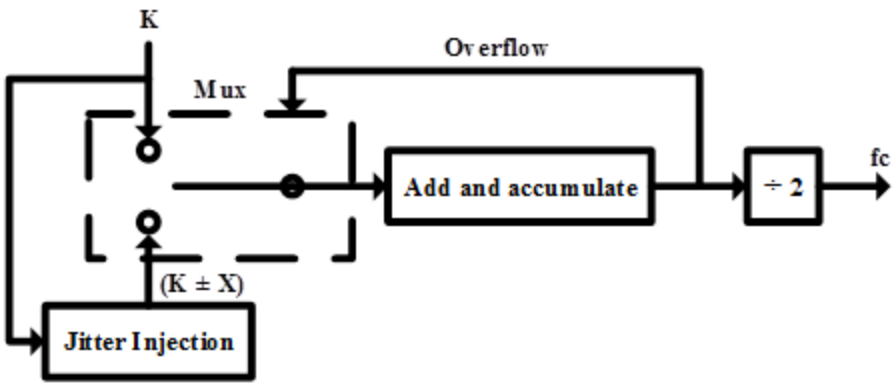

Figure 6. Wheatley Random Jittering Injection DDS Architecture [4]

2.3 GPS

Since GPS became operational over 20 years ago, it has become the de facto standard for worldwide precise navigation, timing, and time transfer solution. The development of GPS did not happen in a few years, but it took decades of research and development from multiple organizations. From its origins on the Soviet Union's Sputnik 1, to the U.S. Navy's Transit and TIMe/navigATION (TIMATION) systems, the U.S. Air Force's 621B program is the culmination of decades of research leading up to modern GPS.

2.3.1 History of Transit.

The Soviet Union launched the first artificial satellite named Sputnik I on October 4, 1957. Not only did it kick off the space race, it also opened a new era of research in navigation technology. William H. Guier and George C. Weiffenbach, two junior physicists at Johns Hopkins Applied Physics Laboratory (APL), were able to track Sputnik by monitoring the doppler shift of the 1 kHz signal at a carrier frequency of 20 MHz [6]. With this information, the orbit and position of the satellite could be determined.

In November 3, 1957, the Soviet Union launched Sputnik II satellite into Earth's

orbit. The satellite transmitted at 20 MHz and 40 MHz. With collected data from both frequencies, it was determined a first-order correction for ionospheric refraction was required, as well as an inferred correction for any oscillator clock drift [6]. This allowed for the creation of a more accurate model of the satellite orbit.

On March 17, 1958, Frank McClure, the chairman of APL Research Center, proposed to invert the solution. Instead of determining the satellite position by monitoring the doppler shifts of the transmitted signal, the position of the receiver can be determined by knowing the locations of satellites at a given time. This led to the development of the Transit system.

The Transit system, or Navy Navigation Satellite System (NNSS), was used by the U.S. Navy to provide accurate two-dimensional navigation solution to its Polaris ballistic missile submarines [7]. A series of experimental satellites were developed and launched. Afterwards, operational satellites were launched.

Transit 1A was the first experimental satellite to be launched from Cape Canaveral on September 17, 1959, but it failed to reach orbit. Transit 1B was launched on April 13, 1960 and it stayed in orbit for 89 days [8]. The satellite transmitted coherently on two frequency pairs to test atmospheric ionospheric error correction and to determine the ideal separation between transmitted frequencies. It also was the first satellite to use magnetic techniques to maintain attitude control for proper Doppler tracking [8].

Transit 2A was launched on June 22, 1960 from Cape Canaveral, and it stayed operating until October 26, 1962. The satellite transmitted on 54, 162, 216, and 324 MHz, and had sensors to measure cosmic noise, satellite rotation, and temperature sensors. Transit 2B was planned but never built.

Transit 3A was launched but failed to reach orbit on November 30, 1960 from Cape Canaveral. Transit 3B was launched on February 21, 1961 from Cape Canaveral, and it stayed operating until March 30, 1961. The satellite was placed in a more

eccentric orbit by accident because the rocket failed to separate from the upper stage. It had a digital clock synchronized with the transmitters and the digital memory. The navigation data containing the satellite's orbital position was sent to the 384-bit digital memory from the ground station, and the data was modulated on to the transmitted signal by using phase modulation of +/- 60 degrees [8][9]. The ground station was able to verify the position of the satellite and the modulated data did not degrade the accuracy of the doppler signal and measurements.

Transit 4A and 4B were launched on June 29, 1961 and November 15, 1961, respectively, from Cape Canaveral. The satellites transmitted coherently on 150 MHz and 400 MHz. Working together, both satellites allowed the determination of harmonics in the Earths gravity field that had not yet been evaluated [8].

2.3.2 History of TIMATION.

The Transit satellite system relied on analyzing the doppler information of the satellite to determine its position. This method of calculating position did not provide an instantaneous solution, precise time transfer, or three-dimensional position capability.

In 1964, the Navy Research Laboratory (NRL) created the TIMATION program. The objectives of the TIMATION project were to speed up the means of determining the position solution by using passive ranging techniques, such as Side Tone Ranging (STR), demonstrate technology for a three-dimensional position solution, and provide precise time transfer capability [10]. Combining the STR technique with doppler information provides an instantaneous positioning solution. To accomplish this, the satellite must have an accurate and stable oscillator. The focus of the TIMATION project is to research and develop a satellite with such an oscillator.

TIMATION I was launched into the two-hour circular orbit on May 31, 1967

from Vandenberg Air Force Base (AFB), and it was operational for 74 months [11]. Compared with previous satellites, it carried two very stable quartz-crystal oscillators operating at 5 MHz. Using the oscillator, a continuous wave (CW) 400 MHz carrier frequency with subcarriers are generated and transmitted. The STR technique was successfully demonstrated with an accuracy to about 0.3 nautical miles [12].

TIMATION II was launched into the two-hour circular orbit on September 30, 1969 from Vandenburg AFB, and it was operational for six years [11]. It carried two stable oscillators with a greater stability compared to the oscillators on TIMATION I. It used the oscillators to generate two CW signals with subcarriers at 150 MHz and 400 MHz.

During the Transit program, it was discovered there was an ionospheric group delay causing the accuracy of the position solution to degrade. Receiving two signals from two different frequencies helped determine the ionospheric group delay. With the ionospheric group delay determined, the position solution had an accuracy within 200 feet [12].

In April 1973, the TIMATION program of NRL was merged with the 621B program of the United States Air Force (USAF) to form the Joint Program Office (JPO) [13]. The JPO was charged to develop the next generation satellite system called Defense Navigation Satellite System (DNSS). It was later to be renamed to the NAVSTAR-GPS program. The continuing development of TIMATION-III was moved to the new program and was re-designated as the Navigation Technology Satellite I (NTS-I).

2.3.3 History of System 621B.

In 1962, while the U.S. Navy was continuing to develop its own satellite-based navigation system, another group was formed to research ways to improve the accuracy

of satellite-based navigation systems. Led by Dr. Ivan Getting from the Aerospace Corporation, the U.S. Air Force 621B program was created.

Dr. Ivan Getting proposed concepts for a satellite-based navigation system with greater accuracy that would provide a three-dimensional position solution, and be available 24 hours a day, seven days a week [14]. The proposed concept of the navigation system consisted of 16 satellites providing 24-hour coverage and a new type of satellite ranging signal based on pseudorandom noise (PRN) [15]. The satellites would be placed in geosynchronous orbits forming four oval shaped clusters that would always provide visibility of a minimum of four satellites on the ground. This would meet the requirements of providing time and three-dimension position solution. Incorporating the PRN into the signal would add the direct-sequence spread spectrum (DSSS) technique to reduce signal interference and allow multiple satellites to transmit on the same frequency without any interference.

In August 1966, James Woodford and Hideyoshi Nakamura, from the Aerospace Corporation, released a comprehensive study on the system aspects of a new navigation satellite system. The study contained three key issues: capabilities and limitations of past and current navigation systems, applications of improved position accuracy, and an analysis of alternative satellite system configurations and techniques for positioning [12]. They advocated the use of passive ranging methods of satellite navigation, atomic clocks for satellites, and experimental demonstrations.

Between 1970 and 1972, research and development began for System 621B. Between June and December of 1970, engineers worked on development plans for the system. It included the design of the equipment, laboratory tests, and data processing. Building of equipment happened throughout 1971. Finally, testing of the entire system was conducted throughout 1972 [16].

In 1972, System 621B was finally tested at White Sands Missile Range in White

Sands, New Mexico. Since satellites of the system werent developed, four ground-based transmitters and an airborne receiver system in the NC-135A aircraft was used. The ground-based transmitters were arranged as a scaled-down version of the Y constellation sub-satellite points [16]. Each transmitter generated a signal with a PRN orthogonal to the others. A mobile calibration station was used to synchronize the transmitters. The data was collected on the in-flight recorder and was post-processed.

Afterwards, a landing navigation aid test was conducted to determine the accuracy of aircraft vertical position and velocity information provided by the navigation system [16]. An additional transmitter was attached to an air balloon and was suspended 5000 ft. Data was also recorded and post-processed for this test.

The data was processed for both tests, and it was determined its accuracy was within a few feet [16]. The tests confirmed the operation of multiple PRN on a common frequency, providing three-dimensional position solution, and the need for atomic clocks on satellites.

2.3.4 History of GPS.

In April 17, 1973, Deputy Secretary of Defense William P. Clements, Jr, consolidated satellite navigation concepts from various agencies into a single comprehensive Department of Defense (DoD) system. This system was known as DNSS and would later be called NAVSTAR-GPS. The JPO at Space and Missile Organization (SAMSO) in Los Angeles AFB would oversee the effort and, the U.S. Air Force was selected to lead the program.

NTS-I, renamed from TIMATION III, was launched into the eight-hour circular orbit on July 14, 1974 from Vandenberg AFB, and it was operational for five years [11]. Instead of crystal oscillator clocks, NTS-I had two rubidium vapor clocks driving

the signal generators. Two CW signals at 335 MHz and 1580 MHz were generated to determine the frequency stability of the clocks. Results from NRL tests indicated the clocks were too sensitive to temperature variations.

Navigation Technology Satellite II (NTS-II) was launched into the 12-hour circular orbit on June 23, 1977 from Vandenberg AFB, and it was operational for only 18 months [11]. Instead of using rubidium clocks, cesium beam oscillators were used. The satellite also had a Pseudo Random Noise Subsystem Assembly (PRNSA) to generate a signal with PRN. The satellite also had the first GPS space borne computer but failed before testing could commence. NTS-II was the first Phase 1 demonstrational satellite for NAVSTAR-GPS [11].

A set of Navigation Development Satellites, called Block 1, were launched from February 22, 1978 until October 9, 1985 from Vandenberg AFB. There were 11 total satellites in Block 1. All but one successfully made it into orbit. The Rockwell International satellites were only designed with a three-year lifespan but lasted for over 10 years. The system was successful in demonstrating Initial Operational Capability (IOC) [3].

After successfully demonstrating initial operational capability, Block 2 operational satellites were launched into orbit. Until 1983, the military was the only intended user of GPS. In 1983, the Soviet Union mistook a Korean passenger jet for a military jet and shot down the passenger jet killing all 269 people on-board [17]. At that point, the U.S. government opened GPS to the public and provided a GPS signal for civilian use but with intentionally degraded accuracy. In the summer of 1993, the 24th satellite was launched, and the system reached FOC.

By 2000, the world-wide dependency for a satellite-based navigation system has increased. At this point, the U.S. and Russia were the only countries that owned and maintained 24/7 satellite-based navigation systems. The European Union (EU),

China, and others envisioned overcoming the monopoly of satellite-based navigation system and started development of their own system [18]. In response to potentially losing the monopoly, on May 1st, 2000 at 8 P.M. EDT, the U.S. government disabled degrading the signal for civilian use [19]. Since then, the civilian GPS signal has had relatively the same level of accuracy as the military signal [20].

After successes of the experimental satellites, forty-six operational satellites were launched until August 25, 1988 [21]. The operational system had an accuracy of 25 meters and only was able to provide a two-dimensional position solution [22]. At the end of 1996, using Transit as a navigation solution was superseded by GPS, but the system was repurposed as the Navy Ionospheric Monitoring System (NIMS).

Over 60 years in either development or in operation, GPS has become ubiquitous in our day-to-day lives. It is being used in critical infrastructure, communications, financial markets, mining, agriculture, aviation, land and air-based navigation, surveying, marine, recreation, and military applications. It is critical to protect the system from emerging threats by developing future iterations of the system with a flexible architecture.

2.4 GPS Payload

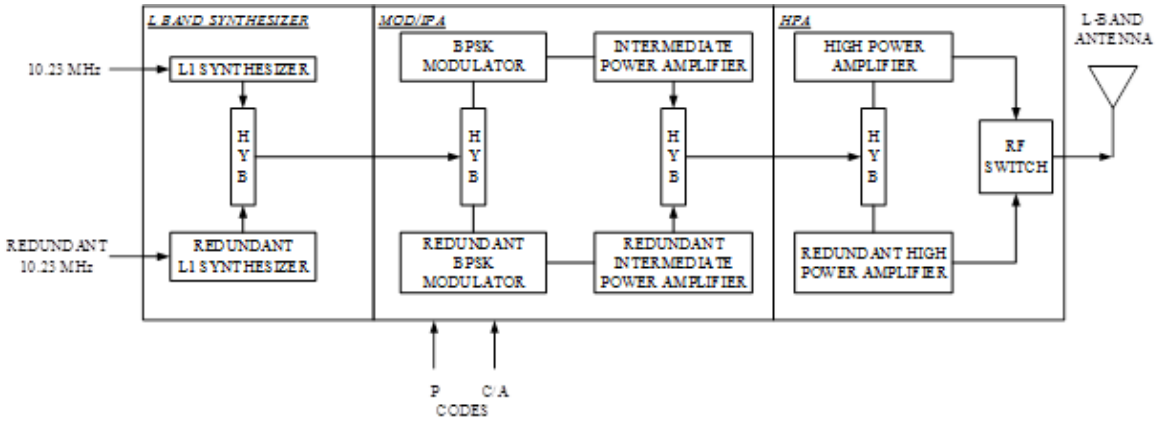

Figure 7. L-Band System Block Diagram [3]

Ever since achieving IOC, the signal generation piece of the satellite payload has remained unchanged. Figure 7 shows the L-band system block diagram of the signal generation payload. Hybrid RF switches (HYB) are put in place at every stage to provide redundancies to mitigate component failures. In the synthesizer stage, a 10.23 MHz reference oscillator is used to synthesize the L-band signal at radio frequency (RF). Afterwards, the Binary Phase Shift Keying (BPSK) modulator shifts the phase of the synthesized L-band signal from 0 to 180 degrees. The phase shifts depend on the binary output of the C/A or Precise (P) code. Afterwards, the modulated signal goes through an intermediate-power amplifier (IPA), then through the high-power amplifier (HPA), and finally out to the antenna. If multiple signals are generated, a signal combiner, such as a diplexer or triplexer, is added right before the antenna.

The gain of amplifiers used in GPS Blocks and specific L band signal can vary. Since L1 is allocated to Aeronautical Radio Navigation Service (ARNS), the signal is considered part of European Geostationary Navigation Overlay Service (EGNOS) safety-of-life (SoL) service. As part of SoL, the signal must meet specific requirements to provide accurate and reliable navigation service. Typically, higher gain from the amplifiers are given to ARNS signals for easier acquisition. For Block 2R satellites, the L-band synthesizer stage generates the 18 dBm signal. The L1 IPA and HPA stages provides an additional 14 dBm and 48.5 dBm gain, respectively. For L2, there is only a 10.7 dBm and 39.5 dBm gain for the IPA and HPA stages, respectively [3].

The C/A and P code generator algorithms are running on the space borne computer, and the output is sent to the BPSK modulator in the signal generator piece of the satellite payload. Figure 8 shows the design of the C/A code algorithm. G1/G2 Shift Registers consist of 10-stage Linear Feedback Shift Registers (LFSR). The initialization and polynomial values for G1/G2 and the values of phase selector for G2

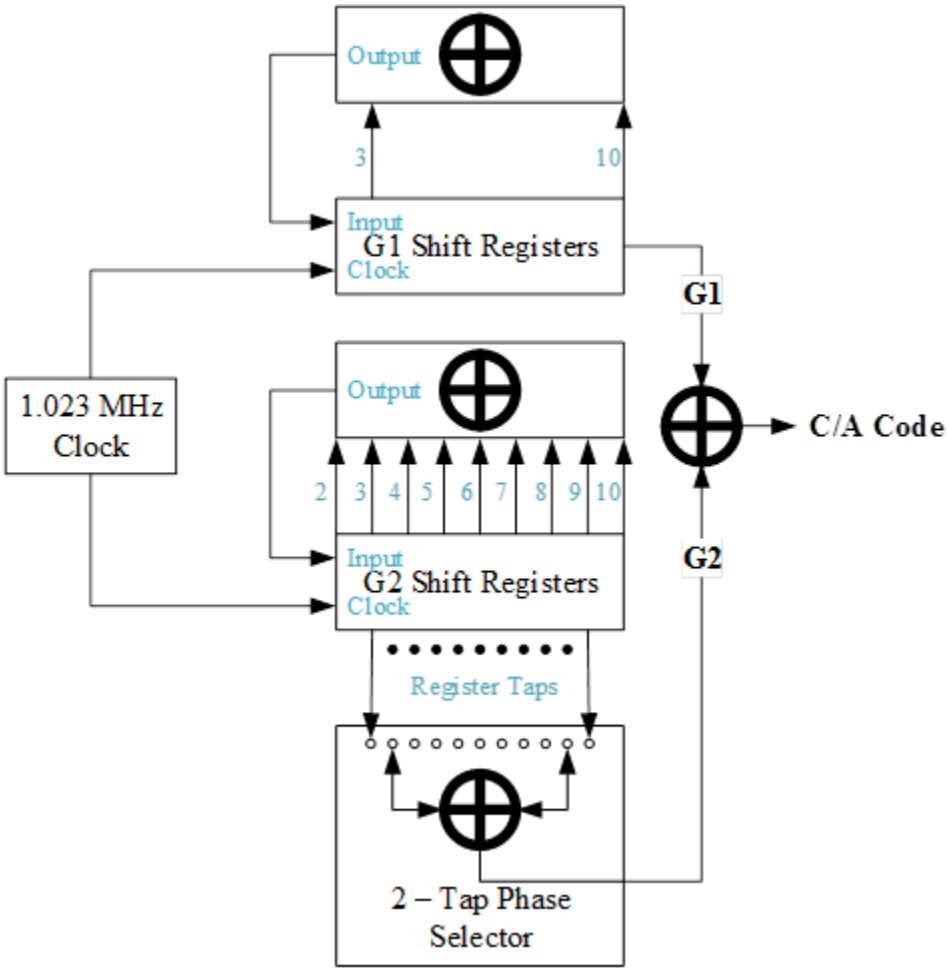

Figure 8. L1 C/A Code Generator [23]

for each PRN are detailed in Global Positioning Systems Directorate Systems Engineering & Integration Interface Specification document [23].

The architectures for the signal and code generators are inflexible designs. The majority of the signal generator design is comprised of analog components which can not be changed while in orbit. The code generators algorithm is mostly inflexible except for the initialization values and phase selector to select a specific PRN. Adding additional capabilities to an existing system is impossible because of the rigidity of the architecture.

2.5 GPS Signal Structure

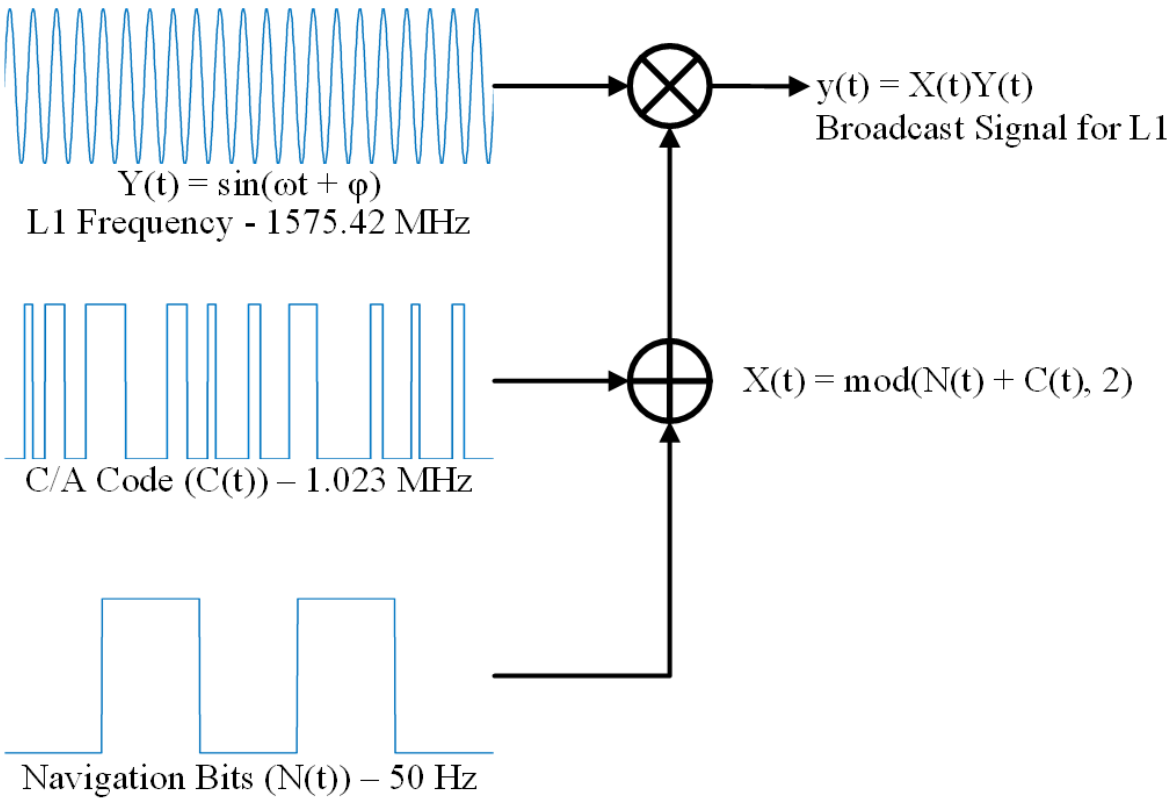

Figure 9. L1 C/A Signal Structure

Figure 9 shows the signal structure for the L1 C/A signal. The C/A code generator produces a bit at 1.023 MHz, while the navigation message outputs a bit at 50 Hz. Modulo-2 addition is performed on the code and navigation bits. The result is multiplied by the generated cosine wave at L1 frequency. It is worth noting that the precise code uses the same structure but is multiplied with a sine wave instead of a cosine wave. The resulting signals for both C/A and P are added together before transmission.

2.6 Hardware Information

To implement the DDS architecture in hardware, high-end components must be used to regenerate the GPS signal. The main components for DDS signal generation are a high-speed DAC, reconstruction filter, and a programmable processor, such as a microprocessor, FPGA, or Application-Specific Integrated Circuits (ASIC).

2.6.1 High-Speed DAC.

The high-speed DAC takes discretized data and reconstructs an analog representation of the signal. The sampling frequency and carrier frequencies must meet Nyquists Law to properly reconstruct the analog signal.

2.6.1.1 Abaco Systems FMC230.

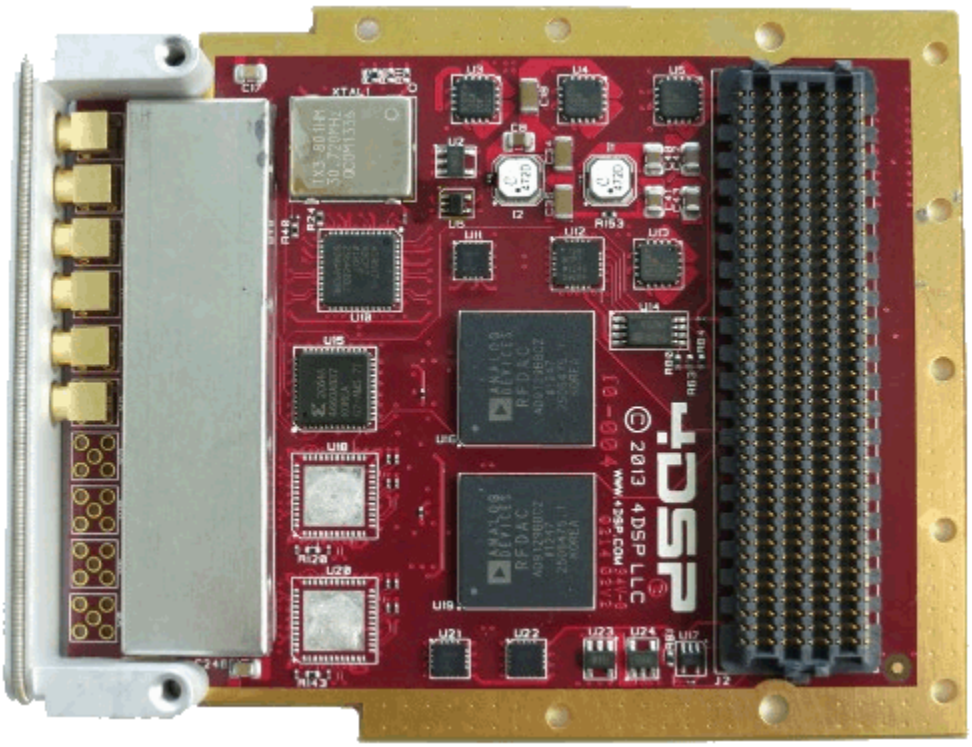

Figure 10. Abaco Systems FMC230

Figure 10 shows Abaco Systems FMC230 daughterboard. The daughterboard has two DAC to convert discretized signals into an analog representation of the signal. The FMC230 features [24]

- Two AD9129: 2-channel 14-bit DAC up to 5.7 GigaSamples Per Second (GSPS) or 2.85 GSPS with or without 2:1 interpolation, respectively
- 2300 MHz 2650 MHz on-board VCO

The Analog Devices AD9129 is a 14-bit high speed DAC with update rates up to 5.7 GHz with 2:1 interpolation or in "Mix-Mode". Without interpolation or "Mix-Mode", the update rate can be up to 2.85 GHz. In "Mix-Mode" operation, the AD9119/AD9129 can reconstruct RF carriers in the second and third Nyquist zone while still maintaining exceptional dynamic range up to 4.2 GHz [25]. To generate a signal at L1, the signal must be generated at the DAC baseband sampling frequency - L1. The DAC in "Mix-Mode" will take the samples and negate the samples of the falling edge of 2x of the DAC baseband sampling frequency. This essentially shifts the 2nd Nyquist zone into the 1st Nyquist zone.

2.6.2 L1 Reconstruction Filter.

After the signal is produced by the DAC, it is still in the quantized form, as shown in Figure 11. After the signal has passed through the reconstruction filter, the filter attenuates frequencies that are not in the pass band region of the filter. As a result, the generated signal is a closer representation of a natural signal, as shown in Figure 11. A K&L Microwave bandpass filter is used as a L1 reconstruction filter, and the specifications are shown in Table 2.

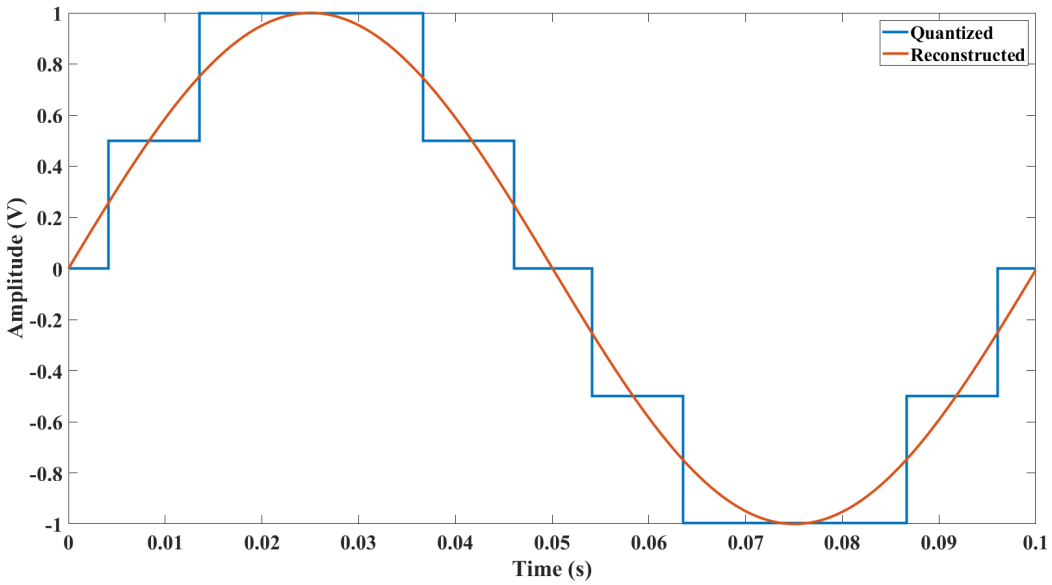

Figure 11. Reconstruction Filter Effects

Table 2. Reconstruction Filter Specification [26]

Description	Specification
Manufacturer	K&L Microwave
Model	6C45-1575.4/T32-O/O
Center Frequency	1575.4 MHz
3.0 dB Bandwidth	32 MHz
Insertion Loss	1.2 dBa
Stopband Attenuation (920 MHz)	193 dBc
Stopband Attenuation (1600 MHz)	20 dBc
Filter Type	Cavity
Return Loss	14 dB (1.5:1 VSWR)
Typical Ultimate Rejection	2363.1 MHz
Dimensions (English)	5.20 x 1.00 x 2.31 inches
Dimensions (Metric)	132.08 x 25.40 x 58.67 mm

2.6.3 FPGA Overview.

An FPGA is a volatile integrated circuit. It is a series of configurable logic blocks (CLBs), Digital Signal Processing (DSP) slices, Random Access Memory (RAM), and clock managers interconnected to each other through a switch matrix in a grid pattern. The switch matrix has transistors to determine the data path. The transistors and configuration modes are set by voltages. Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (HDL) or VHSIC Hardware Description Language (VHDL) and Verilog are HDL used to set the voltages to the transistors inside of the FPGA.

CLB slices consist of multiple flip flops, LUTs, arithmetic units, and multiplexors. DSP slices are dedicated components that can be used to implement fully parallel algorithms. Multiply, multiply accumulate (MACC), and multiply add are dedicated resources inside a DSP slice. Using DSP slices instead of CLB for these operations reduces the routing effort, reduces the amount of resources used, and allows operation at a higher clock rate.

2.6.3.1 FPGA Board.

The Xilinx ML605 Connectivity Kit is an FPGA development board designed for rapid prototyping of high-performance applications [27]. The kit is used in wired telecommunications, wireless infrastructure, broadcast, etc. The board has the following devices [28]:

- Xilinx Virtex-6 XC6VLX240T-1FFG1156 FPGA
- 512 MB DDR3 Memory SODIMM
- 128 Mb Platform Flash XL
- 32 MB Linear BPI Flash

- System ACE CF and CompactFlash Connector
- USB JTAG
- 200 MHz Fixed Oscillator
- Multi-Gigabit Transceivers
- 10/100/1000 Tri-Speed Ethernet PHY
- USB-to-UART Bridge
- User I/O
- VITA 57.1 HPC and LPC FMC Connector

2.6.3.2 Xilinx Virtex-6 XC6VLX240T FPGA.

The FPGA board consists of the Xilinx Virtex-6 FPGA. Each CLB slice contains four LUTs and eight flip flops. The DSP slices inside the Xilinx FPGA are called DSP48E1 slices. Each DSP48E1 slice contains a 25 x 18 multiplier, an adder, and an accumulator. 18 kb and 36 kb are the two types of block RAM that are available. Mixed-Mode Clock Managers (MMCM) are the clock managers for the FPGA [29]. The resources for the FPGA are listed on Table 3.

Table 3. Xilinx Virtex-6 XC6VLX240T Resources [29]

Resource	Quantity
Logic Cells	241,152
CLB Slices	37,680
DSP48E1 Slices	768
18 kb Block RAM	832
36 kb Block RAM	416
MMCM	12

III. SatNav Flexible Architecture Testbed

Chapters I and II discussed the rigidity of the current SatNav architecture and the need for a flexible SatNav architecture to adapt to counter potential threats to the system. The flexible SatNav architecture must also be used to test new signals concepts and determine its impact on current GPS receivers. Since the use of GPS receivers is ubiquitous, minimizing impact on current receivers is critical. GNSS Waveform Prototyping Platform (GWPP) is a testbed to evaluate the flexible SatNav architecture and new signals concepts.

3.1 Digital System Architectures

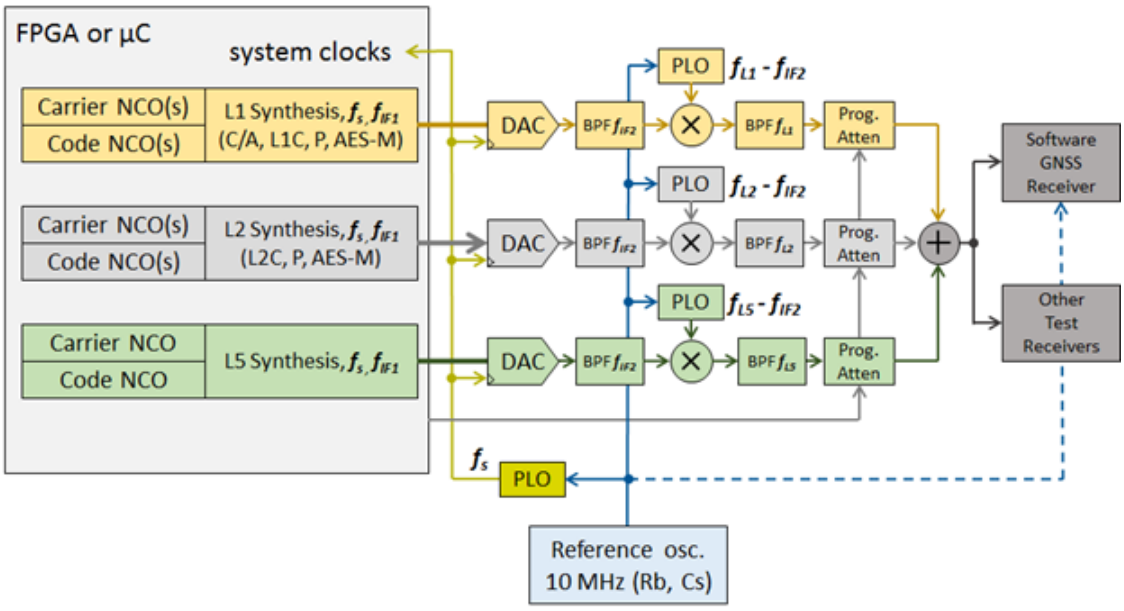

Figure 12. Typical Digital System Architecture

A typical digital system architecture, shown in Figure 12, is a flexible architecture, but its capabilities are limited in generating complex signals. It uses an FPGA or microcontroller (uC) to generate signals at baseband. The signals are sent to a small instantaneous bandwidth DAC, then through an analog reconstruction filter.

Afterwards, the reconstructed signal is upconverted to RF and then to another filter. The signal then goes through a programmable attenuator to set its appropriate gain levels and finally is combined with other signals before being sent out to the antenna.

Since the signal is generated at baseband, multiple DAC and analog upconversion chain is needed. The only advantage of this system architecture is the low power consumption. There are several disadvantages to this system architecture. First, the DAC has a small instantaneous bandwidth. Generating complex signals, such as Military (M) or L1C code, requires a large instantaneous bandwidth, which the DAC is not able to support. Secondly, the analog components for each signal may have different group delays, causing transients to form on the combined signal. Third, the amount of real-estate needed to support the components is large. Finally, aging of analog components is an issue and performance will tend to decrease over time [30].

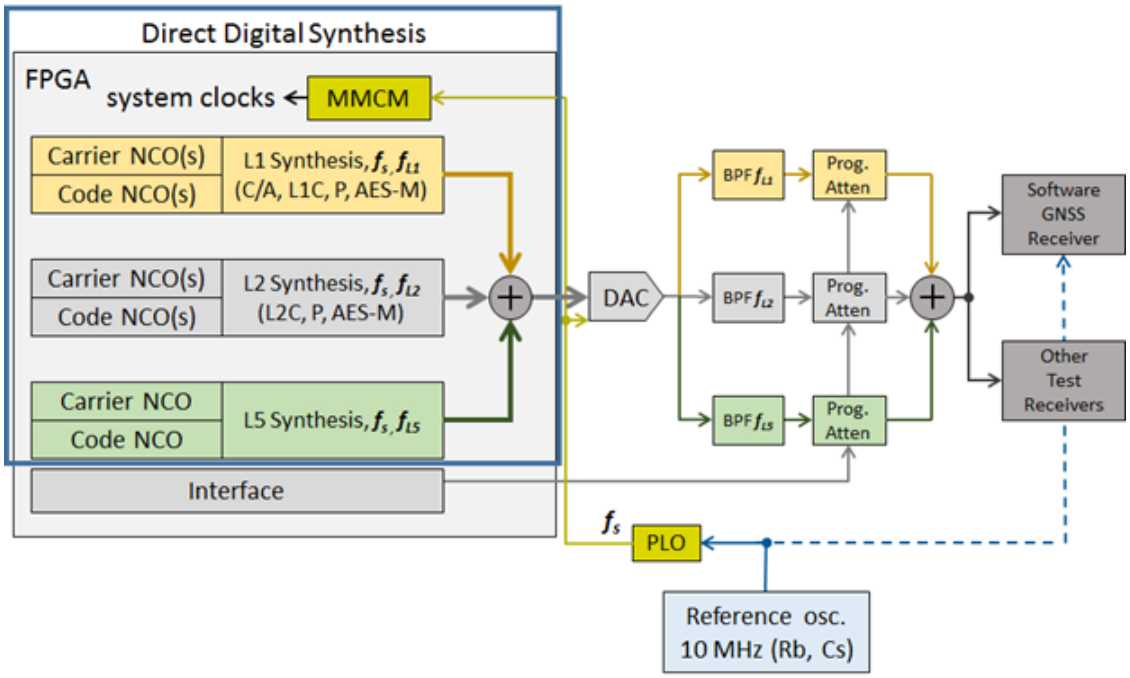

Figure 13. Proposed Digital System Architecture

The proposed system architecture, as shown in Figure 13, uses an FPGA and a large instantaneous bandwidth DAC. Since the signal is being generated at RF inside

the FPGA, there is not any need for an analog upconversion chain. By eliminating the analog upconversion chain, real-estate of the entire design is decreased. However, reconstruction filters for each frequency are still required. The group delay of each frequency still exists because of the filters, but the delays can be eliminated by careful calibration within the FPGA.

3.2 DDS Architecture

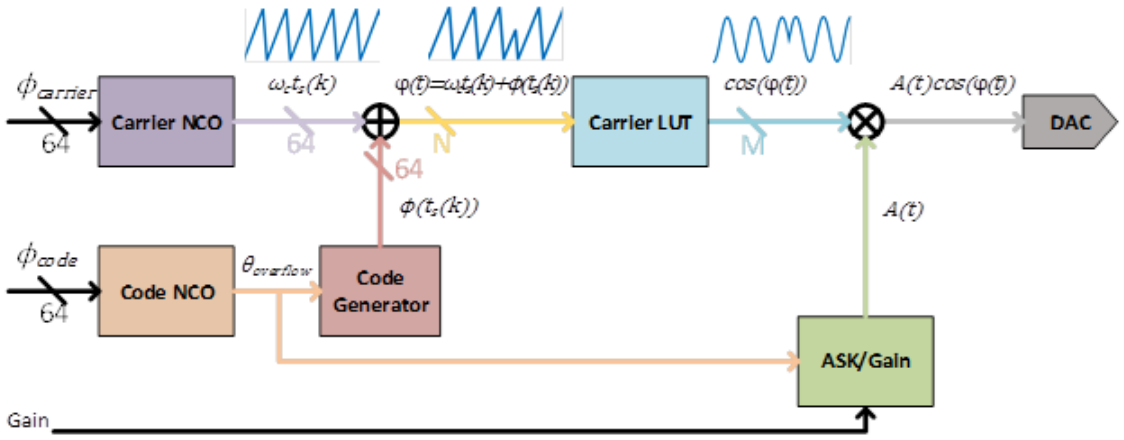

Figure 14. DDS Architecture for Testbed

The DDS architecture, shown in Figure 14, is implemented in the FPGA. The Carrier and Code Numerically Controlled Oscillators (NCOs) generates the phase of a rate using

$$\phi = round\left(2^{64} \cdot \frac{f_c}{f_s}\right), \qquad \text{for } f_c \leq \frac{f_s}{2}. \tag{8}$$

The NCO generate the phase for the carrier and trigger for the Code Generator. Each NCO consist of 64-bit accumulators, shown in Figure 15, to provide precision for any small adjustments in phase. The Code NCO triggers the Code Generator when an overflow condition happens with the accumulator within the NCO.

The Code Generator can be a pattern memory with software-defined values or an algorithm to generate the code. In this case, the Code Generator is the algorithm and

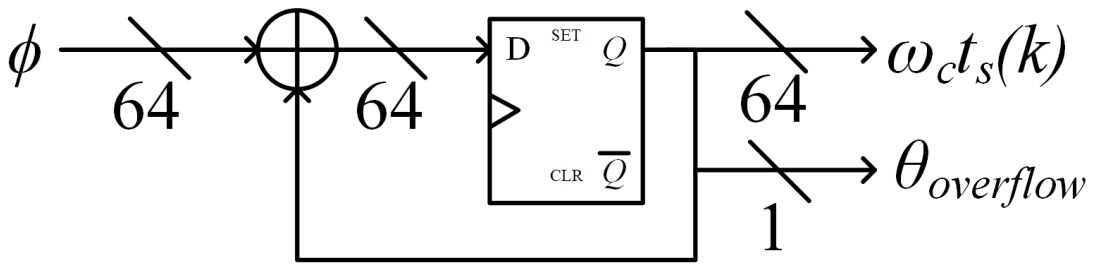

Figure 15. Phase NCO Design

consist of two 10-bit LFSRs, shown in Figure 8, to generate code for L1 C/A. Since the L1 C/A signal is a BPSK modulated signal, the phase for the code must change from 0 degrees to 180 degrees and vice versa. The modulated phase offset is added to the carrier phase. The Carrier LUT consist of one period of a quantized sine wave. The modulated phase is used as an address to the Carrier LUT. The output of the Carrier LUT is a modulated sine wave for the L1 C/A signal.

3.3 Parallel Pipeline Synchronization

The DDS architecture produces signals at RF, and the minimum sample rate for the architecture must be twice the L1 frequency of 1575.42 MHz. Navigation satellites, including GPS, transmit in the L band. To increase flexibility, the DDS architecture must cover the entire L band. To cover L band, the sampling rate should be at 4000 MegaSamples Per Second (MSPS).

FPGAs and uCs can not produce samples at 4000 MSPS sequentially but can produce multiple samples simultaneously. The number of simultaneous samples at a given clock rate must be equal to the sampling rate of the DAC, otherwise an over or under-flow condition may occur. Table 4 shows the number of simultaneous samples at a specific clock rate to match the required sampling rate of 4000 MSPS. With the AD9129 in "Mix-Mode", only half of the sampling rate is required. Table 5 shows the number of simultaneous samples at a specific clock rate to match the required

sampling rate of 2000 MSPS.

Table 4. Clock Rate Requirement for 4000 MSPS

Sampling Frequency (MSPS)	Clock Rate (MHz)	Simultaneous Samples
4000	1000	4
4000	500	8
4000	250	16
4000	125	32

Table 5. Clock Rate Requirement for 2000 MSPS

Sampling Frequency (MSPS)	Clock Rate (MHz)	Simultaneous Samples
2000	1000	2
2000	500	4
2000	250	8
2000	125	16

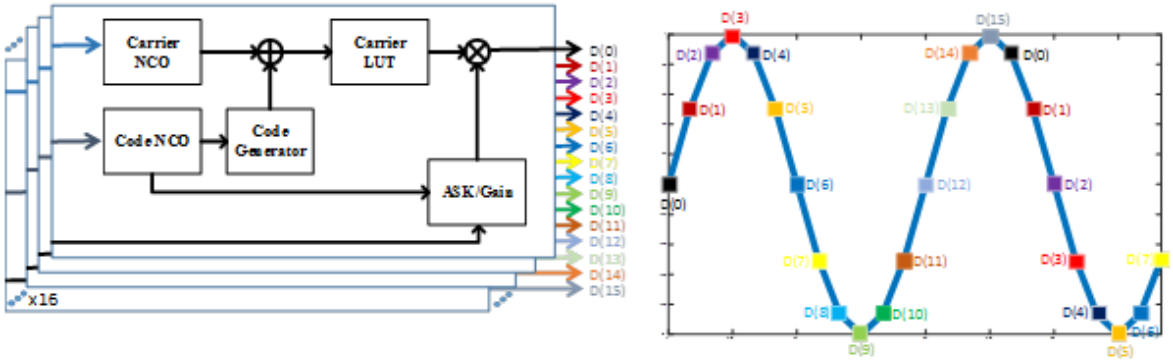

Figure 16. Parallel Pipelines

The disadvantages of increasing simultaneous samples for lower frequency is a higher resource utilization cost for design duplication, shown in Figure 16, and a complex synchronization scheme to generate sequential samples in parallel. The NCO

step size for each parallel pipeline stage must be

$$\Delta = N \cdot \phi \tag{9}$$

where N is the total number of parallel pipeline stages and Δ is the step size for the NCO. Each parallel pipeline stage must be initialized with an offset value y_n for pipeline n using Equation (10) to prevent any kind of discontinuity of the generated signal.

$$y_n = \varphi + n \cdot \phi \ , n \in \{0, 1, ..., N-1\} \tag{10}$$

where n is the number of pipeline stages, φ is the initial phase of the cosine wave, and y_n is the initialization value of each parallel pipeline stage. In cases where the NCO step size must be updated on a regular basis for doppler applications, reinitialization of the NCO with the new step size results in discontinuity of phase of the signal. By using Equation (13) to calculate initialization values for each NCO in each parallel pipeline stage, the phase remains continuous for every NCO step size adjustment.

$$\phi_\Delta = \phi_{new} - \phi_{old} \tag{11}$$

$$\varphi_\Delta = \varphi_{new} - \varphi_{old} \tag{12}$$

$$y_{n,new} = \varphi_\Delta + \phi_\Delta \cdot (n+1) + \Delta_{old} \ , n \in \{0, 1, ..., N-1\} \tag{13}$$

3.4 Verification

GWPP is a testbed to evaluate the flexible SatNav architecture and new signals concepts. Tests are conducted to determine how well it performed compared against commercially available GPS simulators. Two COTS and one GOTS receivers are used to take raw measurements of the signal and determine if the receivers derive a

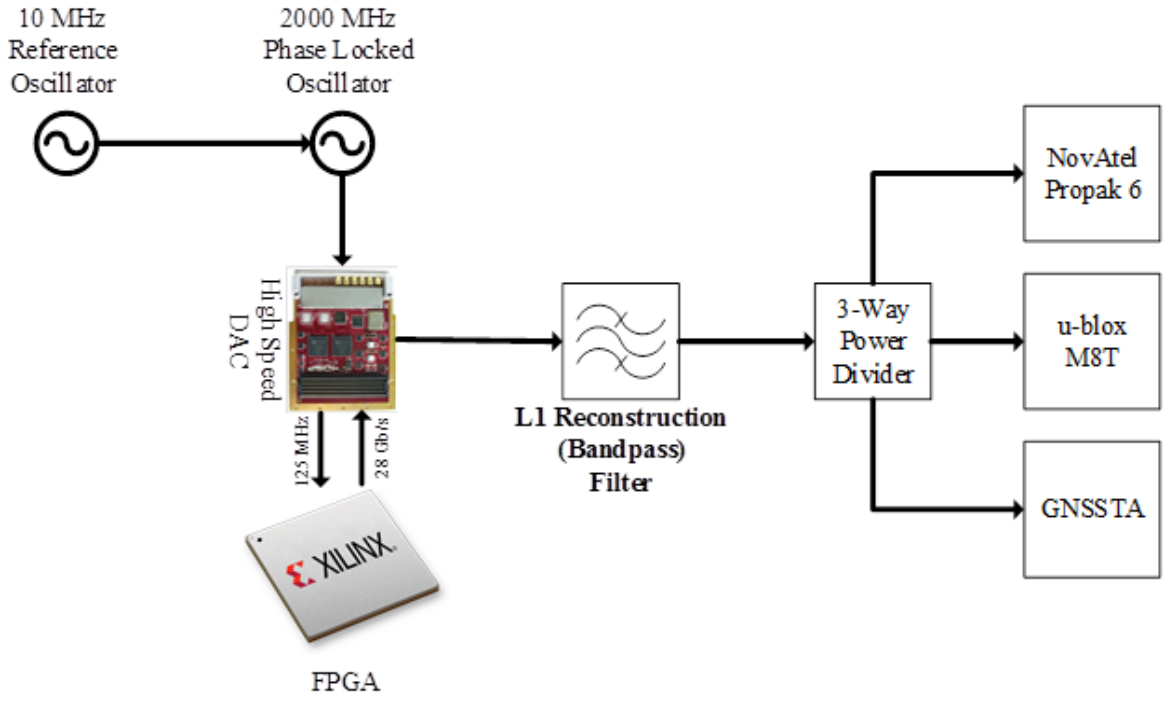

Figure 17. GWPP Testbed

position solution. A comparison of cost, size, weight, and power is done to determine if GWPP is viable alternative solution for a GPS simulator.

GWPP incorporates a DDS architecture to generate GPS signals. Three receivers are used to record raw measurements of the signal and determine if the signal generation meets GPS specification. The NovAtel Propak 6 and u-blox M8T COTS receivers and Global Navigation Satellite System Test Architecture (GNSSTA) GOTS receiver are non-participating receivers used to verify the functionality of GWPP. Figure 17 shows the verification set up for GWPP. A three-way power divider is used to split the GPS signal into three signal paths for each receiver.

The Rohde & Schwarz SMBV100A Vector Signal Generator and Spirent GSS8000 are commercially available products. The performance of these products is compared with GWPP. The set up is similar to Figure 17, but the commercial product is connected to the three-way power divider.

GPS receivers provide a position solution with four different satellite vehicles

(SVs). Within the FPGA, a DDS architecture is required for each SV. Each SV has its own doppler profile and navigation message. Without the navigation message and doppler profile, the receivers will not be able to provide pseudoranges or accurately track the signal.

Realistic doppler and navigation message information for each SV can be found on National Aeronautics and Space Administration (NASA) website `ftp://cddis.gsfc.nasa.gov/gnss/data/hourly/`. Doppler and navigation message information for PRN 16, 23, 27, and 29 at date and time of 11/20/2016 at 02:35:06 AM for coordinates 39.782753 North, -84.082292 West are extracted and fed into GWPP and the commercial products.

3.5 Results

GPS receivers have internal algorithms to check the validity of signals being received from each SV. Once the signals have been verified, the results are shown in their respected user interface, shown in Figures 18 - 26. Figures 18 - 20 show the location of each SV in the sky in relation to the receiver. As shown, all three receivers are providing the same results. Figures 21 - 23 show the carrier-to-noise ratio (C/N_0) values for each SV. The C/N_0 for each receiver vary slightly because the algorithm and the RF front-end used to calculate C/N_0 is unique to each receiver. Figures 24 - 26 show similar position solution of each receiver. However, there is an error in the position solution because the code phase is not properly aligned with navigation message. In later experiments, the delay to the navigation message was adjusted and it had an effect with the position solution.

3.6 Conclusion

The DDS architecture adds flexibility to the signal generation capability. GWPP has demonstrated the capability of the DDS by being able to generate multiple SVs on a single platform. In later experiments, GWPP was able to generate multiple types of signals on single SV while the signal maintained a constant envelope [31]. GWPP also demonstrated software-defined capability of the DDS architecture by being able to adjust transmitter configurations in real-time using a software interface.

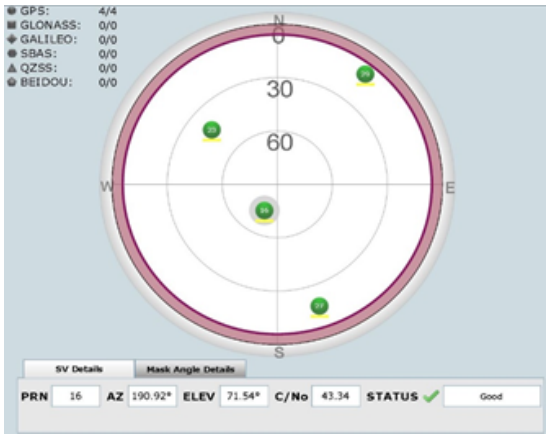

Figure 18. NovAtel Propak 6 Sky Plot

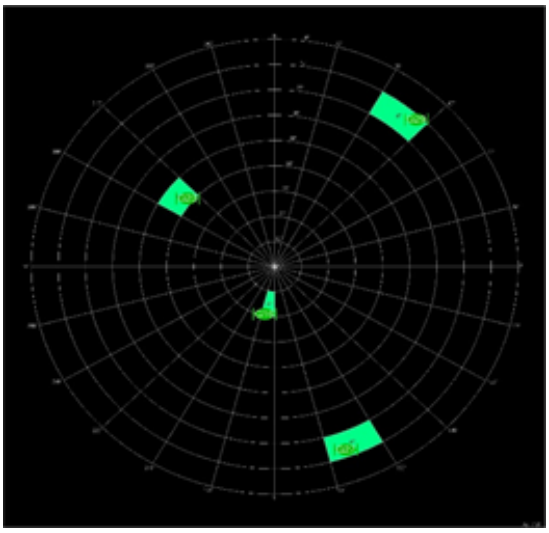

Figure 19. u-blox M8T Sky Plot

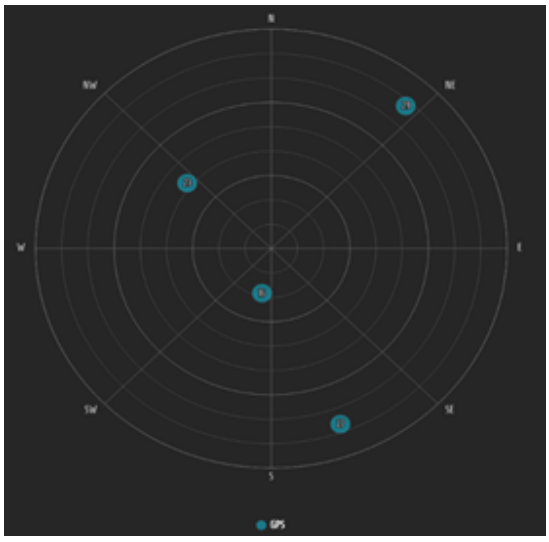

Figure 20. GNSSTA Sky Plot

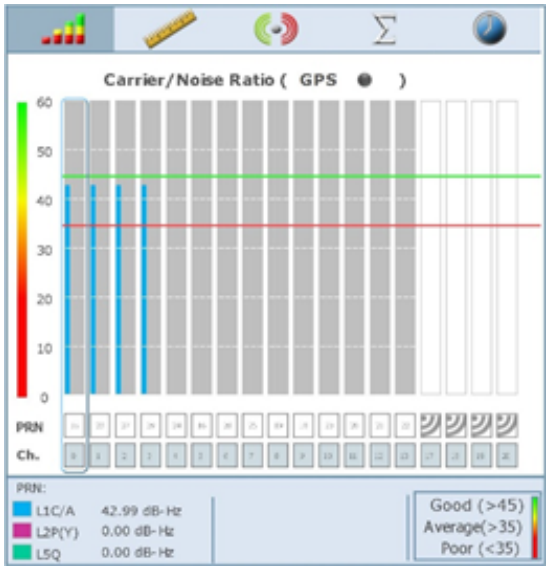

Figure 21. NovAtel Propak 6 Carrier/Noise Ratio

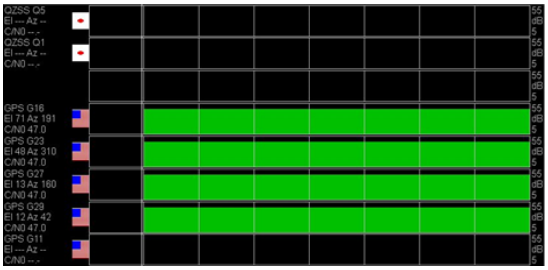

Figure 22. u-blox M8T Carrier/Noise Ratio

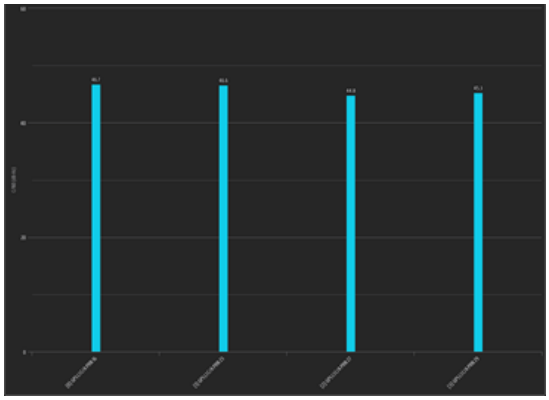

Figure 23. GNSSTA Carrier/Noise Ratio

Latitude	39.77888295°	+/-	2.77m
Longitude	-84.09177392°	+/-	5.32m
Hgt. (MSL)	-413.414m	+/-	6.99m

Solution type	Single
Iono correction	Unknown
Advanced RTK	N/A
Solution age	0 second
Differential age	0 second

# of satellites	4
Used in solution	GPS L1 L2 L5
	GLO L1 L2
	GAL E1
	QZS L1 L2 L5
	BDS B1 B2 B3

Solution status	Computed

Sun 20/11/2016 02:36:00 GMT
Sat 19/11/2016 22:36:00 Local

Figure 24. NovAtel Propak 6 Position Solution

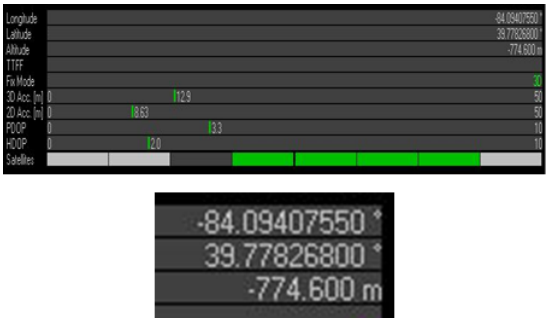

Figure 25. u-blox M8T Position Solution

Figure 26. GNSSTA Position Solution

IV. Phase Noise and Quantization Effects and Modeling

Phase noise and quantization error effects have an impact on the quality of the desired signal. Phase noise causes an increase in the noise floor causing difficulty of detecting weak signals. Quantization errors causes an increase of in-band spurious emissions and decrease in total signal power. Phase noise causes random deviations of instantaneous phase or frequency [32]. This deviation diminishes the achievable received C/N_0. Usually longer integration intervals can be used to compensate for the diminished C/N_0, but phase noise is translated into a rotation of the constellation diagram of a modulated signal which would make integration and demodulating the desired signal less effective.

The reference oscillator, phase locked oscillator, and DAC are contributors to phase noise. The reference oscillator sets the baseline phase noise figure. The phase locked oscillator uses the reference oscillator to generate the sampling frequency clock of the digital system. The clock is used in the FPGA to generate the discretized values of the signal. The DAC converts the discretized signal into an analog representation of the desired signal. The phase noise is carried and accumulated throughout the entire signal generation process.

Quantization errors are caused by the incorrect mapping of digital values of a signal to its analog representation form. The higher the resolution of the digital values, the lower the quantization errors. The lower the resolution of the digital values, the higher the quantization error. Since the mapping is not precise, as shown in Figure 11, there is an effect on the total power of the desired signal and in-band spurs are generated. The power from the mapping error is distributed from the desired signal to the in-band spurs.

The DDS architecture within GWPP, shown in Figure 14, has an impact on quantization error. The Carrier LUT contains one period of a sine wave. The phase

steps and values of the Carrier LUT are quantized to minimize resource utilization inside the FPGA. This quantization of steps and values causes an increase on in-band spurious emissions while reducing the total power of the desired signal.

This chapter will compare the measured phase noise of GWPP and the phase noise of the operational SatNav systems. Afterwards, we examine the effects of quantization when applied to the phase and amplitude. The end-to-end numerical and mathematical modeling of the DDS architecture, and the comparison of quantization error between the models will also be included in this chapter.

4.1 Phase Noise Modeling

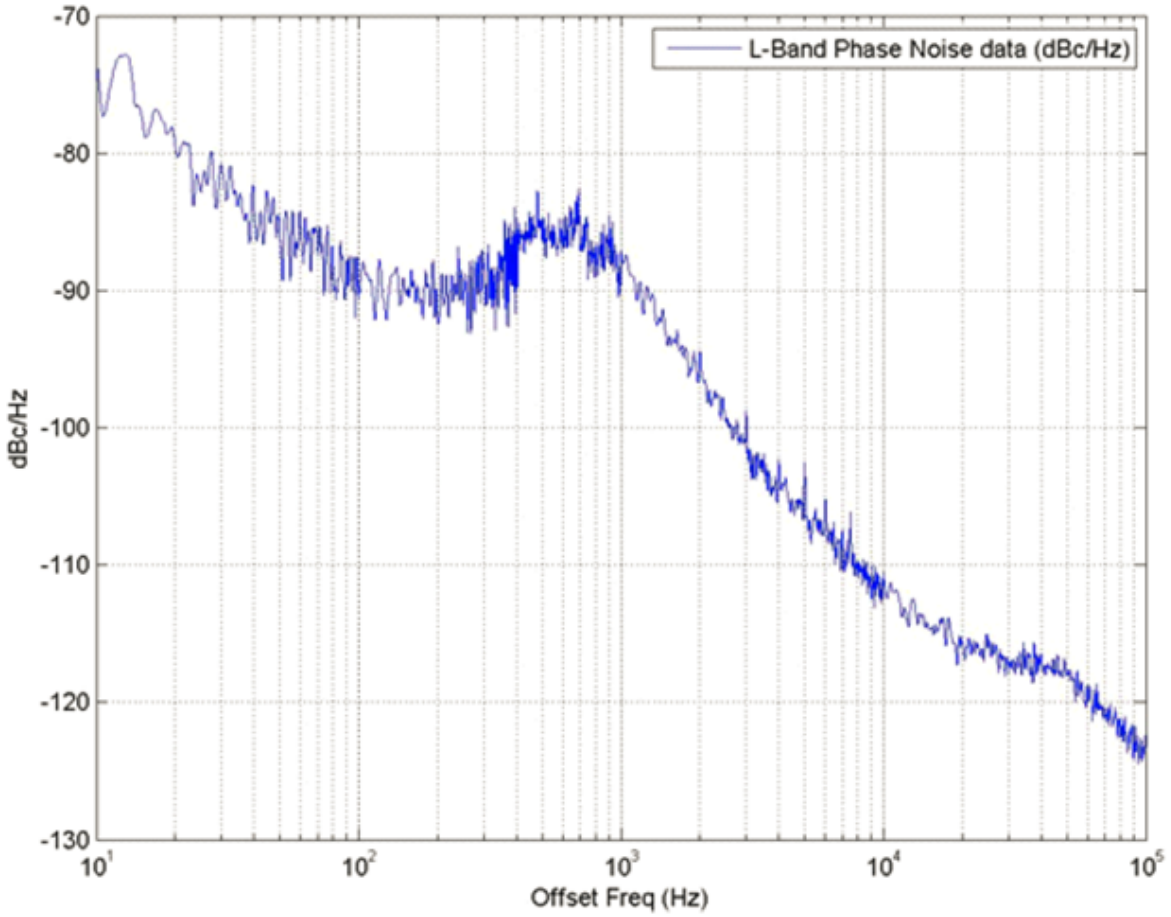

Figure 27. Phase Noise of GPS III L1 Signal [33]

GWPP is a testbed to evaluate the flexible SatNav architecture and new signals concepts. In Chapter III, it was shown that COTS and GOTS receivers can acquire and track the GPS signal generated from GWPP. However, it did not show the quality of the desired signal. Signal quality is evaluated by analyzing the single sideband phase noise of the signal. Close-in, pedestal, and far-out refer to the regions in the phase noise measurements. Close-in phase noise refers to 1 Hz to 1 kHz from f_c. Pedestal is the area between 1 kHz to 100 kHz from f_c. Far-out area refers to the area beyond 100 kHz [34]. For this research, the close-in phase noise of GWPP is evaluated to determine if any phase noise, from the individual active components in the signal generation path, is being introduced into the desired signal.

The close-in phase noise performance of GWPP is compared with that of the latest GPS satellite. GPS III launched late 2019, and its phase noise is shown in Figure 27. For GWPP to comply as a testbed for GPS signals, it must meet or outperform the performance of phase noise on the latest GPS satellites.

4.1.1 Data Collection Equipment.

To evaluate the phase noise of the system, the performance of the test equipment and components must exceed the performance of the system under test by 10 dB of power at every offset frequency. An ultra-low phase noise reference oscillator, signal generator, and a signal analyzer is needed to evaluate the performance of the phase noise.

An ultra-low phase noise reference oscillator is an important component to the system. It sets the baseline for phase noise, and the phase noise from the reference oscillator is propagated through the entire system. After conducting a market survey of various reference oscillator, it was determined 501-27503-35 from Wenzel Associates, Inc. met the 10 dB difference of power requirement for measuring phase noise, shown

in Table 6.

Table 6. 10 MHz Reference Oscillator Phase Noise [35]

Offset Frequency (Hz)	dB/Hz
1	-113
10	-143
100	-161
1000	-173
10000	-174
100000	-175

A signal generator is needed to generate the sampling clock for GWPP. Keysight N5182B Vector Signal Generator was chosen because of availability, and it had the lowest phase noise in the market in late 2019. Using the internal reference oscillator, the phase noise of the signal generator is listed in Table 7.

Table 7. Signal Generator Phase Noise [36]

Carrier Frequency (Hz)	1 Hz	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz
1 GHz	-70	-97	-106	-136	-146	-143
2 GHz	-65	-90	-101	-131	-140	- 137

A signal analyzer is needed to acquire the generated signal at baseband. The signal analyzer will collect I/Q data over a period of time. A Keysight N9030B Signal Analyzer was chosen because of availability, and it had the lowest phase noise in the market. Using the internal reference oscillator, the phase noise of the signal analyzer is listed in Table 8.

Table 8. Signal Analyzer Phase Noise [37]

Deviation from 1 GHz Carrier Frequency	dB/Hz
10 Hz	-95
100 Hz	-112
1 kHz	-129
10 kHz	-136
100 kHz	-141

4.1.2 Phase Noise Verification Process.

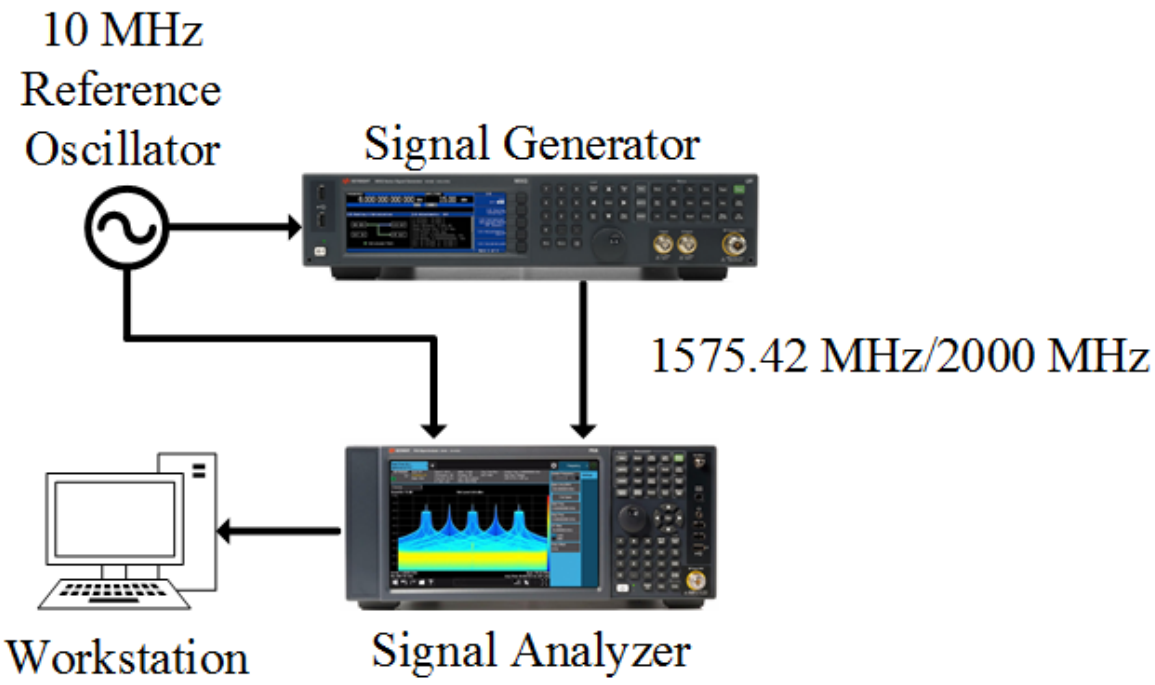

Figure 28. Phase Noise Evaluation of Signal Generator

Multiple components and equipment are needed to examine phase noise of GWPP. Each component and equipment produce its own phase noise, and is introduced into the phase noise measurements of GWPP. The first part of the two part verification process is to measure the phase noise of the test equipment generating a signal at L1

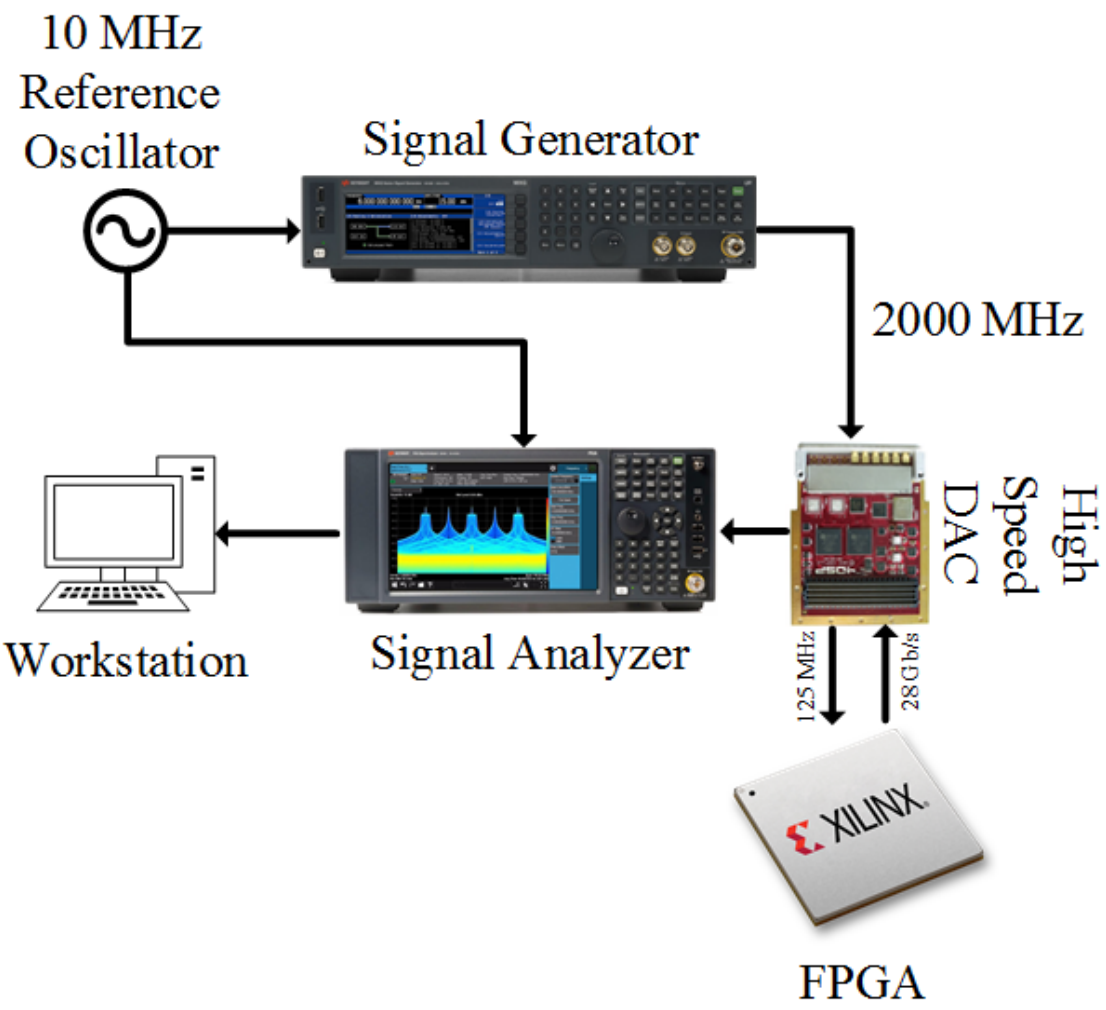

Figure 29. Phase Noise Evaluation of GWPP

and the sampling frequency of GWPP, shown in Figure 28. The second part is to measure the phase noise of GWPP with the test equipment, shown in Figure 29. Once the measurements are taken, they will be compared to each other. The differences will be compared with the phase noise of GPS III system, shown in Figure 27.

4.2 DDS and Mathematical Modeling of Quantization Error and Effects

4.2.1 Notation.

To analyze the numerical and mathematical DDS models, some notation is needed to describe the modeled architecture.

Table 9. DDS Specific Variables

Variable	Description	Variable	Description
$\mathbf{b}$	binary vector	N	total sample size
b_0	MSB of $\mathbf{b}$	q	number of fractional bits
B	total bits	r	number of integer bits
i	bit index	s	unsigned or 2's complement
j	NCO accumulator size	X_m	scale factor
k	phase resolution	μ	upsample rate
n	discrete sample	ν	downsample rate

4.2.2 Overview.

A DDS and mathematical models are developed in a simulation environment to understand the quantization error caused by truncation of the phase and amplitude of a signal. Having both models in a simulation environment allows for a closer examination of the signal generation process. Reference [5] documents the results of the simulated DDS model, and it is comparable to the results from the captured signal from GWPP. The noise floor of the test equipment is higher than the simulated model, therefore many low power signals will not be seen on the test equipment. The models developed in the simulation environment provide a better platform to analyze quantization error.

There are two sections in the DDS model. The first section analyzes the effects of

phase quantization of the signal. The second section analyzes the effects of amplitude quantization of the signal. The mathematical model analytically describes the entire DDS model. Variables in Table 9 are used in the models.

Designing a DDS model with a 64-bit NCO on a system with a 64-bit Intel processor poses a problem because the model uses a combination of double-precision floating-point and 64-bit integer values. Traditionally, Intel-based processors use the IEEE-754 standard to represent a floating-point number. In the standard, the MSB is the sign bit of the number, while the next 11 bits are for the exponent. The final 52 bits Least Significant Bits (LSBs) are the normalized mantissa. The word size of the mantissa restricts the numerical precision of a number.

Software applications overcome this limitation by distributing the value into multiple registers on the processor. Each register is calculated independently and the outputs are added together [38]. This functionality is available in the Fixed-Point Designer toolbox of Mathworks MATLAB, but the implementation details are proprietary. For this effort, the DDS and mathematical models utilize the MATLAB toolbox.

4.2.3 DDS Model.

4.2.3.1 Phase Quantization.

The NCO generates the phase of the signal. The NCO consists of a 64-bit accumulator (j=64), and resolution of the NCO represents $\frac{1}{2^j}$ of a phase cycle of the signal. The step size of the accumulating rate generates the phase at a given frequency of the signal and is expressed by

$$\phi_{step} = round\left(2^j \cdot \frac{f_c}{f_s}\right), \qquad \text{for } f_c \leq \frac{f_s}{2}. \tag{14}$$

The round operation minimizes the amount of phase error that is introduced, and the equation to determine the maximum phase error in radians is expressed by

$$\phi_{stepError} = 2 \cdot \pi \cdot 2^{-j-1}. \tag{15}$$

The resulting phase is expressed in cycles that is normalized from 0 to $2^j - 1$ and is expressed by

$$x_{phase}[n] = n \cdot \phi_{step}, \qquad \text{for } 0 \leq n \leq 2^j - 1. \tag{16}$$

Afterwards, the phase is quantized to the appropriate word size ($k =$ word size). The phase is right shifted until the top k bits are remaining. The floor operation truncates the value once it has been shifted. The resulting quantized phase wraps at 2^k for the Read Only Memory (ROM), which will be discussed later, and is expressed by

$$x_{qphase}[n] = mod\left(floor\left(\frac{x_{phase}[n]}{2^{j-k}}\right), 2^k\right), \qquad \text{for } j \geq k. \tag{17}$$

Using Equation (15) with the accumulator of the NCO being 64 bits ($j = 64$), the error in phase is minuscule. Therefore, Equation (17) is simplified to a close approximation form of

$$x_{qphase}[n] = mod\left(floor\left(\frac{2^k \cdot f_c \cdot n}{f_s}\right), 2^k\right), \qquad \text{for } f_c \leq \frac{f_s}{2}, n \geq 0. \tag{18}$$

A ROM is used to store one period of a cosine signal with a sample length of 2^k. The period of the cosine signal is normalized and expressed by

$$x_{rom}[n] = cos\left(\frac{2 \cdot \pi \cdot n}{2^k}\right), \qquad \text{for } 0 \leq n \leq 2^k - 1. \tag{19}$$

Figure 30 shows the values from Equation (19), and these values are stored in a ROM.

The modulo operation in Equation (17) bounds the values within the sample size of

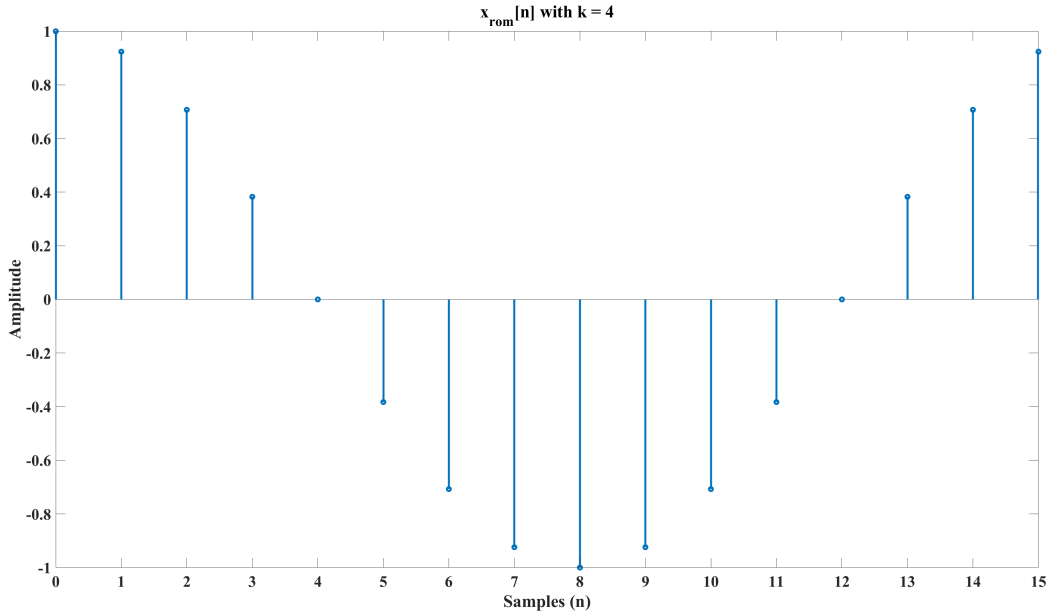

Figure 30. Stem Plot of ROM of a Single Period Cosine Wave

the ROM, shown in Figure 30. The signal is generated by picking out points from Equation (19) by using Equation (17) as the index, and this is expressed by

$$y_{signal}[n] = x_{rom}[x_{qphase}[n]]. \tag{20}$$

Figure 31 shows y_{signal} over 40 samples (n) with the phase incrementing by a value of 1, which is equivalent to $\frac{1}{16}$ of a period or $\frac{2 \cdot \pi}{16}$ radians. Figure 32 shows the phase incrementing twice as large, or at $\frac{4 \cdot \pi}{16}$ radians, over the same number of samples as Figure 31.

4.2.3.2 Amplitude Quantization.

The previous section did not consider the amplitude quantization of the values inside the ROM, Equation (19). In this section, the amplitude values of the signal are quantized or fixed-point, and the ROM consists of quantized values.

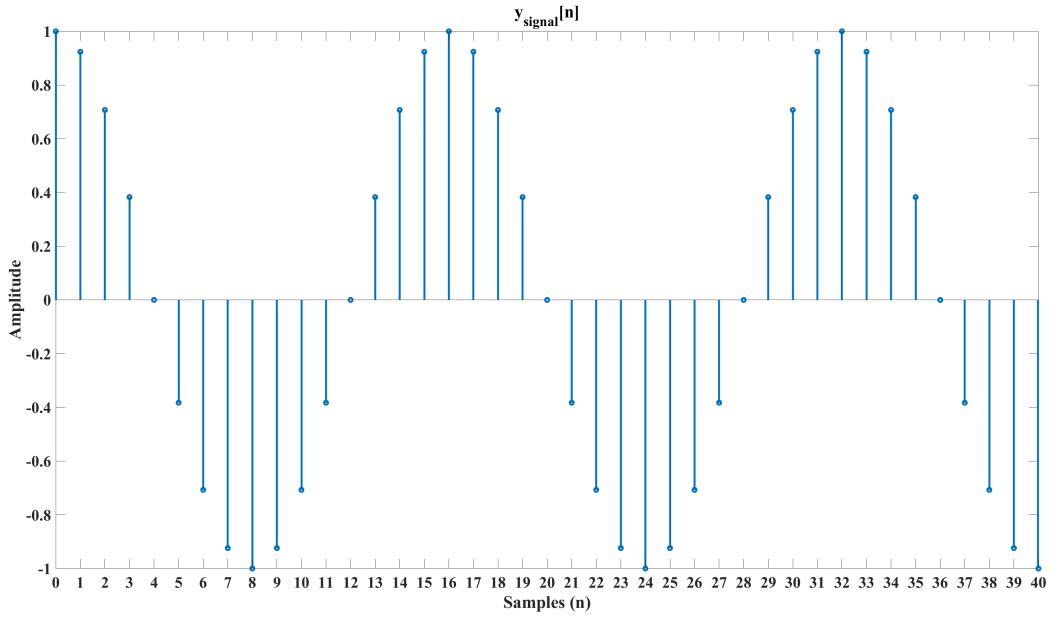

Figure 31. Stem Plot of y_{signal} Incrementing at $\frac{2 \cdot \pi}{16}$ radians

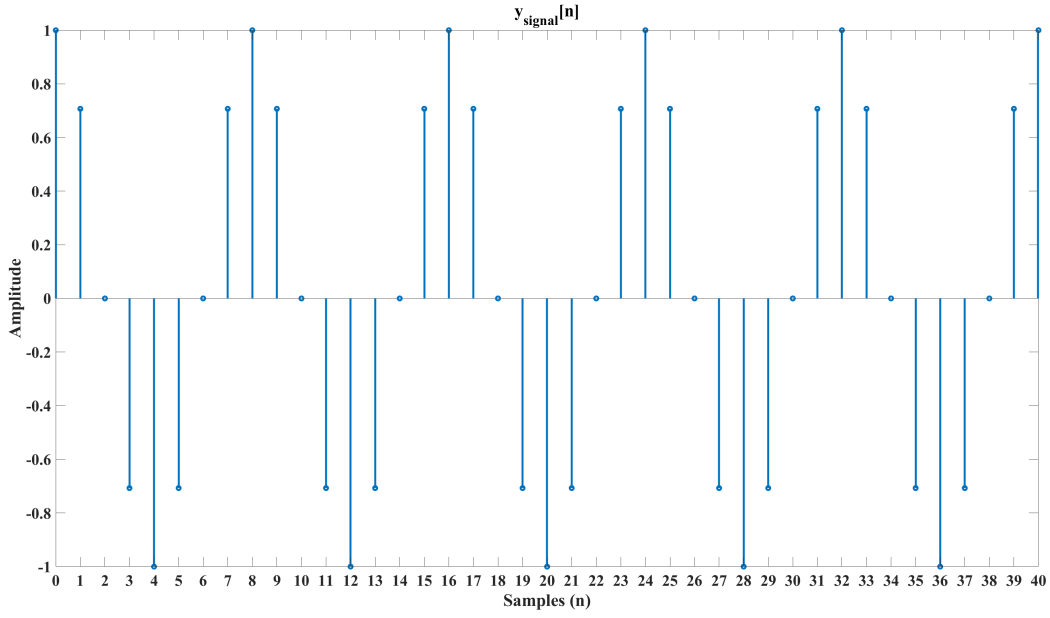

Figure 32. Stem Plot of y_{signal} Incrementing at $\frac{4 \cdot \pi}{16}$ radians

The type of number representation (s), number of integer bits (r) and number of fractional bits (q) define fixed-point value. The type of number representation determines if the value is either unsigned or 2's complement. If the value is an

unsigned number, 0 is used otherwise 1 is used. The total word size, stored in ROM, of the fixed-point value is

$$B = s + r + q. \tag{21}$$

The base-10 floating point cosine value from Equation (19) is converted to an integer form for storing in a ROM. First, the floating point value is converted to a base-2 or binary form. Next, the decimal point of the binary form is shifted right by the specified fractional bits (q). Finally, the value is rounded such that the signal is zero mean centered. This process is expressed by

$$x_{qrom}[n] = round\left(2^q \cdot x_{rom}[n]\right), \qquad \text{for } q \geq 0. \tag{22}$$

The phase of the signal, which is wrapped at 2^k or 2π, is used to look up the amplitude of the desired in the ROM and is expressed by

$$y_{signal}[n] = x_{qrom}[x_{qphase}[n]]. \tag{23}$$

The signal, from Equation (23), is quantized in phase and amplitude. Quantization causes spurious content to appear in the spectrum. The spurious content may potentially cause intermodulation distortion to the desired signal. A mathematical model is useful to explain these types of unpredictable behavior, as shown in Figure 33.

4.2.4 Mathematical Model.

A mathematical model is used to analytically explain the functionality of the DDS model. Also, it allows for an easier explanation of any kind of unpredictable behavior in the signal generation process.

Equation (24) is used to generate a cosine signal in the continuous time domain.

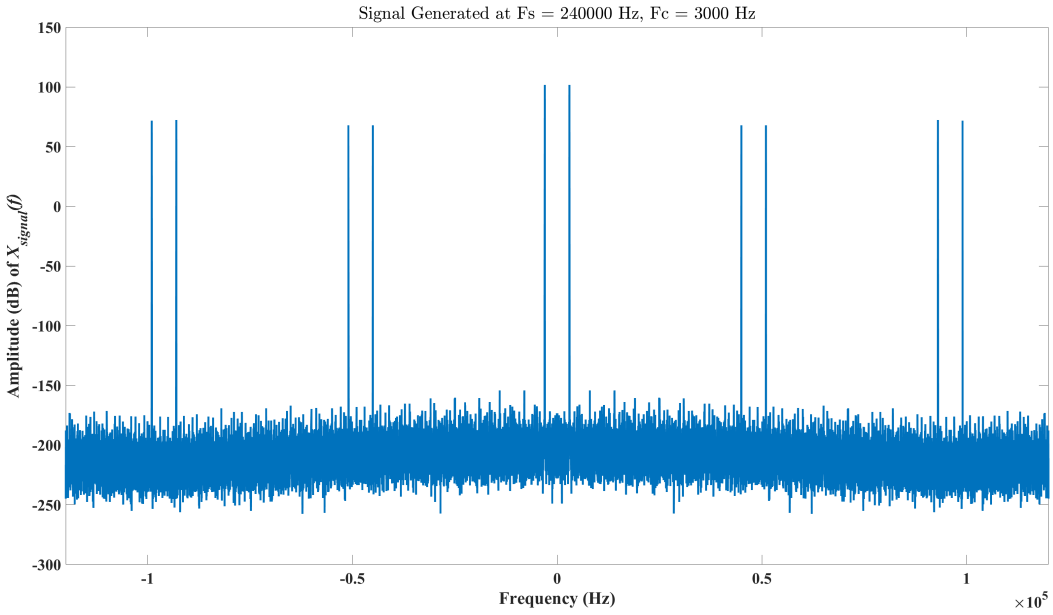

Figure 33. Spectral Plot of Signal with Spurs

A scale factor (X_m) is used to scale the cosine signal to the appropriate amplitude. f_c is the carrier frequency, and t is time. In the digital domain, each point in a cosine signal is generated at a specific interval. This specific interval is a sampling frequency (f_{sl}). The equation for the discrete signal generation of a cosine signal is expressed in Equation (25)

$$x(t) = X_m \cdot cos(2 \cdot \pi \cdot f_c \cdot t), \qquad \text{for } t \geq 0. \tag{24}$$

$$x[n] = X_m \cdot cos\left(2 \cdot \pi \cdot f_c \cdot \frac{1}{f_{sl}} \cdot n\right), \qquad \text{for } n \geq 0. \tag{25}$$

The phase resolution is restricted to the number of phase bits (k), therefore the values of the cosine signal must be increments of $\frac{1}{2^k}$. The sampling rate is expressed by

$$f_{sl} = f_c \cdot 2^k, \qquad \text{for } k \geq 0. \tag{26}$$

Equation (26) is substituted into Equation (25) as expressed by

$$x[n] = X_m \cdot cos\left(2 \cdot \pi \cdot f_c \cdot \frac{1}{f_c \cdot 2^k} \cdot n\right), \qquad \text{for } n \geq 0,\ k \geq 0, \tag{27}$$

which simplifies to

$$x[n] = X_m \cdot cos\left(\frac{2 \cdot \pi \cdot n}{2^k}\right), \qquad \text{for } n \geq 0,\ k \geq 0, \tag{28}$$

and the total energy in $x[n]$ is expressed by

$$e_{sl} = \sum_{n=0}^{N-1} |x[n]|^2. \tag{29}$$

The amplitude of the cosine signal is quantized by the total number of bits (B). The quantized sample is calculated by taking the base-10 number and converting it to a 2's complement binary number ($\mathbf{b}$). The MSB is the sign bit (b_0), where the value is multiplied by a negative one. The remaining bits are multiplied by the power of two raised to the location i of the bit and summed together. Next, this result is added together with previous operation and multiplied with a scale factor. The result is a quantized sample base-10 number, and is expressed by

$$\tilde{x}[n] = X_m \cdot \left(-b_0 + \sum_{i=1}^{B} b_i \cdot 2^{-i}\right). \tag{30}$$

The cosine signal is quantized by adding the individual samples with an quanitization error offset, and the value is scaled by a scale factor (X_m). The quantization error offset takes the difference between the true sample from the quantized sample is

expressed by

$$\epsilon_A[n] = \tilde{x}[n] - x[n], \qquad \begin{cases} -\frac{X_m \cdot 2^{-B}}{2} < \epsilon_A \leq \frac{X_m \cdot 2^{-B}}{2}, & \text{for rounding.} \\ -X_m \cdot 2^{-B} < \epsilon_A \leq 0, & \text{for truncation.} \end{cases} \tag{31}$$

Once the quantization error offsets are calculated it is added to the true samples, and is expressed by

$$x_A[n] = x[n] + \epsilon_A[n]. \tag{32}$$

For complete in-depth discussion on amplitude quantization, please see Reference [39].

Once the cosine signal is generated, and amplitude has been quantized, up and down sampling rates are calculated based on the phase resolution, sampling and carrier frequency parameters. This will adjust the cosine signal to the final sampling and carrier frequency. The upsampling (μ) to downsampling (ν) ratio is reduced to an irreducible fraction and is expressed by

$$\frac{\mu}{\nu} = \frac{f_{sh}}{f_{sl}}. \tag{33}$$

Upsampling and downsampling the signal with the Zero-Order-Hold (ZOH) operation mimics the phase quantization implemented in the DDS model. The ZOH operation is used with the upsampling rate is applied to the cosine signal in two stages. The first stage is to insert zeros to the signal as expressed by Equation (34) and shown in Figure 34.

$$x_u[n] = \begin{cases} x_A[n/\mu], & n{=}0,\ \pm\mu,\ \pm 2\mu,\ .... \\ 0, & \text{otherwise} \end{cases} \tag{34}$$

The total energy of the signal after being upsampled is the same as the original be-

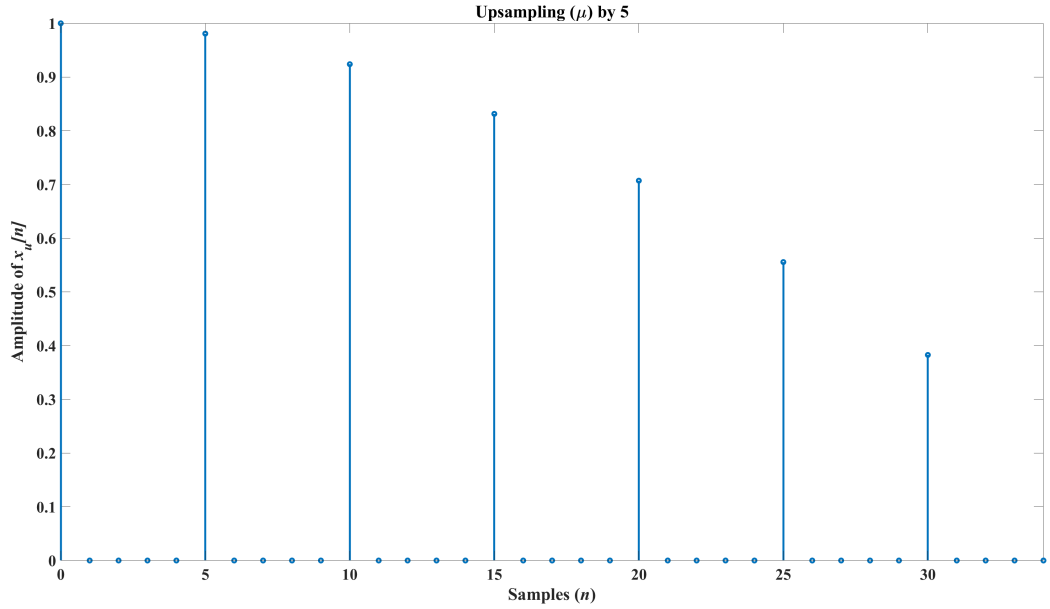

Figure 34. Upsampling of Signal

cause upsampling inserts zeros in-between the samples. The second stage convolves an impulse response signal from Equation (35) with the upsampled signal from Equation (34). Figure 35 shows the resulting signal.

$$h_{ZOH}[n] = rect\left(\frac{n - 0.5 \cdot \mu}{\mu}\right) \tag{35}$$

$$x_{ZOH}[n] = x_u[n] * h_{ZOH}[n] \tag{36}$$

ZOH operation replicates the individual samples by μ causing an increase in total energy and is expressed by

$$e_{ZOH} = \mu \cdot \sum_{n=0}^{N-1} |x[n]|^2. \tag{37}$$

After the ZOH operation, the signal is downsampled without any kind of pre-filtering. It is expressed by Equation (38) and shown in Figure 36. The downsampling operation causes the step widths to become non-uniform, as shown in Figure 36. The total

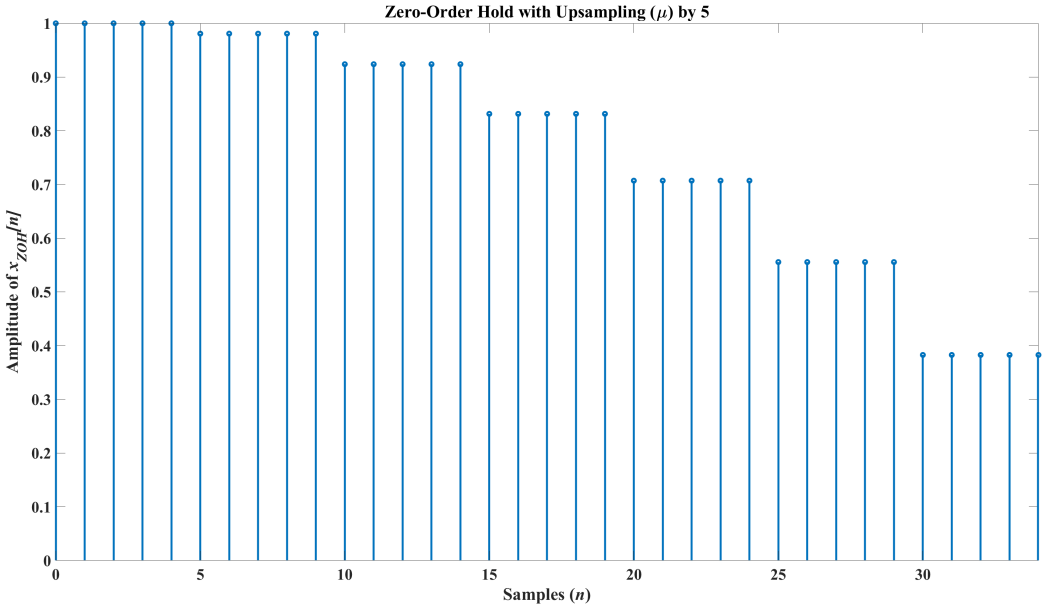

Figure 35. Zero-Order Hold of Signal

energy of the signal can be approximated by using Equation (39).

$$x_{signal}[n] = x_{ZOH}[n \cdot \nu] \tag{38}$$

$$e_s = \frac{\mu}{\nu} \cdot \sum_{n=0}^{N-1} |x[n]|^2 \tag{39}$$

4.3 Results of DDS and Mathematical Model Quantization Effects and Mathematical Solution

Figure 37 shows the spectral plot of Equation (28). The total energy of the signal is focused on the carrier signal. When the signal is upsampled by using Equation (34), the new sampling frequency is the upsampled rate multiplied by the original sampling frequency. The results of the upsampling causes the spectrum to be replicated by multiples of the original sampling frequency. This causes spurs to be generated in the

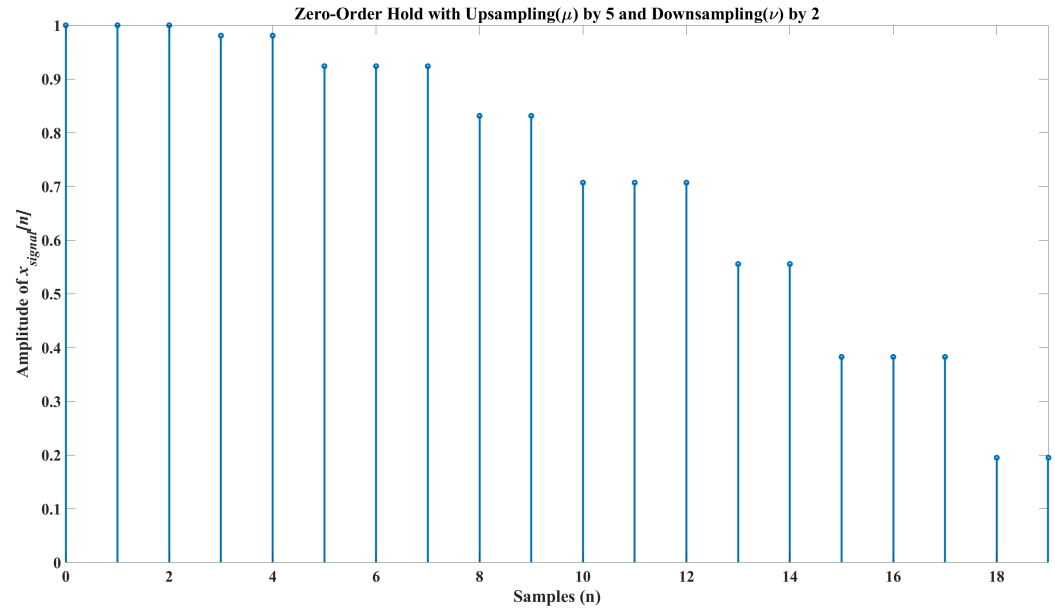

Figure 36. Downsampling of Signal

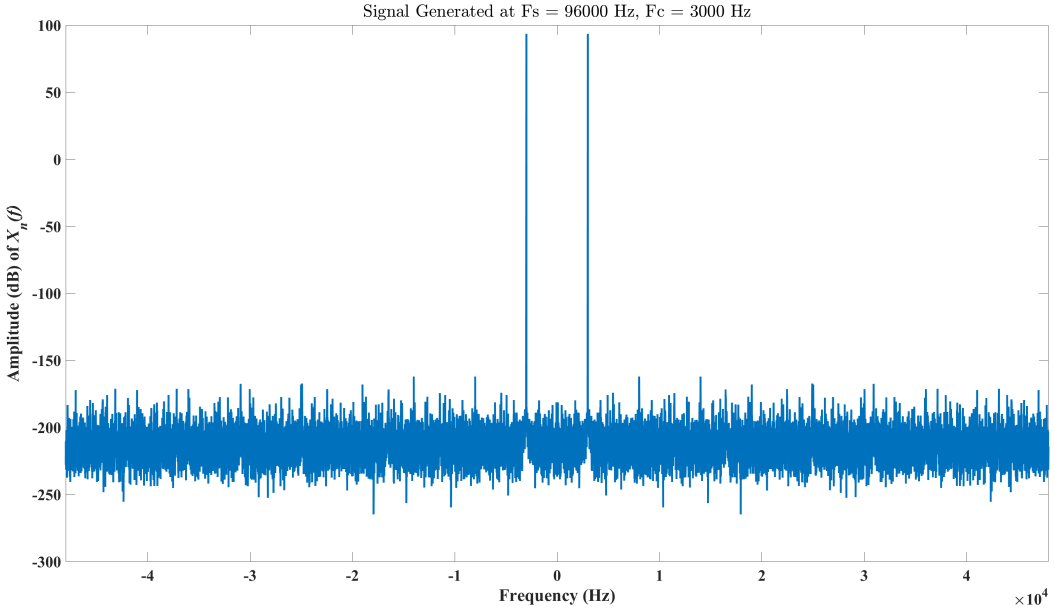

Figure 37. Spectral Plot of Baseband Signal

spectrum and is expressed by

$$x_{sup}[x_{si}] = x_{si} \cdot f_c \cdot 2^k, \qquad \text{for } x_{si} > 0. \tag{40}$$

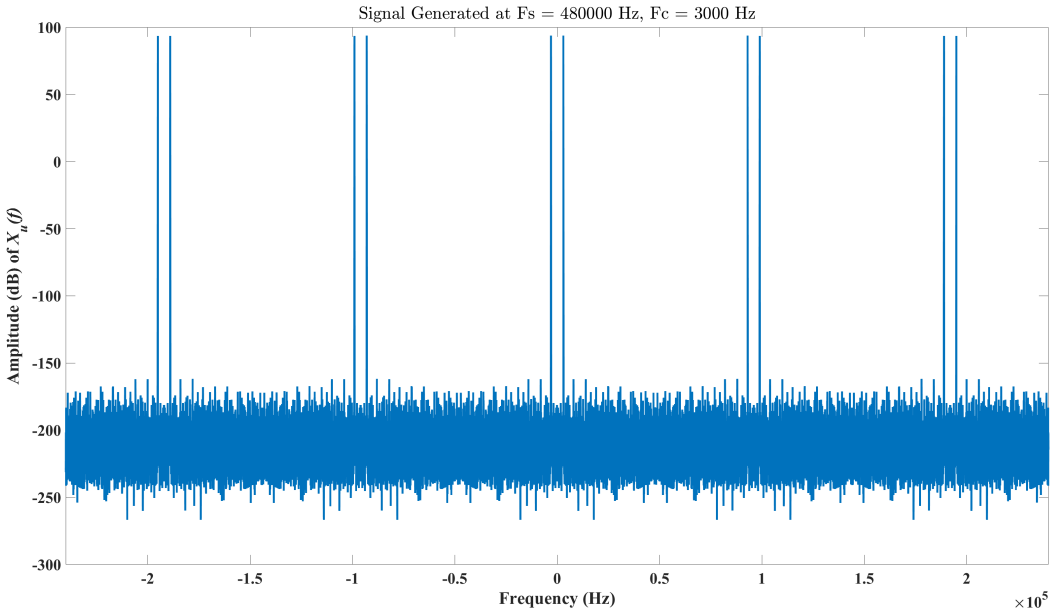

Figure 38. Spectral Plot of Upsampled Baseband Signal

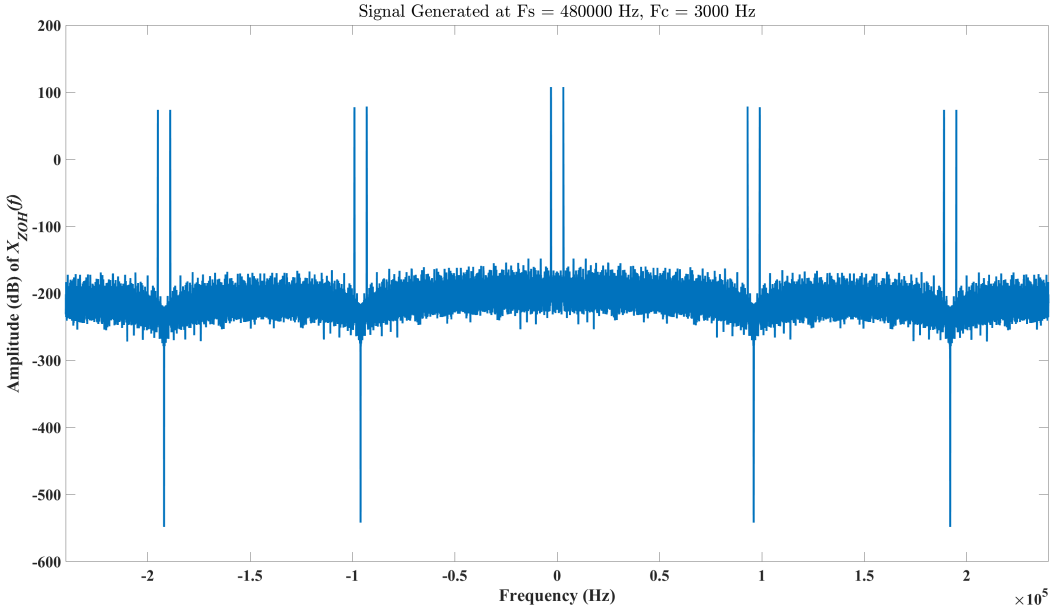

Figure 39. Spectral Plot of ZOH Signal

where x_{si} is the index of the spur from 0 Hz, and shown in Figure 38. The mirror image is centered around the original sampling frequency, and the upsampling operation does

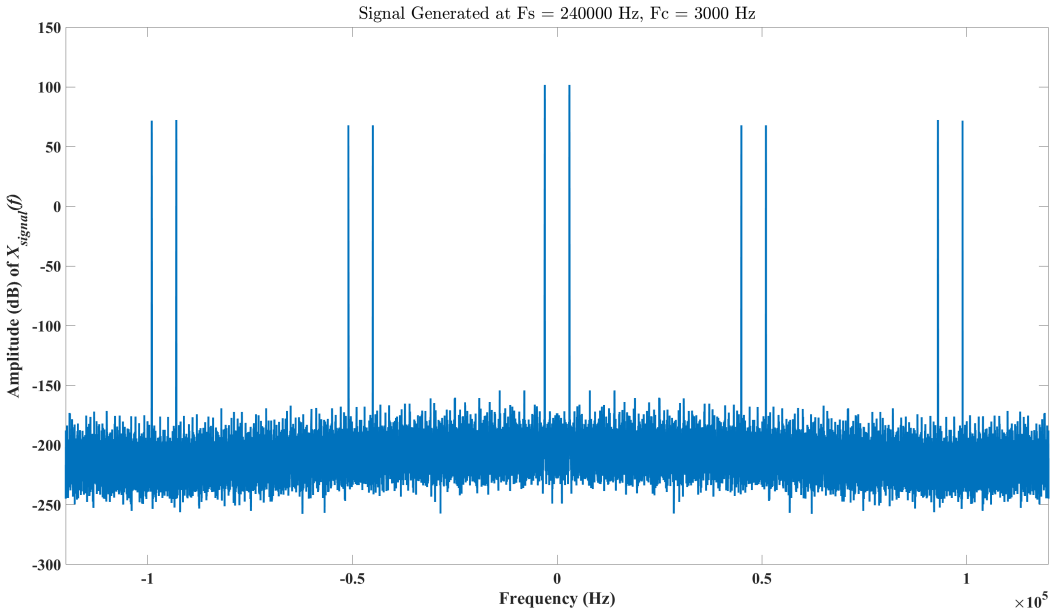

Figure 40. Spectral Plot of Downsampled ZOH Signal

not add any kind of energy of the signal as expressed by

$$e = \frac{1}{N} \cdot \sum_{k=0}^{N} |X[k]|^2. \tag{41}$$

Afterwards, the signal is goes through a ZOH operation, where a rect function with the length of the upsampled rate is convolved with the incoming signal, as described in Equation (35) and Equation (36). The power of the spurs are reduced over frequency. The approximate location is expressed by Equation (40) and the power of each spur is expressed by

$$p_{dBc}[x_{si}] = -20 \cdot log10(x_{si} \cdot 2^k), \qquad \text{for } x_{si} > 0. \tag{42}$$

The downsampling operation is applied causing the signal to be irregular as shown in Figure 36. This irregularity causes additional in-band spurs to be generated as

shown in Figure 40, and the location of each spur is expressed by

$$x_{sdown}[x_{si}] = x_{si} \cdot GCD\left(f_c \cdot 2^k \cdot \frac{\mu}{\nu}, f_c \cdot 2^k\right), \qquad \text{for } x_{si} > 0. \tag{43}$$

The downsampling operation without filtering causes frequency folding to occur. The downsampling operation causes spurs from the other Nyquist zones to be folded over into the first Nyquist zone. This is called frequency folding, and the power of the spurs is uncertain because the downsampled spectrum is filled with irregular spurs. The power of the spurs can still be determined by using the combination of equations before and after the downsampling operation. The power of the carrier, in milliwatts, can be approximated by

$$p_{car} = \frac{X_m^2}{2}. \tag{44}$$

Regularity of the signal is certain when f_s is divisible by $f_c \cdot 2^k$. Figures 41 and 42 show the time and spectral plots of a signal. The plots show periodicity which causes spurious emissions to be generated at every $f_c \cdot 2^k$ Hz with $k = 5, f_c = 2500$, and $f_s = 240,000$ Hz. Figures 43 and 44 show the periodicity with $k = 5, f_c = 1250$, and $f_s = 240,000$ Hz. Figures 45 and 46 show the periodicity with $k = 3, f_c = 1250$, and $f_s = 240,000$ Hz. Figures 47 and 48 show the periodicity with $k = 3, f_c = 1250$, and $f_s = 80,000$ Hz.

Figures 49, 50, 51, and 52 show the results between the mathematical solution and the DDS model. The phase resolution is varied between 1 and 16 bits, and the f_c is set to 3000 Hz for Figures 49 and 50. Figure 49 shows the location of the first spur with respect to the phase resolution. Figure 50 shows the amplitude of the first spur with respect to the phase resolution. The phase resolution is set to 5 bits and f_c is varied throughout the first Nyquist zone for Figures 51 and 52. Figure 51 shows

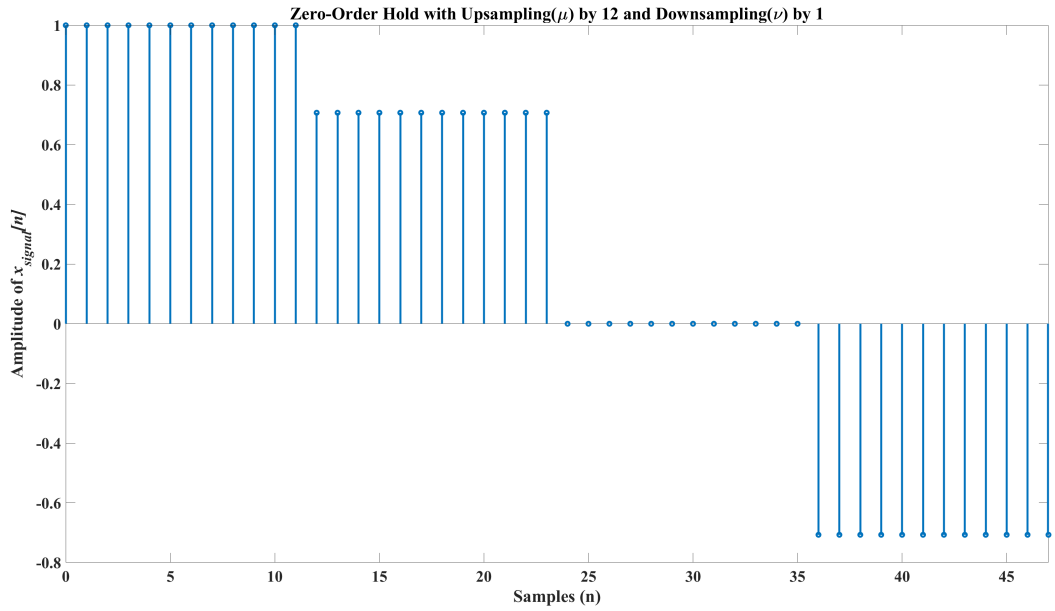

Figure 41. Example 1 of Plot of Periodic Signal

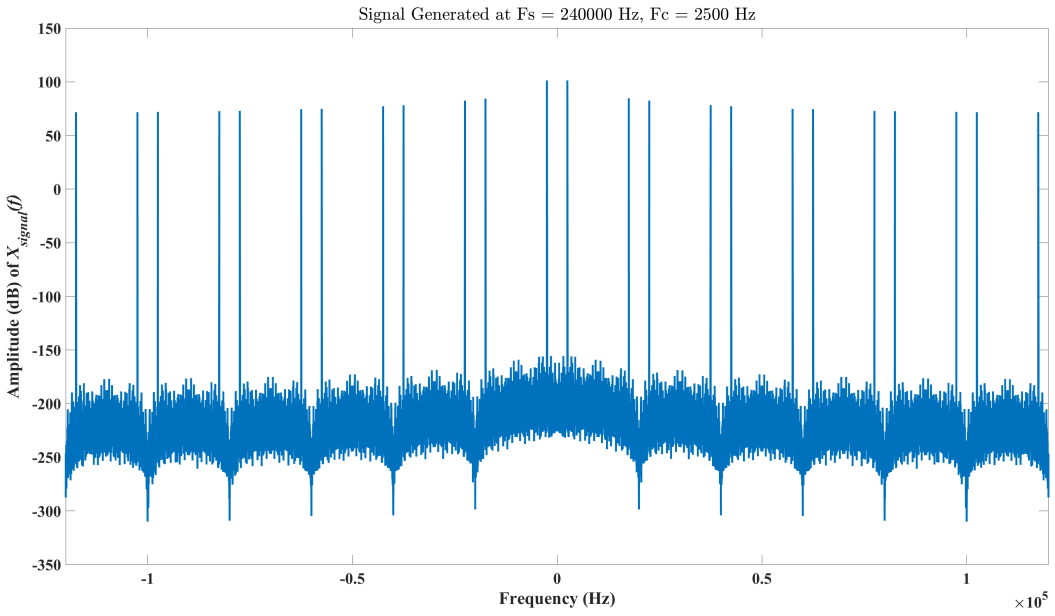

Figure 42. Example 1 of Spectral Plot of Periodic Signal

the location of the first spur with respect to f_c. Figure 52 shows the amplitude of the first spur with respect to f_c. There are small discrepancies between the mathematical and DDS models on Figures 50 and 52. This is because of numerical precision error

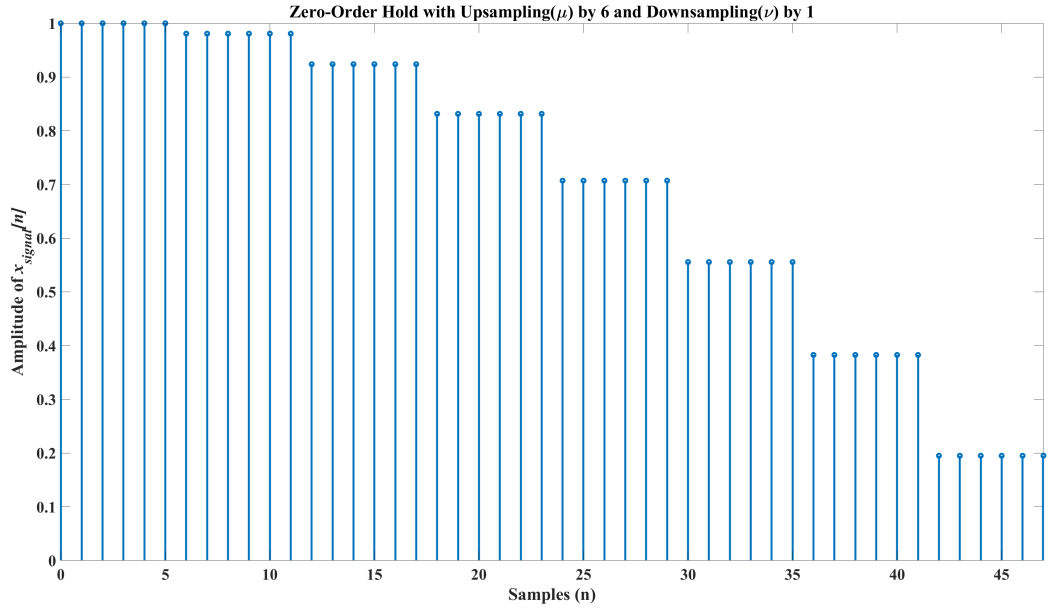

Figure 43. Example 2 of Plot of Periodic Signal

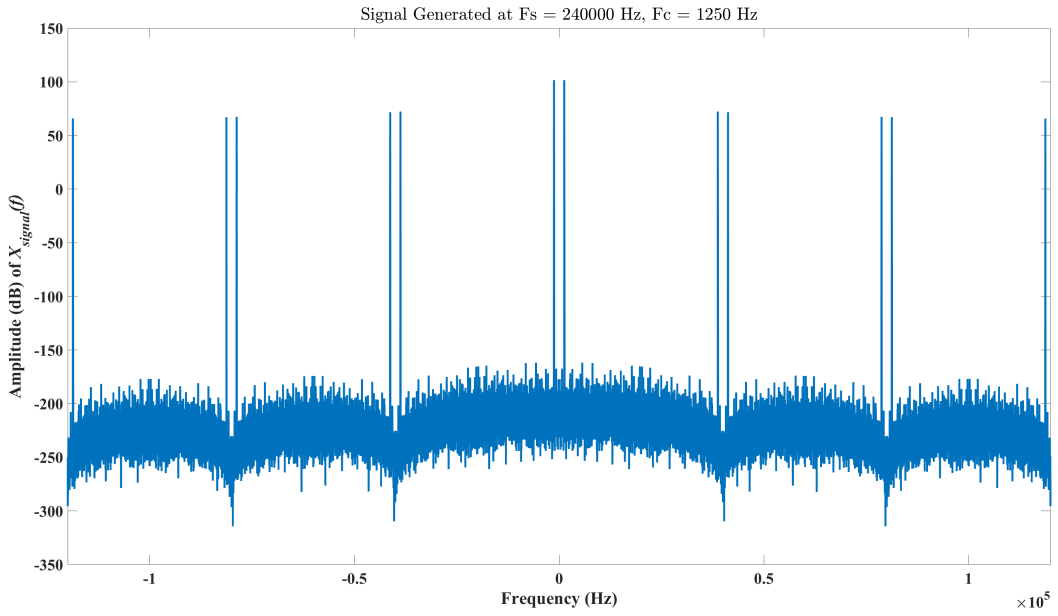

Figure 44. Example 2 of Spectral Plot of Periodic Signal

of the computational program.

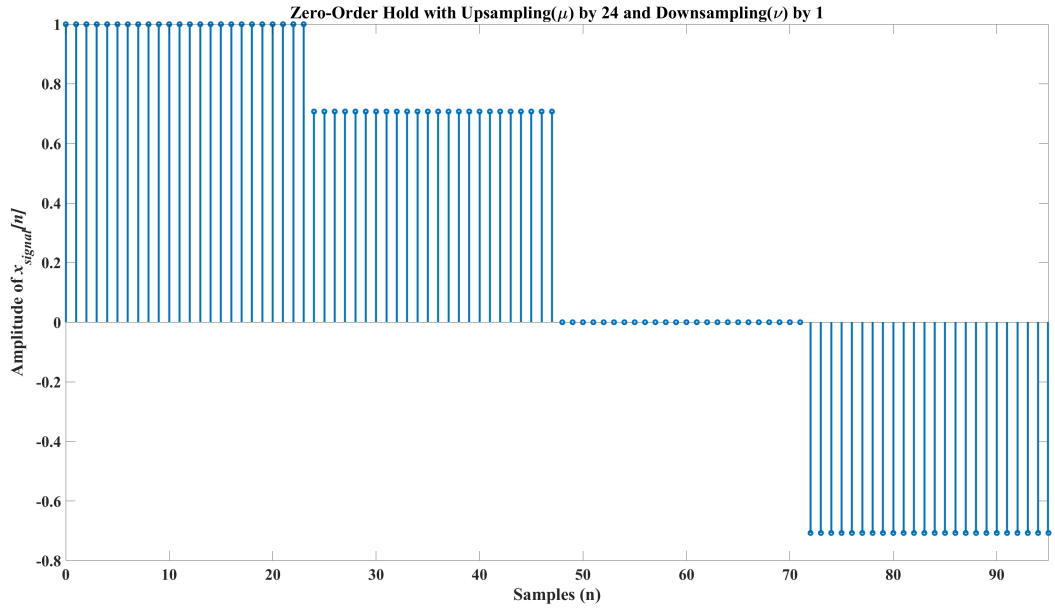

Figure 45. Example 3 of Plot of Periodic Signal

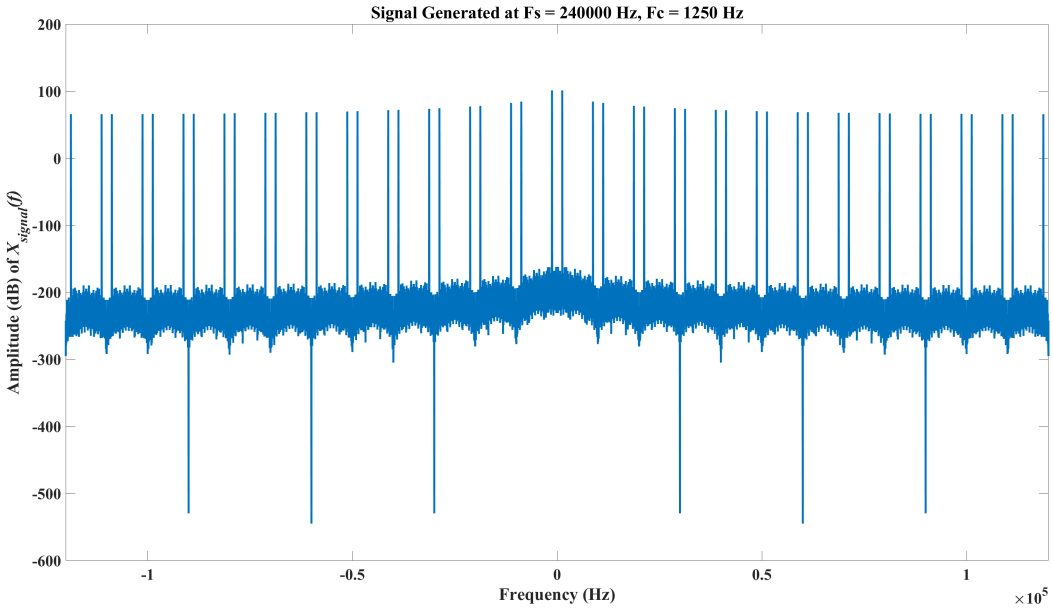

Figure 46. Example 3 of Spectral Plot of Periodic Signal

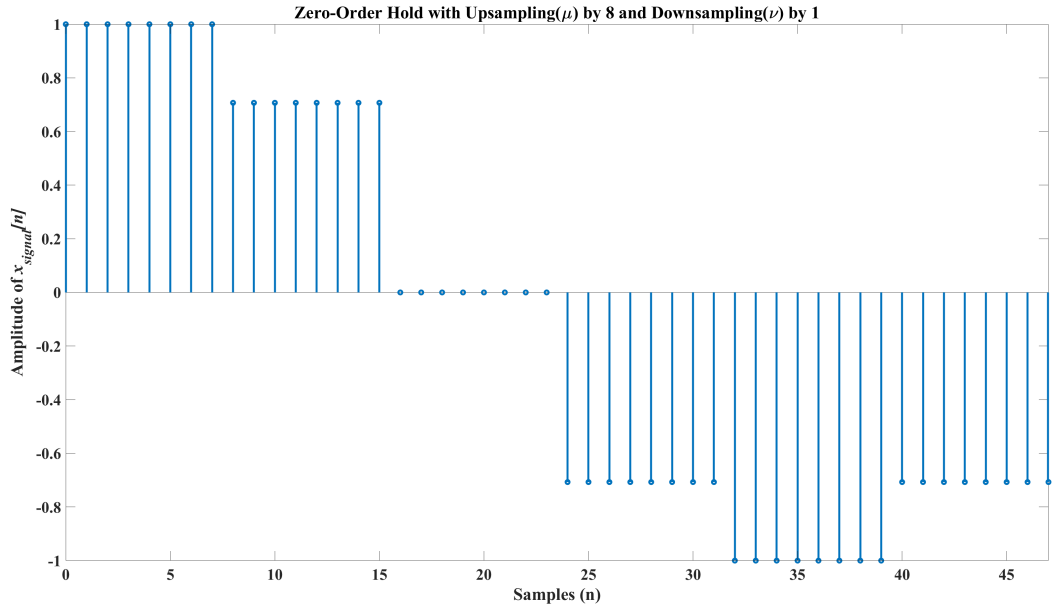

Figure 47. Example 4 of Plot of Periodic Signal

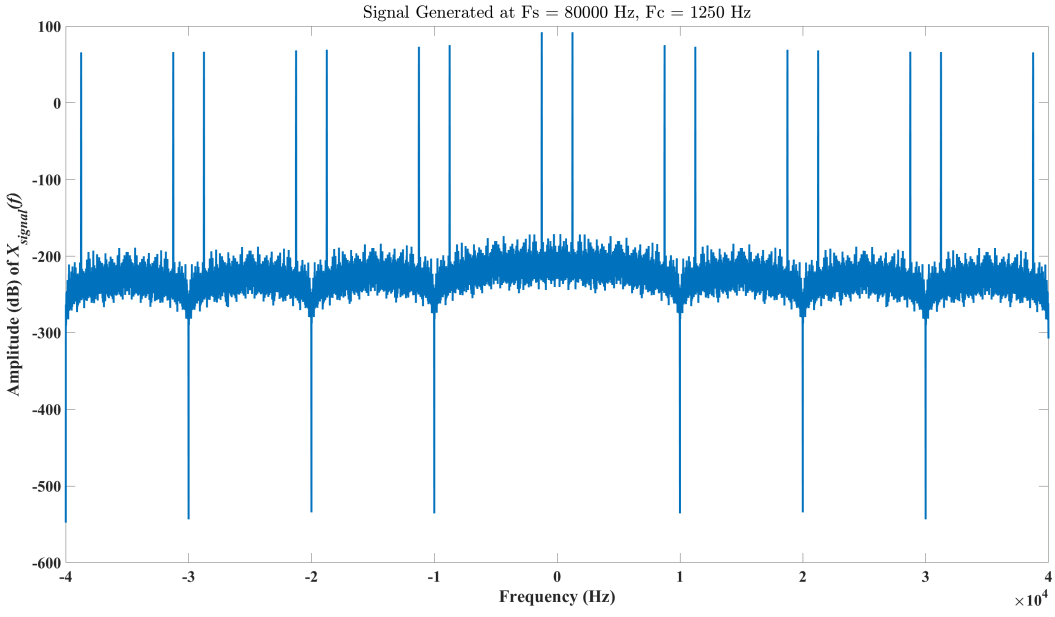

Figure 48. Example 4 of Spectral Plot of Periodic Signal

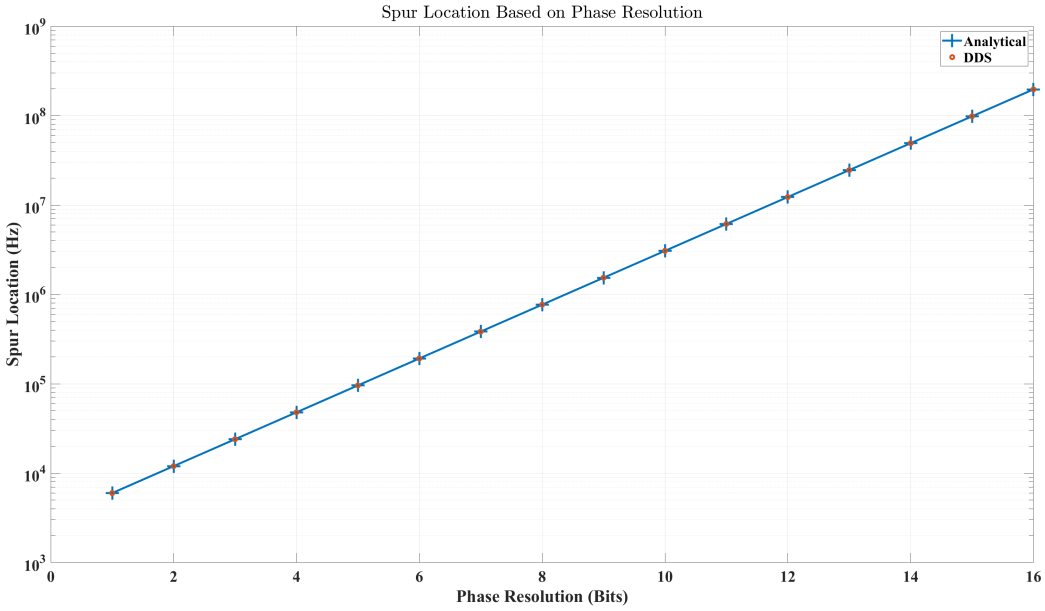

Figure 49. Spur Location Based on Phase Resolution at Fixed f_c

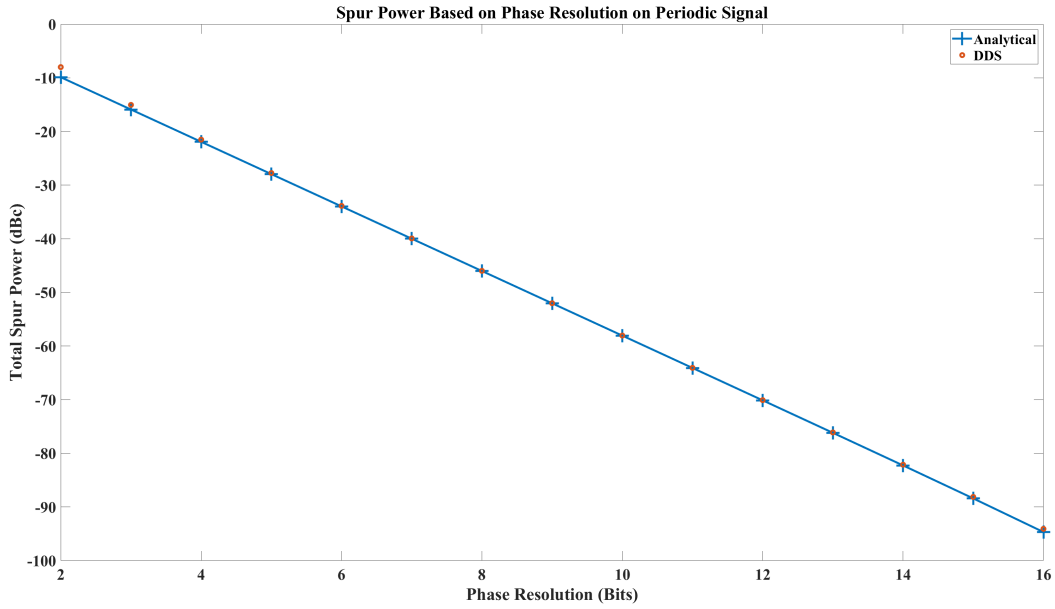

Figure 50. Spur Power Based on Phase Resolution at Fixed f_c

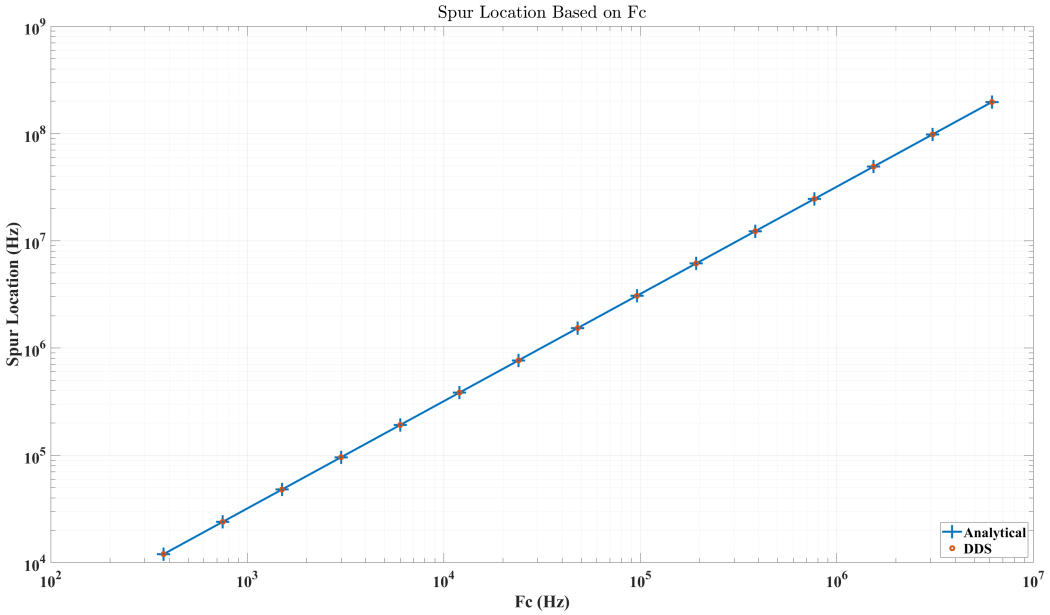

Figure 51. Spur Location Based on f_c at Fixed Phase Resolution

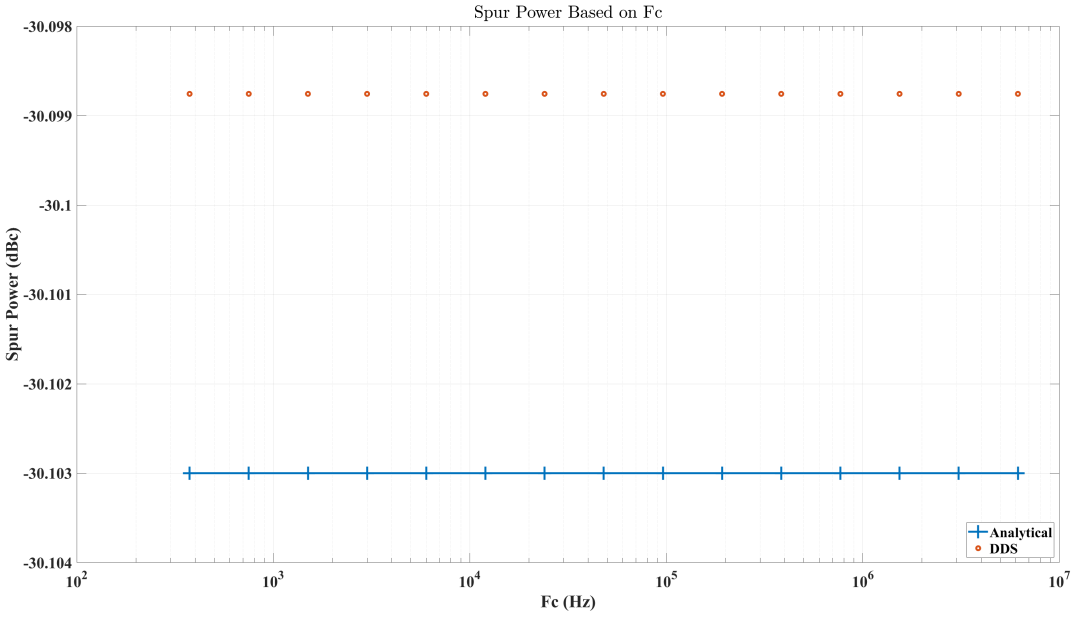

Figure 52. Spur Power Based on f_c at Fixed Phase Resolution

4.4 End to End Results of Phase Noise and Quantization of the System

4.4.1 Phase Noise.

Figures 53 and 54 show the close-in phase noise of the signal generator and GWPP. The collected I/Q data is coherently integrated to reduce the variance of the measurement [5]. Figure 53 shows spurs being present in all three measurements. This means the spurs are originating from the signal generator. At various points, there are 1 dB spurs present only from GWPP, shown in Figure 54. When compared with the phase noise of the L1 signal from GPS III, GWPP exceeds phase noise performance by a minimum of 20 dB.

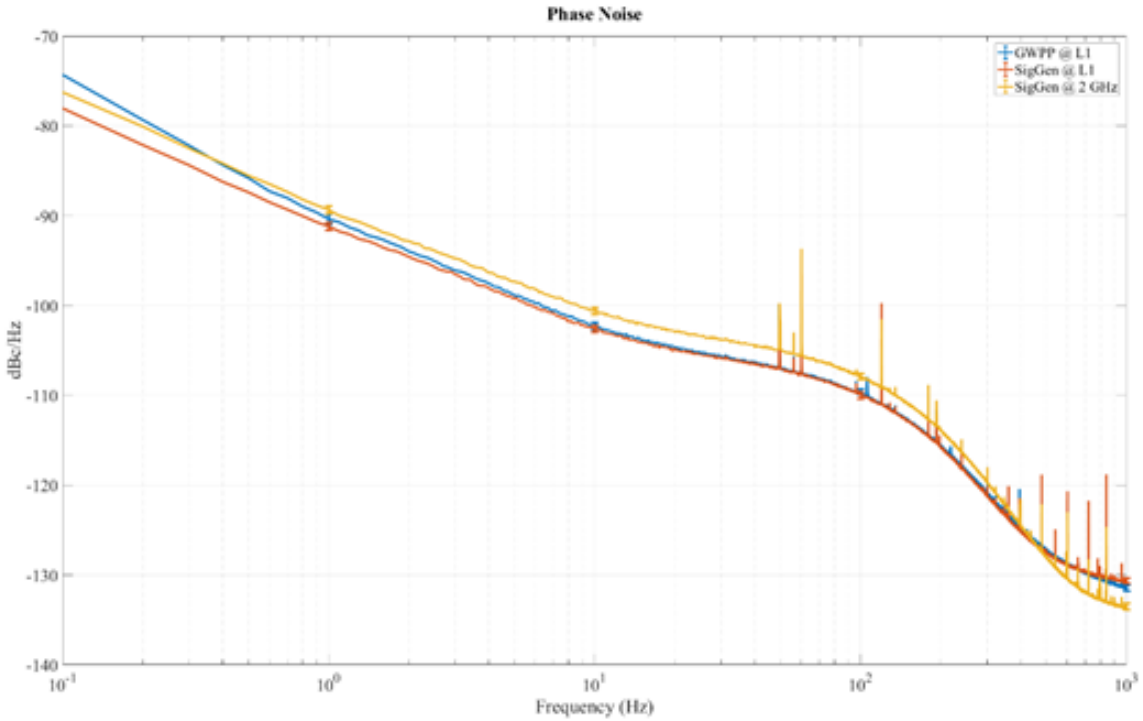

Figure 53. Phase Noise of System

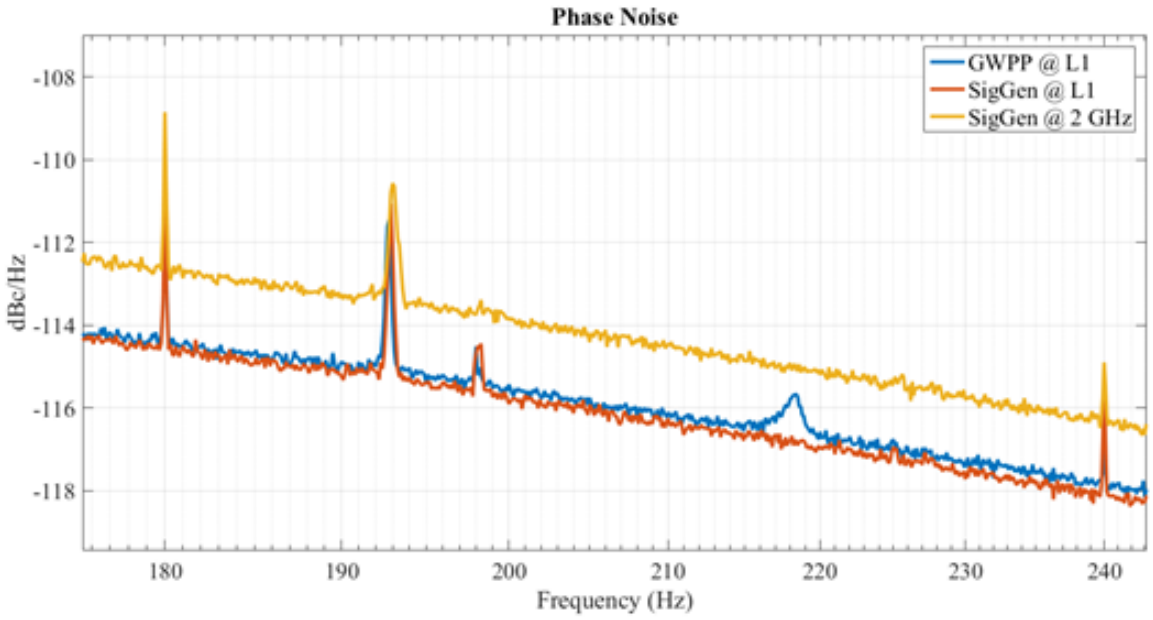

Figure 54. Zoom-In Phase Noise of System

4.4.2 Quantization Error Effect.

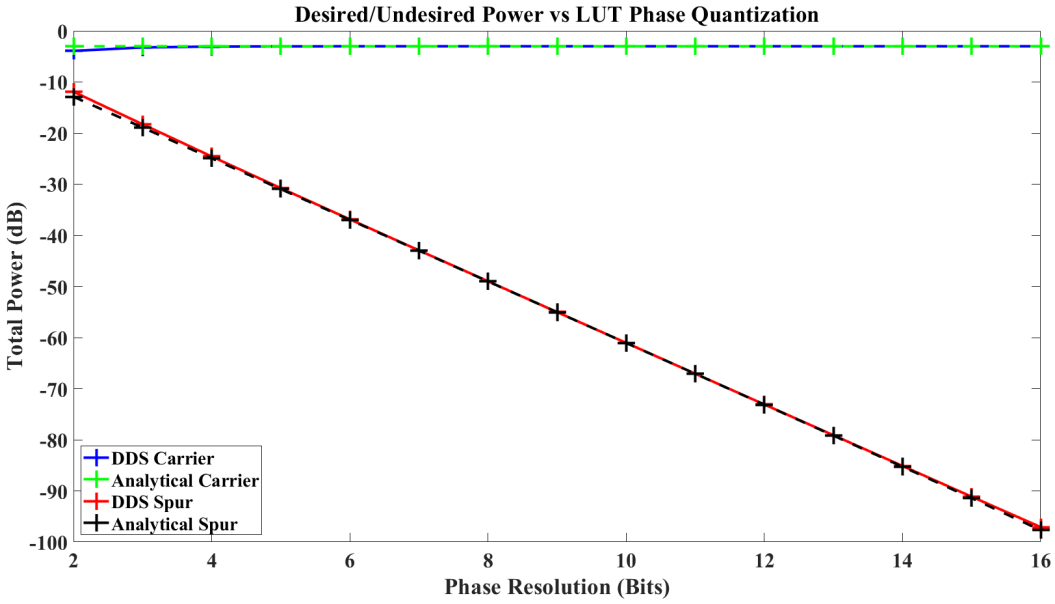

Figure 55. Phase Quantization Error of Periodic Signal

Figures 55, 56, 57, 58, and 59 show the effects of quantization of phase and amplitude on the carrier signal and the spurious content. Figures 55 and 58 show

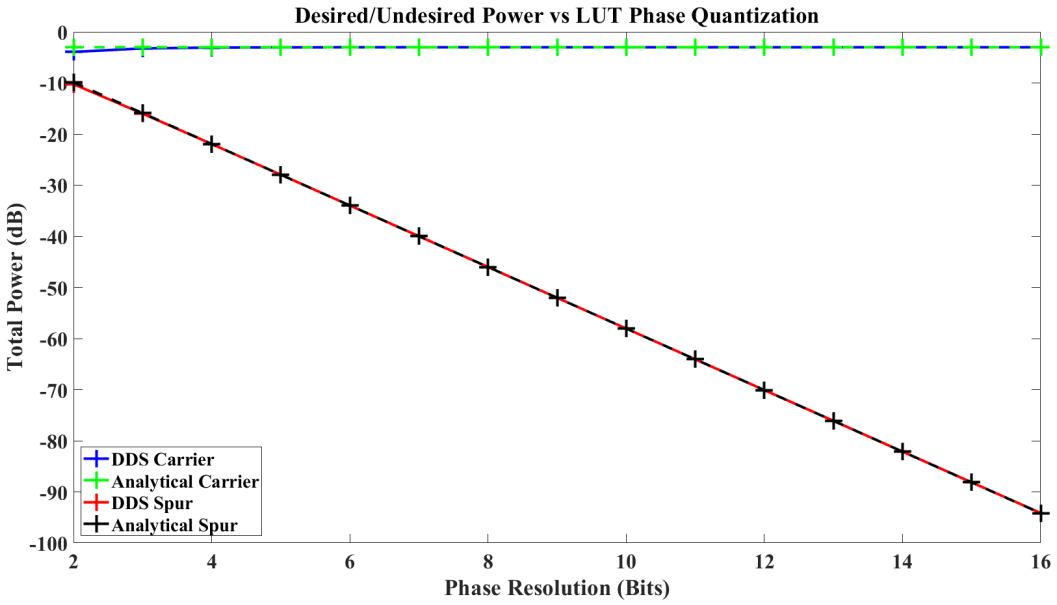

Figure 56. Phase Quantization Error of Non-Periodic Signal

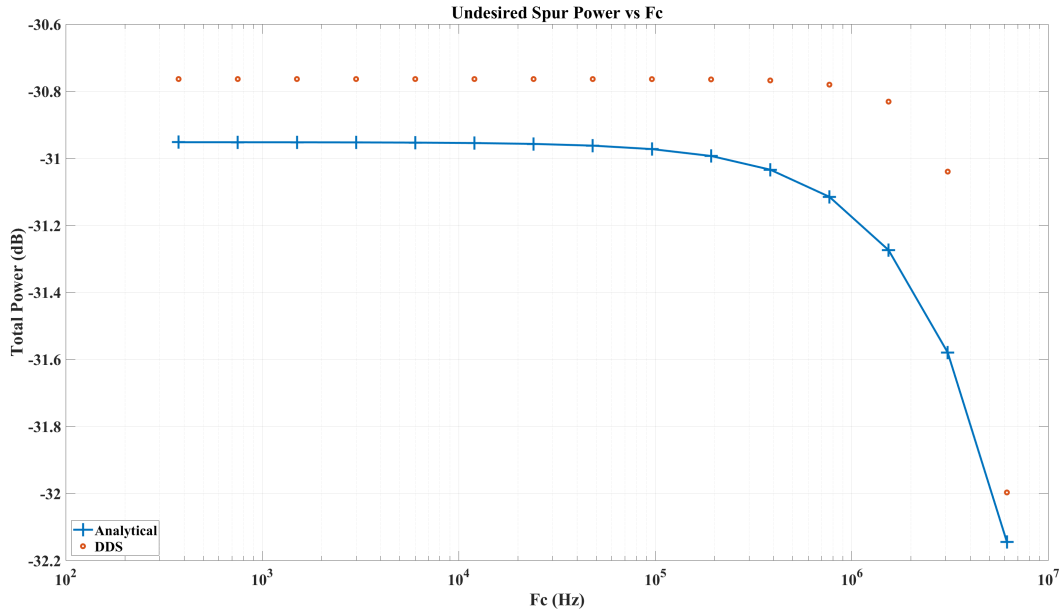

Figure 57. Total Spur Power Between Mathematical and DDS Models

the quantization error when the signal is periodic, and Figures 56 and 59 show the quantization error when the signal is non-periodic. The signal is periodic when f_s is divisible by $f_c \cdot 2^k$, otherwise the signal is considered non-periodic. Simulation models

varied the phase and amplitude quantization range from 2 bits to 16 bits. The phase quantization figures are compared between simulation and mathematical models. The mathematical models are derived from equation from Chapter 4.2.4. The amplitude quantization figures are compared between simulation and mathematical models from Reference [40].

Figures 55 and 56 show phase quantization effects on a periodic and non-periodic carrier signal between the DDS and mathematical models. The figures show the sum of individual spur power throughout the entire spectrum for a specific phase resolution. Equations (42) and (44) are used to determine the mathematical model and to compare against the DDS model. The increase in total power for the spurs could potentially cause intermodulation distortion [5]. Any small discrepancies between the mathematical and DDS models is contributed to the numerical precision error

Figure 57 shows phase quantization effects on the sum of the individual spur power throughout the entire spectrum across various frequencies for a specific phase resolution. Equations (42) and (44) are used to determine the mathematical model and to compare against the DDS model. The mathematical and DDS models are closely matched. Any small discrepancies between the mathematical and DDS models is contributed to the numerical precision error of the computational program.

Figures 58 and 59 shows amplitude quantization effects on the periodic and non-periodic carrier signal and its spurs. The plots show that periodicity of the signal do not have an effect on the power of the spurs. Amplitude quantization affects the amplitude of the carrier and spurs. The carrier power still follows Equation (44). Equation (45) is used to determine the mathematical model of the spurs from amplitude quantization [40]. Any differences between the DDS model and the mathematical

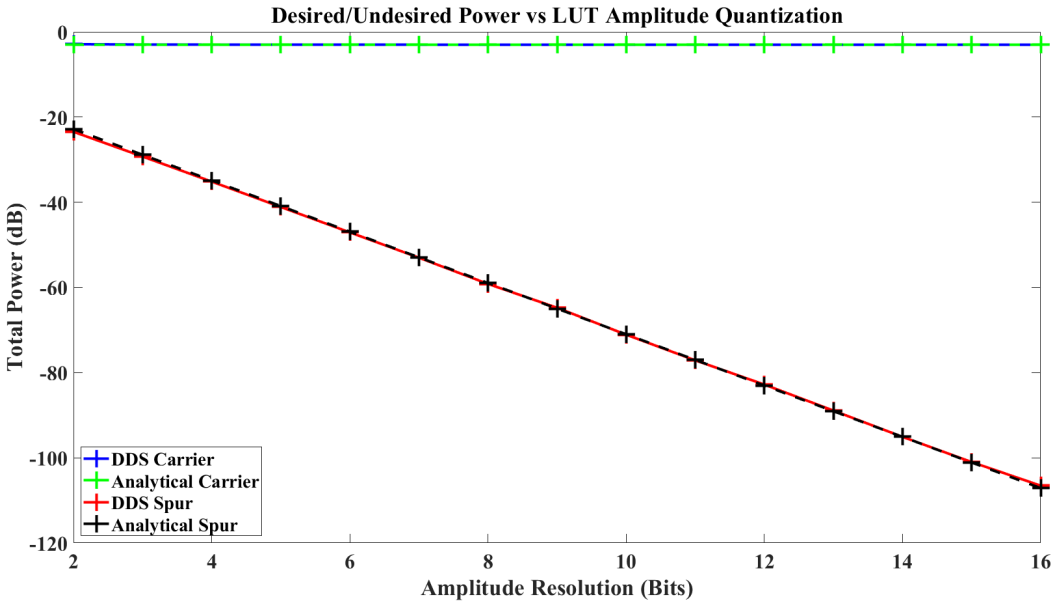

Figure 58. Amplitude Quantization Error of Periodic Signal

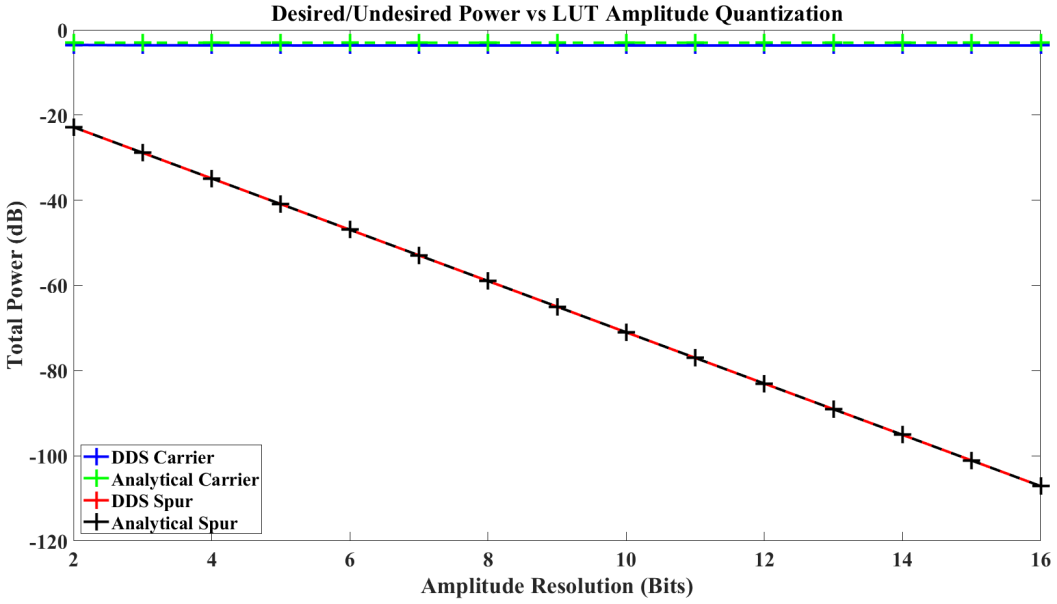

Figure 59. Amplitude Quantization Error of Non-Periodic Signal

model is contributed to numerical precision error.

$$p_{dB}[k] = 10 \cdot log10\left(\frac{2^{-k \cdot 2}}{12}\right), \qquad \text{for } k > 0 \tag{45}$$

4.5 Conclusion

Phase noise and quantization error effects have a detrimental effect on GPS signals. With GPS, the timing of transitions plays a role in position accuracy. If any phase noise exists, the timing of transitions will vary. The results show doppler on the signal, which mimics motion. Minimizing phase noise is critical to provide an accurate position solution. As shown in this chapter, GWPP has minimal effect on phase noise and exceeds phase noise performance compared to the most recent GPS satellites.

Spurious emissions are generated by the DDS when phase and amplitude are quantized. Phase quantization depends on the f_c and the phase resolution. Higher the phase resolution, the further away spurs are generated from f_c, and the spurs are lower in magnitude. The amplitude quantization only depends on the amplitude resolution inside the LUT. The magnitude of spurious emissions from phase quantization is higher than the magnitude of the spurious emissions from amplitude quantization, therefore there is a higher chance of intermodulation distortion in the neighboring bands.

V. Conclusion

This chapter concludes the dissertation by summarizing the results from the three thrusts of the dissertation. Also, this chapter discusses the published papers, contributions made to extend current research, and how this research has an operational impact on current Air Force efforts.

5.1 SatNav Flexible Architecture Testbed

Chapter III implements a proof of concept SatNav system using a DDS architecture. This system is called GWPP, and it mimics a dynamic satellite constellation with the transmission of multiple GPS signals. The research shows that the DDS architecture solves many of the issues plaguing current SatNav systems. It also shows the system retains compatibility with the current SatNav systems by validating the transmission with COTS and GOTS GPS receivers.

Many of the current SatNav deficiencies can be resolved by using the DDS architecture. First, the DDS architecture uses a DAC with a large instantaneous bandwidth in the system. This relieves the problem of incorporating new signals requiring additional bandwidth. Second, the DDS architecture is controlled digitally thus giving software-defined capability to the system. Third, the DDS architecture eliminates the need for having analog components for the upconversion chain. Fourth, the DDS architecture reduces signal transients by decreasing the number of analog upconversion components in the chain and digitally controlling the timing of the signal. Fifth, the footprint of the system is reduced because of the elimination of the analog components. Finally, by reducing the number of analog components, the risk is reduced for degradation of performance or failure.

GWPP is used with COTS and GOTS GPS receivers to determine if the DDS

architecture retains backward compatibility with signals generated by current SatNav systems. The GPS control segment provides an archive of the ephemerides and almanacs of each GPS satellite. With the archival data and as shown in Chapter III, GWPP successfully demonstrated it is able to regenerate valid signals for the GPS receivers.

5.2 Phase Noise and Quantization Effects and Modeling

Chapter IV implements end-to-end modeling and analysis of GWPP. The phase noise of the entire system, including the clock source, digital signal generation, and DAC, is examined and modeled.

5.2.1 Examination of Phase Noise.

Phase noise performance is important to provide an accurate position solution. The DAC within GWPP had a minimal impact on the phase noise of the overall system. The majority of the phase noise from GWPP originated from the external clock source.

5.2.2 Quantization Effects and Modeling.

The overall noise performance of the test equipment is inadequate to do any kind of analysis because the overall noise floor is higher than the power of the spurs. Reference [5] shows that the quantization effects on signals captured with test equipment and the signals from the simulation DDS models are comparable, therefore the simulation DDS model is used to develop the mathematical model.

The DDS and mathematical models implement the phase and amplitude quantization in the signal generation process. In this research, the mathematical model focuses on phase quantization because amplitude quantization has been thoroughly

researched and documented [39]. Also, there is a higher chance of interference from phase quantization because the individual spurs are higher in power. The location of the spurs are dependent on phase resolution, carrier and sampling frequency. If the upsampling and downsampling ratio is a whole number, the spurs are spaced out on the multiple of the lower sampling frequency. If the ratio remains a fraction, additional spurs are generated from frequency folding. Spur power relative to the power of the carrier is only dependent on the phase resolution.

5.3 Publications and Technology Transfer

The work completed in this dissertation lead to four conference papers [5], [31], [41], [42], one journal is in process for submission, assistance with two conference papers [2], [43], assistance with two master's thesis [44], [45], and one technology transfer for operational needs of the USAF. The work in Chapters III and IV lead to five and one conference papers, respectively. GWPP is in operational use at AFRL Space Vehicles Directorate.

The work done in Chapter IV is in preparation for submission to *IEEE Transactions on Circuits and Systems I*. The journal is titled "End-to-End Direct Digital Synthesis Simulation and Mathematical Model to Minimize Quantization Effects of Digital Signal Generation", and it is due to be submitted to the journal in June 2020.

The conference paper titled "Development of a GNSS Waveform prototyping Platform for Advanced Signals Research" was published at *Joint Navigation Conference* in 2017 [41]. The paper describes the development work on implementing the DDS architecture in GWPP in Chapter III.

The conference paper titled "Implementation of L1C on a GNSS Waveform Prototyping Platform for Evaluating Next-Generation GPS Advanced Signal Concepts" was published at *Joint Navigation Conference* in 2017 [43]. The paper describes the

development work extending the capabilities of GWPP to support next-generation GPS signal in Chapter III.

The conference paper titled "Dynamic Power Allocation with Constant Envelope Transmission for Next Generation Software-Defined GPS Payloads" was published at *International Technical Meeting of The Institute of Navigation* in 2018 [2]. The paper describes the development work into incorporating Phase Optimized Constant Envelope Transmission (POCET) to GWPP in Chapter III. The POCET algorithm is able to transmit multiple phase modulated signals with a constant envelope. The POCET algorithm is able change the power levels to each signal while maintaining a constant power envelope. This allows the use of an inexpensive highly efficient high power class C amplifier.

The conference paper titled "Demonstration of Distortionless Flex-Power and the Effects of a CHIMERA-Enabled GPS Authentication Signal on Current-Generation COTS Civilian GNSS Receiver" was published at the *Joint Navigation Conference* in 2018 [31]. The paper takes GWPP and incorporates POCET with Chips-Message Robust Authentication (Chimera) to the GPS signal. The Chimera algorithm places markers on existing GPS for authentication purposes. Backward compatibility is maintained and validated by sending the resulting signal to COTS GPS receivers.

The conference paper titled "Characterization of Phase and Amplitude Quantization Effects in a Direct Digital Synthesis-based Waveform Generator for Future Software-Defined GPS Payloads" was published at *International Technical Meeting of The Institute of Navigation* in 2018 [5]. The paper described the characterization work on GWPP in Chapter IV.

The conference paper titled "Phase Optimized Constant Envelope Transmission-Induced Pseudorange Biases and Mitigation" was published at *Joint Navigation Conference* in 2019 [42]. The paper described in-depth analysis of the effects of POCET

on GPS signals using the DDS architecture in Chapter III.

Air Force Institute of Technology (AFIT) transitioned this research and GWPP to AFRL Space Vehicles Directorate. GWPP serves as a baseline design to verify contractor deliverables to support the Navigation Technology Satellite III (NTS-III) initiative. GWPP is also used to prototype advanced signals for the next-generation GNSS research.

5.4 Future Work

References [31] and [43] demonstrated the implementation of POCET into the DDS architecture. This allowed the DDS to generate multiple Code Division Multiple Access (CDMA) or DSSS signals with various power levels. The DDS architecture can be configure to support multiple frequency or Frequency-Hopping Spread Spectrum (FHSS) signals by modifying the phase NCO for each requested frequency.

LUT stores the type of waveform in the DDS architecture. In this research, a sinusoidal wave is stored in the LUT or a ROM. Replacing the ROM with a RAM will provide the flexibility to generate any type of waveform – square, triangle, sawtooth, etc. Also, implementing multiple RAM instances will provide a multi-type signal generation capability.

In Electronic Warfare (EW) applications, it would be interesting to see the DDS architecture be integrated into a wideband application. This will provide a real-time response time to applications such as cognitive radio, radio jammers, and spoofers. For these applications, spectrum sensing algorithms can be performed on the spectrum and the appropriate signal can be transmitted.

In conjunction with a receiver, the DDS architecture can be used to bridge radio technology. For instance, legacy receivers on existing platforms may not be able to receive the next-generation signals. Upgrading a legacy receiver may be cost prohib-

ited. The receiver can receive the next-generation signals and provide parameters to the DDS architecture to re-transmit a legacy signal to the legacy receiver.

Chapter IV analytically determined the location and power of the spurs, but power of the weakest spurs will require additional analysis. A spur cancellation component will allow the reduction of spur power within the spectrum. A 180 degrees out of phase signal for each spur can be created and multiplied with the resulting signal from the LUT. This will effectively cancel out the spurs.

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