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IRIS PHASE III, SUBPHASE B EVALUATION

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Introduction

The purpose of this report is to provide an evaluation of the primary performers in Phase 3, Subphase B, of the IRIS program against the requirements outlined in DARPA BAA-15-47, dated July 17, 2015. In addition, this report will suggest paths forward to build upon the results of IRIS.

IRIS Phase III was designed to develop physics based models to inform highly accelerated microelectronics reliability testing. Real-time testing of parts to an expected useful lifetime of 100,000 hours (~ 10 years) under operational conditions is clearly not feasible. Standards for accelerated reliability testing have been developed by the microelectronics industry, however even under voltage, temperature, and humidity stress conditions it can still take 30 days or more to induce a statistically relevant number of failures. In IRIS Phase III, performers were asked to develop methodologies to reduce accelerated lifetime testing time to ≤ 1 hour.

The program was divided into two technical areas. TA1 was limited to front-end-of-line (FEOL) device reliability, i.e., failure modes at the transistor level such as Bias Temperature Instability (BTI), Gate Oxide Time Dependent Dielectric Breakdown (TDDB), and Hot Carrier Injection (HCI). TA2 was limited to back-end-of-line (BEOL) reliability, i.e., failure modes at the interconnect metallization levels such as copper electromigration and Low-k Dielectric TDDB. Further the program was divided into two subphases. Subphase A focused on theory and development of physics-based models; no hardware fabrication or data collection was necessary to meet the program requirements. Subphase B focused on demonstration; performers were asked to use their physics-based model to predict test conditions which would induce failures in microelectronic circuits in less than one hour and to demonstrate the highly accelerated reliability testing on test chips fabricated at the 28nm or 14nm technology node.

There were two primary performers in IRIS Phase III: IBM and Boeing. Both teams employed academic subcontracts to advance model developments in specific areas, e.g., TDDB or electromigration. This report will first consider the performance of the Boeing team and then the IBM team. The universities played important roles in the program but this report will not specifically reference their work except as part of the team. The University of California at Riverside had a limited role in Subphase A of TA2 which will be discussed briefly. This assessment is based on team presentations at the program reviews held in March 2017 and March 2018, as well as final written reports received in April 2020.

Boeing

During IRIS Phase III Subphase A, the Boeing team (which included members from ASU, Berkeley, and Purdue) developed a comprehensive statistical model which integrated charge traps generated by three different FEOL wear-out mechanisms: BTI, Gate Oxide TDDB, and HCI. The final-form compact model does not mention HCI so it is assumed that this failure mode was determined in the end to be not important compared to the others. In Subphase B the compact model was realized in Verilog code which could be imported into SPECTRE circuit simulations. This is somewhat beyond the requirements set forth in the BAA and represents a quality effort on the part of the team. The TDDB part of the model at least appears to invoke a physics-based functional form, as required by the BAA.

The model was used to simulate a sea of inverters designed in the GF 14nm process. Under stress conditions of 2.2 V, the model predicted a Weibull distribution lifetime of 4.3 hours, which does not quite meet the 1 hour requirement in the BAA but does represent a substantial advance toward the program goal.

The model was experimentally verified by measuring the threshold voltage (V_t) shift of 28nm planar high-k metal-gate transistors under accelerated stress conditions. The model and data agreement is good at accelerated ageing timescales from 1 second to 1000's of seconds. This demonstrates that integrating these failure mechanisms is a reasonable approximation to make, even as the voltage and temperature stresses become extreme. It also suggests that the test methodology proposed does not induce spurious failure modes which would not normally occur in operational use.

The BAA requires that in Subphase B the predictive capability of the model be evaluated by experimentally testing on complex circuits. Toward this end, a 14nm FinFET test chip was designed by the Boeing team and fabricated at GLOBALFOUNDRIES. The chip did not have a complex logic, but it was a step forward from transistor-level testing as it included arrays of transistors, arrays of inverters, arrays of logic of gates, and some ring oscillators. Although it appears the chip was received sometime in 2018 no experimental results were presented at the program reviews or in the final report. So demonstration of accelerated lifetime testing on complex circuits was not completed.

The Boeing model development and testing focused almost exclusively on TA1. Though some early model development on BEOL failure modes was shown, the team did not deliver a model or verification test data on TA2.

A summary table of the Boeing team performance is given below.

	TA1 (FEOL)	**TA2 (BEOL)**
Compact model provided?	Yes	No
Accelerated test identified?	Not exactly 1 hour, but still highly accelerated	No
Device-level test data?	Yes, 28nm delta-V_y and 14nm I_{gate}	Yes, 14nm ILD TDDB and EM, but not accelerated
Circuit-level experimental verification?	No	No

Other significant factors	Model integrates charge trapping from BTI, gate oxide TDDB, and HCI mechanisms	
Overall assessment	Close to meeting program goals	Did not meet program goals

IBM

The IBM team (which included Georgia Tech) did not provide a compact model for TA1 or TA2. TA1 test articles were fabricated in a 14nm silicon-on-insulator (SOI) FinFET process. HCI and BTI transistor testing and ring oscillator testing were performed, as well as testing of an IBM ASIC scan-chain (array of programmable/addressable flip-flops) test vehicle. The reliability testing seems fairly routine and is not obviously aligned with development of a highly accelerated stress methodology and is novel only that it is applied to a 14nm SOI FinFET technology. The data was fit to empirical models, but it does not appear the models are physics-based, or, if they are, they do not advance from what is already available in the literature.

For much of Subphase B, TA1, IBM focused on an interesting finding that humidity has an effect on ring oscillator frequency during stress testing. Controlled laser ablation was used to open a patch of the chip through which moisture could pass. The data show only a 2% effect after 10 days, but it is possible this effect could become much more pronounced under more extreme stress conditions. After drying, about half of the degradation recovered which may suggest that this effect is not representative of the reliability failure mechanisms one would observe in operational use. It does not appear that humidity significantly accelerated the FEOL reliability testing. The team also reported work on using chip leakage current (IDDQ) for classification of counterfeit chips, though this work does not seem to be aligned with the goals of IRIS Phase III.

For Subphase B, TA2, the IBM team examined the effect of humidity on BEOL test structures, primarily 14nm comb-comb capacitors. Again, controlled laser ablation was used to open a patch of the chip through which moisture could pass. At 80% relative humidity, the capacitors showed a significant increase in capacitance and in dielectric loss over a 20-day period. More importantly, capacitor failure, defined as the voltage at which a sharp increase in capacitance and dielectric loss occurs, decreased substantially from 16V to ~ 8V. This very promising result suggests that aggressive humidity conditions could greatly accelerate the time required to induce BEOL reliability failures.

The team also developed a model including TDDB, HCI, BTI, and electromigration, based on simulations of test processors using input from existing IBM data on BTI and TDDB. This model is interesting and probably represents an advancement of the state of knowledge of circuit-level reliability. Unfortunately it is it is not clear that the model was used to predict highly accelerated test conditions as required by the BAA. However, the model was employed to identify subspaces of test conditions which can be employed to selectively introduce gate oxide TDDB fails (FEOL) and contact-level (middle-of-line, MOL) TDDB failures.

A summary table of the IBM team performance is given below.

	TA1 (FEOL)	**TA2 (BEOL)**
Compact model provided?	No – but simulations including FEOL TDDB, HCI, BTI, and	No – but simulations including FEOL TDDB, HCI, BTI, and

	electromigration were developed which could become a compact model	electromigration were developed which could become a compact model
Accelerated test identified?	No.	Partially – humidity is promising route but was not fully demonstrated
Device-level test data?	Yes, 14nm ring osc. & FFT, but not at 1hr MTTF	Yes, 14nm interdigitated capacitors, but not at 1hr MTTF
Circuit-level experimental verification?	Partially – ring oscillators and scan chain	No
Other significant factors		Found conditions to isolate FEOL BTI and TDDB from MOL TDDB fails.
Overall assessment	Interesting findings which could impact program, but did not meet program goals	Interesting findings which could impact program, but did not meet program goals

University of California Riverside

UC Riverside had a specific role in the program to examine in detail mechanisms for highly accelerated BEOL failure from copper electromigration. This effort developed a novel physics-based model for electromigration by dividing the copper void evolution into three phases: nucleation, incubation, and growth. Based on the model, test conditions for 10,000x acceleration of electromigration failure were predicted, though the team also acknowledged that the required test conditions may be so far beyond the operating specifications of the chip that other unintended failure modes may be induced. The team also proposed a new electromigration test structure which would fail much faster than a conventional metal comb-serpent test vehicle. This could be important for chip makers as a yield vehicle to qualify technologies for production, but it does not apply to the problem of accelerated testing of full circuits by the end user which is the focus of IRIS Phase III. Nevertheless, generally this work is well-aligned with the goals of the program and the new electromigration model will surely be useful for highly accelerated reliability testing.

Summary and Further Recommendations

The compact model provided by Boeing should allow for prediction of test conditions for highly accelerated FEOL reliability testing, possibly achieving the 1 hour goal set forth in TA1 of the program. Boeing did not make significant progress in TA2, BEOL reliability. The IBM team did not provide a compact model or predict highly accelerated testing conditions. They did perform simulations of multiple failure modes in both FEOL and BEOL which do advance the field of reliability engineering. The Riverside BEOL electromigration model is compelling. Combining the FEOL model from Boeing and the BEOL model from Riverside, it is reasonable to assert that the goals of Subphase A and part of Subphase B were met, but not all by one team. The final part of Subphase B, performing the accelerated testing predicted by the models on complete test chips was not completed.

There is an opportunity to build upon what was accomplished in IRIS Phase III. Reduction of the IBM team simulations into a compact model which can predict highly accelerated test conditions would be of value; as it stands it is unlikely another user could realistically implement the IBM simulation platform to inform practical testing. Incorporating the Riverside electromigration model into both the Boeing and IBM frameworks will improve both platforms. Specific test conditions which will enable 1-hour lifetime testing are predicted by the Boeing model and should be verified on 14nm silicon test circuits. The same verification could be performed with the IBM team model once it is in a useable form. Incorporating the effect of humidity identified by the IBM team into both models may provide a strong experimental knob to reduce MTTF and achieve the ≤ 1 hour goal of the IRIS Phase III program.