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A Basic Introduction for Designing a Printed Circuit Board (PCB) with EAGLE eCAD/CAM Software

by Kenneth Kwashnak
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Belcamp, MD 21017

under contract W911QX-16-D-0014

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14. ABSTRACT
Printed circuit boards (PCBs) are ubiquitous elements of modern electronic systems. In DoD research, PCBs play a vital role in creating reliable, economic, and deterministic circuits, apart from their bread-board or perf-board counterparts. The art of transitioning a circuit's schematic to a physical manufacturable board can be challenging, but electrical computer-aided design (eCAD) and computer-aided manufacturing (CAM) software, such as the Easily Applicable Graphical Layout Editor (EAGLE), provides the creator with complete control of the circuit's design and streamlines the PCB fabrication process. This report serves as a general introduction to formulate a custom circuit schematic and two-layer PCB, as well as to process necessary files for design production.

15. SUBJECT TERMS
printed circuit board, Gerber file generation, electrical computer-aided design and manufacturing, PCB design

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1. Introduction

1.1 Prototyping

Bread- and perf-boards are great mediums for prototyping circuits. In prototyping hardware, the design process may evolve from a bread-board (Fig. 1) to a perf-board (Fig. 2) and then to a printed circuit board (PCB) (Fig. 3). The main reason to start with a bread-board is to plan a functional concept. Bread-boards are easy to work with and can expedite testing of a design. Next, a perf-board implementation provides a more rigid and responsive circuit. Finally, perf-board design is transformed into a PCB solution to finely tune and optimize the circuit. The goal of a PCB is to create a reliable, deterministic, and well-packaged device.

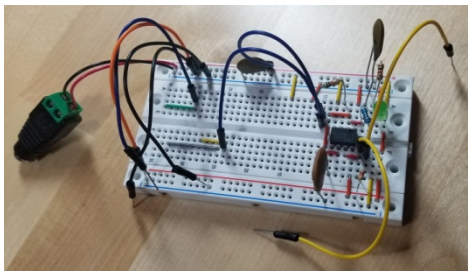


Fig. 1 Example of a bread-board circuit

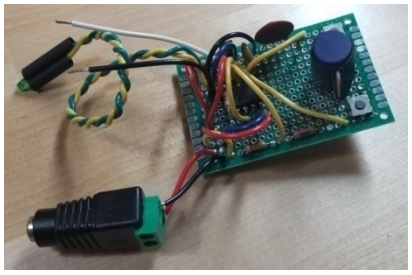


Fig. 2 Example of a perf-board circuit

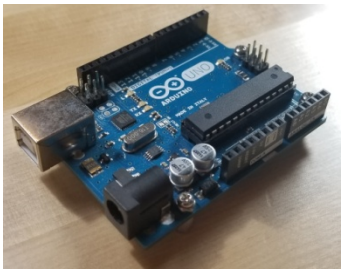


Fig. 3 Example of an assembled PCB

Table 1 provides the advantages and disadvantages of using each method.

Table 1 Prototype method comparison

Method	Pro	Con
Bread-Board	• Fast build for simple small circuits • Relatively inexpensive • Easy to swap out components • No expensive soldering equipment, requires few, if at all, hand tools • Inner rail system easy to connect components	• Difficult to implement large scale systems • Layout can get very messy • Components not fully secured, fragile • Difficult to control signal integrity • Stuck with predefined hole pattern • Limited on what type of parts to use without creating intricate adapters • One sided design • Difficult to reproduce many units • Reused bread-board holes can wear out
Perf-Board	• More secured and ridged design due to soldered / fastened components • Incorporates a wider range of components, such as surface mount devices (SMDs) • Two sided design • Hobbyist look and quality	• Layout can still get very messy • Stuck with predefined hole pattern • Difficult to disassemble • Requires soldering • Difficult to produce many units
PCB	• More secured and ridged design due to soldered / fastened components • Incorporates an even wider range of components, since pad placement can be defined, such as ball grid arrays (BGAs) • Add durable text, labels, and graphics to top and bottom layer • Multi-layered design • Precision Deterministic circuit behavior • Can be rather large projects • Professional look and quality • Plug design files in CNC machine to fab boards • Acid etching boards can produce prototypes	• Requires soldering • Usually requires eCAD software • Send files out for manufacturing, requires time • Boards, depending on complexity or requirements, can get costly for low quantity board count

1.2 eCAD and PCBs

The Easily Applicable Graphical Layout Editor (EAGLE) is an electrical computer-aided design (eCAD) and computer-aided manufacturing (CAM) software. EAGLE supports the designer in transitioning prototype hardware to a more controlled precision design.

PCBs are electrical circuits that are etched on assorted laminates via conducting material, such as copper. The copper branches through various layers of insulating dielectric to form interconnected networks. Figure 4 represents a board layout from EAGLE's example files.

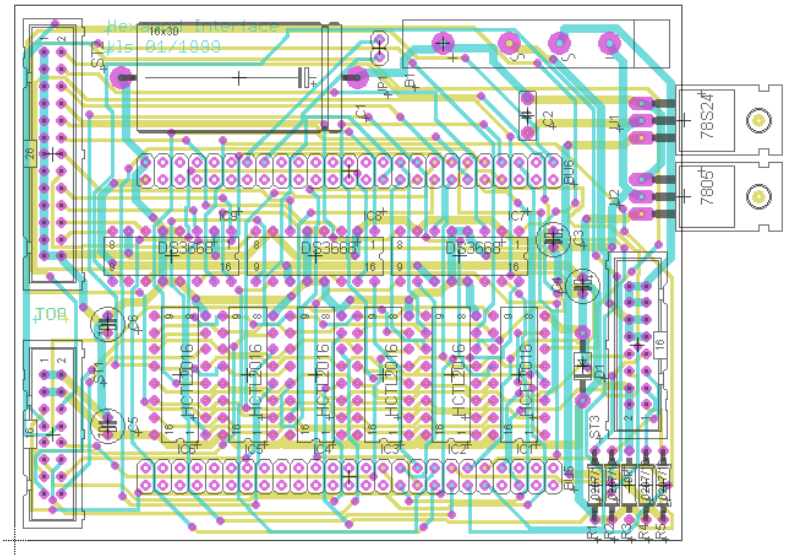


Fig. 4 Example two-layer PCB, hexapod.brd

The light blue and light green lines signify traces that connect the component's pins together. The light purple circles are the vias, which allow the traces from the top layer to connect with bottom layer. Various black outlines assist to define the overall shape of the board and components.

As seen in Fig. 4, a PCB can easily become crowded. Optimizing the overall placement and routing of components is critical in interconnecting hardware and ensuring component functionality. In some designs, multiple layers are required to control power or signal planes. Yet, adding multiple layers and creating additional vias will drive the overall cost of the board, as well as many other factors, such as number of drilled holes, different tool changes to drill those holes, size of the board, thickness of copper material, type of insulating material, and trace tolerances.

1.3 Purpose and Intent

The layout of a PCB is an art form. The placement of traces is not usually as simple as drawing a straight line from one pin to another. When laying out traces for high-precision circuitry, line impedance, thermal expansion, layer capacitance, and signal integrity are just a few critical factors to consider in the design.

Unfortunately, electrical design, cost-reduction, and circuit optimization are beyond the scope of this paper. This report provides a basic introduction on how to compile a simple circuit, prepare a PCB for manufacturing, and recognize the fundamental controls of the EAGLE PCB software.

The designer of a modeled circuit wants the PCB to behave exactly the way it was intended to function. Using eCAD software, the circuit's design is systematically controlled to follow stringent PCB manufacturing requirements. This allows the designer to govern deterministic circuit behavior (i.e., signal integrity, timing of signals), stable board properties (i.e., mechanical rigidity, thermal relief, overall layer capacitance), ease of assembly (i.e., component spacing, clearance room, solder mask pad size), and to neatly and professionally package the product.

Circuit design may become very complex, depending on the application, inter-connection of systems, and definitions of components. This walkthrough will guide the reader with a simple two-layer PCB design. This report 1) discusses material for resource creation (schematic symbols, board layout footprints, compiled devices, and component libraries), 2) reviews the methodology for fabricating a microcontroller board, and 3) presents the assembly and testing of a fabricated microcontroller PCB prototype.

1.4 Equipment

This section highlights the equipment for the design, assembly, and testing of the PCB.

1.4.1 Computer

This report refers to the computer equipment listed in Table 2, which includes an Ubuntu Linux 16.04 operating system (OS) laptop that utilizes VirtualBox (version 5.1.38) to run an isolated instance of Windows 7 Professional x64 OS. The virtual environment recognizes an external CD drive that is directly connected to the laptop (Kanguru, PN: U2-DVDRW-SL). The CD drive is necessary to install the software (Section 1.4.4) to the virtual Windows 7 OS.

Table 2 Virtual computer information

Windows 7 professional x64 OS virtual computer	
Manufacturer	Dell
Model	Dell precision M6800
Processor	Intel(R) Core (TM) i7-4910MQ @ 2.9GHz
Installed memory	16 GB

The reader should have a working proficiency with navigating and using the Windows 7 and the File Explorer interface. In addition, the reader should have general knowledge of computer hardware, resources, and troubleshooting.

The profile on the Windows 7 virtual machine has administrator rights in order to install and configure the EAGLE software.

1.4.2 Circuit Programming and Testing Hardware

Equipment included in Table 3 describes the tools used to assemble and test the fabricated PCB. Assembly is required to test the functionality of the fully populated board, but not necessary for the initial design of the PCB. Yet, when creating a PCB, the designer must be aware of the assembly process and must incorporate viable pathways for tooling and physical component handling.

Table 3 Circuit programming and testing hardware

Line	Description	Manufacturer	PN	Q	Cost per item ($)	Total ($)
1	Lead free no clean solder wire 0.031 in Tin/Cpr Core 66	Kester[1]	24-9574-7618	1	55.39[a]	55.39
2	Soldering station, 35W	Aoyue[2]	936	1	42.75[b]	42.75
3	No clean flux paste rosin	MG Chemicals[3]	8341-10ML	1	16.28[a]	16.28
4	DC linear power supply, regulated, 0-30V, 0-5A	Korad[4]	KD3005D	1	85.00[c]	85.00
5	Banana to alligator clip cable (red and black wires)	B&K Precision[5]	TL 5A	1	10.10[a]	10.10
6	Multimeter, true RMS	Fluke[6]	117	1	219.99[a]	219.99
7	Desolder braid no clean, rosin, non activated (R), LF	Chemtronics[7]	60-5-5	1	6.55[a]	6.55
8	Assorted hook-up wire	Sparkfun[8]	PRT-11375	1	16.95[a]	16.95
9	Cable stripper and cutter, 20 ~ 30 AWG	Hakko[9]	CSP-30-1	1	14.06[a]	14.06
10	Tweezer set	Wiha[10]	44593	1	207.96	207.96

[a] Data from Digikey on October 8, 2020
[b] Data from Aoyue3d on October 8, 2020
[c] Data from SRA Soldering Equipment on October 8, 2020
[d] Data from Amazon on October 8, 2020

Table 3 Circuit programming and testing hardware (continued)

Line	Description	Manufacturer	PN	Q	Cost per item ($)	Total ($)
11	Isopropyl, cleaning agent	MG Chemicals[11]	824-1L	1	16.75[a]	16.75
12	Brush	MG Chemicals[12]	855-5	1	4.45[a]	4.45
13	PICKit3	Microchip[13]	PG164130	1	25.00[d]	25.00
14	PICKit3 programming cable	Digilent[14]	240-035	1	3.99[a]	3.99
15	ESD caliper	Wiha[15]	41105	1	74.56[a]	74.56

[a] Data from Digikey on October 8, 2020
[b] Data from Aoyue3d on October 8, 2020
[c] Data from SRA Soldering Equipment on October 8, 2020
[d] Data from Amazon on October 8, 2020

1.4.3 PCB Component Hardware

Components listed in Table 4 describe the basis for formulating a functioning microcontroller demo circuit. If the board is to be assembled, variations of these components may be used, but the designer must consult the component datasheet to ensure compatibility. In addition, refer to Appendix A for a list of manufacturing resources for enclosures, panel overlays, and component distributors.

Table 4 PCB hardware

Line	Description	Manufacturer	PN	Q	Cost per item ($)[a]	Total ($)
1	Microcontroller, DIP8	Microchip[16]	PIC12LF1501	1	0.77000	0.77
2	IC DIP socket 8POS	Adam tech[17]	ICS-308-T	1	0.15000	0.15
3	Battery, CR2450, 3V	Energizer[18]	CR2450VP	1	1.19000	1.19
4	Battery holder, coin PC pin	MPD[19]	BS-2450	1	1.09000	1.09
5	Regulator linear 3V, TO92-3	Microchip[20]	MCP1700-3002E/TO	1	0.37000	0.37
6	Green SMD LED	Dialight[21]	5988170107F	4	0.39000	1.56
7	Tactile switch, NO	C&K[22]	PTS 647 SK38 SMTR2 LFS	1	0.13000	0.13
8	Res, 0805, 120Ω, 5%, 1/8W	Vishay dale[23]	CRCW0805120RJNEA	4	0.10000	0.40
9	Cap, 0805, 0.1uF, 25V, X7R	KEMET[24]	C0805C104M3RACTU	1	0.10000	0.10
10	0.100 in header, 5 pin, prog	Molex[25]	22-23-2051	1	0.34000	0.34

[a] Price from Digikey as of September 18, 2020

Table 4 PCB hardware (continued)

Line	Description	Manufacturer	PN	Q	Cost per item ($)[a]	Total ($)
11	0.100 in, conn housing, 5POS	Molex[26]	0022012057	1	0.23000	0.23
12	0.100 in header, 2 pin, batt	Molex[27]	22-23-2021	1	0.17000	0.17
13	0.100 in, conn housing, 2POS	Molex[28]	0022012027	1	0.11000	0.11
14	Conn 22-30AWG crimp tin	Molex[29]	0008650804	7	0.10000	0.70

[a] Price from Digikey as of September 18, 2020

1.4.4 Software

EAGLE v5.3.0 Software CD Package (Fig. 5) is used for the eCAD tool in designing and creating the manufacturing files for the two-layer PCB.

Fig. 5 CadSoft EAGLE v5.3.0 professional edition

CadSoft used a stand-alone licensing model until around June 2016 until Autodesk acquired CadSoft - EAGLE. The software migrated to a subscription-based, online-authenticated service, which requires the user to periodically verify their credentials with the Autodesk license server.

EAGLE v5.3.0 uses a stand-alone license, while the most recent version (v9.6.2 at the time of publishing) uses a subscription-based model. Since the virtual computer does not have Internet access, it is impossible to download, install, verify, and run the software. Therefore, an older version of EAGLE is used to design a PCB.

Users may download the most recent version of EAGLE from the Autodesk website.[30] A free version of the software is available, but the user must log in through the Autodesk portal. After 14 days, the user must reverify their credentials.[31]

In addition, there are restrictions and limitations to the license type. The End User License Agreement (EULA) states that the "free" license shall only be used for personal learning.[32]

Fortunately, EAGLE version 5.3.0 was purchased before Autodesk acquired CadSoft and the sole purpose of the license is to perform research and development tasks on a stand-alone non-networked Windows-based machines.

Quick comparison: v5.3.0 and v9.6.2. The tutorial should transfer to the most recent version of EAGLE hosted by Autodesk. The most recent version of EAGLE will be loaded with new features and tools, but the overall premise remains the same (Figs. 6–9).

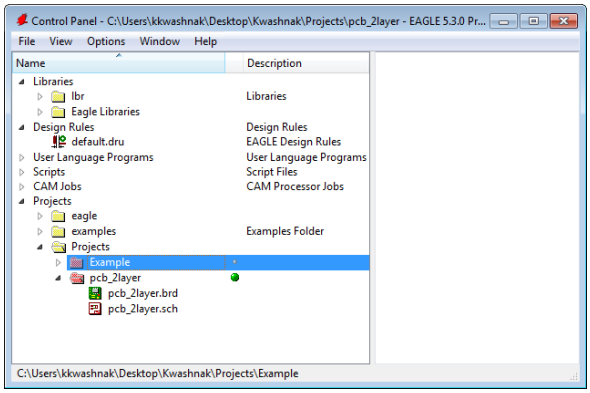


Fig. 6 v5.3.0 control panel

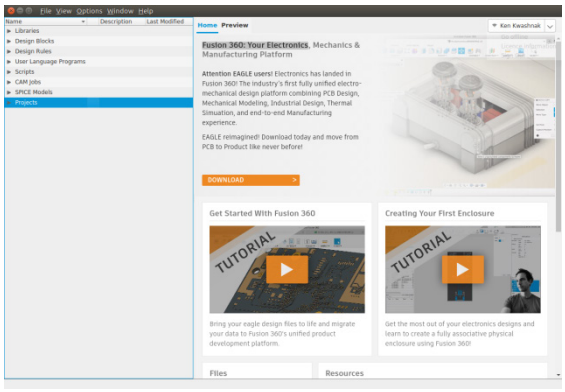


Fig. 7 v9.6.2 control panel

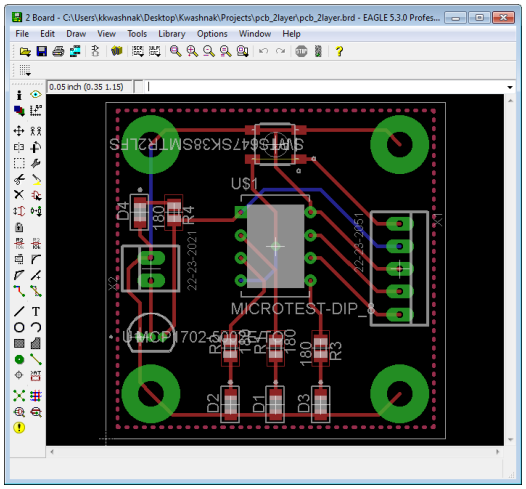


Fig. 8 v5.3.0 board workspace

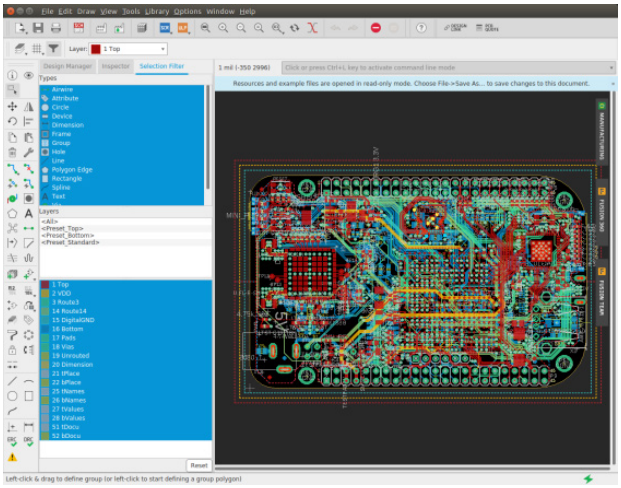


Fig. 9 v9.6.2 board workspace

Over the years there have been improvements to EAGLE designer software, but the core features still remain. It appears the latest version has a few more tools, graphical user interface (GUI) developments, and system tweaks. One of the major advantages of the latest version is integration with Fusion 360, a CAD tool that allows the designer to export their PCB from EAGLE and import into Fusion 360 to review the 3-D design. Newer EAGLE software also supports 3-D models for all components, which ties in with the device creation.

1.4.5 MPLAB X IDE and XC8 Compiler

Microchip's MPLAB X Integrated Development Environment (IDE) v5.4.0[33] and XC8 Compiler v2.30[34] are downloaded from a separate networked computer and burned to a CD. The programming of the microcontroller is briefly discussed in Section 5.3, but ultimately beyond the scope of this report.

1.5 Understanding the Walkthrough

The following conventions are used to describe various elements of the text:

<Options>	Element in EAGLE, such as a button, drop-down menu item, or interactive object.
Library	Source file(s) on Windows virtual computer
C:\Users	Source file location on Windows virtual computer
'Project'	Software property, such as a title on a panel, wording used on a program prompt.
"Hello"	Configurable text, such as a file name, folder, property, etc.
[CTRL] + [V]	Buttons on the physical keyboard. If two elements are conjoined by a "+" sign, simultaneously press both buttons on the keyboard.
`<p> World`	Coding block for programming

2. EAGLE Quick-Start

2.1 Installing the Software

Insert the EAGLE v5.3.0 CD into the CD drive. Navigate to the Windows folder (Fig. 10) and run setup.exe (Fig. 11).

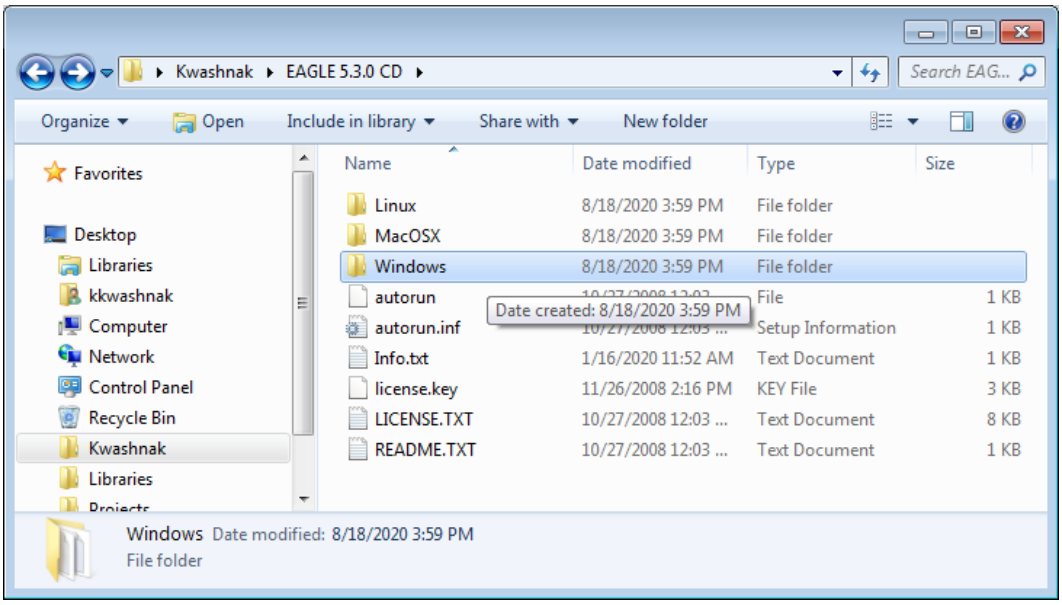


Fig. 10 EAGLE 5.3.0 CD contents

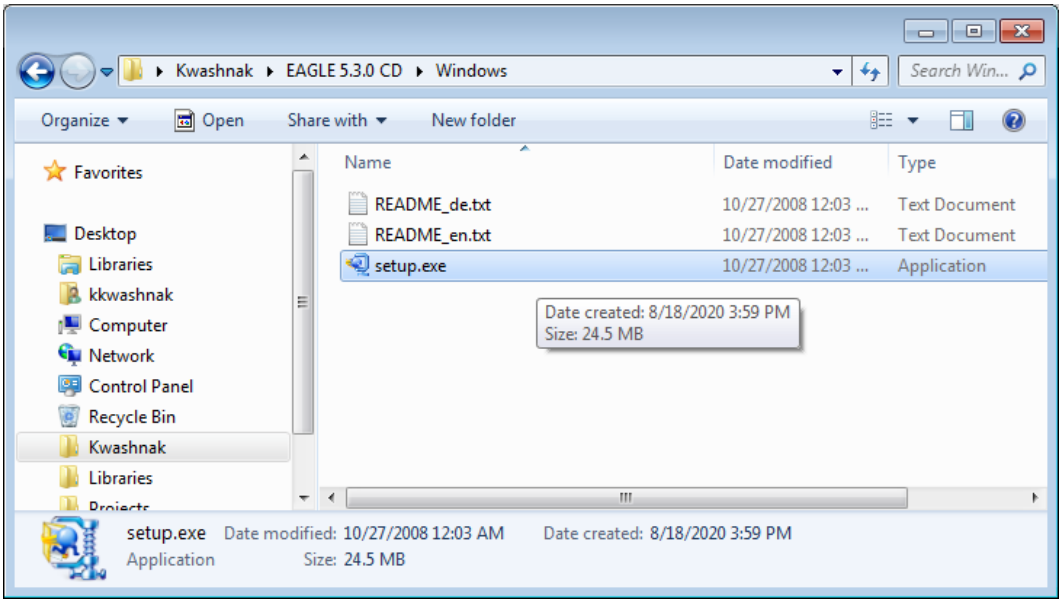


Fig. 11 Installation executable

A CadSoft dialog box appears. Click on the <Setup> button (Fig. 12). Follow the prompted instructions to install the software in a desired location on the OS (Figs. 13–15). Once the installation is completed, click on the <Finish> button (Fig. 16).

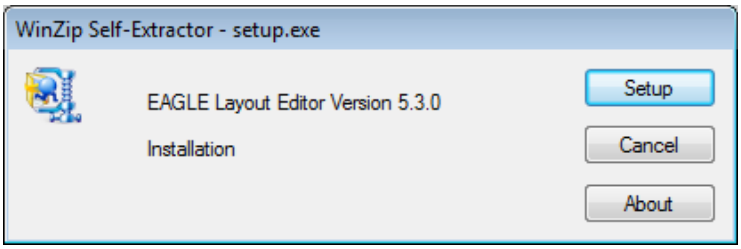


Fig. 12 File extraction splash screen

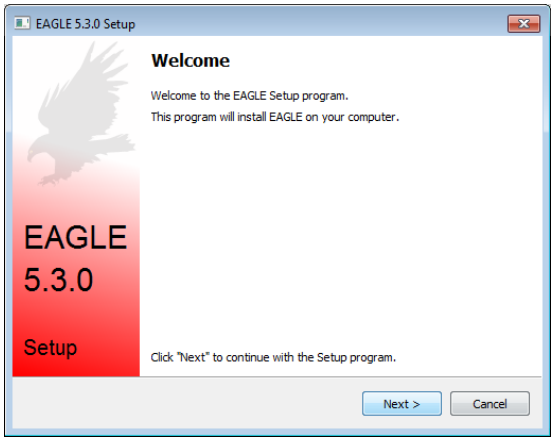


Fig. 13 Setup welcome screen

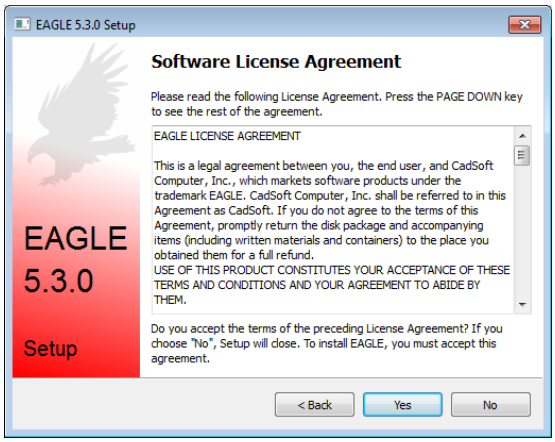


Fig. 14 CadSoft EULA

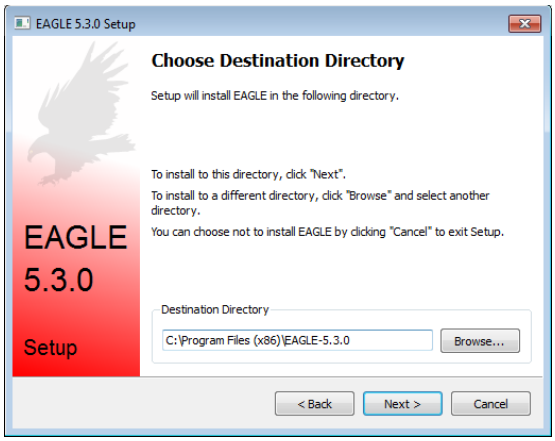


Fig. 15 Install directory location

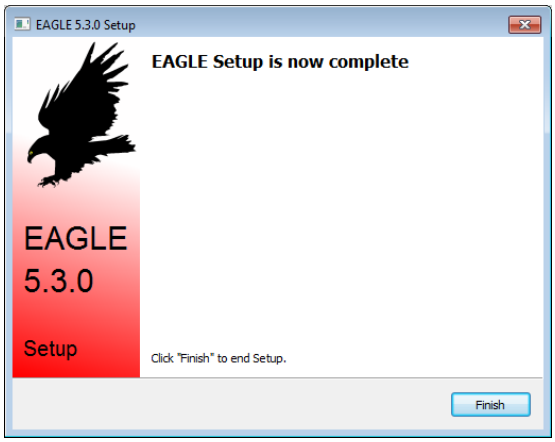


Fig. 16 Setup finish

Open the Windows Charm (Fig. 17) and search through the programs for the EAGLE Layout Editor 5.3.0 folder (Figs. 18 and 19). Left-mouse-click on the app to launch or right-mouse-click on the app to see a list of operations.

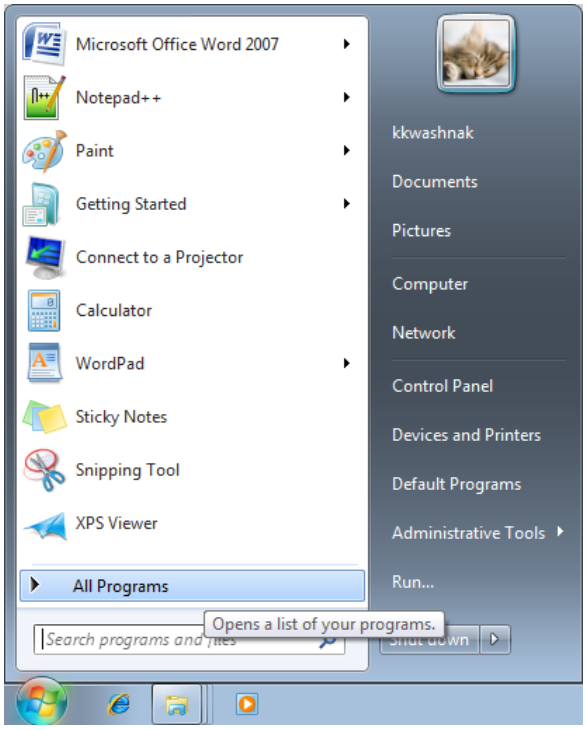


Fig. 17 Window's charm

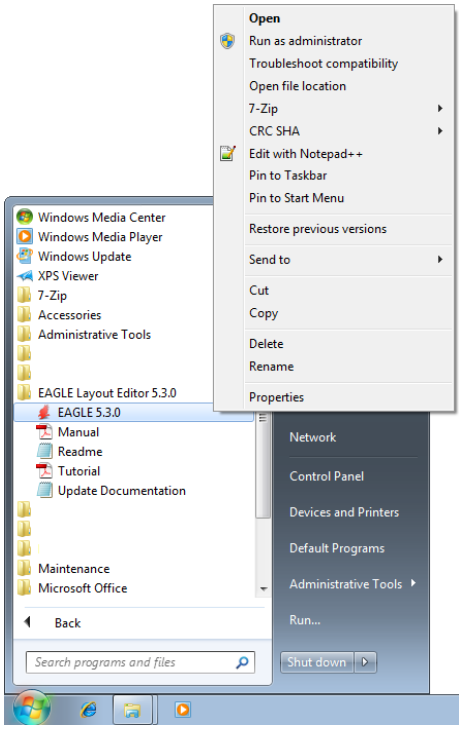


Fig. 18 Opening EAGLE application

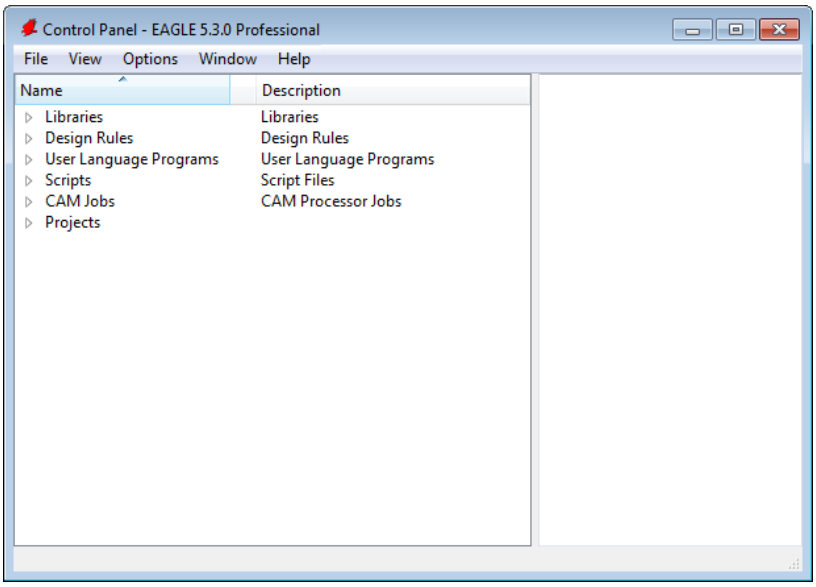


Fig. 19 EAGLE control panel

2.2 Creating a File Structure

Switch to the Windows File Explorer and open a file directory on the computer. Create a main directory location to house Eagle Library (ex.: .lbr) and Project Files (ex: .epf, .brd, .sch) as shown in Fig. 20.

For example:

- Main Directory: *C:\Users\kkwashnak\Desktop\Kwashnak*
- Eagle Libraries: *C:\Users\kkwashnak\Desktop\Kwashnak\Eagle Libraries*
- Eagle Projects: *C:\Users\kkwashnak\Desktop\Kwashnak\Projects*

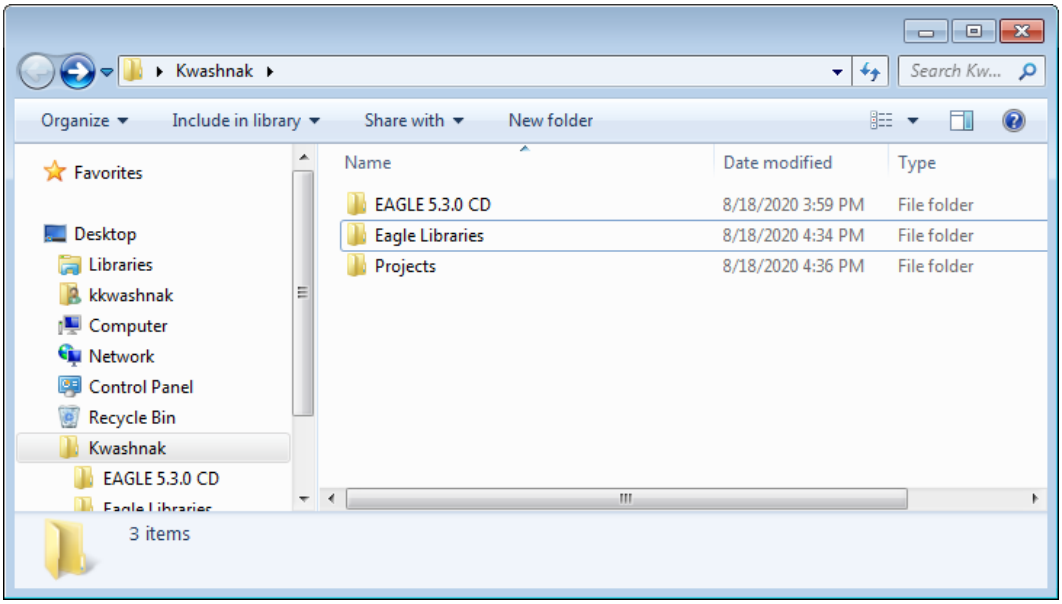


Fig. 20 File directory structure

Eagle Library files (.lbr) are a collection of symbols, footprints, and devices that are compiled into configurable components used in schematic and board files. The project file (.epf) assembles information about the project and associates the respective schematics (.sch) to board files (.brd).

2.3 Using the EAGLE Control Panel

Return to the EAGLE v5.3.0 application Control Panel and examine the main tabs: <File>, <View>, <Options>, <Window>, and <Help>. The Control Panel (Fig. 21) is the main interface to create, navigate, and configure project resources.

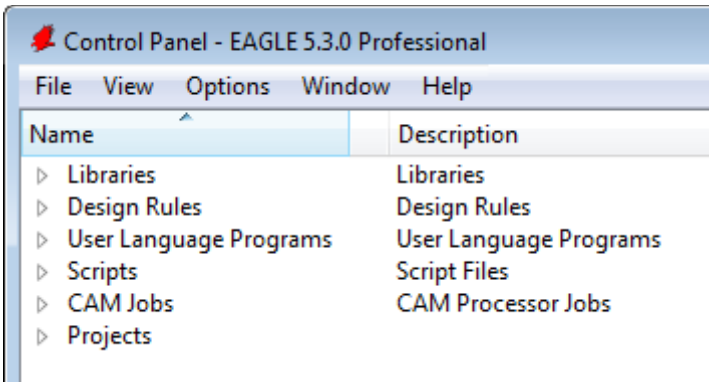


Fig. 21 EAGLE control panel tabs

2.3.1 File

The <File> tab (Fig. 22) contains options to create or open projects, schematics, boards, libraries, CAM jobs, scripts, and text files.

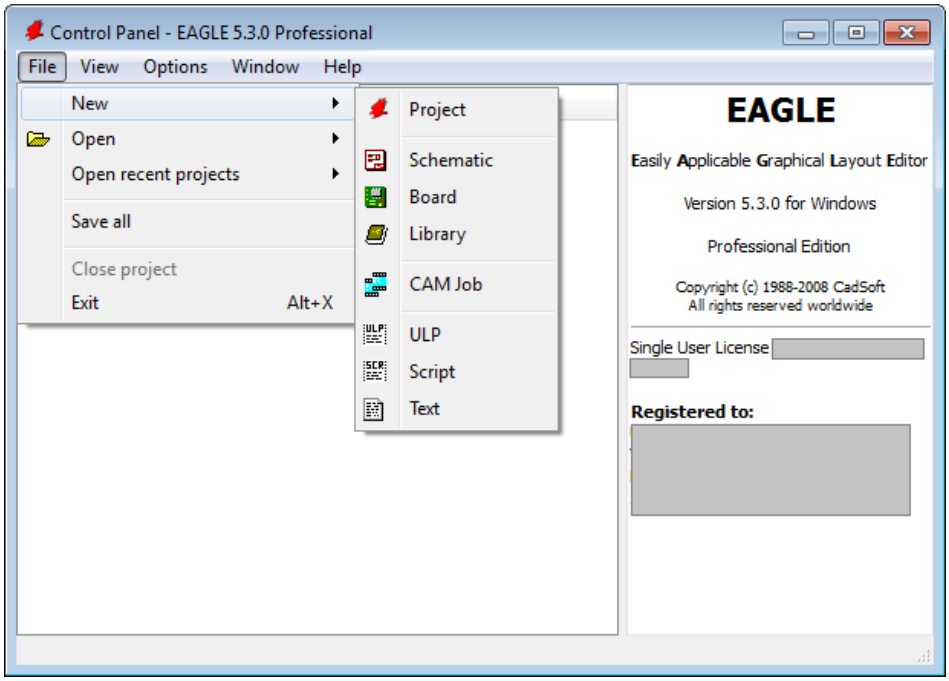


Fig. 22 EAGLE control panel, file tab

Creating a new project generates a 'Project' folder inside a specified project directory that will contain necessary schematic and board files (Fig. 23).

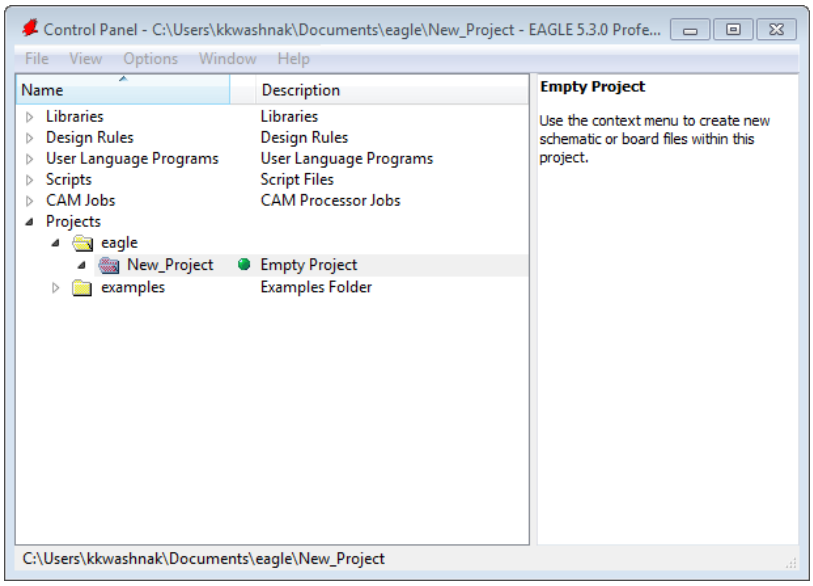


Fig. 23 Creating a new project

A schematic file (.sch) is the layout design of a system portraying components and their connections with other elements, such as microcontrollers, resistors, capacitors, power supply lines, ground, and signals lines (Fig. 24).

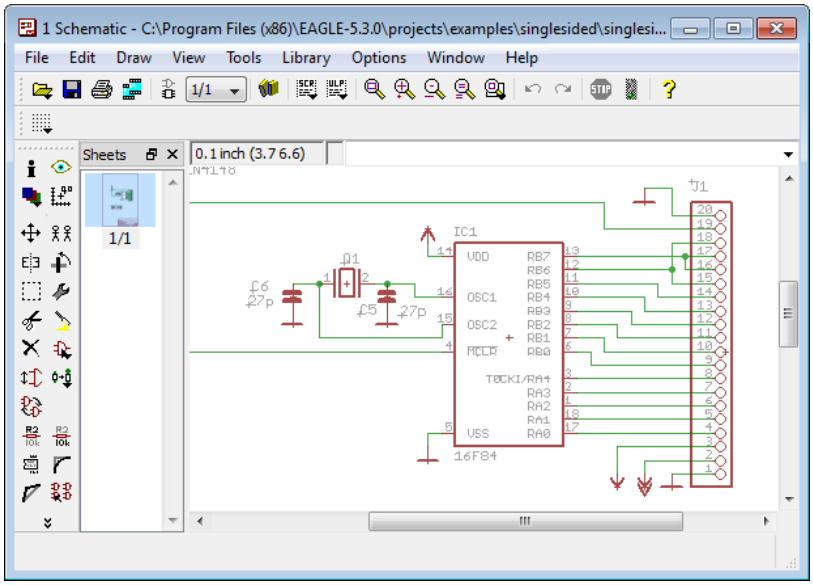


Fig. 24 Example of a schematic

A board file (.brd) is the collection of schematic elements that are placed onto a physical PCB (Fig. 25). The board file defines the overall shape and dimension of the PCB. Components are rearranged, organized, and connected to other components via traces.

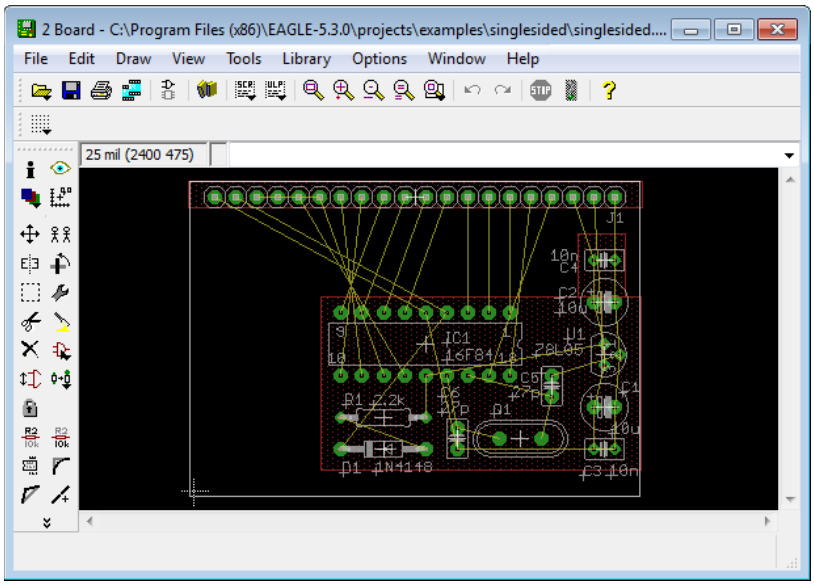


Fig. 25 Example of a board

Library files (.lbr) contain schematic symbols, board component footprints, and compiled devices (associates symbols to footprints (Fig. 26).

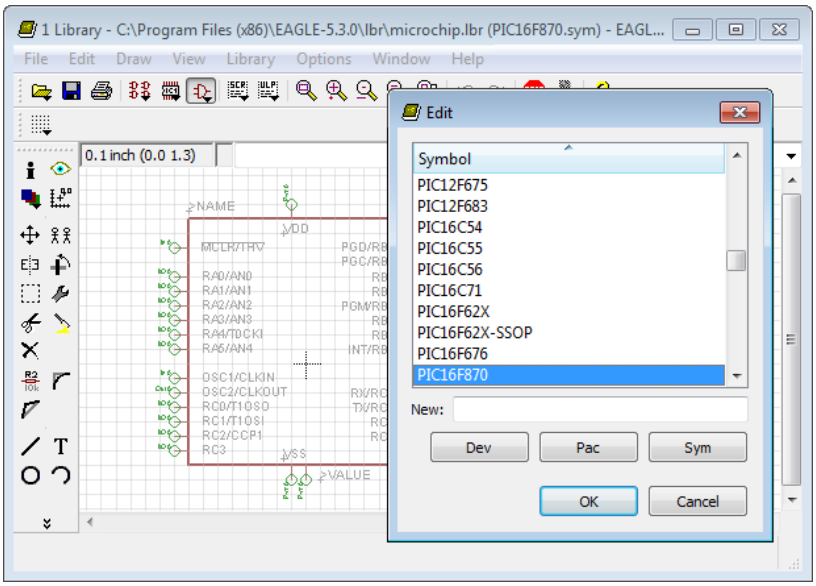


Fig. 26 Example of a schematic

A CAM job creates required files necessary for PCB fabrication (Fig. 27).

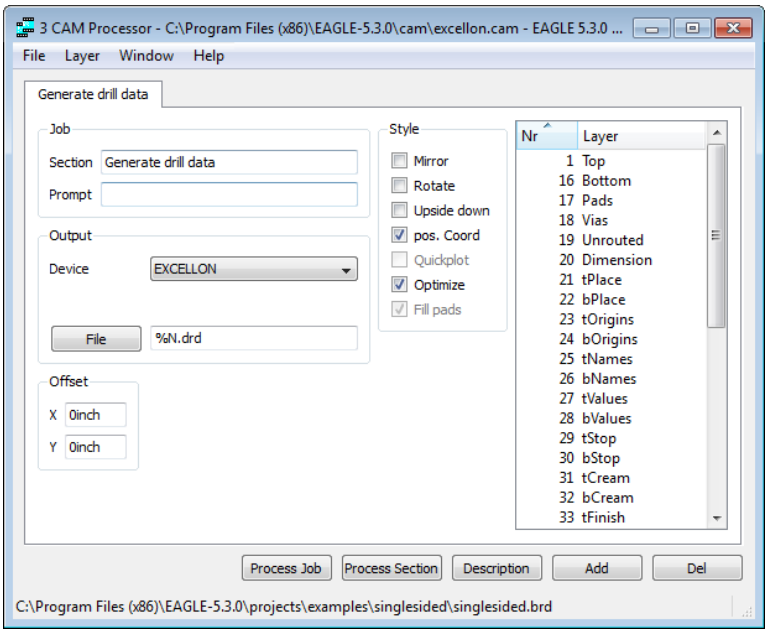


Fig. 27 Example CAM processor

User Language Programs (ULPs) (.ulp) are code that automates tedious tasks and intricate processes (Fig. 28).

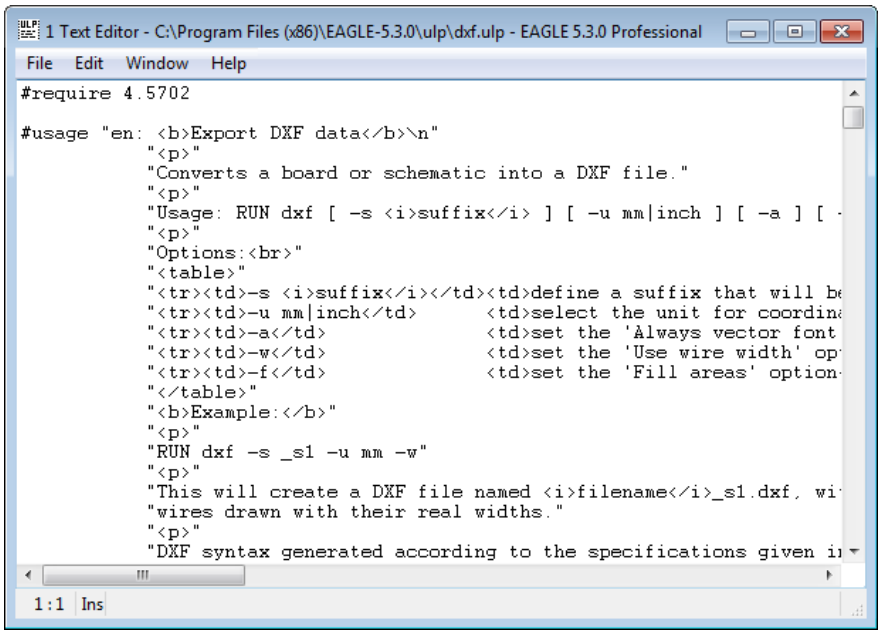


Fig. 28 Example ULP

Script files (.scr) are code for configuring EAGLE default values, such as grid options, custom menus, shortcuts, and drill values (Fig. 29).

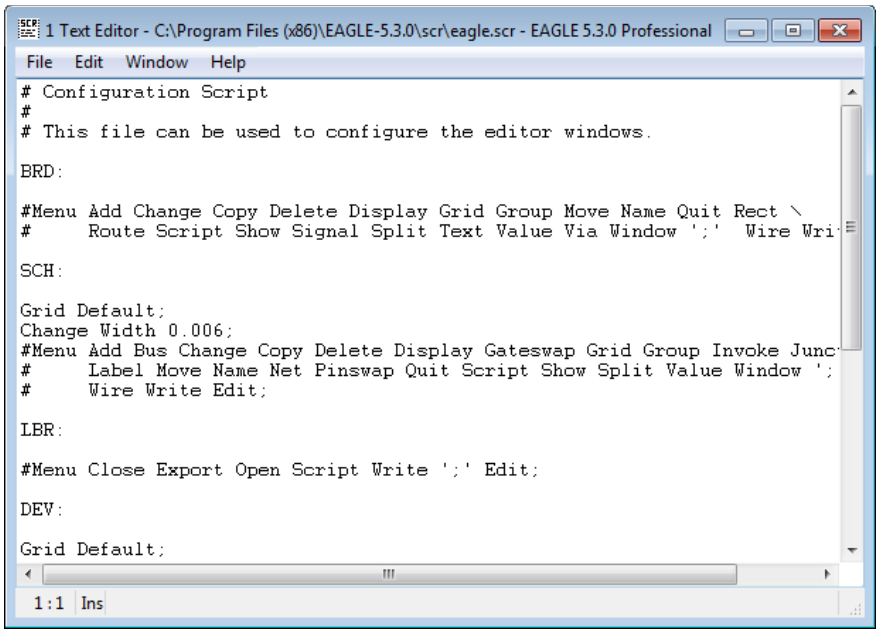


Fig. 29 Example script

Text files (.txt) are a workspace for creating ULPs, scripts, or general text-based files (Fig. 30).

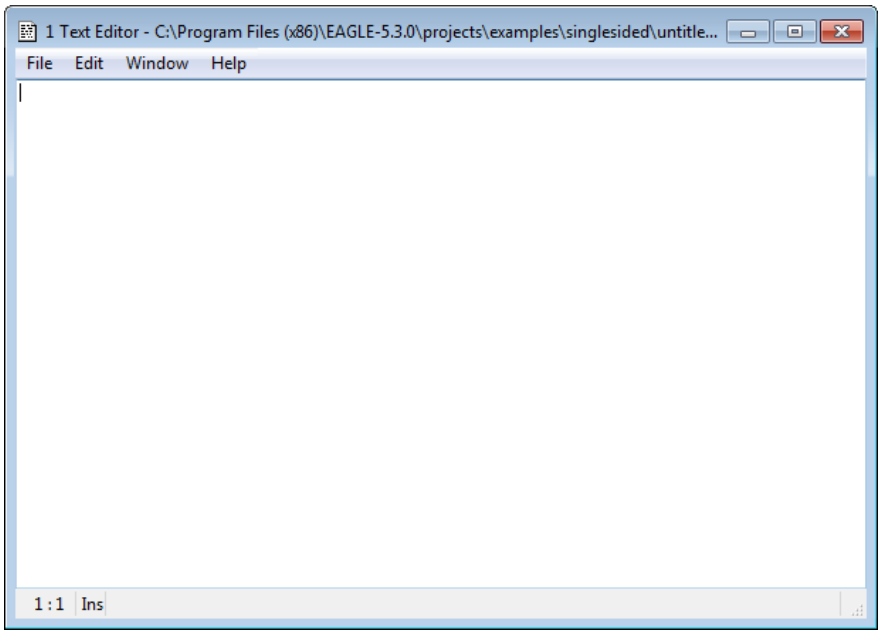


Fig. 30 Example text editor

2.3.2 View

The <View> tab covers two options, <Refresh> and <Sort> (Fig. 31). <Refresh> restarts the Control Panel GUI contents, which allows for file discovery. <Sort> reorganizes file contents, either by file alphabetical name or file program type.

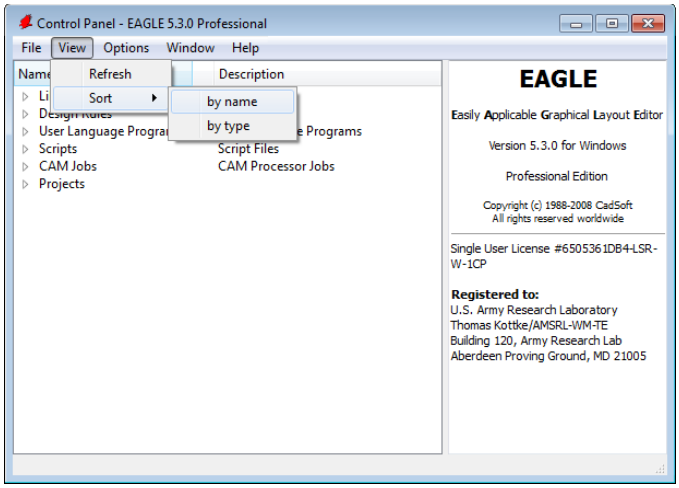


Fig. 31 View tab

2.3.3 Options

The <Options> tab contains <Directories>, <Backup>, <User Interface>, and <Window positions> (Fig. 32). The <Directories> option allows configuration of source file locations. <Backup> configures the auto-save feature. <User Interface> configures EAGLE GUI components. <Window positions> saves or deletes the various screen coordinates for later use.

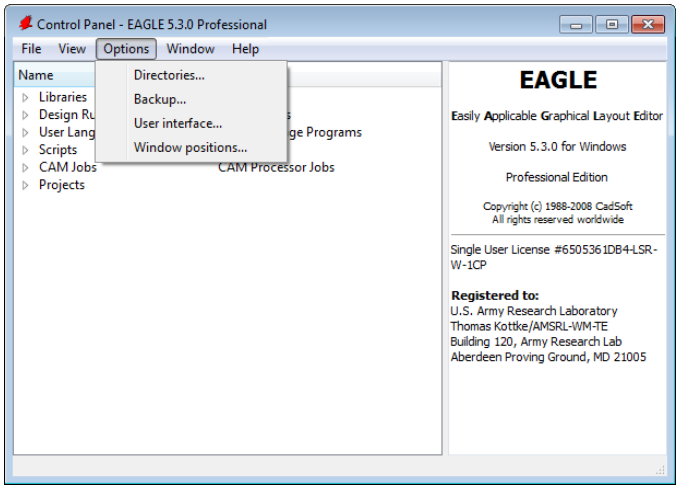


Fig. 32 Options tab

2.3.4 Window

The <Window> tab allows the user to navigate through the multiple open windows in the EAGLE program (Fig. 33).

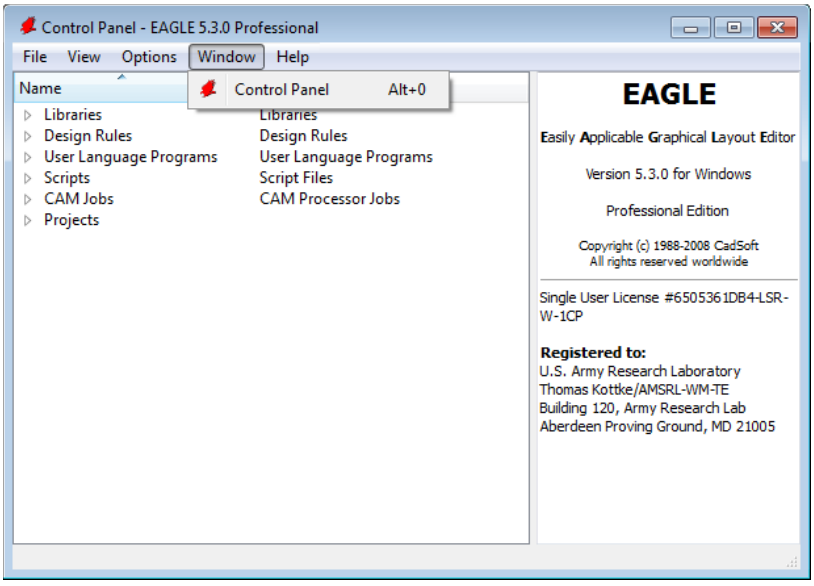


Fig. 33 Window tab

2.3.5 Help

The <Help> tab contains general information about the EAGLE program (Fig. 34). The <General> and <Context> options both yield a wealth of information on using the program.

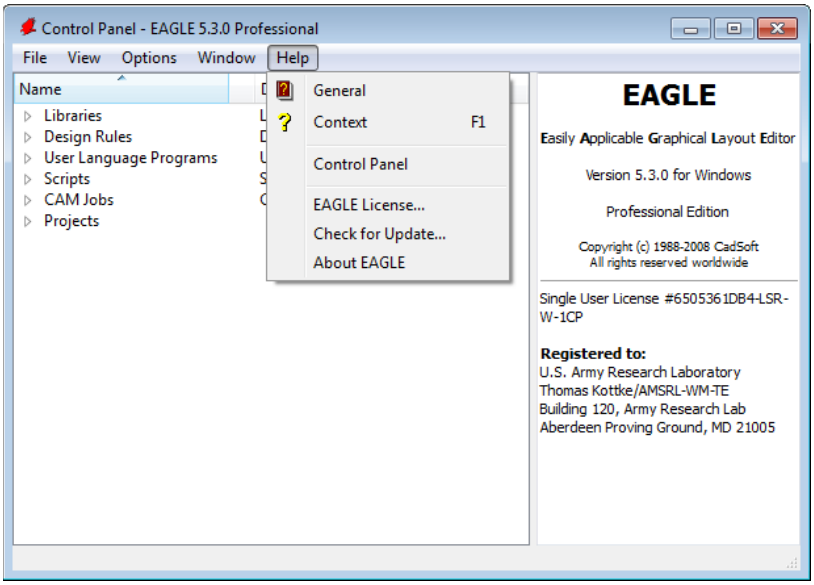


Fig. 34 Help tab

2.4 Configuring the Directory

On the EAGLE Control Panel's top ribbon, go to <Options>, <Directories>. Add the recently created Projects folder to EAGLE's 'Projects' pathway and add the recently created EAGLE Libraries folder to EAGLE's 'Libraries' pathway (Fig. 35). Add a pathway to the textbox by entering ";" after the previous text and immediately paste the Windows address (do not leave a space between the ";" and the address). Afterward, click <OK> to exit.

Directories before revising folders are shown in Fig. 35.

Libraries: *$EAGLEDIR\lbr*

Projects: *$HOME\eagle;$EAGLEDIR\projects\examples*

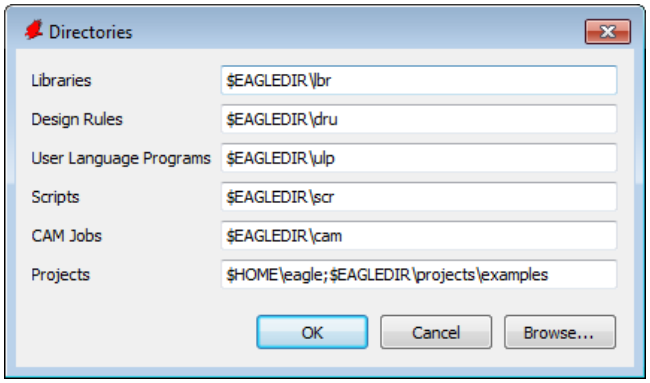


Fig. 35 Directory, initial setup

Directories after revising folders are shown in Fig. 36.

Libraries: *$EAGLEDIR\lbr;C:\Users\kkwashnak\Desktop\Kwashnak\Eagle Libraries*

Projects: *$HOME\eagle;$EAGLEDIR\projects\examples;C:\Users\kkwashnak\Desktop\Kwashnak\Projects*

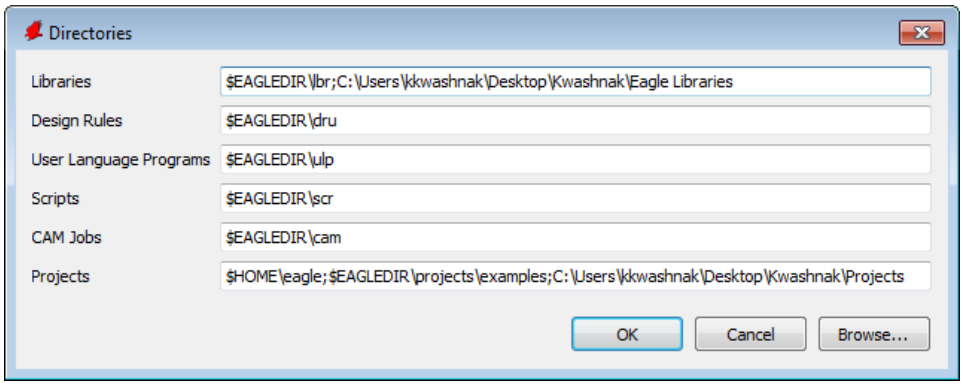


Fig. 36 Directory, sourced pathways

Once the Project and Library folders are included into the EAGLE directory, click <OK>. The EAGLE Control Panel will automatically refresh. If not, use <View>, <Refresh>.

In the Control Panel's element tree, click the drop-down < ►> on <Projects> top-level heading and right-mouse-click on the <Projects> folder (Fig. 37). On the drop-down menu, click <New Project> and name the project. For instance, the new folder was named “Example” (Fig. 38).

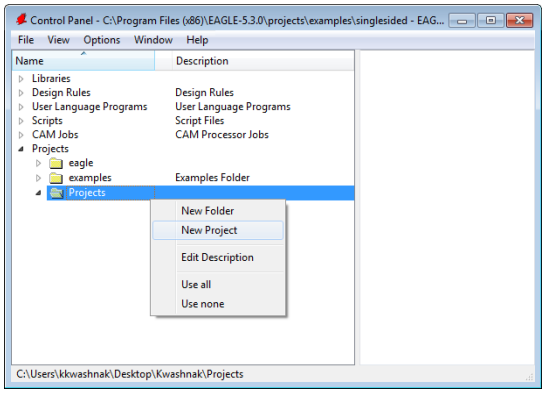


Fig. 37 Projects directory structure

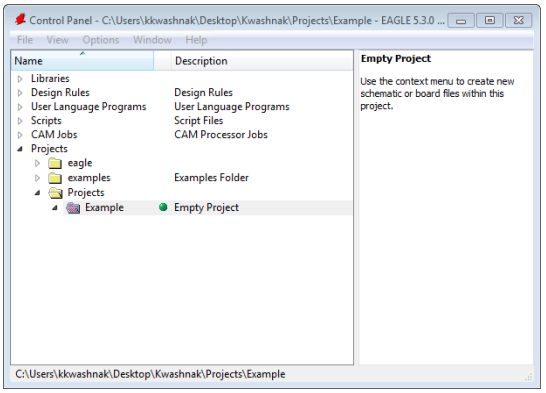


Fig. 38 Creating a new project

Upon creation of the project, a red folder icon will appear and there will be a green dot next to the description. The red folder indicates a project and the green dot signifies that the project is active. Only one project can be active per EAGLE instance (one may open multiple instances of EAGLE at a time). To activate/deactivate a project, click the dot; it will cycle for green-active (Fig. 39) and gray-inactive (Fig. 40). Active translates to working on the current project and linking the project schematic with the board files.

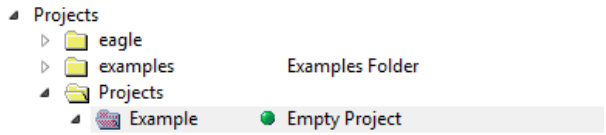


Fig. 39 Active project

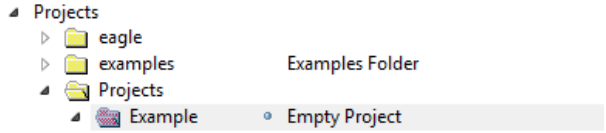


Fig. 40 Inactive project

Note, a new folder appears in the file structure:

C:\Users\kkwashnak\Desktop\Kwashnak\Projects\Example

2.5 Creating a Schematic and Board

To start creating a schematic, go to the top ribbon of the Control Panel, select <File>, <New>, and click on <Schematic> (Fig. 41). Once the schematic editor screen opens (Fig. 42), save the file in the project directory (Fig. 43):

C:\Users\kkwashnak\Desktop\Kwashnak\Projects\Example

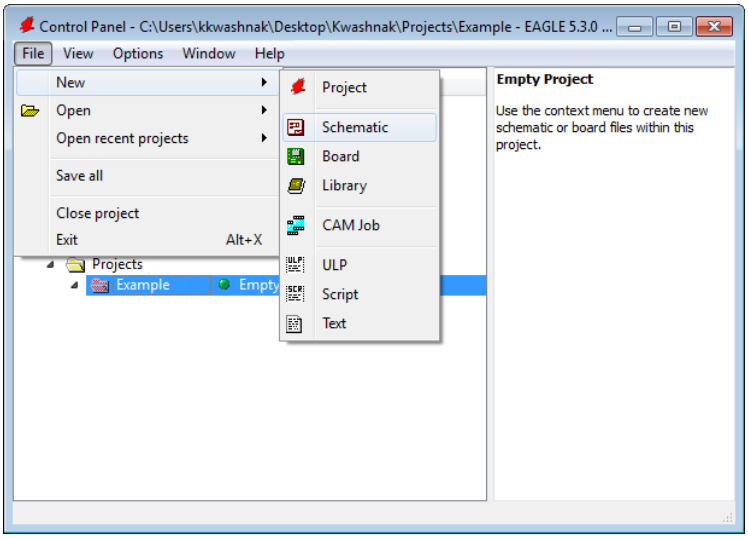


Fig. 41 Creating a schematic

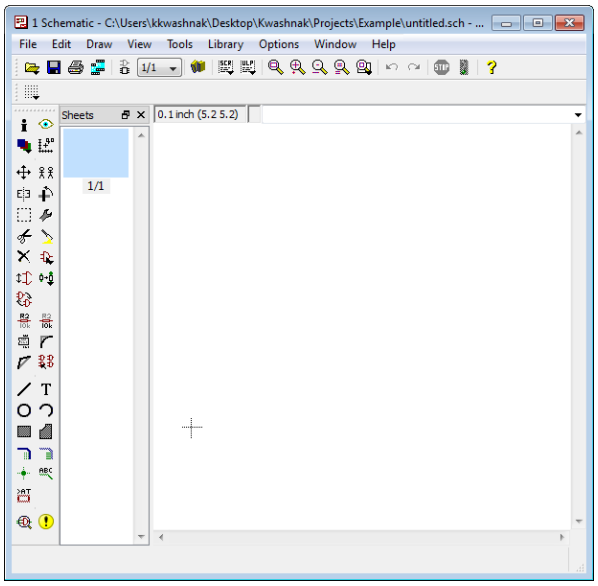


Fig. 42 Schematic editor

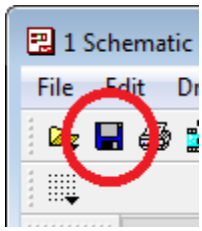


Fig. 43 Save button

Next, click on the <Display> icon, shown in Fig. 44.

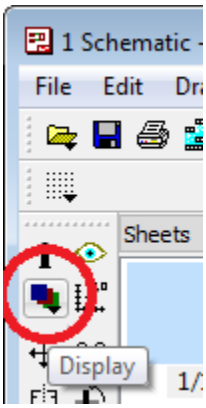


Fig. 44 Display (layer) icon

The selected layers will be visible on the schematic's workspace (Fig. 45). Edit the layer's properties by pressing the <Change> button (Fig. 46). Follow Table 5 for general layer-setting guidelines.

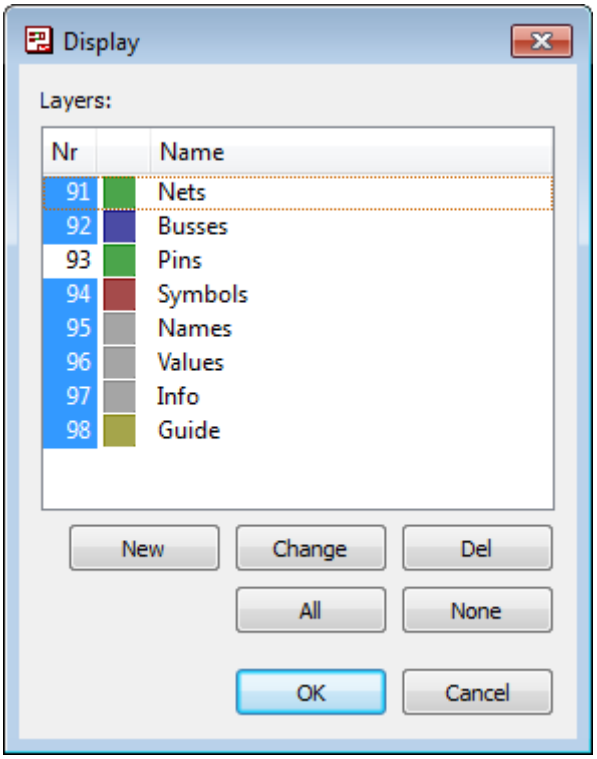


Fig. 45 Schematic layer view and values

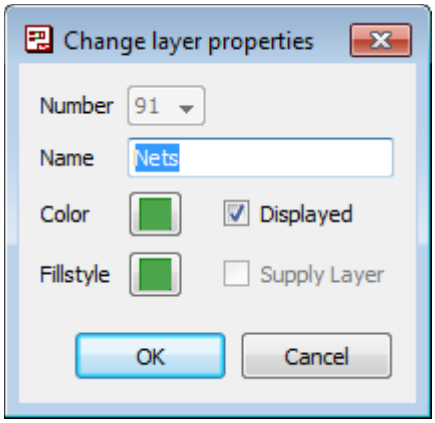


Fig. 46 Layer properties

Table 5 Schematic layer settings

Schematic editor					
No.	**Name**	**No.**	**Color**		**Comment**
1	Nets	91	Dark green		Connection lines
2	Buses	92	Dark purple		Consists of multiple nets
3	Pins	93	Dark green		Connection point
4	Symbols	94	Dark red		Component graphics
5	Names	95	Dark gray		Component's name
6	Values	96	Dark gray		Component's value
7	Info	97	Dark gray		Supplemental information
8	Guide	98	Dark yellow		Supplemental information

Once all schematic layer values are set, click on the <Board> icon to swap to the EAGLE Board Editor (Fig. 47).

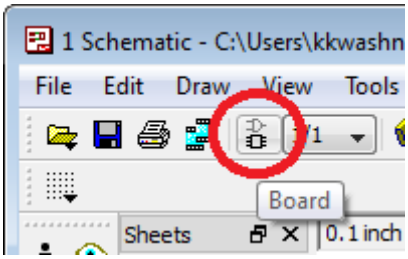


Fig. 47 Schematic/board icon

Since the board file is extracted from the schematic view, a prompt appears as shown in Fig. 48.

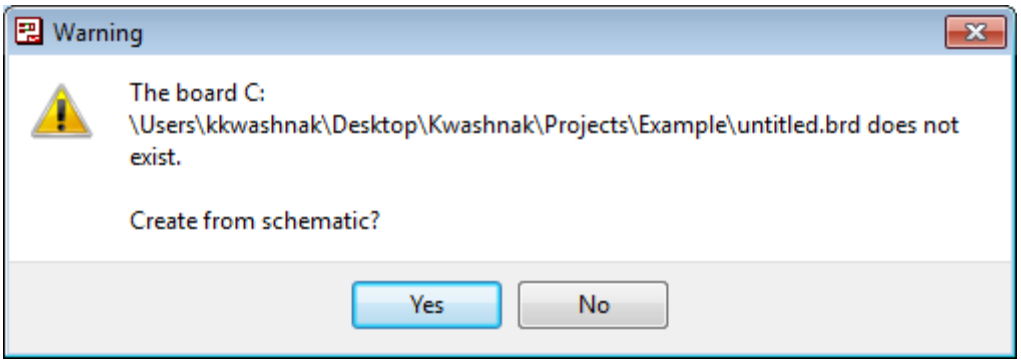


Fig. 48 Warning message, create board file from schematic

Click <Yes> to create the board file from the schematic and the Board Editor will appear (Fig. 49).

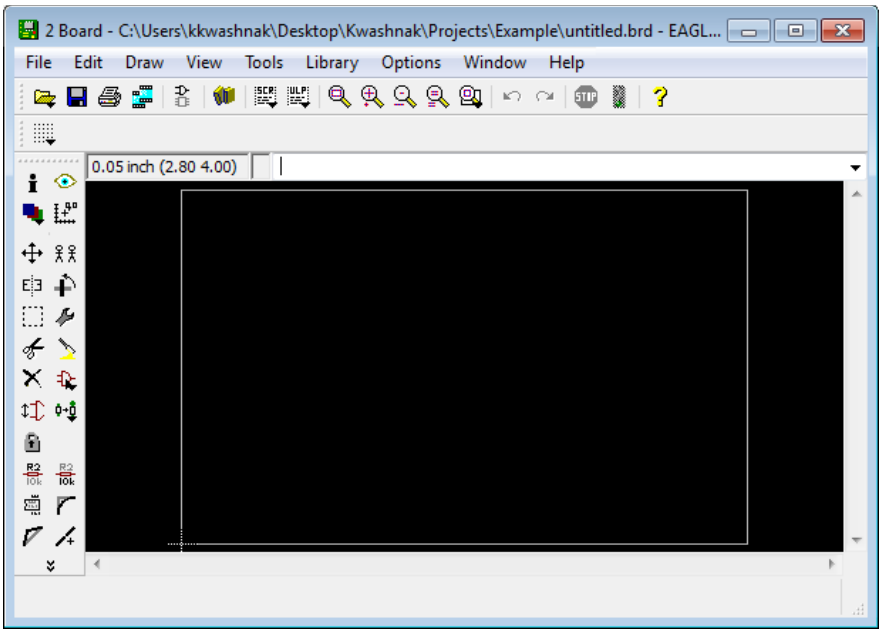


Fig. 49 Board editor

Use the <Display> button to configure layer settings for the EAGLE Board Editor. Table 6 indicates the general configuration settings for the main layers in EAGLE Board Editor. Note that the convention is lighter color on the top side of board.

After reviewing the board settings, save the file in the project directory:

C:\Users\kkwashnak\Desktop\Kwashnak\Projects\Example.

Table 6 EAGLE board editor settings

Board Editor								
No.	**Layer Group**	**Name**	**No.**	**Color Name**	**Color**		**Comment**	**Gerber**
1	Top silkscreen	tPlace	21	Light gray			. . .	.tslk
2	Green top	tStop	29	Black with Line			Keep out region	.tstp
3	Top copper	Top, pads, vias	1, 17, 18	Red, dark green, dark green			. . .	.tcpr
4	Bottom copper	Bottom, pads, vias	16, 17, 18	Blue, dark green, dark green			. . .	.bcpr
5	Green bottom	bStop	30	Black with Line			. . .	.bstp
6	Bottom silkscreen	bPlace	22	Dark gray			. . .	.bslk
7	Board outline	Dimension	20	Light green			. . .	.dout
8	Drills, holes	Drills, holes	44, 45	Dark gray, dark gray			. . .	.ddrl
9	Top restriction zone	tRestrict	41	Red with dots			. . .	. . .
10	Bottom restriction zone	bRestrict	42	Blue with dots			. . .	. . .
11	Origins, top	tOrigins	23	Light purple			Part manipulation	. . .
12	Origins, bottom	bOrigins	24	Dark purple			Part manipulation	. . .
13	Name, top component	tNames	25	Light gray			Appears on silkscreen	. . .
14	Name, bottom component	bNames	26	Dark gray			Appears on silkscreen	. . .
15	Document notes, top	tDocu	51	Light yellow			PCB physical view	. . .
16	Document notes, bottom	bDocu	52	Dark yellow			PCB physical view	. . .

2.6 Configuring the Design Review Check (DRC)

On the EAGLE's board editor, click on the Design Review Check <Drc> button (Fig. 50). This option configures the board's properties and creates rules to assist with the overall structure of the PCB. These rules should be reviewed with respect to a manufacturer's requirements.

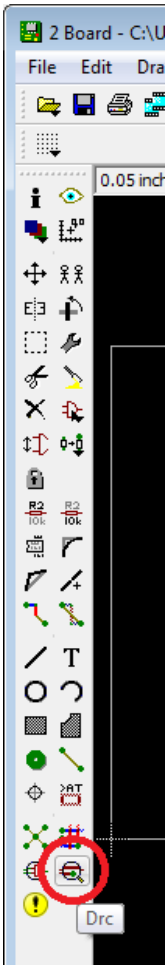


Fig. 50 Board editor DRC

In Fig. 51, after clicking on the <DRC> button, the DRC (default) window appears (Fig. 52). Edit the project's Design Rules description with the <Edit Description...> button or use the <Load> / <Save as...> button (see Appendix B, HTML, and Appendix C, Sample Library Device HTML Description). Text entry follows basic HTML formatting.

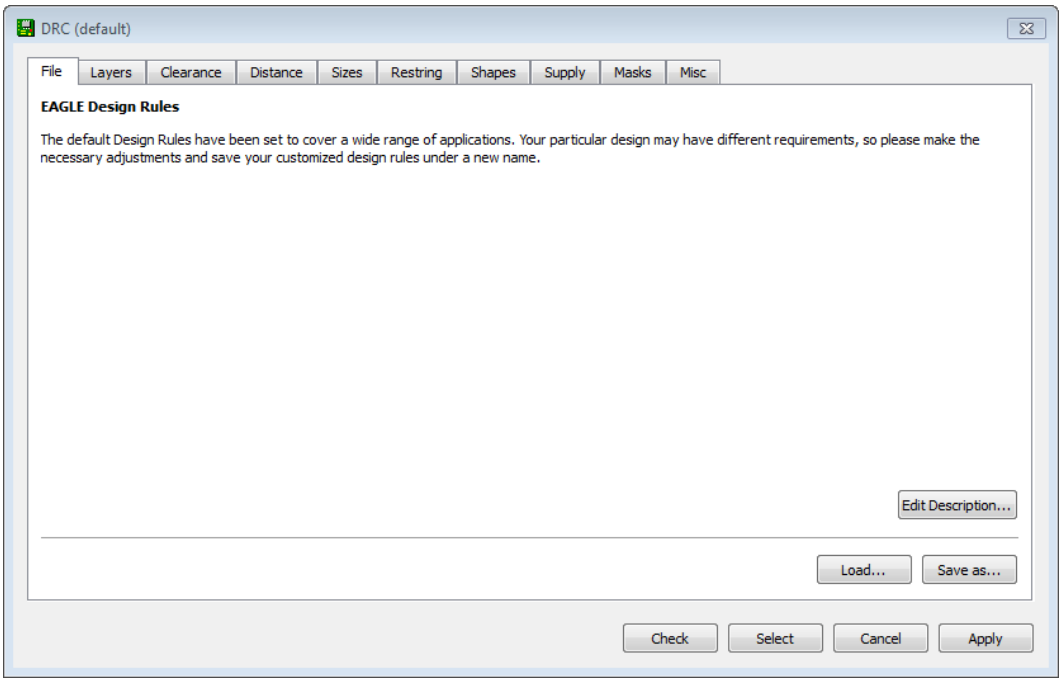


Fig. 51 DRC

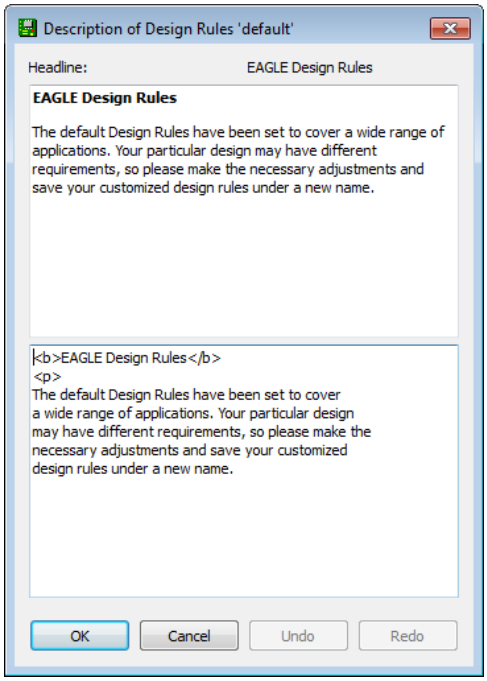


Fig. 52 DRC description

The ‘Layers’ tab controls each layer’s copper thickness and isolation materials (Fig. 53). The setup field defines the board’s construction (Table 7).

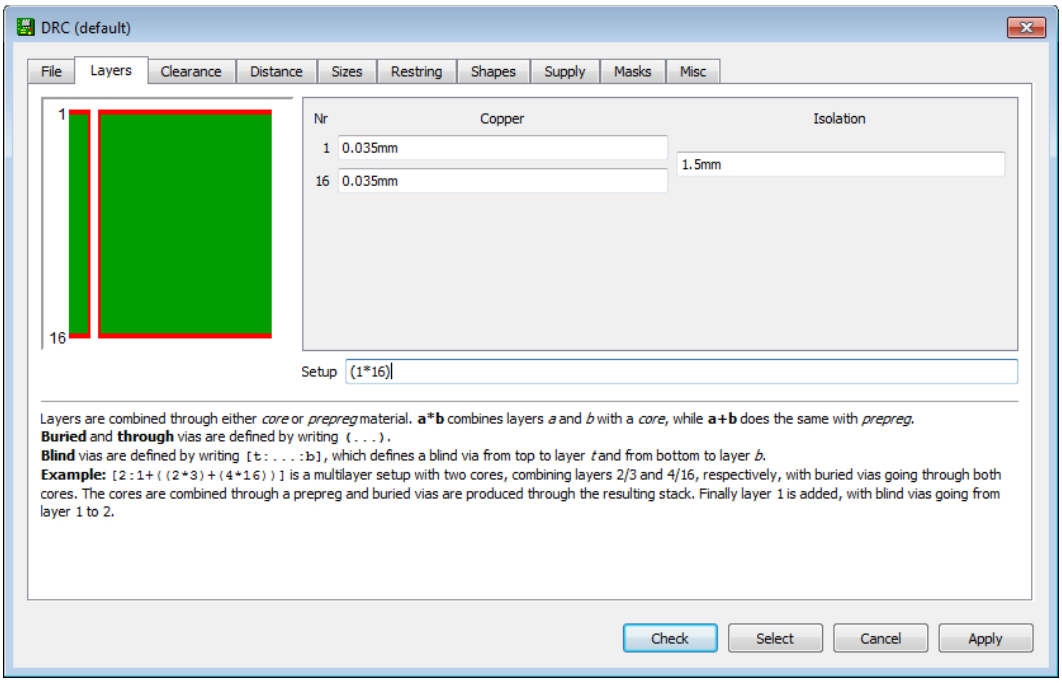


Fig. 53 DRC layers

Table 7 DRC, layer tab, setup definitions

Convention	Definition	Example
*	Core material	FR4 or similar material
+	Prepreg	Isolation material
...	Via	…
t:...:b	Blind Via	t and b are layer numbers, top and bottom, respectively

The example board is set with (1*16), meaning a two-layer board with layers 1 and 16 paired and vias going through both layers.

The following are examples from MIT archives[35]:

An example of a multilayered board would be ((1 * 2) + (15 * 16)):

- layer set 1, layers 1 and 2 are paired
- layer set 2, layers 15 and 16 are paired
- layer sets 1 and 2 combined via prepreg material in between
- vias are drilled through the entire board

The difference between buried and blind vias is the distinction on what layers they pass through. Vias that go through the entire board, not connecting the top and

bottom layer) are referred to as buried vias, while vias that go to and from select layers are called blind vias.

The following is an example of a multilayered board with blind vias, (2:1 + ((2 * 3)+(14 * 15)) + 15:16):

- layer set 1, layer 2 and 3 are paired
- layer set 2, layer 14 and 15 are paired
- layer set 1 and 2 are combined via prepreg material in between
- via from layer 2 to layer 1, thus connecting layer 1 to layer 2
- via from layer 15 to layer 16, thus connecting layer 15 to layer 16

Also, blind vias can be through inner layers, (2:1 + (3:2 + (3 * 4) + 5:4) + 16:5):

- layer set 1, layer 3 and 4 are paired
- via from layer 3 to layer 2
- via from layer 5 to layer 4
- via from layer 16 to layer 5
- via from layer 2 to layer 1

The ‘Clearance’ tab describes the minimum distance between object signal layers (Fig. 54).

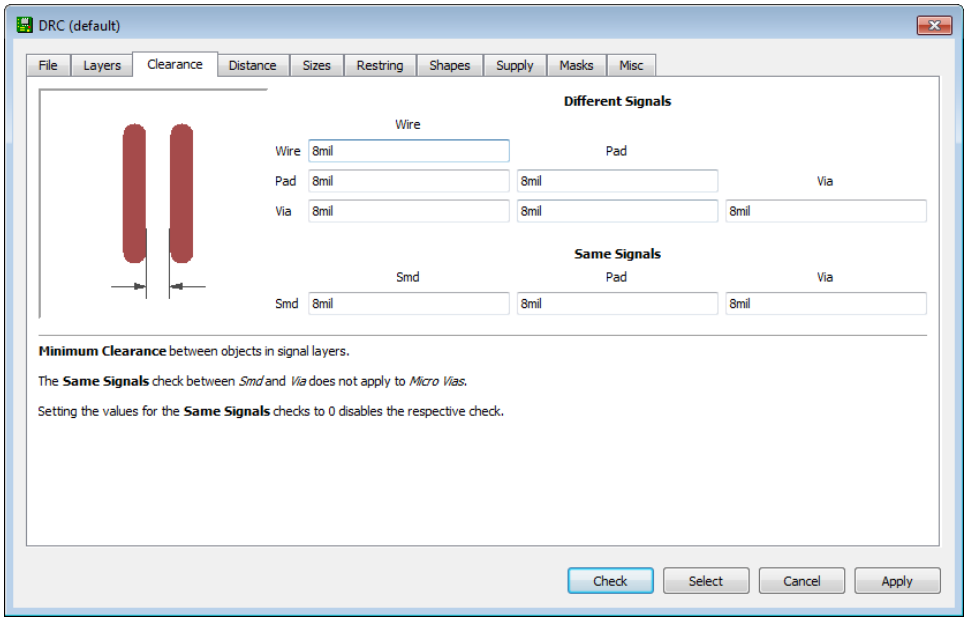


Fig. 54 DRC clearance

The ‘Distance’ tab describes the minimum distance between objects in signal layers, dimensions, and between drill holes (Fig. 55).

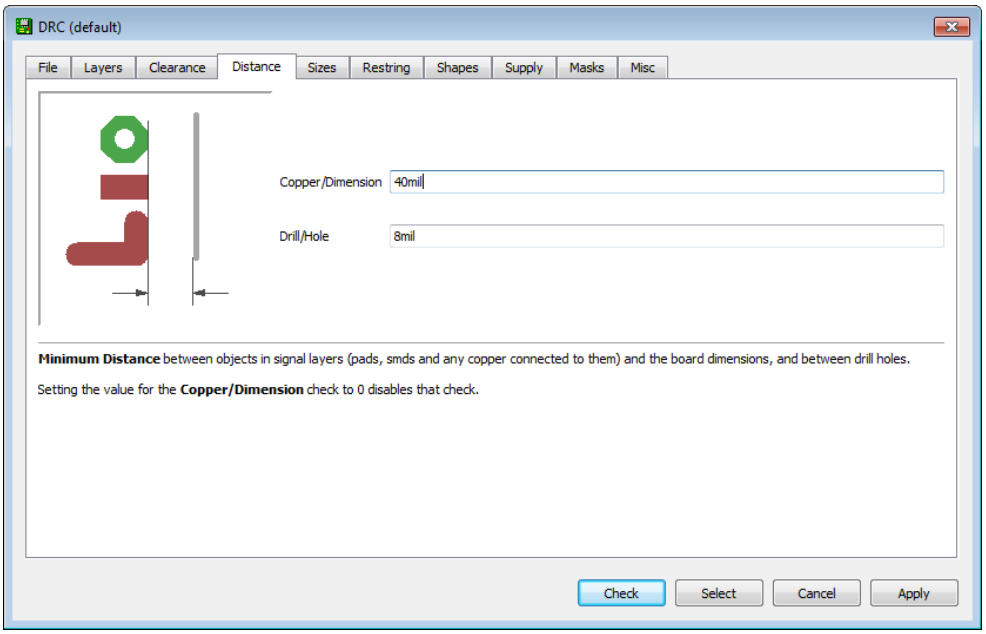


Fig. 55 DRC distance

The ‘Sizes’ tab describes the minimum width of any objects in the signal layers and drill holes (Fig. 56).

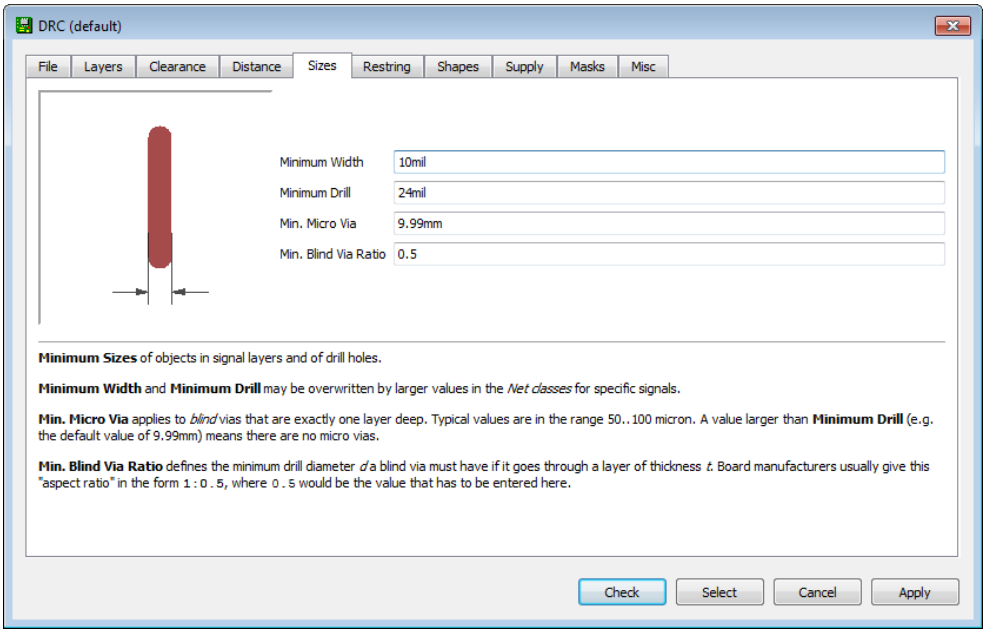


Fig. 56 DRC sizes

The ‘Restring’ tab describes the width of the copper ring that has to remain after the pad or via that has been drilled (Fig. 57).

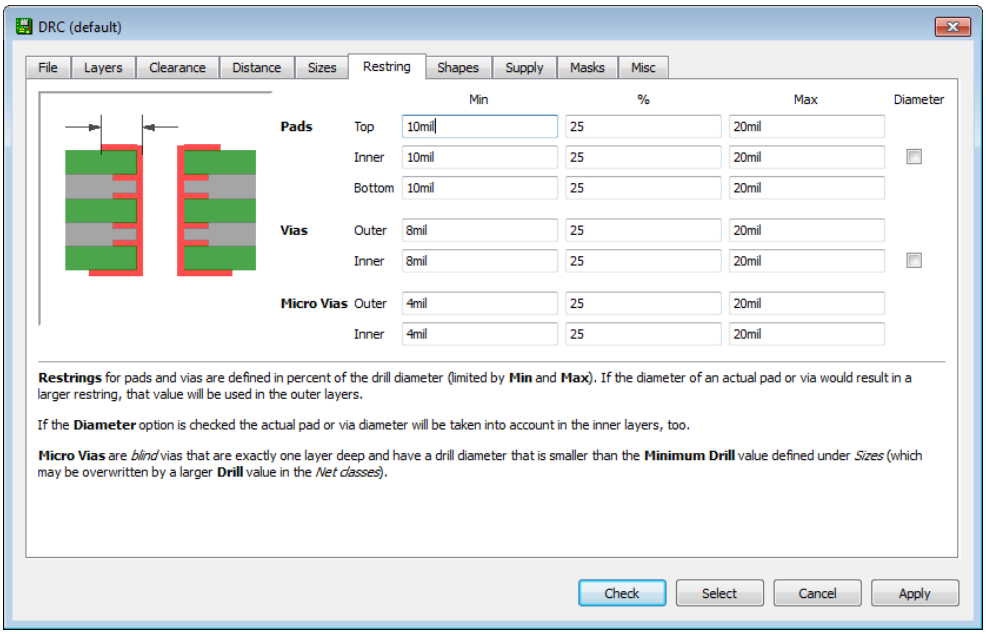


Fig. 57 DRC restring

The ‘Shapes’ tab describes the geometry of SMDs and pads (Fig. 58).

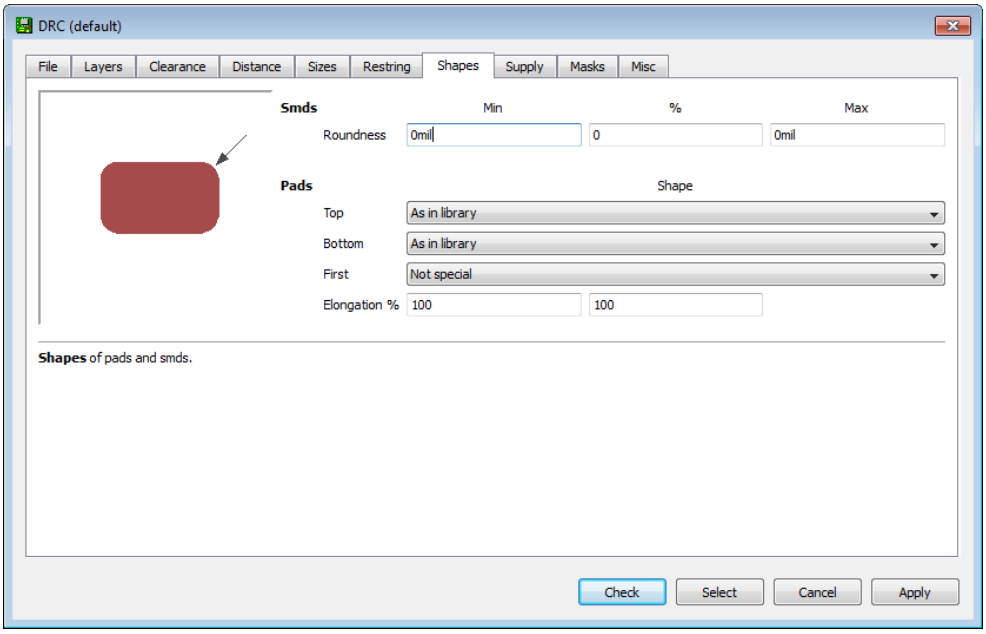


Fig. 58 DRC shapes

The ‘Supply’ tab describes the geometry of the thermal and annulus symbols used in the supply layers (Fig. 59).

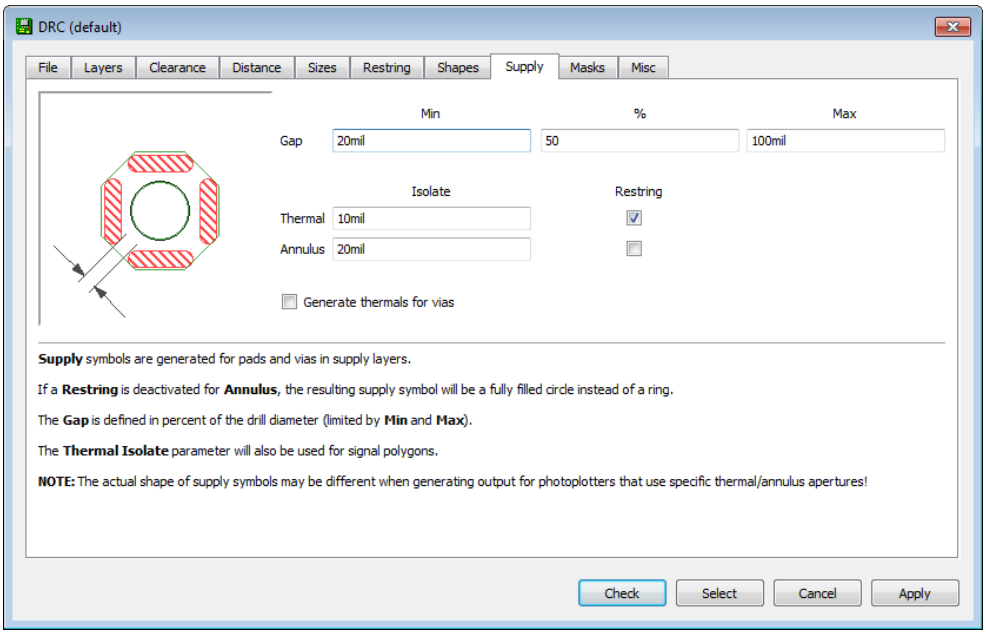


Fig. 59 DRC supply

The ‘Masks’ tab describes the dimensions of the solder stop and cream masks (Fig. 60).

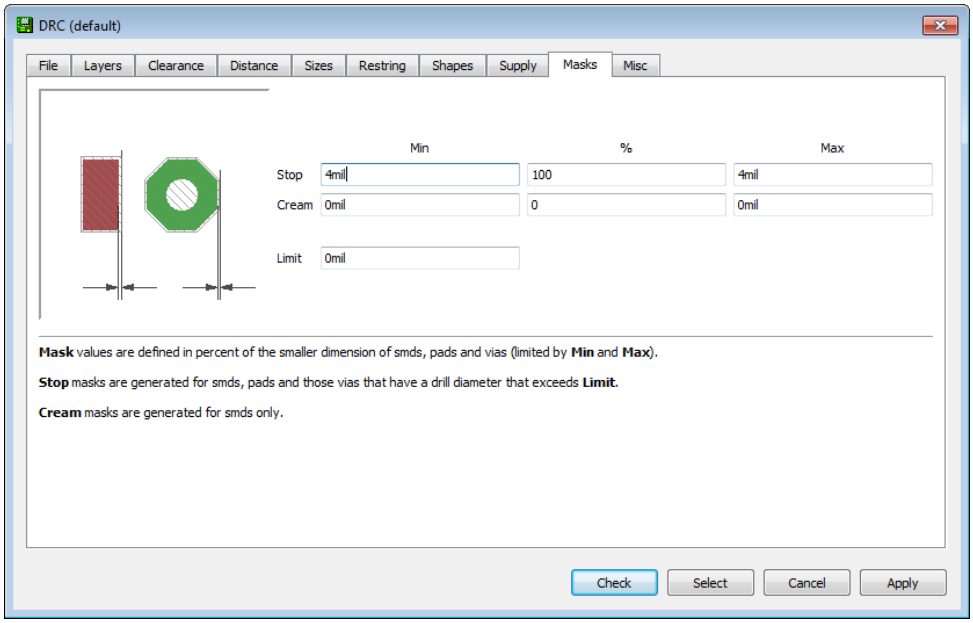


Fig. 60 DRC masks

The ‘Misc’ tab describes the grid settings and angle checks (Fig. 61).

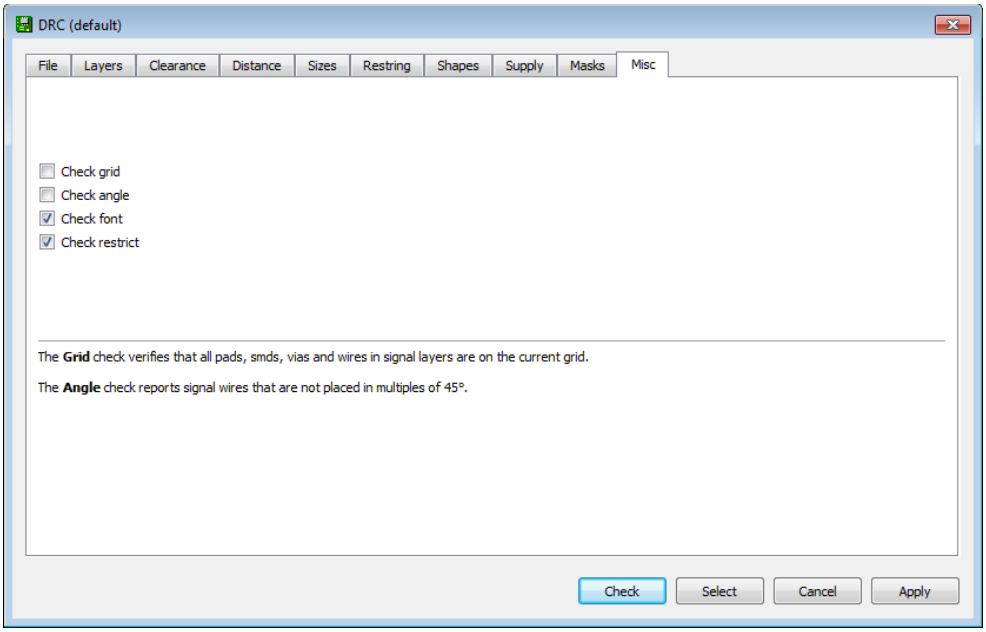


Fig. 61 DRC misc

3 Creating a Component

3.1 Creating a Library

In order to populate a schematic and a board, one must create or use a library file, which contains component information such as symbols, footprints, and devices. The Library may contain multiple variations of a component, as well as several other devices related to the library. Typically a library file is dedicated to one manufacturer of a particular series of hardware. For example, a manufacturer may make an EAGLE library that is specific to their line of microcontroller devices.

On the EAGLE Control Panel’s top ribbon, navigate to <File>, <New>, and <Library> (Figs. 62 and 63).

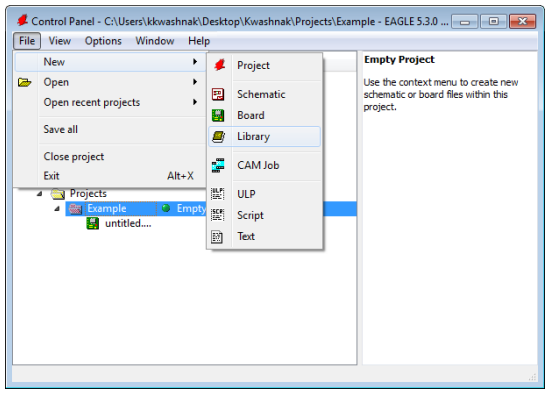


Fig. 62 Creating a new library

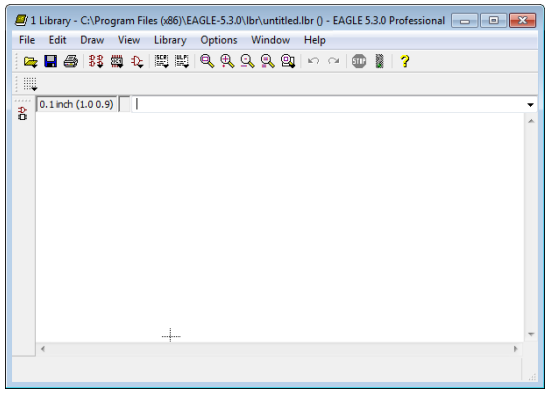


Fig. 63 Library editor

Save the library in the Eagle Libraries folder:

C:\Users\kkwashnak\Desktop\Kwashnak\Eagle Libraries

For this walkthrough, the library is named “ExampleManu”.

If you need to open a library file, such as “ExampleManu”, on the EAGLE Control Panel, go to <File>, <Open>, and <Library> (Fig. 64). Browse the file explorer for the specified file. Then select the .lbr and click <Open> (Fig. 65).

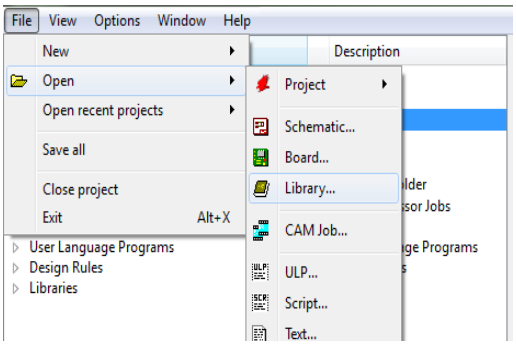


Fig. 64 Opening a library

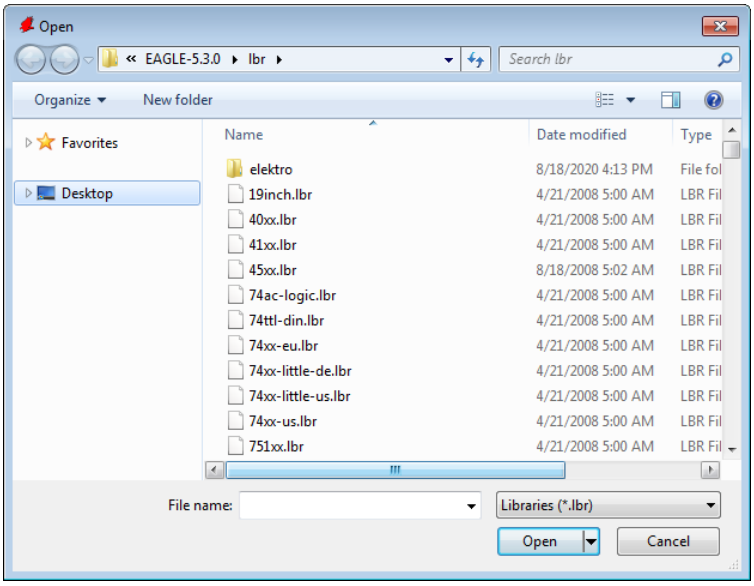


Fig. 65 Base library file directory

The base EAGLE directory for libraries was mounted upon installing the software as follows:

C:\Program Files (x86)\EAGLE-5.3.0\lbr

To open the recently created library file, “ExampleManu”, navigate to

C:\Users\kkwashnak\Desktop\Kwashnak\Eagle Libraries

The Eagle Libraries were added to the directories in the previous steps (Fig. 66).

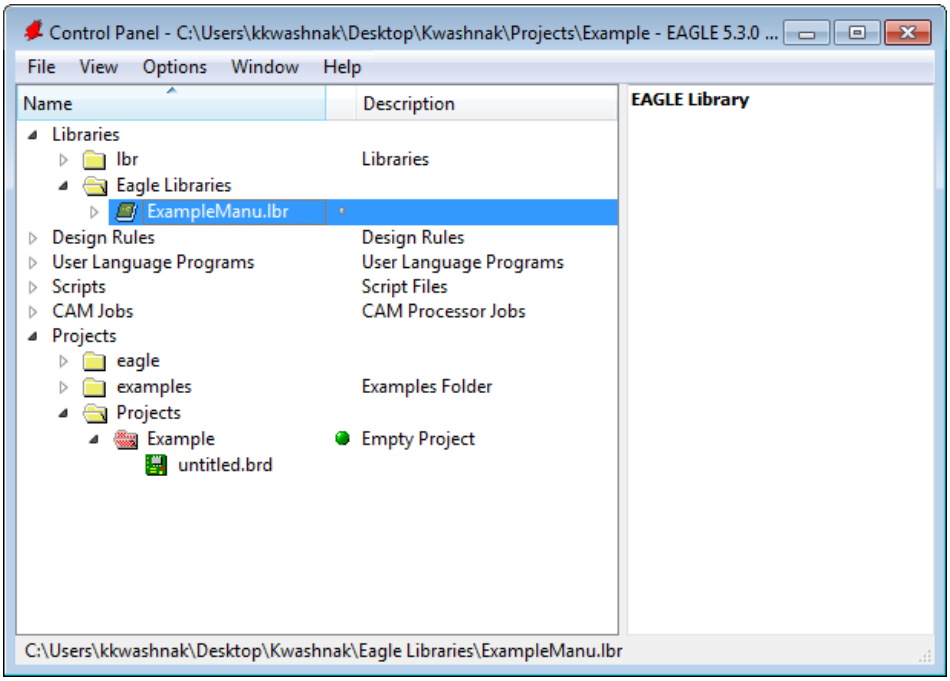


Fig. 66 Libraries file structure

The next steps will examine creating the Symbol (Sym), Package (Pac), and Device (Dev). A device is generated via a symbol and a package. Devices are incorporated into board and schematic designs.

3.2 Creating a Symbol

The Library Editor window will appear when creating or opening a Library as in Fig. 63.

Click on the <Edit> button on the left-hand tool bar (Fig. 67).

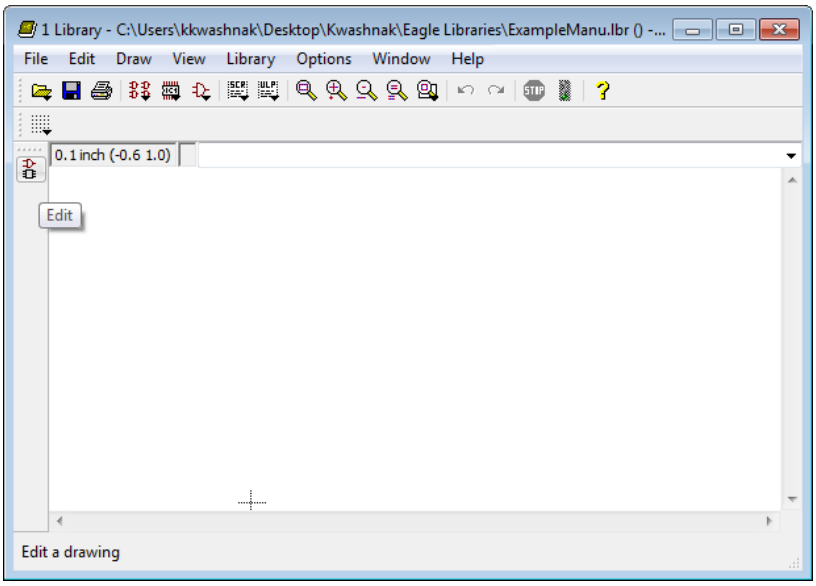


Fig. 67 Library edit button

Click on <Sym> button (Fig. 68) and type the component's name, such as "MICROTEST" (Fig. 69). This will appear on the schematic. When prompted to create a new symbol, click <YES>, and the Symbol Editor will open (Fig. 70).

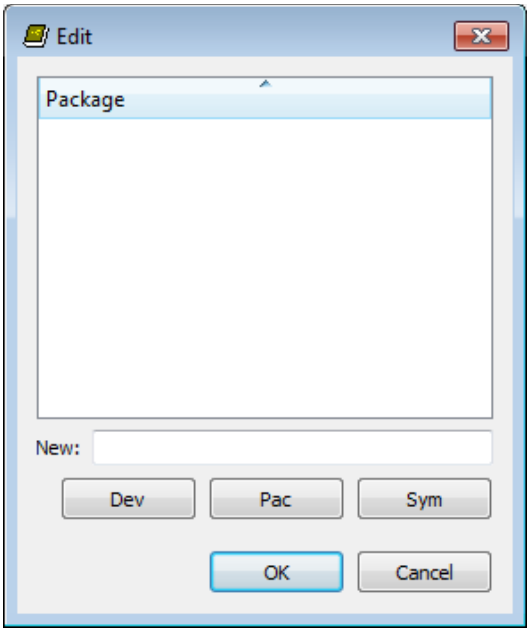


Fig. 68 Edit window

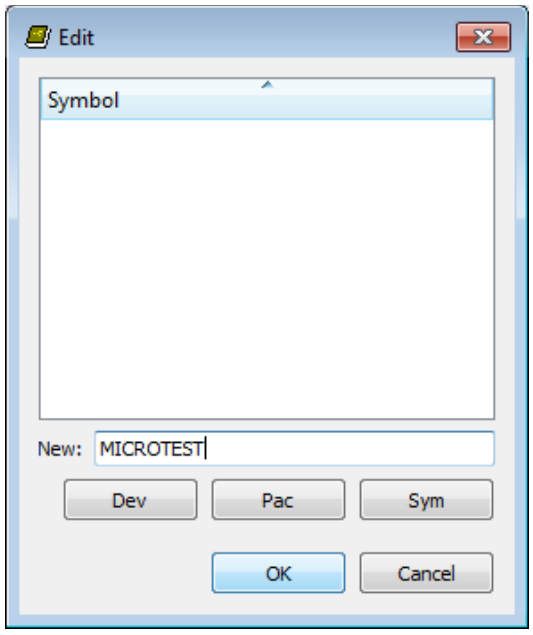


Fig. 69 Symbol edit window

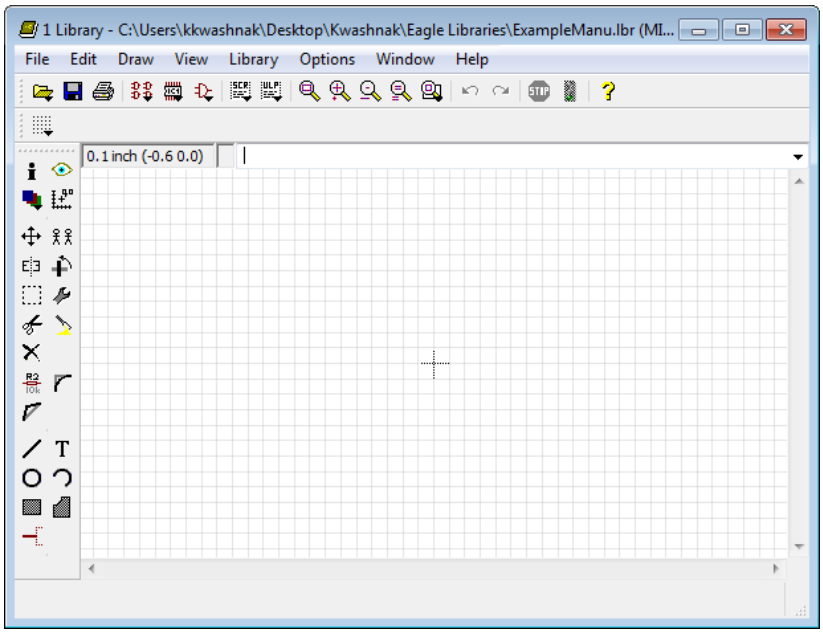


Fig. 70 Symbol editor

Once the Symbol Editor is opened, click the <Save> icon.

Next, navigate to <View> (Fig. 71) and click on <Grid>. When finished selecting settings, click <OK> (Fig. 72). For designing multiple symbols, which will be combined on a schematic, follow a similar spacing scheme. This will assist in keeping the schematic clear and legible.

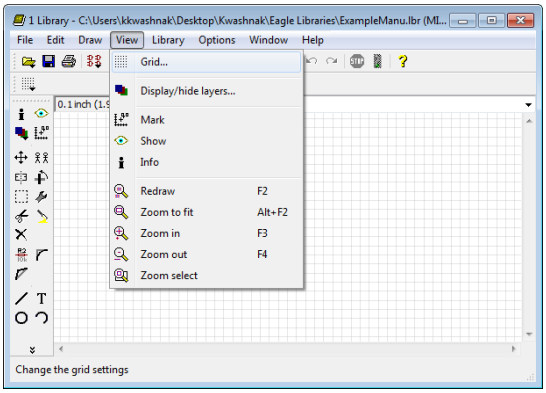


Fig. 71 View tab

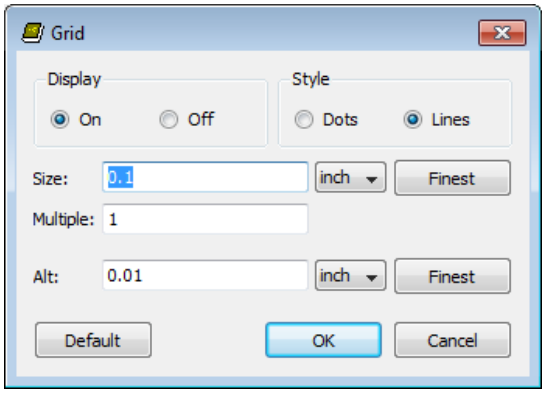


Fig. 72 Grid settings

Examine the component's datasheet and review the pin out specifications. A generic component is created for the following example.

Next, click on the <Line> tool, set the layer to <94 Symbols> and proceed to draw a rectangle in the design space (Fig. 73). While in mid-draw, right-clicking the mouse will cycle through different wire bending styles. Once completed, hit the [ESC] key on the keyboard. If the line is not placed in the correct location, use the <Move> or <Delete> tools. Exit the tools via [ESC].

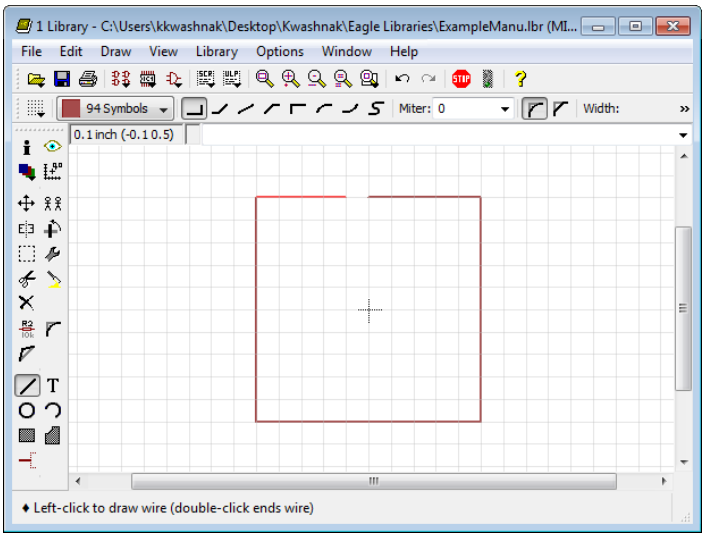


Fig. 73 Rectangle on 94 symbol layer

After the rectangle is completed, click the <Pin> tool (Fig. 74). Pins denote connections to the chip. Right-click the mouse to reorient the pin placement. Exit the tool via [ESC].

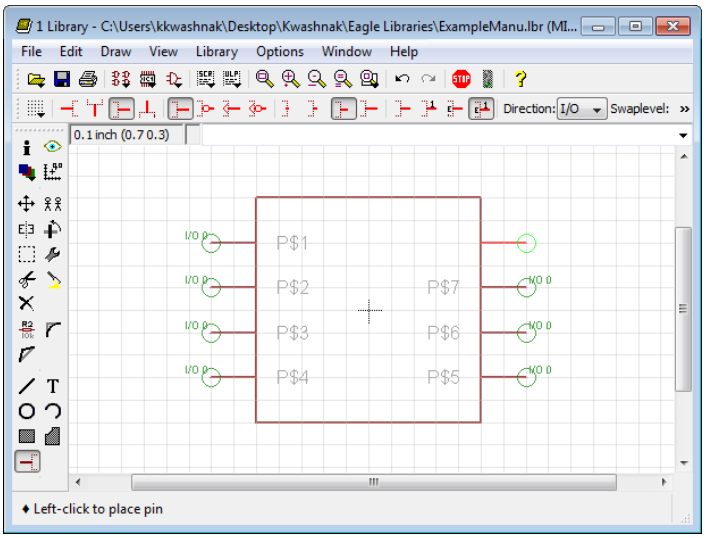


Fig. 74 Pin creation

To move multiple objects at once, highlight an area of objects using the <Group> tool (Fig. 75). Then, change to the <Move> tool (Fig. 76) and right click on the highlighted objects and select 'Move: Group'.

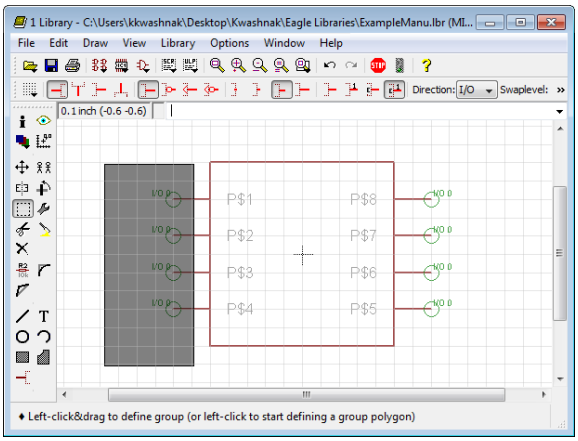


Fig. 75 Group select tool with highlight area

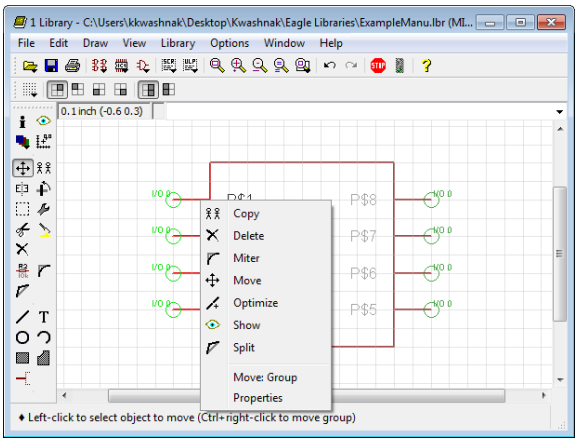


Fig. 76 Moving multiple objects

Click the <Info> tool and click on a pin. The <Info> tool enables changing of pin parameters (Fig. 77).

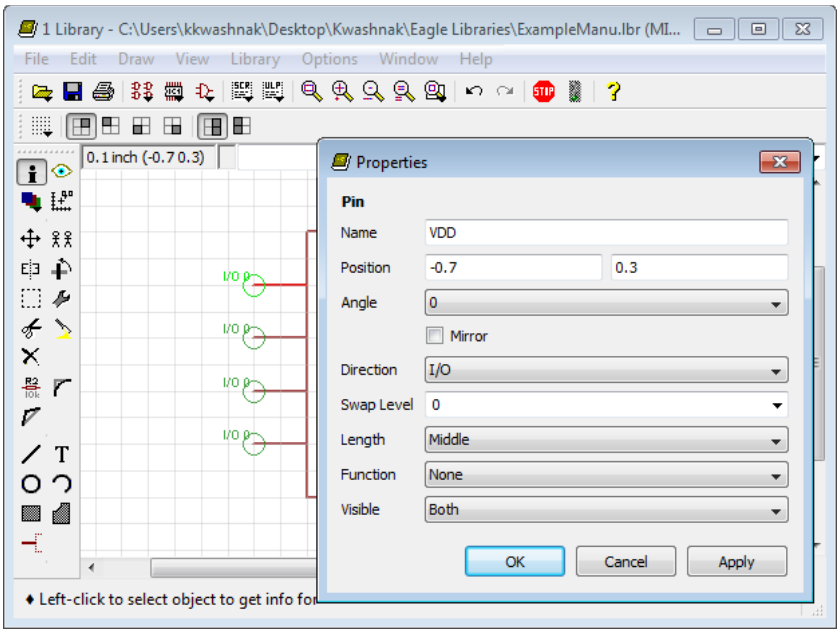


Fig. 77 Edit pin information

In the 'Properties' window, rename Pin 1, "P$1", to "VDD". 'Position' states its coordinates in the Symbol Editor. Angle denotes the orientation of the object. Mirror creates a reflected image of the component. Direction denotes the type of pin function, such as NC (not connected), In (Input Only), Out (Output Only), I/O (either Input or Output), OC (Open Collector/Drain), Pwr (Power [i.e., VDD, GND]), Pas (Passive [i.e., resistor or capacitor]), Hiz (High Impedance), or Sup (General Supply). Continue to configure all pins as listed in Table 8 and shown in (Fig. 78).

Table 8 Example component pin assignments

Pin	Assignment
1	VDD
2	CP5
3	CP4
4	MCLR/VPP/CP3
5	CP2
6	CP1/PCLK
7	CP0/PDAT
8	VSS

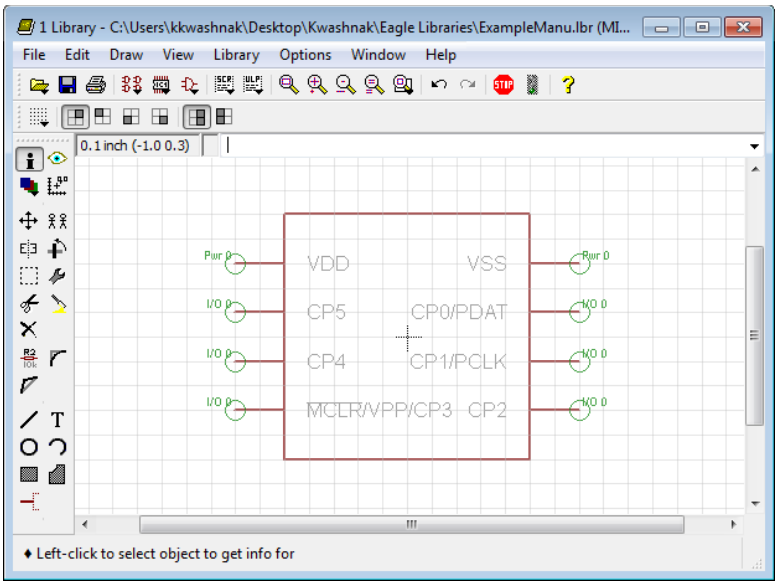


Fig. 78 Completed symbol

To create the bar over Pin 4, “MCLR” enter: “!MCLR!”.

Click the <Text> tool to add the following text below the symbol: “>Name” and “>Value”; set the text layer to ’95 Names’ and ’96 Values’, respectfully, using the <Info> tool (Fig.79). The “>” tells EAGLE to fetch the device’s metadata when the symbol is displayed in schematic view. Save the file once the symbol is complete.

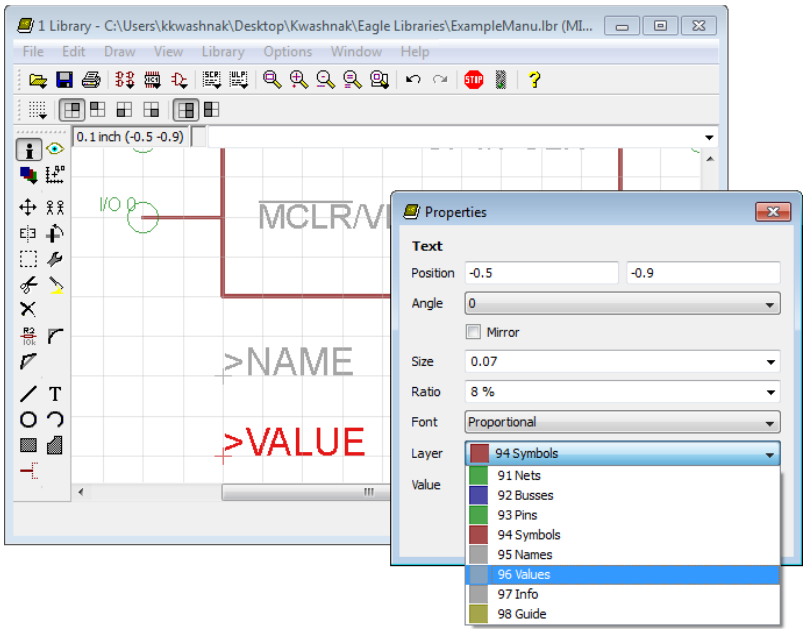


Fig. 79 Symbol annotations

Symbol element guidelines are listed in Table 9.

Table 9 Guidelines for symbol element properties

Parameter	Value
Grid settings: Adjust for ease of symbol design and may correlate to schematic grid settings	
Size	0.01
Multiple	1
Alt	0.005
Symbol, line: Adjust symbol outline for schematic aesthetics	
Width	0.01
Style	Continuous
Cap	Round
Layer	94 Symbols
Curve	0
Symbol, name: Text of ">NAME" is assigned to the '95 Names' layer near the symbol	
Size	0.07
Ratio	8%
Font	Proportional
Layer	95 Names
Symbol, value: Text of ">VALUE" is assigned to the '96 Values' layer near the symbol	
Size	0.07
Ratio	8%
Font	Proportional
Layer	96 Values

3.3 Package

Click on the <Package> icon (Fig. 80).

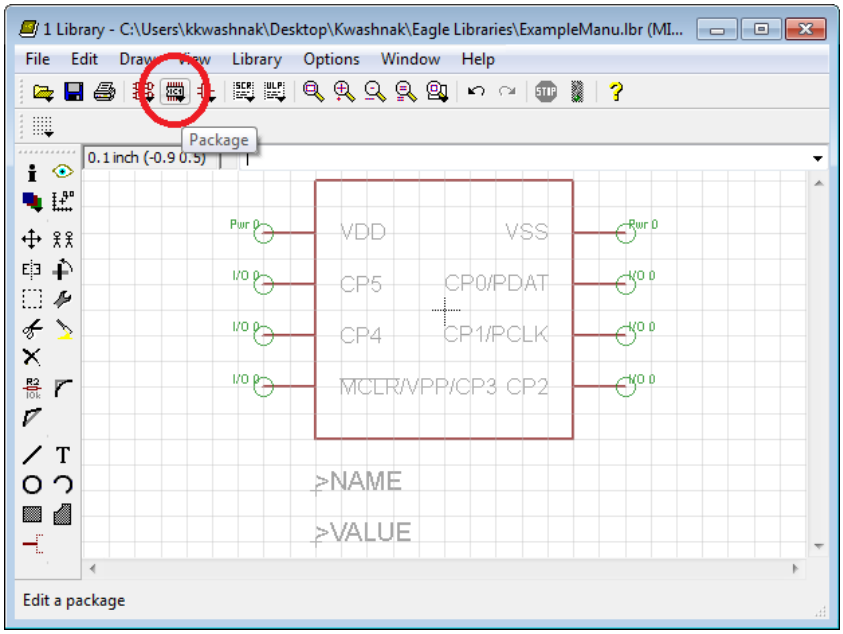


Fig. 80 Completed symbol

The <Package> icon will transfer the workspace to the overview screen of the library. Click on the <Pac> button, enter a Package name, for instance “DIP_8”, and click <OK> (Fig. 81). The Package name should denote the physical package of the component. When prompted to create a new package, select <Yes> and the Package Editor will appear (Fig. 82).

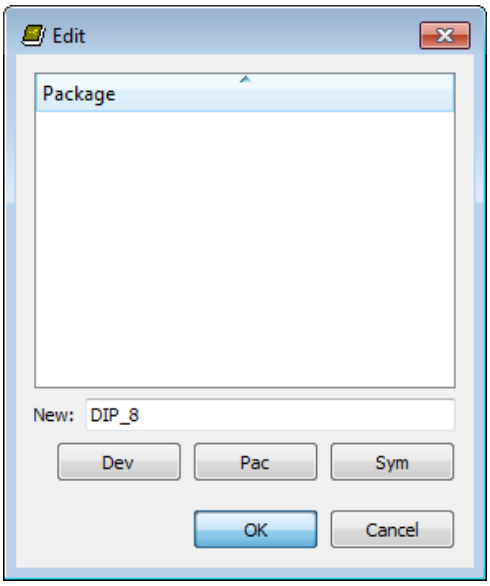


Fig. 81 Package creation

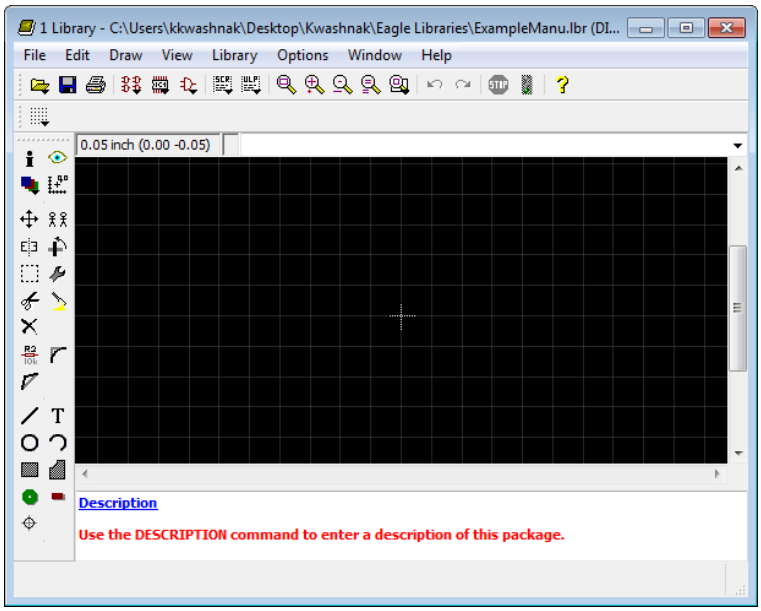


Fig. 82 Package editor

Navigate to <View>, <Grid>, and edit settings. The grid spacing should reflect the units and spacing as denoted by the component's datasheet (Fig. 83).

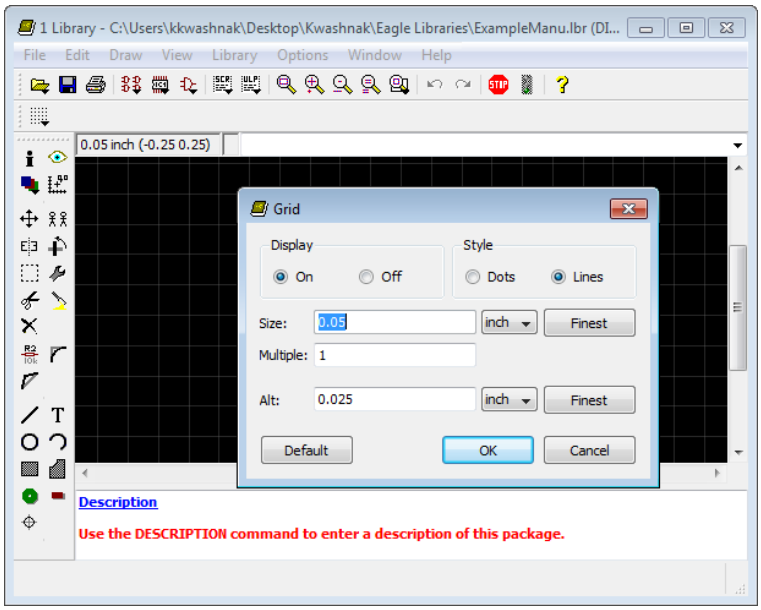


Fig. 83 Grid settings

Click on the <Rect> tool and draw a rectangle using two left clicks: one to start the rectangle and one to end (Fig. 84). Then, using the <Info> tool, edit the rectangle's properties. Ensure the layer is set to '51 tDocu'. This layer will be used to denote the components physical body. Observe the use of symmetry to simply dimensioning.

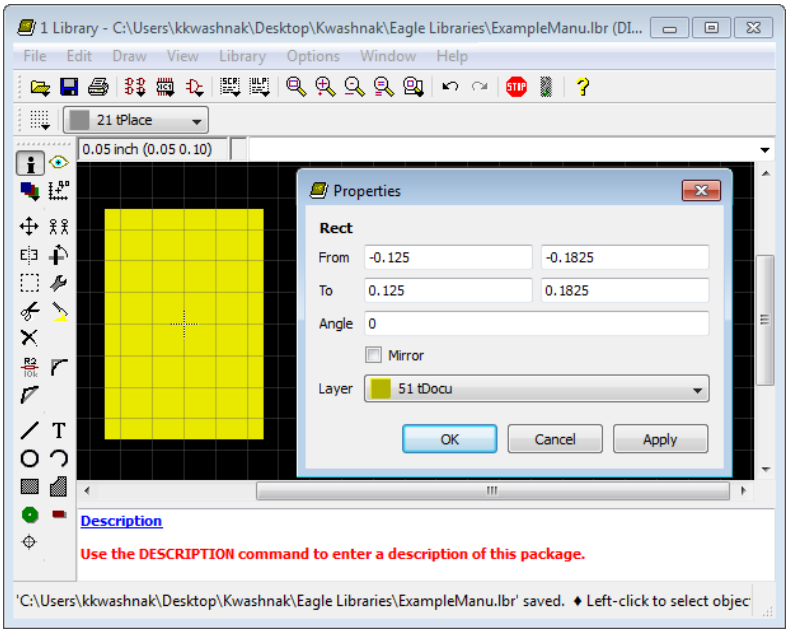


Fig. 84 Component physical outline

To add connection mounting points, use the surface mounting pads <Smd> or padded hole <Pad> tool. For this chip, use the <Pad> tool (Figs. 85 and 86). Use the <Info> tool to configure pad properties. For pin 1 of the device, the pad's properties, 'Shape', is set to 'Square' in order to specify the orientation of the device.

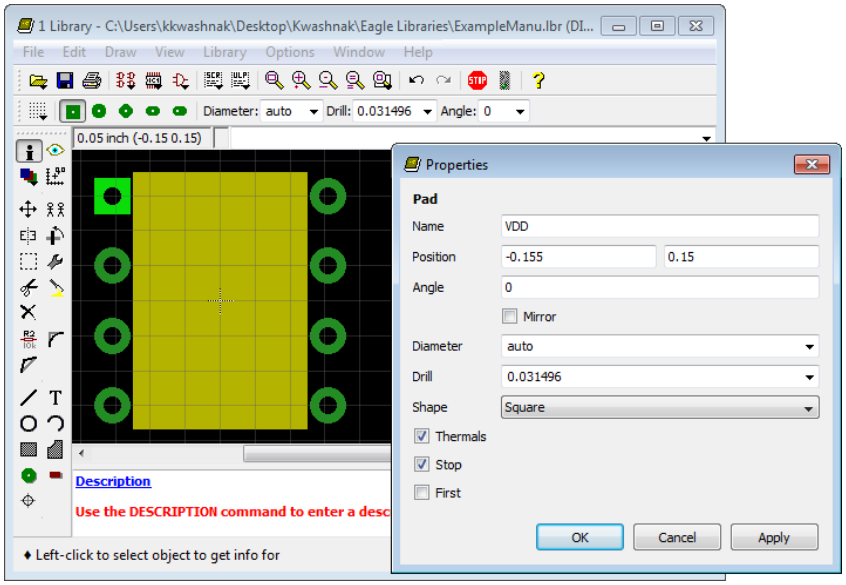


Fig. 85 Pin 1 padded hole placement

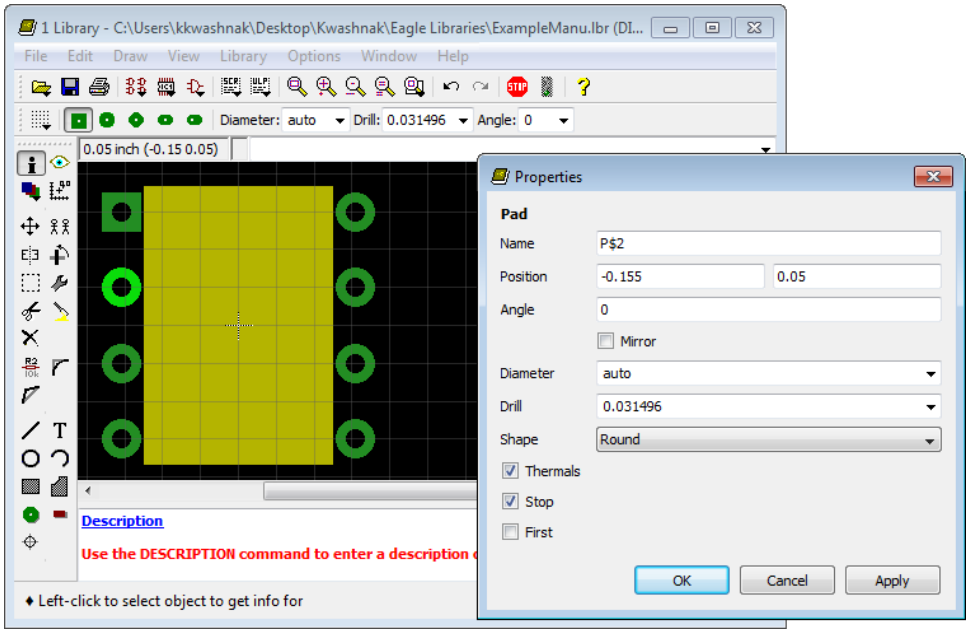


Fig. 86 Pin 2 padded hole placement

If a <smd> pad is used, ensure the layer is set to ‘1 TOP’ (Fig. 87). ‘1 TOP’ is a copper trace on the top side of the board (assuming the package is made for a two-layer board).

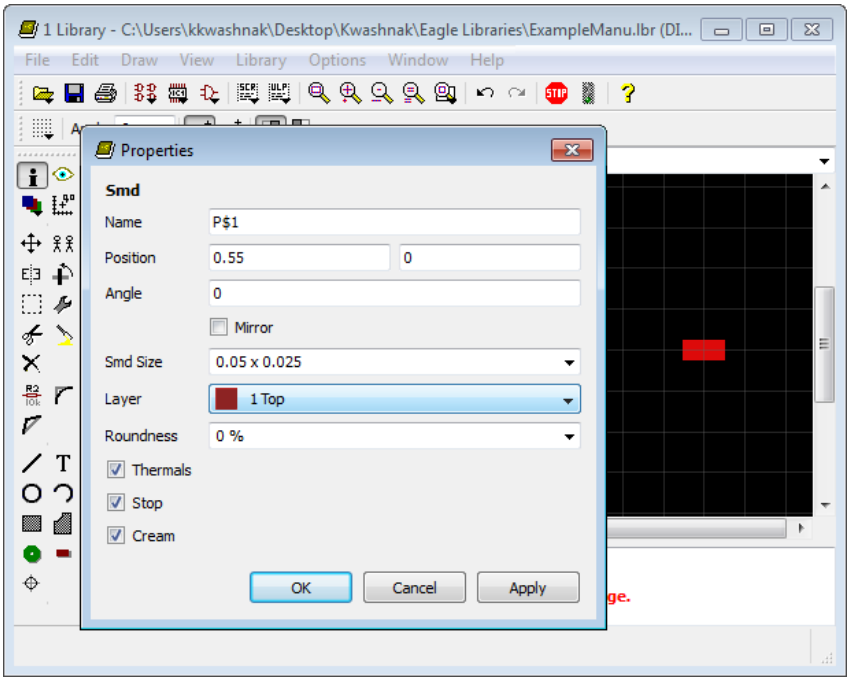


Fig. 87 SMD pad information

Next, add an outline to the chip, using the <Line> tool (Fig. 88). Inspect the line properties and ensure layer is set to ‘21 tplace’. Also, some package silkscreens use a dot near the first pin of the device to help indicate the orientation of the device.

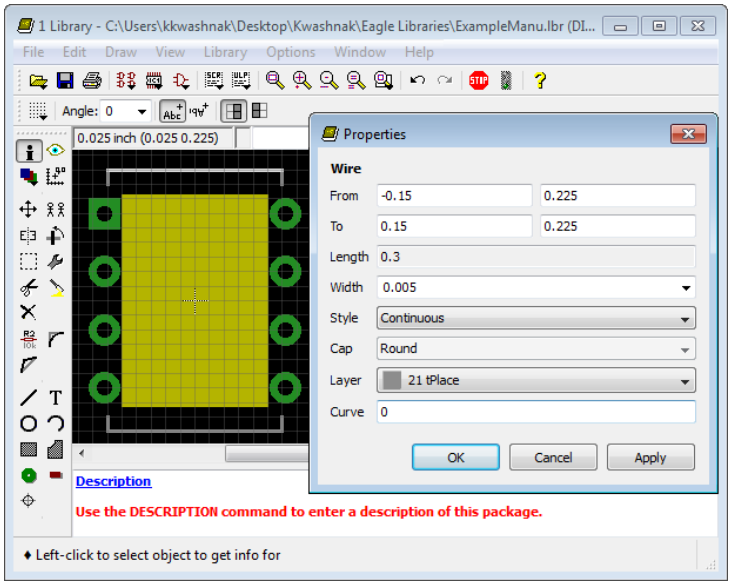


Fig. 88 Silkscreen outline

Likewise to the symbol, use the <Text> tool to add “>NAME” and “>VALUE” to the package, where “>NAME” and “>VALUE” resides on the ‘25 tNames’ and ‘27 tValues’ layers, respectively (Fig. 89). When completed, save the package. The silkscreen on the top layer of the board will portray elements from the ‘21 tPlace’ and ‘25 tNames’.

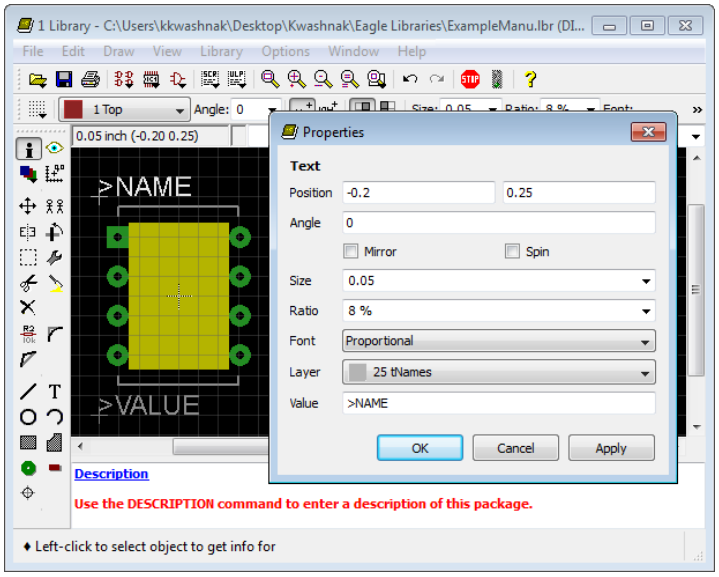


Fig. 89 Package annotations

Package element guidelines are listed in Table 10.

Table 10 Guidelines for package element properties

Parameter	Value
Grid settings: Adjust for ease of symbol design and may correlate to the component's datasheet	
Size	0.01
Multiple	1
Alt	0.005
Silkscreen, circle: Pin 1 identification marker	
Width	0.005
Layer	21 tPlace
Radius	0.009843
Silkscreen, line: Chip outline	
Width	0.012
Style	Continuous
Cap	Round
Layer	21 tPlace
Curve	0
Silkscreen, name: Text of ">NAME" is assigned to the '25 tNames' layer near the footprint	
Size	0.05
Ratio	8%
Font	Proportional
Layer	25 tNames
Silkscreen, value: Text of ">VALUE" is assigned to the '27 tValues' layer near the footprint	
Size	0.05
Ratio	8%
Font	Proportional
Layer	27 tValues

3.4 Device

After completing the package, navigate to and click on the <Device> icon (Fig. 90).

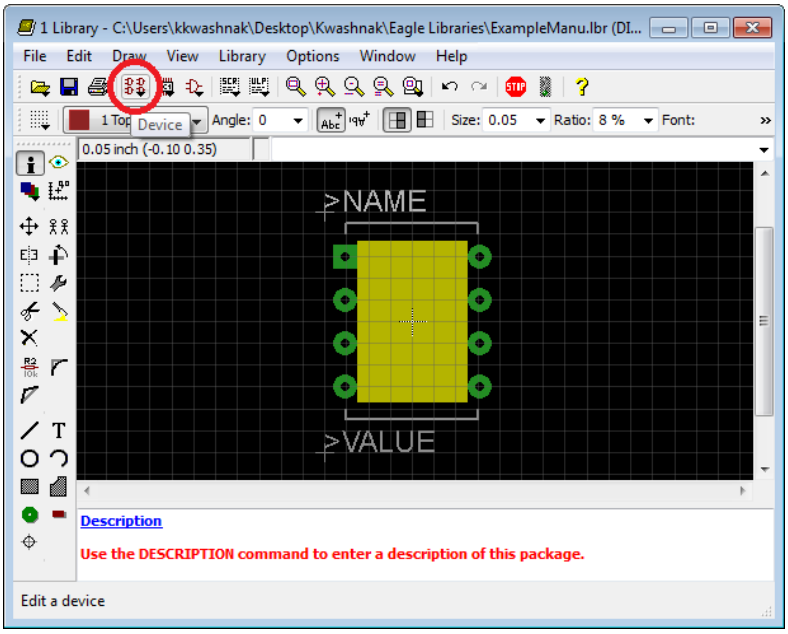


Fig. 90 <Device> icon

Create a new device with the chip's name and package type (Fig. 91), for example, "MICROTEST-DIP_8".

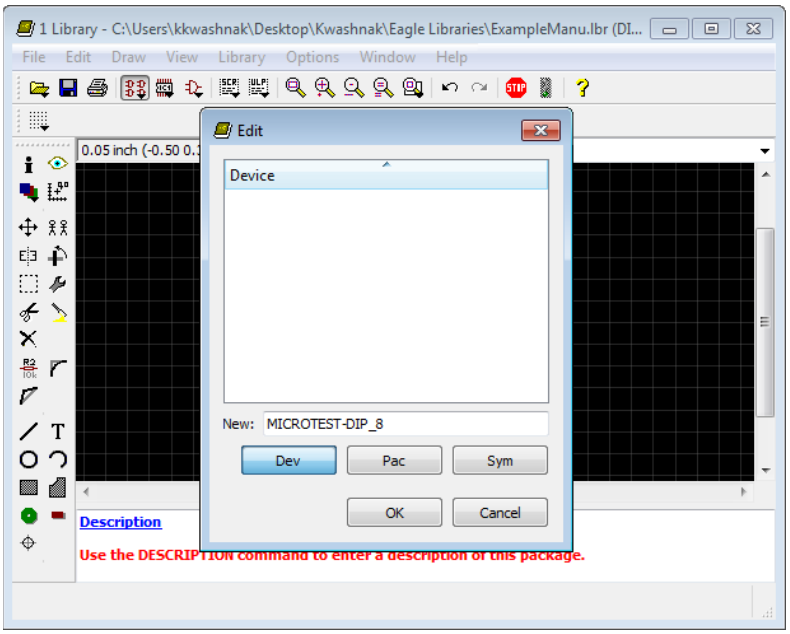


Fig. 91 Device creation

Inside the device configuration, navigate to and click on the <Add> tool (Fig. 92).

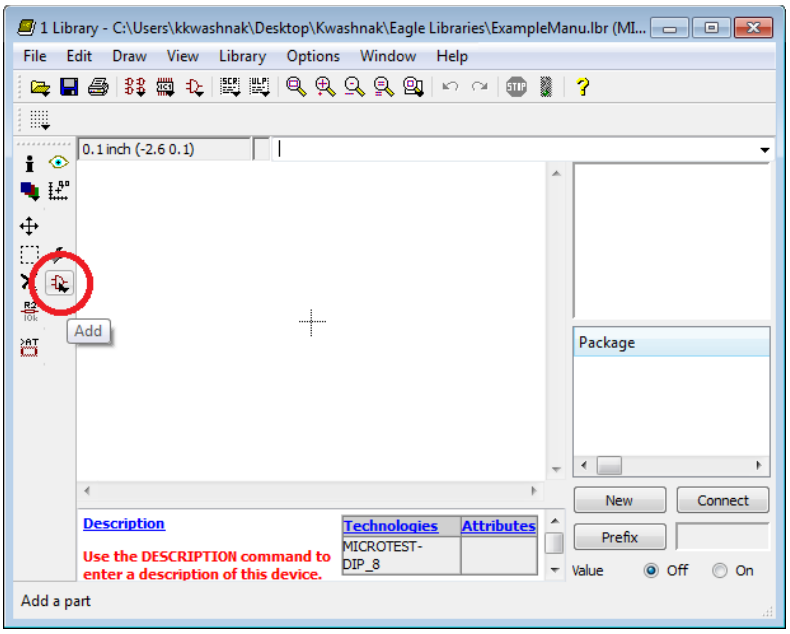


Fig. 92 Device configuration <Add> tool

Previously created symbols will appear in the selection window (Fig. 93). In this case, “MICROTEST” appears. Click on the symbol and click <OK>.

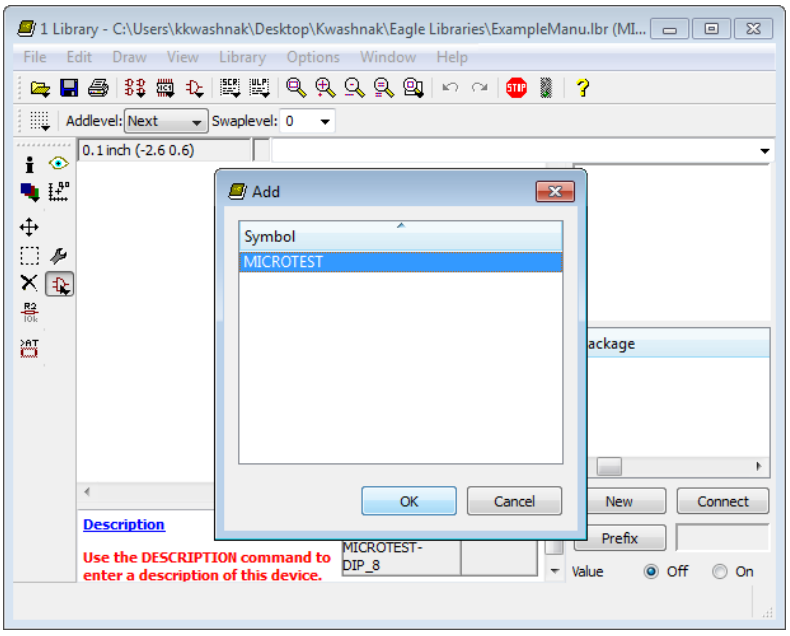


Fig. 93 Select created symbol

The MICROTEST symbol will float inside the workspace. Click to place and [ESC] to exit (Fig. 94).

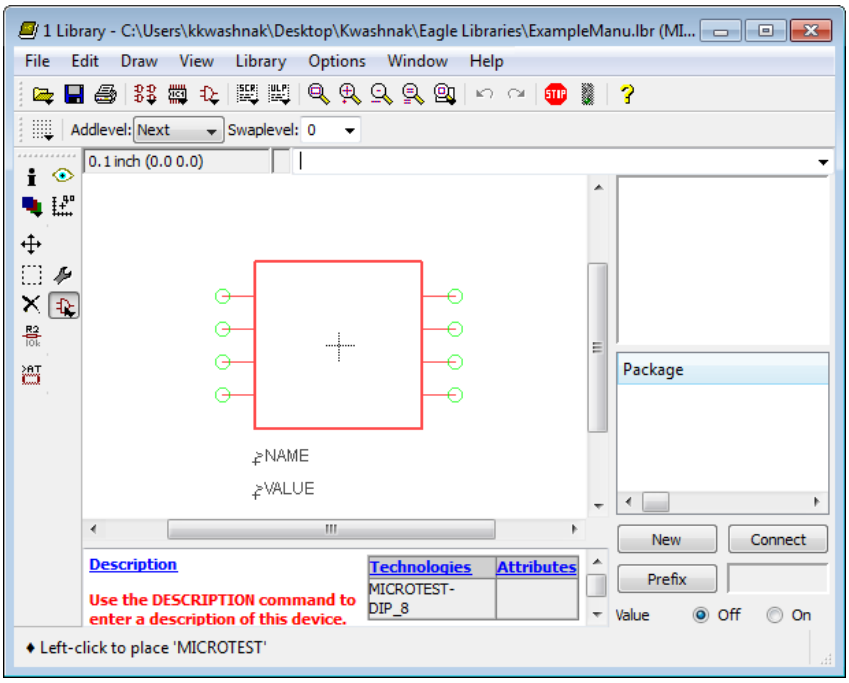


Fig. 94 Symbol placement

Navigate to and click on the <New> button (Fig. 95).

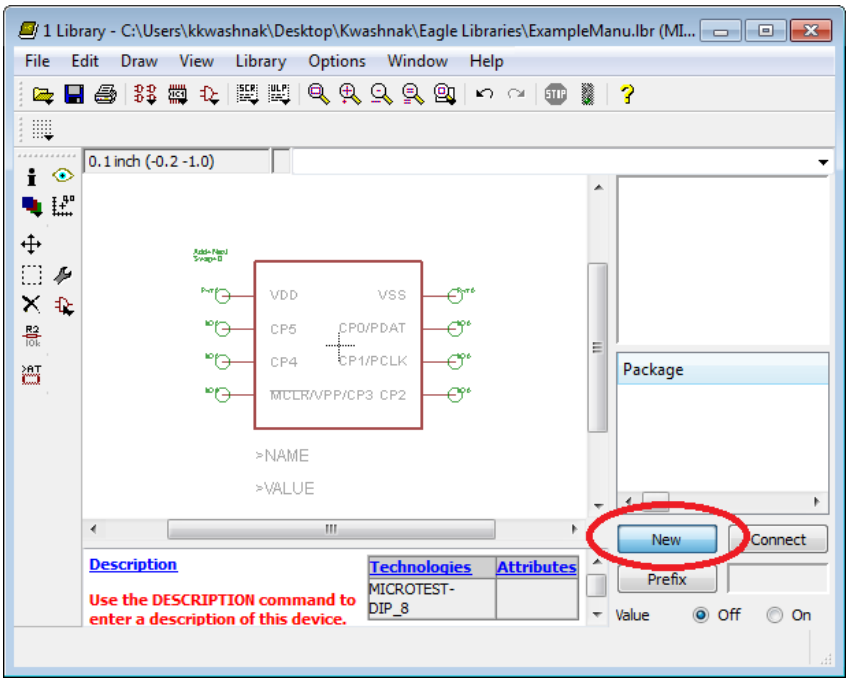


Fig. 95 Adding a package to the symbol

All packages that are designed in the library appear in the ‘Packages’ window (Fig. 96), in this case, “DIP_8”. Click on the package and click <OK>. The ‘Variant Name’ bar may be used if you wish to assign multiple packages to a symbol.

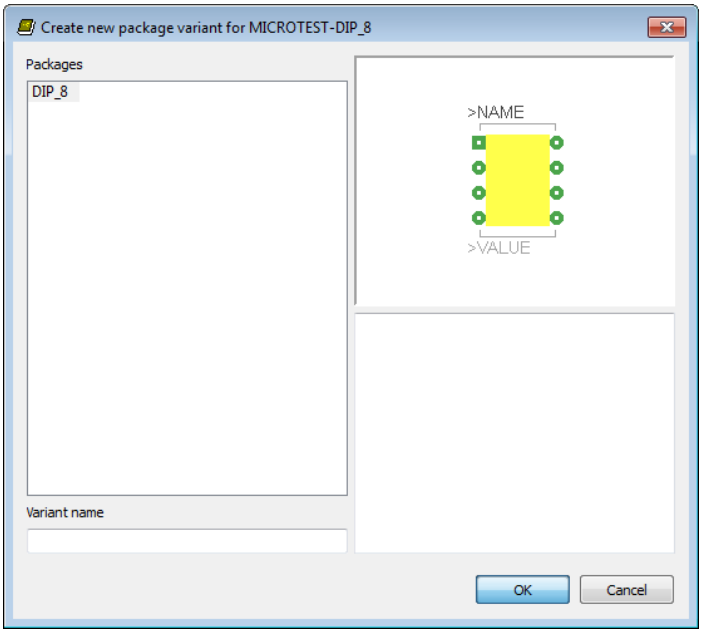


Fig. 96 Package assignment

Navigate and click on the <Connect> button (Fig. 97).

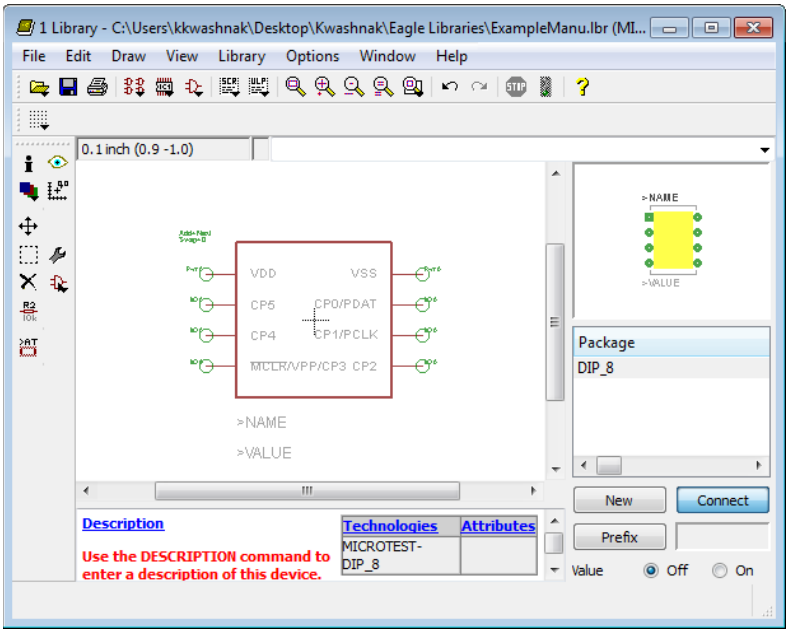


Fig. 97 Connecting pins

Match up connections from the ‘Pin’ and ‘Pad’ columns, one selection at a time. Once each Pin and Pad is selected, press the <Connect> button (Figs. 98–100). Configure all pins and pads. Afterward, click <OK>.

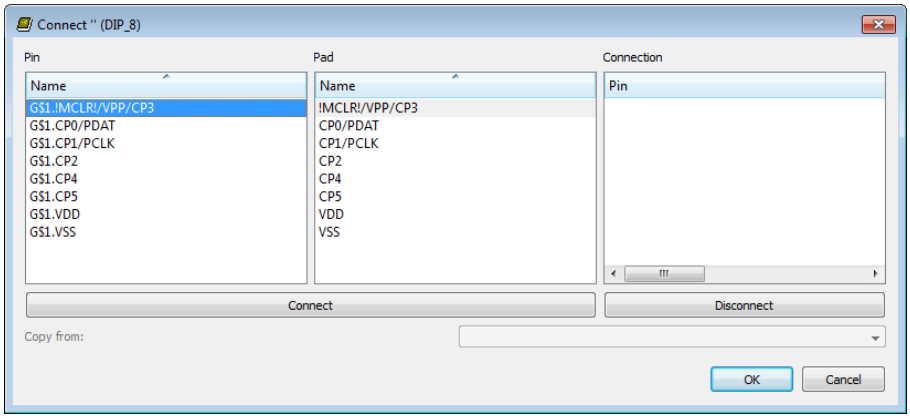


Fig. 98 Initial pin assignment

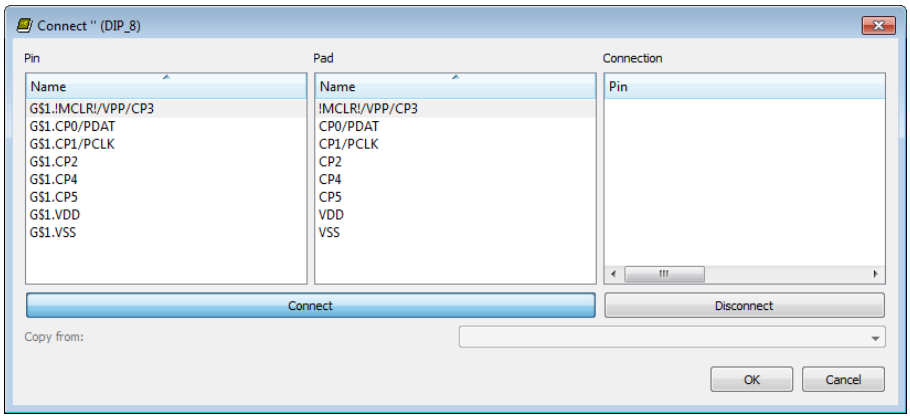


Fig. 99 Associate pin to pad

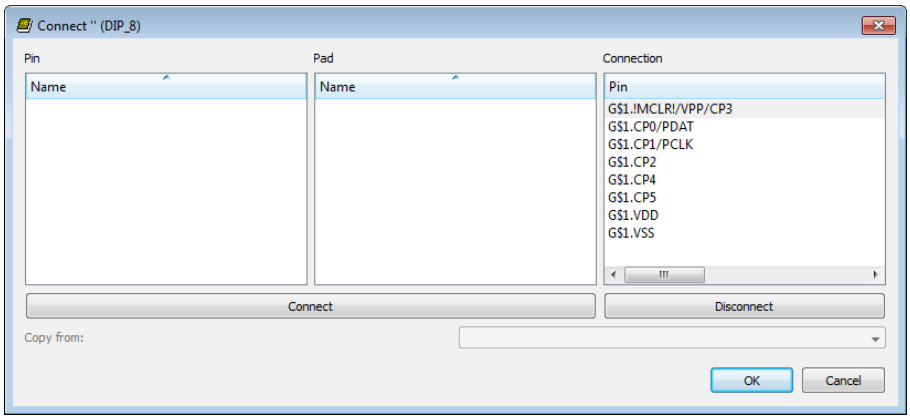


Fig. 100 Pin assignment complete

After the device is configured, click <SAVE> (Fig. 101).

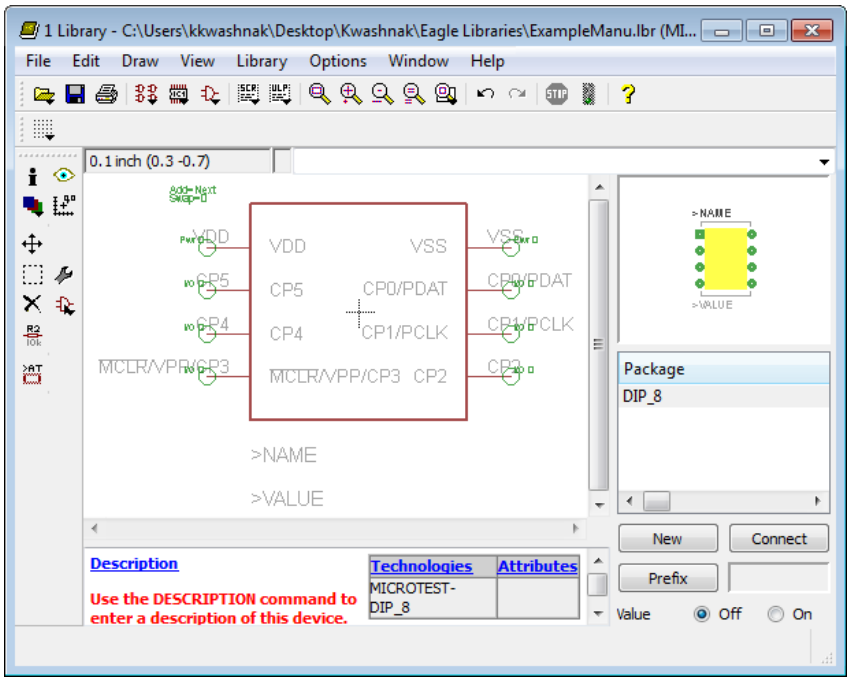


Fig. 101 Device creation complete

3.5 Activating the Library

Move to the EAGLE Control Panel and find the “ExampleManu.lbr” library under ‘Libraries’. Notice how there is a grayed out circle, signifying that the library file is not active (Fig. 102).

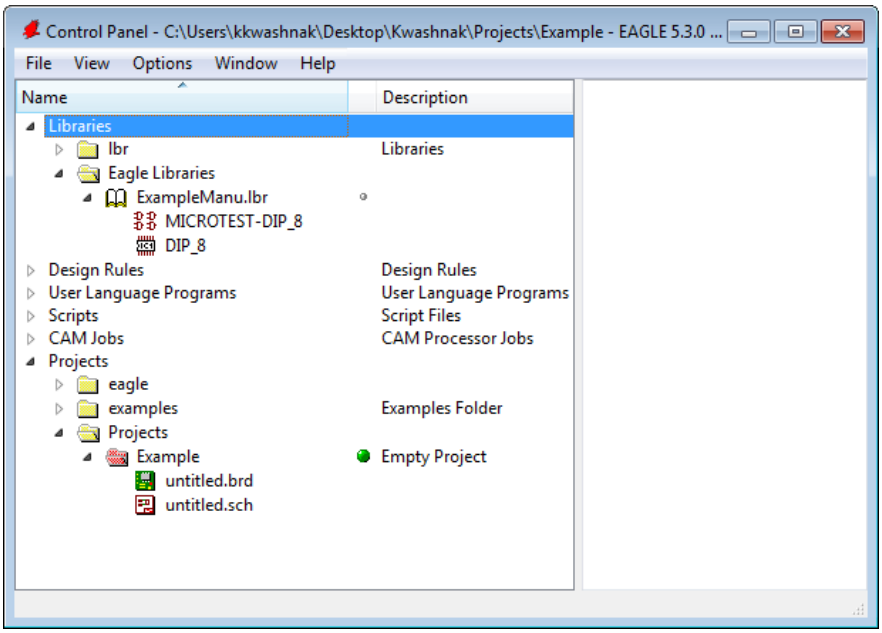


Fig. 102 New library and associated files

Click on the grayed out circle to enable the library (Fig. 103). The circle should turn green.

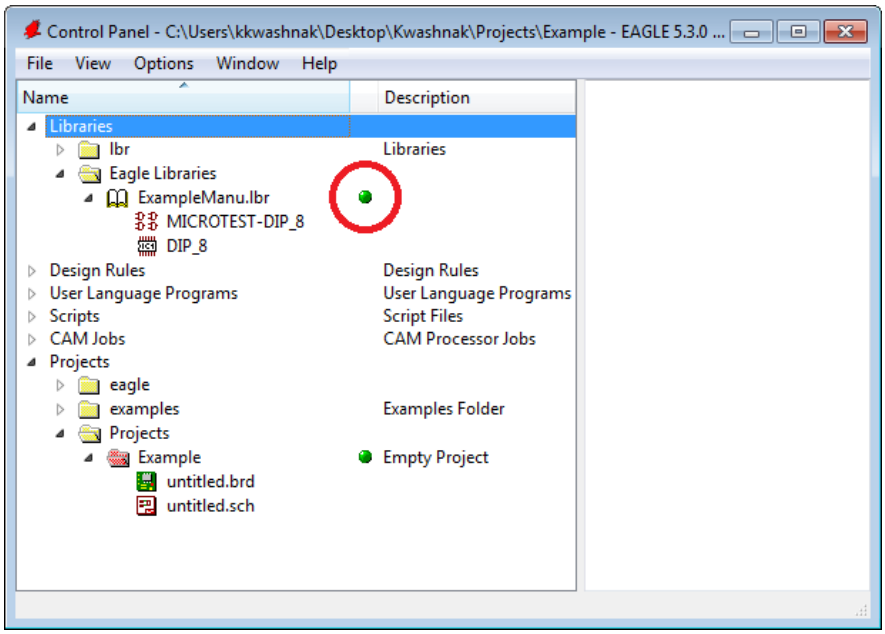


Fig. 103 Activate library

4. Two-Layer PCB Design: General Design Cycle

This section will use lessons learned from the previous sections to create the resources for the microcontroller board. Figure 104 depicts the general methodology for designing and manufacturing a two-layer PCB in EAGLE.

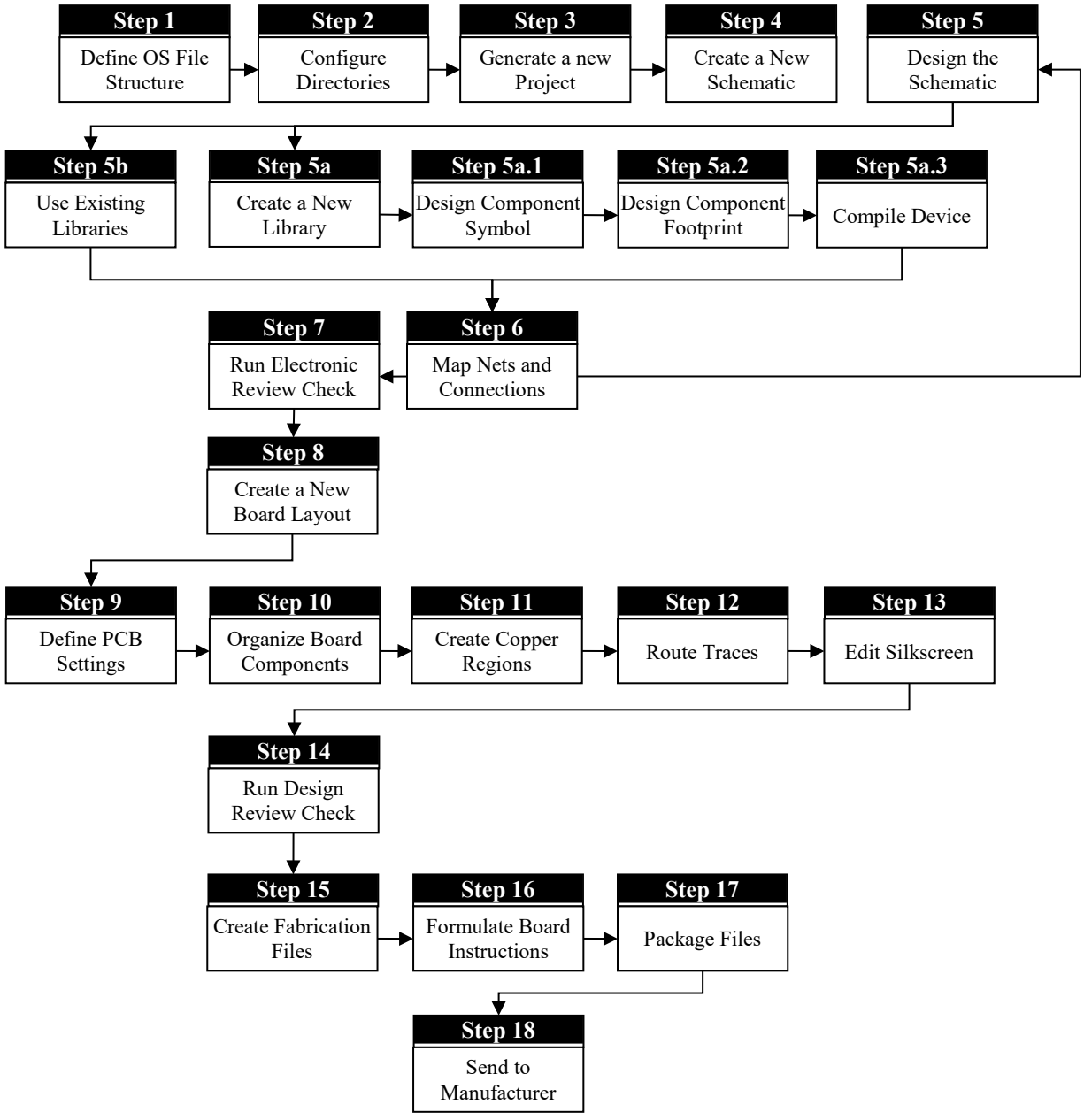


Fig. 104 PCB design cycle

4.1 Step 1: Define OS File Structure

In Windows File Explorer, create a similar file structure as shown in Fig. 105.

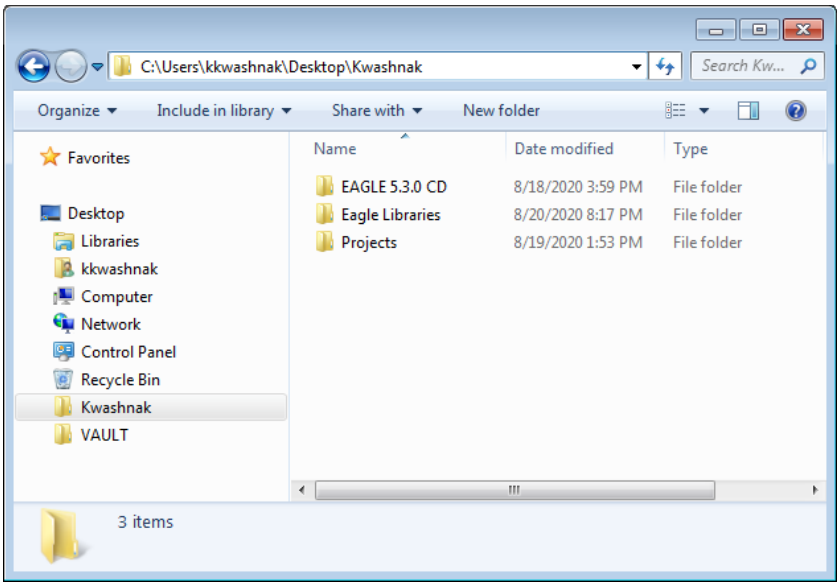


Fig. 105 EAGLE control panel tree

C:\Users\kkwashnak\Desktop\Kwashnak

C:\Users\kkwashnak\Desktop\Kwashnak\Eagle Libraries

C:\Users\kkwashnak\Desktop\Kwashnak\Projects

4.2 Step 2: Configure Directories

In the EAGLE Control Panel, open <Options>, <Directories...>, and add the links to the OS file locations for both the Library and Project folders (Figs. 106 and 107).

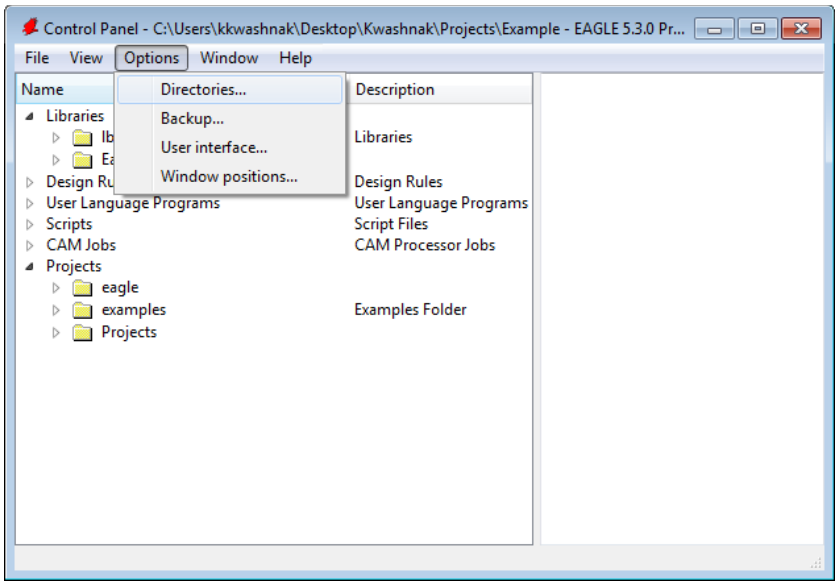


Fig. 106 EAGLE control panel directories

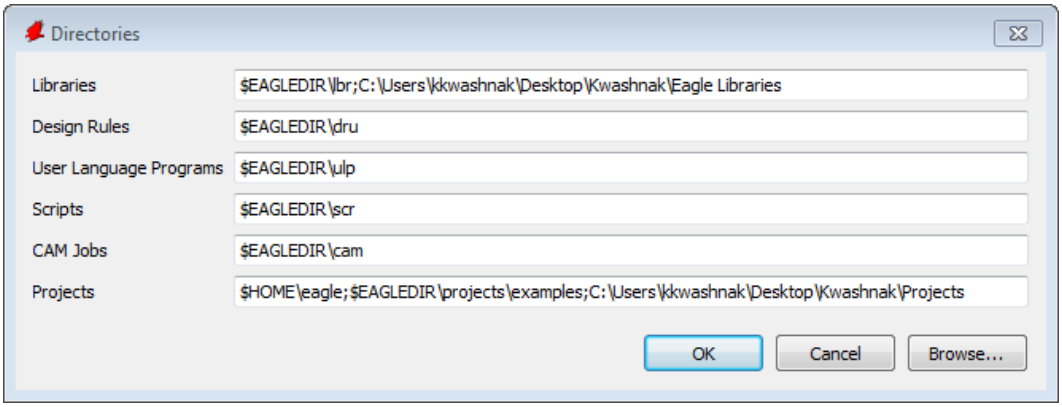


Fig. 107 Directory locations

Libraries: *$EAGLEDIR\lbr;C:\Users\kkwashnak\Desktop\Kwashnak\Eagle Libraries*

Projects: *$HOME\eagle;$EAGLEDIR\projects\examples;C:\Users\kkwashnak\Desktop\Kwashnak\Projects*

Note, the “Example” Project folder appears from the previous section (Fig. 108). In the tree, 'Libraries' should house custom and manufacturer libraries. Also, ‘Projects’ should encompass design files, such as schematics and board files. The ‘Design Rules’ folder contains edits to the board’s specifications, which will be edited via the DRC in the Board Editor. Advanced users will use the other folders for custom scripts and manufacturing processes.

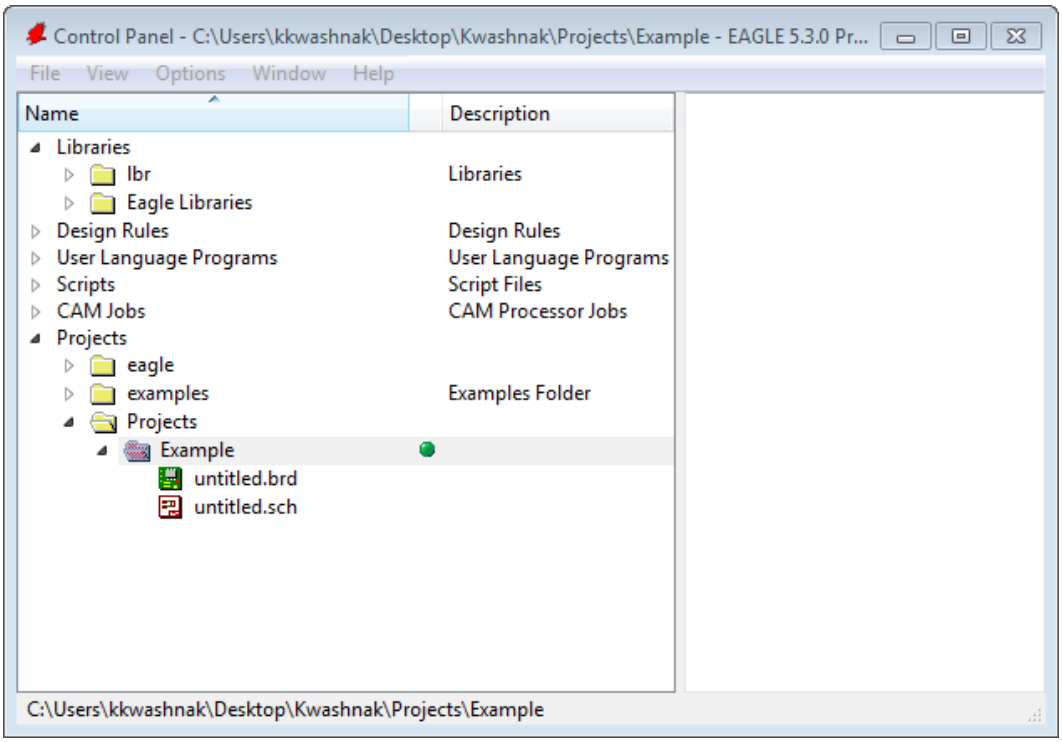


Fig. 108 Example EAGLE control panel file tree

4.3 Step 3: Generate a New Project

Create a new project in the 'Projects', "Projects" folder, rename file as "pcb_2layer" (Fig. 109).

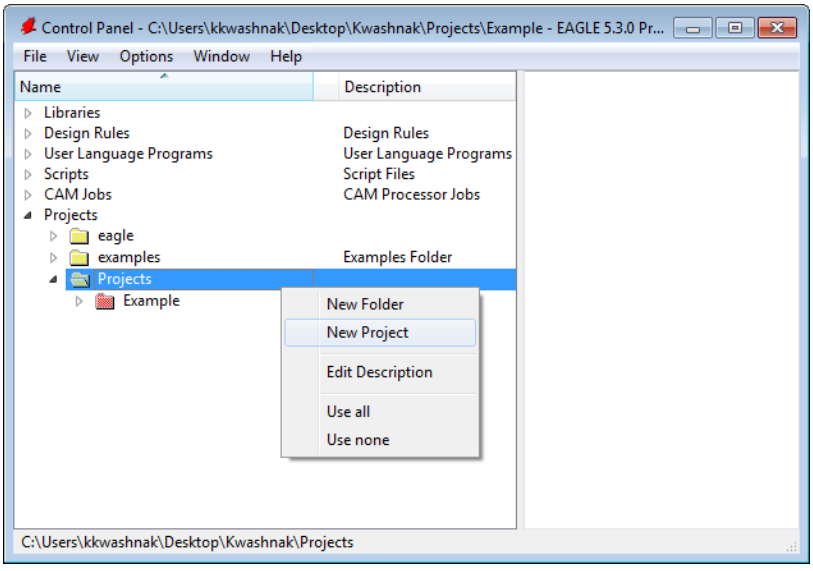


Fig. 109 pcb_2layer project creation

After creating the file, the “pcb_2layer” project should become the active file (Fig. 110). If not, click on the circle next to the project name. Green means the file is active, gray means the file is not in use.

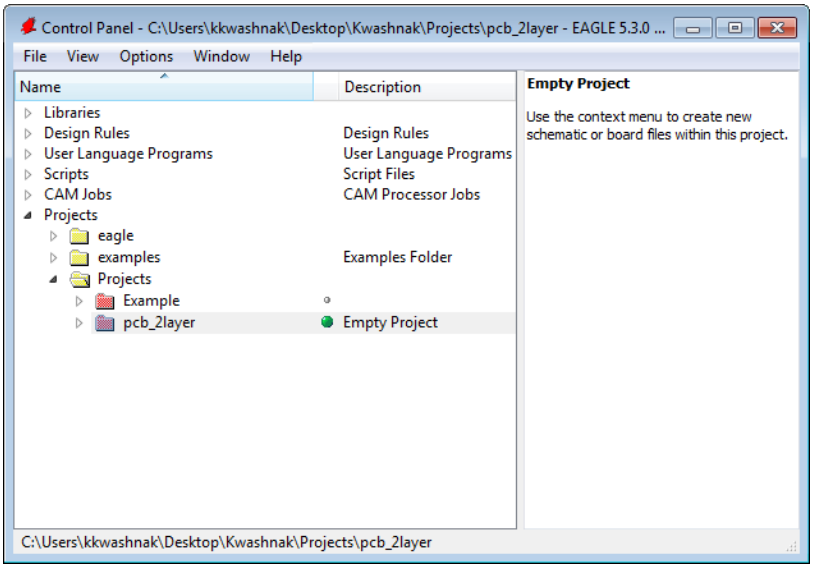


Fig. 110 Active project

4.4 Step 4: Create a New Schematic

Add a schematic to the project folder, as shown in (Fig. 111).

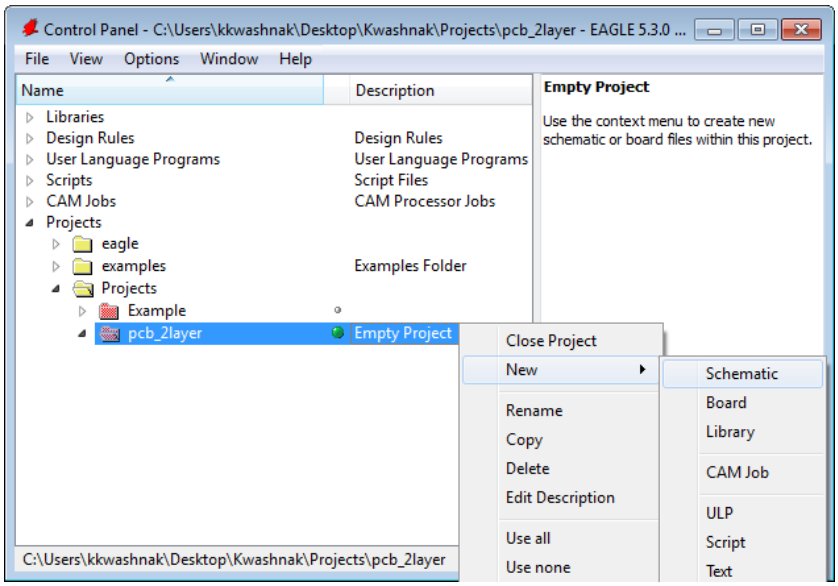


Fig. 111 Creating a new schematic

After creating a new schematic, the Schematic Editor will open. Save the file in the designated project folder location. In the EAGLE Control Panel, the schematic will appear in the tree (Fig. 112).

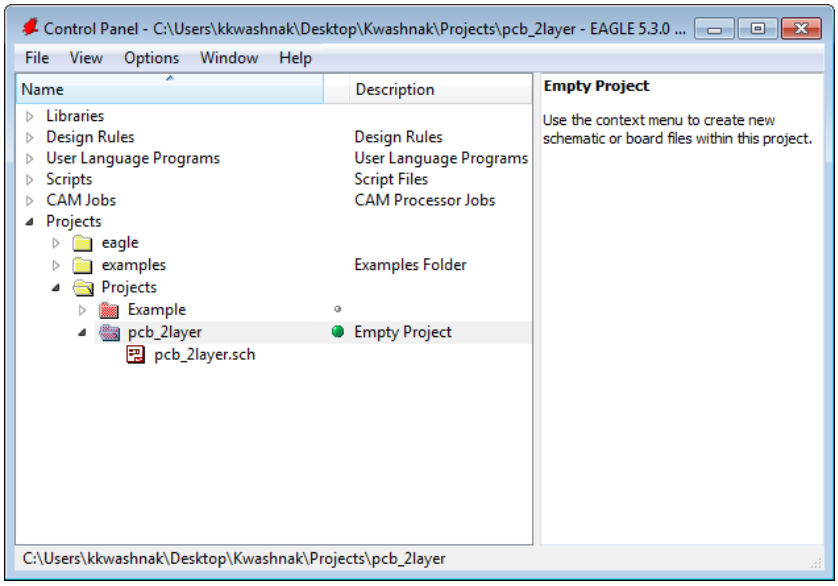


Fig. 112 Schematic file in tree

Save Schematic to folder:

C:\Users\kkwashnak\Desktop\Kwashnak\Projects\pcb_2layer

4.5 Step 5: Design the Schematic

In the EAGLE Control Panel, examine the 'Libraries' tree, 'lbr' folder (Fig. 113).

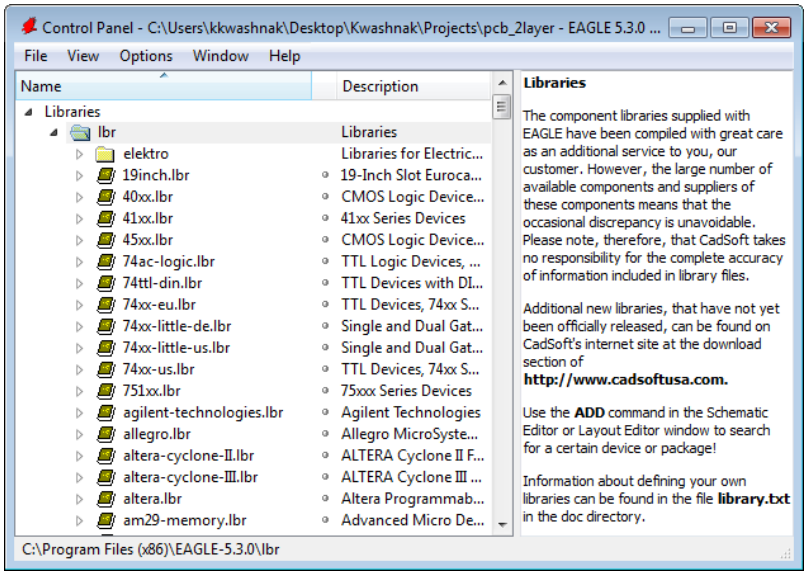


Fig. 113 Inactive default libraries

Right click on the ‘Libraries’ tree main folder and select <Use All> (Fig. 114).

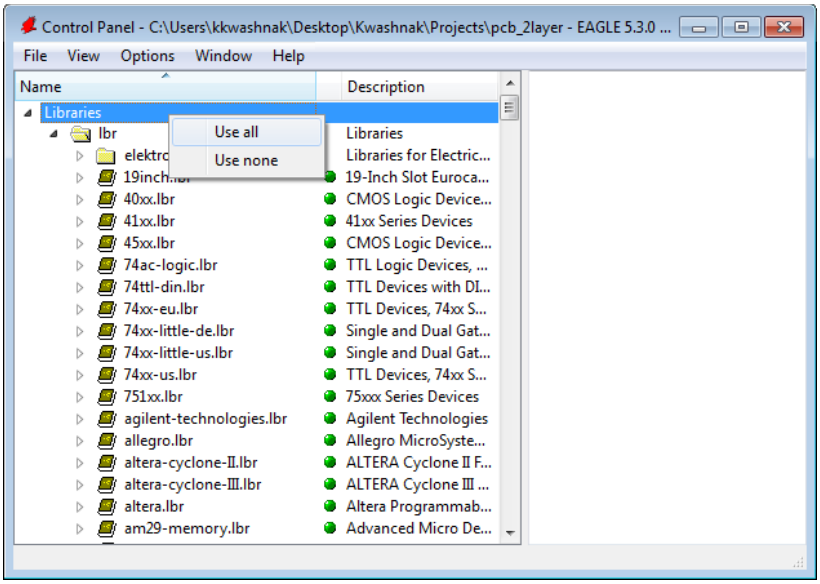


Fig. 114 Activating all libraries

Back in the Schematic Editor, navigate to and click on the <Add> tool from the left-hand toolbar (Fig. 115). In the ‘Search’ bar, type “Frame” and hit [Enter]. Double click or select <OK> on the desired frame size, in this case, ‘FRAME_A_L FRAME A SIZE, 8 1/2 × 11 INCH, Landscape’.

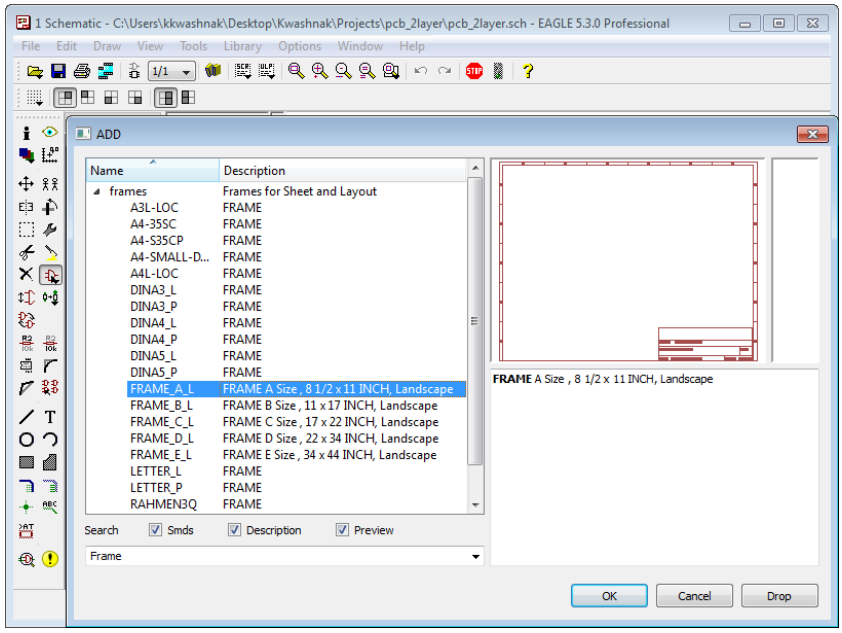


Fig. 115 Adding a frame to schematic

Place the object at the origin of the workspace (Fig. 116). Left click once to place the frame and then hit [Esc], to exit placing additional frame objects.

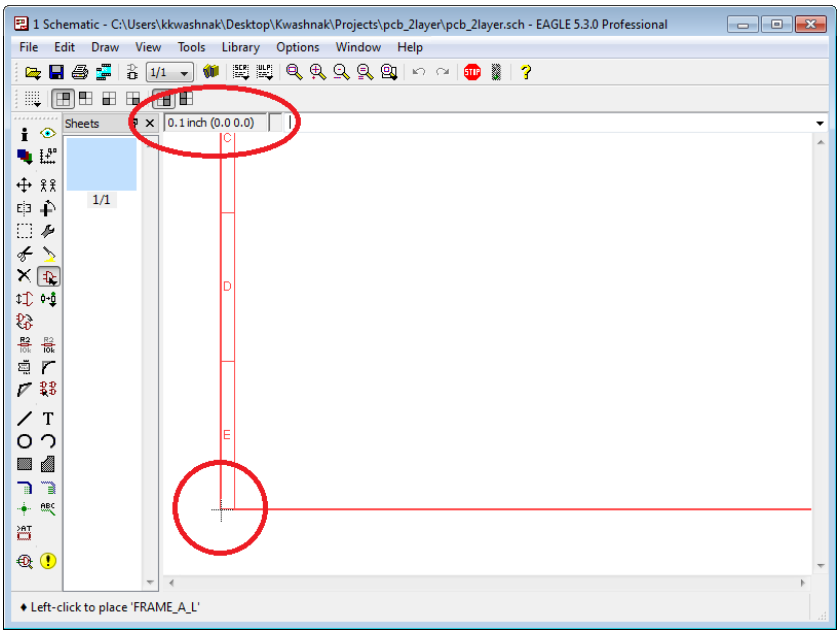


Fig. 116 Frame placement

Just as the frame is placed, the microcontroller previously created in this tutorial will be placed in the schematic. Using the <Add> tool and 'Search' bar, type "MICROT*". The " * " is a wildcard that allows indexing to multiple instances. Find "MICROTEST-DIP_8" and place into the schematic (Fig. 117).

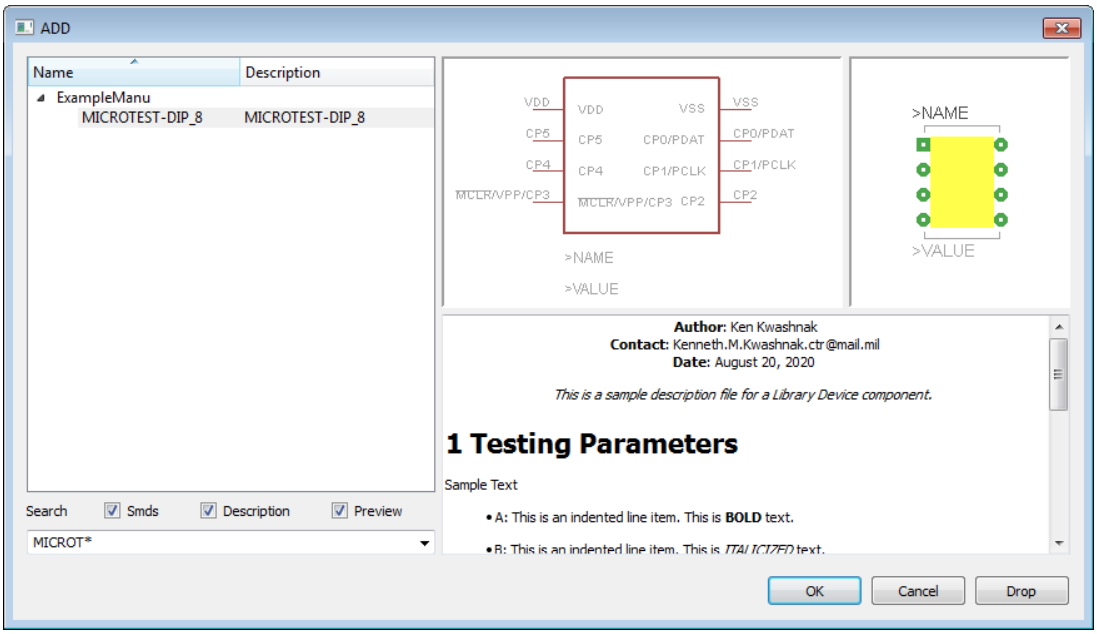


Fig. 117 Adding MICROTEST-DIP_8 to the schematic

Left click to place component, press [ESC], and click <Cancel> or press [ESC] again (Fig. 118).

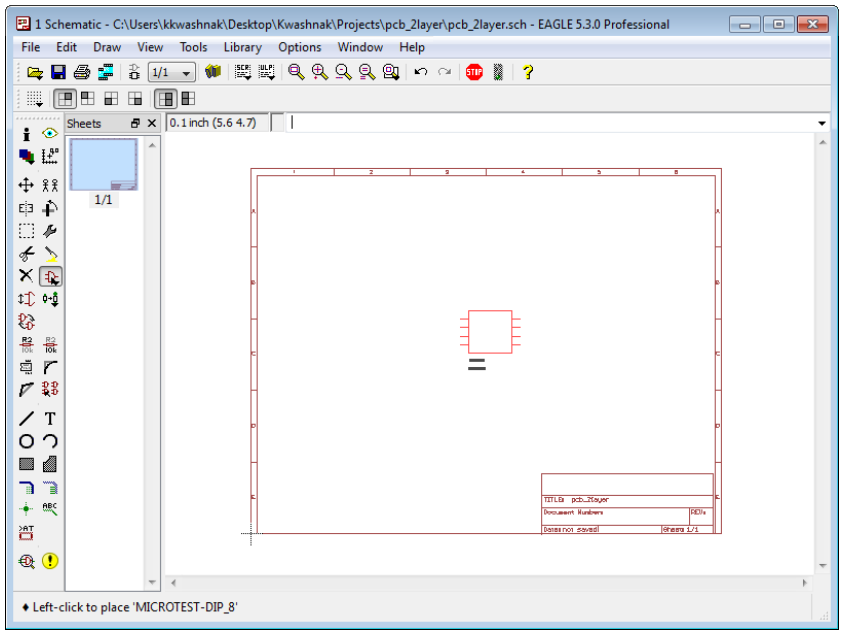


Fig. 118 Frame and component in schematic editor

Add components, as stated in Table 11, to the schematic using the <Add> tool; reference the Schematic Object for the object's name. Arbitrarily place the devices on the sheet. Use the <Move> tool to reorder and organize the devices. For the general schematic design, see Section 4.6.

Table 11 Schematic custom two-layer board objects

Line	Schematic object	Description	Manufacturer	PN	Q
1	MICROTEST-DIP 8[a]	Microcontroller, DIP8	Microchip	PIC12LF1501[16]	1
2	No device[b]	IC DIP socket 8POS	Adam Tech	ICS-308-T[17]	1
3	No device[b]	Battery, CR2450, 3V	Energizer	CR2450VP[18]	1
4	BS-2450[c]	Battery holder, coin PC pin	MPD	BS-2450[19]	1
5	MCP1702-5002E/TO[c]	Regulator linear 3V, TO92-3	Microchip	MCP1700-3002E/TO[20]	1
6	5988170107F_0805[a]	Green SMD LED	Dialight	5988170107F[21]	4
7	PTS647SK38SMTR2L	Tactile switch, NO	C&K	PTS 647 SK38 SMTR2 LFS[22]	1
8	R-US_R0805	Res, 0805, 120Ω, 5%, 1/8W	Vishay	CRCW0805120RJNEA[23]	4
9	C-USC0805	Cap, 0805, 0.1uF, 25V, X7R	KEMET	C0805C104M3RACTU[24]	1
10	22-23-2051	0.100” header, 5 pin, Prog	Molex	22-23-2051[25]	1
11	No device[b]	0.100”, conn housing, 5POS	Molex	0022012057[26]	1
12	22-23-2021	0.100” header, 2 pin, Batt	Molex	22-23-2021[27]	1
13	No device[b]	0.100”, conn housing, 2POS	Molex	0022012027[28]	1
14	No device[b]	Conn 22-30AWG crimp tin	Molex	0008650804[29]	7
15	SYM-MOUNT-HOLE[d]	0.125” plated mount hole	…	…	4
16	supply2, GND	Ground symbol, GND	…	…	5

[a] Custom device.
[b] No device created, only need to reference component for assembly.
[c] Extracted symbol from Ultra Librarian. Edited device footprint.
[d] Custom symbol.

Either a battery, CR2450VP, or external power supply provides power to a two pin header, 22-23-2021 (The board must only be powered by a battery or an external power supply; never simultaneously hook up both inputs). The header connects to a linear regulator, MCP1700-3002E/TO. A PIC12LF1501 microcontroller receives power from a linear regulator. Pin 1 of the microcontroller is tied to the linear regulator output and Pin 2 of the 5-pin programming header. Pins 2, 3, and 5 of the microcontroller are tied to a resistor-led network (LED and resistor). Pin 4 of the microcontroller is tied to a reset switch and pin 1 of the 5-pin programming header. Pins 6 and 7 of the microcontroller are tied to the 5-pin programming header for the clock and data signals, PCLK and PDAT, respectively. Pin 8 of the microcontroller is tied to ground. The board has four plated mounting holes to assist with assembly and for placement into an enclosure.

The components listed in Table 11 are chosen to build a demo two-layer microcontroller PCB. Unfortunately, the circuit is not optimized or tuned but will function as desired. Always read the manufacturer’s datasheets and compare specs of components to ensure compatibility and functionality, as well as applying safe and fundamental electrical engineering knowledge when designing a circuit.

It is always a good practice to make a detailed schematic, noting all voltages, connections, part numbers, signal profiles, and so on. But, for larger and more intricate projects, this method becomes too cumbersome and difficult. Documentation of expected circuit behavior is essential when testing and evaluating boards.

Using the <Text> tool, enter external connection information above the headers (Fig. 119). For example, the two-pin header 22-23-2021 connects the linear regulator to an external battery/power supply, while the five-pin header 22-23-2051 connects the microcontroller to a programming device. For each header, comment above the respective device: “Battery Connection” and “Programming Connection” (Fig. 120). Also, change the layer of the text to ‘97 – Info’.

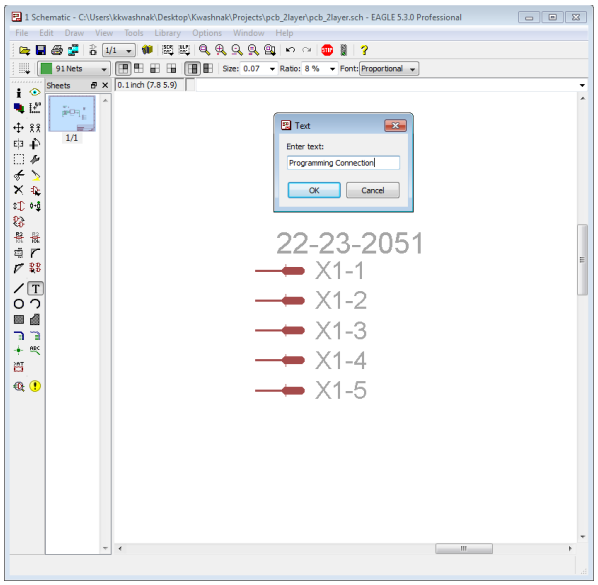


Fig. 119 <Text> tool

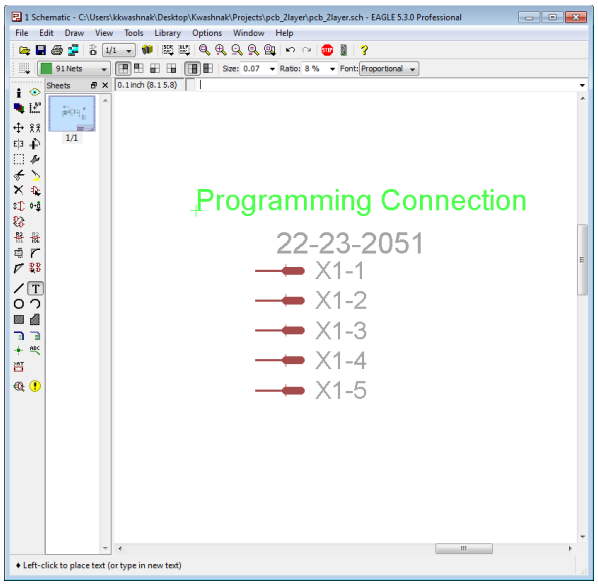


Fig. 120 Custom schematic text

4.5.1 Editing Imported Symbols

If a device is imported into the main library and added to the design, the symbol, footprint, or the device may need to be adjusted to fit the design scheme. For example, examine Figs. 121 and 122.

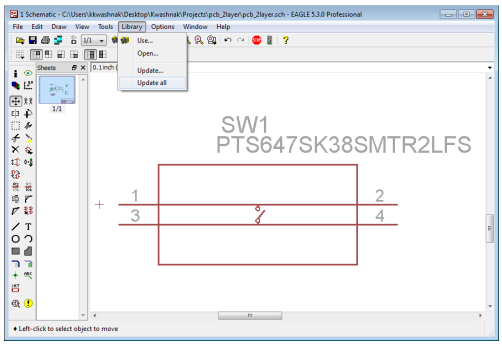


Fig. 121 Raw imported symbol

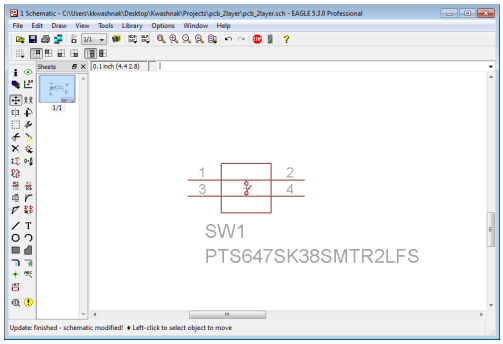


Fig. 122 Edited symbol

Figure 121 illustrates the imported original symbol design and Fig. 122 is the updated symbol design that fits the schematic's current scheme. Each device may have numerous symbol variations in order to accommodate documentation requirements. If the symbol is added to the schematic and edited later, the symbol must be manually updated via <Library>, <Update...> or <Update All...>.

Symbols may represent the actual component layout, but others may be optimized for functionality. For example, on an integrated circuit (IC), there may be many ground (GND) lines. The symbol may have those GND lines grouped together to keep the schematic's routing clear and concise.

If a symbol is placed on the schematic, but the “>NAME” and/or “>VALUE” obstructs other objects, use the <Smash> tool and click on the obstructing object's center (Fig. 123). Then, use the <Move> tool to arrange selected text (Fig. 124). Always check the device, package, and symbol definitions with the datasheet when importing a library!

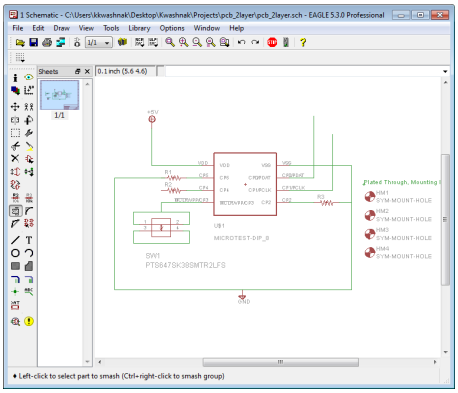


Fig. 123 <Smash> tool on object

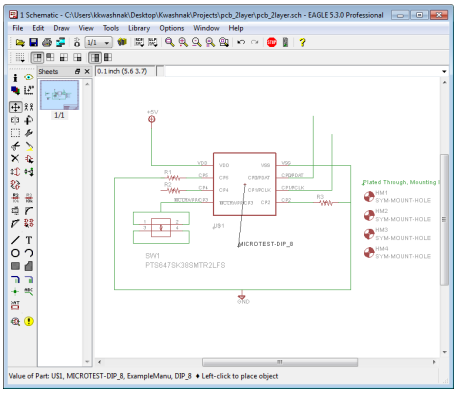


Fig. 124 Moving smashed text

4.5.2 Creating Grounded Mounting Hole Symbols

One method to create a grounded mounting hole is to simply use a via and adjust the annulus (the ring of copper around the drill hole) and drill size on the board file. A different method would involve creating a highly detailed device. For this small project, the former is used due to its relative simplicity and ease of use.

It is essential to place all elements of the design on the schematic, even if there is no fully defined device (a device that has a paired package and symbol) placed on the board. Therefore, in addition to creating a custom via on the board, a symbol is placed on the schematic.

Create a new library, “holes_mount” and place in the “Eagle Libraries” folder.

C:\Users\kkwashnak\Desktop\Kwashnak\Eagle Libraries\holes_mount.lbr

Create a new symbol, “MOUNT-HOLE”, in the library (Figs. 125–129).

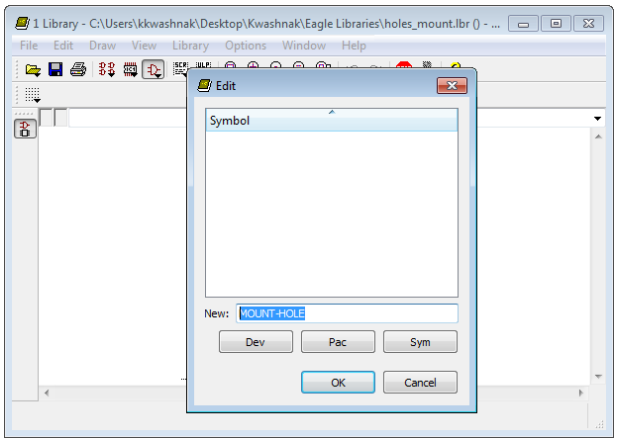


Fig. 125 mount_hole library

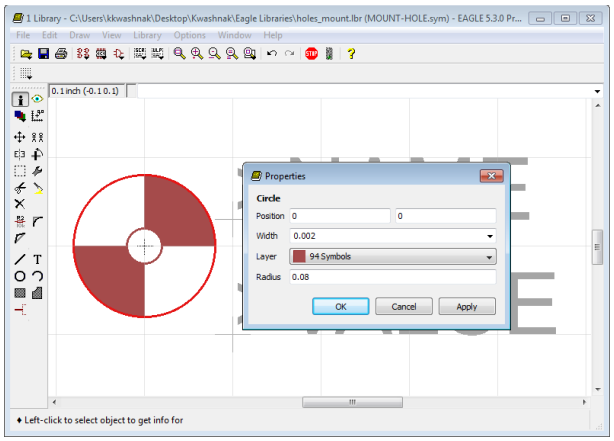


Fig. 126 MOUNT-HOLE symbol circle 1

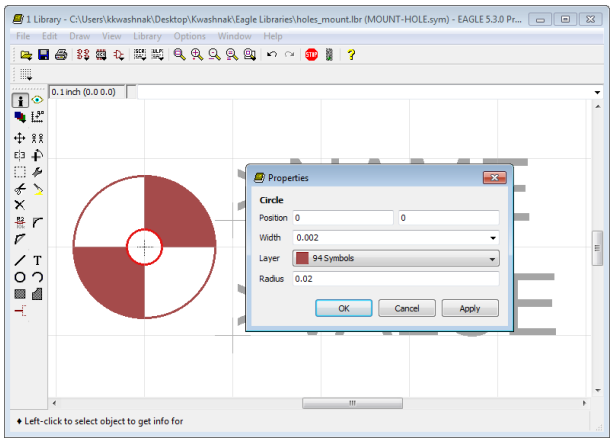


Fig. 127 MOUNT-HOLE symbol circle 2

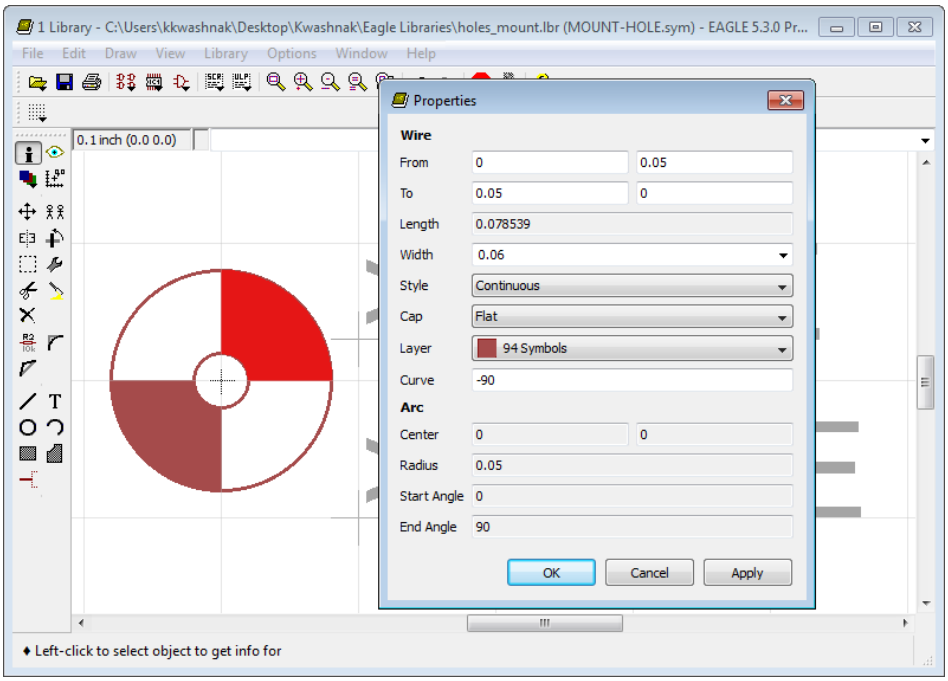


Fig. 128 MOUNT-HOLE symbol infill

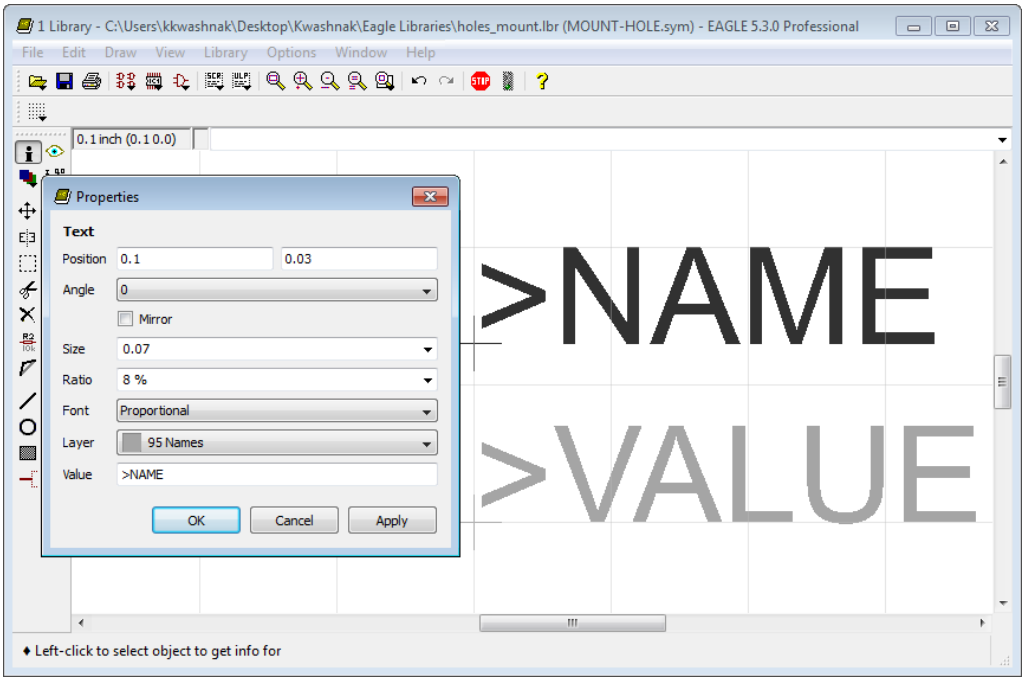


Fig. 129 MOUNT-HOLE symbol text

Once the symbol is completed, save the file.

Navigate to the <Device> and create a new device called “SYM-MOUNT-HOLE” (Figs. 130 and 131).

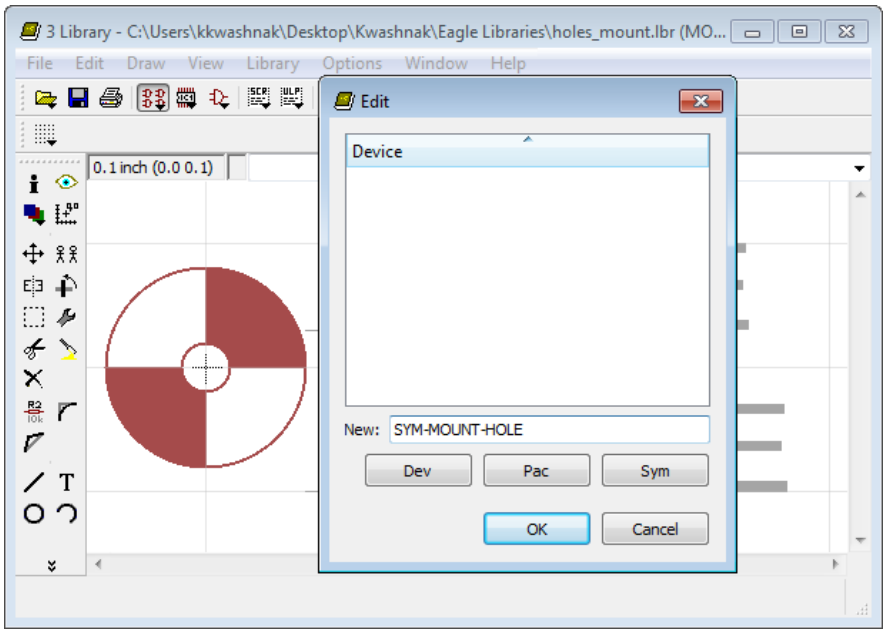


Fig. 130 SYM-MOUNT-HOLE device creation

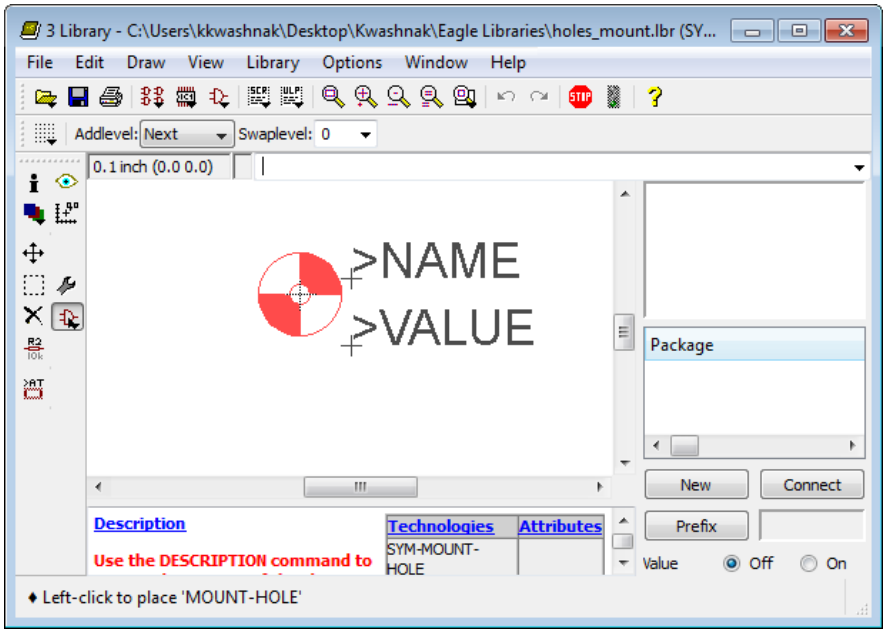


Fig. 131 SYM-MOUNT-HOLE device complete

After completing the device, save the file and return to the schematic.

In the schematic, use the <Add> tool to insert the 'SYM-MOUNT-HOLE' object (Fig. 132).

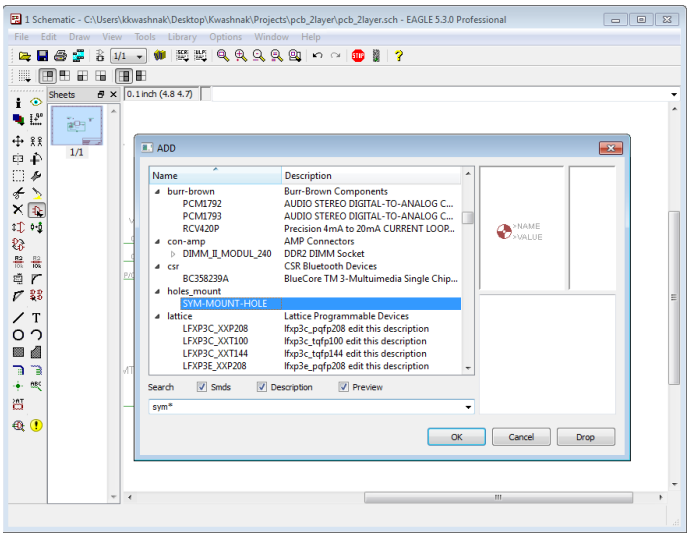


Fig. 132 SYM-MOUNT-HOLE object

Use the <Text> tool to incorporate necessary information on the schematic, like "Plated Through, Mounting Holes". Next, navigate to the <Board> tool and use the <Via> tool to construct mounting holes (Fig. 133). Configure the object's information with the <Info> tool.

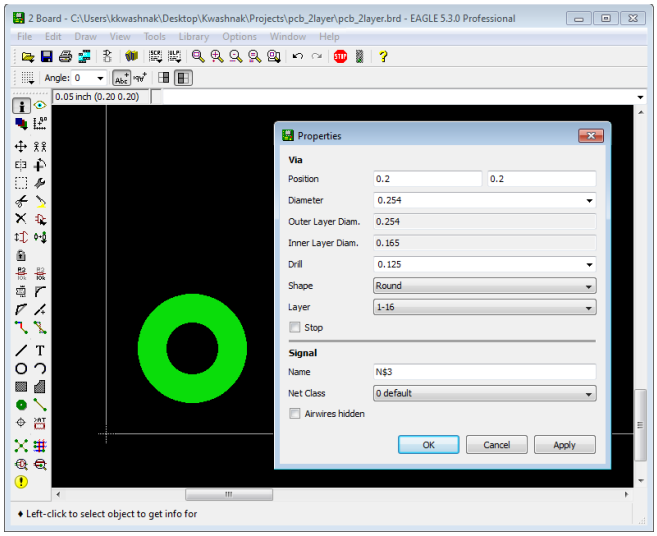


Fig. 133 Via used as plated through hole

Remember, the schematic only shows the symbol of the mounting holes, whereas on the board there is a via/mounting hole element. There is a disconnect between the schematic and the board with this method, but the user must understand the project's specifications upon designing and inspecting the project.

4.5.3 Changing Component Designation

Once a component is placed on the schematic, the “>NAME” tag displays the symbols name. In Fig. 134, the microcontroller is referred to as ‘U$1’. If multiple microcontrollers are added, the number increments +1, thus the schematic would state ‘U$2’, ‘U$3’, and so on. To change the designation ‘U’ to another letter or prefix, edit the device in the library and configure the <Prefix> option (Fig. 135).

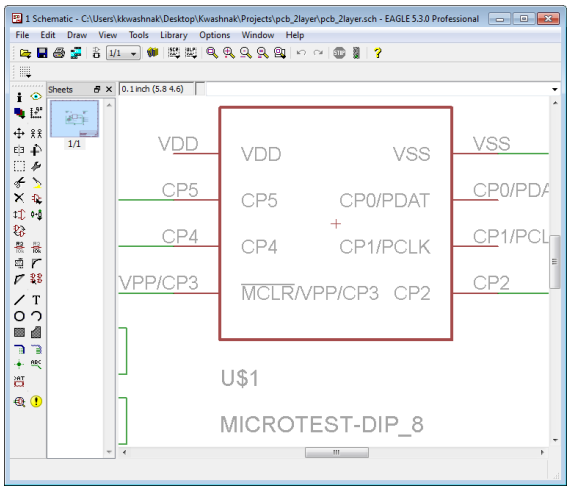


Fig. 134 >NAME $U1 component designation

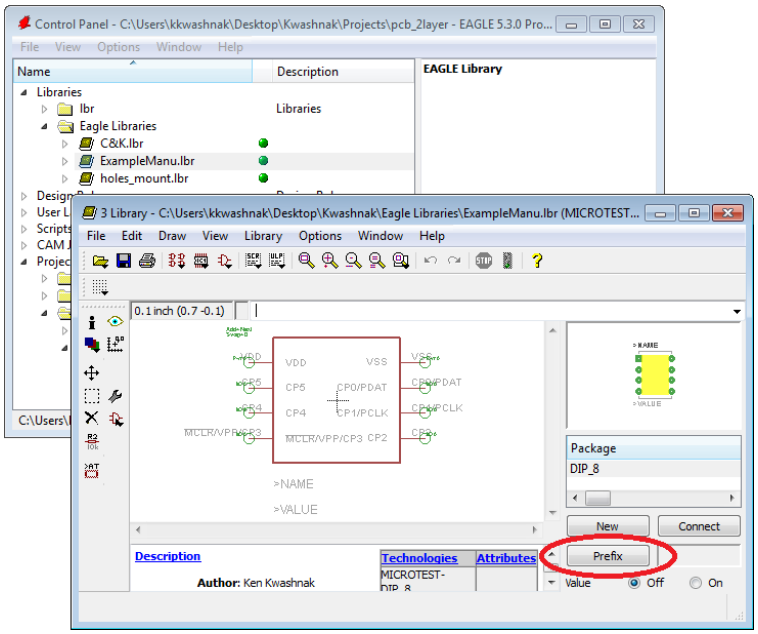


Fig. 135 <Prefix> Option

Once a prefix is added and if a device is already on the schematic, delete the object and reinsert. The object designation will change to the next prefix.

Use the <Line> tool to connect component pins together (Fig. 136). Use the <Info> tool to change the line's name (also called a 'Net') (Fig. 137). A 'Bus' is simply a connection of 'Nets'.

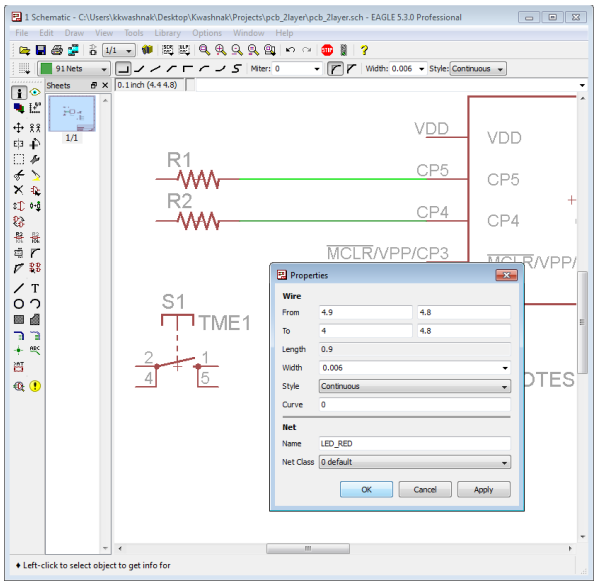


Fig. 136 Defining line properties

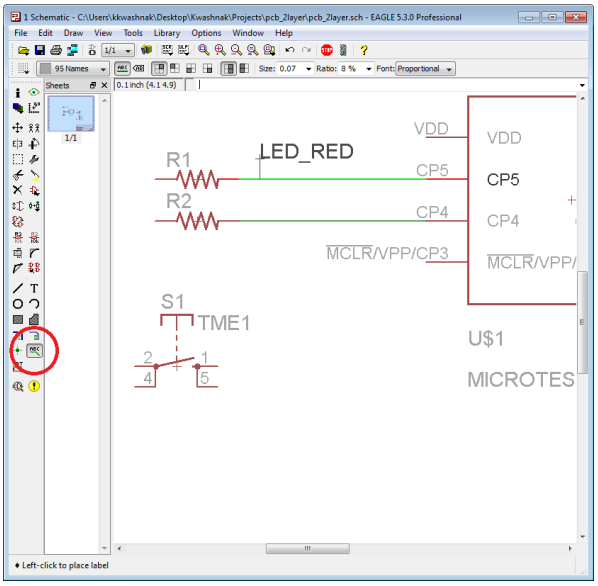


Fig. 137 <Label> Tool

4.6 Step 6: Map Nets and Connections

Use the <Wire> tool to connect component pins (Fig. 138).

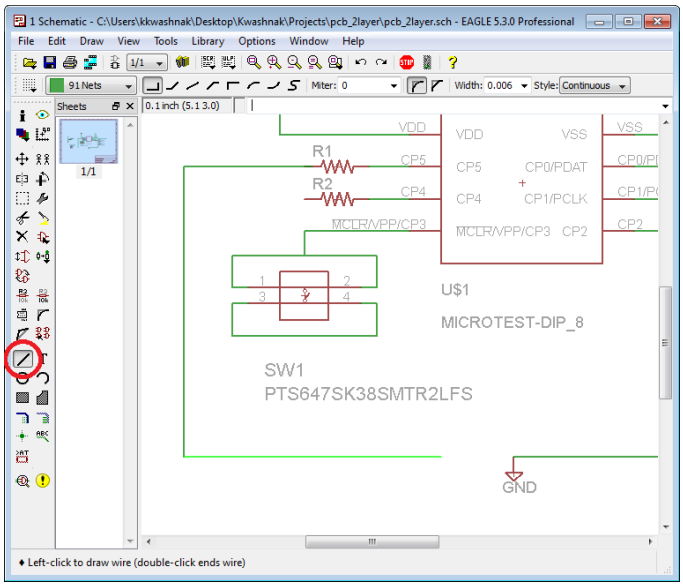


Fig. 138 Connecting component with <Wire> tool

Use the <Name> tool on wire elements to formulate signal names (Fig. 139). If a wire is renamed to an existing wire name, a prompt for merging two nets arises (Fig. 140). Wires may be renamed from their 'N$1' or 'N$2' to assist organizing signals and nets.

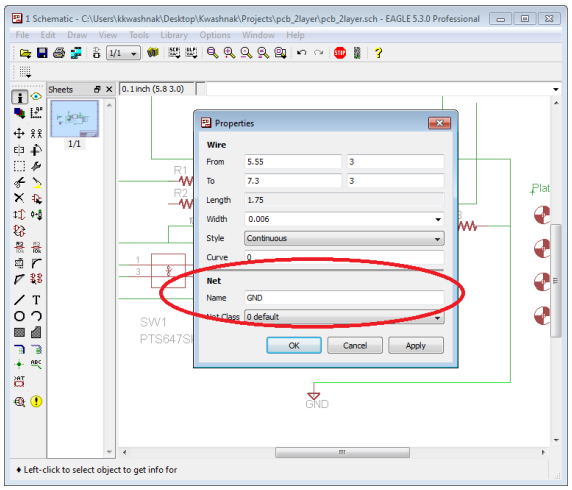


Fig. 139 Renaming nets and defining signals

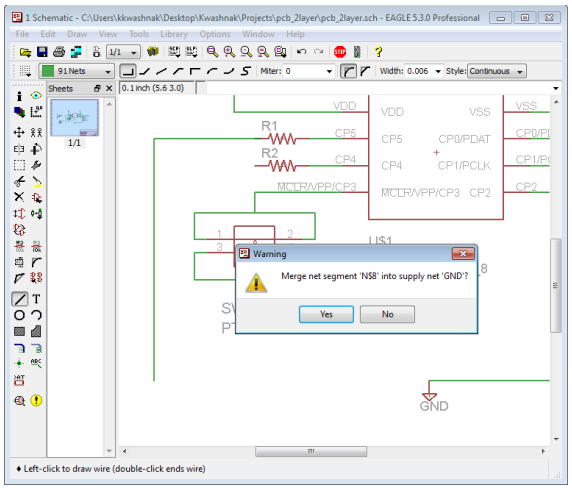


Fig. 140 Merging nets

In the end, the schematic may look like Fig. 141.

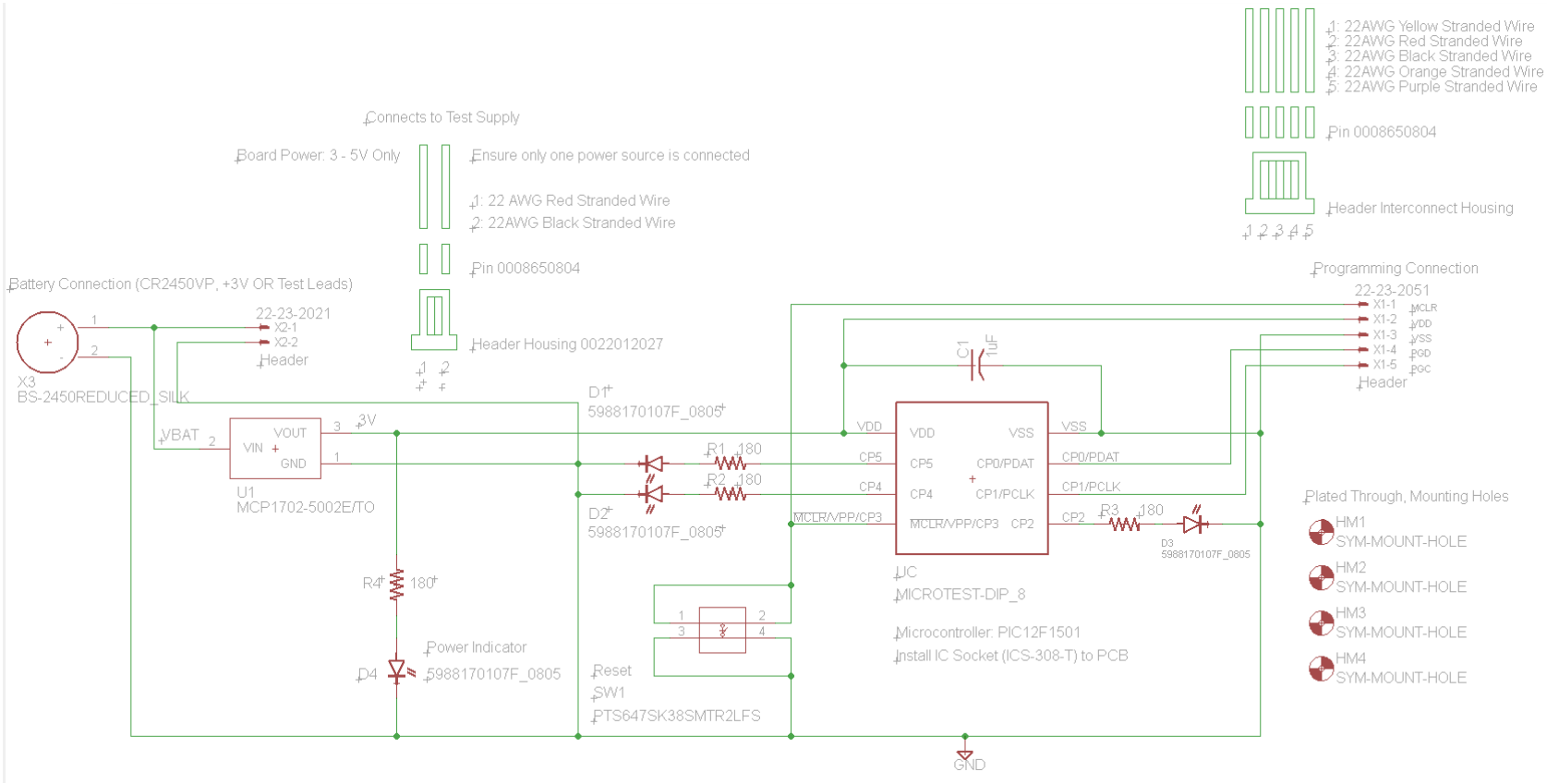


Fig. 141 Completed schematic

4.7 Step 7: Run Electronic Review Check

The Electronic Rule Check, <Erc> tool, checks over the schematic for connection errors, such as improperly routed pins, missing connections, and paired pin state configurations (Fig. 142). Using this tool will jump to the Schematic Editor.

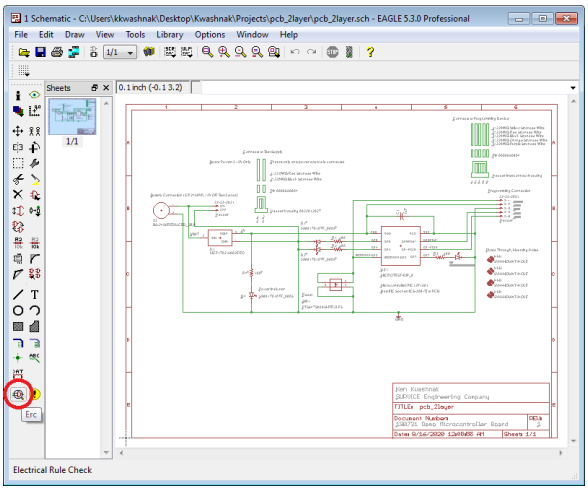


Fig. 142 <ERC> tool

The ERC reviews connections and related properties (Fig. 143). For example, if a pin is labeled as ‘pwr’, the ERC checks if the incoming connection is also labeled with ‘pwr’, so the signal type is in agreement.

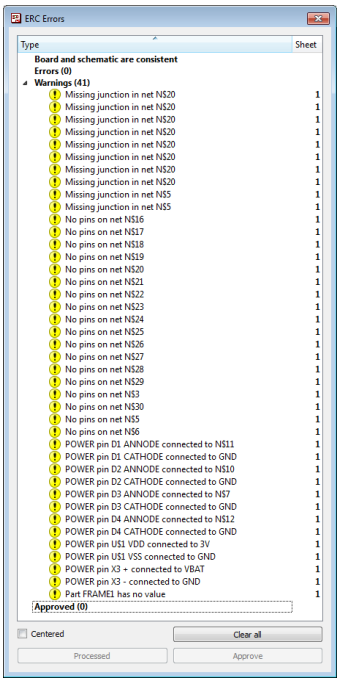


Fig. 143 ERC dialog

Although this design does not have any glaring errors, there are multiple warnings that could potentially be critical errors. Clicking on the warning moves the screen to the issue location (Fig. 144).

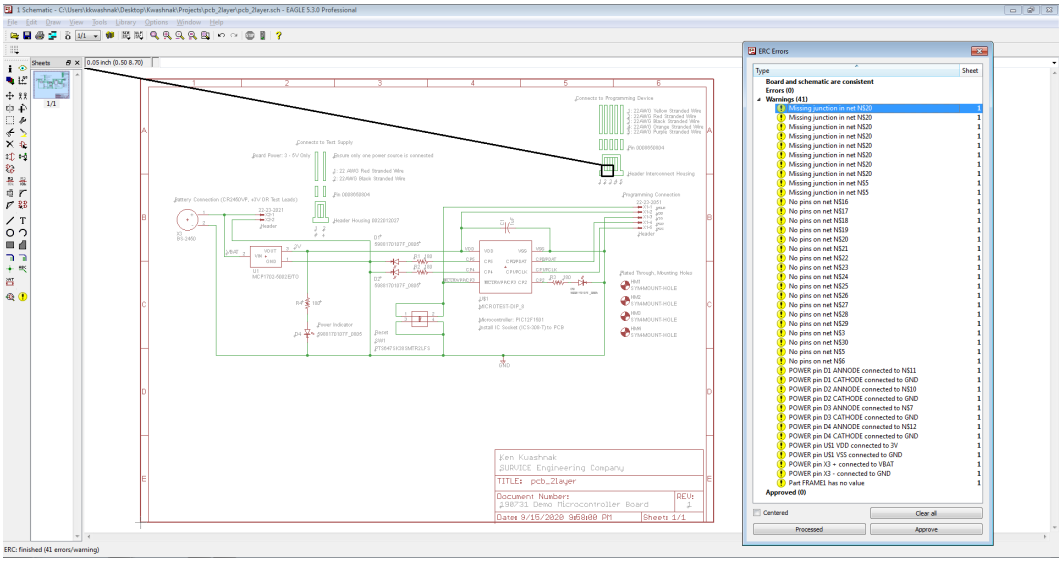


Fig. 144 Warning list

The top set of ‘missing junctions’ and ‘no pins’ makes sense; the <Wire> tool was used to create a diagrams. These diagrams have no connection to the PCB, so the warnings may safely be ignored or <Approved>. These floating wire segments will not affect the board file.

Next, after examining the ‘POWER pin D1 ANNODE connected to N$11’, the LED object's pins are configured as both 'pwr' pins. Thus, the ERC is checking to make sure that the object is indeed hooked up correctly. This is for the designer to examine and approve, since the designer knows about the input and out connections of the device. In this case, the LED is configured correctly; the warning is <Approved>.

Following through, the remaining errors can be reviewed and <Approved> (Fig. 145).

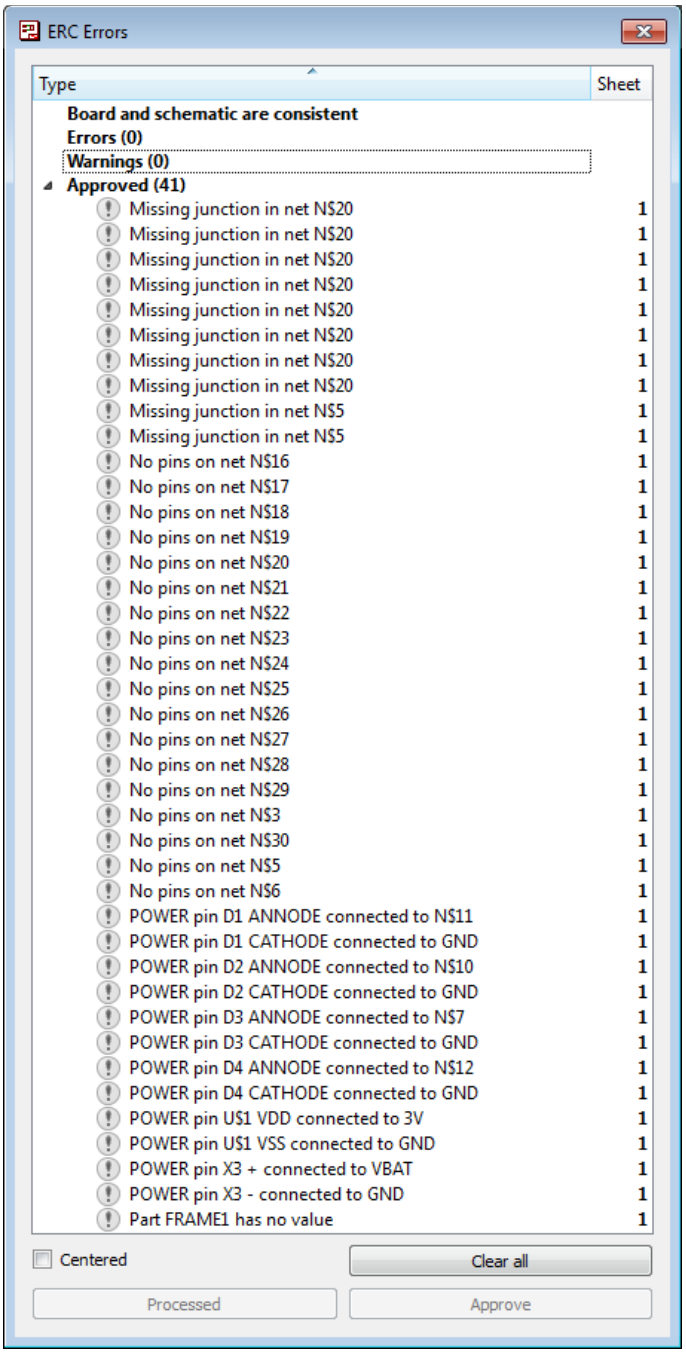


Fig. 145 Approved ERC

4.8 Step 8: Create a New Board Layout

Click on the <Board> icon to switch views (Fig. 146). Navigate to <View>, <Grid>, and edit desired settings.

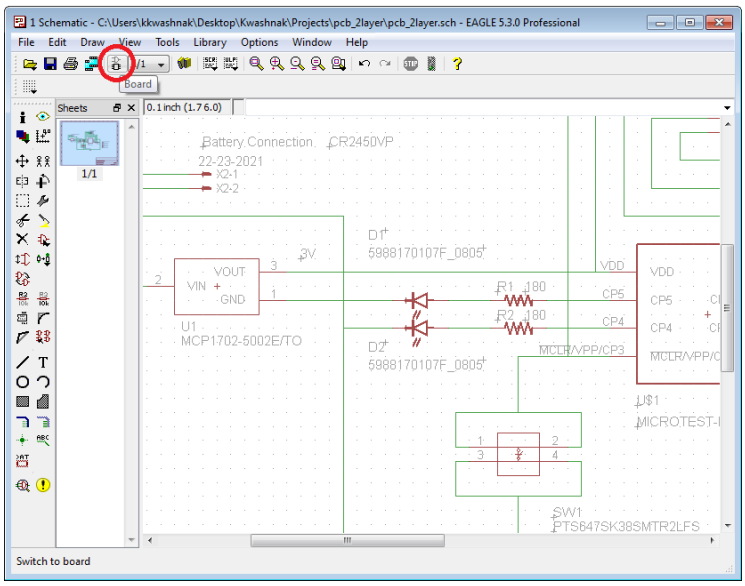


Fig. 146 <Board> icon

In addition, for this tutorial, the default black background for the Board workspace is changed to white. To mirror this step, switch to the EAGLE Control Panel, go to <Options>, and finally <User interface...> (Fig. 147). Under 'Layout', change 'Background' from <Black> to <White>.

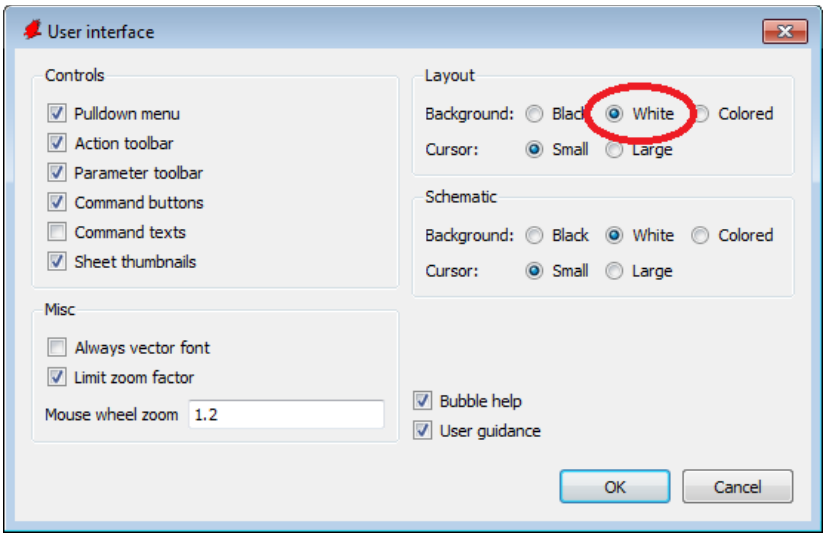


Fig. 147 Changing board workspace background color

4.9 Step 9: Define PCB Settings

Use the <Drc> tool in the Board Editor to check and modify the standards for the PCB (Figs. 148–158). If errors are found, the board may need trace rework, components edits, and/or and device redesign. For this step, review PCB manufacturers and their manufacturing specifications.

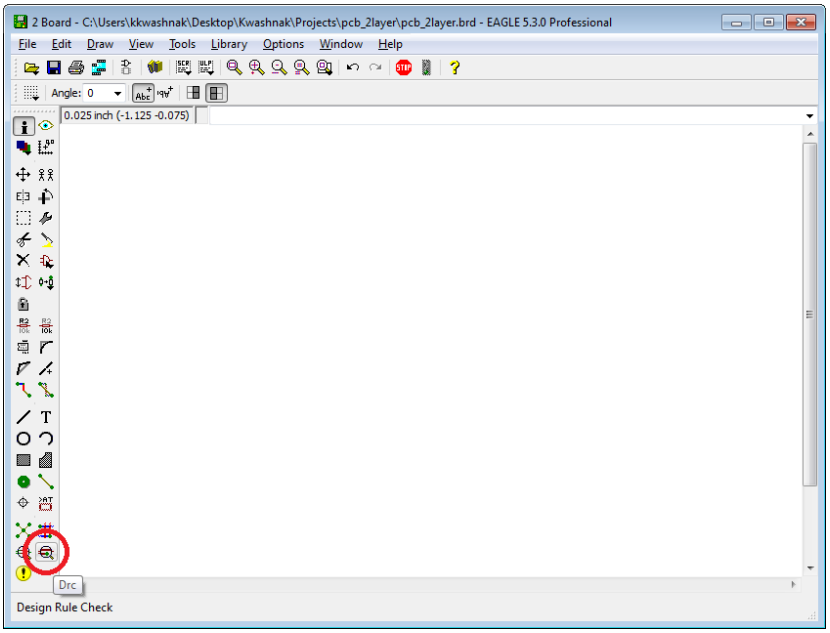


Fig. 148 Design rule check on completed board

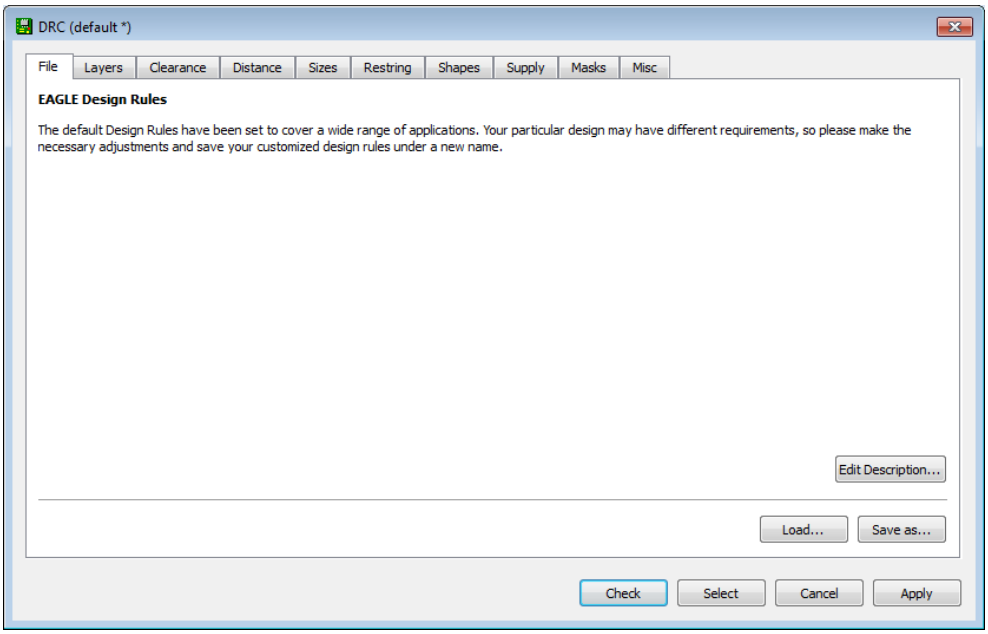


Fig. 149 DRC dialog

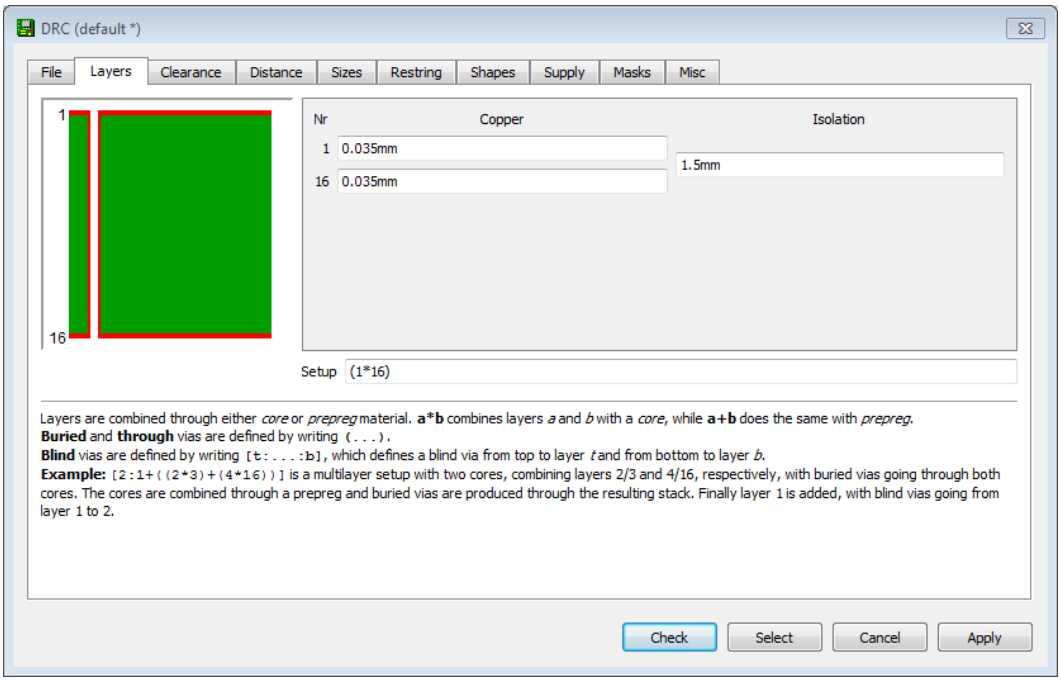


Fig. 150 Layers

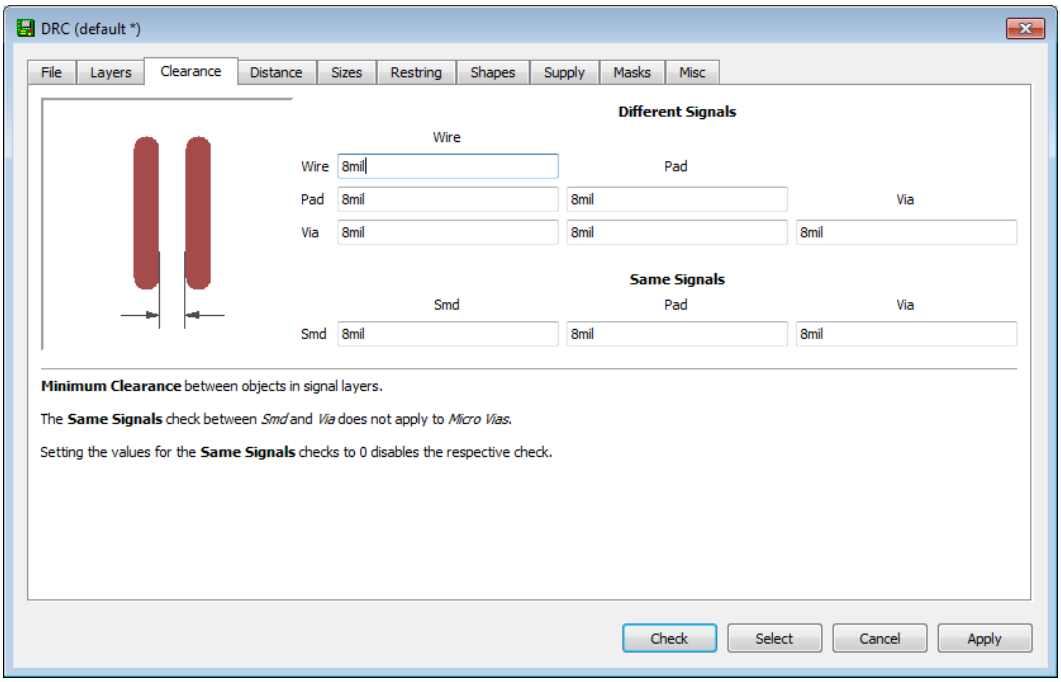


Fig. 151 Clearance

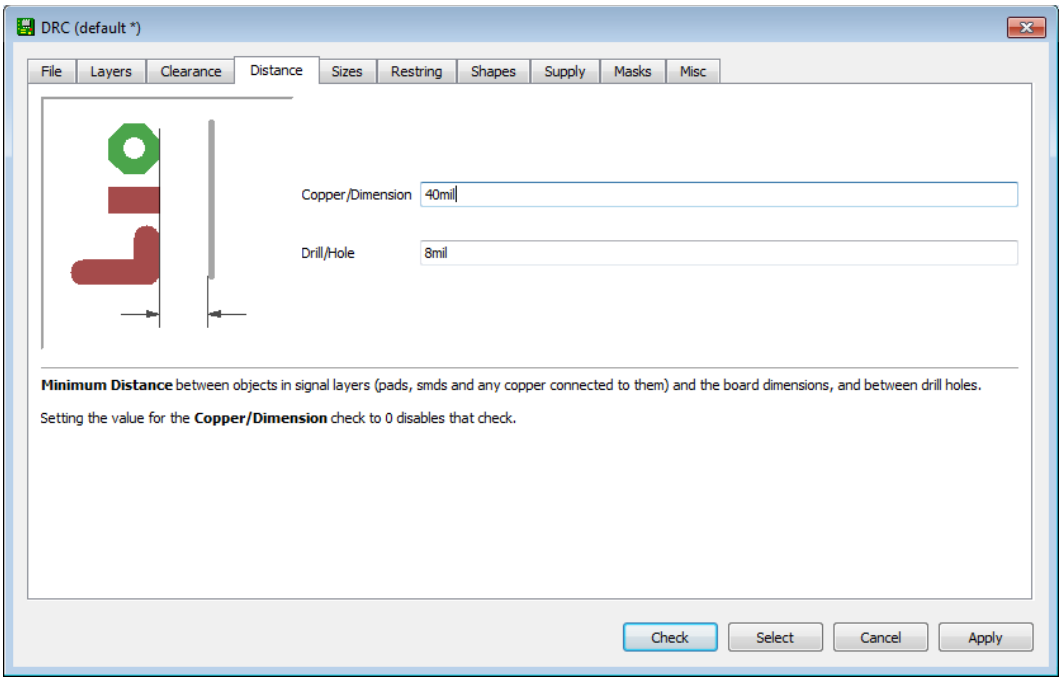


Fig. 152 Distance

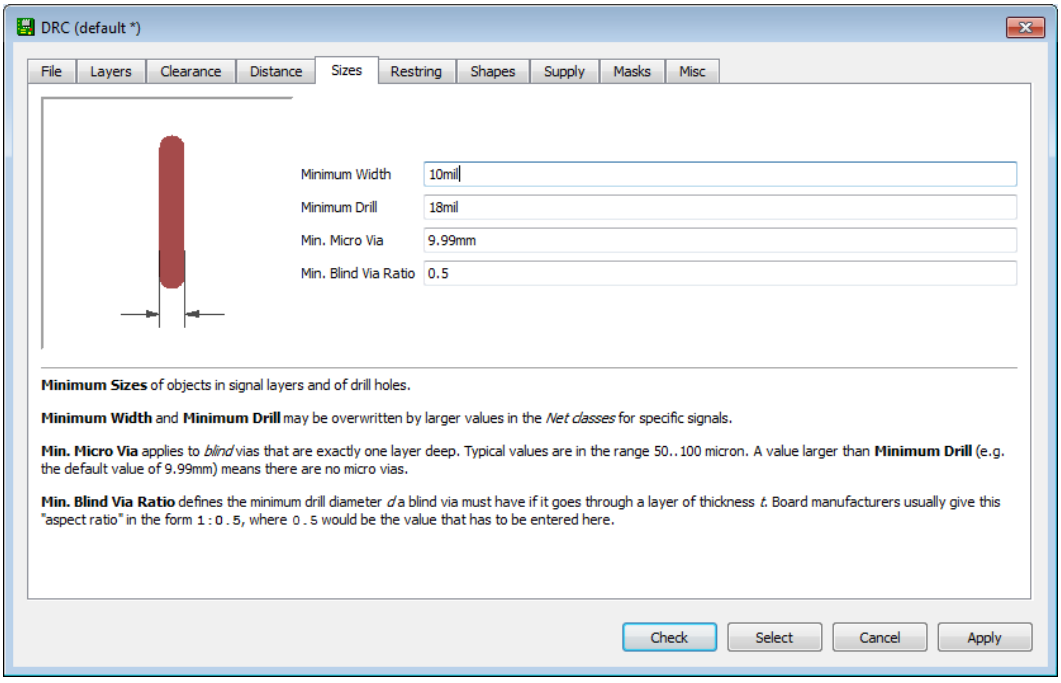


Fig. 153 Sizes

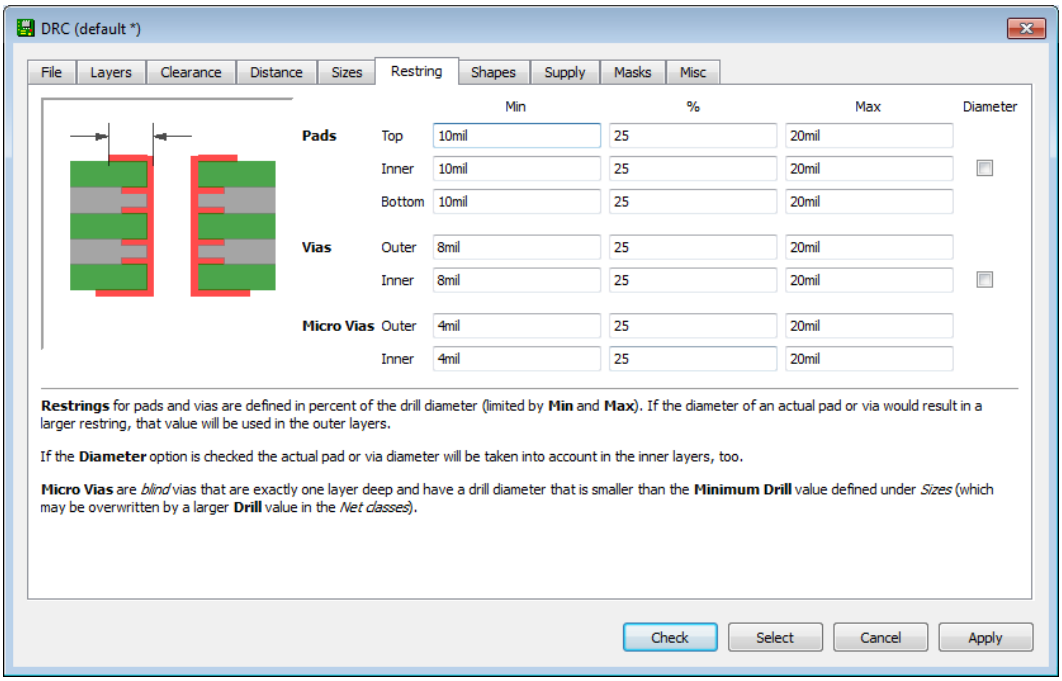


Fig. 154 Restring

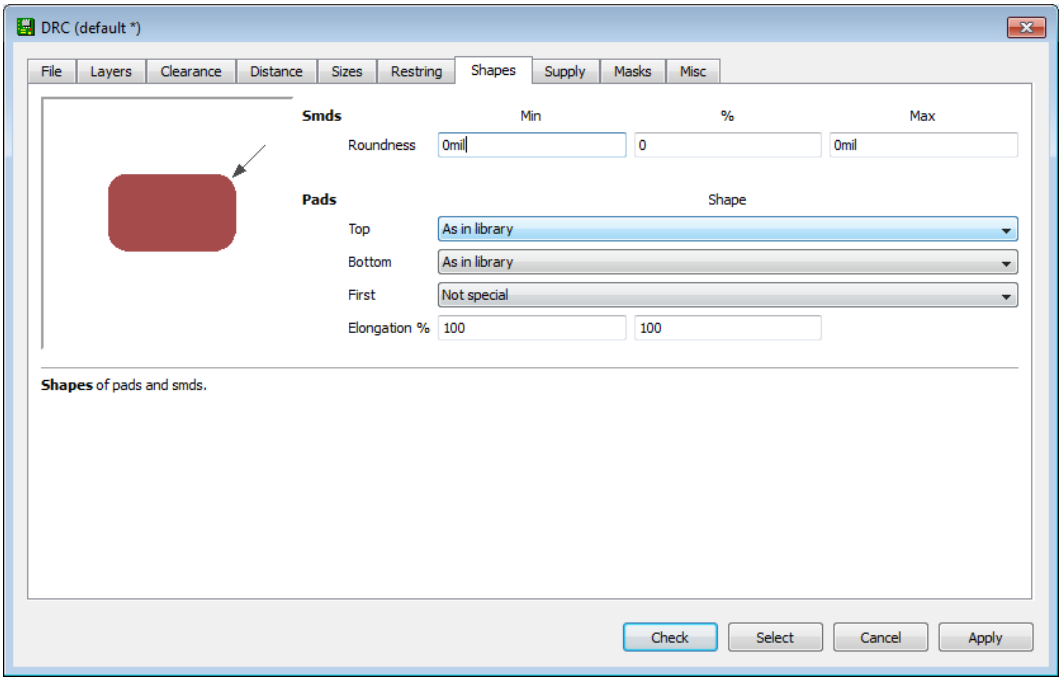


Fig. 155 Shapes

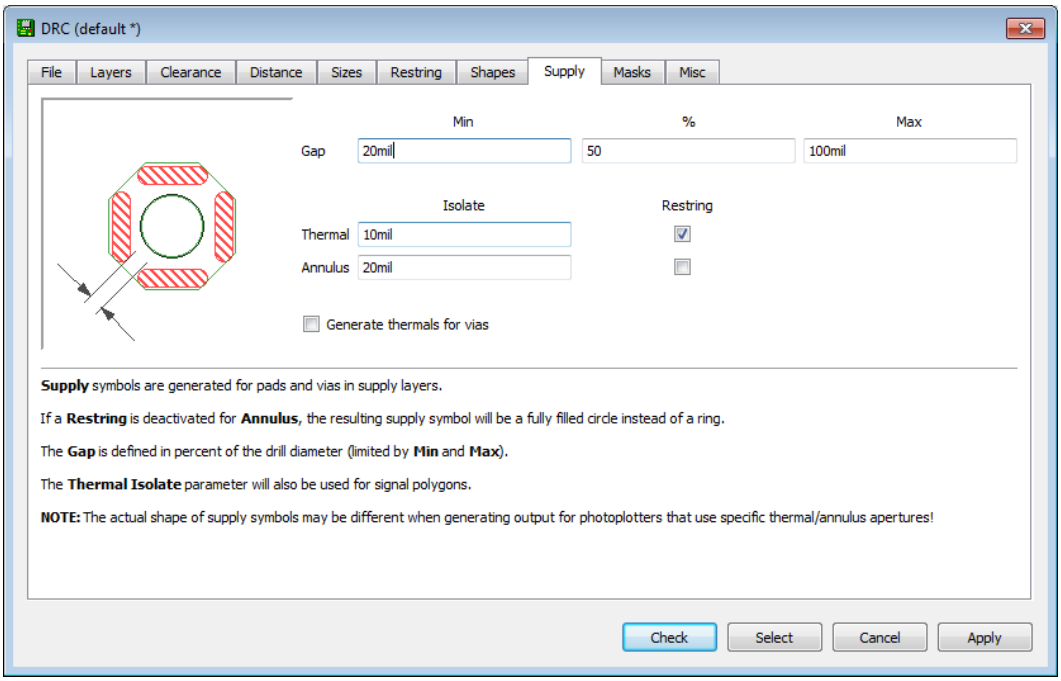


Fig. 156 Supply

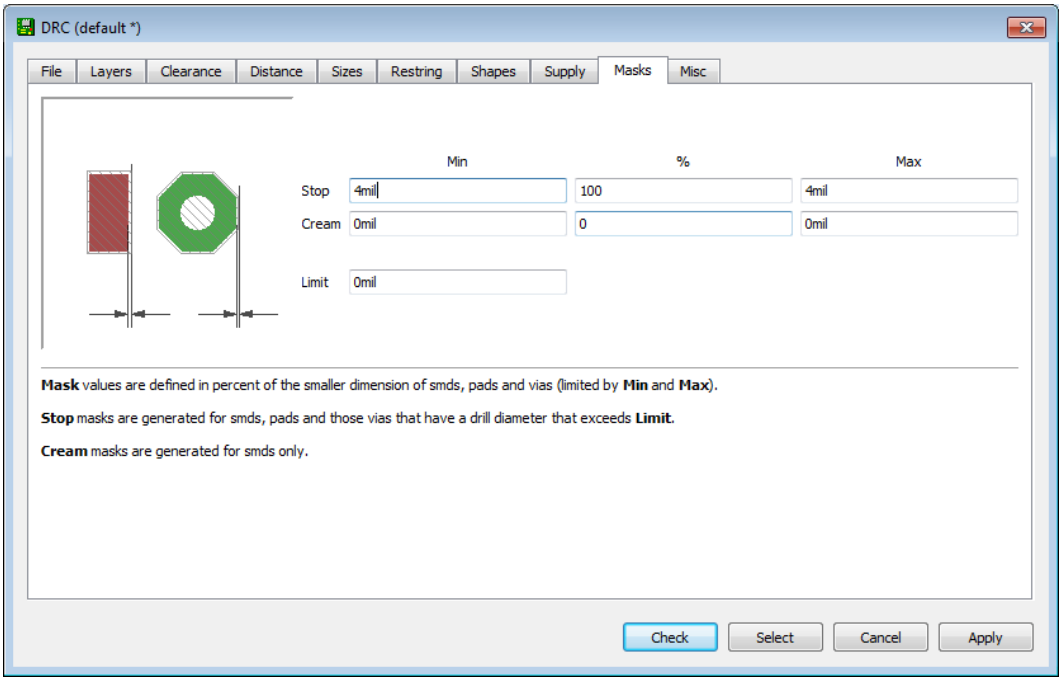


Fig. 157 Masks

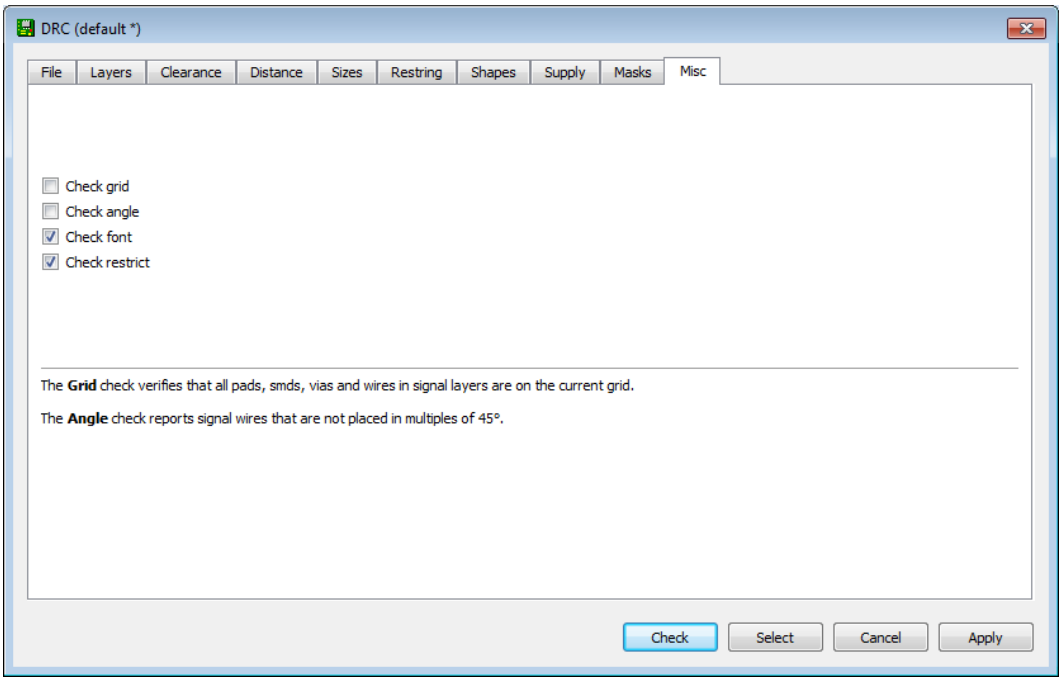


Fig. 158 Misc

4.10 Step 10: Organize Board Components

Moving back to the Board Editor, resize the board using <Info> or <Move> tool. The exact board size may not be known at this moment, but set the desired overall dimension. To assist with sizing via the <Move> tool, examine the cursor coordinates, circled in red in the Fig. 159. When creating a board's physical outline, use the layer '30 Dimension'.

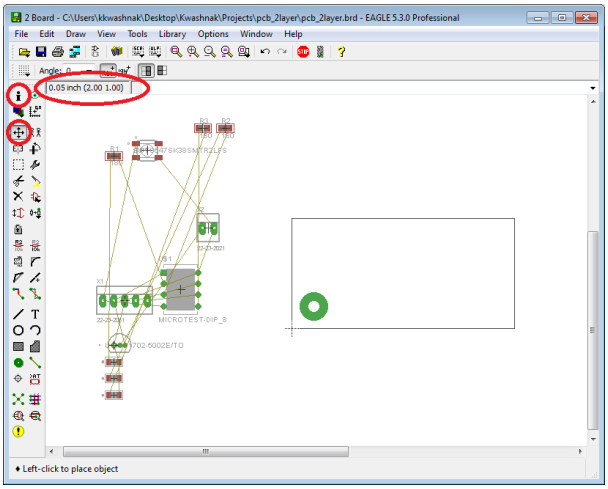


Fig. 159 Organizing components

On the <Info> tool, notice the ‘Layer’ the object is residing. Using the <Move> tool, arrange the components within the board outline as in Fig. 160. The yellow airwires are the connections to each component, as in the schematic. If an object is missing these airwires, double-check your connections in the schematic. Upon clicking on an object, if a component overlaps another, right-click the mouse to cycle through the selection.

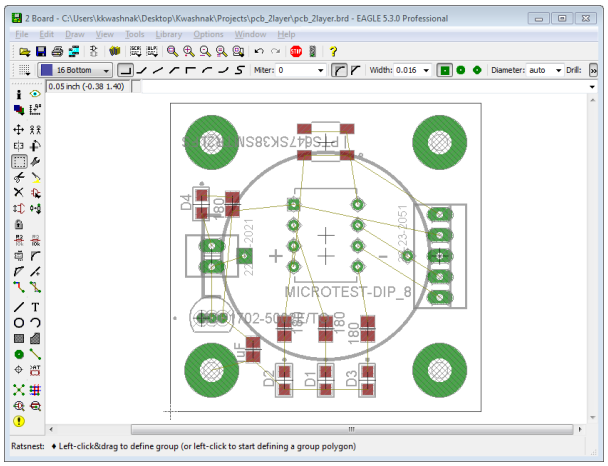


Fig. 160 Board layout

To move a device to the bottom of the board, use the <Info> tool on the object and select the ‘Mirror’ option (Fig. 161).

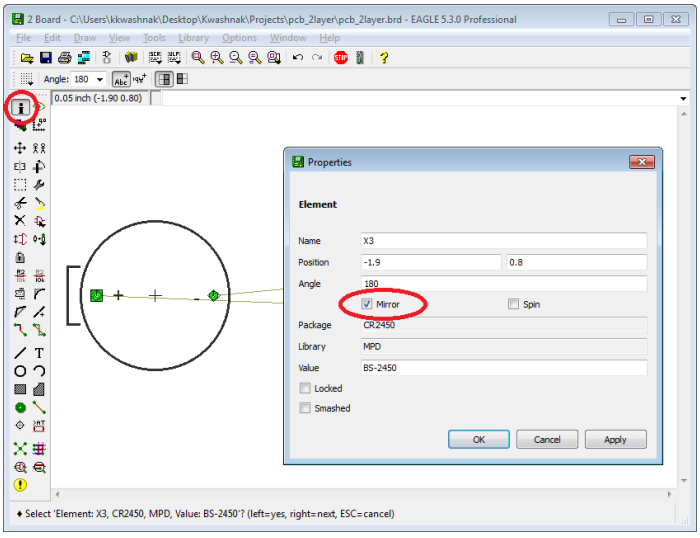


Fig. 161 Placing component on bottom of board

Use the <Ratsnest> tool to reallocate airwires. The yellow lines (layer ‘19 – Unrouted’) between objects are created via connections between elements in the schematic (Fig. 162).

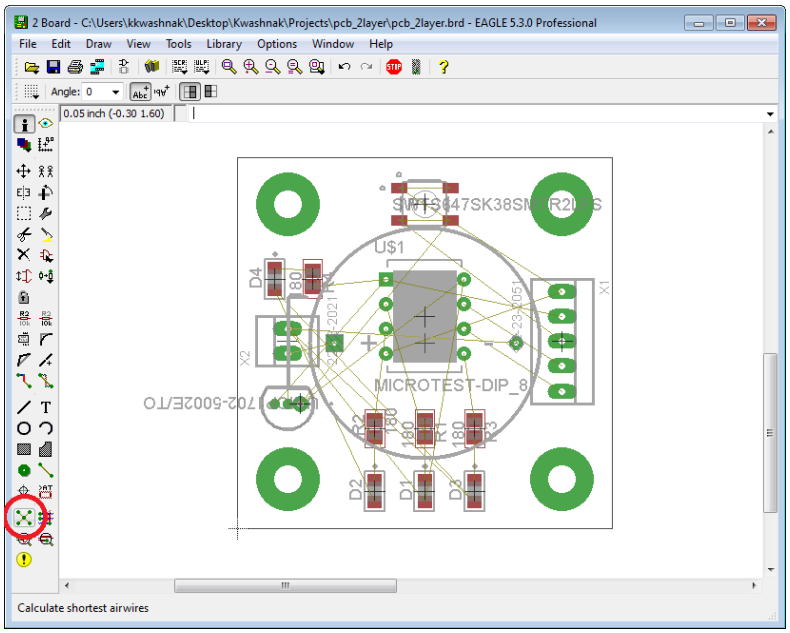


Fig. 162 Recalculating airwire locations

4.11 Step 11: Create Copper Regions

Now, to create copper pours for the top and bottom layers, encapsulate the board's top copper layer via the <Polygon> tool (Fig. 163).

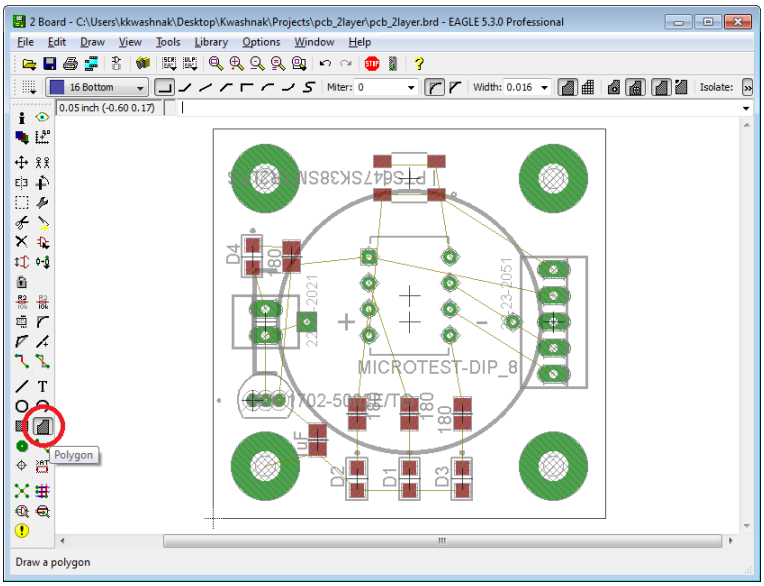


Fig. 163 <Polygon> tool

Draw a square inside the board, spaced away from the board's edge about 50 mils, on the '1 Top' layer (Fig. 164). Repeat for the '16 Bottom' layer (Fig. 165). After each polygon is drawn, the lines from the <Polygon> tool will appear dotted.

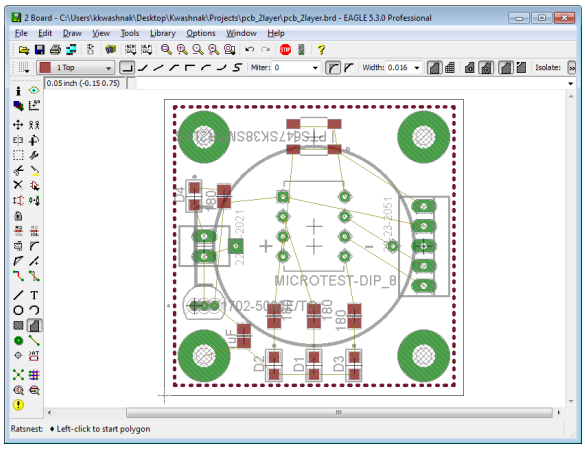


Fig. 164 <Polygon> top copper layer

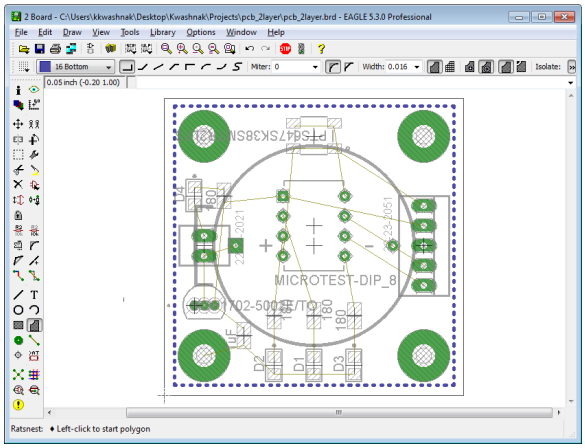


Fig. 165 <Polygon> bottom copper layer*

Double-check the information of the polygon to ensure the polygons are on their respective layers.

Using the <Info> tool and selecting one of the polygons under the 'Polygon' tab, 'Polygon Pour', check the 'Solid' option (Fig. 166). This will generate a copper layer on the specified layer.

* '1 Top' layer was hidden using the <Display> tool.

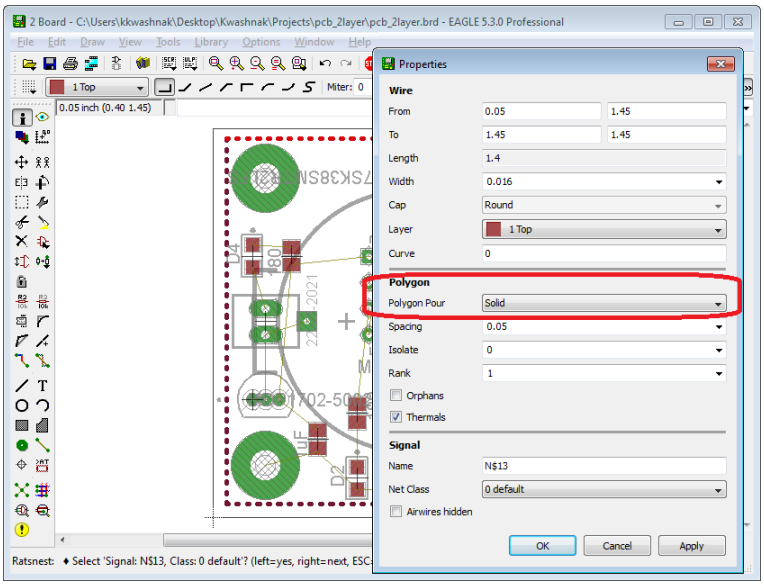


Fig. 166 Polygon information

Rename the bottom layer (blue) polygon to GND, using the 'Signal' area in the 'Properties' window (Fig. 167).

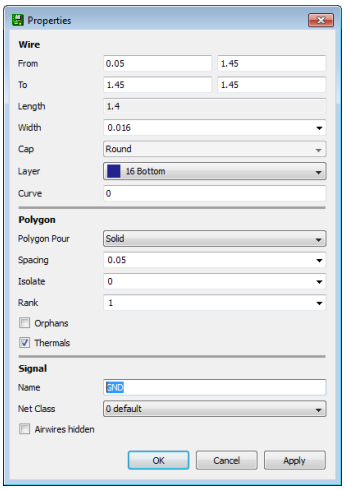


Fig. 167 Polygon signal name

If an error is received, in the board workspace, use the <Name> tool to edit the object's Signal name (Figs. 168 and 169).

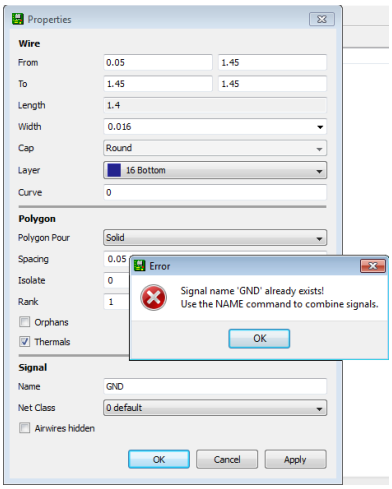


Fig. 168 Renaming signal error

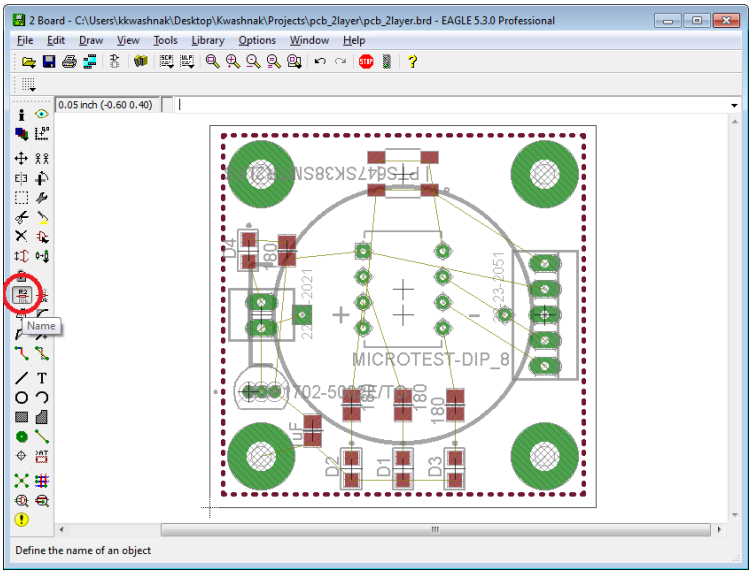


Fig. 169 <Name> Tool on bottom layer

Afterward, use the <Ratsnest> tool once again to formulate copper layers and airwires (Fig. 170).

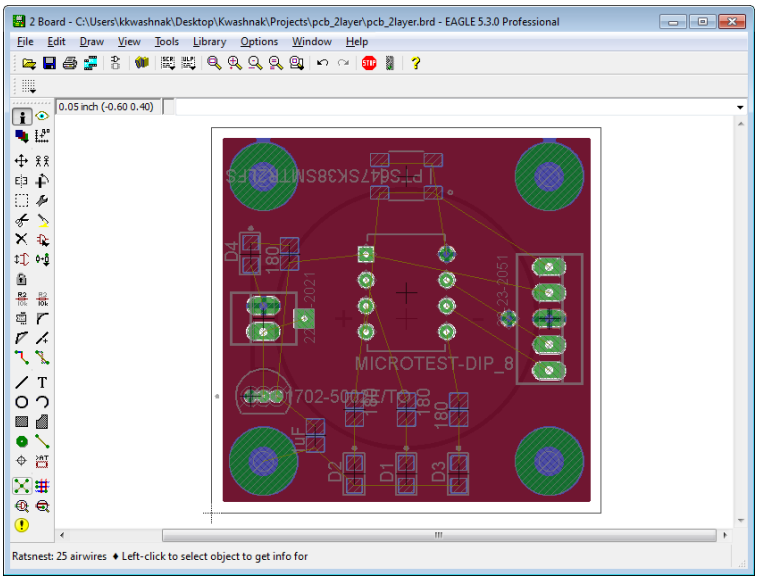


Fig. 170 Formulating copper layers

If the in-filled polygons obstruct the view of airwires and routing work, use the <Ripup> tool on the drawn polygons (Figs. 171 and 172). The infill should revert back to the dotted lines. After clicking on the <Ratsnest> tool, click on the <Go> icon to remove all signals on the board. This will also remove any vias, even the custom vias for the mounting holes.

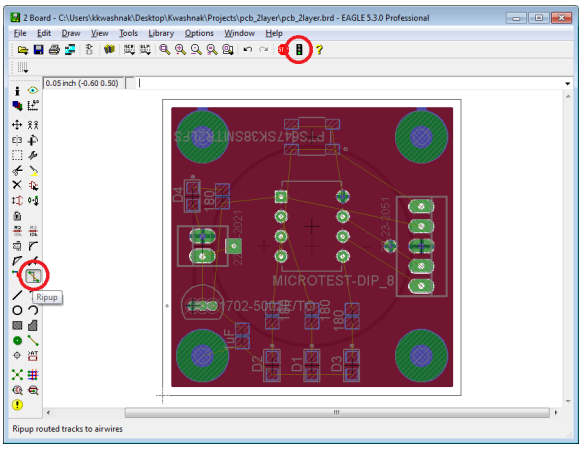


Fig. 171 <Ripup> tool, delete all signals

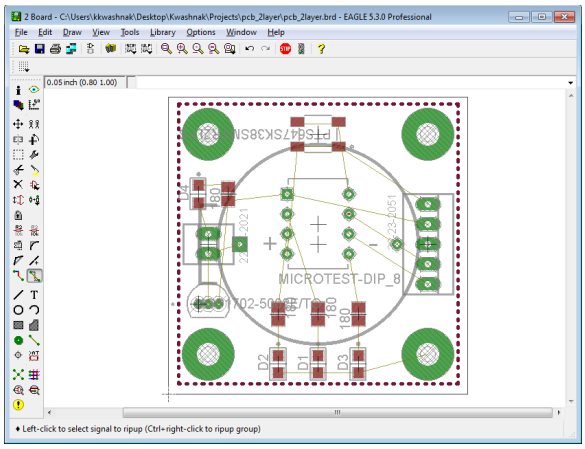


Fig. 172 Cleared workspace

4.12 Step 12: Route Traces

Use the <Route> tool to place trace connections between components (Fig. 173). Follow the airwires to connect components or create custom net designs.

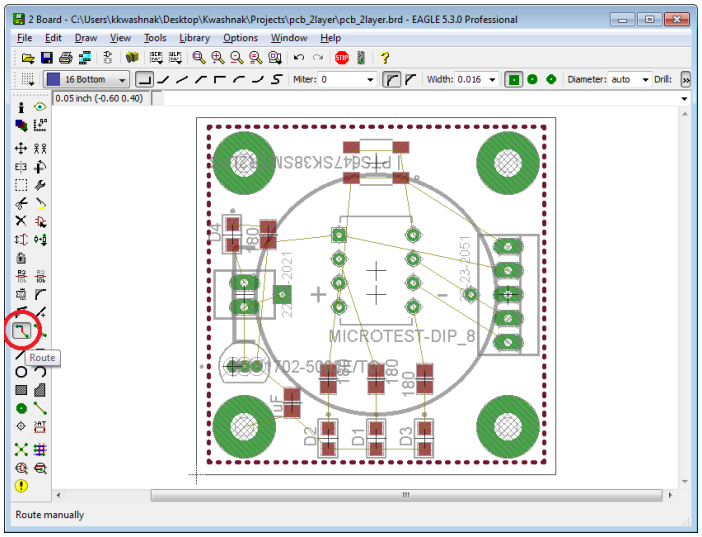


Fig. 173 Creating traces with the <Route> tool

Using the <Info> tool on a wire, examine the 'Wire' and 'Signal' properties of the trace. Due to the simple nature of this PCB, routing traces at a default width will suffice, but for more complicated circuits, trace properties become incredibly important. One reference for trace calculation is the "PCB Trace Width Calculator" from Advanced Circuits.[36] Continue to route all traces on the board. Right-clicking while placing a trace adjusts the type of line used, and the options for the line may be found in the property bar circled in Fig. 174.

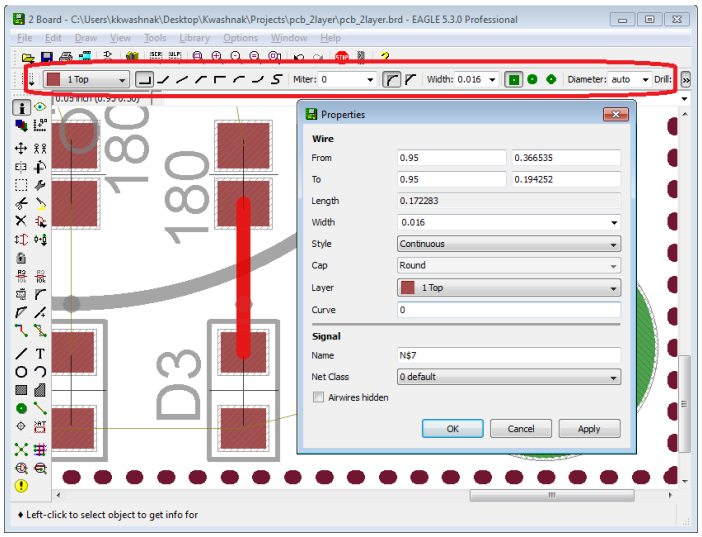


Fig. 174 Trace properties

If the trace is improperly placed, use the <Ripup> tool to delete the trace and use the <Ratsnest> tool to auto-replace the airwire. Switching from the '1 Top' to '1 Bottom' layer mid-route will create a via, which can travel from the top of the board to the bottom (Figs. 175–177).

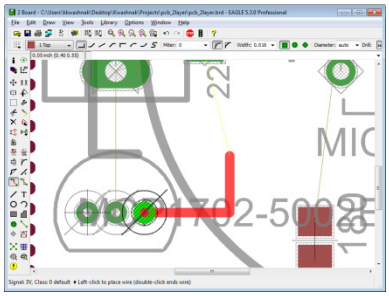


Fig. 175 Trace top layer

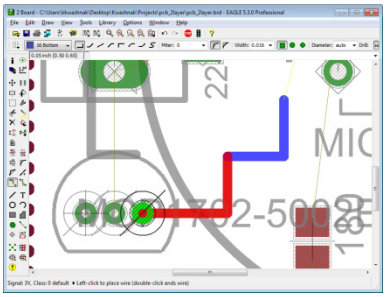


Fig. 176 Trace bottom layer

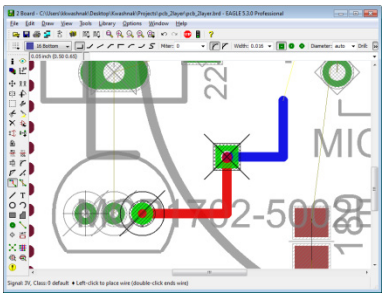


Fig. 177 Via

The <Auto> tool is a trace auto-router (Fig. 178), which may be useful in guiding board design or for quickly producing trace layouts. The '41 tRestrict', '42bRestrict', and '43 vRestrict' layers control the auto-router layout behavior. For example, if a polygon (square) was placed over a region, the auto-router will not set traces within the specified area.

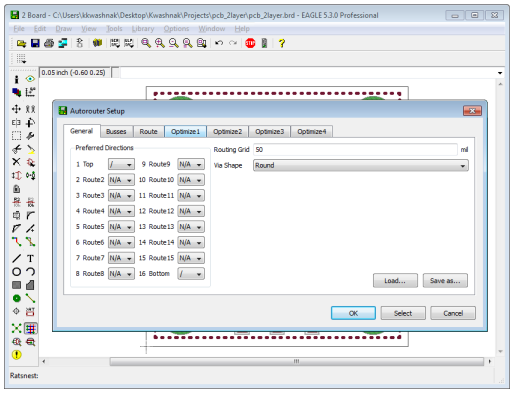


Fig. 178 <Auto> Tool settings

Following the autorouter conventions defined in Table 12, the output mirrors Fig. 179. The infill of the PCB now has traces routed between components.

Table 12 Auto-router directions

Symbol	Preferred Direction
-	Left to right
|	Up and down
/	45 deg, bottom left to top right
\	45 deg, top left to bottom right
*	No preference
Auto	EAGLE will access and optimize

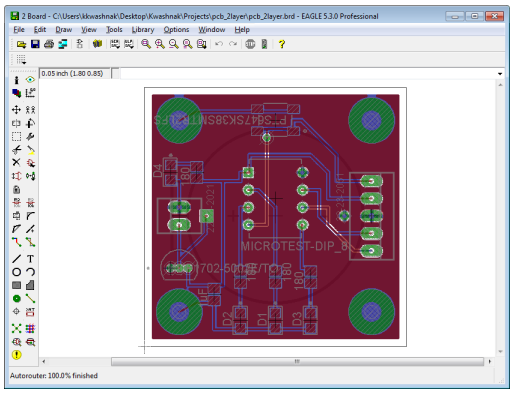


Fig. 179 Auto-routed board

4.13 Step 13: Edit Silkscreen

Each device's package may have a soldermask (silkscreen) that references text from the '21 tPlace', '22 bPlace', '25 tNames', and '26 bNames' layers. The soldermask dictates the component's outline, description, and/or value on the surface of the PCB. Using the <Display> tool, turn off all layers except layer '21 tPlace'. Use the <Text> tool to create "Top Silkscreen" and place it next to the board (Fig. 180). Ensure the text is on layer '21 tPlace'. This note is used as a reference and will not be printed on the board.

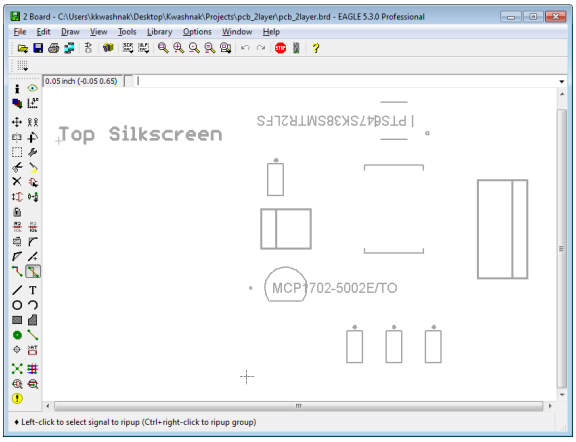


Fig. 180 Top silkscreen

It is evident that some of the imported component's silkscreen will need a few edits because the text is too long and it overlaps other objects. Find the device in the Library and edit the text. For example, the MCP1702-5002E/TO's ">NAME" and ">VALUE" text layers are changed from layer '25 tPlace', to layer '51 tDocu'. Continue to edit all necessary component text. Later, custom text will be written adjacent to their respective component.

After editing all the devices' packages, update all libraries with <Library> tab, <Update all...> (Fig. 181).

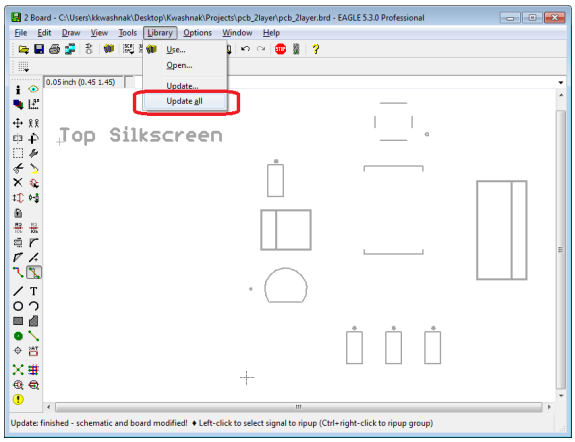


Fig. 181 Updating libraries

Since there are only a handful of parts, each component will be manually labeled to assist with PCB assembly. Use the <Text> tool to label components, the designer's name, date, board version, and any other necessary details (Fig. 182). Text is assigned to either layer '21 tPlace' or '22 bPlace'. It may be helpful to turn on/off other layers to help with character placement, such as '1 Top', '16 Bottom', '17 Pads', '18 Vias', '20 Dimension', '21 tPlace', '22 bPlace', '29 tStop', '30 bStop', '41 tRestrict', '42 bRestrict', '44 Drills', and '45 Holes'.

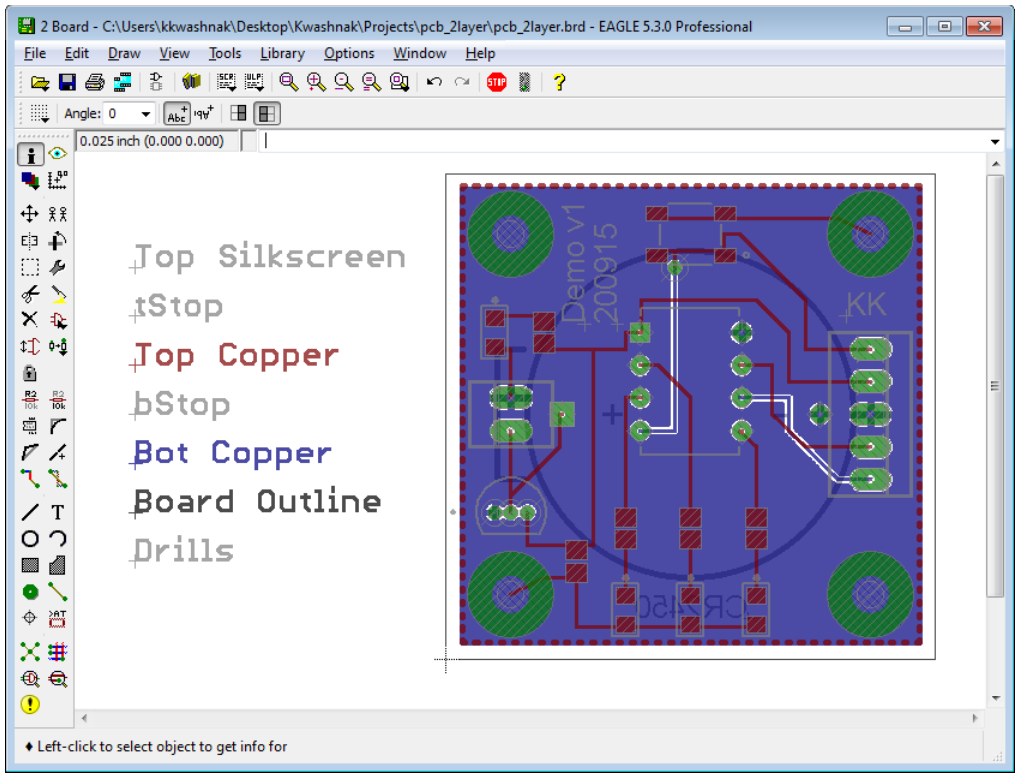


Fig. 182 Completed board

4.14 Step 14: DRC

The <DRC> tool checks the board for various issues, such as component overlap, layer interference, open traces, and so on (Fig. 183).

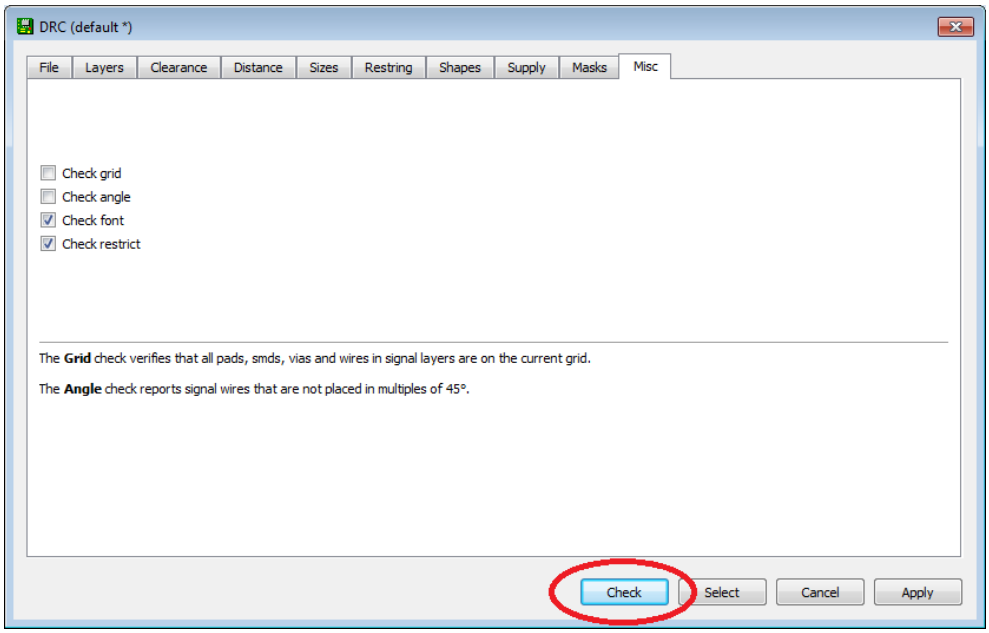


Fig. 183 DRC check

After examining the errors (Fig. 184), it looks like a majority of the silkscreening interferes with pads. There are multiple solutions:

1) Rearrange components and/or traces
2) Increase the size of the board and space out components
3) Adjust silkscreen on device packages or create package variants
4) Add restricted zones to the board and re-run auto-route

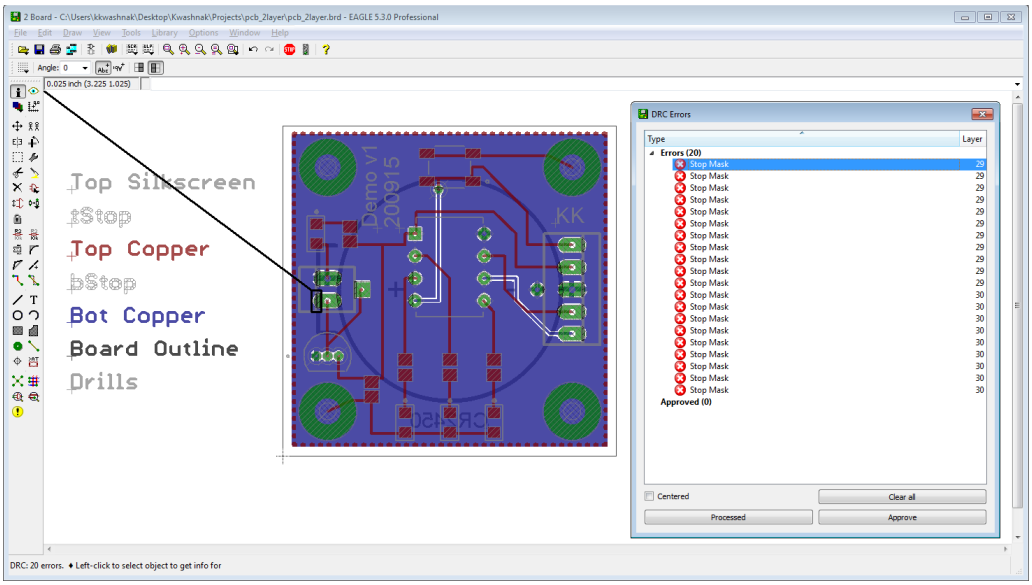


Fig. 184 DRC errors

Creating a variant to a device requires using the <Cut> and <Paste> tools. First, open the original device from the Library Editor, then use the <Group> tool to highlight the entire object, and finally use the <Cut> tool to add the object to EAGLE's clipboard buffer (Fig. 185).

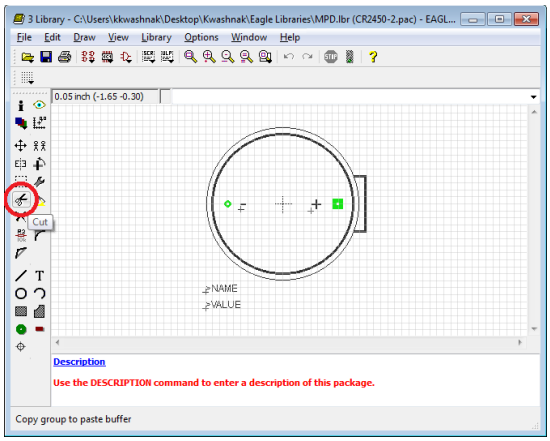


Fig. 185 <Cut> tool

Create a new package (Fig. 186).

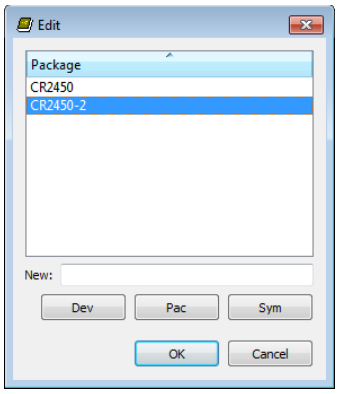


Fig. 186 Create a new package

Paste object using the <Paste> tool (Fig. 187).

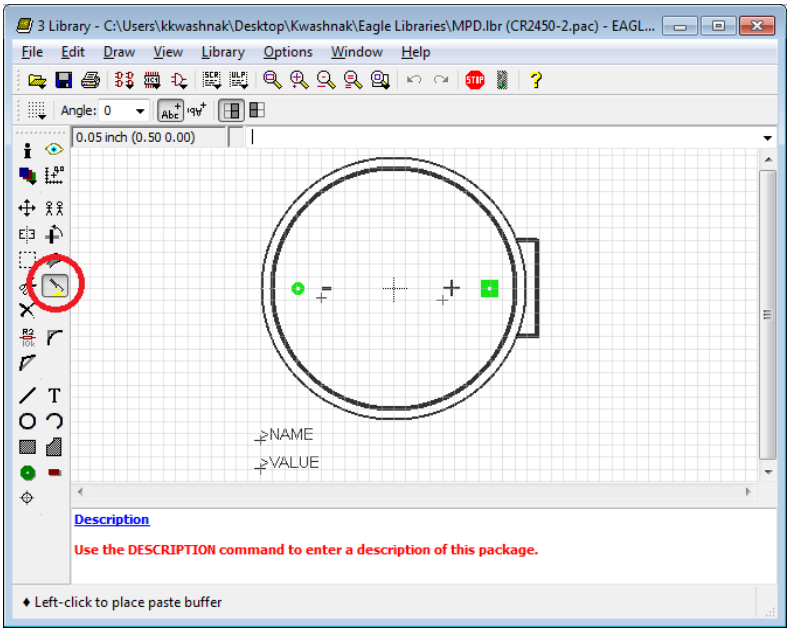


Fig. 187 <Paste> tool

Edit the component. To overcome the error, the silkscreen circle's outline was reduced to a smaller diameter. Notice the original diameter interfered with the power input header. If the circle diameter is too small, it may now interfere with the through-holes from the microcontroller.

After editing the duplicate symbol, open the original device. Click <New> associated with the updated symbol (Fig. 188).

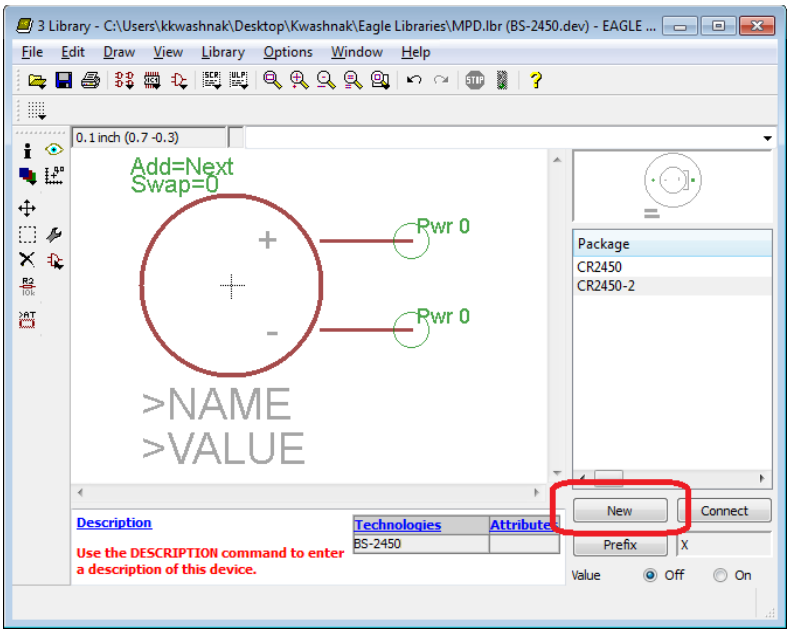


Fig. 188 Device management

Enter a variant name and click <OK> (Fig. 189).

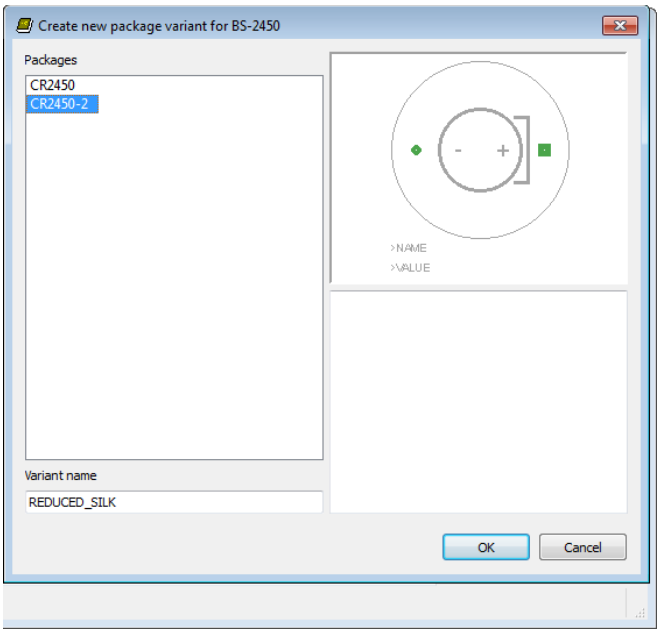


Fig. 189 Variant name

Go to <Connect> and configure the pins (Fig. 190).

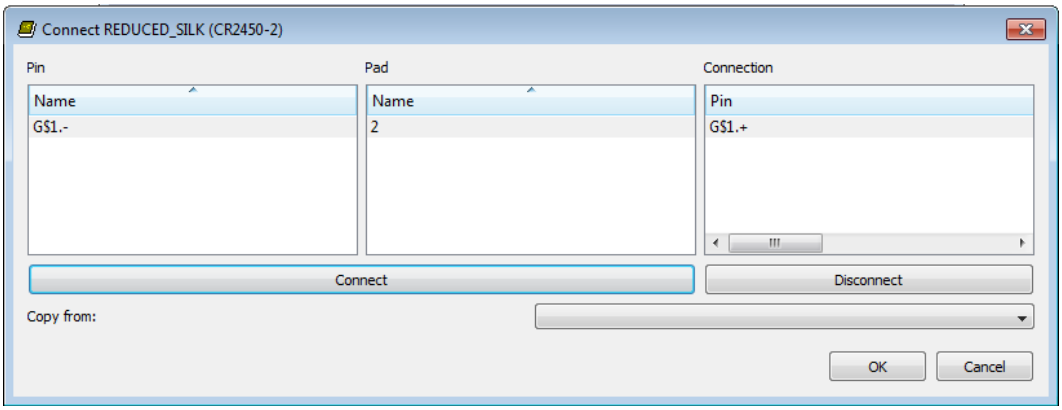


Fig. 190 Configure pins

New symbol is ready for use. Return to the Schematic Editor and use the <Delete> tool to remove the original BS-2450 object. <Add> the updated variant. Switch to the Board Editor and rearrange the object. Use the <Ratsnest> to update the copper pours and airwires. Re-run the <Auto> auto-router. Afterward, check the DRC again and configure the rest of the errors (Fig. 191).

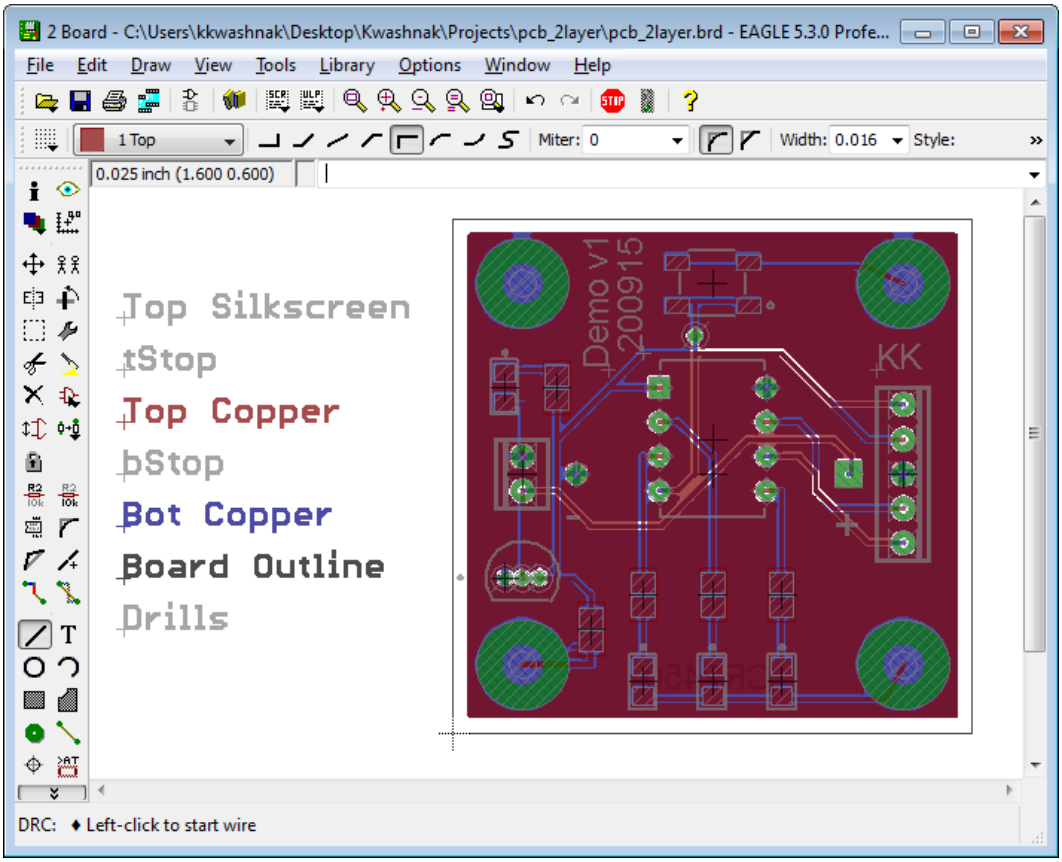


Fig. 191 Final board

4.15 Step 15: Create Fabrication Files

4.15.1 Creating the Drill List .drl

To start creating the fabrication files, such as drill information, navigate to ‘File’ >> ‘Run’ >> ‘Drillcfg.ulp’, and select <Open> (Figs. 192 and 193).

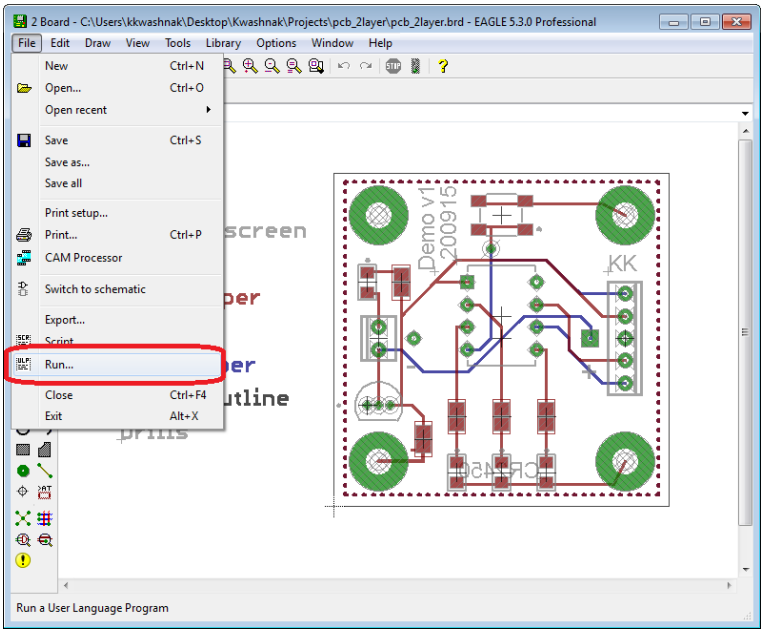


Fig. 192 <Run> ULP option

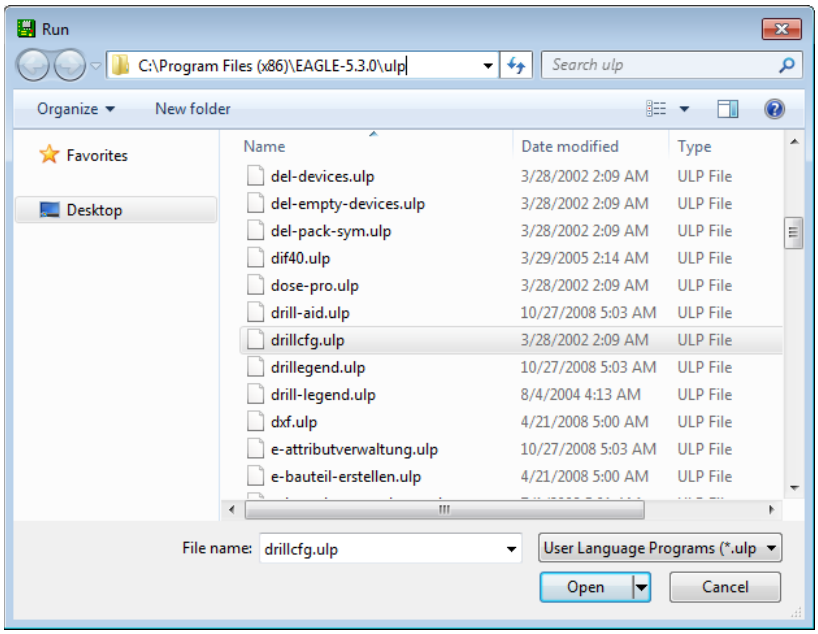


Fig. 193 drillcfg.ulp

When prompted for output units, select either <inch> or <mm> (Fig. 194).

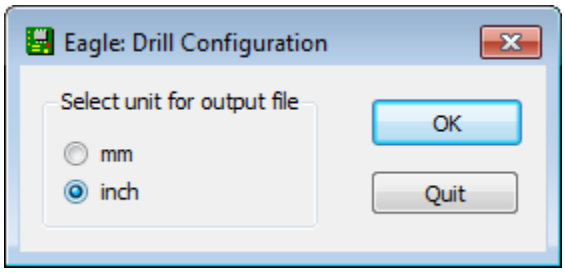


Fig. 194 Unit select

Review and edit drill sizes. Minimizing tool changes may save on the total board cost.

Notice in Fig. 195, "T02 0.031in" is pretty close in diameter to "T03 0.039". It is possible to configure either of those lines to a similar drill size, but double-check that the part used will be able to handle the change. Click on <Ok> to proceed and save the file in a new folder, called "Fab":

C:\Users\kkwashnak\Desktop\Kwashnak\Projects\pcb_2layer\Fab\pcb_2layer.drl

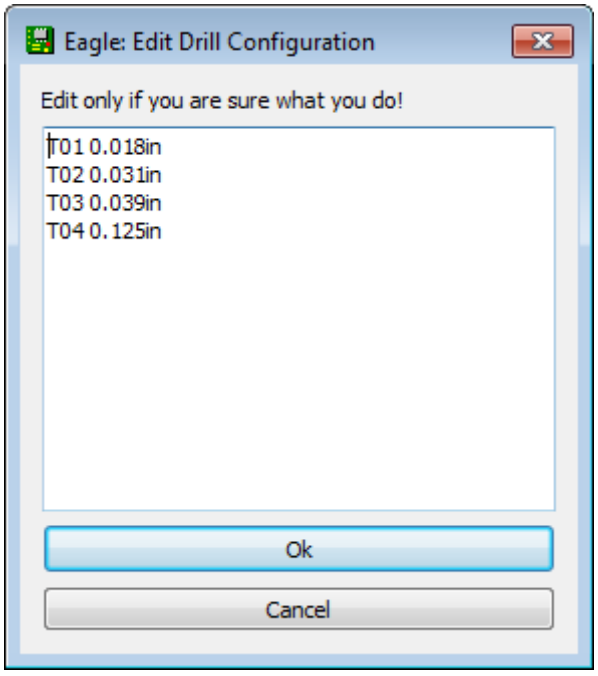


Fig. 195 Board drill sizes

4.15.2 Creating Drill Location Information .drd and .dri

Navigate to ‘File’, ‘CAM Processor’ (Fig. 196).

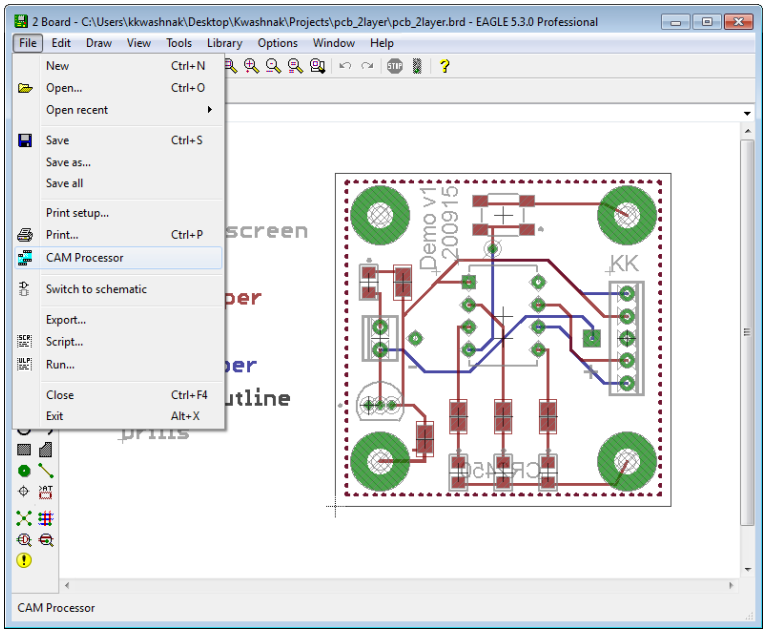


Fig. 196 CAM processor

Inside CAM Processor window, navigate to ‘File’, ‘Open’, ‘Job’ (Fig. 197).

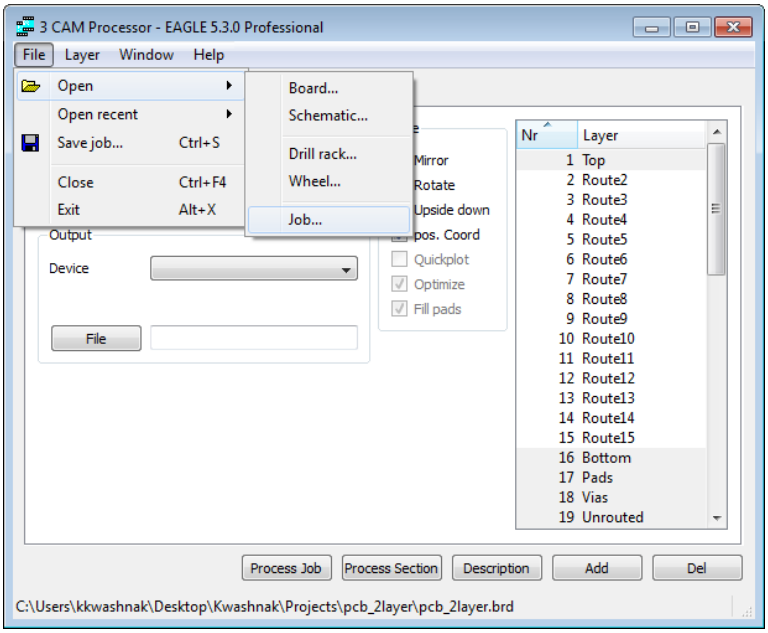


Fig. 197 CAM job

Select the ‘excellon.cam’ file and click on <Open> (Fig. 198).

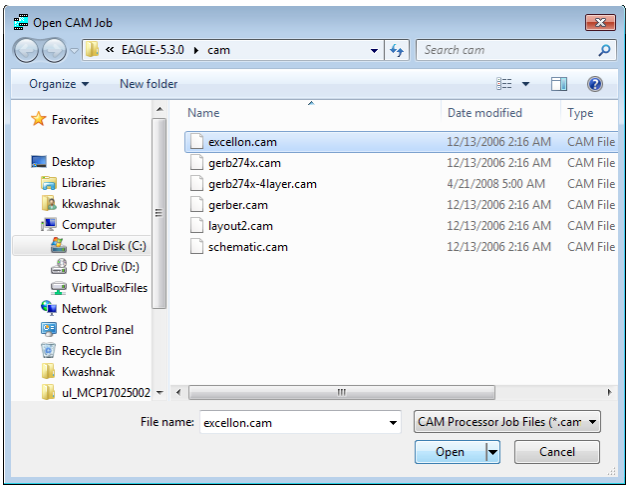


Fig. 198 excellon.cam

The CAM Processor will open with a configured “Generate drill data” tab (Fig. 199). Configure section as follows:

1) ‘Section’ “Generate drill data”.

2) ‘Style’ Check ‘pos. Coord.’ and ‘Optimize’. Fill pads will be checked, but grayed out.

3) ‘Layer’ Select layers ‘44 Drills’ and ‘45 Holes’ only.

4) ‘Device’ EXCELLON

5) ‘File’ “%N.dhd”, (notation indicates filename-drill hole data), click on <File> and save in “Fab” folder (Fig. 200).

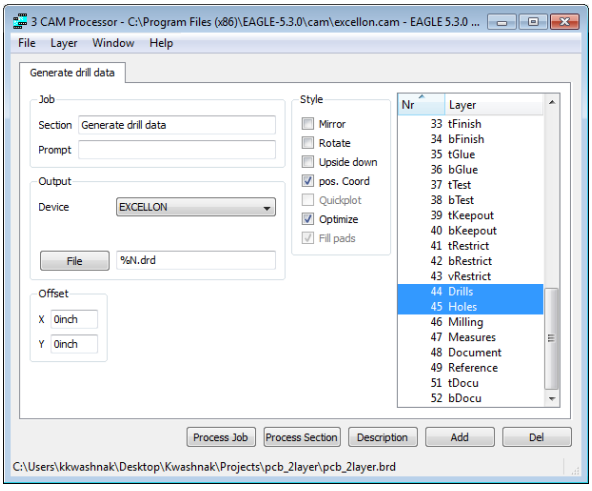


Fig. 199 Generate drill data

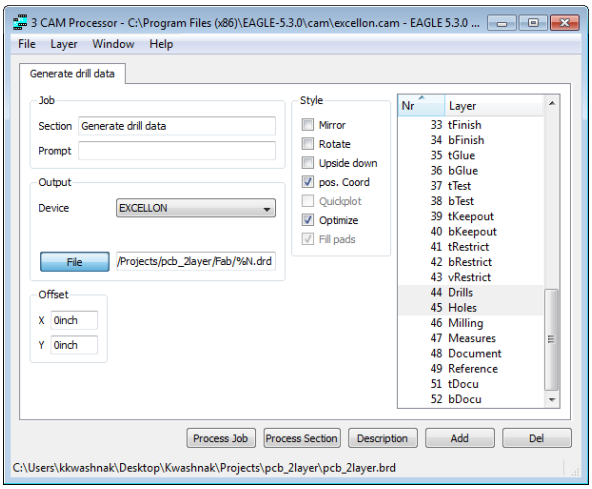


Fig. 200 Configuring file save location

Click on <Process Job> and review “Fab” folder (Fig. 201). The folder is populated with the .drd and .dri files (Fig. 202).

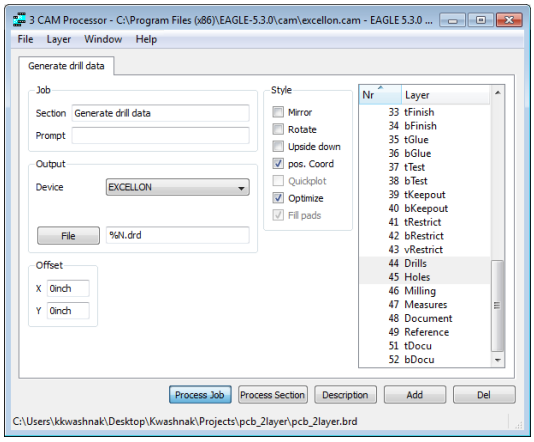


Fig. 201 Process job generate drill data

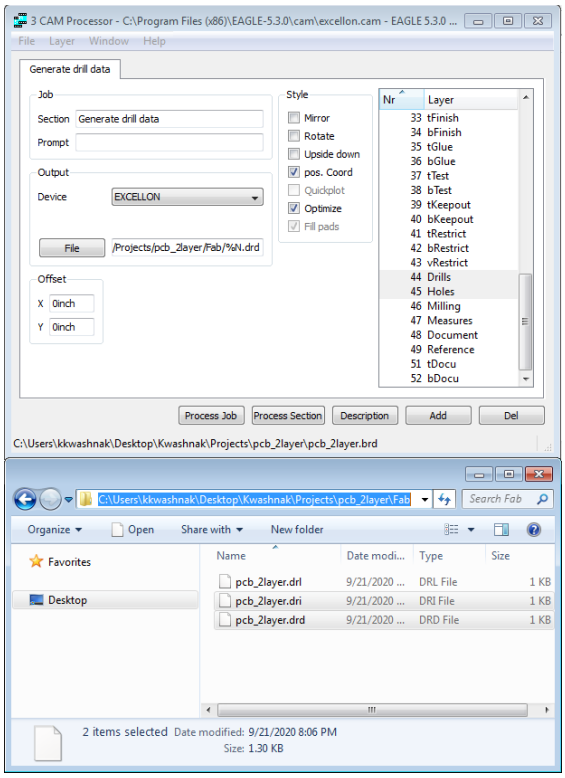


Fig. 202 Creation of drd and dri files

When exiting the CAM Job, EAGLE prompts to save the job. Create a new folder named “Jobs” in the “pcb_2layer” project folder and save the updated excellon.cam:

C:\Users\kkwashnak\Desktop\Kwashnak\Projects\pcb_2layer\Jobs\excellon.cam

4.15.3 Creating Layer Information (Gerber274x.cam or Custom)

Open CAM Processor, ‘File’, ‘Open’, ‘Job’, ‘gerb274x.cam’ and click on <Open>.

The directory may have updated due to the previous .cam file save. Check the default install directory for the original cam files (Fig. 203), such as

C:\Program Files (x86)\EAGLE-5.3.0\cam

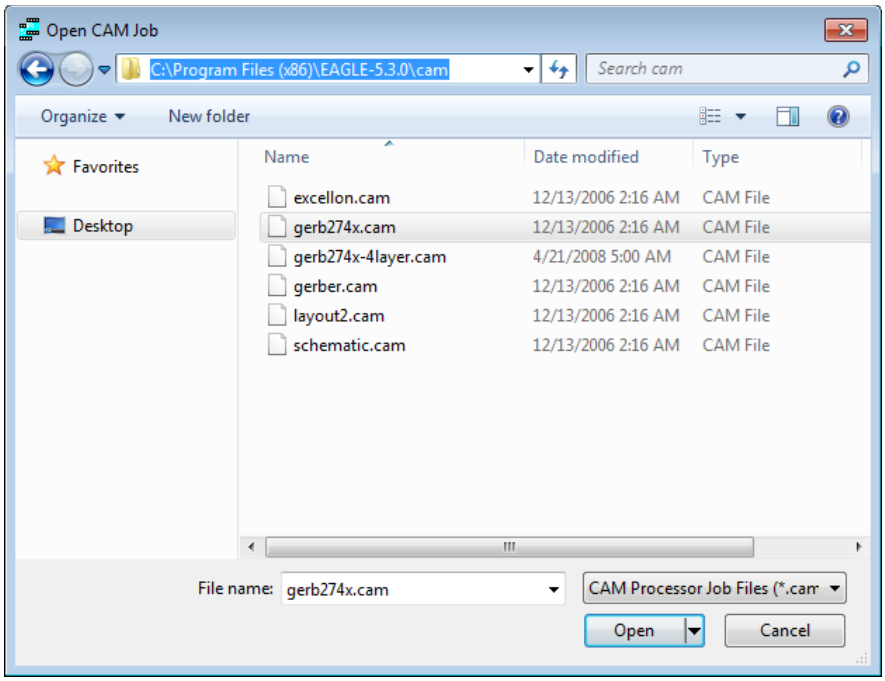


Fig. 203 gerb274x.cam

The default standard will have multiple sections, such as ‘Component side’, ‘Solder side’, Silk screen CMP’, and so on. These sections will be altered for the custom two-layer PCB. When a section tab is selected, click on the <Del> button to remove the page and <Add> to insert a new page.

Section details are described in the following modules.

4.15.3.1 Top Silkscreen .tslk

The Top Silkscreen section instructions are as follows (Fig. 204):

1) 'Section' "Top Silkscreen"
2) 'Style' Check 'pos. Coord.' and 'Optimize'. Fill pads will be checked, but grayed out.
3) 'Layer' Select layer '21 tPlace' and '25 tNames'.
4) 'Device' GERBER_RS274X
5) 'File' "%N.tslk", click on <File> and save in "Fab" folder.

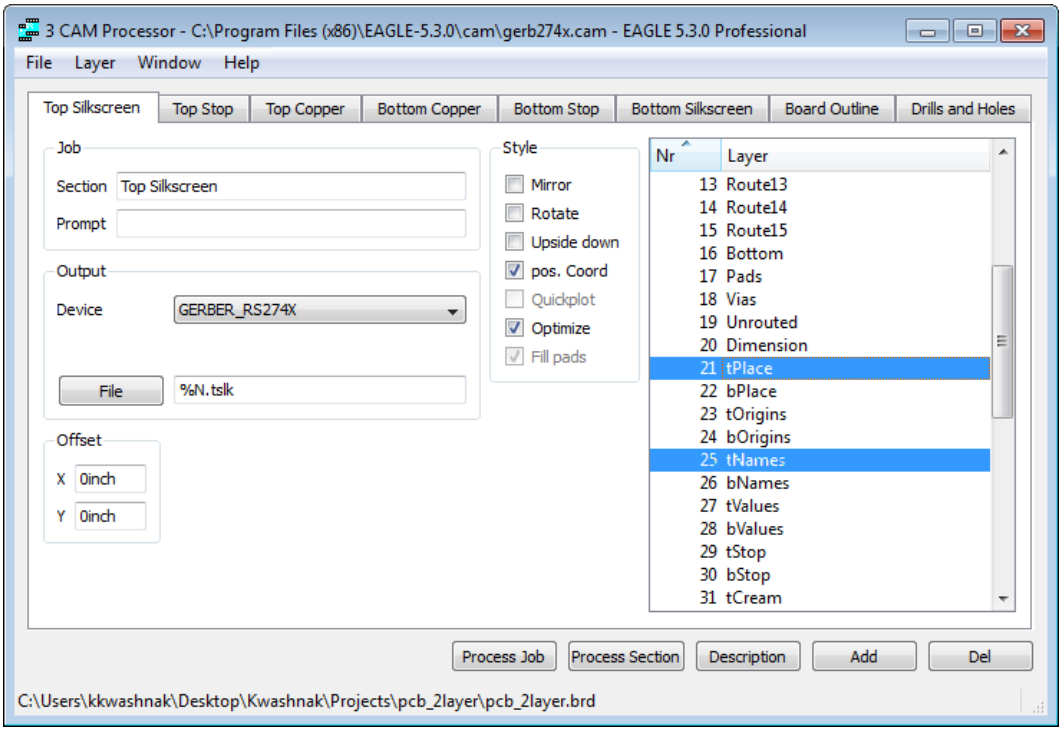


Fig. 204 Gerber_RS274X top silkscreen section

4.15.3.2 Top Stop .tstp

The Top Stop section instructions are as follows (Fig. 205):

1) ‘Section’ “Top Stop”
2) ‘Style’ Check ‘pos. Coord.’ and ‘Optimize’. Fill pads will be checked, but grayed out.
3) ‘Layer’ Select layer ‘29 tStop’.
4) ‘Device’ GERBER_RS274X
5) ‘File’ “%N.tstp”, click on <File> and save in “Fab” folder.

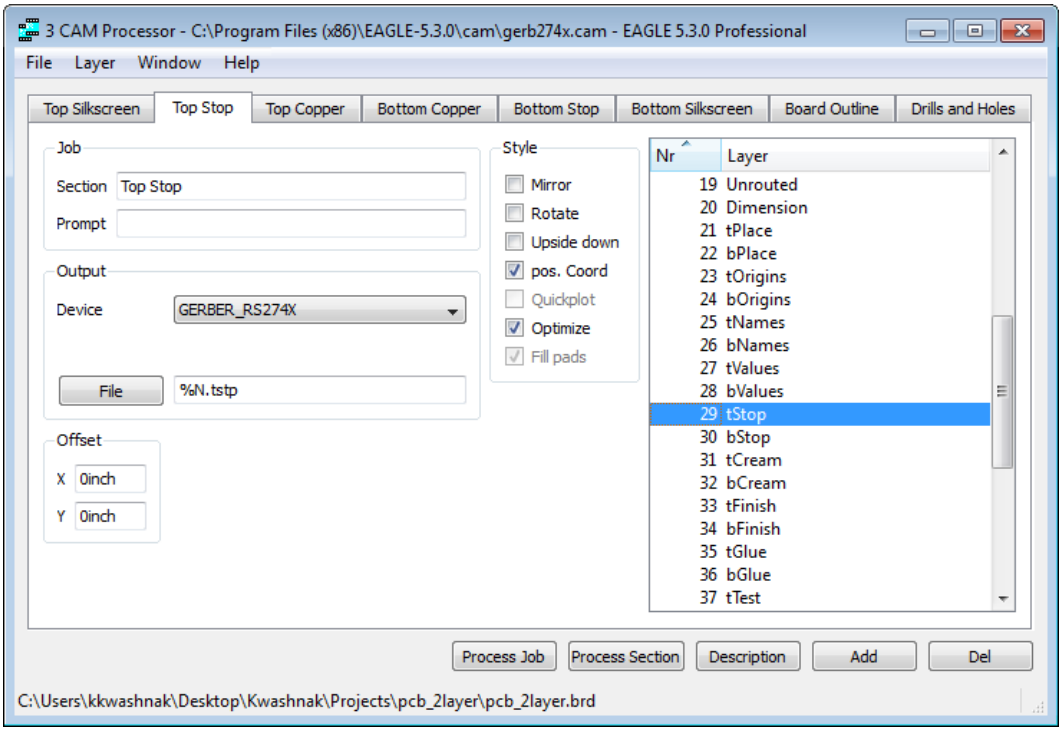


Fig. 205 Gerber_RS274X top stop section

4.15.3.3 Top Copper .tcpr

The Top Copper section instructions are as follows (Fig. 206):

1) 'Section' "Top Copper"
2) 'Style' Check 'pos. Coord.' and 'Optimize'. Fill pads will be checked, but grayed out.
3) 'Layer' Select layers '1 Top', '17 Pads', and '18 Vias'.
4) 'Device' GERBER_RS274X
5) 'File' "%N.tcpr", click on <File> and save in "Fab" folder.

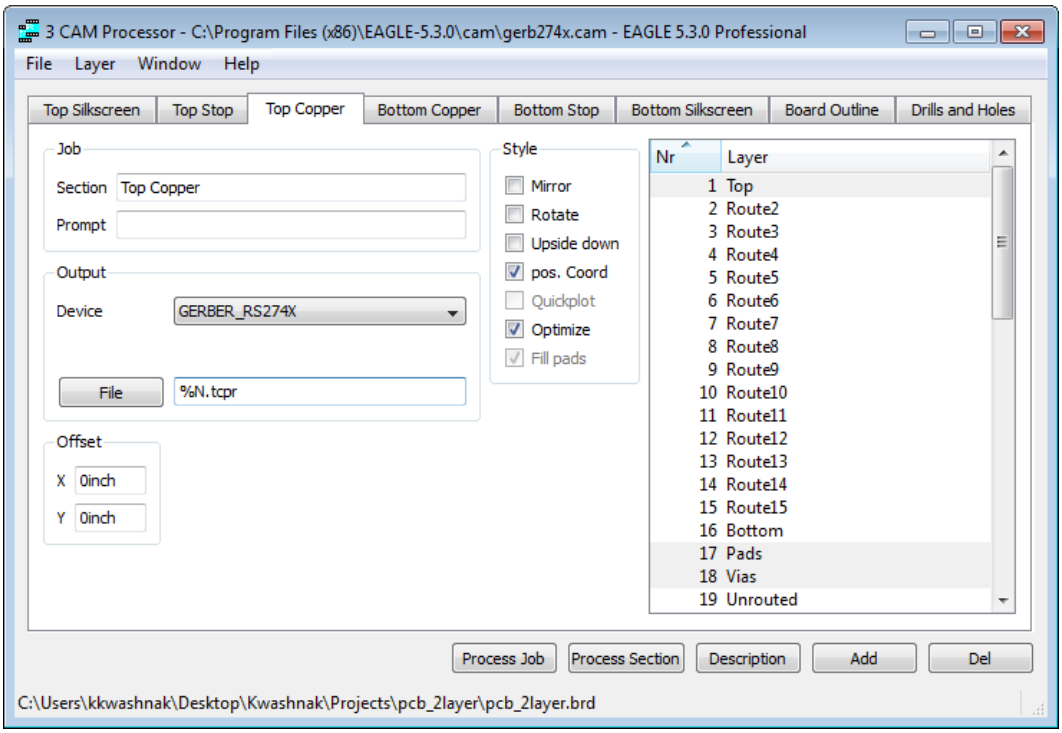


Fig. 206 Gerber_RS274X top copper section

4.15.3.4 Bottom Copper .bcpr

The Bottom Copper section instructions are as follows (Fig. 207):

1) 'Section' "Bottom Copper"
2) 'Style' Check 'pos. Coord.' and 'Optimize'. Fill pads will be checked, but grayed out.
3) 'Layer' Select layers '16 Bottom', '17 Pads', and '18 Vias'.
4) 'Device' GERBER_RS274X
5) 'File' "%N.bcpr", click on <File> and save in "Fab" folder.

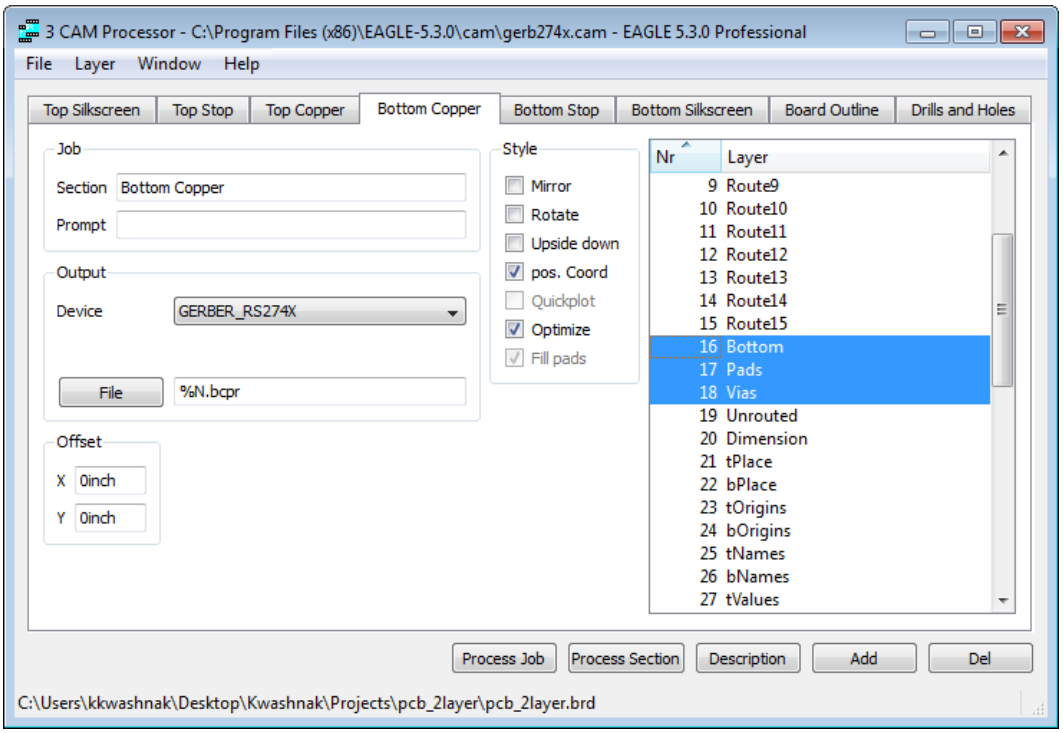


Fig. 207 Gerber_RS274X bottom copper section

4.15.3.5 Bottom Stop .bstp

The Bottom Stop section instructions are as follows (Fig. 208):

1) ‘Section’ “Bottom Stop”
2) ‘Style’ Check ‘pos. Coord.’ and ‘Optimize’. Fill pads will be checked, but grayed out.
3) ‘Layer’ Select layer ‘30 bStop’.
4) ‘Device’ GERBER_RS274X
5) ‘File’ “%N.bstp”, click on <File> and save in “Fab” folder.

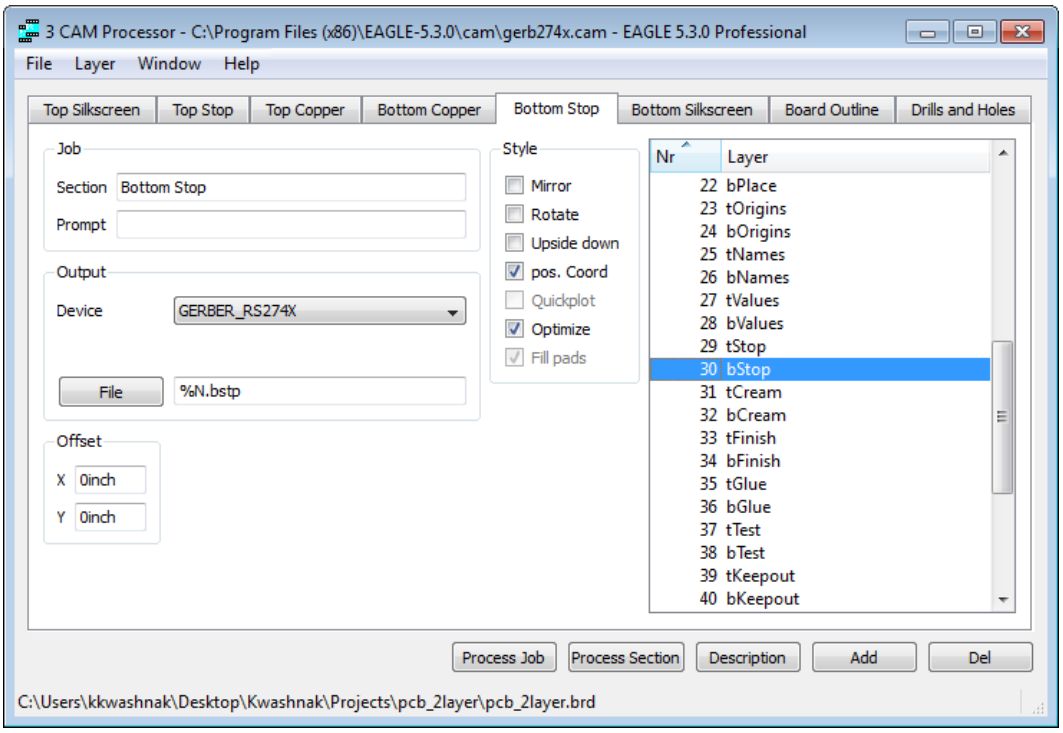


Fig. 208 Gerber_RS274X bottom stop section

4.15.3.6 Bottom Silkscreen .bslk

The Bottom Silkscreen section instructions are as follows (Fig. 209):

1) 'Section' "Bottom Silkscreen"
2) 'Style' Check 'pos. Coord.' and 'Optimize'. Fill pads will be checked, but grayed out.
3) 'Layer' Select layer '22 bPlace'.
4) 'Device' GERBER_RS274X
5) 'File' "%N.bslk", click on <File> and save in "Fab" folder.

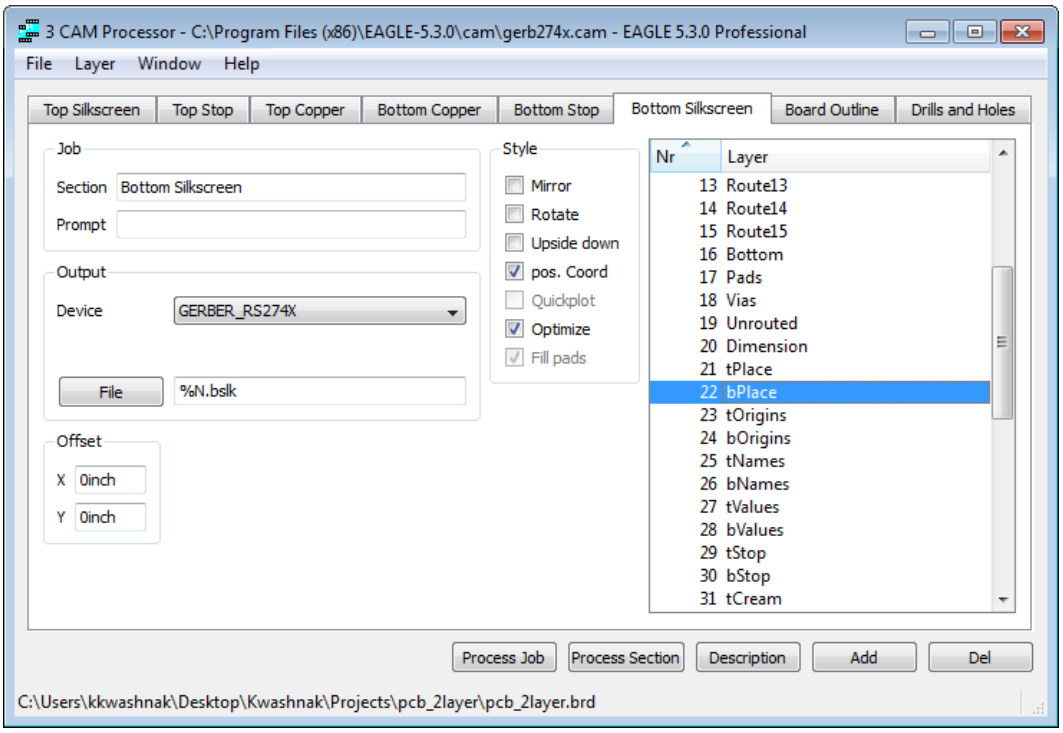


Fig. 209 Gerber_RS274X bottom silkscreen section

4.15.3.7 Board Outline .dout

The Board Outline section instructions are as follows (Fig. 210):

1) ‘Section’ “Board Outline”
2) ‘Style’ Check ‘pos. Coord.’ and ‘Optimize’. Fill pads will bechecked, but grayed out.
3) ‘Layer’ Select layer ‘20 Dimension’.
4) ‘Device’ GERBER_RS274X
5) ‘File’ “%N.dout”, click on <File> and save in “Fab” folder.

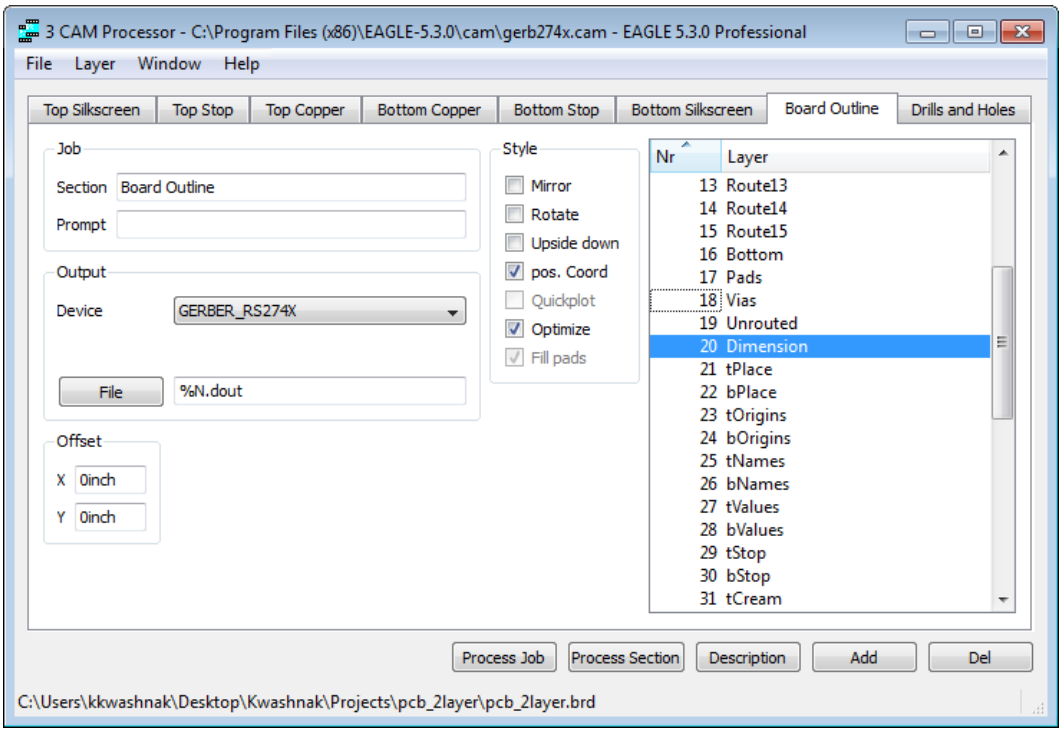


Fig. 210 Gerber_RS274X board outline section

4.15.3.8 Drills and Holes .ddrl

The Drills and Holes section instructions are as follows (Fig. 211):

1) ‘Section’ “Drills and Holes”
2) ‘Style’ Check ‘pos. Coord.’ and ‘Optimize’. Fill pads will be checked, but grayed out.
3) ‘Layer’ Select layers ‘44 Drills’ and ‘45 Holes’.
4) ‘Device’ GERBER_RS274X
5) ‘File’ “%N.ddrl”, click on <File> and save in “Fab” folder.

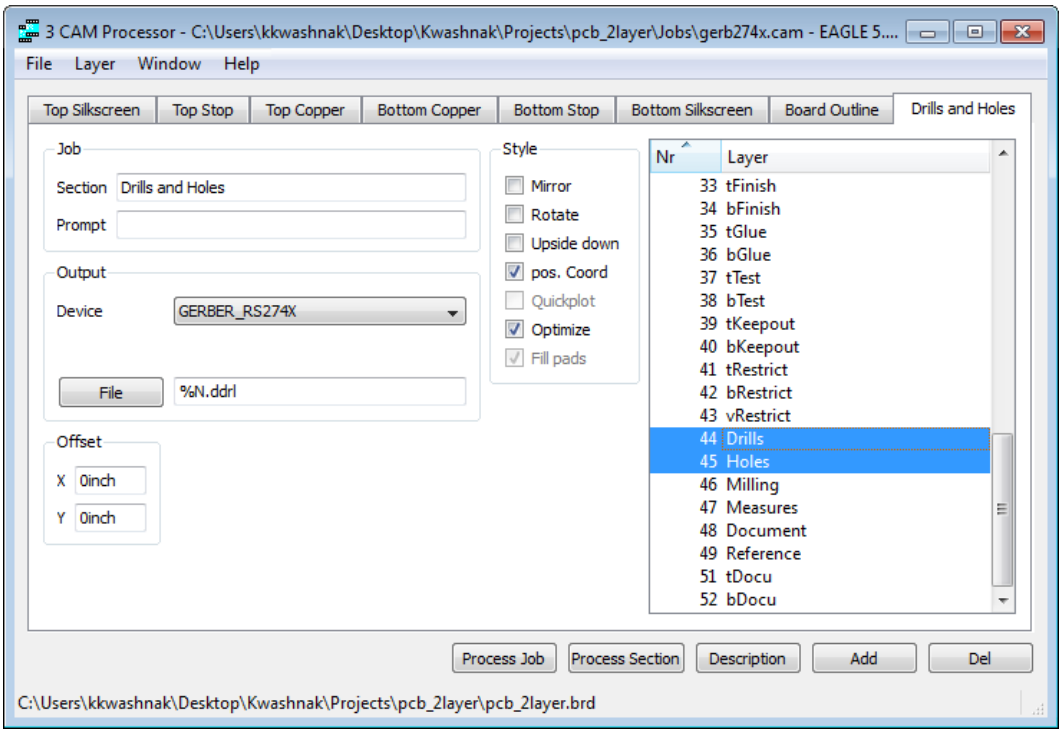


Fig. 211 Gerber_RS274X drills and holes section

4.15.3.9 Description

The description (Fig. 212) of the custom Gerber_274x cam file provides information (Fig. 213) to the manufacturer about how to handle the Gerber files.

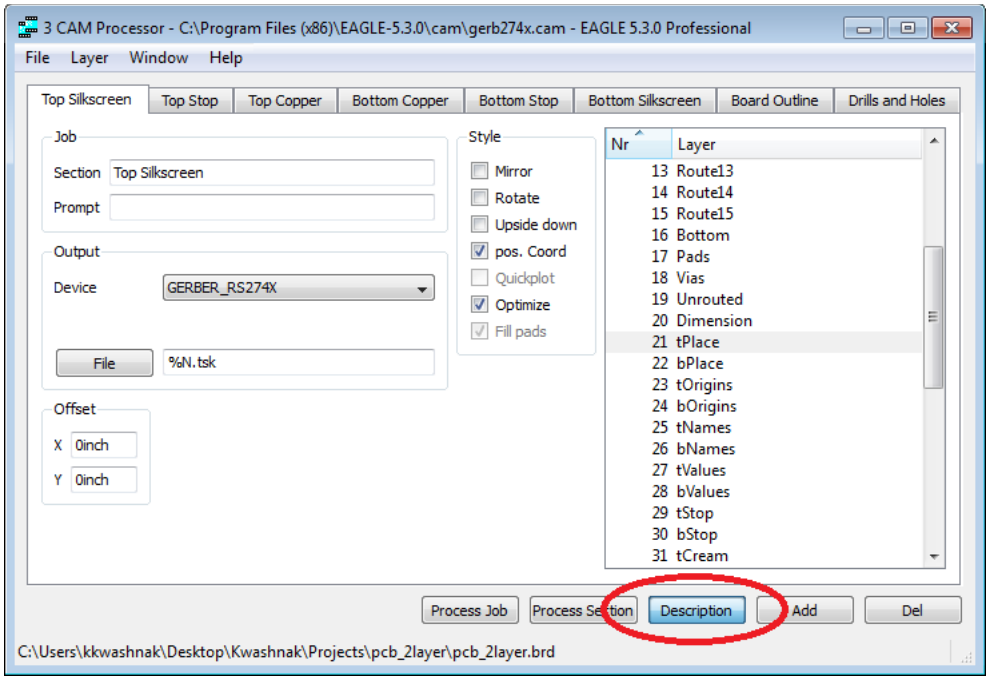


Fig. 212 Gerber_274X description section

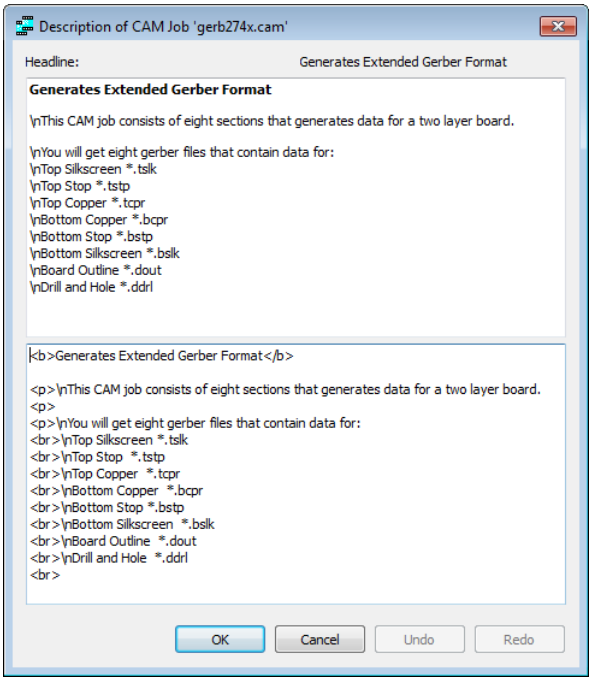


Fig. 213 Gerber_274X description information

```
<b>Generates Extended Gerber Format</b>
<p>\nThis CAM job consists of eight sections that generate data for a two layer board.
<p>
<p>\nYou will get eight gerber files that contain data for:
<br>\nTop Silkscreen *.tslk
<br>\nTop Stop *.tstp
<br>\nTop Copper *.tcpr
<br>\nBottom Copper *.bcpr
<br>\nBottom Stop *.bstp
<br>\nBottom Silkscreen *.bslk
<br>\nBoard Outline *.dout
<br>\nDrill and Hole *.ddrl
<br>
```

Code block 1 HTML gerber_274X description

Finally, navigate to <File> >> <Save Job>, and save the CAM file in the Jobs folder (Fig. 214):

C:\Users\kkwashnak\Desktop\Kwashnak\Projects\pcb_2layer\Jobs\gerb274x.cam

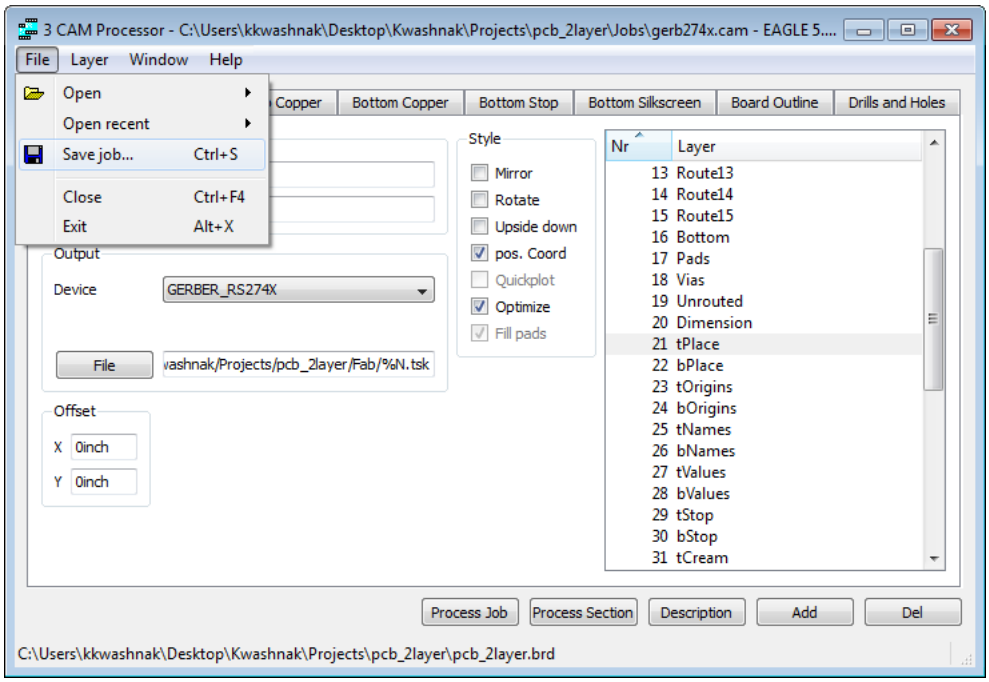


Fig. 214 Save Gerber_274X job

Click on <Process Job> (Fig. 215).

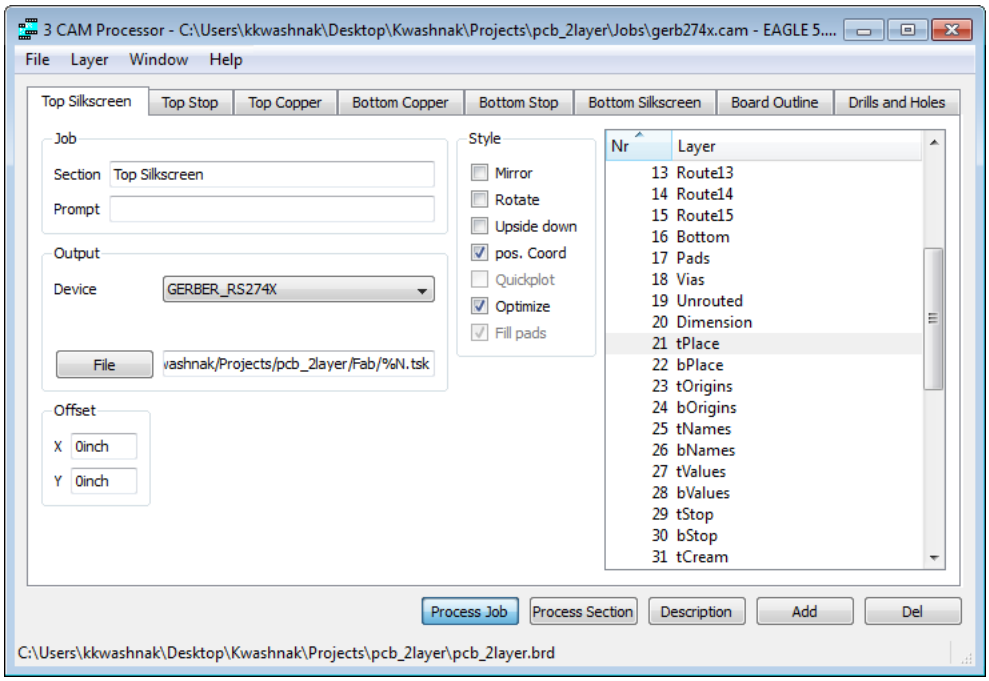


Fig. 215 Processing Gerber files

Review all files in Windows Explorer (Fig. 216).

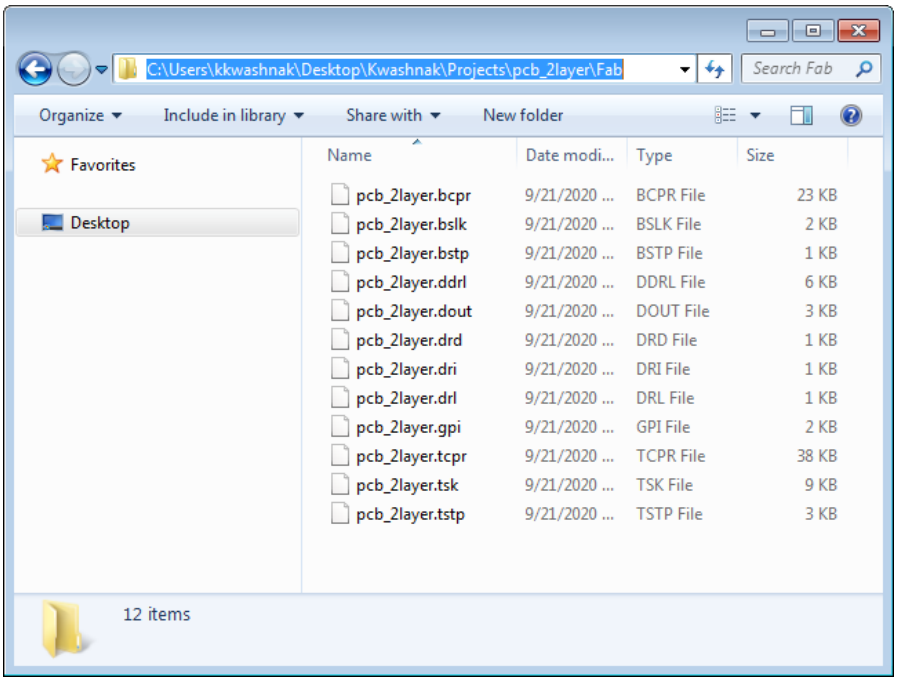


Fig. 216 Gerber files complete

4.15.3.10 excellon.cam

File contents of the excellon.cam are stated in code block 2.

```
[CAM Processor Job]
Description[de]="<b>Erzeugt Bohrdaten im Excellon-Format</b><p>\nDieser CAM-Job kann
verwendet werden, um Bohrdaten im Excellon-Format für numerisch gesteuerte Bohrmaschinen
zu erzeugen.<p><p>\nDer EXCELLON-Treiber erzeugt eine Bohrdatendatei, die bereits
die\nBohrertabelle im Dateikopf enthält."
Description[en]="<b>Generates Excellon Drill Data </b><p>\nThis CAM job can be used to
generate data for drilling machines in Excellon format.<p><p>\nThe EXCELLON device
generates a drill data file which contains the drill table in the header of the file.\n"
Section=Sec_1

[Sec_1]
Name[de]="Bohrdaten erzeugen"
Name[en]="Generate drill data"
Prompt[en]=""
Device="EXCELLON"
Wheel=".whl"
Rack=""
Scale=1
Output="C:/Users/kkwashnak/Desktop/Kwashnak/Projects/pcb_2layer/Fab/%N.drd"
Flags="0 0 0 1 0 1 1"
Emulate="0 0 0"
Offset="0.0mil 0.0mil"
Sheet=1
Tolerance="0 0 0 0 0.025 0.025"
Pen="0.0mil 0"
Page="12000.0mil 8000.0mil"
Layers=" 44 45"
Colors=" 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 6 6 4 8 8 8 8 8 8 8 8 8 8 8 8 8 4 4 1 1 1 1 3 3
1 2 6 8 8 5 8 8 8 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 4 2 4 3 6 6 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0"
```

Code block 2 Custom CAM job for Excellon file

4.15.3.11 gerb274x.cam

File contents of gerb274x.cam are stated in code block 3.

```
[CAM Processor Job]
Description[de]="<b>Erzeugt Extended-Gerber-Format (RS274X)</b><p>\nDieser CAM-Job
besteht aus fünf Arbeitsschritten und erzeugt Fertigungsdaten für eine zweilagige
Platine.<p><p>\nDie fünf Gerberdateien enthalten Daten für:<br>\nBestückungsseite
*.cmp<br>\nLötseite *.sol<br>\nBestückungsdruck oben *.plc<br>\nLötstoplack
Bestückungsseite *.stc<br>\nLötstoplack Lötseite *.sts<br>"
Description[en]="<b>Generates Extended Gerber Format</b>\n\n<p>\nThis CAM job consists
of eight sections that generates data for a two layer board.\n<p>\n<p>\nYou will get
eight gerber files that contain data for:\n<br>\nTop Silkscreen *.tslk\n<br>\nTop Stop
*.tstp\n<br>\nTop Copper *.tcpr\n<br>\nBottom Copper *.bcpr\n<br>\nBottom Stop
*.bstp\n<br>\nBottom Silkscreen *.bslk\n<br>\nBoard Outline *.dout\n<br>\nDrill and
Hole *.ddrl\n<br>"
Section=Sec_1
Section=Sec_2
Section=Sec_3
Section=Sec_4
Section=Sec_5
Section=Sec_6
Section=Sec_7
Section=Sec_8
```

```
[Sec_1]
Name[de]="Bestückungsseite"
Name[en]="Top Silkscreen"
Prompt[en]=""
Device="GERBER_RS274X"
Wheel=".whl"
Rack=""
Scale=1
Output="C:/Users/kkwashnak/Desktop/Kwashnak/Projects/pcb_2layer/Fab/%N.tsk"
Flags="0 0 0 1 0 1 1"
Emulate="0 0 0"
Offset="0.0mil 0.0mil"
Sheet=1
Tolerance="0 0 0 0 0 0"
Pen="0.0mil 0"
Page="12000.0mil 8000.0mil"
Layers=" 21"
Colors=" 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 6 6 4 8 8 8 8 8 8 8 8 8 8 8 8 4 4 1 1 1 1 3 3
1 2 6 8 8 5 8 8 8 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 4 2 4 3 6 6 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0"

[Sec_2]
Name[de]="Bestückungsseite"
Name[en]="Top Stop"
Prompt[en]=""
Device="GERBER_RS274X"
Wheel=".whl"
Rack=""
Scale=1
Output="C:/Users/kkwashnak/Desktop/Kwashnak/Projects/pcb_2layer/Fab/%N.tstp"
Flags="0 0 0 1 0 1 1"
Emulate="0 0 0"
Offset="0.0mil 0.0mil"
Sheet=1
Tolerance="0 0 0 0 0 0"
Pen="0.0mil 0"
Page="12000.0mil 8000.0mil"
Layers=" 29"
Colors=" 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 6 6 4 8 8 8 8 8 8 8 8 8 8 8 8 4 4 1 1 1 1 3 3
1 2 6 8 8 5 8 8 8 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 4 2 4 3 6 6 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0"

[Sec_3]
Name[de]="Bestückungsseite"
Name[en]="Top Copper"
Prompt[en]=""
Device="GERBER_RS274X"
Wheel=".whl"
Rack=""
Scale=1
Output="C:/Users/kkwashnak/Desktop/Kwashnak/Projects/pcb_2layer/Fab/%N.tcpr"
Flags="0 0 0 1 0 1 1"
Emulate="0 0 0"
Offset="0.0mil 0.0mil"
Sheet=1
Tolerance="0 0 0 0 0 0"
Pen="0.0mil 0"
Page="12000.0mil 8000.0mil"
Layers=" 1 17 18"
Colors=" 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 6 6 4 8 8 8 8 8 8 8 8 8 8 8 8 4 4 1 1 1 1 3 3
1 2 6 8 8 5 8 8 8 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 4 2 4 3 6 6 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
```

```
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0"

[Sec_4]
Name[de]="Bestückungsseite"
Name[en]="Bottom Copper"
Prompt[en]=""
Device="GERBER_RS274X"
Wheel=".whl"
Rack=""
Scale=1
Output="C:/Users/kkwashnak/Desktop/Kwashnak/Projects/pcb_2layer/Fab/%N.bcpr"
Flags="0 0 0 1 0 1 1"
Emulate="0 0 0"
Offset="0.0mil 0.0mil"
Sheet=1
Tolerance="0 0 0 0 0 0"
Pen="0.0mil 0"
Page="12000.0mil 8000.0mil"
Layers=" 16 17 18"
Colors=" 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 6 6 4 8 8 8 8 8 8 8 8 8 8 8 8 8 4 4 1 1 1 1 3 3
1 2 6 8 8 5 8 8 8 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 4 2 4 3 6 6 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0"

[Sec_5]
Name[de]="Bestückungsseite"
Name[en]="Bottom Stop"
Prompt[en]=""
Device="GERBER_RS274X"
Wheel=".whl"
Rack=""
Scale=1
Output="C:/Users/kkwashnak/Desktop/Kwashnak/Projects/pcb_2layer/Fab/%N.bstp"
Flags="0 0 0 1 0 1 1"
Emulate="0 0 0"
Offset="0.0mil 0.0mil"
Sheet=1
Tolerance="0 0 0 0 0 0"
Pen="0.0mil 0"
Page="12000.0mil 8000.0mil"
Layers=" 30"
Colors=" 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 6 6 4 8 8 8 8 8 8 8 8 8 8 8 8 8 4 4 1 1 1 1 3 3
1 2 6 8 8 5 8 8 8 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 4 2 4 3 6 6 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0"

[Sec_6]
Name[de]="Bestückungsseite"
Name[en]="Bottom Silkscreen"
Prompt[en]=""
Device="GERBER_RS274X"
Wheel=".whl"
Rack=""
Scale=1
Output="C:/Users/kkwashnak/Desktop/Kwashnak/Projects/pcb_2layer/Fab/%N.bslk"
Flags="0 0 0 1 0 1 1"
Emulate="0 0 0"
Offset="0.0mil 0.0mil"
Sheet=1
Tolerance="0 0 0 0 0 0"
Pen="0.0mil 0"
Page="12000.0mil 8000.0mil"
Layers=" 22"
```

```
Colors=" 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 6 6 4 8 8 8 8 8 8 8 8 8 8 8 8 8 4 4 1 1 1 1 3 3
1 2 6 8 8 5 8 8 8 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 4 2 4 3 6 6 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0"

[Sec_7]
Name[de]="Bestückungsseite"
Name[en]="Board Outline"
Prompt[en]=""
Device="GERBER_RS274X"
Wheel=".whl"
Rack=""
Scale=1
Output="C:/Users/kkwashnak/Desktop/Kwashnak/Projects/pcb_2layer/Fab/%N.dout"
Flags="0 0 0 1 0 1 1"
Emulate="0 0 0"
Offset="0.0mil 0.0mil"
Sheet=1
Tolerance="0 0 0 0 0 0"
Pen="0.0mil 0"
Page="12000.0mil 8000.0mil"
Layers=" 20"
Colors=" 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 6 6 4 8 8 8 8 8 8 8 8 8 8 8 8 8 4 4 1 1 1 1 3 3
1 2 6 8 8 5 8 8 8 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 4 2 4 3 6 6 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0"

[Sec_8]
Name[de]="Bestückungsseite"
Name[en]="Drills and Holes"
Prompt[en]=""
Device="GERBER_RS274X"
Wheel=".whl"
Rack=""
Scale=1
Output="C:/Users/kkwashnak/Desktop/Kwashnak/Projects/pcb_2layer/Fab/%N.ddrl"
Flags="0 0 0 1 0 1 1"
Emulate="0 0 0"
Offset="0.0mil 0.0mil"
Sheet=1
Tolerance="0 0 0 0 0 0"
Pen="0.0mil 0"
Page="12000.0mil 8000.0mil"
Layers=" 44 45"
Colors=" 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 6 6 4 8 8 8 8 8 8 8 8 8 8 8 8 8 4 4 1 1 1 1 3 3
1 2 6 8 8 5 8 8 8 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 4 2 4 3 6 6 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0"
```

Code block 3 Custom CAM job for Gerber files

4.16 Step 16: Formulate Board Instructions

Before proceeding to combine all files into one package, such as a compressed file format .zip, a generic instruction sheet must be generated. In the Windows Explorer, navigate to

C:\Users\kkwashnak\Desktop\Kwashnak\Projects\pcb_2layer\Fab

Right-click inside the File Explorer "Fab" folder contents area, hover over 'New', and select 'Text Document' (Fig. 217).

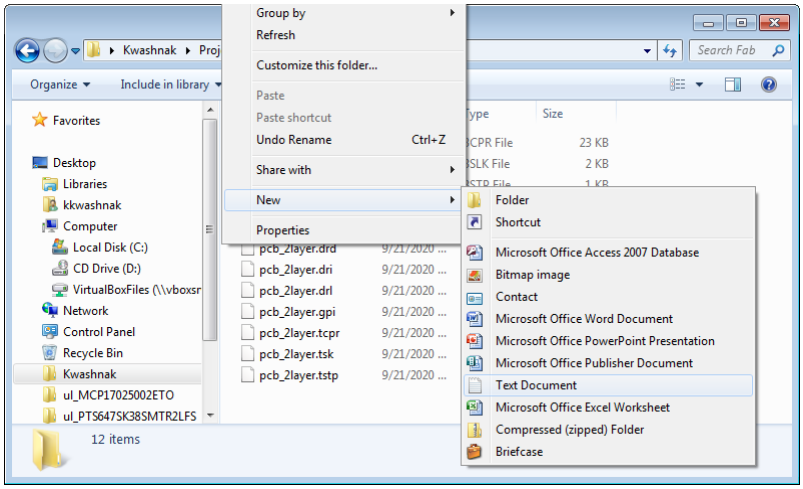


Fig. 217 Creating an instruction file

Name the text file "Instructions" (Fig. 218).

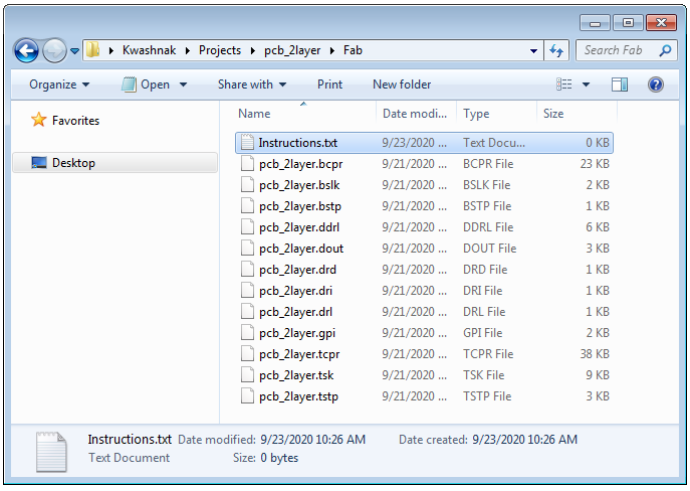


Fig. 218 Instructions text file

Edit the text file with similar contents as shown in code block 4:

```
Author                      Ken Kwashnak
Author Email                ***@***.***
Author Phone                (***)***-****
Date                        September 23, 2020

Board Name                  Demo Board (pcb_2layer)
Board Version               1.0 (baseline)

Board Dimension             1.5" x 1.5" x 0.063"
Board Material              FR4
Copper Weight               1 oz
Lead Free                   Yes
Soldermask                  Both Sides
Soldermask Color            Green
Silkscreen                  Both Sides
Silkscreen Color            White

The attached fabrication files were processed from EAGLE v5.3.0:
- pcb_2layer.drl  (Drill List)
- pcb_2layer.drd  (excellon.cam, Drill Location Information)
- pcb_2layer.dri  (excellon.cam, Drill Location Information)
- pcb_2layer.tslk (Gerber274x.cam, Top Silkscreen)
- pcb_2layer.tstp (Gerber274x.cam, Top Stop)
- pcb_2layer.tcpr (Gerber274x.cam, Top Copper)
- pcb_2layer.bcpr (Gerber274x.cam, Bottom Copper)
- pcb_2layer.bstp (Gerber274x.cam, Bottom Stop)
- pcb_2layer.bslk (Gerber274x.cam, Bottom Silkscreen)
- pcb_2layer.dout (Gerber274x.cam, Board Outline)
- pcb_2layer.ddrl (Gerber274x.cam, Drills and Holes)
- pcb_2layer.gpi  (Gerber274x.cam, Photoplotter)

Additional Notes:
- Plated Through Holes, Sized for No 4 Holes, Quantity 4
```

Code block 4 Instructions file content

4.17 Step 17: Package Files

Packaging the files is very simple in the Windows Explorer. Navigate to the following location (Fig. 219):

C:\Users\kkwashnak\Desktop\Kwashnak\Projects\pcb_2layer

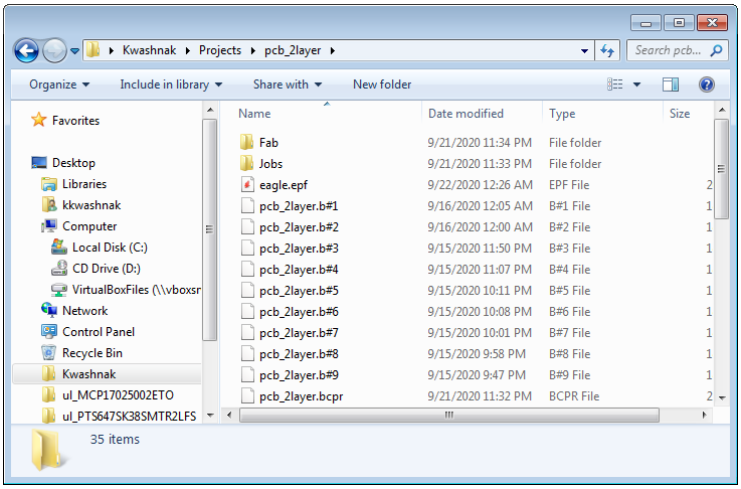


Fig. 219 Fab folder location

Right-click the Fab folder, mouse over <Send to>, and select <Compressed (zipped) folder> (Figs. 220 and 221).

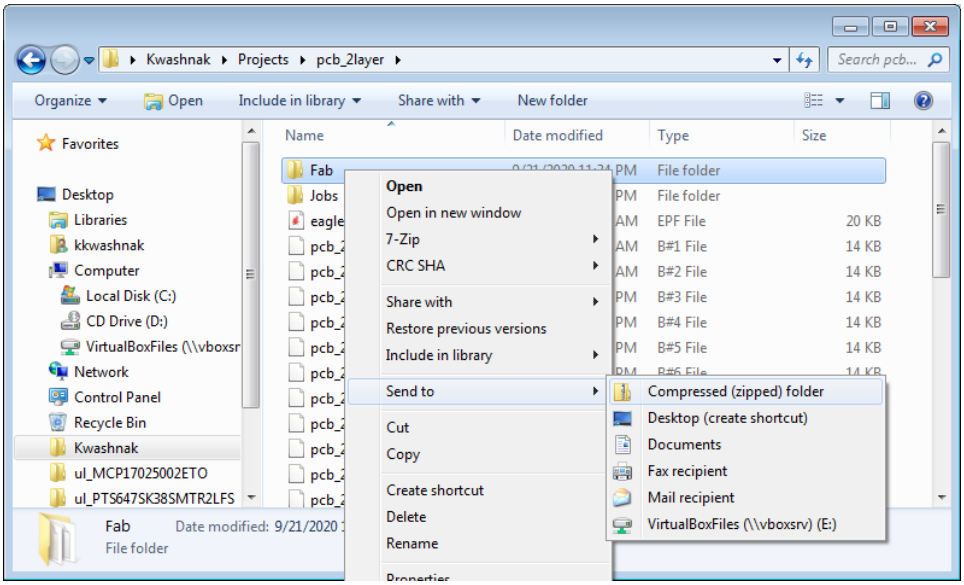


Fig. 220 Compressing to a .zip file

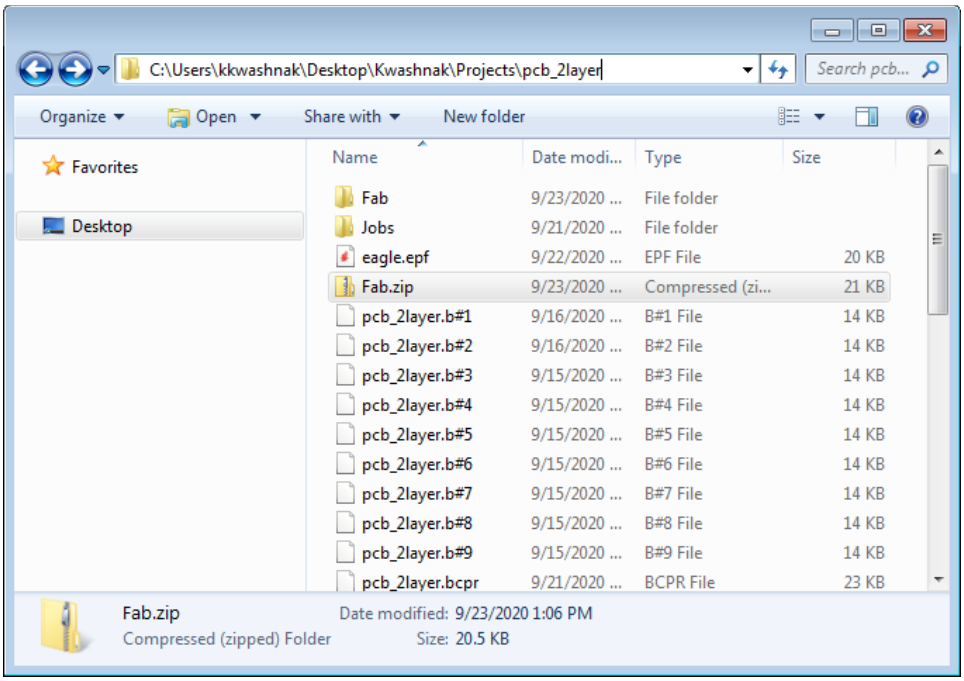


Fig. 221 Compressed fab file

Rename the "Fab" compressed zip file to "pcb_2layer_fab" (ensure the .zip extension is still attached to the file name) (Fig. 222).

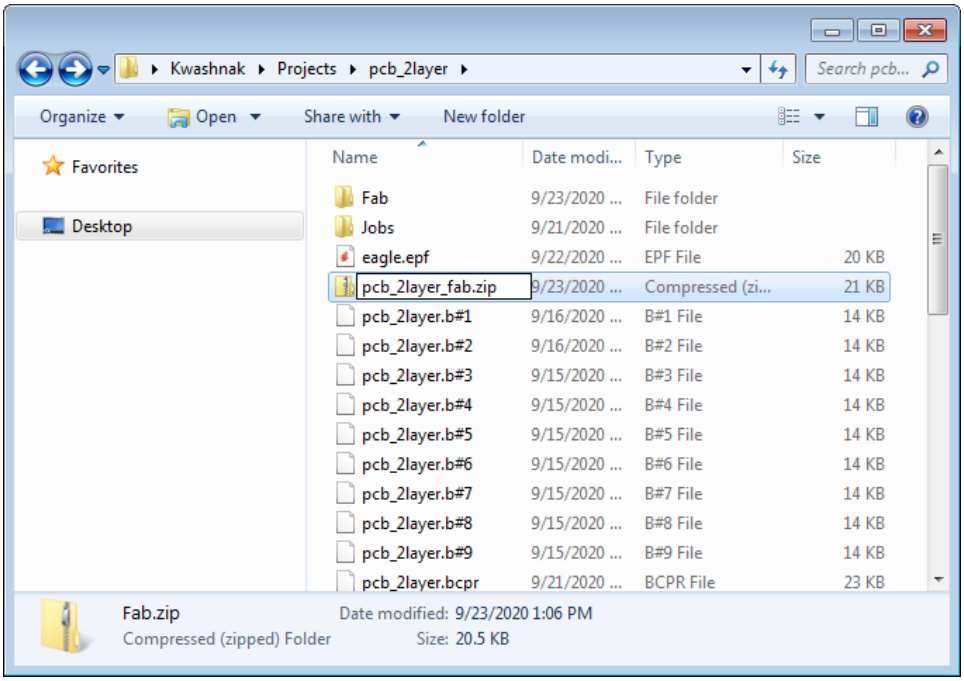


Fig. 222 Renaming compressed file

4.18 Step 18: Send to Manufacturer

This step can get involved, primarily with maximizing cost per board and delivery time. Online quotes may go through a few iterations because of user inputs (designer might not know what the manufacturer is specifying) or the algorithms used in PCB manufacturer's auto-quoting software might make a few critical (and perhaps wrong) assumptions about the board. Contacting the manufacturer directly may help with reducing costs, but now there is another person in the loop, which might affect the fabrication/delivery time.

For the manufacture's online auto-quoting tool, the software might not state the price of a 12 × 12 FR4 sheet of material, but will charge for the entire sheet for the board. The tool may not specify how many boards will fit onto one sheet. If one board is created, the manufacturer may charge for the use of an entire sheet. If the quote asks for multiple boards, the manufacturer may fill up the FR4 sheet and the cost per board may drop, but how many boards are able to fit onto one sheet? Therefore, using the auto-quote tool might take some time finding the price curve in quantity versus cost.

In addition, when reviewing the quote, compromises in copper weight, silkscreen, or other factors may weigh in for the cost. For example, if the board has various graphics and text on the top and bottom layers, is it really necessary? Will this board be installed in a professional setting? Who will see it? The overall price of the board is also driven by the type of material used, how many holes, how many different sized holes (tooling changes), layers thickness, via or signal trace size, and so on.

Also, before giving any files to a manufacturer, always read their license agreements to understand how the manufacturer will handle project files and materials.

4.18.1 Advanced Circuits

The PCB manufacturer Advanced Circuits[37] is used to generate a quote for the two-layer PCB (Fig. 223).

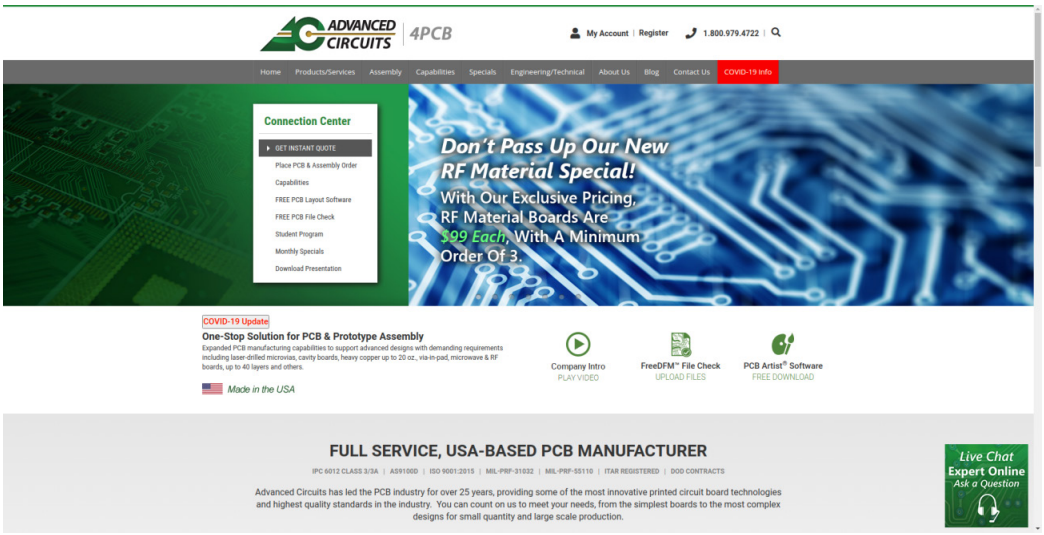


Fig. 223 Advanced circuits welcome screen

Create an account and login with proper credentials. On the left of Fig. 224, click on "Upload Files to FreeDMF".

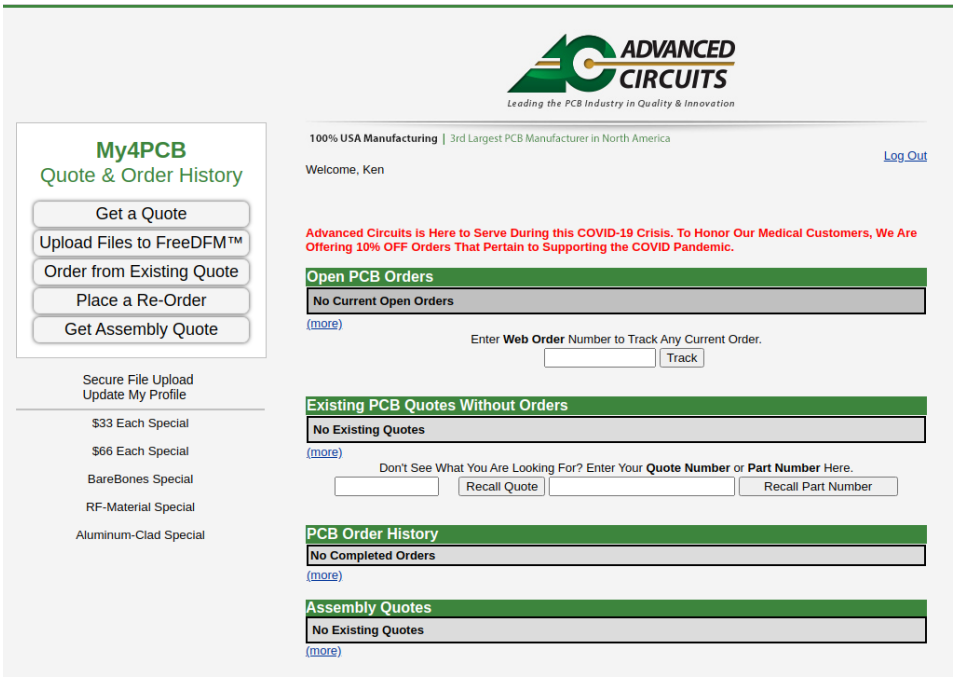


Fig. 224 Advanced circuits main screen

Enter user email and upload the "pcb_2layer_fab.zip" compressed file (Figs. 225 and 226).

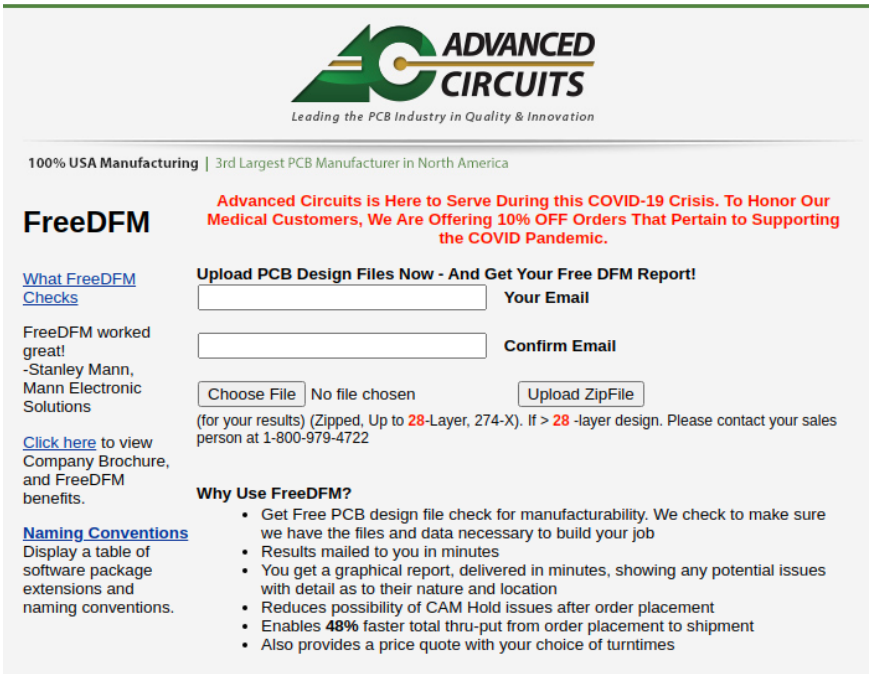


Fig. 225 Advanced circuits FreeDFM

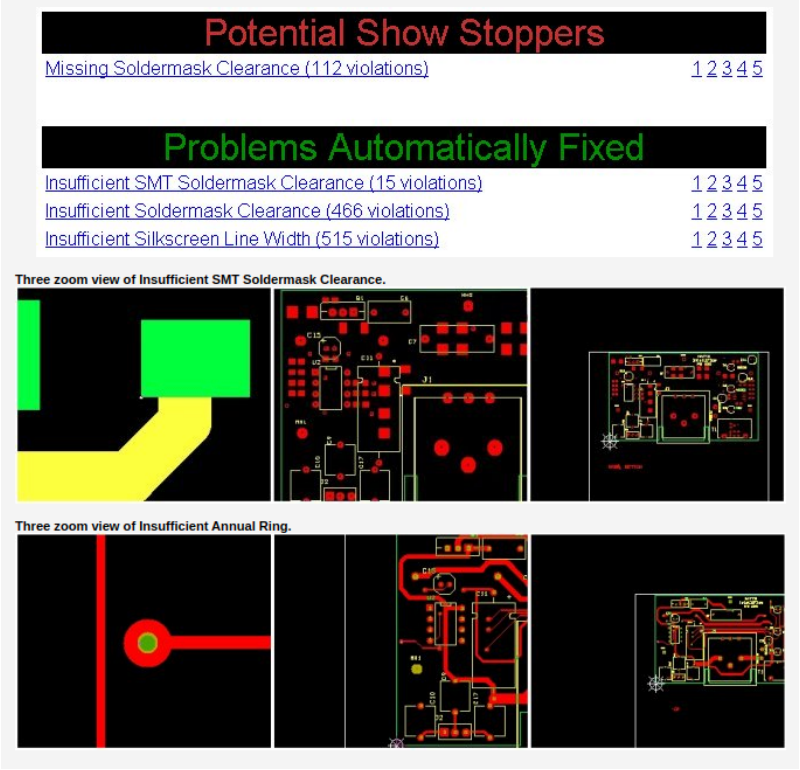


Fig. 226 FreeDFM sample results

Once uploaded, Advanced Circuits will need to parse the files to match their convention. Pair selected files to the appropriate designation, as in Fig. 227.

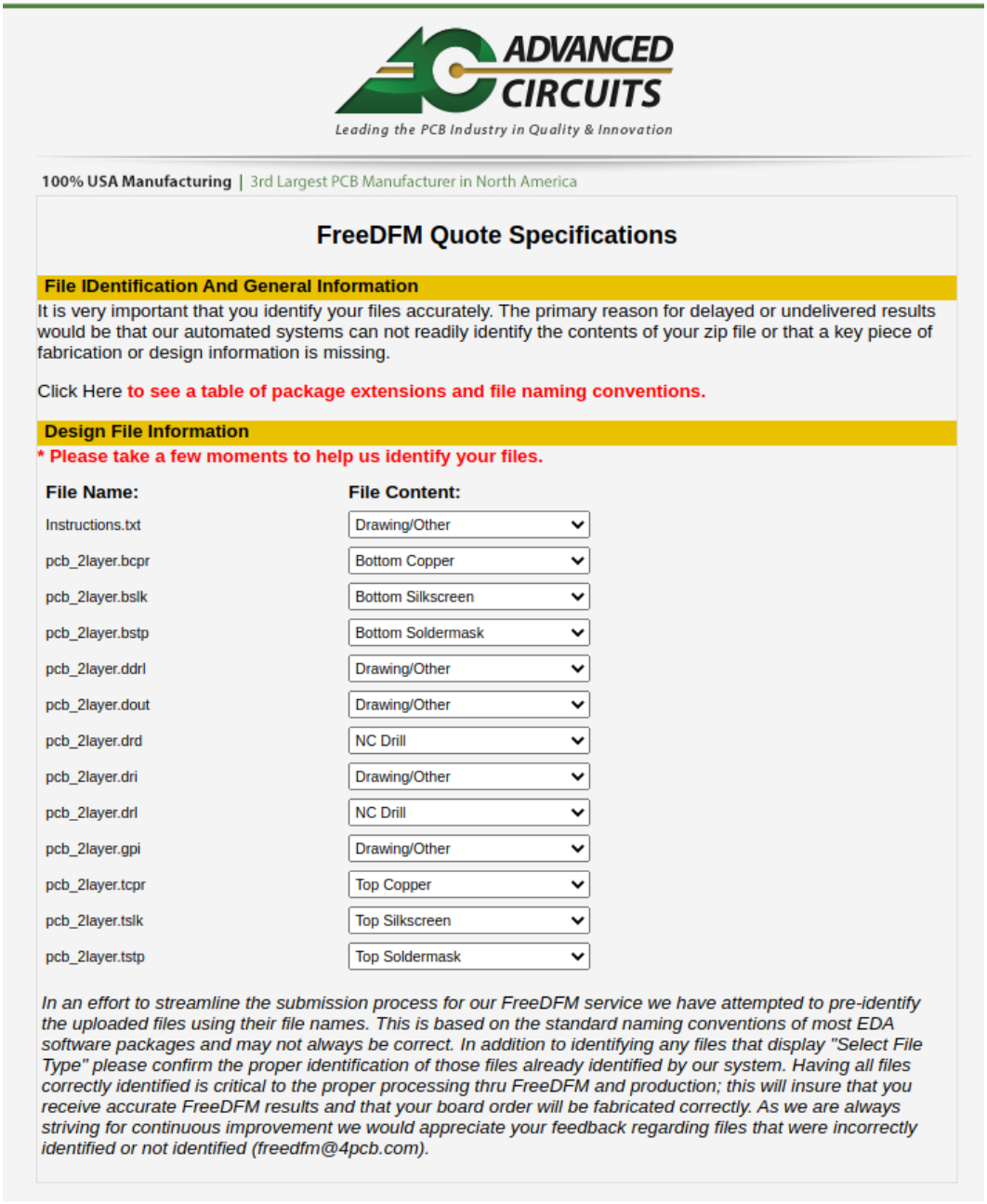


Fig. 227 Advanced circuits quote specifications, page 1

Once files are associated, input board information, as in Fig. 228.

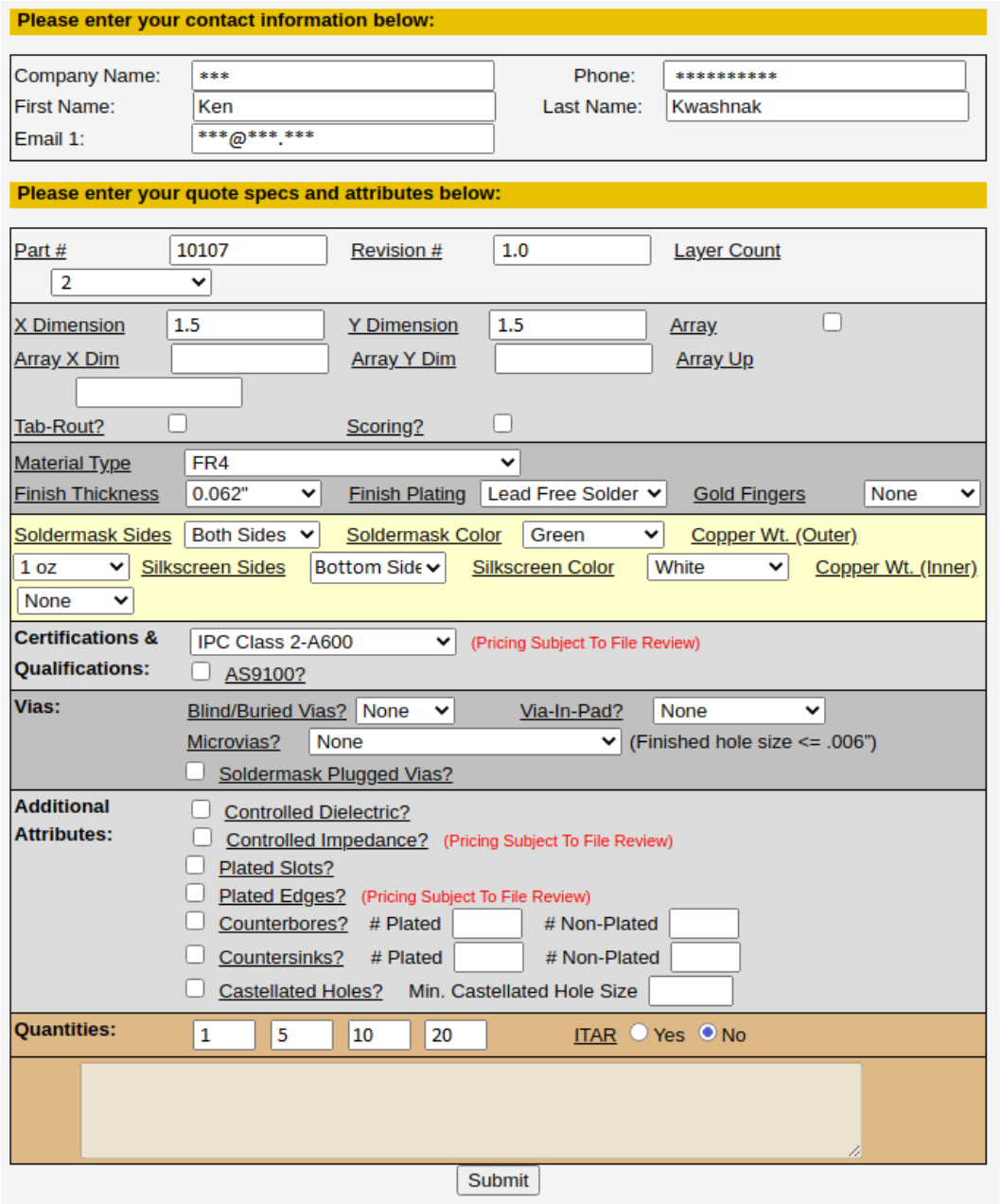


Fig. 228 Advanced circuits quote specifications page 2

The board has custom Gerber file names that do not conform to an industry standard. Advanced Circuits has gathered similar file names and their association, as shown in Table 13.

Table 13 Filename alternatives[38]

Top copper	Bottom copper	Top soldermask	Bottom soldermask	Top silkscreen	Bottom silkscreen	NC drill	Inner layers	Fab print
.TOP	.BOT	.MSK	.STS	.GTO	.GBO	.TAP	.SIG	.DD1
.CMP	.SOL	.STC	.SMB	.OVL	.BSK	.TXT	.G1	.DRD
.GTL	.GBL	.SMT	.MK2	.SLK	.PLS	.DRL	.P1	art.*
.LY1	.LY2	.GTS	.BMK	.SK1	.SK2	.NCD	.GP1	fab.*
art01.pho	art02.pho	.GTM	.GBS	.SS1	.SS2	.DRD	.GNMD	print.*
		.MK1	.GBM	.TSK	ssb01	.TH	.PWR	.DWG
		.TMK	.BSM	.PLC	ssb0226.pho	thruhole.*	.L1	
		.TSM	.SM2	sst0126.pho			plane.*	
		.SM1	sm02.*				art.*	
		sm01.*	sm0228.pho				.GM1	
		sm0128.pho						

Notes:
.TXT may be a drill file or readme file
.DRD may be a drill file or fabrication drawing
.GM1 may either be a mechanical or inner layer
.GKO is a "keep out" layer note -- do not use

Quote information is directed to the email entered in the earlier steps. Navigating back to the Advanced Circuits account main page, the quote will appear in the "Existing PCB Quotes Without Orders". Click on the hyperlink, under the Quote # (Figs. 229–232).

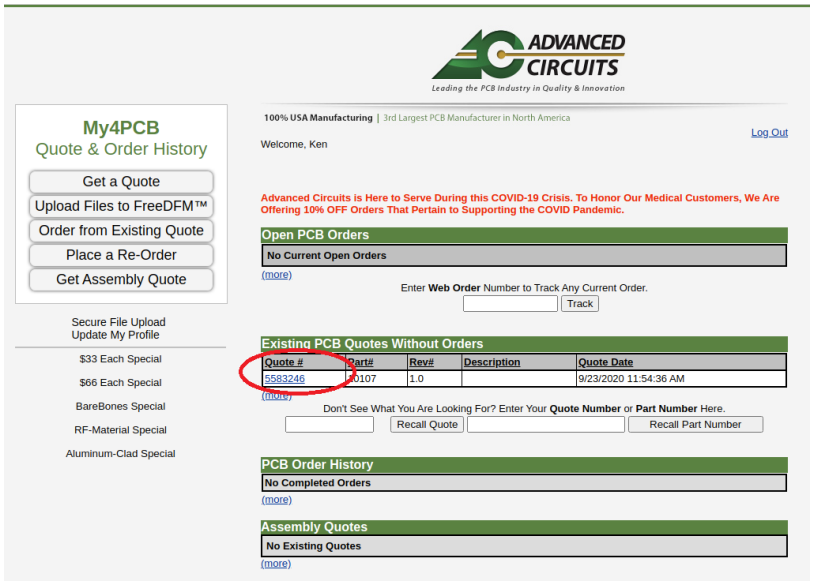


Fig. 229 Quote number

FreeDFM Viewer 2.0

Click to View FreeDFM Results

Part #: 10107	Revision: 2.0	Date: 9/23/2020	Quote #: 5583593
Self			Quote valid for 30 days

STANDARD SPEC Price Matrix:

(Qty = Pieces, Not Arrays)

1. Standard Spec bare board pricing assumes lead-free HAL (alternatively, board finish may be upgraded to ENIG or Silver at no additional cost in the rare event lead-free HAL becomes temporarily unavailable), FR4, green mask, white silkscreen, and non-plated slots.
2. We now offer both non-plated and plated thru holes on all of our standard spec boards (if no specifications provided, holes will be plated).
3. INCLUDES UL markings and date codes. 94V-0 is added if requested at time of order entry or if noted in files. Minimum finished hole size .010". Hole tolerance +/- .005". Minimum Trace/Space .005".
4. All files receive full CAM review and inspection to IPC class 2-A600.
5. If your design includes countersink/counterbore or if you have controlled dielectric/stackup or impedance requirements, refer to Custom Spec matrix.
6. Electrical Test is optional for 0-6 layer board. Unit price does not include shipping and handling. AC Terms and Conditions apply.
7. Advanced Circuits has a 90 day limited warranty and we will not accept liability for any cost in addition to the value of the bare boards including but not limited to components, labor, business interruptions and any other consequential damages or losses. Advanced Circuits disclaims any open-ended acceptance of liability for losses beyond our control.

To Place Order, Click on UNIT PRICE below:

Qty	Same Day	1-day	2-day	3-day	4-day	5-day	E Test(Lot)
3	$352.17	$220.06	$169.25	$128.60	$124.53	$120.47	$75.00
6	$176.09	$110.03	$84.62	$64.30	$62.27	$60.23	$90.00
12	$92.29	$59.26	$46.56	$36.40	$35.38	$34.37	$120.00
24	$46.15	$29.63	$23.28	$18.20	$17.69	$17.18	$144.20
Tooling NRE = $0							

AS A SPEC & PRICING ALTERNATIVE THE STANDARD SPEC MATRIX ASSUMES:

See #1 thru #7 above.

CUSTOM SPEC Price Matrix: (Qty = Pieces, Not Arrays)

1. The Custom Spec bare board Matrix reflects pricing for the EXACT SPECS you QUOTED (except as noted in the comments).
2. Our default multi-layer FR4 material is Isola 185HR or equivalent.
3. All files receive full CAM review and inspection to the certification / qualification you select below.
4. INCLUDES UL markings and date codes. 94V-0 is added if requested at time of order entry or if noted in files. Finished hole tolerance +/- .003"(if requested). Unit price does not include shipping and handling. AC Terms and Conditions apply.
5. Advanced Circuits has a 90 day limited warranty and we will not accept liability for any cost in addition to the value of the bare boards including but not limited to components, labor, business interruptions and any other consequential damages or losses. Advanced Circuits disclaims any open-ended acceptance of liability for losses beyond our control.

To Place Order, Click on UNIT PRICE below:

Qty	Same Day	1-day	2-day	3-day	4-day	1-week	2-week	3-week	4-week
3	$309.76	$270.19	$181.14	$129.19	$116.82	$111.88	$106.93	$97.03	$87.14
6	$156.26	$136.27	$91.29	$65.06	$58.81	$56.31	$53.81	$48.82	$43.82
12	$79.51	$69.31	$46.37	$32.99	$29.81	$28.53	$27.26	$24.71	$22.16
24	$41.13	$35.83	$23.91	$16.96	$15.30	$14.64	$13.98	$12.66	$11.33
Tooling NRE = $163.77 (Tooling waived when re-ordered) * Testing = $144.20									

*** ET charges shown above do not include Hi-Pot test charges.**

Fig. 230 Quote information

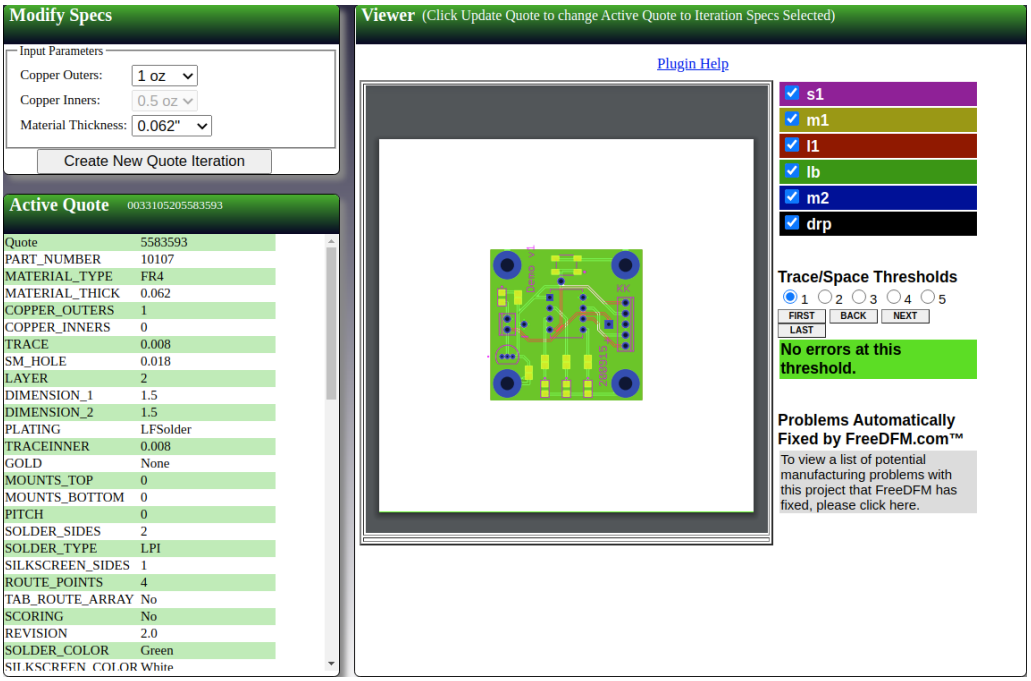


Fig. 231 Advanced circuits DFM, page 1

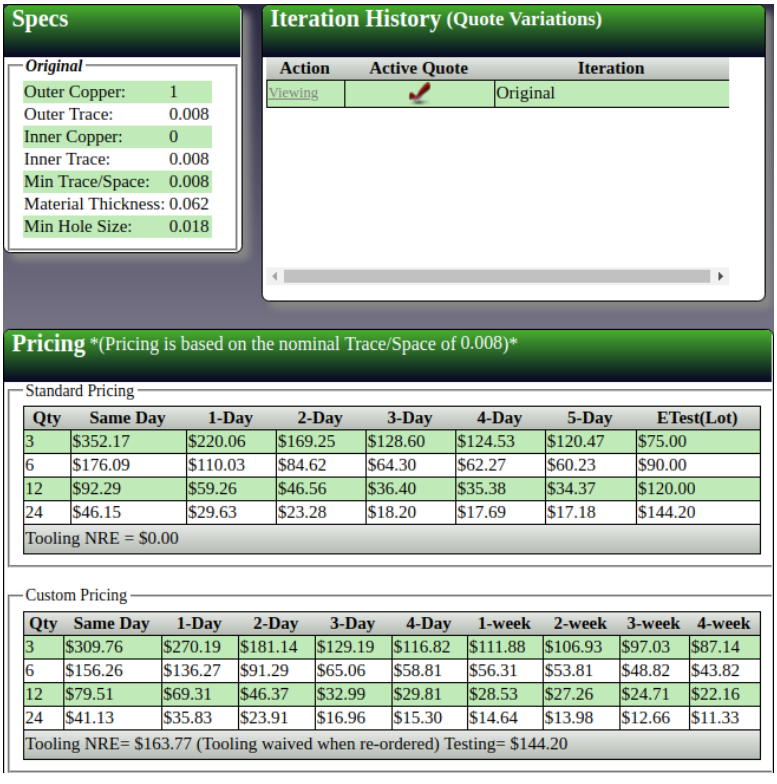


Fig. 232 Advanced circuits DFM, page 2

4.18.2 Oshpark

The PCB manufacturer Oshpark[39] is used to generate a quote for the two-layer PCB Click on <BROWSE FOR FILES>, indicated on Fig. 233, and select the project board file .brd (Fig. 234).

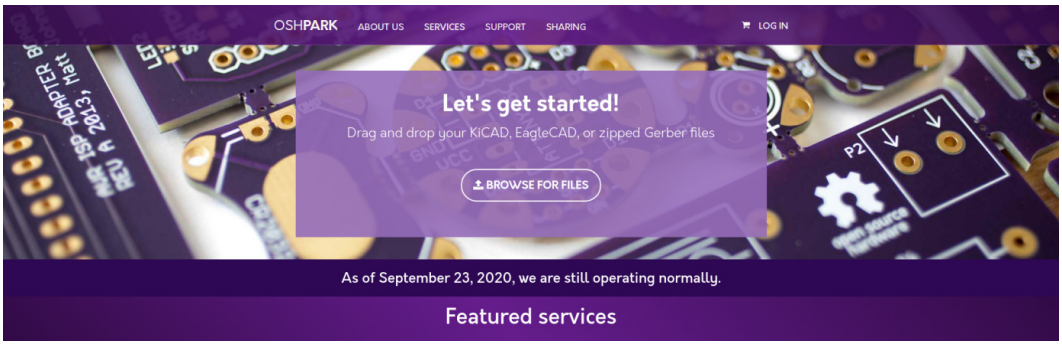


Fig. 233 Oshpark welcome screen

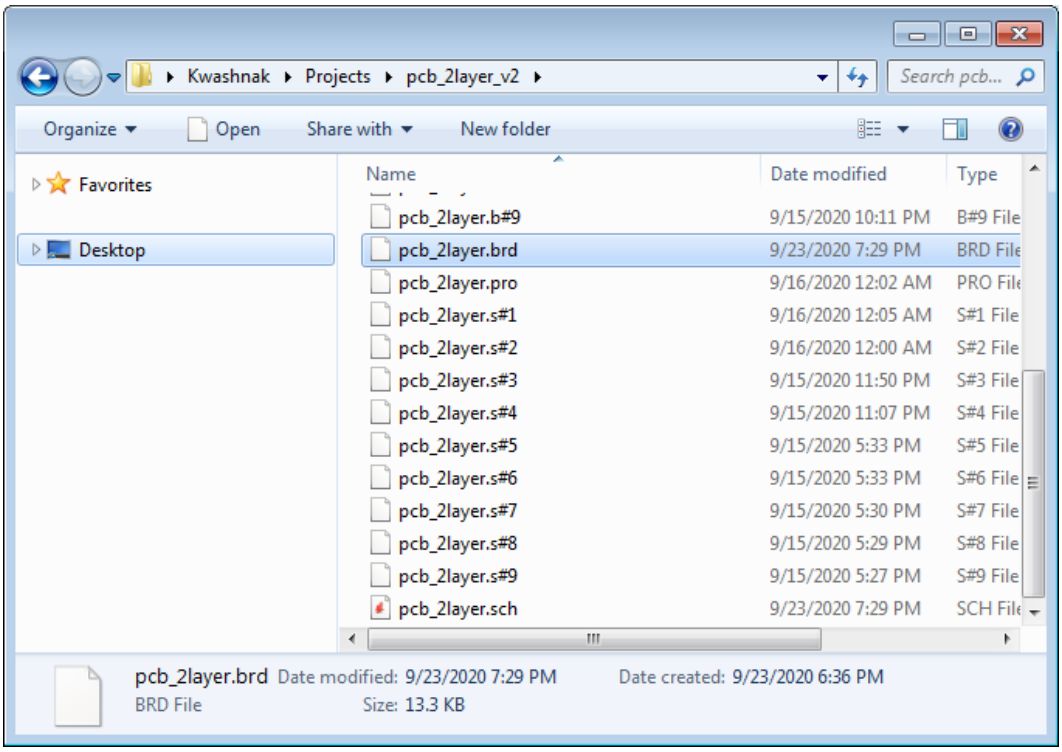


Fig. 234 Project board .brd file

Enter project name, details, and contact email information as in Fig 235.

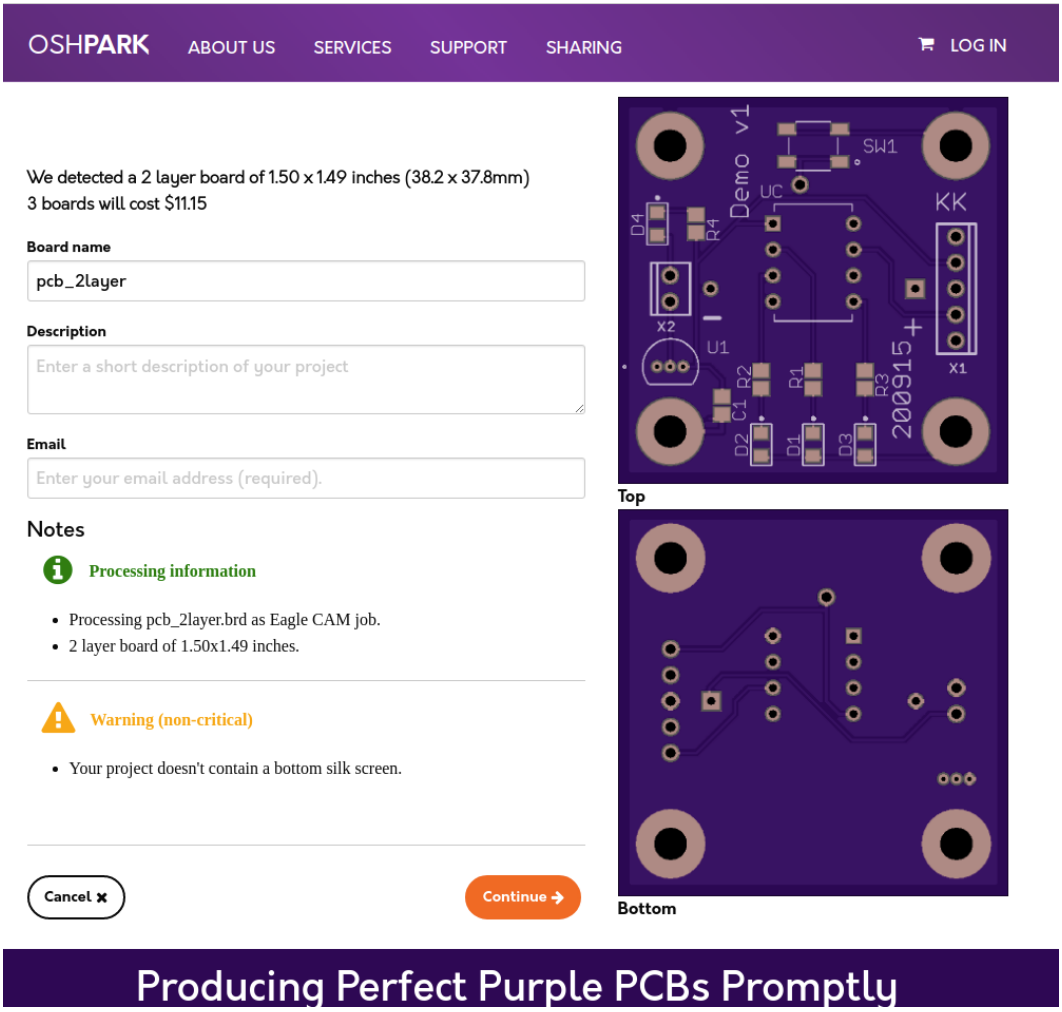
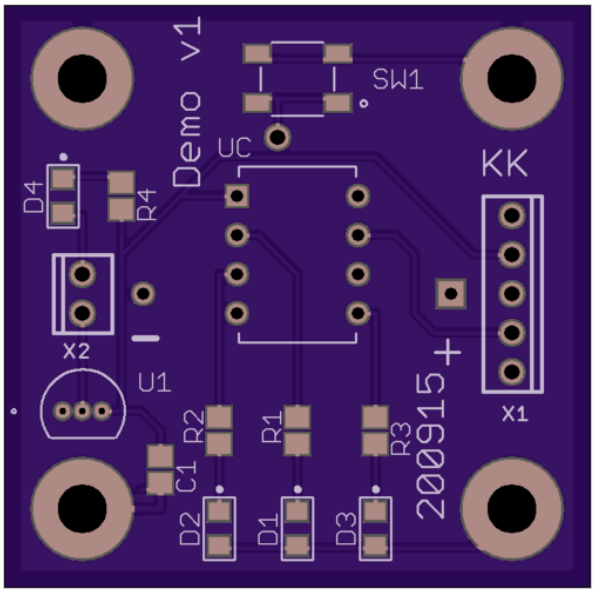


Fig. 235 Oshpark instant quote

The following images (Fig. 236–244) are Oshpark's extracted layer information from the imported project. Review these images to make sure the board pairs with the EAGLE design.



Board Top

This shows the final manufactured board as if you held it in your hand.

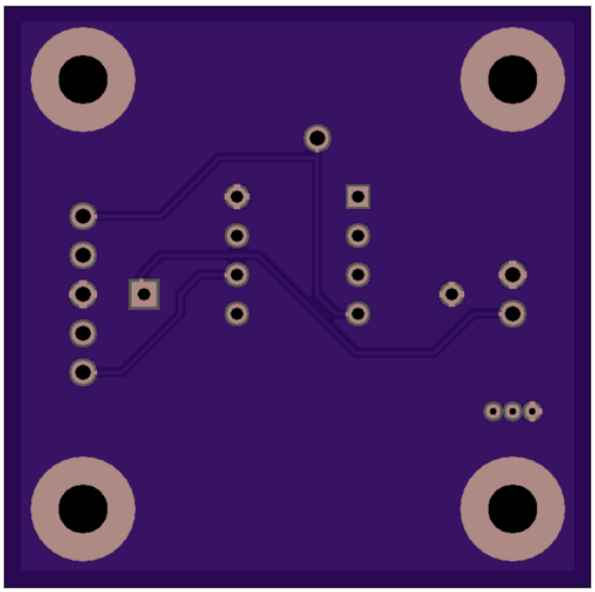
Your design should show gold copper, purple mask, white silk, black drills, and the board outline.

Internal cutouts are indicated by a black outline but are not filled in.

If the image here is entirely white, you'll want to find and fix any gaps in the board outline.

There should be no dimension or measurement ruler

Fig. 236 Oshpark board top



Board Bottom

This shows the final manufactured board as if you held it in your hand.

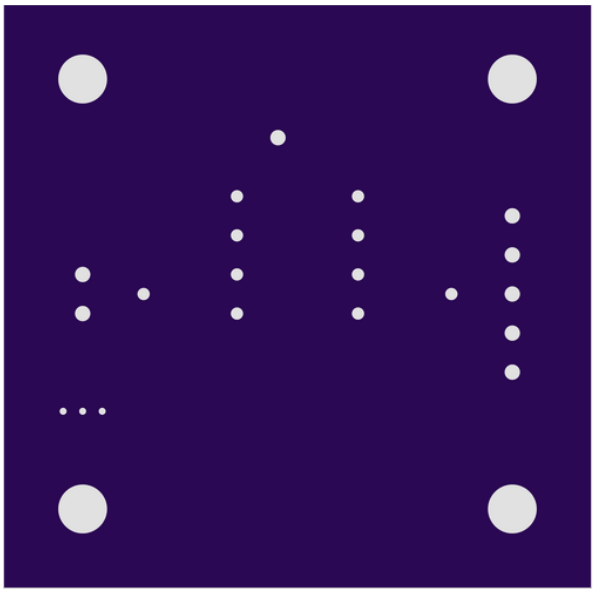
Your design should show gold copper, purple mask, white silk, black drills, and the board outline.

Internal cutouts are indicated by a black outline but are not filled in.

If the image here is entirely white, you'll want to find and fix any gaps in the board outline.

There should be no dimension or measurement ruler

Fig. 237 Oshpark board bottom



Rendered from "Drills.xln"

Drills

Drills should show up as white circles or dots on a purple background.

Drill files should be NC Drill or Excellon format files. Multiple files will be accepted, and merged into one for fabrication.

Drill hits that pass through copper will be plated. All other drill hits will be non-plated.

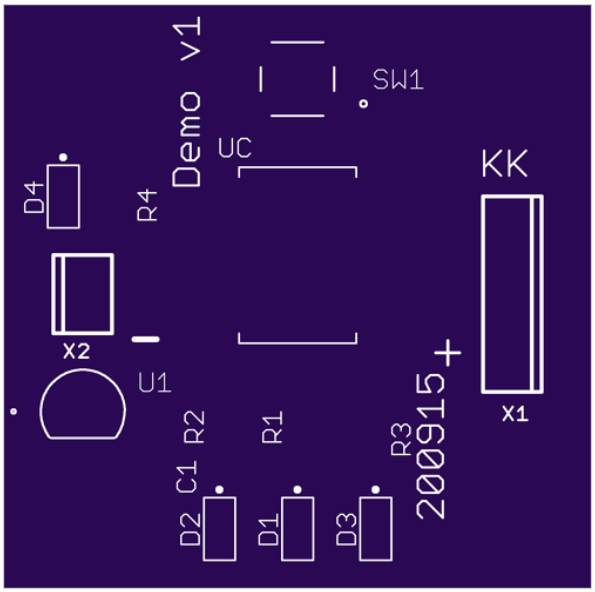
Most drill formats are detected and displayed as you'd see on the board. If your drills look incorrect, try exporting with INCH units and either No Zero Suppression or Leading Zero Suppression.

Drill slots and "oval" drills included as part of the drill file are supported. Most design tools do this when using the tool's native slot commands. Supported slots will appear on this preview. Note, it's possible to use this supported callout in an unsupported way. See our Cutouts and Slots page for details regarding unsupported applications of slot drill commands.

Drills sizes below our minimums will be increased to the minimum size. See the design rules or our drills help page. for additional details on drill specs.
Additionally, the following are not supported.

- **Overlapping drill hits**
- **Blind or buried vias**

Fig. 238 Oshpark drills



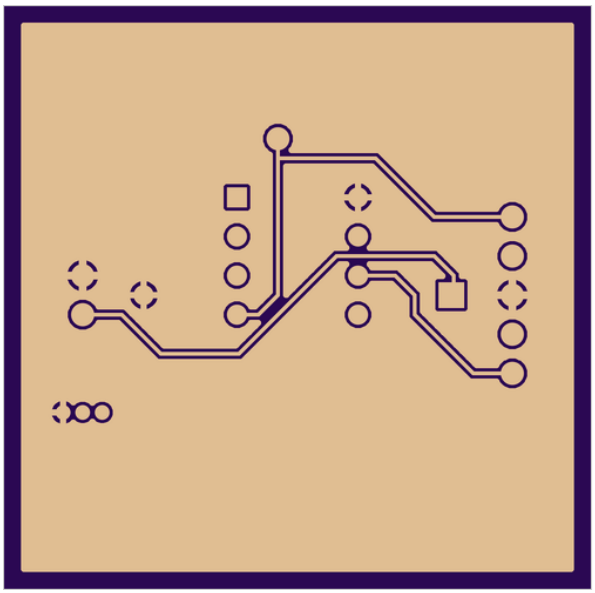
Top Silk Screen

We will ignore the portion of the silkscreen that extends beyond the board outline.

We will automatically remove any silkscreen that crosses drilled holes or exposed copper.

If a logo isn't showing up on this layer, try changing your design tool import settings to create that silk image with 400 DPI or less, or check out our Eagle-specific import-bmp script instructions.

Fig. 239 Oshpark top silkscreen



Bottom Layer

This layer should appear 'mirrored' as if you were looking down on it through the board from the top.

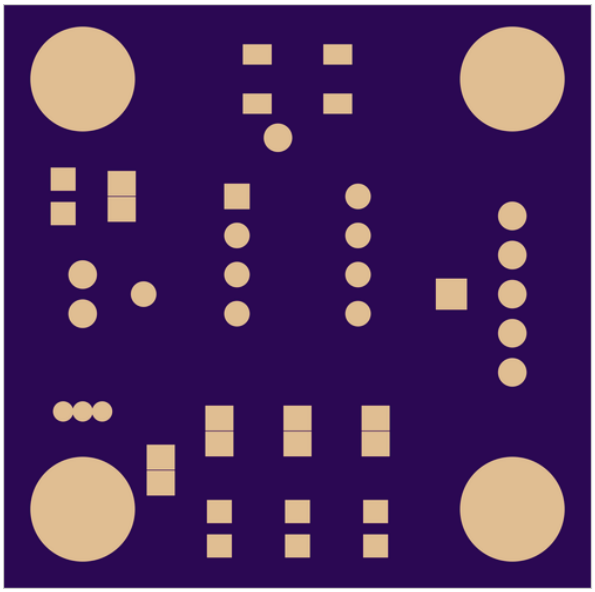
We will place copper everywhere we see gold color on this layer.

If you are using Altium Designer or Altium CircuitMaker, carefully examine the board to make sure there are no shorts from the mechanical layers being included on this layer. See here for more.

If you are using Eagle, be aware that airwires are not the same as routed traces. If there are no copper links between pads showing on this layer, please review your .brd file for airwires.

See our design tools pages for more.

Fig. 240 Oshpark bottom layer



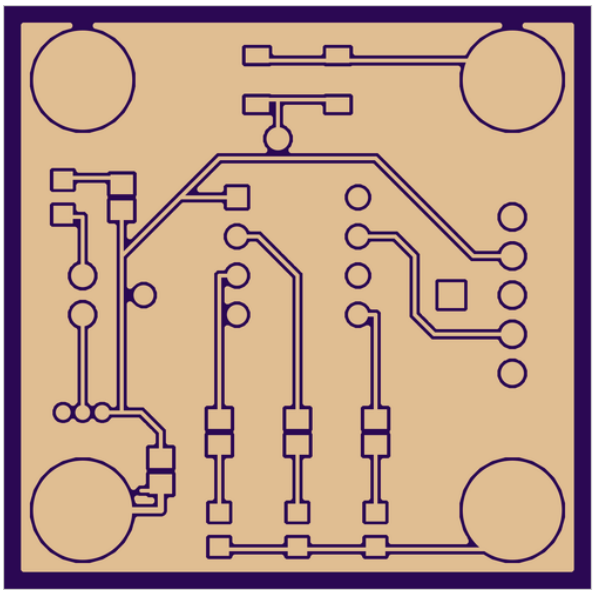
Top Solder Mask

Soldermask layers show us where to remove the purple solder resist. The gold-colored areas will be exposed on the final board, and purple areas will be covered.

If you submitted an empty file, we won't remove any mask so this entire side of the board will be covered in purple soldermask

To expose the entire board, submit this file with a single polygon that covers the entire board. We will remove all mask everywhere and expose all the copper and board substrate.

Fig. 241 Oshpark top solder mask



Top Layer

We will place copper everywhere we see gold color on this layer.

If you are using Altium Designer or Altium CircuitMaker, carefully examine the board to make sure there are no shorts from the mechanical layers being included on this layer. See here for more.

If you are using Eagle, be aware that airwires are not the same as routed traces. If there are no copper links between pads showing on this layer, please review your .brd file for airwires.

See our design tools pages for more.

Fig. 242 Oshpark top layer

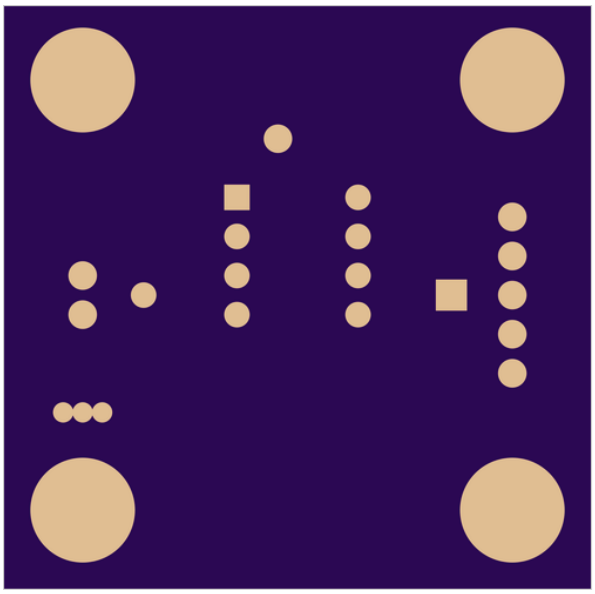
Board Outline

The board outline should be a watertight purple outline showing at least the edge of the board with no gaps.

We will cut non-rectangular board shapes, but you will be billed for the smallest rectangle that will encompass the design.
As an example, a 2in diameter circle is billed the same as a 2in by 2in square.

Non-plated Board Cutouts can be represented on the board outline layer, with some limitations. Slots are unsupported when indicated on the board outline layer, but usually work. To make slots with full support, use Drill Slots on the drill layer.

Fig. 243 Oshpark board outline



Bottom Solder Mask

This layer should appear 'mirrored' as if you were looking down on it through the board from the top.

Soldermask layers show us where to remove the purple solder resist. The gold-colored areas will be exposed on the final board, and purple areas will be covered.

If you submitted an empty file, we won't remove any mask so this entire side of the board will be covered in purple soldermask

To expose the entire board, submit this file with a single polygon that covers the entire board. We will remove all mask everywhere and expose all the copper and board substrate.

Fig. 244 Oshpark bottom solder mask

5. Reception and Testing of PCB

5.1 Reception of Oshpark Boards

The PCB manufacturer Oshpark fabricated the boards shown in Fig. 245. Upon physical inspection, the ordered PCB mirrors the eCAD design. Using a caliper to inspect the physical dimensions of the board, the board and hole sizes are in

agreement with the manufacturer's tolerances. In addition, the silkscreen graphics look decent, with no blur. The board does have sharp protruding material projecting from the edges. This is most likely left-over spurs from holding/cutting the PCB array; a file or sandpaper is used to clean up the board's edges. Using a multimeter, all traces are tested for proper connections and there is no error found on the board.

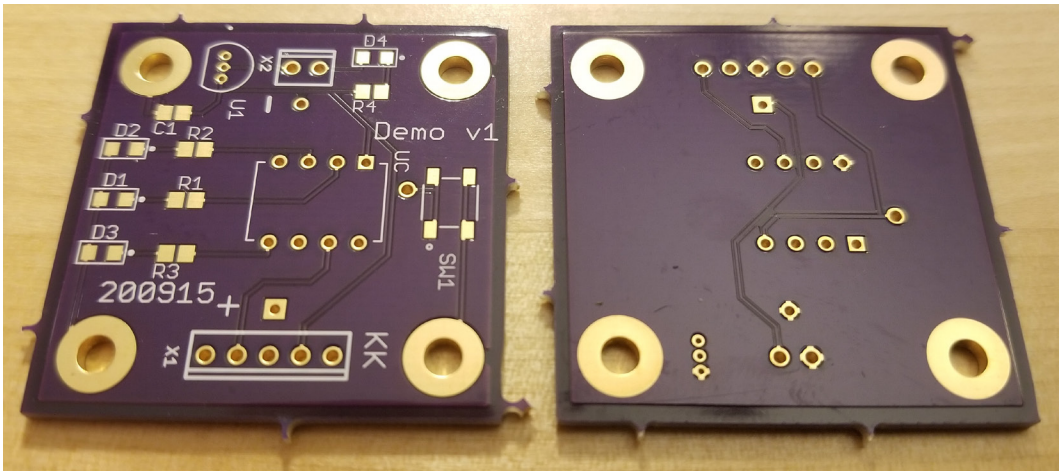


Fig. 245 Oshpark fabricated board

5.2 Assembling and Testing PCB Power

Utilizing readily available components, a prototype board is assembled, as shown in Fig. 246. The board is powered with an external power supply set to 3.70 V. The substitute linear regulator (STMicroelectronics, PN: L78L33ACZ-AP) outputs 2.825 V to the microcontroller. The blue LED illuminates signifiying power to the system.

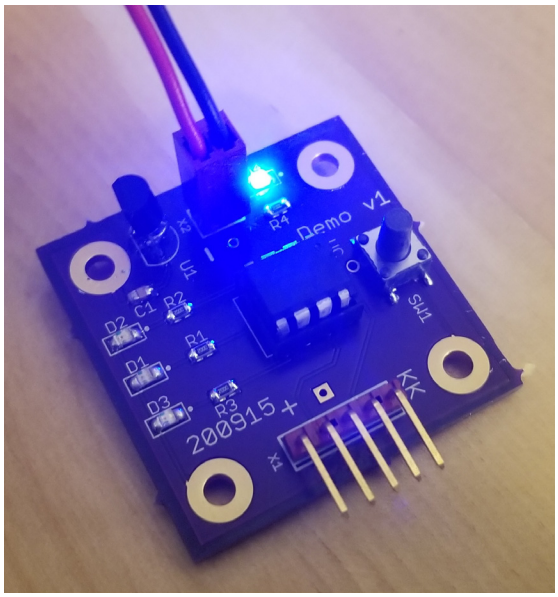


Fig. 246 Testing power on prototype PCB

5.3 Extended Testing

In order to assess each LED, the board is programmed using Microchip's MPLAB X Integrated Development Environment (IDE) v5.4.0[33] and XC8 compiler v2.30.[34] A serial progrogramming kit (PICKit3) is connected from the laptop to the PCB.

Once the MPLAB X IDE and the XC8 compiler are installed on the virtual machine, open the software (Fig. 247).

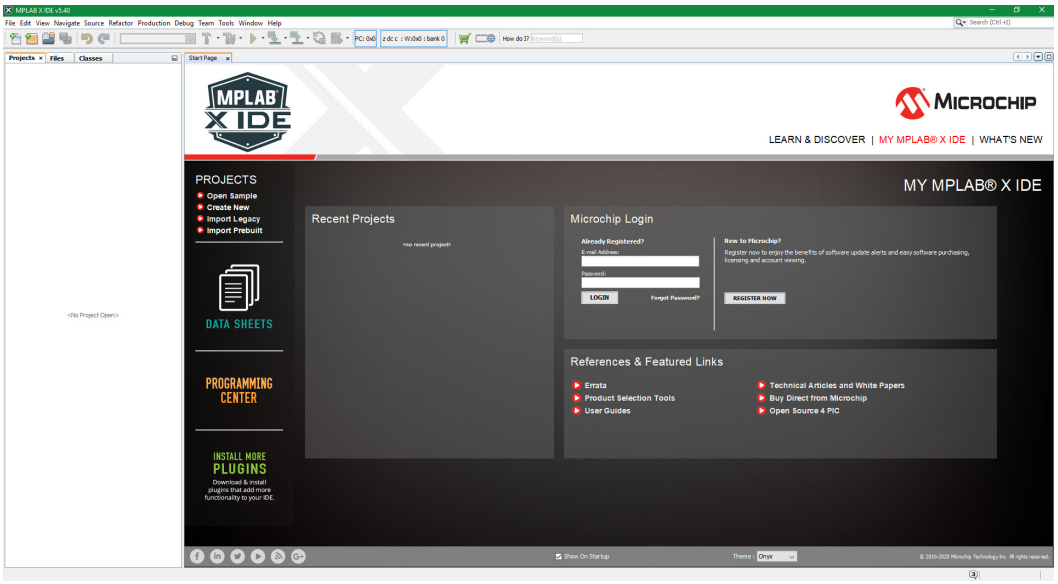


Fig. 247 MPLAB X welcome screen

In the top left of the MPLAB window go to <File>, <New Project> (Fig. 248).

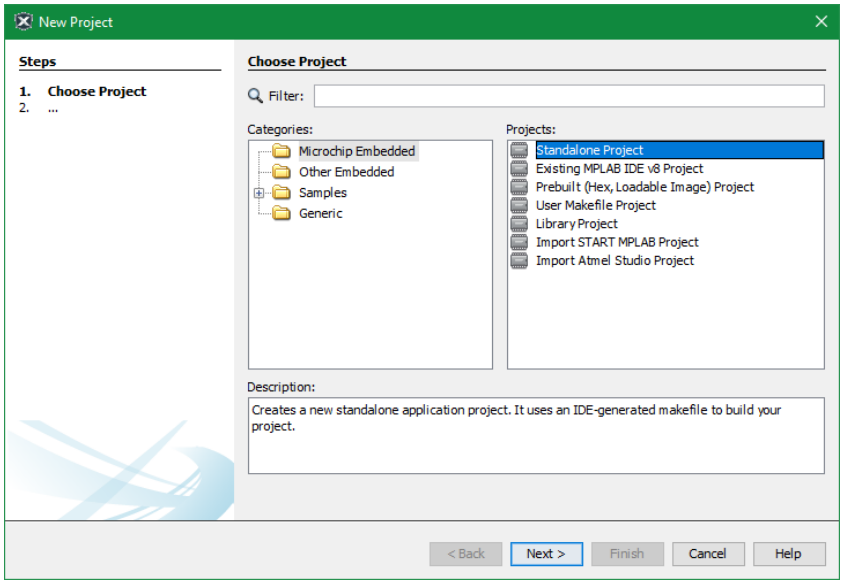


Fig. 248 Creating a standalone project

Select the drop-down menus in Fig. 249; Family: Mid-Range 8-bit MCUs (PIC10/12/16/MCP), Device: PIC12F1501, and Tool: PICkit3-SN:***. The PICkit must be attached to the computer in order to be recognized by the program. Ensure the PICkit's pins are correctly paired with the PCB. Once finished, click the <Next> button.

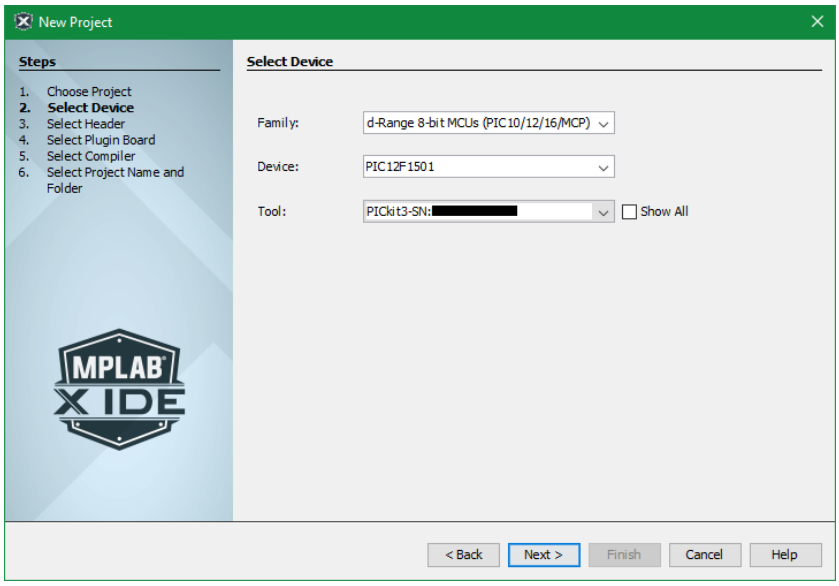


Fig. 249 Project creation

When prompted for a Supported Debug Header, select 'None' from the drop-down menu (Fig. 250). Afterward, click on <Next>.

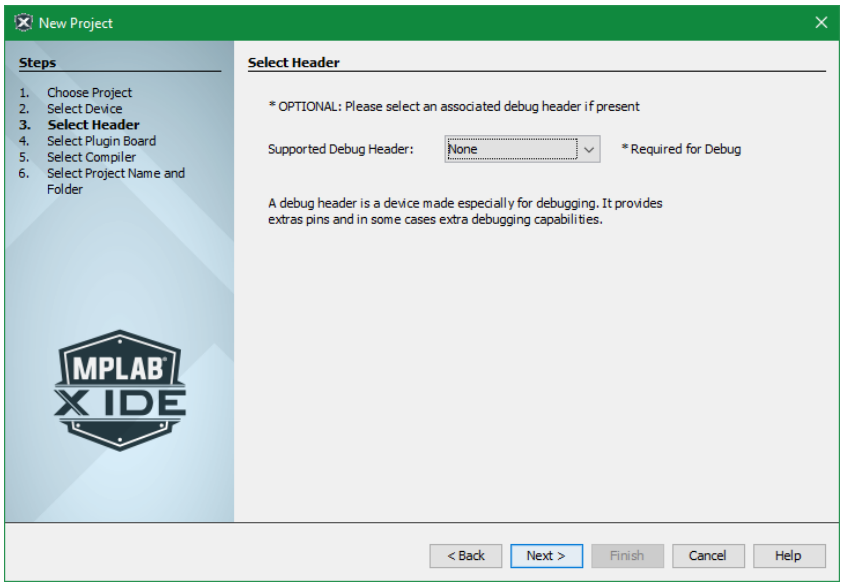


Fig. 250 Supported debug header

Select the Cross Compiler Toolchain: XC8 (v2.30) [pathway to cross compiler] (Fig. 251). Afterward, click <Next>.

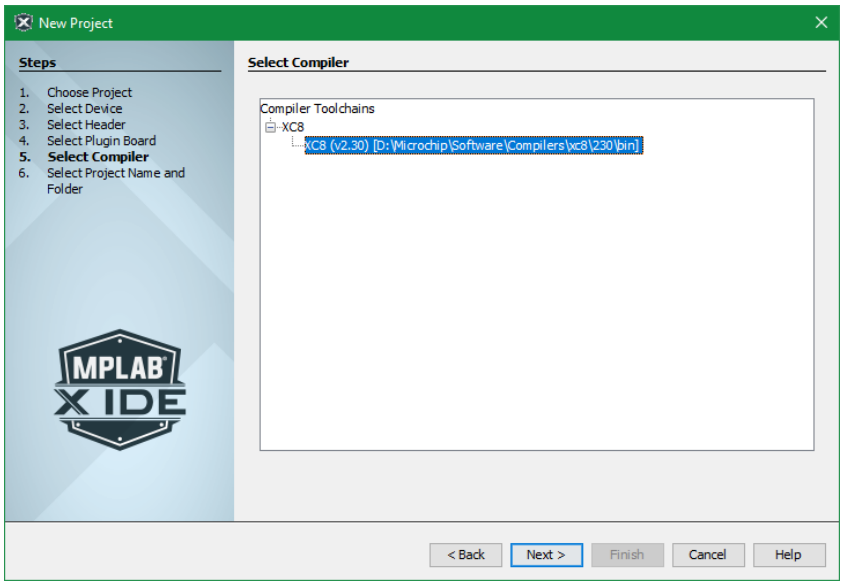


Fig. 251 Cross compiler toolchain

Enter the project's name and define its location on the computer (Fig. 252).

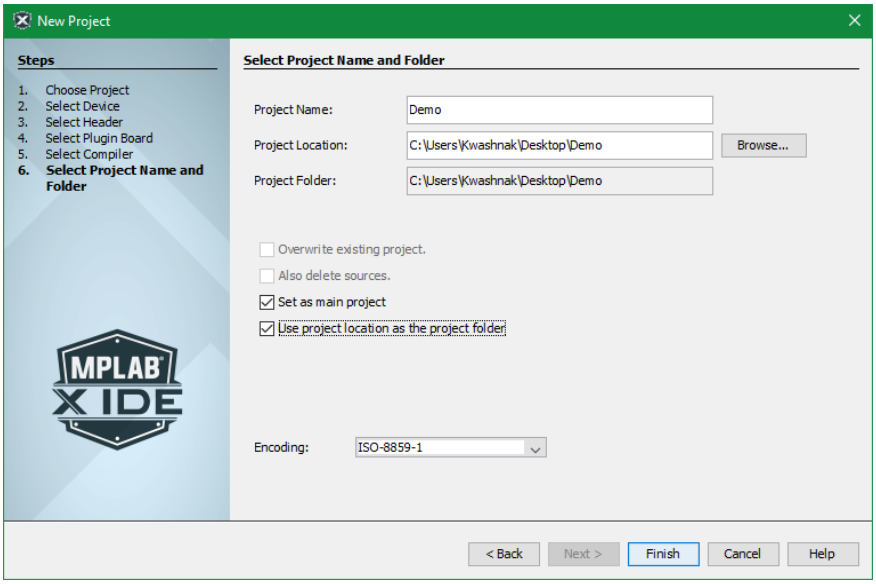


Fig. 252 Project name and location

In the project tree, on the left, navigate to the 'Source Files' folder, right-click, mouse over to 'New', 'C Source File…'. Name the file "main.c" and select 'c' for the 'Extension' (Fig. 253). This file is our main code to program the microcontroller.

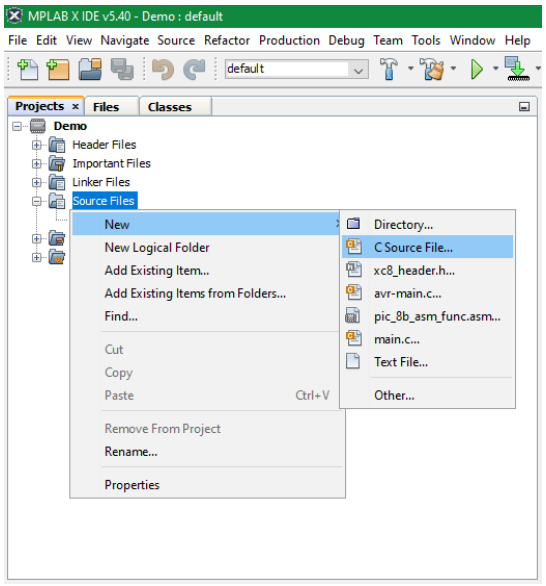


Fig. 253 Creating main.c source file

Once completed, paste the contents of code block 5 into the "main.c", which implements Microchip's microcontroller configuration parameters.[40]

```
/* Author:        Ken Kwashnak
   Contact (e):   ***@***.***
   Contact (p): (***)***-****
   Date:        October 8, 2020
   Platform:    Program intended for PIC12(L)F1501 for testing Demo v1.0 PCB functionality.
   Function:    Upon power on, individual LEDs illuminate. If switch is pressed, LEDs turn off.
*/
// define crystal frequency
#define _XTAL_FREQ 16000000
#include <xc.h>
// Device Configuration, pg 38-39 of Microchip DS40001615C
// In order for the device to function properly, all registers must be configured.
// Clock settings
#pragma config CLKOUTEN = 1
// Brown-Out Reset
#pragma config BOREN = 00
// Code Protection
#pragma config CP = 1
// MCLR Pin Function
// since LVP is enabled, 1, this bit is ignored
#pragma config MCLRE = 0
// Power-Up Timer
#pragma config PWRTE = 1
// Watchdog timer
#pragma config WDTE = 00
// Oscillator settings
// using internal oscillator INTOSC
#pragma config FOSC = 00
// Low Voltage Programming
// based off of the voltage supplied to microcontroller
#pragma config LVP = 1
// Low-Power Brown-out Reset
#pragma config LPBOR = 1
// Brown-out Reset Voltage
#pragma config BORV = 1
// Stack Over/Underflow Reset
#pragma config STVREN = 0
// Flash Memory Self-Write
#pragma config WRT = 11
void init(){
// I/O, PORTA Settings
// No alternate pin functions
// RA2, RA4, RA5 = Output = LEDs
// RA3 = Input = Push Button
// Direction Control, 1 input, 0 output
  TRISA = 0x0B; // Binary: 0000 1011
// No Latch Register Definitions
// Analog Select Register
// Digital only
  ANSELA = 0;
// Weak Pull-Up
// grounds input push button with switch closure, prevents floating
// input will read a high state, until button pressed
// no debouncing method or circuity, not necessary
// Clearing register for individual pull-up use
  OPTION_REGbits.nWPUEN = 0;
// R3 Pull-up
  WPUA = 0x08; // Binary: 0000 1000
}
void main(void){
// Frequency Configuration
  OSCCONbits.IRCF = 0xF; // 1111 = 16MHz
// Internal Clock Configuration
  OSCCONbits.SCS = 3;
// Initializes device, as per function above
  init();
// Infinite Loop, Stay in State
// PORTAbits = reads state
// LATA = write state
```

```
// __delay_ms( time in milliseconds ); note, not best if you have interrupt service routines, ISRs
// the delay assists with the microcontroller performing the selected instruction
// ensures there's enough time to execute the next statement
// the loop essentially reads state of switch, if value is high, then write ON values to LEDs
// once the switch is pressed, input state goes low, and LEDs turn off
  while(1){
    if(PORTAbits.RA3){
      LATA = 0b000100; // RA2
      __delay_ms(100);
      LATA = 0b010000; // RA4
      __delay_ms(100);
      LATA = 0b100000; // RA5
      __delay_ms(100);
    }else{
      LATA = 0b110100;
    }
  }
}
```

Code block 5 PIC12F1501 code

Afterward, click on the <Clean and Build Project> button to compile the program, as in Fig 254.

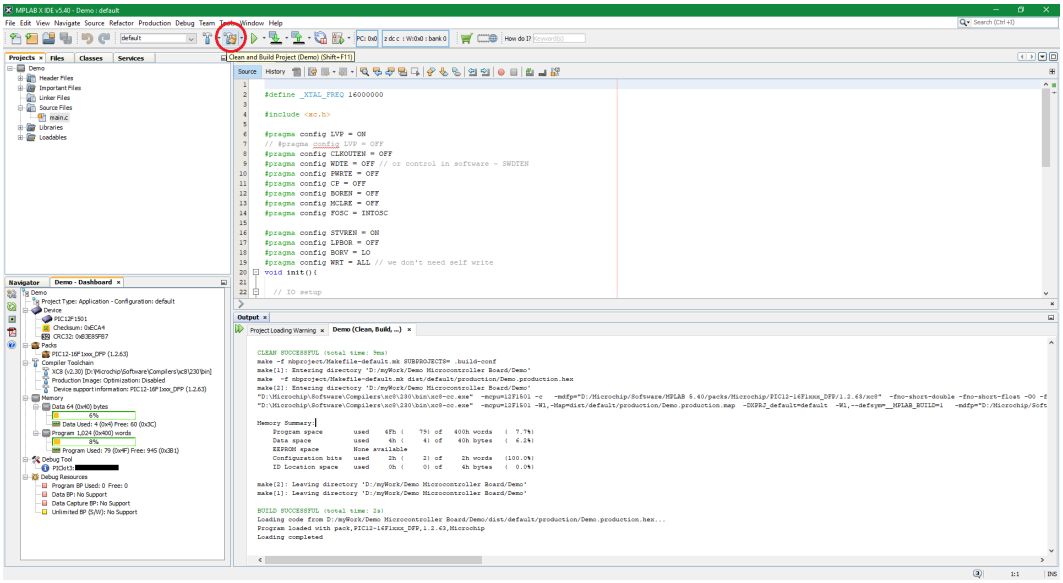


Fig. 254 main.c code compilation

With no errors in the code, ensure the PCB is powered with 3.7 V and the PCB is hooked up to the laptop via the PICkit 3. Click on the <Make and Program Device> button, as shown in Fig 255.

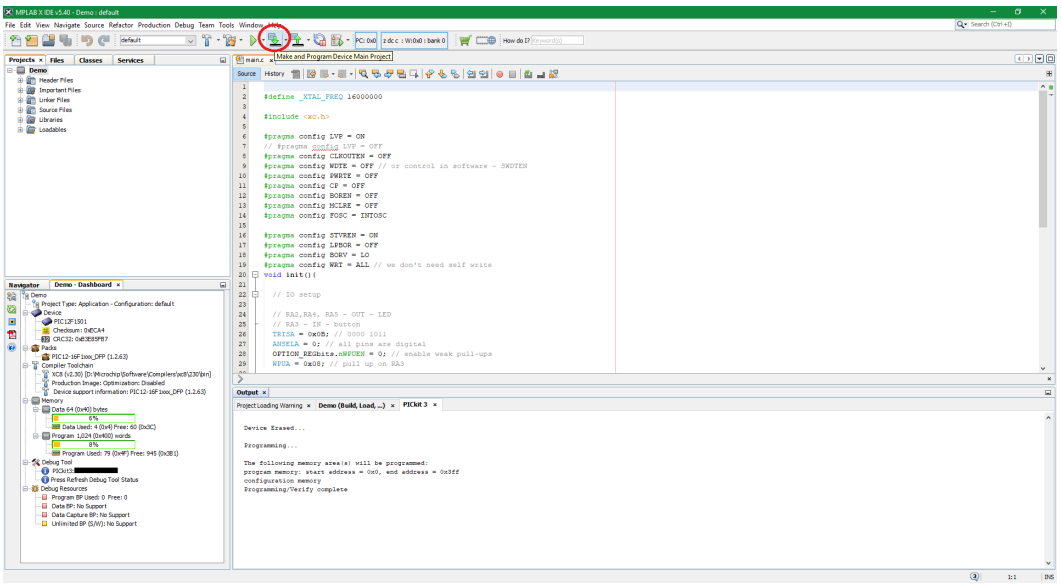


Fig. 255 PCB programming

6. Conclusion

Overall, the EAGLE design process is easy and straightforward. Creating resources may take some time, but it is necessary in order to ensure proper component functionality. Various manufacturers and designers have complete devices readily available for use—just check the license agreement and core design elements (symbol and package). A schematic is useful for assembling the design and essential for associating board components. Once the schematic is completed, a board file is manipulated to form a well-defined PCB (Fig. 256). The CAM feature allows generation of board information and Gerber files that a PCB manufacturer uses to make the eCAD board into a physical entity. After employing all steps described in this paper, a two-layer microcontroller PCB is fabricated, assembled, programmed, and tested.

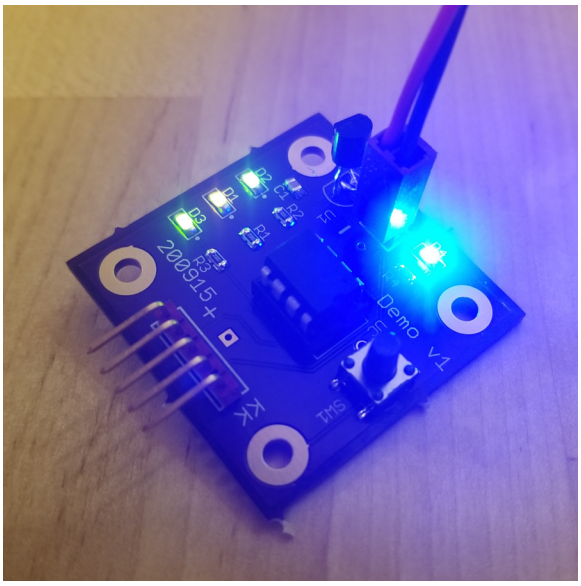


Fig. 256 Completed functional microcontroller PCB

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Appendix A. List of Manufacturing References

A.1 PCB

1) Advanced Circuits
2) OshPark
3) Sierra Circuits
4) Sunstone Circuits
5) JLC PCB
6) Avanti Circuits

A.2 Enclosure and Panel

1) Protocase
2) Lansing Enclosures
3) Phoenix Mecano
4) Front Panel Express

A.3 Panel Overlay

1) Bradley Nameplate
2) Pannam Imaging
3) Design Mark

A.4 Component References and Distributors

1) Octopart
2) Digikey
3) Mouser
4) Arrow

A.5 List of eCAD Software Packages

1) KiCAD
2) Altium
3) pSpice
4) SolidWorks Electrical
5) Falstad Circuit Simulator Applet

Appendix B. Hypertext Markup Language (HTML)

Tables B-1 through B-3 provide descriptions of Hypertext Markup Language (HTML) formatting basic, formatting, and color code tags.[1] Other resources include a color mixer[2] and color picker[3] to assist with the design.

Table B-1 Basic HTML

Tag	Description
<!DOCTYPE>	Defines the document type
<html>	Defines an HTML document
<head>	Contains metadata/information for the document
<title>	Defines a title for the document
<body>	Defines the document's body
<h1> to <h6>	Defines HTML headings
<p>	Defines a paragraph
 	Inserts a single line break
<hr>	Defines a thematic change in the content
<!--...-->	Defines a comment

Table B-2 HTML formatting

Tag	Description
<acronym>	Not supported in HTML5. Use <abbr> instead. Defines an acronym
<abbr>	Defines an abbreviation or an acronym
<address>	Defines contact information for the author/owner of a document/article
<b>	Defines bold text
<bdi>	Isolates text that may be formatted in a different direction from other text outside it
<bdo>	Overrides the current text direction
<big>	Not supported in HTML5. Use CSS instead. Defines big text
<blockquote>	Defines a section that is quoted from another source
	Not supported in HTML5. Use CSS instead. Defines centered text
<cite>	Defines the title of a work
<code>	Defines a piece of computer code
<del>	Defines text that has been deleted from a document
<dfn>	Specifies a term that is going to be defined within the content
	Defines emphasized text
<font>	Not supported in HTML5. Use CSS instead. Defines font, color, and size for text
<i>	Defines a part of text in an alternate voice or mood
<ins>	Defines a text that has been inserted into a document
<kbd>	Defines keyboard input
<mark>	Defines marked/highlighted text
<meter>	Defines a scalar measurement within a known range (a gauge)
<pre>	Defines preformatted text
<progress>	Represents the progress of a task
<q>	Defines a short quotation
<rp>	Defines what to show in browsers that do not support ruby annotations

[1] HTML element reference. Refsnes Data; c1999–2020 [accessed 2020 Aug 20]. https://www.w3schools.com/TAGS/default.asp.
[2] Color mixer. HTML color mixer. Refsnes data; c1999–2020 [accessed 2020 Aug 20]. https://www.w3schools.com/colors/colors_mixer.asp?colorbottom=00FFFF&colortop=FFFFFF.
[3] Color picker. Refsnes data; c1999–2020 [accessed 2020 Aug 20]. https://www.w3schools.com/colors/colors_picker.asp?colorhex=F0F8FF.

Table B-2 HTML formatting (continued)

Tag	Description
<rt>	Defines an explanation/pronunciation of characters (for East Asian typography)
<ruby>	Defines a ruby annotation (for East Asian typography)
<s>	Defines text that is no longer correct
<samp>	Defines sample output from a computer program
<small>	Defines smaller text
<strike>	Not supported in HTML5. Use <del> or <s> instead. Defines strikethrough text
	Defines important text
<sub>	Defines subscripted text
<sup>	Defines superscripted text
<template>	Defines a container for content that should be hidden when the page loads
<time>	Defines a specific time (or datetime)
<tt>	Not supported in HTML5. Use CSS instead. Defines teletype text
<u>	Defines some text that is unarticulated and styled differently from normal text
<var>	Defines a variable
<wbr>	Defines a possible line-break

Table B-3 HTML color codes

Color name	HEX	RGB	Color name	HEX	RGB
AliceBlue	F0F8FF	240,248,255	LightSkyBlue	87CEFA	135,206,250
AntiqueWhite	FAEBD7	250,235,215	LightSlateGray	778899	119,136,153
Aqua	00FFFF	0,255,255	LightSteelBlue	B0C4DE	176,196,222
Aquamarine	7FFFD4	127,255,212	LightYellow	FFFFE0	255,255,224
Azure	F0FFFF	240,255,255	Lime	00FF00	0,255,0
Beige	F5F5DC	245,245,220	LimeGreen	32CD32	50,205,50
Bisque	FFE4C4	255,228,196	Linen	FAF0E6	250,240,230
Black	0	0,0,0	Magenta	FF00FF	255,0,255
BlanchedAlmond	FFEBCD	255,235,205	Maroon	800000	128,0,0
Blue	0000FF	0,0,255	MediumAquaMarine	66CDAA	102,205,170
BlueViolet	8A2BE2	138,43,226	MediumBlue	0000CD	0,0,205
Brown	A52A2A	165,42,42	MediumOrchid	BA55D3	186,85,211
BurlyWood	DEB887	222,184,135	MediumPurple	9370DB	147,112,219
CadetBlue	5F9EA0	95,158,160	MediumSeaGreen	3CB371	60,179,113
Chartreuse	7FFF00	127,255,0	MediumSlateBlue	7B68EE	123,104,238
Chocolate	D2691E	210,105,30	MediumSpringGreen	00FA9A	0,250,154
Coral	FF7F50	255,127,80	MediumTurquoise	48D1CC	72,209,204
CornflowerBlue	6495ED	100,149,237	MediumVioletRed	C71585	199,21,133
Cornsilk	FFF8DC	255,248,220	MidnightBlue	191970	25,25,112
Crimson	DC143C	220,20,60	MintCream	F5FFFA	245,255,250
Cyan	00FFFF	0,255,255	MistyRose	FFE4E1	255,228,225
DarkBlue	00008B	0,0,139	Moccasin	FFE4B5	255,228,181
DarkCyan	008B8B	0,139,139	NavajoWhite	FFDEAD	255,222,173
DarkGoldenRod	B8860B	184,134,11	Navy	80	0,0,128
DarkGray	A9A9A9	169,169,169	OldLace	FDF5E6	253,245,230
DarkGreen	6400	0,100,0	Olive	808000	128,128,0
DarkKhaki	BDB76B	189,183,107	OliveDrab	6B8E23	107,142,35

Table B-3 HTML color codes (continued)

Color name	HEX	RGB	Color name	HEX	RGB
DarkMagenta	8B008B	139,0,139	Orange	FFA500	255,165,0
DarkOliveGreen	556B2F	85,107,47	OrangeRed	FF4500	255,69,0
DarkOrange	FF8C00	255,140,0	Orchid	DA70D6	218,112,214
DarkOrchid	9932CC	153,50,204	PaleGoldenRod	EEE8AA	238,232,170
DarkRed	8B0000	139,0,0	PaleGreen	98FB98	152,251,152
DarkSalmon	E9967A	233,150,122	PaleTurquoise	AFEEEE	175,238,238
DarkSeaGreen	8FBC8F	143,188,143	PaleVioletRed	DB7093	219,112,147
DarkSlateBlue	483D8B	72,61,139	PapayaWhip	FFEFD5	255,239,213
DarkSlateGray	2F4F4F	47,79,79	PeachPuff	FFDAB9	255,218,185
DarkTurquoise	00CED1	0,206,209	Peru	CD853F	205,133,63
DarkViolet	9400D3	148,0,211	Pink	FFC0CB	255,192,203
DeepPink	FF1493	255,20,147	Plum	DDA0DD	221,160,221
DeepSkyBlue	00BFFF	0,191,255	PowderBlue	B0E0E6	176,224,230
DimGray	696969	105,105,105	Purple	800080	128,0,128
DodgerBlue	1E90FF	30,144,255	RebeccaPurple	663399	102,51,153
FireBrick	B22222	178,34,34	Red	FF0000	255,0,0
FloralWhite	FFFAF0	255,250,240	RosyBrown	BC8F8F	188,143,143
ForestGreen	228B22	34,139,34	RoyalBlue	4.17E+04	65,105,225
Fuchsia	FF00FF	255,0,255	SaddleBrown	8B4513	139,69,19
Gainsboro	DCDCDC	220,220,220	Salmon	FA8072	250,128,114
GhostWhite	F8F8FF	248,248,255	SandyBrown	F4A460	244,164,96
Gold	FFD700	255,215,0	SeaGreen	2E8B57	46,139,87
GoldenRod	DAA520	218,165,32	SeaShell	FFF5EE	255,245,238
Gray	808080	128,128,128	Sienna	A0522D	160,82,45
Green	8000	0,128,0	Silver	C0C0C0	192,192,192
GreenYellow	ADFF2F	173,255,47	SkyBlue	87CEEB	135,206,235
HoneyDew	F0FFF0	240,255,240	SlateBlue	6A5ACD	106,90,205
HotPink	FF69B4	255,105,180	SlateGray	708090	112,128,144
IndianRed	CD5C5C	205,92,92	Snow	FFFAFA	255,250,250
Indigo	4B0082	75,0,130	SpringGreen	00FF7F	0,255,127
Ivory	FFFFF0	255,255,240	SteelBlue	4682B4	70,130,180
Khaki	F0E68C	240,230,140	Tan	D2B48C	210,180,140
Lavender	E6E6FA	230,230,250	Teal	8080	0,128,128
LavenderBlush	FFF0F5	255,240,245	Thistle	D8BFD8	216,191,216
LawnGreen	7CFC00	124,252,0	Tomato	FF6347	255,99,71
LemonChiffon	FFFACD	255,250,205	Turquoise	40E0D0	64,224,208
LightBlue	ADD8E6	173,216,230	Violet	EE82EE	238,130,238
LightCoral	F08080	240,128,128	Wheat	F5DEB3	245,222,179
LightCyan	E0FFFF	224,255,255	White	FFFFFF	255,255,255
LightGoldenRodYellow	FAFAD2	250,250,210	WhiteSmoke	F5F5F5	245,245,245
LightGray	D3D3D3	211,211,211	Yellow	FFFF00	255,255,0
LightGreen	90EE90	144,238,144	YellowGreen	9ACD32	154,205,50
LightPink	FFB6C1	255,182,193	. . .	. . .	. . .
LightSalmon	FFA07A	255,160,122	. . .	. . .	. . .
LightSeaGreen	20B2AA	32,178,170	. . .	. . .	. . .

Appendix C. Sample Library Device Hypertext Markup Language (HTML) Description

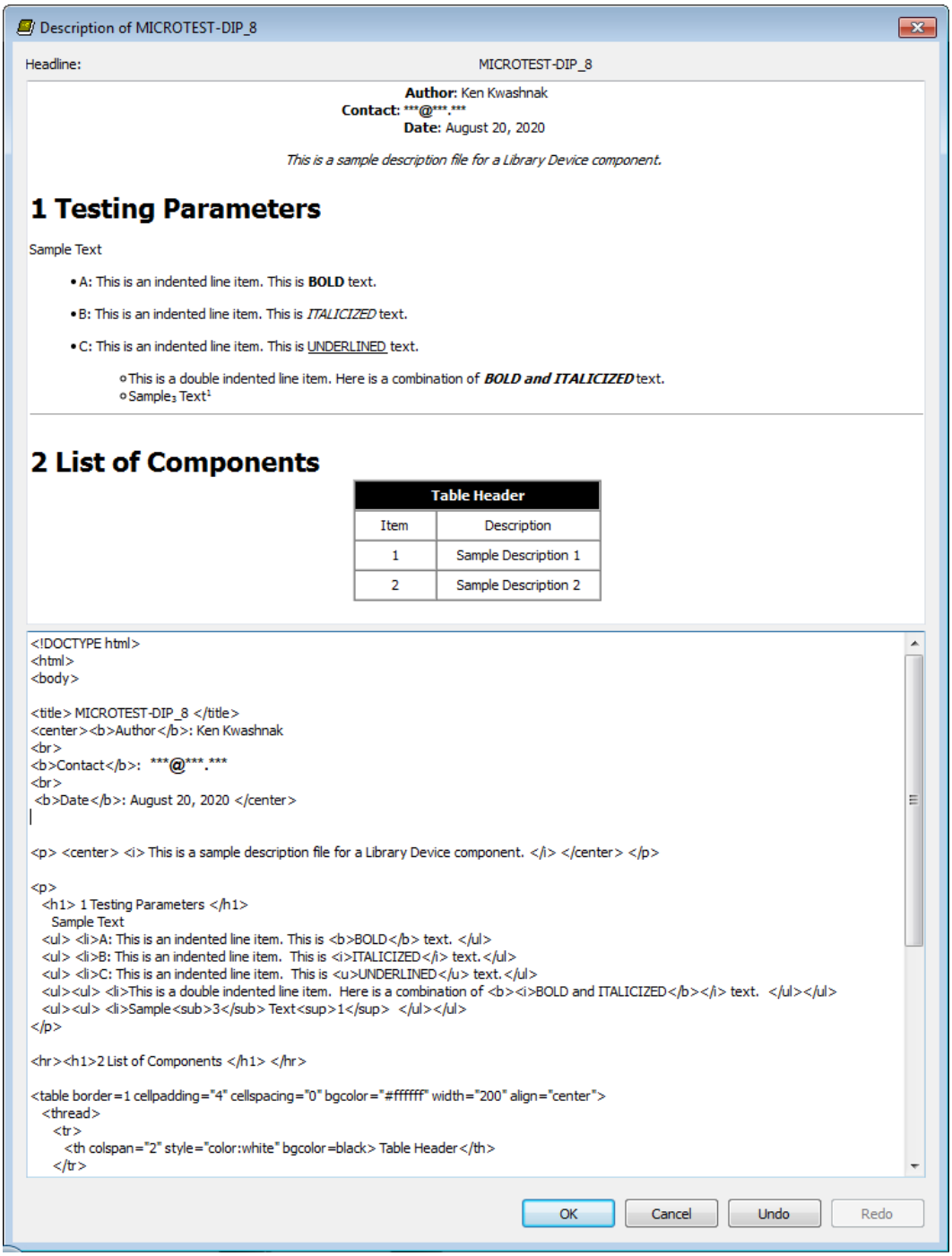

Fig. C-1 Hypertext Markup Language (HTML) example

```
<!DOCTYPE html>
<html>
<body>
<title> MICROTEST-DIP_8 </title>
<center><b>Author</b>: Ken Kwashnak
<br>
<b>Contact</b>: ***@***.***
<br>
<b>Date</b>: August 20, 2020 </center>
<p> <center> <i> This is a sample description file for a Library Device component. </i>
</center> </p>
<p>
<h1> 1 Testing Parameters </h1>
Sample Text
<ul> <li>A: This is an indented line item. This is <b>BOLD</b> text. </ul>
<ul> <li>B: This is an indented line item. This is <i>ITALICIZED</i> text.</ul>
<ul> <li>C: This is an indented line item. This is <u>UNDERLINED</u> text.</ul>
<ul><ul> <li>This is a double indented line item. Here is a combination of <b><i>BOLD
and ITALICIZED</b></i> text. </ul></ul>
<ul><ul> <li>Sample<sub>3</sub> Text<sup>1</sup> </ul></ul>
</p>
<hr><h1>2 List of Components </h1> </hr>
<table   border=1   cellpadding="4"   cellspacing="0"   bgcolor="#ffffff"   width="200"
align="center">
<thread>
<tr>
<th colspan="2" style="color:white" bgcolor=black> Table Header</th>
</tr>
</thread>
<tbody>
<tr>
<td> <center>Item</center></td>
<td><center>Description</center></td>
</tr>
<tr>
<td> <center>1</center></td>
<td><center>Sample Description 1</center></td>
</tr>
<tr>
<td> <center>2</center></td>
<td><center>Sample Description 2</center></td>
</tr>
</tbody>
</table>
<!--This is a comment-->
</body>
</html>
```

Code block 6 HTML code for sample library device description

Appendix D. Advanced Circuits Manufacturing Specifications

This appendix contains Advanced Circuits manufacturing specifications for the two-layer printed circuit board (PCB) listed in Table D-1.[1]

Table D-1 Advanced circuits manufacturing specifications

Rule	Value	Unit
Inner layer clearance	0.010	Inch
Copper to edge of PCB, outer layers	0.010	Inch
Copper to edge of PCB, inner layers	0.015–0.020[a]	Inch
Scoring, outer layers	0.015	Inch
Scoring, inner layers	0.020	Inch
Pad size/annular ring	0.010 over finished hole size for vias 0.014 over finished hole size for components	Inch
Hole size, tolerance	0.003–0.005	Inch
Hole size, minimum	0.004	Inch
PCB tolerance	10	%
Minimum	0.005	Inch
Board thickness		Inch
2-Layer	0.020	
4-Layer	0.020	
6-Layer	0.031	
8-Layer	0.047	
10-Layer	0.062	
Rout (board outline)	0.005[b]–0.010	Inch
Copper spacing[c]		Inch
1 oz finished copper weight (inner layers)	0.003 0.005	
2 oz finished copper weight (inner & outer)	0.009 0.010	
3 oz finished copper weight (inner & outer)		
4 oz finished copper weight (inner & outer)		
Copper trace width/air gap[c]	20 0.002	% Inch
Copper thickness, maximum	20	oz
Slot width	Custom—0.031[a]	Inch
Tab rout	0.100	Inch
Silkscreen (legend)	0.005 minimum	Inch
Bevel options	20 30[a] 45	Degree
Acceptability standard	IPC A600 class 2 through IPC 6012 class 3A	
Underwriter's laboratory approval	Yes	
CAM software used	Frontline's genesis	

[a] preferred
[b] special request
[c] premium charge for trace width/spacing less than 0.007 inch. Will process .004 in for 1 oz. CU. finished (outer layers) and 0.5 oz. CU finished (inner layers)

[1] Advanced circuits specs. Advanced circuits; 2020 [Accessed 2020 Oct 8]. https://www.4pcb.com/pcb-prototype-2-4-layer-boards-specials.html.

Appendix E. Oshpark Manufacturing Specifications

This appendix contains Oshpark manufacturing specifications for the two-layer printed circuit board (PCB).[1]

E.1 Two-Layer 2-oz 0.8-mm Service

The PCB is a special stackup intended for a variety of high-power and low-weight circuit designs. This service features a 0.032-inch (0.8-mm)-thick PCB, and includes 2-oz (2.8-mil, 70-um) copper.

E.2 Pricing

The pricing is $5 per square inch, which includes three copies of your design. For example, a 2-square-inch board would cost $10 and you would get three copies of your board. You can order as many copies as you want, as long as they are in multiples of three.

E.3 Turn Times

Orders are sent to fabrication every week and have a turnaround time from the fabrication of 1 week.

E.4 Fabrication Specs

E.4.1 Common Specs

Spec	Value
Manufactured in the United States	Yes
Lead Free compatible	Yes
RoHS complaint	Yes
High temp	Yes, 175 Tg or higher (see Material Specs)
PCB finish	ENIG (Gold), compliant with IPC-4552
Soldermask type	SMOBC (Soldermask over bare copper), both sides
Silkscreen type	High res DLP, both sides

[1] Services. Oshpark; 2017. [accessed 2020 Oct 8]. https://docs.oshpark.com/services/two-layer-hhdc/.

E.4.2 Stackup

Thickness	Layer	Tolerance
1 mil (0.0254 mm)	Silkscreen	+/-0.2 mil (0.00508 mm)
1 mil (0.0254 mm)	Solder resist	+/-0.2 mil (0.00508 mm)
2.8 mil (0.0711 mm)	2-oz copper	. . .
30 mil (0.762 mm)	Core	+/-3 mil (0.0762 mm)
2.8 mil (0.0711 mm)	2-oz copper	. . .
1 mil (0.0254 mm)	Solder resist	+/-0.2 mil (0.00508 mm)
1 mil (0.0254 mm)	Silkscreen	+/-0.2 mil (0.00508 mm)

E.4.3 Material Specs

Spec	Value
Substrate	175 Tg FR4
Board thickness	32 mil (0.8 mm) nominal
Dielectric	4.5 at 10 Mhz
Soldermask color	Purple
Minimum soldermask web	4 mil (0.1016 mm)
Maximum soldermask alignment	3 mil (0.0762 mm)
Silkscreen minimum line width	5 mil (0.127 mm) (recommended minimum) 3 mil (0.0762 mm) (short lines, text, graphics)
Maximum board size	16 inch (406.4 mm) by 22 inch (558.8 mm)
Minimum board size	0.25 inch (6.35 mm) by 0.25 inch (6.35 mm)

E.4.4 Copper Specifications

Spec	Value
Copper layers	2
Copper weight	2 oz
Trace spacing	6 mil (0.1524 mm)
Trace width	6 mil (0.1524 mm)
Annular ring	5 mil (0.127 mm)
Board edge keepout	15 mil (0.381) from nominal board edge
Via plating thickness	1 mil (0.0254 mm)

E.4.5 Drill Specifications

Spec	Value
Minimum annular ring	5 mil (0.127 mm)
Minimum drill size	10 mil (0.254 mm)
Minimum slot size	20 mil (0.508 mm) (drill slot only)
Drill size tolerance	Max: +/- 2.5 mil (0.0635 mm) Typical: +/- 1.0 mil (0.0254)
Drill positional tolerance	Max: 2 mil (0.0508 mm) Typical: <1 mil (0.0254 mm)
Via tenting	Yes (filled hole and flat surface not guaranteed)
Buried via	No
Blind via	No
Overlapping drills	Allowed, but not guaranteed. May result in missing or slotted holes. 5 mil (0.127 mm) clearance is recommended between holes.
Castellations	Allowed, but not guaranteed
Maximum drill size	None

Additional Reading

Schematics

Jimblom. How to read a schematic. Sparkfun Electronics; n.d. [accessed 2020 Nov 23]. https://learn.sparkfun.com/tutorials/how-to-read-a-schematic/all.

Board Materials

Peterson Z. PCB core versus prepreg material: what designers need to know. Altium; 2020 Jan 17 [accessed 2020 Aug 27]. https://resources.altium.com/p/pcb-core-vs-prepreg-material-what-designers-need-to-know.

EAGLE Software Manual

CadSoft. EAGLE manual version 5. Pembroke Pines (FL): CadSoft Computer; 2010 [accessed 2020 Aug 31]. 7th Edition. Also available at www.hades.mech.northwestern.edu/images/b/b4/Eagle_Manual.pdf.

List of Symbols, Abbreviations, and Acronyms

3-D	three-dimensional
CAD	computer-aided design
CD	compact disc
COTS	commercial off the shelf
DIP	dual inline package
DRC	Design Review Check
EAGLE	easily applicable graphical layout editor
eCAD	electrical computer-aided design
eCAM	electrical computer-aided manufacturing
ESD	electro-static discharge
EULA	End User License Agreement
GND	ground
HTML	Hypertext Markup Language
IC	integrated circuit
IDE	Integrated Development Environment
LED	light-emitting diode
OS	operating system
PCB	printed circuit board
PWM	pulse width modulation
SMD	surface mount device
ULP	user language program

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