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14. ABSTRACT
This Test Operations Procedure (TOP) defines specifications and describes test methods used by the U.S. Army Aberdeen Test Center (ATC) for measuring the performance of electronic waveform digitizing systems, but the procedures could be tailored to be used at other test facilities. The TOP is directed toward, but not restricted to, general-purpose waveform recorders and analyzers.

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U.S. ARMY TEST AND EVALUATION COMMAND
TEST OPERATIONS PROCEDURE

*Test Operations Procedure 02-2-632 8 December 2020
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DATA ACQUISITION SYSTEM (DAS) TEST PROCEDURES

1. SCOPE.

a. This Test Operations Procedure (TOP) defines specifications and describes test methods used by the U.S. Army Aberdeen Test Center (ATC) for measuring the performance of electronic waveform digitizing systems, but the procedures could be tailored to be used at other test facilities. The TOP is directed toward, but not restricted to, general-purpose waveform recorders and analyzers. Both in-house ATC waveform recorder characterization techniques and the Institute of Electrical and Electronics Engineers (IEEE) Standard 1057-2007[**1] (Standard for Digitizing Waveform Recorders) techniques are utilized in this document.

b. It is important to thoroughly test a Data Acquisition System (DAS) unit before purchasing to make sure the DAS responds as expected and there are no major limitations in the areas of most concern. Manufacturers will generally test a DAS under laboratory conditions, which are not necessarily how a DAS will be used in its everyday environment. It is important to thoroughly evaluate a system (before or after purchase) instead of relying on the manufacturers stated specifications. Many of the Army’s ballistic testing requirements are congressionally mandated and require instrumentation to be evaluated before it can be used to acquire data. Requirements are explained in detail in the U.S. Army Test and Evaluation Command (ATEC) Regulation 73-1[2]. This TOP is provided to ensure that Army personnel have a well-defined set of specifications and test methods that can easily be used to evaluate and compare the performance of new and past recorders using a common test set and language. These tests do not need to be conducted in any specific order, each test is its own standalone procedure.

** Superscript numbers correspond to Appendix F, References.

2. TEST EQUIPMENT.

The data acquisition market has been steadily improving in performance from the 1980's until today. Today's modern Analog-to-Digital Converters (ADCs) have faster conversion speeds, higher resolutions, and significantly lower price points. Lower ADC prices have facilitated the integration of signal conditioning features onto data acquisition devices to improve accuracy and ease of use. Signal conditioning features such as amplifiers, filters, and sensor-specific circuitry on data acquisition devices further improve their accuracy and simplify connectivity for the users. On the back-end, onboard field-programmable gate arrays have allowed DASs to become small and very flexible allowing for inline signal processing and data reduction. The increased flexibility of these devices makes them ideal for custom data acquisition requirements and embedded applications. With all of these enhancements driving orders of magnitude improvement in the DAS industry, the test equipment industry has struggled to keep pace of late. At times, it seems the data acquisition systems will soon outpace the test instruments used to evaluate them. ATC adheres to the rule of thumb that the test instrumentation must have a 10x greater resolution than the waveform recorder being characterized. The test equipment specifications outlined in this section are not necessarily the most stringent available but are intended as a minimum performance guide to aim for when choosing test instrumentation. Table 1 is a list of important instrument specifications used for waveform recorder characterization.

TABLE 1. MINIMUM SPECIFICATIONS

INSTRUMENTATION	SPECIFICATION	MINIMUM PERFORMANCE
Function Generator (Sine Wave Generation)	Amplitude Accuracy	±0.1 decibel (dB) (1%)
	Frequency Accuracy	30 parts per million (0.003%)
	Total Harmonic Distortion	-110 dB
Digital Multimeter	Resolution	6 ½ digits
	Accuracy @ (10 Volts Direct Current (VDC))	0.0016% of reading
	Accuracy @ (10 Hertz (Hz) - 20 kilohertz (kHz) Alternating Current (AC))	0.04% of reading
Time Counter	Speed	12 digits/sec
	Resolution	20 ps single-shot
Time Reference	Time Resolution	0.2 nanosecond (ns)
Inductance, Capacitance, Resistance (LCR) Meter	Basic Accuracy	0.1%

3. TERMINOLOGY EXPLANATION.

This Section is provided to explain what is actually meant by certain electronic terminology used in this document that is often used by other disciplines, fields, and in other practices, with different or slightly different meanings. All of the terminology used in Section 4, Test Methods, is explained in paragraphs 3.1 - 3.7.

3.1 Input Amplitude.

a. The voltage for AC waveforms shown in Figure 1 can be expressed a few different ways, peak (Vp), peak-to-peak (Vpp), and/or Root Mean Square (Vrms). Peak amplitude is typically represented as the greatest positive (+Vp) value, but it may also be the most negative peak (-Vp) of the waveform. For a sine wave, Vp is always one half Vpp. Peak-to-peak amplitude is the difference between the highest value (+Vp) and the lowest value (-Vp) of the waveform. The RMS value is defined as the square root of the mean over time of the square of the value from a zero average reference. For a sinewave, this value is calculated as $Vp / \sqrt{2}$.

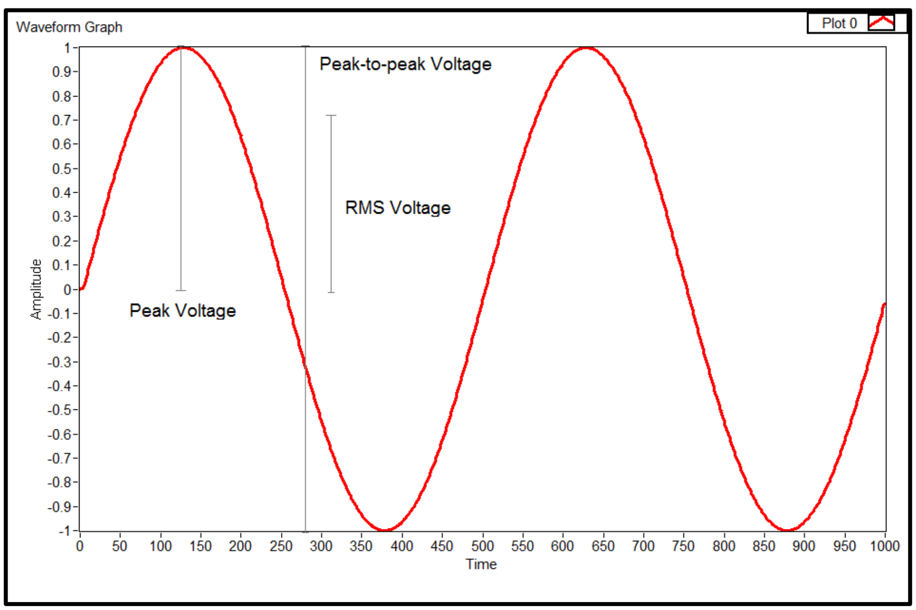

Figure 1. Amplitude example.

b. RMS values are important when evaluating instrumentation, but due to the nature of ballistic shock impulse peak or peak-to-peak may be considered more important.

c. Throughout this document, amplitudes may be expressed in percentage of full-scale (FS) with respect to the input range of the waveform recorder under test. Typically, systems are evaluated at 90 percent of the full scale input range which normally equates to a worst case measurement. For example, a ±10 Vp waveform recorder has a full scale of 20 Vpp. Ninety percent of full scale is 18 Vpp, ±9 Vp, and 6.36Vrms.

3.2 Input Frequency.

a. Frequency is defined as the number of cycles per second (Hz) in an AC sinewave. The sinewave period is defined as the time of one cycle, and its value is the reciprocal of the frequency. Figure 2 shows a 1 kHz sinewave with its frequency and period indicated. An AC sinewave from an external source consists of a frequency (*f*) and voltage (*v*). The input frequency and the input voltage are typically referenced as f_{in} and v_{in} and come from an external source such as a function generator.

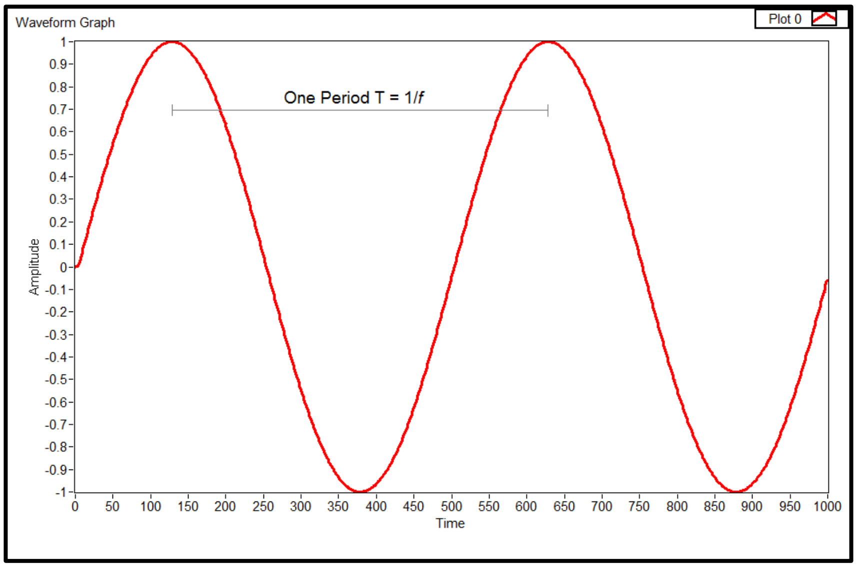

Figure 2. Frequency example.

b. The term Bandwidth (BW) will be referenced many different times with many different applications, but all bandwidth definitions reference the ability of a particular transmission line to pass the information or product. For example: for a given water pipe the bandwidth is measured in gallons per minute, and for analog applications bandwidth is measured in Hz. Throughout this TOP the analog application will be used most often, so bandwidth will be referenced in Hz, and is defined as the difference between the lower frequency and the upper frequency of a continuous waveform. A systems passband is the difference between the lower cutoff frequency and the upper cutoff frequency. The cutoff frequency is the point where the signal is 3 dB down from the input voltage. Figure 3 shows how bandwidth is measured where f_L and f_H and the lowest and highest frequencies the transmission line or system can pass. Generally, all applications within this document will reference low pass filters, so f_L will equal zero (DC).

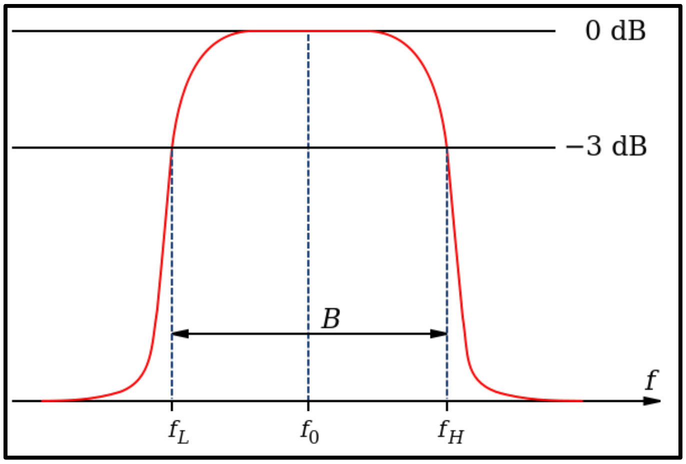

Figure 3. Bandwidth measurement.

c. The frequency of an input waveform for testing purposes should be chosen relative to the sample rate and bandwidth restrictions of the waveform recorder or item under test. For tests where the input frequency of the waveform is not critical, but the amplitudes of the measurement are critical, choose test frequencies well within the passband of the test item. A typical rule of thumb is to choose an input frequency that is approximately 10 percent of the stated BW. Some tests will note that a frequency selection is critical to the test and state the input frequency must be relatively prime to the sample rate (SR) chosen. This is done to prevent harmonics and other undesired results. Relatively prime does not mean that the parameters chosen must be prime numbers but rather the numbers are prime to each other. Two numbers are relatively prime when their common divisor is one. Use Equation 1 to determine f_{in} from an approximate input frequency. All math is integer math with the exception of the final product.

$$fin = \frac{J}{M} fs \qquad \textit{(Equation 1)}$$

where:

M is the record length that is a power of 2 (2^5, 2^6, … 2^n)
J is an integer odd number of cycles within M
f_s is the sample rate

example:

Choose an approximate input frequency f_a (400Hz)
Choose record length M (2^{16} = 65536 samples)
Choose the SR (40000 samples/sec)
Determine the number of cycles (J) $J = \frac{M}{SR} fa$, $J = \frac{65536}{40000} 400 = 655\ cycles$
Determine $fin = \frac{655}{65536} 40000 = 399.78 Hz$

The input frequency of 399Hz is relatively prime to the sample rate of 40 kilo Samples per second (kS/s).

3.3 Sample Rate.

a. Sample rate is the rate at which the waveform recorder converts the analog input signal to digital data. Sample rate is measured in samples per second. Higher sample rates can record higher frequencies. The Nyquist criterion states the sample rate must be at least two times the input frequency to correctly determine the waveform frequency, but in order to reconstruct the waveform and provide accurate peak measurements, a higher sample rate must be used. If the sampling rate is not specified, then the general guideline is to set the sampling rate 10x higher than the filter cutoff frequency chosen.

b. The equation to determine the relationship between sampling rate and peak measurement error for a sinusoidal signal is shown in Equation 2.

$$\%Error = 100 * (1 - cos\frac{2\pi F}{2f}) \qquad \textit{(Equation 2)}$$

where:

F	Signal Bandwidth Frequency
f	Sample Rate
Note:	Remember to use radians when calculating

c. The equation can be transformed (Equation 3) to calculate the minimum sampling rate required for a specific acceptable error value and frequency bandwidth.

$$f = \frac{F\pi}{cos^{-1}\left(1-\frac{\%error}{100}\right)} \qquad \textit{(Equation 3)}$$

d. For a maximum allowable error of 10 percent in any amplitude measurement, a sampling rate of 7x the signal bandwidth is necessary. The relationship between the sample time and the time of the analog signal peak is random and thus the sample time may occur at any time during the signal cycle with equal probability. In other words, it is as likely that the sample time coincides with the true peak as it is that it coincides with a lowest value that results in a 10 percent error. This means that the average error expected would be 5 percent. Table 2 shows the error associated with a common anthropomorphic test dummy (ATD) metric (highlighted bold) and the effect of sampling on the maximum and average errors.

TABLE 2. PEAK ERROR

SAMPLE RATE	FREQUENCY BANDWIDTH	BW LIMIT SAMPLING FACTOR	MAXIMUM PERCENT ERROR	AVERAGE PERCENT ERROR
20 kS/s	4 kHz	5x	19.09%	9.54%
28 kS/s	4 kHz	7x	9.90%	4.95%
40 kS/s	**4 kHz**	**10x**	**4.89%**	**2.44%**
60 kS/s	4 kHz	15x	2.18%	1.09%
80 kS/s	4 kHz	20x	1.23%	0.61%
400 kS/s	4 kHz	100x	0.04%	0.02%

e. Take into account the errors in Table 2 are based purely on a sinusoidal waveform and do not accurately represent real ballistics data. The potential errors based on the sampling rate and filter BW may in fact be better or worse depending on the frequency content of the data being measured. For the most part, the signals of interest should fall well below the filter BW and would not produce errors anywhere near the levels listed in Table 2. See Appendix C for a more complete explanation of why this error occurs.

3.4 Record Length.

a. The record length is the number of samples collected on the waveform recorder. The record length divided by the sample rate gives the total time the waveform recorder recorded sampled data. For example, if a waveform recorder has a sample rate of 1 kS/s, a record length of 500 samples will record data for 0.5 seconds. Record length will determine the size of the digital file needed to store the data. For example, a record length of 500 samples at 16 bits per sample = 8000 bits = 1 kB. Keep in mind a waveform recorder may store other digital information resulting in larger file sizes.

b. The record length is often divided into pre-trigger and post-trigger segments. The trigger event is the marker between pre-trigger data and post-trigger data. Typically pre-trigger is set to a particular size and functions as a circular buffer that starts recording data when the system is armed and stops recording data when the trigger event occurs. When the pre-trigger recording stops, post-trigger recording starts and continues to record until the desired record length is achieved. Practically speaking the recording doesn't actually start and stop between pre-trigger and post-trigger. Only a marker is placed in the memory at the trigger point time and that marker is then used to reference the end of pre-trigger and start of post-trigger.

(1) Record Length = Pre-Trigger + Post-Trigger.

(2) Post-Trigger = Record Length – Marker (trigger point).

(3) Pre-Trigger = Record Length – Post-Trigger.

3.5 Filters.

a. A filter removes unwanted frequency components (stop band) from a signal while preserving the desired frequency components (pass band). A filter's pass band is the range of frequencies over which it will pass an incoming signal. The stop band is all frequencies that lie outside of the pass band and are attenuated. Most filters fall into one of the following four response categories, based on the overall shape of their pass band.

(1) Low-pass filters (Figure 4) pass low-frequency signals while blocking high-frequency signals. The pass band ranges from DC (0 Hz) to a corner frequency f_C.

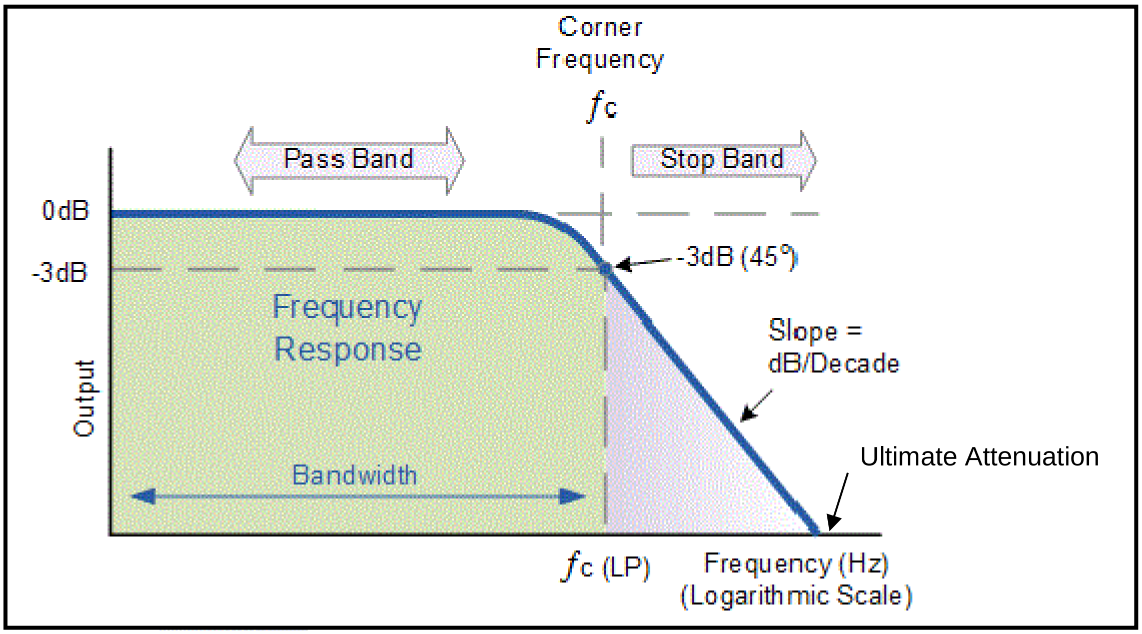

Figure 4. Low pass filter response.

(2) High-pass filters (Figure 5) pass high-frequency signals while blocking DC and low frequency signals. The pass band ranges from a corner frequency (f_C) to infinity.

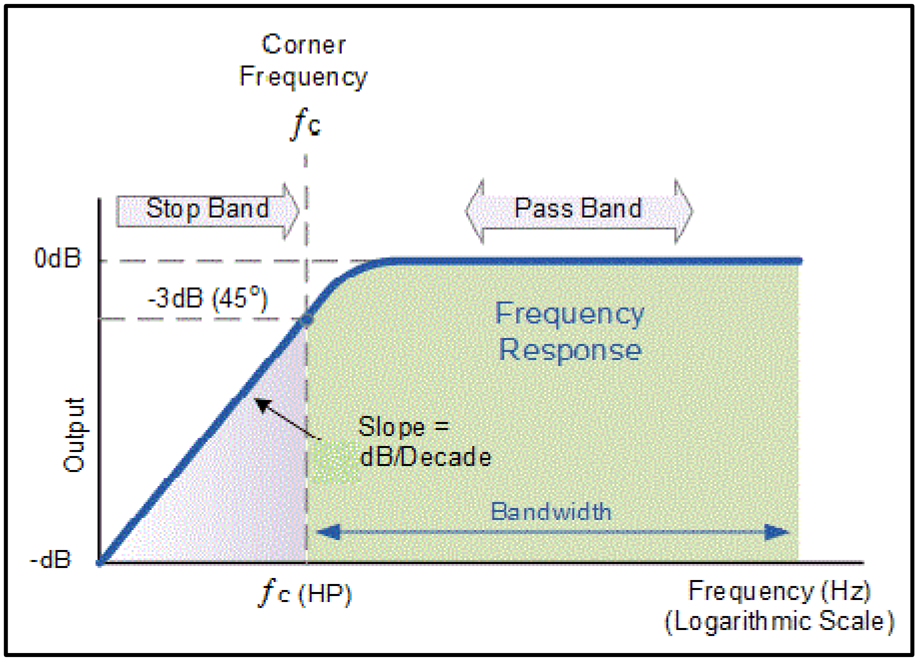

Figure 5. High pass filter response.

(3) Band-pass filters (Figure 6) pass only signals between two given frequencies, blocking lower and higher signals. The pass band lies between two frequencies, f_L and f_H. Signals between DC and f_L are blocked, as are signals from f_H to infinity. The pass band of these filters is often characterized as having a bandwidth that is symmetric around a center frequency.

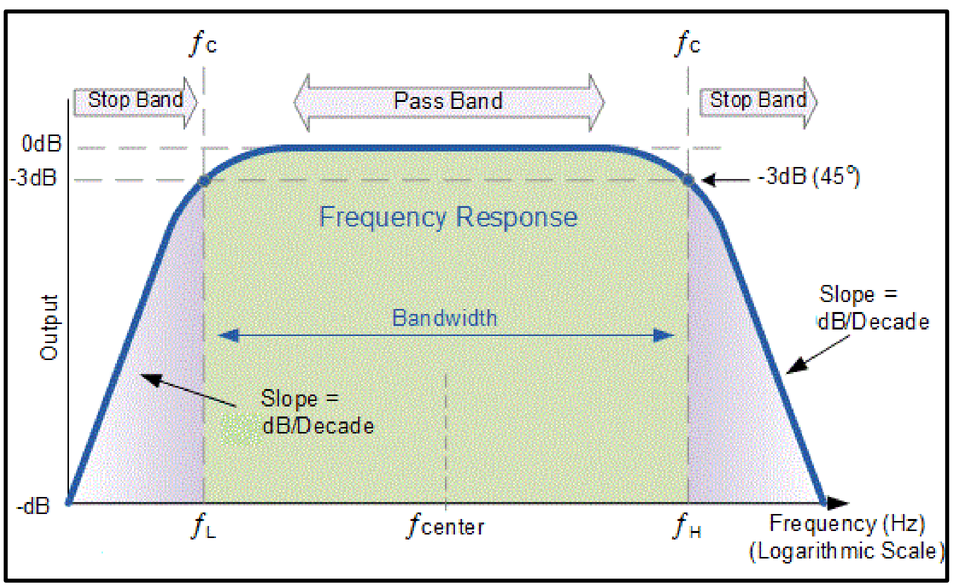

Figure 6. Band pass filter response.

(4) Band-stop filters (Figure 7) block signals occurring between two given frequencies, f_L and f_H. The pass band is split into a low side (DC to f_L) and a high side (f_H to infinity). For this reason, it is often simpler to specify a band-stop filter by the width and center frequency of its stop band. Band-stop filters are also called notch filters, especially when the stop band is narrow.

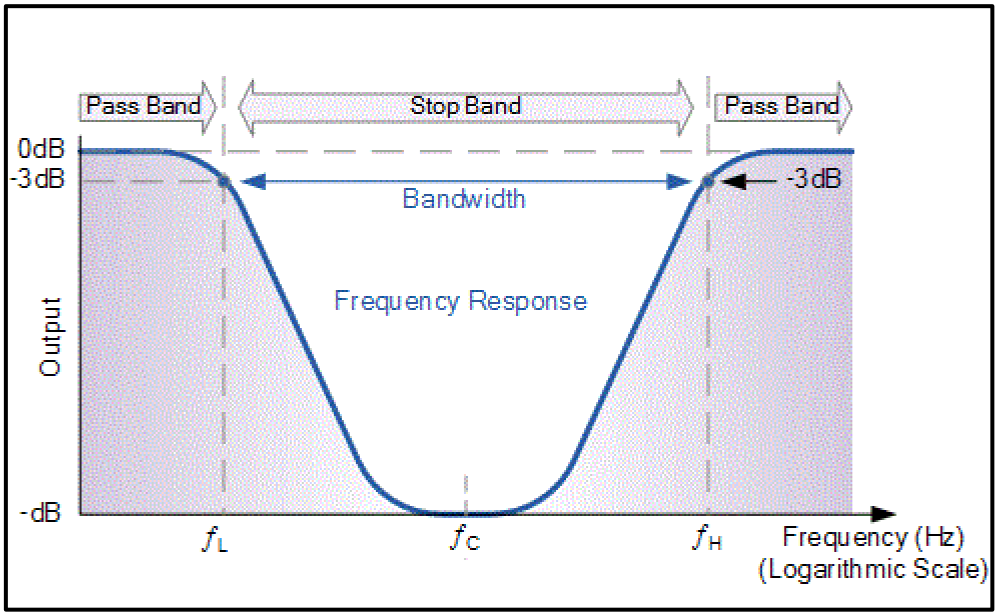

Figure 7. Band stop filter response.

b. The remainder of this document, when referencing a filter, will be referencing a low pass filter unless otherwise stated. The vast majority of DASs only incorporate built-in low pass filter options for noise rejection and anti-alias protection.

3.6 Load Termination.

Tests will state when the input should be terminated with a specific load and what the load value should be. Most tests require loads that are typical of the application, so using a realistic value indicative of a field transducer is always a good choice. If it is not possible to test all load configurations, choose the worst case option (largest load = lowest resistance) that is a realistic value for the system under test. For all tests in this document where a specific load is required the load will be either a 350 Ω signal resistor (Figure 8) or a 350 Ω Wheatstone bridge (Figure 9).

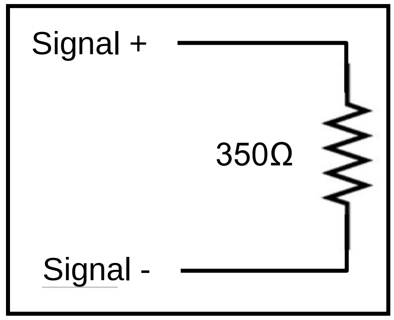

Figure 8. Single resistor load.

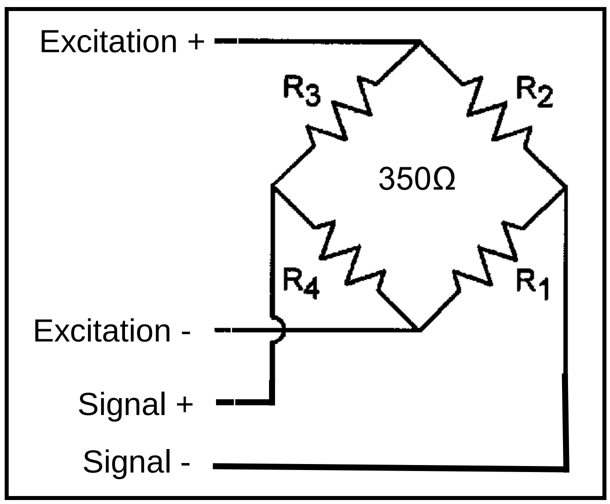

Figure 9. Wheatstone bridge load.

3.7 Input Modes and Input Types (Signal Conditioning).

a. The two most common inputs modes utilized in a DAS are single-ended input mode and differential input mode. A single-ended input has no common mode range because there is only one return (negative), shared by all positive inputs. In single-ended mode, the negative is typically referenced to analog ground. In differential input mode, the signal has both a positive and negative input for each channel and they are not referenced to analog ground, but are electrically floating with respect to ground. This provides superior common mode rejection whenever electromagnetic interference (EMI) or radio frequency interference is present. Differential input amplifiers reject common mode voltage, provided that the common mode voltage plus the input signal does not exceed the device's common mode rejection ratio (CMRR) specification. Figure 10 is a perfect example of the wanted high frequency signal riding on an unwanted lower frequency common mode signal.

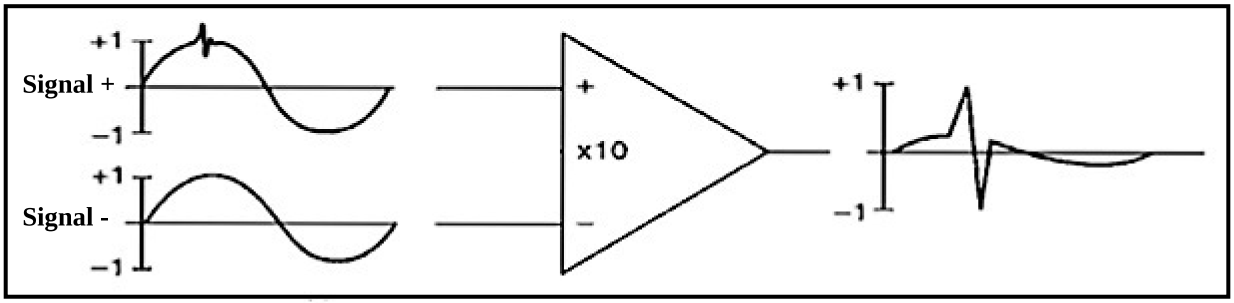

Figure 10. Common mode rejection example.

b. Notice the unwanted common mode signal is present on both the signal + and signal – input leads. A differential amplifier will reject the unwanted common mode signal and pass the wanted real data. A good CMRR is -80 dB or better.

c. The four most common input types are strain (or bridge), charge, Integrated Electronic PiezoElectric (IEPE), and voltage. Each input type interfaces with a certain type sensor, providing the signal conditioning needed for the chosen sensor.

(1) Bridge type signal conditioning is used for strain gages and/or piezoresistive sensors. A typical piezoresistive sensor has an output bridge resistance of 350 - 9,000 Ω. The resistance value most typically used is important to DAS evaluation, as the higher the bridge resistance, the higher the potential noise entering the system, and for field measurements the lower the potential bandwidth. For the bridge circuit to function, stable excitation must be present and a completion resistor circuit (module) may or may not be required. The use of bridge completion modules provide a convenient means for completing the Wheatstone Bridge circuit (used in strain gage measurements) but are typically not used in the evaluation of the DAS. However, it is becoming more common that systems are providing internal completion circuits and they should be validated. In addition, the excitation voltage and bridge balance adjustment circuitry is also commonly provided and should be validated.

(2) Charge type signal conditioning is used for piezoelectric charge mode sensors. Historically, these sensors were used on most if not all dynamic measurement applications until single crystal silicon became prevalent in the digital age. A charge mode sensor contains a piezoelectric sensing element (quartz crystal) that produces a small charge when compressed. A special charge amplifier is required to convert the charge to a voltage proportional to the input signal from the sensor. Charge amplifiers may be built into the DAS or reside outside the DAS. If they are built in they must be evaluated with the system taking into consideration the charge amplifiers time constant, frequency response, insulation resistance, and accuracy. If the amplifier is outside of the DAS, the signal is typically recorded in a voltage mode so no additional effort is required as far as the DAS is concerned.

(3) IEPE type signal conditioning uses charge type sensors incorporated with an integrated circuit (electronic amplifier) and powered with a constant current signal conditioner. This approach provides several improvements over the standard charge type measurement. IEPE signal conditioners may be built into the DAS or reside outside the DAS. If they are built in they must be evaluated with the system taking into consideration the signal conditioners time constant, frequency response, supply current, and accuracy. If the conditioner is outside of the DAS, the signal is typically recorded in a voltage mode so no additional effort is required as far as the DAS is concerned.

(4) Voltage type measurements are the least complicated measurements as they require no additional signal conditioning as with other sensor types. A simple voltage measurement can be directly connected to the DAS and recorded as long as the voltage being measured does not exceed the input range of the DAS.

4 TEST METHODS.

4.1 Noise.

Noise is a characteristic found in all electronics and it is typically represented by random fluctuation in the electrical signal (Figure 11). These fluctuations project errors and/or undesired random disturbances onto the real information of a signal. Noise is typically a summation of the unwanted or disturbing energy from natural and sometimes man-made sources. Unfortunately, measuring analog signals with a data acquisition device is not always as simple as wiring the signal source leads to the data acquisition device. Knowledge of the nature of the signal source, a suitable configuration of the data acquisition device, and an appropriate cabling scheme are required to produce accurate and “noise-free” measurements as possible. The integrity of the acquired data depends upon the entire analog signal path. In order to cover a wide variety of applications, most data acquisition devices provide flexibility in their analog input stage configuration. The price of this flexibility is that it can sometimes produce unwanted noise. It is important to know as much as possible about the amplitude aspect of a systems noise to determine the smallest useable range. For example, if the system exhibits up to ±5 µV of vertical noise and the waveform being recorded measures only 20 μV_p, the peak of the recorded waveform could actually be anywhere from 15 μV_p up to 25 μV_p depending on when the sample is actually taken. The following noise tests unfortunately only characterize the noise of the DAS and not the potential man-made noise caused by the test setup or less than ideal use of the DAS. Currently ATC uses two different methods to measure noise. The Baseline Noise test method measures the noise present on the system with the input leads (Signal + and Signal -) tied together through a load. The System Noise test method allows the noise to be measured over the full range of the DAS.

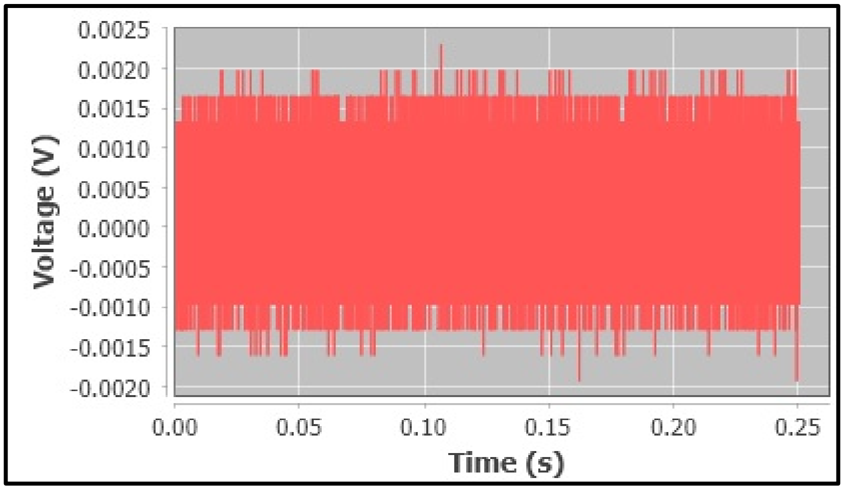

Figure 11. Random noise.

4.1.1 Baseline Noise - Test Method.

The Baseline Noise test method is used to determine maximum peak-to-peak, RMS, and frequency content of the noise as well as the distribution of the noise data (Histogram) of the DAS at baseline with no connections to a signal source. Using this method, the input is terminated with a load resistor typical of a common bridge resistance used in testing. Data are collected over a short period of time to avoid drift (about 1.0 s or a typical length of the intended applications). This test is performed on each channel, at each gain, and then averaged together for an overall system noise specification.

4.1.1.1 Test Setup.

The test setup and procedures are shown in Figure 12 and Table 3.

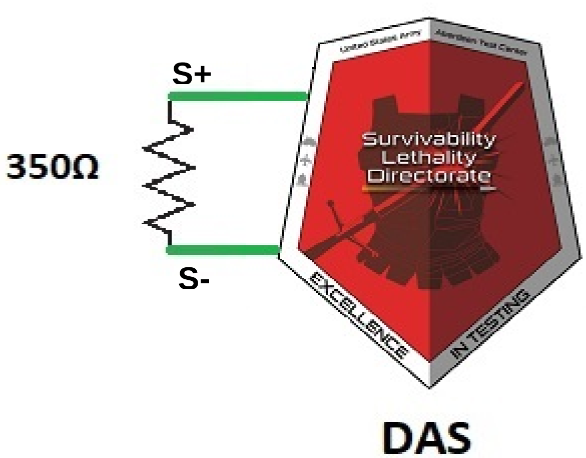

Figure 12. Baseline noise test setup.

TABLE 3. BASELINE NOISE TEST PROCEDURES

<table>
<tr><th colspan="3">BASELINE NOISE

Test Standard: ATC</th></tr>
<tr><td colspan="2">Equipment Needed:
• DAS
• Input Load Resistor (Typically 350 Ω)</td><td>Connections Needed
• Connect Load to the input channel(s) as indicated in Figure 12, clip leads are acceptable</td></tr>
<tr><th>Step</th><th>Action</th><th>Parameters</th></tr>
<tr><td>1</td><td>Make Connections</td><td>N/A</td></tr>
<tr><td>2</td><td>Set DAS Parameters</td><td>Trigger: Set to manual
Gain/Range: Unity
Sample Rate: Max
Filters: None</td></tr>
<tr><td>3</td><td>Acquire Data</td><td>Typically 1s or less</td></tr>
<tr><td>4</td><td>Analyze Data</td><td>See Analysis Section 4.1.1.2</td></tr>
<tr><td>5</td><td>Repeat steps 2-4 for each Gain/Range and different resistive loads (if desired)</td><td>N/A</td></tr>
</table>

4.1.1.2 Analysis.

a. For each channel, determine the Vpp, and Vrms noise levels over the entire record length. The peak-to-peak noise is the difference between the overall maximum and overall minimum peaks measured.

(1) A Fast Fourier Transform (FFT) will show the frequency content of the noise for each channel.

(2) The histogram will show noise distribution for each channel.

b. Determine if the noise is correlated or uncorrelated.

(1) -1 = never occurs together (correlated).

(2) 0 = absolutely independent (uncorrelated).

(3) +1= always occurs together (correlated).

c. Repeat for each gain/range setting.

4.1.1.3 Results.

a. The results from the analysis should be placed in a table to show the average channel Vpp, Vrms, max frequency content, and correlation for the noise at each gain/range level. Frequency content can indicate unwanted noise pollution caused by environmental factors not attributed to the DAS. A histogram of the noise data for each measurement will show the distribution of the data related to each channel. This distribution should be uniform around 0 volts, indicating random noise patterns. A typical distribution is shown in Figure 13. The histogram only needs to be done once for each channel.

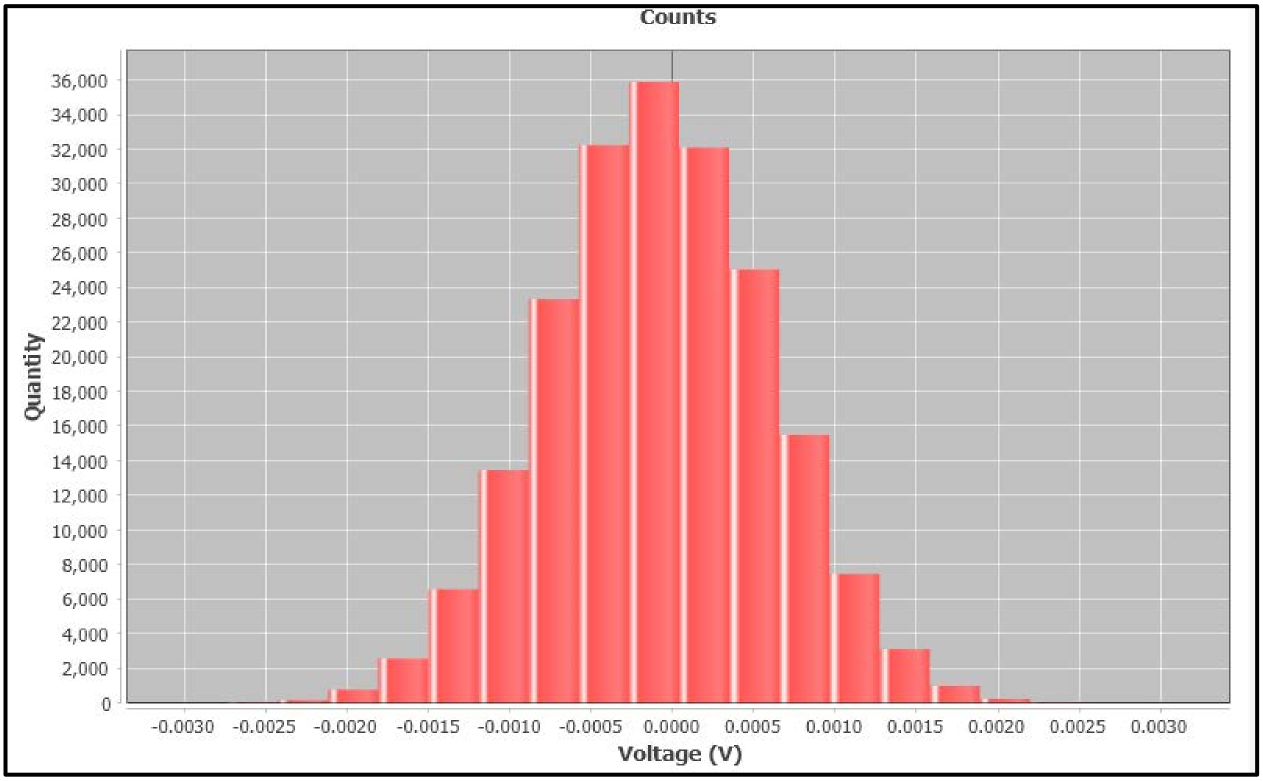

Figure 13. Typical distribution of data related to each channel.

b. If counts are not available, selecting the appropriate amount of bins for the histogram will be difficult. A good rule of thumb for Vpp noise is shown in Table 4.

TABLE 4. Vpp NOISE RULE OF THUMB

SAMPLE RATE	NOISE
100 kHz	5.0 m Vpp
10 kHz	1.5 m Vpp
1 kHz	350 μ Vpp

4.1.2 System Noise - IEEE 1057 Test Method.

The IEEE 1057 - 2007 noise test method described in paragraph 4.1.2.3 provides the ability to determine the systems Signal to Noise Ratio (SNR), and the Ratio of Signal to Noise and Distortion (SINAD). Both ratios are dependent on the Vrms amplitudes of the sinewave signal and it is typical to use a 90 percent full scale input signal for these measurements. However, if clipping does occur, the measurements will be severely degraded, so ensure the signal is not clipped. The frequency chosen should be well within the passband of the filter (~10 percent f_c) and should be relatively prime to the record length (samples) and sample rate (refer to paragraph 3.2 of this document). Almost any error source in the sinewave other than frequency accuracy, gain accuracy, and dc offset can affect the test result; therefore, it is highly recommended that a sinewave of good stability/accuracy be used from a high precision signal source.

4.1.2.1 Test Setup.

The test setup and procedures are shown in Figure 14 and Table 5.

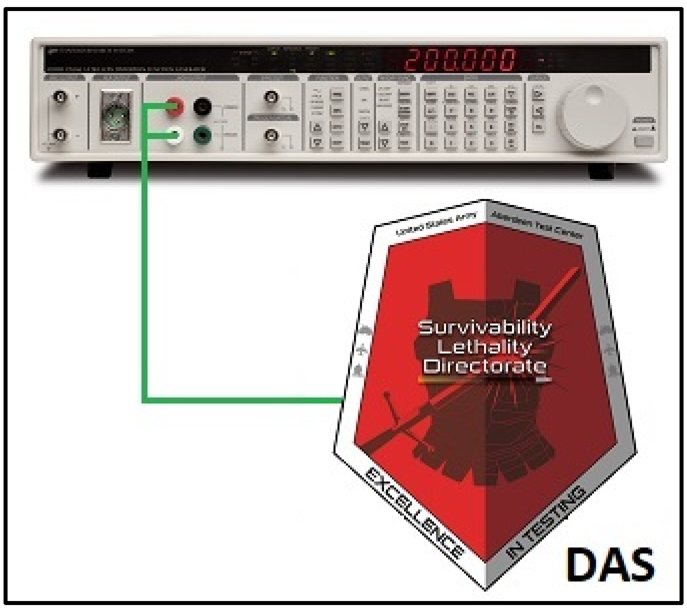

Figure 14. System noise test setup.

TABLE 5. SYSTEM NOISE TEST PROCEDURES

<table>
<tr><th colspan="3">SYSTEM NOISE

Test Standard: IEEE 1057</th></tr>
<tr><td colspan="2">Equipment Needed:
• DAS
• Precision signal generator PSG</td><td>Connections Needed
• Connect the high PSG to the DAS as indicated in Figure 14</td></tr>
<tr><th>Step</th><th>Action</th><th>Parameters</th></tr>
<tr><td>1</td><td>Make Connections</td><td>N/A</td></tr>
<tr><td>2</td><td>Set DAS Parameters</td><td>Trigger: Set to manual
Gain/Range: Unity
Sample Rate: Max
Filters: 10% of sample rate</td></tr>
<tr><td>3</td><td>Set PSG Parameters</td><td>Input Amplitude: 90% DAS Full Scale
Frequency: 10% of Filter Cutoff
Frequency should be adjusted to be relatively prime</td></tr>
<tr><td>4</td><td>Acquire Data</td><td>Collect at least 65536 samples</td></tr>
<tr><td>5</td><td>Analyze Data</td><td>See Analysis Paragraph 4.1.2.2</td></tr>
<tr><td>6</td><td>Repeat steps 2-5 for each Gain/Range</td><td>N/A</td></tr>
</table>

4.1.2.2 Results.

The System Noise Test should be analyzed for the following results and compared to legacy systems as well as current system specifications for any discrepancies.

a. Frequency.

b. Amplitude.

c. Phase angle.

d. Rms error.

e. Peak error.

4.1.2.3 Mathematical Equations for Noise and Distortion / Effective Number of Bits (ENOB).

a. ENOB is mathematically calculated using a curve fitting test method with a variety of different algorithms that can be used. For help getting started using the curve fit algorithms, IEEE recommends using the toolbox available for free at http://www.mit.bme.hu/projects/adctest/. This software toolkit contains software procedures for the IEEE 1057 standard.

b. Once data have been recorded per the test method above, and a best-fit sinewave dataset has been created using the provided software, the Noise and Distortion (NAD) must first be calculated using Equation 4.

$$NAD = \left[\frac{1}{M}\sum_{n=1}^{M}(x[n] - x'[n])^2\right]^{1/2} \qquad \textit{(Equation 4)}$$

where:

x[n] is the data set of the waveform recorded under test
x'[n] is the data set of the best-fit sinewave
M is the number of samples in the record

c. Once NAD has been calculated, Equation 5 is used to calculate ENOB.

$$ENOB = log_2\left(\frac{FSR}{NAD * \sqrt{12}}\right) \qquad \textit{(Equation 5)}$$

where:

FSR is the full-scale range of the data recorder under test

4.2 <u>Analog Bandwidth</u>.

Analog bandwidth for a low pass filter is the area between the lowest frequency, typically DC, and the highest frequency, typically f_c, where the input amplitude response has been attenuated no greater than 3 dB. f_c is typically the frequency at which the input amplitude is -3 dB (0.707 * input amplitude). Low pass filters are most often provided with data acquisition systems so only an upper f_c will normally apply. The bandwidth can be measured at any stated signal amplitude and sampling rate. When the sampling rate is not specified, bandwidth is measured at the maximum sampling rate, and when amplitude is not specified, bandwidth is measured using a signal ~90 percent FS.

4.2.1 Analog Bandwidth– Test Method.

To measure analog bandwidth manually, inject a constant amplitude sinewave with a starting relatively prime frequency well within the passband (~10 percent f_c) into a channel. Measure the maximum peak-to-peak or rms voltage of the recorded data and establish the reference amplitude. Increase the frequency to another relatively prime value and measure again. Do this many times (~20) increasing the measurements near the knee regions. Map the frequency (x axis) with the amplitude (y axis) and create a bode plot of the data.

4.2.2 The test setup and procedures are shown in Figure 15 and Table 6.

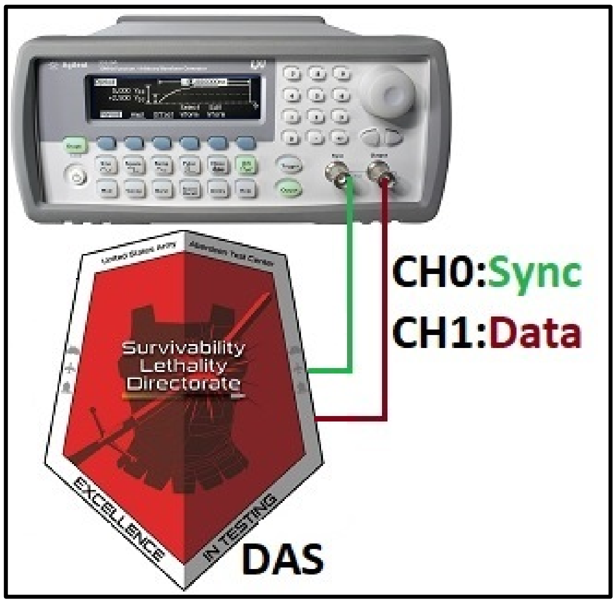

Figure 15. Analog bandwidth test setup.

TABLE 6. ANALOG BANDWIDTH TEST PROCEDURES

ANALOG BANDWIDTH Test Standard: ATC Bode		
Equipment Needed: • DAS • PSG		**Connections Needed** • Connect the signal generator to the DAS as indicated in Figure 15
Step	**Action**	**Parameters**
1	Make Connections	N/A
2	Set DAS Parameters	**Trigger:** Set to manual(Or live if possible) **Gain/Range:** Unity (Unless Specified by DAS Specs) **Sample Rate:** Max (Unless Specified by DAS Specs) **Filters:** Filter Bandwidth Under Test
3	Set PSG Parameters	**Input Amplitude:** 90% DAS Full Scale **Frequency:** 10% of Filter Cutoff
4	Acquire Data	Acquire data at increasing frequencies until enough data has been taken to create an accurate bode plot. In the interest of time if the DAS has a real time display, peak amplitude may be written down in real time as frequencies are changed.
5	Analyze Data	See Analysis Paragraph 4.2.3
6	Repeat steps 2-5 using different filter cutoffs as desired	N/A

4.2.3 Analysis.

a. Create a Bode plot of all the waveform data collected. Note the measured bandwidth (-3 dB), stop-band (Hz), Roll Off rate (dB/decade or dB/octave), ultimate attenuation (dB), Phase (θ°) and Phase Linearity. Assuming the DAS has a low pass filter, DC to f_c is the bandwidth. The stop-band is the lowest point of attenuation. The Roll Off (slope) is the rate of change between the cutoff frequency and the stop-band. The ultimate attenuation is the point where the slope becomes zero or positive, and may be the same as the stopband. Figure 16 shows an example Bode plot.

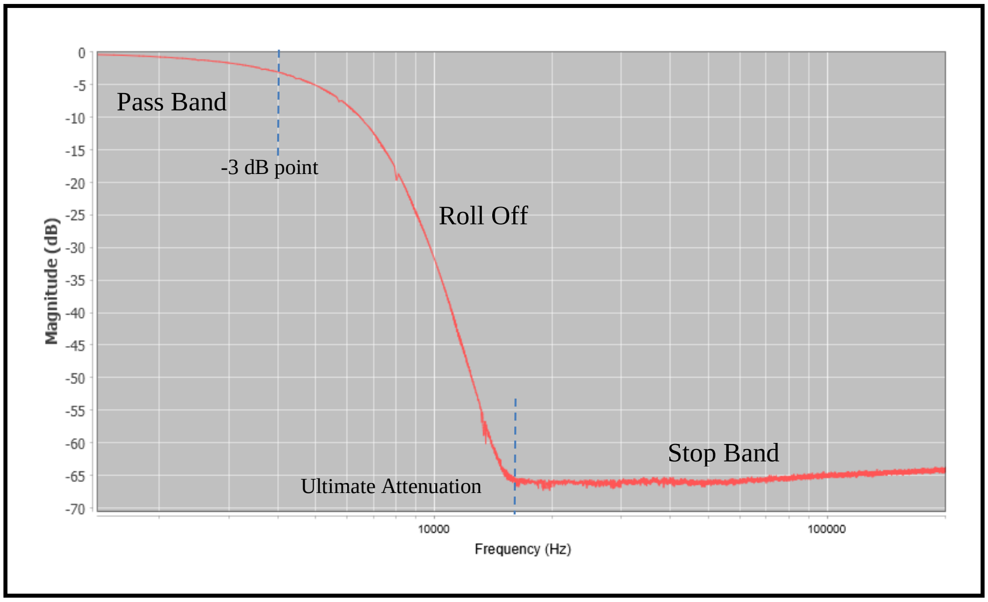

Figure 16. Example Bode plot.

b. The Roll Off rate for a filter is dependent on the filter order. A filter with an n^{th} order, will have a subsequent roll-off rate of 20(n) dB/decade or 6(n) dB/octave. A first-order filter has a roll-off rate of 20 dB/decade or 6 dB/octave, a second-order filter has a roll off rate of 40 dB/decade or 12 dB/octave, and a fourth-order filter has a roll-off rate of 80 dB/decade or 24 dB/octave and so on. A decade is equal to $f_1 * 10$ and an octave is equal to $f_1 * 2$. Figure 17 shows the dB/decade v.s dB/octave.

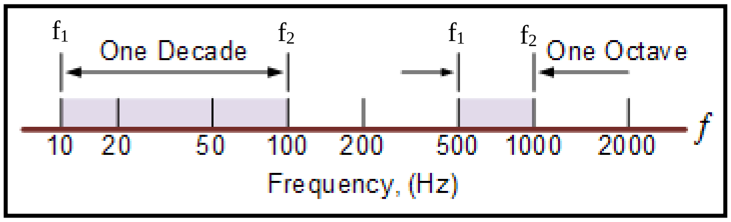

Figure 17. dB/decade v.s dB/octave.

c. Phase Linearity describes how a filter's propagation delay is affected by frequency. If a different amount of time is required for each different frequencies then each frequency will have a different time period, and that different period will correspond to a phase shift or delay. To achieve equal delays at all frequencies, all frequencies must have a different phase shift. The goal is to have a phase shift response that increases linearly with frequency, because as the frequency increases a fixed phase shift corresponds to a gradually diminishing length of time, and thus more phase shift is needed to compensate.

d. An ideal linear-phase filter, exhibits phase shift that increases linearly with frequency and provides a constant delay or Group Delay. Group Delay typically only references frequencies within the passband and is measured in time with respect to frequency. A Bessel filter is a linear phase filter that has a constant Group Delay. In simple terms, Group Delay is the amount of time required for a signal to propagate through a device and more importantly it indicates how much a filter will distort a signal. See Appendix B for a discussion on group delay.

4.2.4 Results.

a. Verify the f_c is within 1.0 percent of the stated value.

b. Verify the slope is within 10 percent of the theoretical value for the filter tested.

c. Verify the Ultimate Attenuation meets Military Standard (MIL-STD)-810H[3].

d. Verify Phase angle is linear. A Bessel filter should be linear.

4.3 Alias/Out of Band Energy.

4.3.1 The test setup and procedures are shown in Figure 18 and Table 7.

Figure 18. Alias test setup.

TABLE 7. ALIASING TEST PROCEDURES

Aliasing Test Standard: MIL-STD-810H		
Equipment Needed: • DAS • PSG		**Connections Needed** • Connect the signal generator to the DAS as indicated in Figure 18
Step	**Action**	**Parameters**
1	Make Connections	N/A
2	Set DAS Parameters	**Trigger:** Set to manual **Gain/Range:** Unity **Sample Rate:** 40 kS/s **Filters:** 4 kHz Bessel 8th Order (Or similar)
3	Set PSG Parameters	**Input Amplitude:** 90% DAS Full Scale **Frequency:** 36 kHz
4	Acquire Data	Typically 1s or less will suffice
5	Analyze Data	See Analysis Paragraph 4.3.2
6	Repeat steps 2-5 using a 44 kHz input signal	N/A

4.3.2 Analysis.

Based on the alias frequency selected, look for the fold over frequency in the pass band of the filter. A FFT may be required to determine the magnitude of the aliased frequency. As the input frequency changes the alias frequency will change proportionally making it easier to identify and measure.

4.3.3 Results.

To meet MIL-STD-810H, the magnitude of the aliased frequency must be attenuated by -50 dB for all frequency above Nyquist. Though -50 dB is the requirement for MIL-STD-810H, a more stringent requirement of -80 dB would be more appropriate for the advancements made in DAS.

4.4 Alternating Current/Direct Current Accuracy.

a. Accuracy may be best described for technology as the largest error detected / measured under specific operating conditions as compared to the absolute truth. Accuracy is typically expressed as a percentage that indicates how close the recorded measurement is to the actual value of the signal source. Figure 19 is a graphical representation of accuracy and precision. Inaccuracy for most recording systems can be corrected by calibration, making the measurement more accurate but when a system is not precise there is no way to correct or remove that error from the measurement.

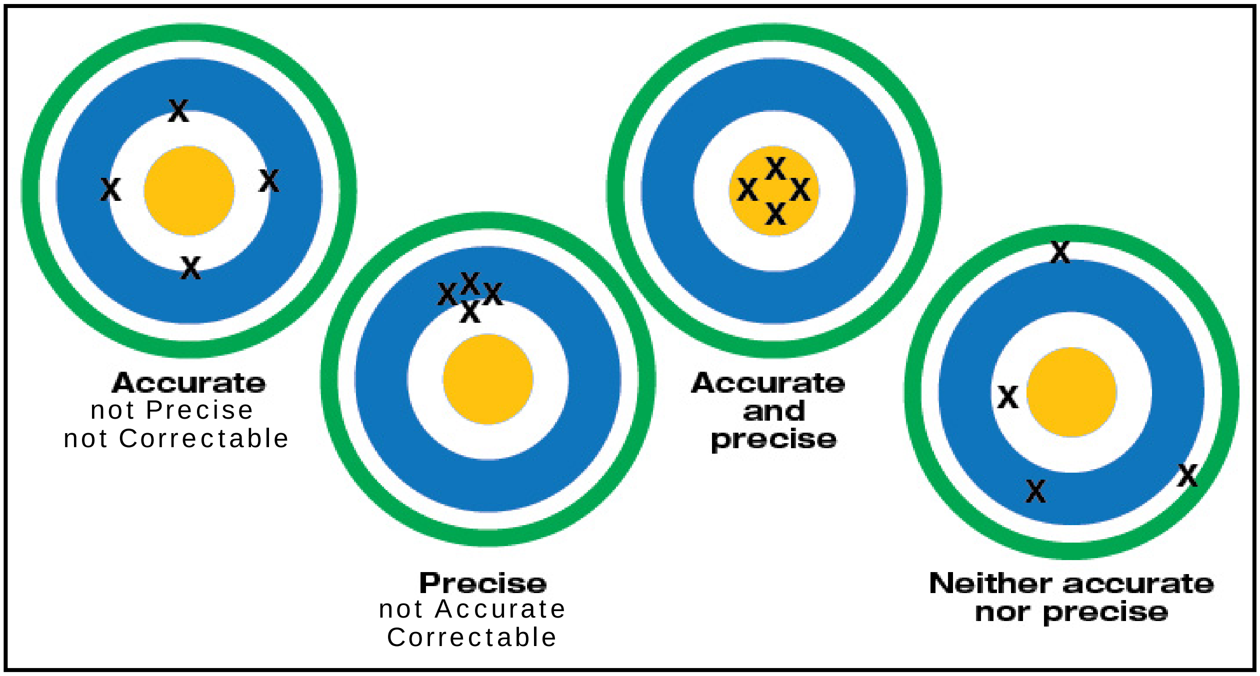

Figure 19. Accuracy and precision pictorial.

b. The definitions of commonly used terms are as follows.

(1) Accuracy - How close a measurement comes to the actual reference value.

(2) Resolution - The smallest increment the instrument can detect or display.

(3) Range - The upper and lower limits of the instrument.

(4) Precision - The instruments repeatability or how reliably it can make the same measurements over and over.

4.4.1 Test Method.

The AC / DC accuracy measurement method for a waveform recorder is to determine to what degree the result or measurement conforms to the correct value or standard as referenced by National Institute of Standards and Technology (NIST) traceable devices. Traceability is defined as a property of a measurement where the results can be related back to a reference through clear and unbroken chain of calibrations. For AC signals, measuring RMS is the standard and for DC signals, a simple voltage level measurement using a precision voltmeter is the standard. Avoid analyzing data at the start and stop of each record. This will eliminate potential transients caused by the startup and shutdown of the voltage source and will ensure the best steady state measurement possible.

4.4.2 The test setup and procedures are shown in Figure 20 and Table 8.

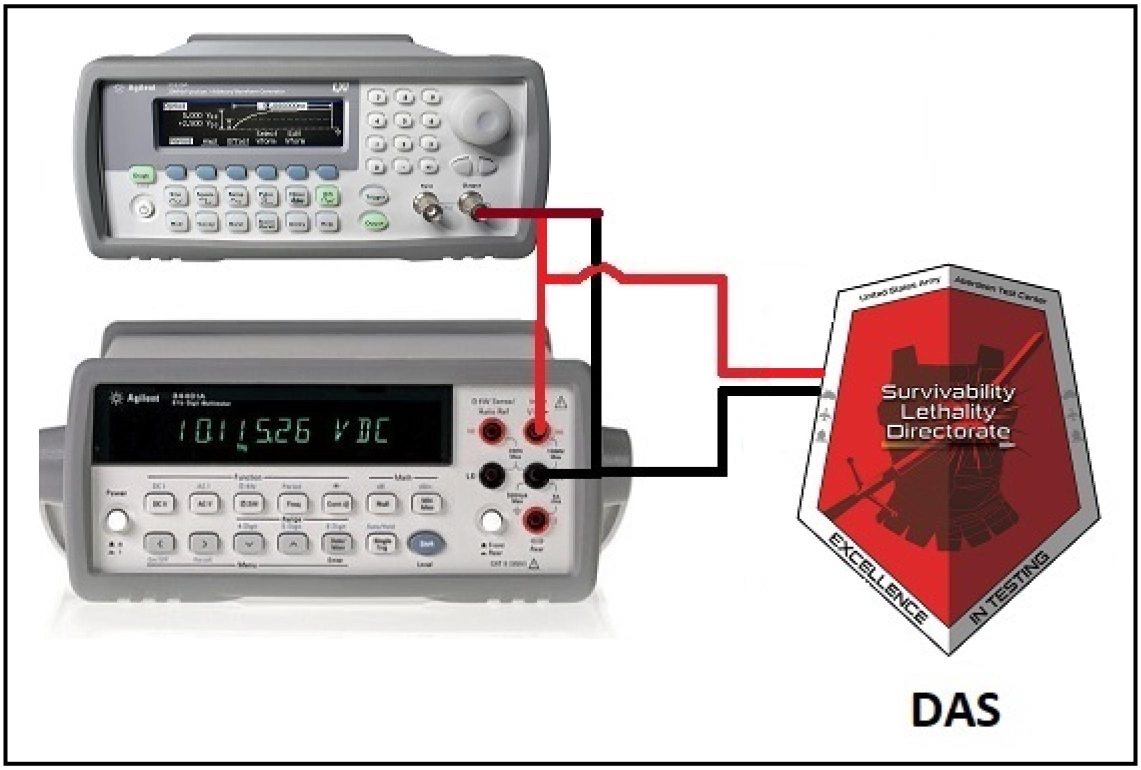

Figure 20. AC/DC Accuracy test setup.

TABLE 8. AC/DC ACCURACY TEST PROCEDURES

<table>
<tr><th colspan="3">AC/DC Accuracy

Test Standard: ATC NIST Traceable</th></tr>
<tr><td colspan="2">Equipment Needed:
• DAS
• Precision PSG
• Digital Multi-Meter (DMM) (minimum of 6.5 digit accuracy)</td><td>Connections Needed
• Connect the DMM,PSG, and DAS as shown in Figure 20. Keep the Cables as short as possible for most accurate results</td></tr>
<tr><th>Step</th><th>Action</th><th>Parameters</th></tr>
<tr><td>1</td><td>Make Connections</td><td>N/A</td></tr>
<tr><td>2</td><td>Set DAS Parameters</td><td>Trigger: Set to manual
Gain/Range: Unity (Testing various ranges is recommended)
Sample Rate: Max (Unless Specified by DAS Specs)
Filters: Commonly used filter for Users application</td></tr>
<tr><td>3A</td><td>Set PSG Parameters (AC Test)</td><td>Input Amplitude: 90% DAS Full Scale
Frequency: 10% of Filter Cutoff</td></tr>
<tr><td>3B</td><td>Set PSG Parameters (DC Test)</td><td>90% Full Scale Square wave with a 10s period (5s negative, 5s positive)
Record the DC peak-peak levels of the square wave from the DMM and DAS</td></tr>
<tr><td>4</td><td>Acquire Data</td><td>Record at least 5 periods of the input signal for analysis</td></tr>
<tr><td>5</td><td>Analyze Data</td><td>See Analysis Paragraph 4.4.3</td></tr>
<tr><td>6</td><td>Repeat steps 2-5 for other Gain/Ranges</td><td>N/A</td></tr>
</table>

4.4.3 Analysis.

Since the DMM is the traceable source, calculate the percent error from the DMM measured value (actual value) and the waveform recorder value. Remember to avoid using data from either end of the data file to avoid on/off transients. Find the average error, minimum error, and maximum error for each gain/range and note in a table.

4.4.4 Results.

a. When presenting results for AC measurements, list the RMS values from both the source and the unit under test. Then solve for Full Scale Average error (%) at each gain/range for all channels, maximum error (%) - highest error for each gain/range and minimum error (%) – lowest error for each gain/range.

b. When presenting the DC results use the DMM measured peak-to-peak value and the DAS peak-to-peak value, and display the average error (%), minimum error (%), and maximum error (%) for each gain/range in a table.

4.5 Dynamic Range.

Dynamic range of the waveform recorder is the ratio of the smallest recordable input signal to the largest recordable input signal. Spurious-Free Dynamic Range (SFDR) is the ratio of the input signal to the peak spur. A spur is any frequency component (noise or harmonics) that is not the carrier wave (main input signal component). The SFDR can be expressed relative to FS or relative to the carrier. An ideal dynamic range for any ADC is based on the bit depth. A 16 bit ADC will have an ideal dynamic range of 96 dB (96 dB = $20*\text{Log}(2^{16}-1)$) and a 24 bit ADC will have an ideal dynamic range of 144 dB (144 dB = $20*\text{Log}(2^{24}-1)$), each bit is approximately 6 db.

4.5.1 Test Method.

At unity gain / range, measure the peak to peak baseline noise (Vmin) and the peak to peak full scale (Vmax) of the system and record the results. The ratio of these two numbers is the dynamic range of the system.

4.5.1.1 For tips on how to measure baseline noise see setup in paragraph 4.1.1.1. The peak-peak full scale of the DAS can be measured at unity with any full scale input signal. The test setup is shown in Figure 21.

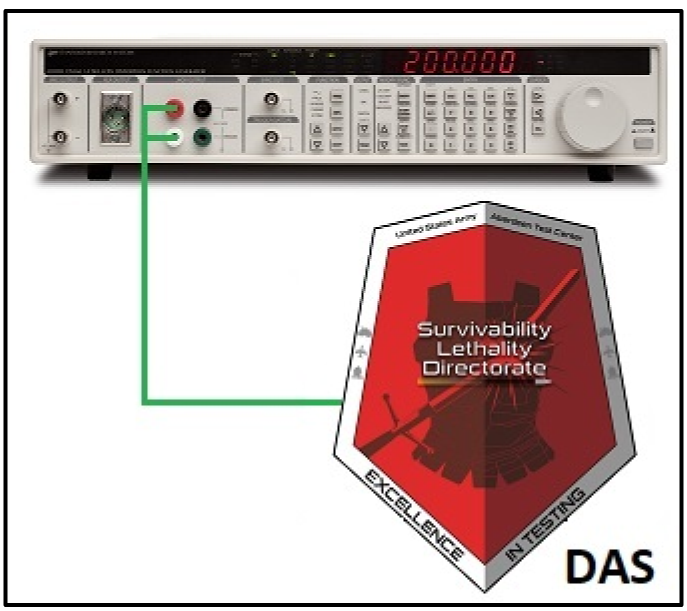

Figure 21. Dynamic Range test setup.

4.5.1.2 Analysis.

Dynamic range is the ratio of the highest recordable value and the lowest recordable value and can be determined by: Dynamic Range = 20 log(V_{Max}/V_{Min}). If the dynamic range measured ever exceeds the ideal dynamic range of the system as explained above, there is a problem in the measurement process and the test should be conducted again. The real dynamic range can never exceed the ideal dynamic range.

4.5.1.3 Results.

Record the results for each channel at unity gain.

4.5.2 Spurious Free Dynamic Range (SFDR).

A large signal is recorded and a Fourier transform is performed on the record set. An average of five separate transforms is preferable to reduce unwanted noise artifacts. The difference between the input signal and the highest spur is the SFDR. This test should be run at multiple frequencies and different gains.

4.5.2.1 Setup.

The test procedures are shown in Table 9.

TABLE 9. SFDR TEST PROCEDURES

<table>
<tr><th colspan="3">Spurious Free Dynamic Range

Test Standard: IEEE 1057</th></tr>
<tr><td colspan="2">Equipment Needed:
• DAS
• Precision PSG</td><td>Connections Needed
• Connect the signal generator to the DAS as indicated in Figure 21</td></tr>
<tr><td>Step</td><td>Action</td><td>Parameters</td></tr>
<tr><td>1</td><td>Make Connections</td><td>N/A</td></tr>
<tr><td>2</td><td>Set DAS Parameters</td><td>Trigger: Set to manual
Gain/Range: Unity
Sample Rate: Max set for DAS
Filters: Commonly used filter for Users application</td></tr>
<tr><td>3</td><td>Set PSG Parameters</td><td>Input Amplitude: 100% FS
Frequency: 10% of Filter Choice</td></tr>
<tr><td>4</td><td>Acquire Data</td><td>Acquire 1s of data</td></tr>
<tr><td>5</td><td>Analyze Data</td><td>See Analysis Paragraph 4.5.2.2</td></tr>
</table>

4.5.2.2 Analysis.

Once the data has been acquired, the SFDR should be presented in graphical format as an FFT along with results in tabular format depicting magnitude of SFDR in dB. Note the peak signal and peak spur from the FFT plot shown in Figure 22.

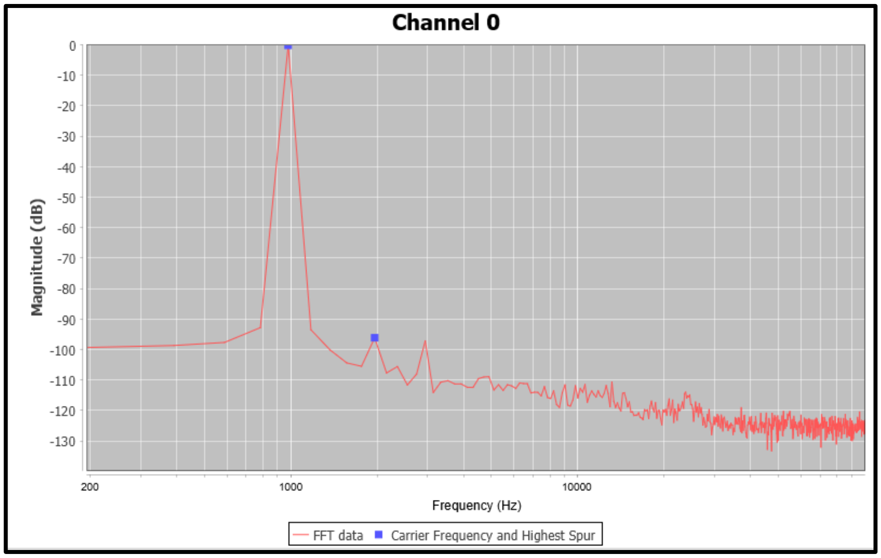

Figure 22. SFDR FFT results.

4.5.2.3 Results.

SFDR is calculated simply as the difference between the peak signal and peak spur. This should be reported in dB and compared to legacy system and system specifications.

4.6 Slew Rate.

a. Slew rate is defined as the maximum rate of change in voltage per unit of time for the input amplifiers of a waveform recorder. Slew rate is typically expressed in Volts per microsecond (V/µs). Figure 23 shows theoretical examples of how a square wave and sinewave can be affected by the slew rate of an operational amplifier.

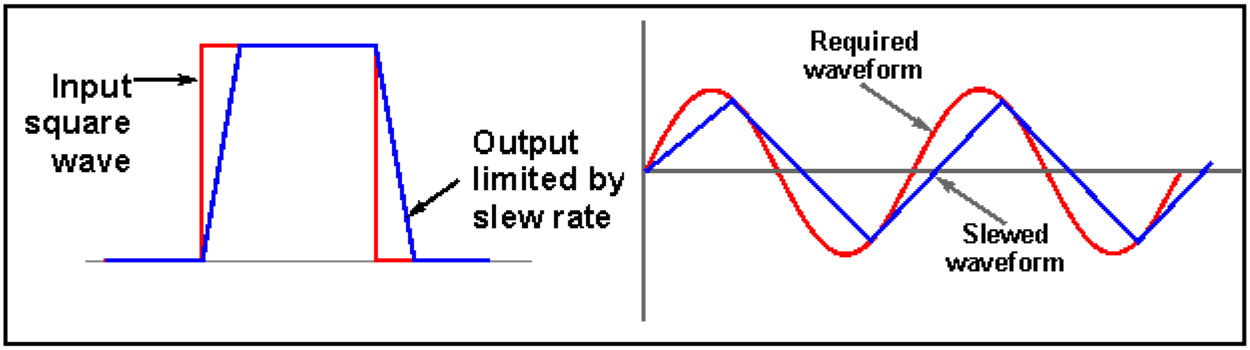

Figure 23. Waveforms effected by slew rate.

b. Knowing the maximum possible slew rate of a DAS is important for insuring that the frequencies being measured are not inadvertently corrupted due to the insufficient slew rate of the recording system. When testing hybrid analog and digital systems be sure to bypass all filtering so the measurement is an actual representation of the amplifiers slew rate and not affected by the filters response. If a DAS has an integrated anti-alias filter that cannot be bypassed, be aware that the filter will most likely be the dominant cause for a reduced slew rate measurement.

4.6.1 Test Method.

a. The procedure for measuring slew rate is found in IEEE 1057, Section 9.3. The slew rate is measured by finding the rate of voltage change of an input step waveform (square wave). Record the step response for an input step having an amplitude 10 percent of full scale. Determine and store the maximum rate of change of the output transition. Repeat the process of increasing the amplitude of the input step and noting the maximum rate of change of the output transition. When the maximum rate of change ceases to increase proportionally with increasing step amplitude, slew rate limiting is taking place, and the slew rate limit is the largest recorded value for the maximum rate of change. When sampling these results digitally it is sometimes difficult to get more than a couple samples on the rising edge of the waveform so, in these instances interpolate the rate of change in the 10 - 90 percent voltage range and record that region as the slew rate measured.

b. The test setup and procedures are shown in Figure 24 and Table 10.

Figure 24. Slew rate test setup.

TABLE 10. SLEW RATE TEST PROCEDURES

Slew Rate Test Standard: IEEE 1057		
Equipment Needed: • DAS • PSG		**Connections Needed** • Connect the signal generator to the DAS as indicated in Figure 24
Step	**Action**	**Parameters**
1	Make Connections	N/A
2	Set DAS Parameters	**Trigger:** Set to manual **Gain/Range:** Max for system **Sample Rate:** Max set for DAS **Filters:** None if possible, Filter will cause Slew Rate to appear much slower
3	Set PSG Parameters	**Input Amplitude:** 10% FS to start **Frequency:** Square wave, Pulse mode
4	Acquire Data	Acquire 5 pulses of data
5	Analyze Data	See Analysis Paragraph 4.6.2
6	Repeat steps 2-5	Increment the Input Amplitude of the PSG by 10% each iteration until 100% FS is met

4.6.2 Analysis.

a. From the table of results, the slew rate is the maximum rate of change in the linear region. (Example results: 2 V/µs, 4 V/µs, 6 V/µs, 7 V/µs; the slew rate is 6 V/µs, the maximum rate of change in the linear region).

b. If it was not possible to record two or more samples on the rising edge and it is also not possible to increase the sample rate, just interpolate the rate of change between the 10 - 90 percent range of the rising edge of the waveform and document the rate of change as the systems measured slew rate.

c. Typically the slew rate on instrumentation amplifiers is greater than 10 V/µs. If the test is conducted on a Hybrid system and the maximum slew rate measured is less than 5 V/µs then it is very probable there is a filter in the signal path and that filter is the dominant reason for the low slew rate measurement. Most likely the actual slew rate is greater than 10 V/µs. MIL-STD-810H states that the slew rate of an instrumentation amplifier for pyro-shock requirements must be able to record a change of half of the full scale voltage of the system in 1 µs.

4.6.3 Results.

Report the slew rate from the square step response directly in V/µs. When performing this test manually, it is helpful to plot the points and create a line of best fit in order to visually inspect if there are any issues with slew rate. Table 11 and Figure 25 show the results of a slew rate test performed on Ballistics High Speed Dewesoft DAS. The results showed the DAS stayed linear through its entire input range.

TABLE 11. SLEW RATE

INPUT, V	RATE OF CHANGE, V/µS
10	7.64
20	15.15
30	22.73
40	30.62
50	38.77
60	46.11
70	53.95
80	61.82

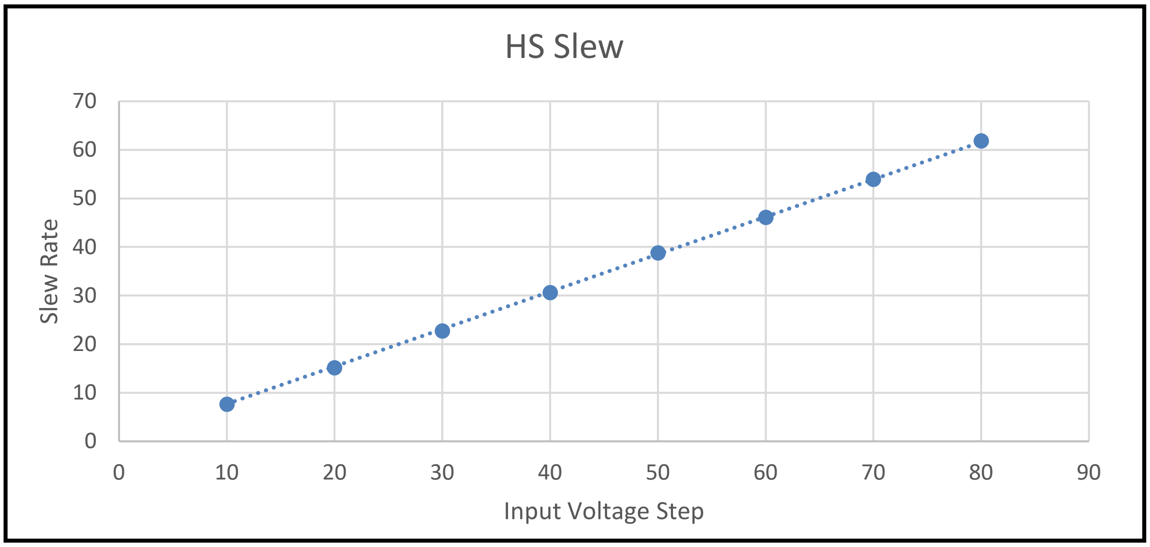

Figure 25. Linearity of slew rate.

4.7 Sine Wave Test (Effective Number of Bits).

a. The sine wave test is a measure of the ENOB, essentially the dynamic range of an ADC expressed in bits. The full resolution of an ADC is specified by the number of bits used to represent the analog value, in principle giving 2^N signal levels for an N-bit signal. However, all real ADC circuits introduce noise and distortion. ENOB specifies the actual resolution of the ADC circuit under consideration. An ideal ADC will have a signal to noise ratio equal to (SNR= 6.02N + 1.76dB) where N is the number of bits for the waveform recorder. Generally, ENOB is defined as (Equation 6):

$$ENOB = \frac{SINAD(dB) - 1.76(dB)}{6.02} \qquad \textit{(Equation 6)}$$

where:

SINAD is a ratio of the signal quality.
The term 6.02 converts dB to bits.
The term 1.76 comes from quantization error in an ideal ADC.

b. A Sine Wave Test is a good place to start when first evaluating a new system. The test is a quick way to evaluate the overall performance of a system and the ENOB results can be used to compare different systems very quickly. If poor ENOB results are achieved, the other tests in this document will shed some light as to where a problem may exist.

4.7.1 Test Method.

The IEEE 1057 method (Section 8.2.1) for determining ENOB uses a fitted sinewave to determine the noise and then indirectly calculates the ENOB based on the noise. The sinewave test should be run at each gain to determine the ENOB for the overall DAS. The test frequency is typically well within the passband (~10 %f_c) of the systems filter cutoff.

4.7.2 The test setup and procedures are shown in Figure 26 and Table 12.

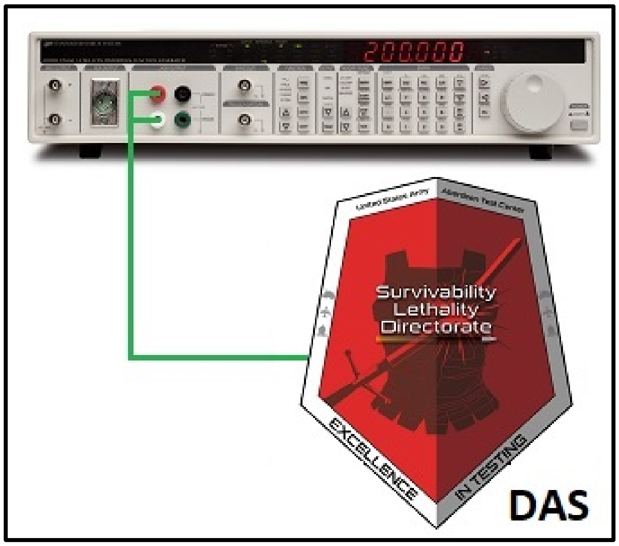

Figure 26. Sine wave test setup.

TABLE 12. SINE WAVE TEST PROCEDURES

ENOB Test Standard: IEEE 1057		
Equipment Needed: • DAS • Precision PSG		**Connections Needed** • Connect the signal generator to the DAS as indicated in Figure 26
Step	**Action**	**Parameters**
1	Make Connections	N/A
2	Set DAS Parameters	**Trigger:** Set to manual **Gain/Range:** Unity **Sample Rate:** Max for DAS **Filters:** 10% Sample Rate
3	Set PSG Parameters	**Input Amplitude:** 90% Full Scale **Frequency:** 401.101 Hz
4	Acquire Data	Acquire at least 65,536 Samples
5	Analyze Data	See Analysis Paragraph 4.7.3
6	Repeat steps 2-5 for various gain/rage and sample rate combinations	ENOB can change dramatically when moving away from Unity Gain. It is recommended to test the entire spread of gain/range combinations as well as high and low sample rates

4.7.3 Analysis.

Run the ENOB analysis following the mathematical equations and suggested literature in paragraph 4.1.2.3, and determine the $ENOB_{pp}$ and $ENOB_{rms}$ at each gain for an overall system response. Sample results are shown in Figure 27.

Sine Wave Statistics Report

	freq	offset	Amplitude	phase	rmsError	rms Num bits	peak Error	peak num bits
Max=	401.1010889648	-0.00007000	0.90087000	270.61283000	0.00001230	15.63865000	0.00008607	14.26617000
Min=	401.1010883049	-0.00008000	0.90084000	270.60375000	0.00001136	15.52422000	0.00008316	14.21660000
Spread=	0.0000006599	0.00001000	0.00003000	0.00908000	0.00000094	0.11443000	0.00000291	0.04957000
AVG=	401.1010886859	-0.00007333	0.90085000	270.60725667	0.00001177	15.58828000	0.00008485	14.23738667
SD=	0.0000002789	0.00000471	0.00001414	0.00398455	0.00000039	0.04770827	0.00000123	0.02101200

Figure 27. ENOB results.

4.7.4 Results.

To compare ENOB results to legacy systems, acquire the data using the following parameters:

a. Sample Rate = 40 kHz.

b. Filter Cutoff = 4 kHz.

c. Input Frequency = 401.101 Hz.

d. Input amplitude = 90 percent FS.

e. Acquire 1.0 s of data (or at least 65,536 samples).

4.8 Sampling Time Base.

4.8.1 Test Method.

This test is used to determine if the DAS maintains accurate time when acquiring data over a long period of time. Twenty-five seconds was chosen as a long period of time based on a typical ballistic acquisition time of less than one second. Conducting this test on a high sample rate system will make large data files so choose the parameters accordingly. The PSG sends out a 25 second pulse to a digital counter and the waveform recorder simultaneously. The length of the pulse recorded by the DAS is then compared to the pulse width measured by the counter time. The test setup and procedures are shown in Figure 28 and Table 13.

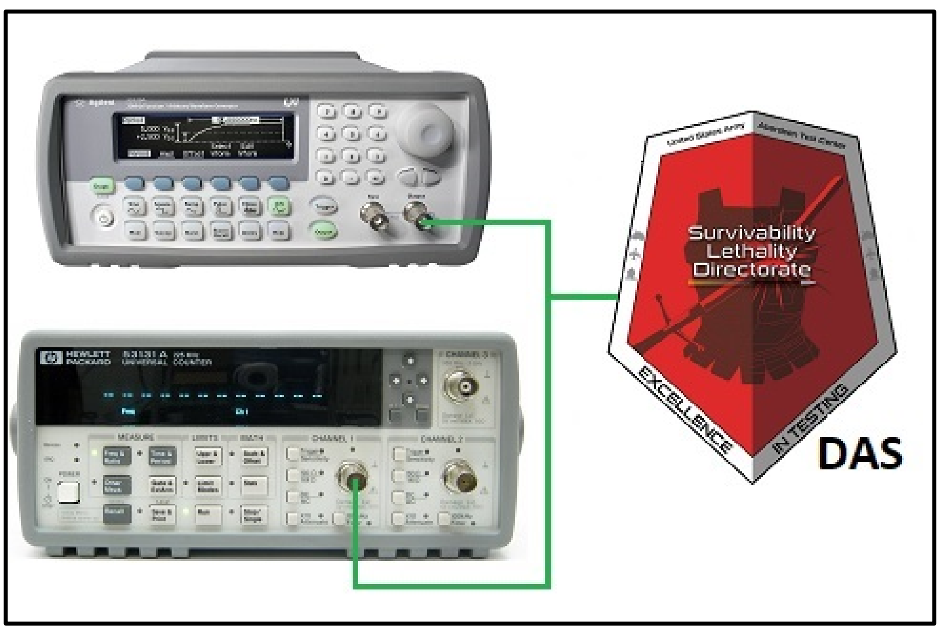

Figure 28. Sampling Time Base test setup.

TABLE 13. SAMPLING TIME BASE TEST POCEDURES

Sampling Time Base Test Standard: ATC Internal Operating Procedure (IOP) / NIST Counter Timer		
Equipment Needed: • DAS • NIST Traceable Counter Timer • PSG		**Connections Needed** • Connect the signal generator to the DAS • Connect the signal generator to the Counter Timer • Try to keep connections to the same length
Step	**Action**	**Parameters**
1	Make Connections	N/A
2	Set DAS Parameters	**Trigger:** Rising Edge of PSG **Gain/Range:** 10 V (Or closest Range) **Sample Rate:** Max if data storage device will allow for 25 seconds of data, else lower as necessary **Filters:** None if possible
3	Set PSG Parameters	**Input Amplitude:** 90% Full Scale **Frequency:** Square wave, 25 second duration
4	Set Counter Timer Parameters	Set Counter Timer to trigger on rising edge of wave form
5	Acquire Data	Acquire entire 25 second signal making sure to catch rising and falling edge
6	Analyze Data	See Analysis Paragraph 4.8.2

4.8.2 Analysis.

The digital counter will measure and display the actual pulse width in microseconds. Compare the relative digital counter results to the relative DAS results and record the difference in time and samples. If the DAS has Global Positioning System (GPS) time, also compare the absolute times by using the Time Spy or some other GPS time source.

4.8.3 Results.

The sample time base should remain constant throughout the data acquisition. The time difference, ideally, would not be greater than the one sample.

4.9 Step Response.

From a practical standpoint, knowing how a system responds to a sudden input that steps from zero amplitude to near maximum levels is important as systems seldom pass an identical shaped step from the input to the output. A typical step response will produce the characteristics of overshoot, undershoot, and delayed settling times on both the positive and negative transitions. It is important to know how each different system responds to a step input especially when used in ballistic testing where impulses are expected.

4.9.1 Test Method.

When testing, use a relatively low frequency square wave (slow enough to ensure steady state is reached after each transition) and injected into the channel(s) under test. If the system under test has integrated filtering, keep in mind the step response should match the characteristics of the filter used. The test should be repeated on each filter type used. The test setup and procedures are shown in Figure 29 and Table 14.

Figure 29. Step Response test setup.

TABLE 14. STEP RESPONSE TEST PROCEDURES

Step Response Test Standard: IEEE-1057		
Equipment Needed: • DAS • PSG		**Connections Needed** • Connect the signal generator to the DAS as indicated in Figure 29
Step	**Action**	**Parameters**
1	Make Connections	N/A
2	Set DAS Parameters	**Trigger:** Set to Manual **Gain/Range:** Unity **Sample Rate:** Max of DAS **Filters:** 4 k Bessel 8th Order
3	Set PSG Parameters	**Input Amplitude:** 90% Full Scale **Frequency:** Square wave, 10 Hz, 50% Duty Cycle
4	Acquire Data	Acquire 5 periods of data
5	Analyze Data	See Analysis Paragraph 4.9.2
6	Repeat steps 2-5 for all desired filter types	Repeat for all available filter types of DAS under test

4.9.2 Analysis.

a. Evaluate one full square cycle in the middle of the data set. Do not use the data near turn-on or turn-off of the PSG to avoid any anomalies. The flat portions of the square wave must reach steady state before the next transition. If that is not happening, slow the input frequency of the square wave being used. Note the overshoot, undershoot, and settling time for the positive and negative transitions. Also note the step response shape. The input characteristics may be used to pin down any unreported filtering that a DAS might be using as well as validating the type of filter being used, if any is selected. An example of Step Response characteristics is shown in Figure 30. Characteristics of classic Bessel and Butterworth filters are shown in Table 15.

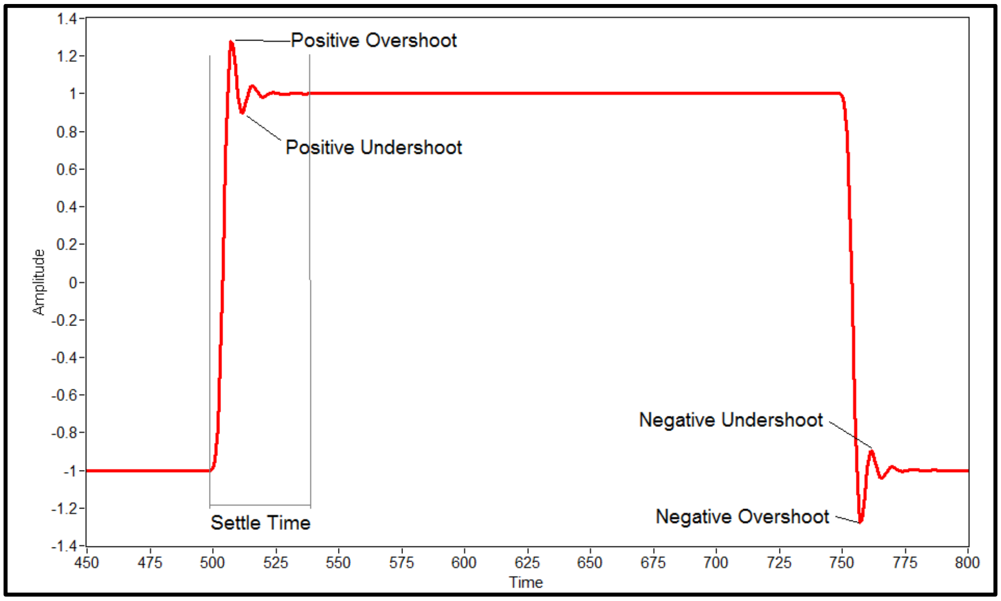

Figure 30. Example of Step Response characteristics.

TABLE 15. CHARACTERISTICS OF CLASSIC BESSEL AND BUTTERWORTH FILTERS[4]

Filter		Voltage gain at DC	STEP RESPONSE			FREQUENCY RESPONSE		
			Overshoot	**Time to settle to 1%**	**Time to settle to 0.1%**	**Ripple in passband**	**Frequency for x100 attenuation**	**Frequency for x1000 attenuation**
Bessel	2 Pole	1.27	0.4%	0.60	1.12	0%	12.74	40.40
	4 Pole	1.91	0.9%	0.66	1.20	0%	4.74	8.45
	6 Pole	2.87	0.7%	0.74	1.18	0%	3.65	5.43
	8 Pole	4.32	0.4%	0.80	1.16	0%	3.35	4.53
Butterworth	2 Pole	1.59	4.3%	1.06	1.66	0%	10.00	31.60
	4 Pole	2.58	10.9%	1.68	2.74	0%	3.17	5.62
	6 Pole	4.21	14.3%	2.74	3.92	0%	2.16	3.17
	8 Pole	6.84	16.4%	3.50	5.12	0%	1.78	2.38

b. The Bessel filter provides the best step response, making it the clear choice for time domain signals and the Butterworth optimizes passband flatness and is ideal for frequency domain signals.

4.9.3 Results.

Verify the overshoot, undershoot, and settling time as well as the step response to confirm the waveform matches the characteristics of the filter(s) being used.

4.10 Direct Current Linearity.

A linear circuit's output is a linear function of its input. A linear circuit is one in which the electronic components value of gain does not change with the level of voltage or current input to the circuit. Linear circuits are important because they can amplify electronic signals without distortion.

4.10.1 Test Method.

To test a DAS for DC Linearity at a specific gain, inject nine or more discrete DC voltages into the system across the FS input range. Plot each point from both the DMM reference and the recorded value. The largest difference of the actual (DMM) and the recorded value determines the non-linearity. DC linearity is expressed in %FS. The test setup and procedures are shown in Figure 31 and Table 16.

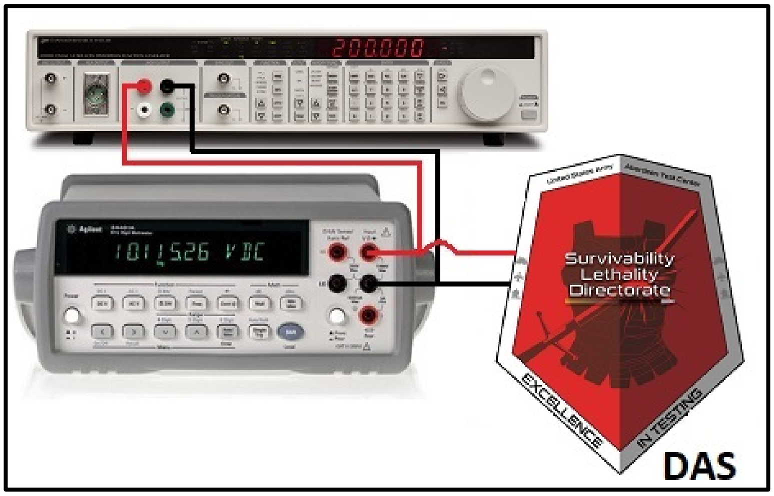

Figure 31. DC Linearity test setup.

TABLE. 16. DC LINEARITY TEST PROCEDURES

DC Linearity Test Standard: IEEE-1057		
Equipment Needed: • DAS • Precision PSG • DMM (Minimum of 6.5 digit accuracy)		**Connections Needed** • Connect the signal generator and DMM to the DAS as indicated in Figure 31
Step	**Action**	**Parameters**
1	Make Connections	N/A
2	Set DAS Parameters	**Trigger:** Set to Manual **Gain/Range:** 10-V **Sample Rate:** 100 kS/s **Filters:** 10 k Bessel 8th Order
3	Set PSG Parameters	**Input Amplitude:** 10%-90% full scale in at least 9 steps **Frequency:** Step Wave, Wait for step to settle Note: Steps can be done individually or programmed in sequence if PSG permits
4	Acquire Data	Acquire all 9 steps
5	Analyze Data	See Analysis Paragraph 4.10.2

4.10.2 Analysis.

Plot each DC voltage level, as measured by the DMM and the DAS. Create a line to connect the lowest point and the highest point. An example plot is shown in Figure 32.

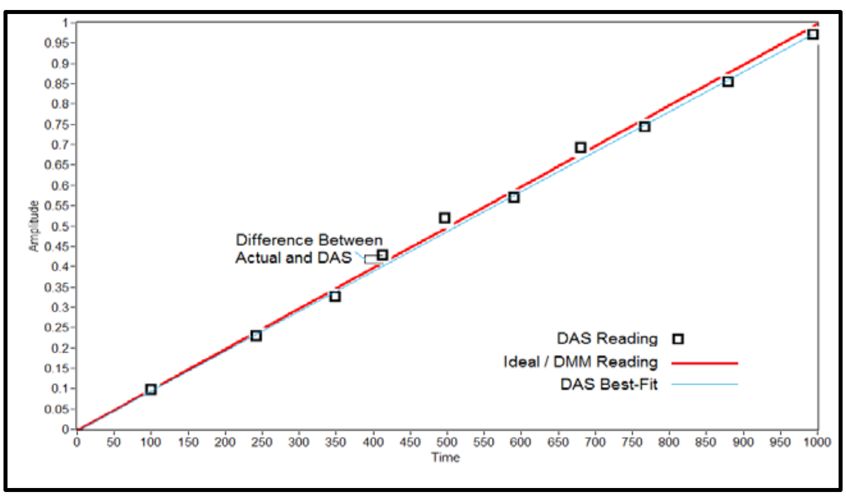

Figure 32. Example DC Linearity test plot.

4.10.3 Results.

Find the maximum difference (dV) between the line and the DAS value using Equation 7. Compare the difference to the manufacturers specification.

$$\%FS = (dV / FS) * 100\% \qquad \textit{(Equation 7)}$$

4.11 Drift.

Drift is defined as the tendency for a DAS system to gradually increase or decrease its output response over time with no change to the input of the system. Many sources of error can cause the apparent circuit drift to be much higher than would be typically expected. Temperature effects caused by temperature gradients across dissimilar metals are perhaps the worst offenders. Whenever dissimilar metals are joined, a thermocouple results. The voltage generated by the thermocouple is proportional to the temperature difference between the junction and the measurement end of the metal. This voltage can range between essentially zero and hundreds of microvolts/degree, depending on the metals used. Every integrated circuit is subject to this problem and it is especially critical in high-count DAS systems when low signal level measurements are required. The temperature drift problems in a DAS is most evident immediately after the system is turned on. To minimize this problem allow ample time for a system to warm up before acquiring data. Some systems will need longer warm up times than others.

4.11.1 Test Method.

This test is designed to measure the amount of drift in a DAS channel or group of channels. The approach is to allow a DAS or system under test sufficient time to warm up and stabilize before acquiring a prolonged data set. Depending on the type of system, the system stabilization time could be drastically different. Typically, a rack mounted DAS that is always on is allowed two hours to stabilize before conducting the drift test. More portable or battery powered system may have significantly less time available, so the stabilization time will need to be adjusted based on how the system is used. Use a resistor as an input load to keep the differential voltage input to the system steady at 0 V and the noise as low as possible. The record length will most likely be dependent on the DAS sample rate, so the rule of thumb to follow is to record 10x longer than the typical data acquisition event that is recorded. Then, analyze the data and note any drift tendencies over the entire recorded event. The test setup and procedures are shown in Figure 33 and Table 17.

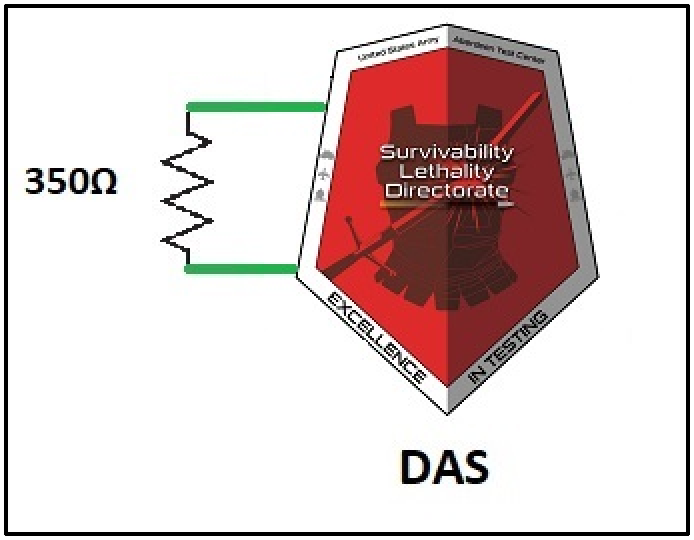

Figure 33. Input Drift test setup.

TABLE 17. INPUT DRIFT TEST PROCEDURES

Drift Test Standard: IEEE-1057		
Equipment Needed: • DAS • Input load (Typically 350 Ω)		**Connections Needed** • Connect the load to the DAS as indicated in Figure 33, clip leads are acceptable
Step	**Action**	**Parameters**
1	Make Connections	N/A
2	Set DAS Parameters	**Trigger:** Set to Manual **Gain/Range:** Unity **Sample Rate:** 1,250 Hz **Filters:** 40 k Bessel 8^{th} Order
3	Acquire Data	Allow typical stabilization time for DAS. Record 10X longer than typical test events. Note file size will be $(SR \times Acquisition\ Time\ \times bits\ of\ resolution)\ /$ 8 bytes
4	Analyze Data	See Analysis Paragraph 4.11.2
5	Repeat steps 2-5	Repeat for min and max gain/range

4.11.2 Analysis.

When analyzing the recorded data and obvious trends are not found, it may be necessary to separate the data record into groups of time, average the amplitude results for the individual time groups, and then compare the averaged results looking for a drift in the data. Note the drift characteristics such as V_{max} and V_{min}. Figure 34 shows the typical trace of a Drift Measurement. The drift on channel 1 and 2 were 2.97 uV and -0.47 uV respectively.

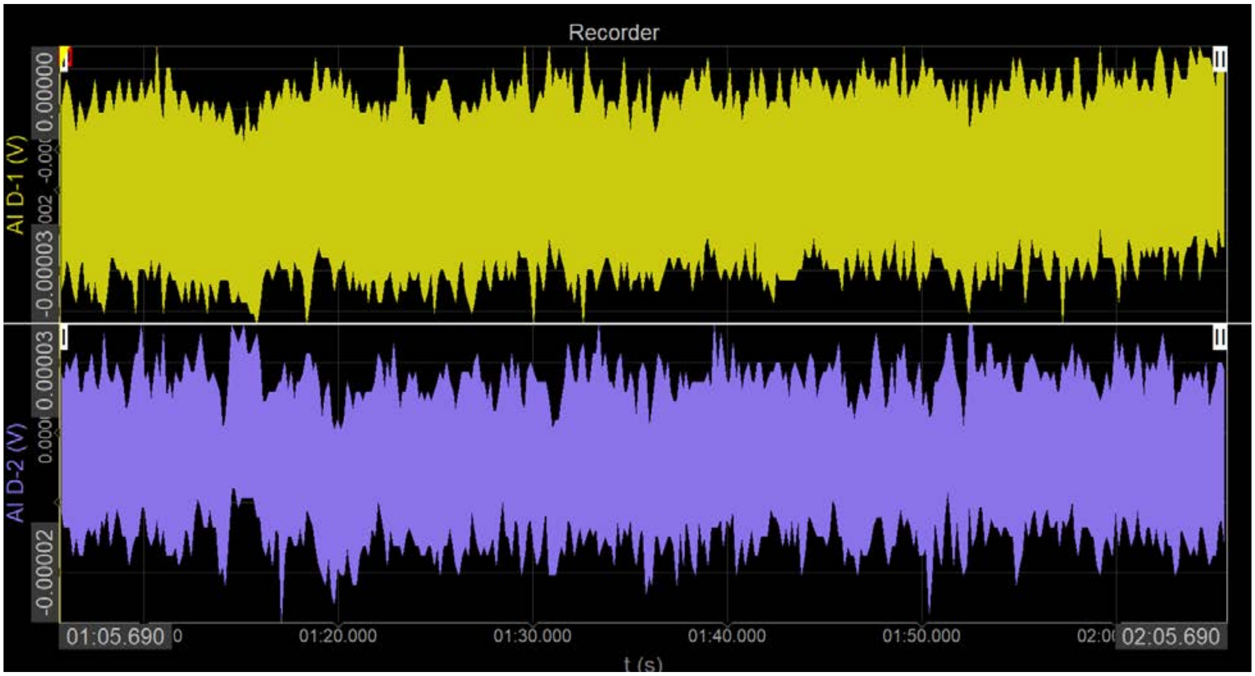

Figure 34. Typical Drift trace.

4.11.3 Results.

The drift should be within range of the system specifications and/or typically less than 0.01 percent of the FS range or 1 µV/s with respect to the input.

4.12 Global Positioning System (GPS)/Precision Time Protocol (PTP) Time Accuracy.

4.12.1 Test Method.

This test is designed to compare a known calibrated GPS time source to the time (GPS or Inter-Range Instrumentation Group) used by the DAS. The DAS must have an accurate time source and have mechanisms in place with the capability of time stamping incoming data with microsecond resolution. There are two different times (relative and absolute) that must be evaluated. Relative time is referenced only to itself or its own position and that position can be moved with no effect on the data (example: the plot shows the event happened at 2.5 seconds).

Absolute time is referenced to something other than itself and its position is fixed to a reference position (example: the plot shows the event happened April 1, 2020 @ 14:00:02.5). The precision time source should be capable of sourcing a 100 ms duration square wave pulse to the input of a DAS at an exact absolute time with nanosecond resolution. The DAS will record this pulse and the recorded and source times will be compared. The test setup and procedures are shown in Figure 35 and Table 18.

Figure 35. GPS Accuracy test setup.

TABLE 18. GPS/PTP TIME ACCURACY TEST PROCEDURES

GPS / PTP Time Accuracy Test Standard: ATC IOP		
Equipment Needed: • DAS • Precision Time Source		**Connections Needed** • Connect the precision time source output to the DAS as indicated in Figure 35
Step	**Action**	**Parameters**
1	Make Connections	N/A
2	Set DAS Parameters	**Trigger:** Rising Edge of timing Source output **Gain/Range:** Unity **Sample Rate:** Max for DAS **Filters:** None
3	Set Timing source Parameters	Configure time source to send pulse at a known absolute time
4	Acquire Data	Record the waveform on the DAS taking care to catch the beginning of the timing pulse
5	Analyze Data	See Analysis Paragraph 4.12.2
6	Repeat steps 2-5	Configure time source to output 1 Pulse Per Second and record multiple pulses

4.12.2 Analysis.

a. Compare the absolute time indicated on the time source with the recorded time stamp of the event form the DAS. The amount of agreement will depend on the SR and f_c used to acquire the data. The lower the f_c the larger the time difference will be between the source and the DAS. One will need to use their judgement when evaluating if the timing results are satisfactory.

b. Compare the relative time between multiple pulses as recorded and time stamped in the data. The amount of agreement will again depend on the SR and f_c used to acquire the data. Judgement will again be needed when evaluating if the timing results are satisfactory.

4.13 Input Range and Clipping.

The purpose of the input range test is to determine the maximum and minimum useful amplitude range of the DAS and provide information as to any non-linearity or clipping abnormalities that may occur.

4.13.1 Test Method.

A low frequency (10% f_c) triangle wave is injected into one channel using 120 percent of the FS amplitude. The data are acquired and evaluated based on the slope of the triangle wave. If digitizer counts are available, it is important to document both the voltage and count at which the channel clips. All channels should clip at the same voltage/count but this is not always the case due to non-linearity. A 16-bit analog/digital (A/D) will have 65,535 counts (2^{16}-1) that is typically divided into 32,767 counts (2^{16}/2-1) positive and 32,768 counts (2^{16}/2) negative. The volts/count is determined using the maximum peak-to-peak voltage range divided by the maximum counts (V_{pp} / 2^n). The test setup and procedures are shown in Figure 36 and Table 19.

Figure 36. Input Range test setup.

TABLE 19. INPUT RANGE TEST PROCEDURES

Input Range/Clipping (Saturation) Test Standard: ATC IOP		
Equipment Needed: • DAS • PSG		**Connections Needed** • Connect the load to the DAS as indicated in Figure 36, clip leads are acceptable
Step	**Action**	**Parameters**
1	Make Connections	N/A
2	Set DAS Parameters	**Trigger:** Rising Edge **Gain/Range:** Unity **Sample Rate:** Max for DAS **Filters:** AAF
3	Set PSG Parameters	**Input Amplitude:** 120% Full Scale **Frequency:** 100 Hz triangle wave
4	Acquire Data	Take care to catch the peak of the triangle as it enters a clip and exits a clip
5	Analyze Data	See Analysis Paragraph 4.13.2

4.13.2 Analysis.

Determine the slope of the line for the input triangle wave and compare that slope to the theoretical slope for the input triangle wave. If there are differences in the slope ascertain where the slopes diverge. Be sure to evaluate both the positive and negative sides of the waveform and record the following:

a. Identify the Positive / Negative clip levels (voltage and counts). This is the effective input range of the waveform recorder. Identify when non-linearity is first detected, typically the point where the slopes diverge.

b. Identify the clip abnormalities both positive and negative. A clip should be a flat line.

4.13.3 Results.

Record all results noting any abnormalities in the waveform. If possible adjust the software so any non-linear portion of a channel is never used. If the DAS software is not sophisticated enough to detect when it is in the clipped region it is important for the operator to accurately know the clip levels for each channel. Since there can be many channels in a system it is best if all channels clip at the same point. An example of a nonlinearity is shown in Figure 37.

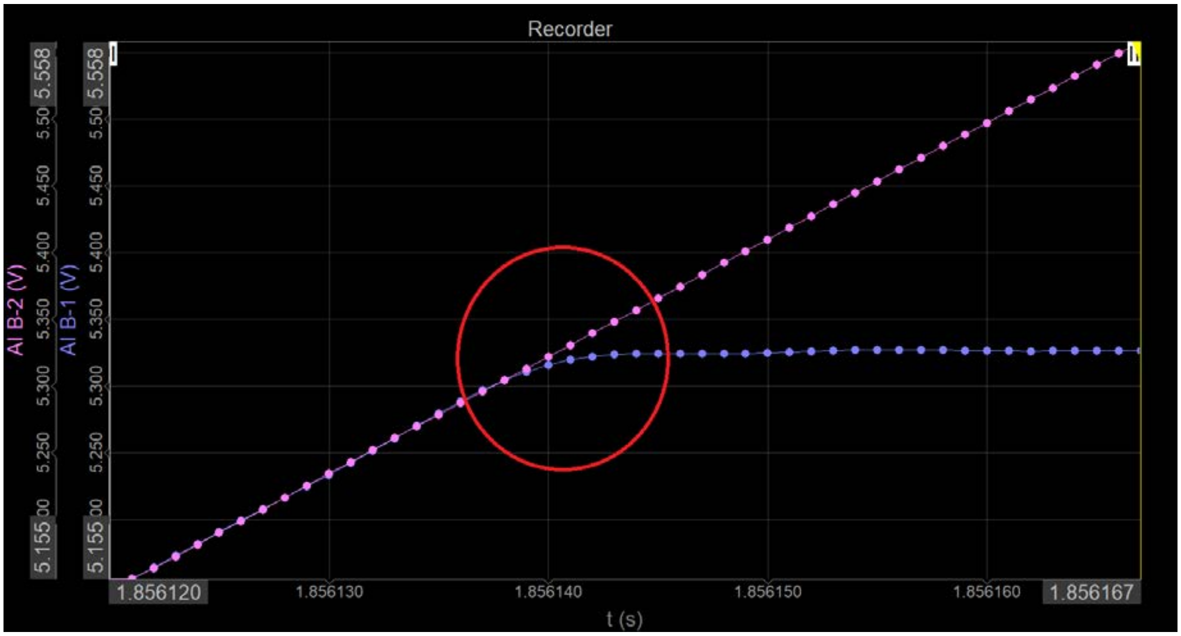

Figure 37. Nonlinearity example.

Note: Hard clips sometimes make Sigma-Delta ADC's act strangely. Therefore, if a Sigma-Delta ADC is being used, make sure a hard clip (>150% FS) is applied and the response thoroughly evaluated.

4.14 Input Resistance/Impedance.

The input impedance and resistance of an electrical circuit, is the measure of the opposition to current flow, both static (Resistance/DC) and dynamic (Reactance/AC), into the load network. In this case the load network is the DAS and it is connected to an external electrical source which is the transducer. The input admittance (1/impedance) is a measure of the DAS's propensity to draw current from the transducer. The transducer (source) is the electrical network that transmits the power. The DAS (load) is the electrical network that consumes power. If the DAS (load) draws more current then the sensor (source) can provide, then the signal being measured will be attenuated and will not be measured correctly. A sensors output impedance is typically low in comparison to a DAS's input impedance. A typical input impedance for a differential input channel of a DAS is 1 MΩ - 2 MΩ, while a typical piezoresistive sensor will have an output impedance of 350 Ω - 2200 Ω.

4.14.1 Test Method.

This test notes the input resistance and input impedance of the DAS. The resistance and impedance is measured with a calibrated LCR meter. The test setup and procedures are shown in Figure 38 and Table 20.

Figure 38. Input Resistance/Impedance test setup.

TABLE 20. INPUT RESISTANCE/IMPEDANCE TEST PROCEDURES

<table>
<tr><th colspan="3">Input Range/Clipping

Test Standard: ATC IOP</th></tr>
<tr><td colspan="2">Equipment Needed:
• DAS
• Calibrated LCR meter</td><td>Connections Needed
• Various connections needed. See steps below.</td></tr>
<tr><th>Step</th><th>Action</th><th>Parameters</th></tr>
<tr><td>1</td><td>Setup LCR Meter</td><td>AC Frequency: As stated in DAS technical specifications or as slow as LCR meter will allow.
Voltage: Approximately 1 V
Follow LCR meter instruction for test lead compensation and open/short compensation</td></tr>
<tr><td>2</td><td>Make first connection and note reading</td><td>Connect the LCR meter to the input channel positive + and ground
Note reading</td></tr>
<tr><td>3</td><td>Make second connection and note reading</td><td>Connect the LCR meter to the input channel negative - and ground
Note reading</td></tr>
<tr><td>4</td><td>Make third connection and note reading</td><td>Connect the LCR meter to the input channel negative - and input channel positive +
Note reading</td></tr>
<tr><td>5</td><td>Repeat steps 1-4 for resistance measurements</td><td>If LCR meter is not capable of measuring resistance a calibrated DMM may be used</td></tr>
</table>

4.14.2 Analysis.

Measurements should be recorded in a table. Impedance measurements should note the setup parameters used.

4.14.3 Results.

Results for both resistance and impedance should be compared to the datasheet for the DAS and are typically greater than 1 MΩ.

4.15 Excitation.

a. Transducers and/or sensors are classified as either active or passive. Passive sensors transform the physical energy into electrical energy directly and require no external power or excitation from the DAS. Active sensors require an excitation current or voltage from the DAS in order to transform the physical energy into electrical energy.

b. Active transducers can be excited using either a controlled current or voltage. Controlled or constant voltage (±10 V) is what is typically used with piezoresistive sensors and is typically referred to as sensor excitation. This testing will validate the excitation voltage from the DAS is accurate, constant, and noise free. To maintain a constant voltage level the excitation circuit includes excitation monitoring known as excitation sense. The sense leads continuously monitor and adjust the excitation voltage to maintain a constant voltage output to the sensor.

4.15.1 Excitation Voltage Accuracy and Noise.

The excitation voltage (DC) and noise (Vpp and RMS) will be measured in this test and the results documented for each system channel available in the DAS. Two channels are used for this test. The first channel will provide the excitation and sense input to a full bridge circuit while the second channel will be used to measure the noise from the first channel through the bridge circuit.

4.15.1.1 Test Method.

The Channel Excitation test setup and procedures are shown in Figure 39 and Table 21.

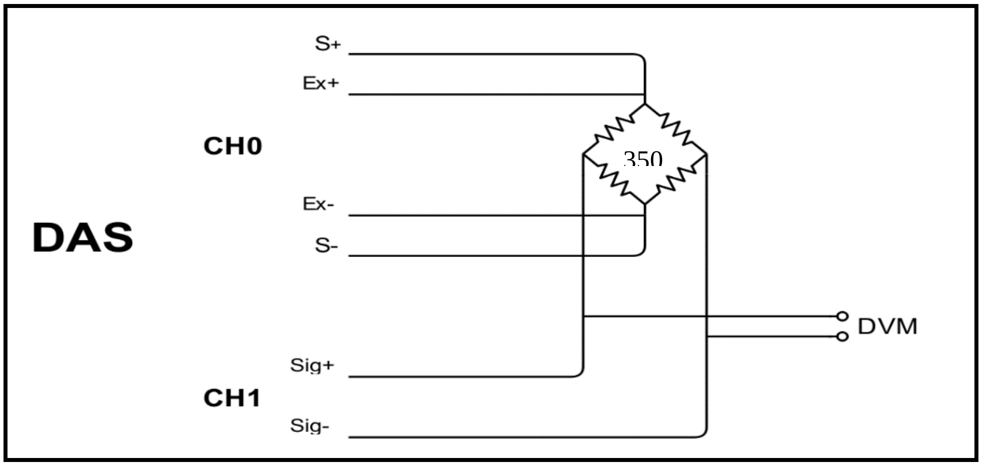

Figure 39. Channel Excitation test setup.

TABLE 21. EXCITATION ACCURACY AND NOISE TEST PROCEDURES

<table>
<tr><td colspan="3">Excitation Accuracy and Noise

Test Standard: ATC IOP</td></tr>
<tr><td colspan="2">Equipment Needed:
• DAS
• Input load (350 Ohm Bridge)
• Digital voltmeter (DVM)</td><td>Connections Needed
• Connect the excitation and sense leads of one channel as well as the signal leads as shown in Figure 39
• Connect DVM to the Signal leads of the DAS</td></tr>
<tr><th>Step</th><th>Action</th><th>Parameters</th></tr>
<tr><td>1</td><td>Make Connections</td><td>N/A</td></tr>
<tr><td>2</td><td>Set DAS Parameters</td><td>Trigger: Manual
Gain/Range: Unity
Sample Rate: Max for DAS
Filters: AAF
Excitation: 10 V</td></tr>
<tr><td>3</td><td>Acquire Data</td><td>Turn on Excitation and allow 30 seconds of warmup

Record value of excitation from DVM

Record one second of data from the channel not supplying the excitation to the bridge, Ch. 1 in Figure 39. This will be the excitation noise data</td></tr>
<tr><td>4</td><td>Analyze Data</td><td>See Analysis Paragraph 4.15.1.2</td></tr>
</table>

4.15.1.2 Analysis.

a. Compare the expected excitation voltage (set by the DAS software) with the DC measurement of the DMM.

b. Note the maximum and minimum voltage peaks along the record set. This is the peak-to-peak noise of the excitation. Take the RMS of the record length to determine the RMS noise of the excitation voltage.

4.15.1.3 Results.

Record the excitation voltage level and noise associated with the excitation for each channel.

4.15.2 Excitation - Drift.

a. Excitation Drift is described as the tendency for a DAS system to gradually increase or decrease its voltage excitation output over time to the sensor. Many sources of error can cause an apparent drift, like temperature effects (See paragraph 4.11).

b. It is important that the sensor excitation voltage remain stable over the duration of every test. To evaluate the stability, this test will determine the excitation voltage drift over a longer than normal length of time. A long record length will capture any drift in the excitation.

4.15.2.1 Test Method.

The Drift test procedures are shown in Table 22.

TABLE 22. DRIFT TEST PROCEDURES

Excitation Drift Test Standard: ATC IOP		
Equipment Needed: • DAS • Input load (350 Ohm Bridge)		**Connections Needed** • Connect the excitation and sense leads of one channel as well as the signal leads as shown in Figure 39
Step	**Action**	**Parameters**
1	Make Connections	N/A
2	Set DAS Parameters	**Trigger:** Manual **Gain/Range:** Unity **Sample Rate:** 1,250 S/s **Filters:** AAF **Excitation:** 10 V
3	Acquire Data	Turn on Excitation and allow typical stabilization time for DAS system. For a sanity check the channel may be monitored to see if sense leads are bringing any drift back to the expected excitation level Record data 10 X longer than typical data record
4	Analyze Data	See Analysis Paragraph 4.15.2.2

4.15.2.2 Analysis.

When analyzing the recorded data and obvious trends are not found, it may be necessary to separate the data record into groups of time, average, the amplitude results for the individual time groups and then compare the averaged results looking for a drift in the data. Note the drift characteristics such as V_{max} and V_{min}. Make sure to note any slight but sudden changes in voltage levels as this is indicative of the sense measurements taking place and the DAS adjusting itself to provide the correct excitation. These sense adjustments are likely to be more frequent and noticeable during the warm up period of the DAS.

4.15.2.3 Results.

The drift should be within range of the system excitation specifications and/or typically less than 0.01 percent of the expected excitation.

a. Note file size will be: $SR \times Acquisition\ Time\ \times bits\ of\ resolution / 8$ bytes.

b. Large data files will require more memory and longer processing times.

4.15.3 <u>Excitation - Current</u>.

a. Active transducers are typically excited with a constant voltage. A constant voltage requires the current to change (increase or decrease) in response to the changing load of the piezoresistive sensor. This testing will validate the excitation current is sufficient to drive the maximum required resistive load.

b. The channel excitation current test determines the maximum current the excitation can provide to the load. The load will start within range (typical load within DAS specifications), then gradually increase (lowering resistance) until the excitation current can no longer provide the expected excitation voltage set on the waveform recorder.

4.15.3.1 <u>Test Method</u>.

a. The Channel Excitation test setup and procedures are shown in Figure 40 and Table 23.

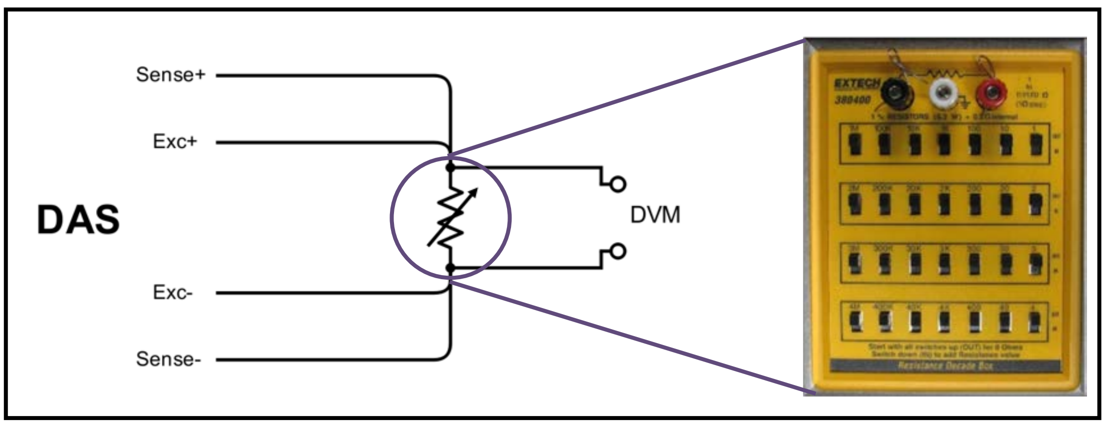

Figure 40. Excitation Current test setup.

TABLE 23. EXCITATION CURRENT TEST PROCEDURES

<table>
<tr><td colspan="3" align="center">Excitation Current

Test Standard: ATC IOP</td></tr>
<tr><td colspan="2">Equipment Needed:
• DAS
• Variable Load (Digital loads should have current and voltage readings available)
• DVM if using manual variable load</td><td>Connections Needed
• Connect the excitation and sense leads of one channel to the variable load.
• Connect the DVM across the variable load as well.</td></tr>
<tr><th>Step</th><th>Action</th><th>Parameters</th></tr>
<tr><td>1</td><td>Make Connections</td><td>N/A</td></tr>
<tr><td>2</td><td>Set DAS Parameters</td><td>Trigger: Manual
Gain/Range: Unity
Sample Rate: Max for DAS
Filters: AAF
Excitation: 10 V</td></tr>
<tr><td>3</td><td>Set variable load</td><td>Start the variable load at application use case (Typically 350 ohm)
Decrease resistance in 10 ohm increments until excitation voltage no longer remains constant.</td></tr>
<tr><td>4</td><td>Record current and resistance values</td><td>When excitation in previous step is no longer constant, record the current and resistance values</td></tr>
<tr><td>5</td><td>Analyze Data</td><td>See Analysis Paragraph 4.15.3.2</td></tr>
</table>

b. Equipment required.

(1) Variable load.

(2) Digital load should have voltage and current measurements available.

c. Connect the variable load to the channel excitation.

d. Set variable load to the application use value (within the channel excitation specification).

e. Increase the load in 10 milliamp (mA) increments or decrease the resistance proportionally until the excitation voltage no longer remains constant.

4.15.3.2 Analysis.

Note the maximum current and resistance on the variable load before the excitation voltage starts to decrease. This is the maximum load the DAS can source.

4.15.3.3 Results.

These results should match the waveform recorder specifications and for a 10 V excitation with a 350 Ω load the source current provided should be 28.57 mA.

4.15.4 Excitation - Sense.

a. Excitation Sense is a technique used in power supplies to produce a constant voltage independent of the changing load. An electronic feedback circuit is used to automatically make adjustments based on the difference between its intended output and its actual output. If the system is working, the actual will be very close to the intended.

b. Sense or "remote sense" requires separate leads to be connected to the load's input terminals, to measure the excitation voltage at the load. This will counteract the voltage drop due to the resistance of long cables by raising the voltage at the output terminals of the power supply. The sensing function only draws a very small amount of current, so there is practically no additional voltage drop due to the sense leads themselves and the drop in excitation voltage is canceled out providing the desired voltage at the source.

c. This test will determine the effectiveness of the excitation sense operation when used in conjunction with varying length cables. Set the excitation voltage to a desired level and verify the excitation voltage set with a short cable or no cable. Add cables of longer length and verify the excitation voltage remains the same for each different length. If measurements are identical, the sense system is functioning properly.

Note: Excitation sense only compensates for the DC voltage used to power piezoresistive sensors over long cables but provides no compensation or benefit for AC voltages traveling over the same long cables. See the Cable Testing IOP for more information on the effect of long cables on bandwidth. The Cable Testing IOP is available upon request from ATC.

4.15.4.1 Test Method.

The Excitation Current test procedures are shown in Table 24.

TABLE 24. EXCITATION CURRENT TEST PROCEDURES

Excitation Current Test Standard: ATC IOP		
Equipment Needed: • DAS • 100, 250, and 500 foot cables • DVM • Input Load (Typically 350 Ω)		**Connections Needed** • Connect one long cable at a time to the excitation and sense leads of one DAS channel • Connect input load to the far end of the long cable. • Connect the DVM directly to the input load NOT through the cable
Step	**Action**	**Parameters**
1	Make Connections	N/A
2	Set DAS Parameters	**Trigger:** Manual **Gain/Range:** Unity **Sample Rate:** Max for DAS **Filters:** AAF **Excitation:** 10 V
3	Record excitation value	Record excitation voltage as read by the DVM
4	Analyze Data	See Analysis Paragraph 4.15.4.2
5	Repeat steps 2-4	Repeat this procedure with all other cable lengths

4.15.4.2 Analysis.

Note the DVM reading is less than 0.1 percent of FS.

4.15.4.3 Results.

The DVM reading should match the expected set excitation value. If sense is working, the excitation voltage will adjust to compensate for the voltage drop over the long cables.

4.16 Common-Mode Rejection Ratio (CMRR).

Common-mode rejection ratio of a DAS is the ability of the differential amplifier within the DAS to reject common mode signals. CMRR is the metric used to quantify the ability of the device to reject the unwanted common-mode signals (See Section 3.7). A common-mode signal appears simultaneously and in-phase on both the signal+ and signal- input leads. An ideal differential amplifier would have an infinite CMRR, however this is not achievable in practice, so a CMRR of -80 dB or lower is typically considered good common-mode noise rejection.

Common-mode noise is often caused by EMI and is most evident when a low amplitude differential input signal must be amplified while in the presence of a large common-mode input.

4.16.1 Test Method.

To determine the CMRR, a common-mode voltage signal must first be generated and injected into the signal+ and signal- inputs of one DAS channel. A special adapter has been made using 350 Ω resistors to inject an identical common-mode signal into the DAS. Test with multiple frequencies of 60 Hz, 100 Hz, and 400 Hz at 90 percent FS amplitude using the special common-mode adapter as shown in Figure 41. Acquire data and determine the CMRR (dB). Test procedures are shown in Table 25.

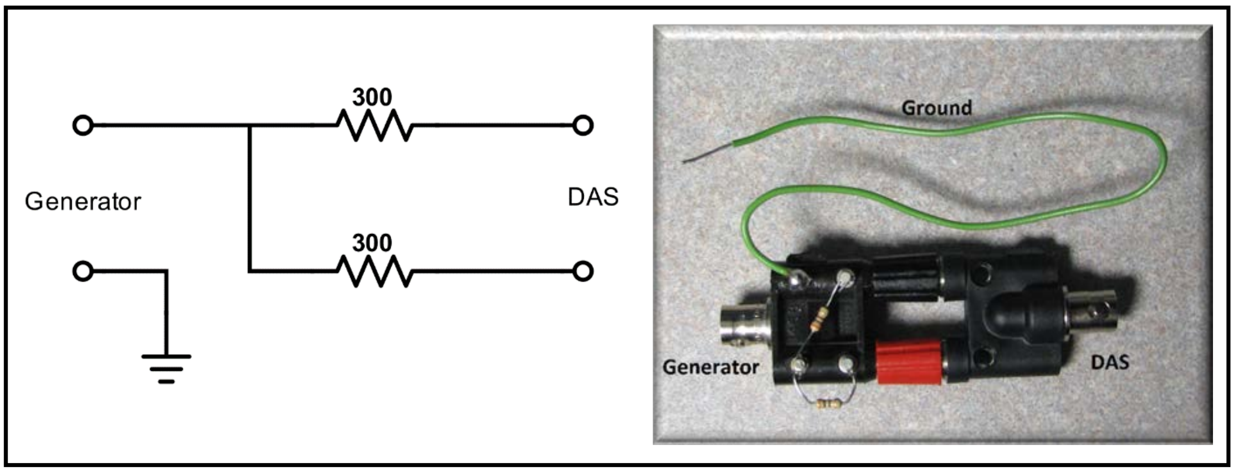

Figure 41. CMRR test setup.

TABLE 25. CMRR TEST PROCEDURES

<table>
<tr><th colspan="3">Common Mode Rejection Ratio

Test Standard: ATC IOP</th></tr>
<tr><td colspan="2">Equipment Needed:
• DAS
• CMRR Adapter
• PSG</td><td>Connections Needed
• Connect the PSG output to the “Generator” side of the CMRR adapter. Connect the DAS input channel to the “DAS” side of the adapter</td></tr>
<tr><th>Step</th><th>Action</th><th>Parameters</th></tr>
<tr><td>1</td><td>Make Connections</td><td>N/A</td></tr>
<tr><td>2</td><td>Set DAS Parameters</td><td>Trigger: Manual
Gain/Range: Unity
Sample Rate: Max for DAS
Filters: None if possible</td></tr>
<tr><td>3</td><td>Set PSG Parameters</td><td>Input Amplitude: 90% full scale
Frequency: 60 Hz Sine Wave</td></tr>
<tr><td>4</td><td>Acquire Data</td><td>Record at least 3 periods of the input waveform</td></tr>
<tr><td>5</td><td>Analyze Data</td><td>See Analysis Paragraph 4.16.2</td></tr>
<tr><td>6</td><td>Repeat steps 2-5 for other frequencies</td><td>Repeat for 100 Hz and 400 Hz (Other frequencies as desired)</td></tr>
</table>

4.16.2 Analysis.

a. In each record set, determine V_{in} and V_{out}.

b. V_{out} is the maximum amplitude in the data set and V_{in} is the input amplitude from the PSG. Calculate the CMRR for each frequency tested using Equation 8. An FFT may be required to determine the magnitude if the common-mode signal out if it is too small to accurately measure.

$$CMRR(dB) = 20log_{10}\frac{V_{out}}{V_{in}} \qquad \textit{(Equation 8)}$$

4.16.3 Results.

Compare the results of the CMRR test to the CMRR listed in the waveform recorder specifications of follow the rule of thumb listed below:

a. -40 dB CMRR very poor noise rejection.

b. -50 dB CMRR poor noise rejection.

c. -60 dB CMRR average noise rejection.

d. -70 dB CMRR good noise rejection.

e. -80 dB CMRR very good noise rejection.

f. -90 dB CMRR excellent noise rejection.

g. -100 dB CMRR world class noise rejection.

4.17 Crosstalk.

a. Crosstalk is any phenomenon by which the signal on one channel is transmitted to another channel causing an undesired effect (see Figure 42). Crosstalk is usually caused by mutual capacitance, inductance, or conductive coupling from one channel to another. Crosstalk can be a significant issue in data acquisition systems if care is not taken in the choice of wiring or channel setup/layout.

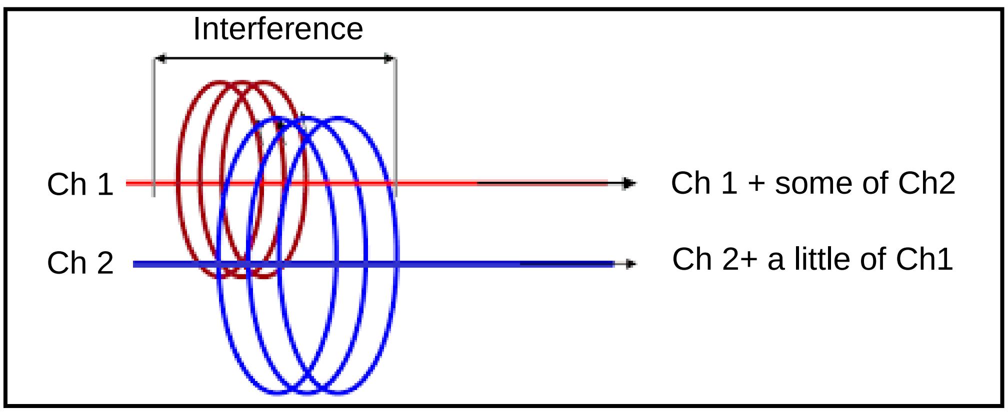

Figure 42. Depiction of crosswalk between channels.

b. Crosstalk can also exist between traces on a printed circuit board (PCB) within the DAS causing interference internal to the system. This is the type of crosstalk being tested for in this section, and it is accomplished by injecting a signal into all of the channels on a single card except one, then monitoring the individual channel looking for artifacts of the input signal from the other channels.

4.17.1 Test Method.

The Crosstalk test setup and procedures are shown in Figure 43 and Table 26.

Figure 43. Crosstalk test setup.

TABLE 26. CROSSTALK TEST PROCEDURES

Crosstalk Test Standard: ATC IOP		
Equipment Needed: • DAS • Input load (Typically 350 Ω) • PSG		**Connections Needed** • Connect the PSG to all channels on DAS except channel under test • Connect input load to channel under test
Step	**Action**	**Parameters**
1	Make Connections	N/A
2	Set DAS Parameters	**Trigger:** Set to Manual **Gain/Range:** Unity **Sample Rate:** Max for DAS **Filters:** None if possible
3	Set PSG Parameters	**Input Amplitude:** 90% full scale **Frequency:** 10% of filter used else10 kHz if no filter used
4	Acquire Data	Record at least 5 periods of the input signal on each channel
5	Analyze Data	See Analysis Paragraph 4.17.2
6	Repeat steps 2-5	Repeat until every channel has been tested for Crosstalk If DAS has multiple cards or slices, no additional testing is necessary if cards are identical

4.17.2 Analysis.

Find the RMS value of the input signal (V_{in}) and the RMS value of the channel under test (V_{out}) (Equation 9). An FFT may be required to determine the magnitude if the crosstalk signal if it is too small to accurately measure.

$$Crosstalk(dB) = 20log_{10}\frac{V_{out}}{V_{in}} \qquad \textit{(Equation 9)}$$

4.17.3 Results.

Compare the Crosstalk results to the Crosstalk listed in the waveform recorder specifications.

4.18 <u>Channel Synchronization</u>.

Over the years two different digitizer sampling problems have been detected. The first being a sample time alignment problem detected when evaluating channels that are sampled at different rates. The second was a time alignment problem detected when evaluating channels that are sampled at the same rate but the channel hardware resides in a separate packages (i.e., not all channels on the same back plane). Several analysis routines (i.e., Crew Injury) require data from multiple channels for evaluation purposes so it is extremely important that all data align properly in time.

4.18.1 <u>Test Method</u>.

The Channel Synchronization test will determine if all channels are asynchronous or synchronous within the DAS, whether the DAS is a standalone unit, or a set of two or more units connected together with synchronization cables. Inject a 90 percent FS amplitude sinewave at 1 percent f_c into at least two channels of each unit. Set each channel up with a different sample rate but the identical filter using the maximum f_c available. Compare the trace alignment for each channel one to another, verifying that the channel alignment is within one sample of the lower of the two channels evaluated. The Channel Synchronization test setup and procedures are shown in Figure 44 and Table 27.

Figure 44. Channel Synchronization test setup.

TABLE 27. CHANNEL SYNCHRONIZATION TEST PROCEDURES

Channel Synchronization Test Standard: ATC IOP		
Equipment Needed: • DAS • PSG		**Connections Needed** • Connect the signal generator to the DAS as indicated in Figure 44
Step	**Action**	**Parameters**
1	Make Connections	N/A
2	Set DAS Parameters	**Trigger:** Set to Manual **Gain/Range:** Unity **Sample Rate:** Set each channel to different sample rate **Filters:** AAF
3	Set PSG Parameters	**Input Amplitude:** 90% full scale **Frequency:** 10% of filter used
4	Acquire Data	Record at least 5 periods of the input signal
5	Analyze Data	See Analysis Paragraph 4.18.2

4.18.2 Analysis.

Overlay all of the channels to find any deviations outside of the expected noise. Determine the difference in the sample times between channels. Consider using the zero-crossing times as a reference.

4.18.3 Results.

The channel alignment should be within one sample of the slower of the two channels evaluated. Keep in mind, integrated filters will have an effect on the sample times measured which could cause the channel alignment to be off more than one sample. Figure 45 shows what to expect with perfect synchronization.

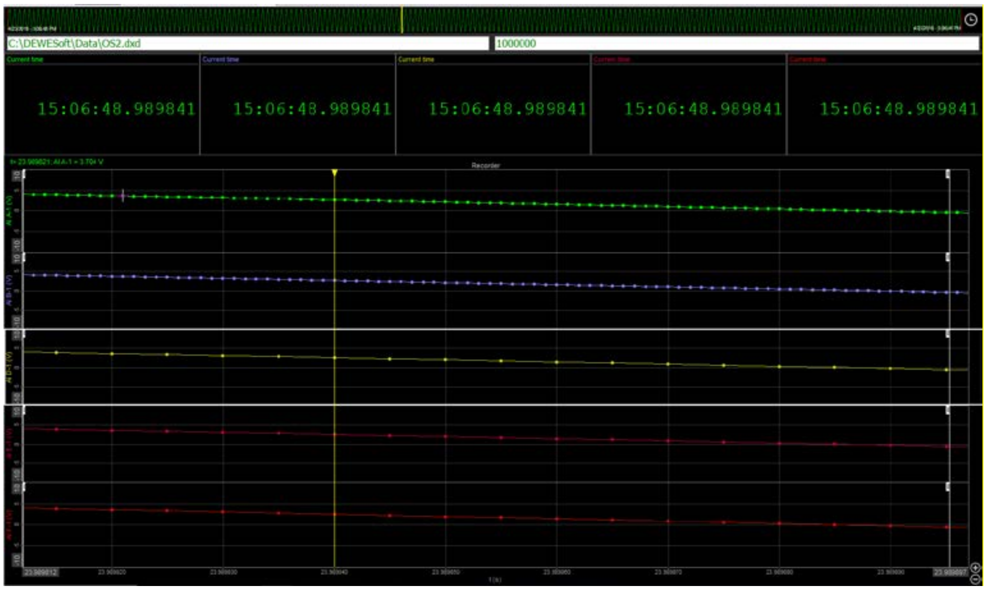

Figure 45. Channel synchronization.

4.19 Auto Balance.

An auto-balance feature automatically adjusts the signal input leads until they measure zero volts between the signal+ and signal-. This removes any sort of DC offset by compensating internally with a known bias voltage. For example, a slightly unmatched bridge would show a non-zero voltage between signal+ and signal-. After the auto balance operation, the same unmatched bridge would produce a zero voltage between signal+ and signal-. By adjusting the balance to zero, the FS range of the input amplifier is now available.

4.19.1 Test Method.

This test will measure the minimum and maximum DC offset voltage that can be compensated for, and the accuracy of the compensation. To artificially offset the signal leads, inject a known DC signal into the signal leads using the offset option of the PSG. Execute the auto-balance routine and verify the amount of offset measured by the DAS is zero or near zero. The Auto Balance test setup and procedures are shown in Figure 46 and Table 28.

Figure 46. Auto Balance test setup.

TABLE 28. AUTO BALANCE TEST PROCEDURES

AutoBalance Test Standard: ATC IOP		
Equipment Needed: • DAS • PSG		**Connections Needed** • Connect the signal generator to the DAS as indicated in Figure 46
Step	**Action**	**Parameters**
1	Make Connections	N/A
2	Set DAS Parameters	**Trigger:** Set to Manual **Gain/Range:** Unity **Sample Rate:** Max for DAS **Filters:** AAF
3	Set PSG Parameters	**Input Amplitude:** Positive DC offset **Frequency:** DC Offset only
4	Acquire Data	Record 1 second of data
5	Analyze Data	See Analysis Paragraph 4.19.2
6	Repeat steps 2-5	Repeat using an increasing positive offset as well as a decreasing negative offset until the DAS can no longer compensate the offset out

4.19.2 Analysis.

Determine the minimum and maximum offset voltages that can be compensated out. When the minimum and maximum voltages are found, determine the accuracy of the overall compensation. Also measure the time required to execute the auto-balance routine for a full up system.

4.19.3 Results.

Document the minimum and maximum accuracy and time information for several individual channels, and also document the overall time required to auto-balance a full system. The time required to auto-balance a full system can indicate an aging and failing system if time required for a full balance increases dramatically from baseline.

4.20 Test Bus.

A test bus is a very important tool to assist in the testing and calibration of data acquisition systems, though not all DAS's are equipped with a test bus input. Typically, a test bus consists of one software selectable input that is distributed internally to all channels within a DAS chassis. Sometimes a test bus is limited in its electrical characteristics so it is important to characterize the test bus limitations before conducting system tests using the test bus input. Bandwidth, Noise, ENOB, Input Range, and Slew Rate are important characteristics that can have a large influence on the results. Conduct these tests for a single channel or group of channels using both the test bus input and the normal channel input. Compare the results and document any limitations. If the test bus degrades the results, as compared to the normal channel input, then use of the test bus may be unsatisfactory for some testing. If not, the test bus may be used for many tests. Bandwidth restrictions are the most prevalent in a test bus so pay careful attention to the bandwidth results. Even if the bandwidth through the test bus is restricted, tests that require a lower bandwidth may still be used.

4.21 Electrostatic Discharge (ESD).

ESD can cause problems with both DAS and transducer functionality and is an inherent issue in some test scenarios. Airdrop testing is especially susceptible to ESD since the fabric parachute rapidly deploys, causing electrostatic charge to build up. Without a solid ground available in the air to dissipate the charge buildup (i.e., Earth ground), any electronics on the airdrop payload are susceptible to ESD interference. ESD can cause noise on data channels, an offset shift in data, or DAS recording to prematurely stop/reset. Effects of ESD are usually not permanent to the DAS and just affect the current recording, although prolonged long-term effects are harder to quantify. Previous testing has shown that ESD discharge on both the DAS and transducers or cables connected to the DAS can cause noise in the data and/or DAS malfunction. Therefore, it is important to introduce ESD discharges to both the DAS and attached transducers that will be commonly connected to it, while the DAS is powered on and recording. An ESD discharge to a sensor that is wired to the DAS can cause more issues than an ESD discharge to the DAS housing itself.

4.21.1 Test Method.

ESD testing can be conducted with an ESD gun with a variable output on either contact or air discharge delivery modes. Although one can achieve better control on a specific discharge point with contact mode, contact mode often has a lower maximum discharge setting (under 10 kilovolt (kV)) versus an air contact discharge (15 kV or more). Test items should be electrically isolated from the surrounding area (i.e., placed on non-conductive surface and powered by a battery) and ESD discharges should start low and progress to higher voltages. Multiple discharges should be conducted at each voltage level to ensure there is no interference since ESD may not dissipate the same way each time, especially with air discharge mode. Testing should continue to as high an ESD value as possible (at least up to 15 kV), or until the DAS consistently indicates an anomaly. ESD test procedures are shown in Table 29.

TABLE 29. ESD TEST PROCEDURES

ESD Test Standard: International Electrotechnical Commission (IEC) 61000-4-2[5] ESD		
Equipment Needed: • DAS • Keytek Mini Zap MZ-15 • Standard Sensor Payload		**Connections Needed** • Connect standard sensor payload to the DAS under typical operating configuration
Step	**Action**	**Parameters**
1	Make Connections	N/A
2	Set DAS Parameters	**Trigger:** Set to Manual **Gain/Range:** Unity **Sample Rate:** Max for DAS **Filters:** AAF
3	Set Keytek Mini Zap Parameters	**Output Potential:** 2 kV **Frequency:** 1 pulse per second
4	Acquire Data	Record 30 seconds of data
5	Analyze Data	See Analysis Paragraph 4.21.2
6	Repeat steps 2-5	Repeat test increasing Output Potential in 1 kV increments or until DAS repeatedly shows failure at same Output level
7	Repeat steps 2-6	Repeat test at different test points on DAS where electronic components might be most susceptible to electric interference

4.21.2 Analysis.

Determine the output potential of the ESD simulator that causes frequent and consistent failures of the DAS. Check data record and DAS functionality after each test for missed data points or device failure. Look for points on chassis where ESD may not be properly grounded, or routed away from sensitive electrical components.

4.21.3 Results.

Document any failures as well as point of contact (or air discharge location) where the failures occur. Failures are more common at higher ESD potentials and care needs to be taken to determine if testing events are likely to create high levels of electrostatic discharge. A failure of this test does not in itself indicate an issue with the DAS under test, only that the device is susceptible to ESD at and above the levels of failure, so care must be taken to mitigate risks during testing. ESD may be present during test events and a separate evaluation may need to be undertaken to understand those risks.

4.22 Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC).

EMI and EMC testing is conducted to see if instrumentation interferes with the electronics of the test article. Even if the DAS is not radiating a radio frequency (RF) signal, or it doesn't directly connect to the test article's electronics, it can have unintended and adverse effects on surrounding electronics. EMI/EMC testing is conducted to verify the DAS is not causing any interference and is required to get airworthiness approval for the DAS to be used on an aircraft. EMI testing is usually conducted in a laboratory or anechoic chamber with a spectrum analyzer measuring the RF environment; the DAS is powered on and used in different operational modes to see if it is emitting any spurious RF emissions. For EMC testing, either the test article or a simulated version of the test article is used with the DAS powered on and connected to it. If the DAS does not directly connect to the test article, then EMC testing may not be required for airworthiness approval. Relevant operational modes of the test article are checked to see if the DAS causes adverse reactions when connected to it. Although EMI testing can be done in general, EMC testing is platform specific and needs to be conducted with each test article to see if it causes adverse consequences.

5. DATA REQUIRED.

Data required during DAS testing are provided in the individual subtests of Section 4.

6. PRESENTATION OF DATA.

Samples of how data can be presented are provided in the individual subtests of Section 4.

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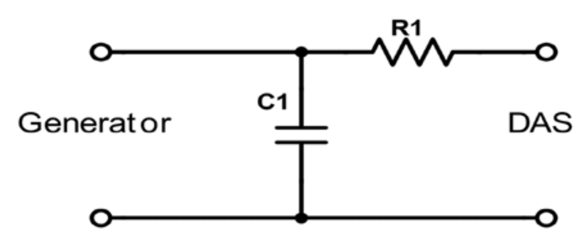
APPENDIX A. INTEGRATED ELECTRONICS PIEZOELECTRIC (IEPE) ACCURACY / CHARACTERISTICS.

A.1 IEPE CHARACTERISTICS.

IEPE is a charge transducer (see Appendix B) that has a built in amplifier and impedance conversion electronics. Due to the nature of charge transducers having an output signal that is quite small, the electrical signal produced by the sensing element can be highly susceptible to noise. The electronics integrated into the IEPE transducers are used to amplify and condition these small signals to increase noise immunity. The electronics convert the high impedance signal from the piezoelectric sensing element into a low impedance voltage signal, allowing the signal to be transmitted across long cable lengths without loss of signal quality or need for special low noise cabling. The electronics within the transducer is powered with approximately 27 V DC at a constant current of 4 mA to 20 mA. The AC signal from the sensing element rides on the same wires as the 27 V DC power, so only two wires are required. The main disadvantage of IEPE type sensors is that they do not have a DC response, as they are AC coupled with a relatively short discharge time constant.

A.2 GAGE SIMULATION CIRCUIT.

PCB Piezotronics*** makes an IEPE gage simulator that allows a voltage to be injected into the measurement system for testing purposes. These simulators work well in the field for diagnostics purposes but they are not accurate enough for validating instrumentation. The RC circuit in Figure A-1 was used to act as a simple gage simulator circuit for the purpose of injecting accurate voltage levels into the IEPE coupler circuitry of the DAS for comparison. Using two DAS channels, one setup for IEPE mode and one setup for voltage mode, the input voltage (voltage pulse) is injected into the gage simulator and recorded simultaneously on the DAS voltage channel, while the IEPE channel measures the response from the gage simulator. Both signals should have identical amplitude results validating the IEPE coupler is functioning properly.



R1 = 10 Ohm - Output Impedance of Gage
C1 = 40 pF - Best Guess Capacitance to Use

Figure A-1. RC circuit.

*** The use of brand names does not constitute endorsement by the Army or any other agency of the Federal Government, nor does it imply that it is best suited for its intended application.

APPENDIX A. INTEGRATED ELECTRONICS PIEZOELECTRIC (IEPE) ACCURACY / CHARACTERISTICS.

A.3 DETERMINE DISCHARGE TIME CONSTANT (DTC).

a. Since IEPE is an AC coupled measurement it has an associated DTC that is proportional to the capacitor used in the IEPE coupler. DTC is defined as the time it takes for the signal to discharge to 37 percent of its peak value. Along with this, there should be a 1:1 ratio between the percentage of instantaneous charge and the Time Constant (TC), up to the first 10 percent of the TC. This means that at 1 percent of the TC, 1 percent of the signal will be discharged; at 10 percent TC, 10 percent of the signal will be discharged, etc. Using this relationship, the accuracy of your data can be determined based on the DTC. A standard DTC is shown in Figure A-2.

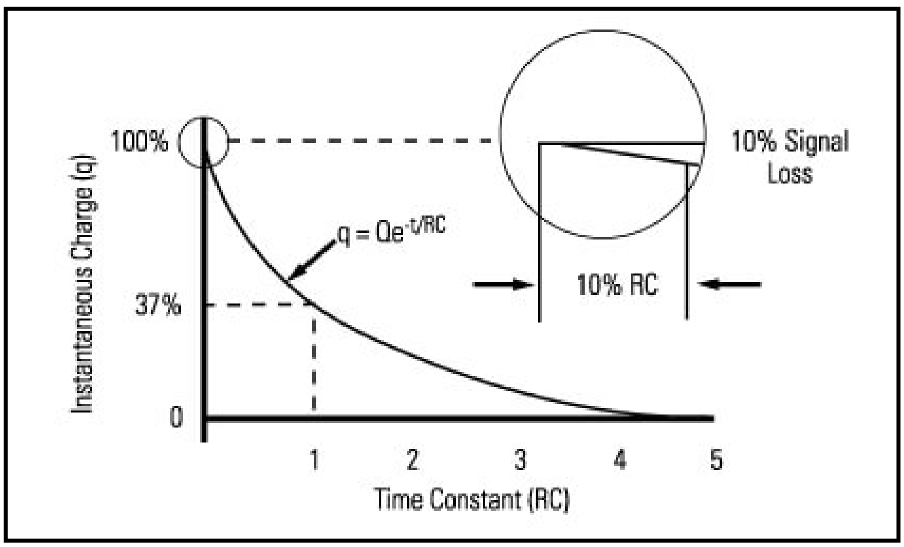


Figure A-2. Standard DTC

b. To measure DTC, set the generator to pulse mode with an amplitude of 1 V, and offset of 500 millivolt (mV). Set the pulse width long enough to allow the user to observe the entire discharge cycle (see Figure A-3), as the pulse should extend well beyond the normal DTC cycle. Make sure to set the sampling frequency 10 times faster than the cutoff frequency.

APPENDIX A. INTEGRATED ELECTRONICS PIEZOELECTRIC (IEPE) ACCURACY / CHARACTERISTICS.

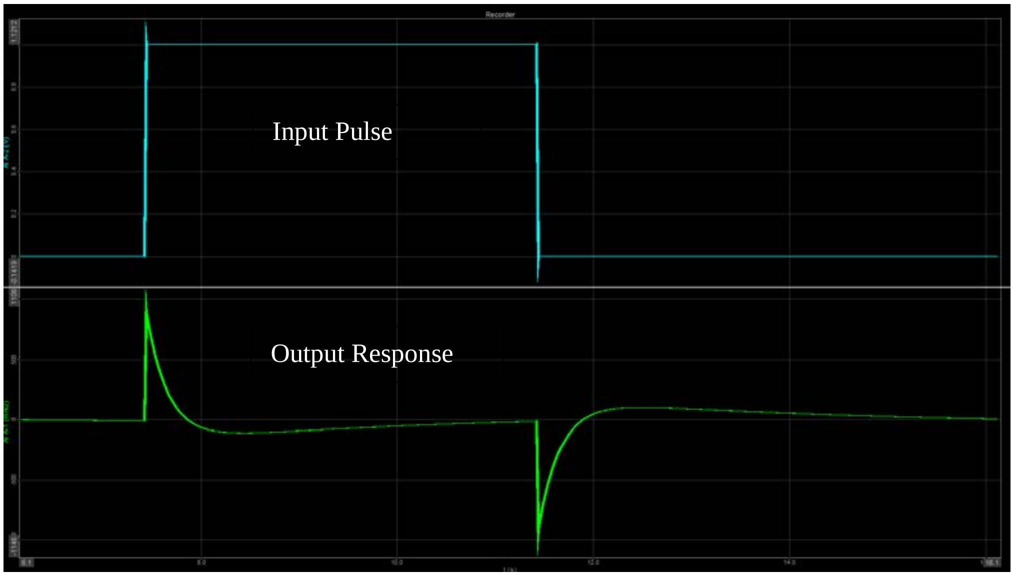


Figure A-3. Complete TC cycle.

c. Store the data using the DAS and record the time the peak occurs (T1). Record the time where the signal discharges to 37 percent of the peak (T2) as shown in Figure A-2. The difference between T1 and T2 is the DTC.

A.4 DETERMINE/VERIFY ACCURACY OF IEPE CONDITIONER.

a. Peak Accuracy. Connect the output of the PSG to both a Voltage channel and IEPE channel through the RC network (transducer simulator). Measure and determine the difference between the peak amplitude of each signal (should be less than 0.10 percent).

b. Frequency Sweep. Inject a sine sweep (1 kHz - 1 MHz) and observe the captured waveform for any anomalies.

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APPENDIX B. CHARGE CHARACTERISTICS/ACCURACY.

B.1 CHARGE INFORMATION.

Charge transducers are made with piezoelectric elements which require an external charge amplifier to convert the charge signal into a voltage signal so it can be measured with a DAS. The charge amplifier typically consists of a high gain inverting voltage amplifier with a metal–oxide–semiconductor field-effect transistor at the input, to achieve the high insulation resistance the piezoelectric element requires. Maintaining the high insulation resistance ($> 10^{12}\Omega$) from the sensor to the charge amplifier is critical. If the insulation resistance is not maintained, drift and noise will be a problem when trying to make measurements. Simple problems such as wet or damp connections can cause significant noise and/or drift. Large caliber chamber pressure measurements are often the most critical measurements made by ATEC and require accuracy to less than 1.0 percent, so noise and drift are very problematic.

B.2 CHARGE CALIBRATION/CHARGE CAPACITOR.

a. Charge amplifiers are typically temperature sensitive, adding to the problematic nature of the measurement. For this reason, it is recommended that the charge amplifier be calibrated before each use, allowing ample time for the electronics to warm up and stabilize. Likewise, the Calibration Capacitor used to calibrate the charge amplifier is also temperature sensitive so maintaining calibration of the charge capacitor is also critical. The charge capacitors are typically calibrated at an ambient temperature of 21.1 °Celsius (°C) (70 °Fahrenheit (°F)) so when using them to calibrate the charge amplifier make sure the temperature is within a few degrees of 21.1 °C (70 °F).

b. Calibrating the charge amplifier is a simple process and can be accomplished by injecting a DC level voltage into a calibration capacitor to produce a known amount of charge (see Figures B-1 and B-2). Charge amplifiers are typically inverting amplifiers so a positive DC input voltage will produce a negative output from the charge amplifier and a negative DC input voltage will produce a positive output from the charge amplifier. For example, a typical E30MAZ pressure transducer produces a charge of 30,000 picocoulombs (pC) at 100,000 pounds per square inch (psi), so to simulate that using a calibration capacitor, inject -3 V into a 10,000 pf capacitor to produce 30,000 pC into the charge amplifier.

APPENDIX B. CHARGE CHARACTERISTICS/ACCURACY.

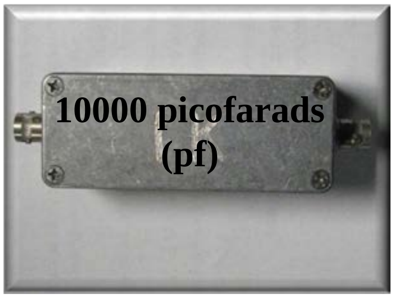


Figure B-1. Calibration capacitor.

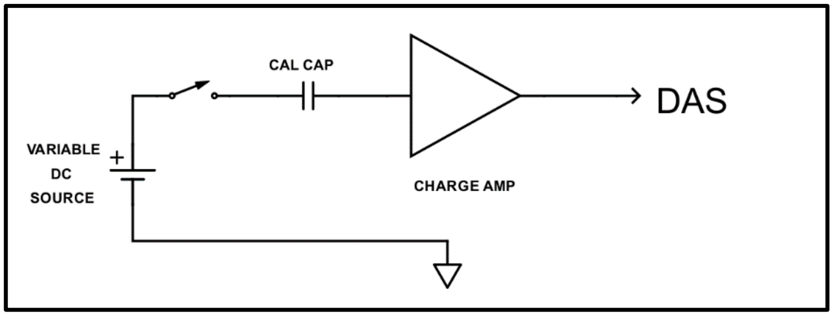


Figure B-2. Calibration diagram.

c. Typical E30MAZ gage sensitivity = 0.3pC/psi

0.3pC/psi * 100,000psi = 30,000pC

d. Typical Simulation = -3.0V * 10,000pf = 30,000pc, equivalent charge for 100,000psi.

e. To determine the Charge Amplifiers Discharge Time Constant and Peak Accuracy, use the same approaches outlined for IEPE transducers in Appendix A.

APPENDIX C. TOP SIX CONCERNS FOR NEW DATA ACQUISTION SYSTEM INSTRUMENTATION.

C.1 OUT OF BAND ENERGY.

Out of Band Energy encompasses three different issues:

a. Traditional Aliasing. Signal above Nyquist "folds over", contaminating true data below Nyquist. The aliased frequency can be calculated using Equation C-1.

$$Fa = Fs*n-F \qquad \textit{(Equation C-1)}$$

where:

Fa = frequency of "alias".
F = frequency of input signal.
Fs = sample rate.
n = integer number of sample rate (Fs) closest to input signal frequency (F).

(1) Assume you have a 4 kHz passband (F) and a sample rate (Fs) of 40 kHz, then the frequency range that can fold back into the passband is 36 kHz - 44 kHz for a successive approximation A/D. Due to the oversampling of a sigma Delta A/D, the fold back signal would be at a much greater frequency and most likely not an issue (see Figure C-1).

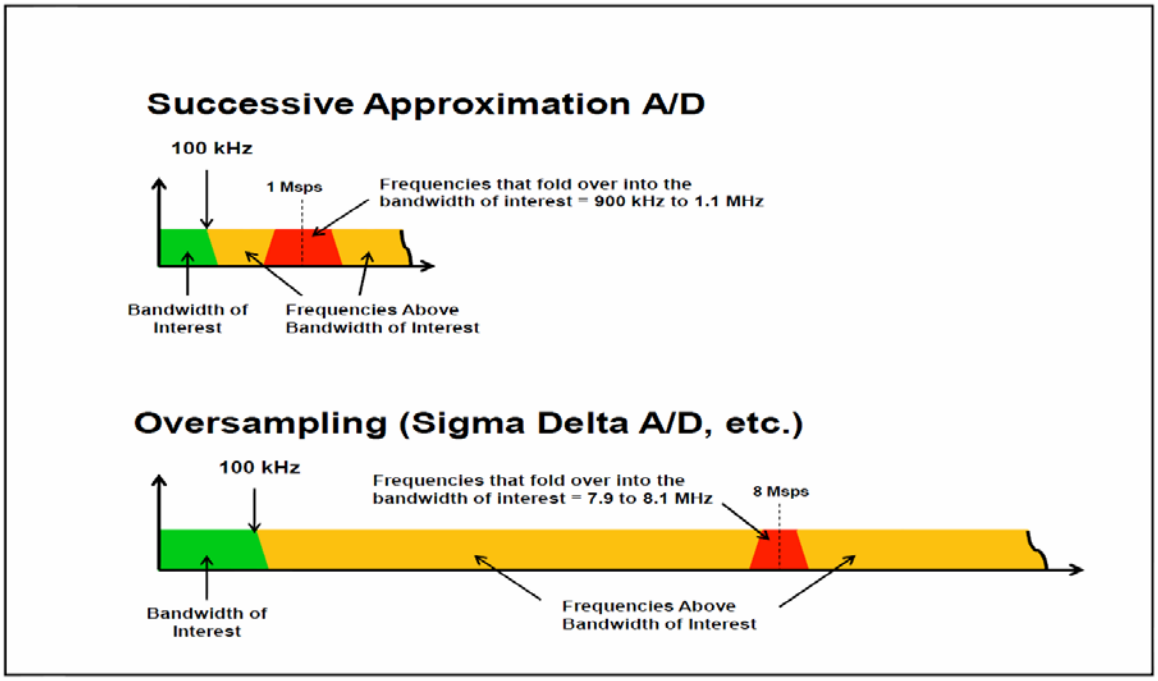


Figure C-1. Fold back example.

APPENDIX C. TOP SIX CONCERNS FOR NEW DATA ACQUISTION SYSTEM INSTRUMENTATION.

(2) The fix for this problem is to meet the specifications shown in Figure C-2.

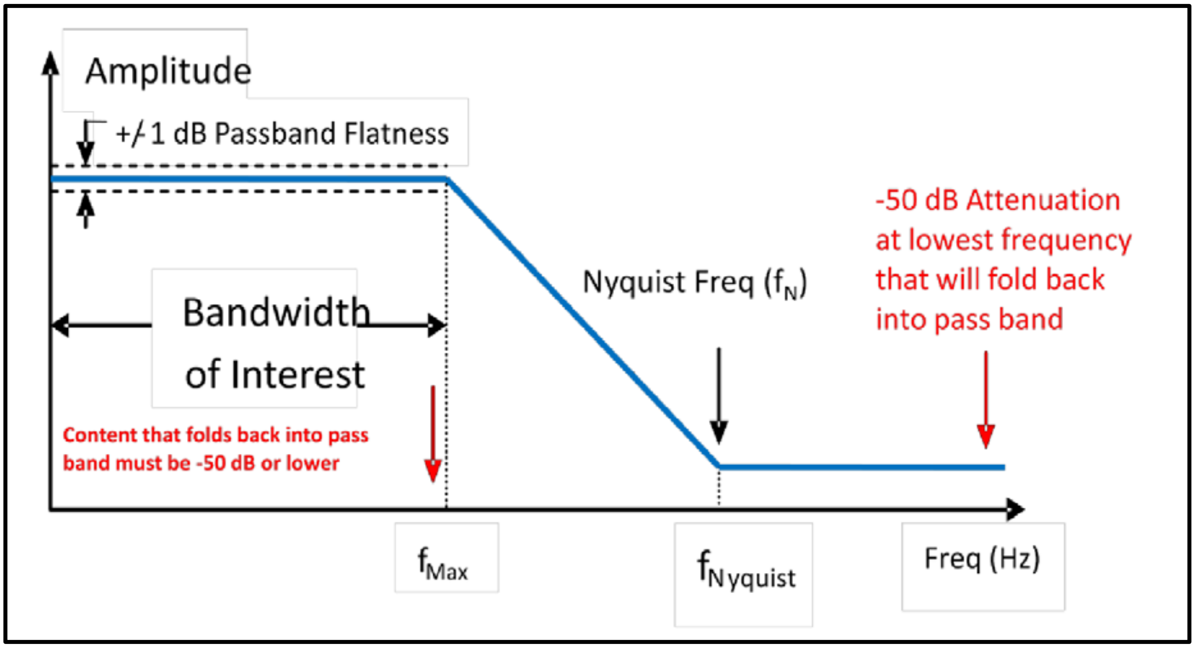


Figure C-2. Fold back specifications.

(3) Using the example from Figure C-2, fmax = 4 kHz, fnyquist = 20 kHz (1/2 sample rate), the theory says at 20 kHz the signals passed must be attenuated by 50 dB.

b. Transducer Resonance. Undamped accelerometers can resonant (overshoot) 2x to 1000x above the expected input level. If not careful, this overshoot can be interpreted as real acceleration data (see Figure C-3).

APPENDIX C. TOP SIX CONCERNS FOR NEW DATA ACQUISTION SYSTEM INSTRUMENTATION.

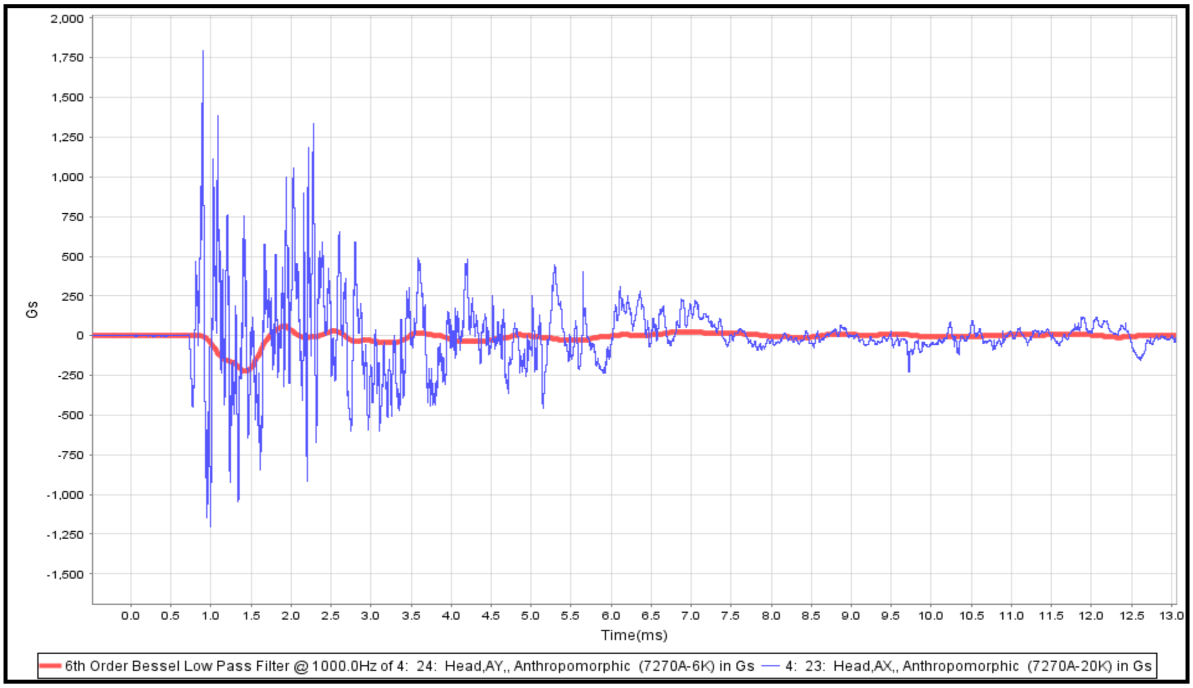


Figure C-3. Overshoot example.

(1) The blue trace in Figure C-3 represents the resonating accelerometer (7270-6 K rings at 200 kHz, Blue Trace) and it indicates 1800 g. The actual level could be as high as 7200 g due to the attenuation of the cable (6 dB/octave at 40 kHz). The red trace represents the true expected level of 250 g using the 1 kHz channel frequency class. The difference between the resonate signal and the expected signal is approximately 30X.

(2) The fix for this problem is to build in headroom. As stated in the 2010 Shock and Vibration Handbook[6], the headroom should be set to 50x. If there is also a potential for slew rate issues, headroom of greater than 50x should be used.

(3) Example using the D4D with a 16 bit A/D and a 5V (+/- 2.5V) input range:

(a) Signal maximum value = 2.5 V / 50 = 50 mV.

(b) Volts / Count = 5 V / 65536 = 76.3 uV/Ct.

(c) Signal maximum count = 50 mV / 76.3 uV/Ct = 655.36 Ct.

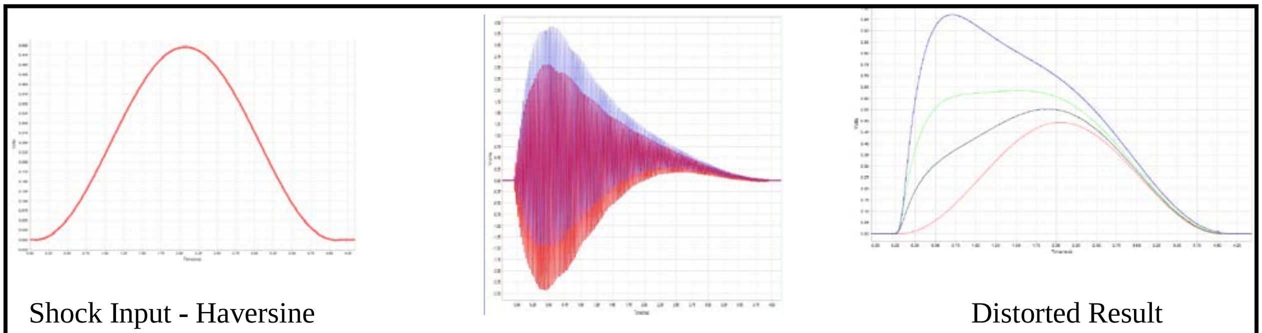
(d) Dynamic Range = 20 * log (655.36 Ct) = 56.3 dB.

APPENDIX C. TOP SIX CONCERNS FOR NEW DATA ACQUISTION SYSTEM INSTRUMENTATION.

(e) ENOB = (Dynamic Range – 1.76) / 6.02 = (56.3 dB – 1.76) * 6.02 = 9.06 bits.

(4) Hence we would use only 9 bits of a 16 bit digitizer system for the “signal”, but all 16 bits would be used to measure the Out of Band Energy (noise).

c. Invisible Clipping. Accelerometer ringing (10x to 1000x above signal level) is clipped internal to the electronics and the operator has no way of knowing that this problem has occurred. This issue is caused by transducer resonance and/or transducer resonance riding on top of the actual desired signal. The resonance is typically caused by the use of undamped accelerometers with high Q factors. The input resonance exceeds the output of the amplifier causing the signal to be distorted (see Figure C-4).



Shock Input - Haversine

Distorted Result

Resonance (noise) combined w/signal

Figure C-4. Distortion example.

(1) If the operator was not aware of the large resonance issue the distorted result could very well be mistakenly reported as the result instead of the correct Haversine result that should have been reported.

(2) Asymmetric Clipping is also a problem and will cause unexpected distortion in the output results. Figure C-5 is an example of asymmetric clipping.

APPENDIX C. TOP SIX CONCERNS FOR NEW DATA ACQUISTION SYSTEM INSTRUMENTATION.

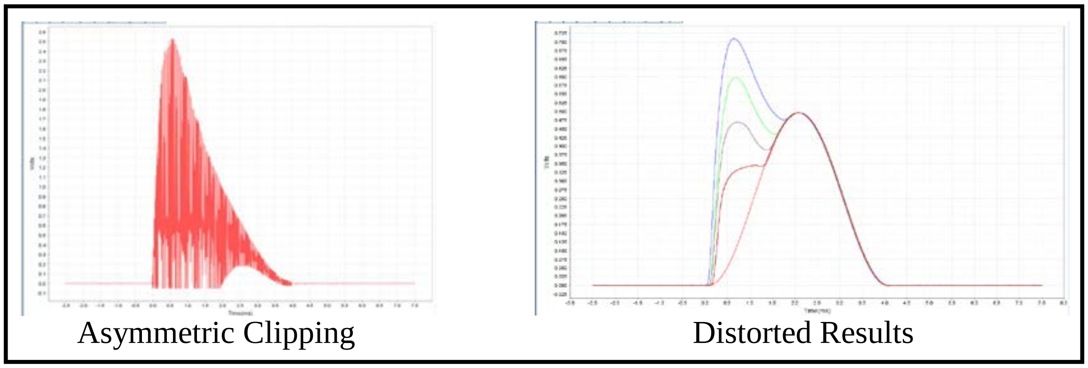


Figure C-5. Asymmetric clipping example.

(3) The Kyowa figure (Figure C-6) is a good example of invisible clipping. Typically the internal amplifier clips the signal off at either the positive, negative rail, or it clips both the positive and negative rail at the output of the amplifier as seen in the diagram below. The result of the clipping distorts the results.

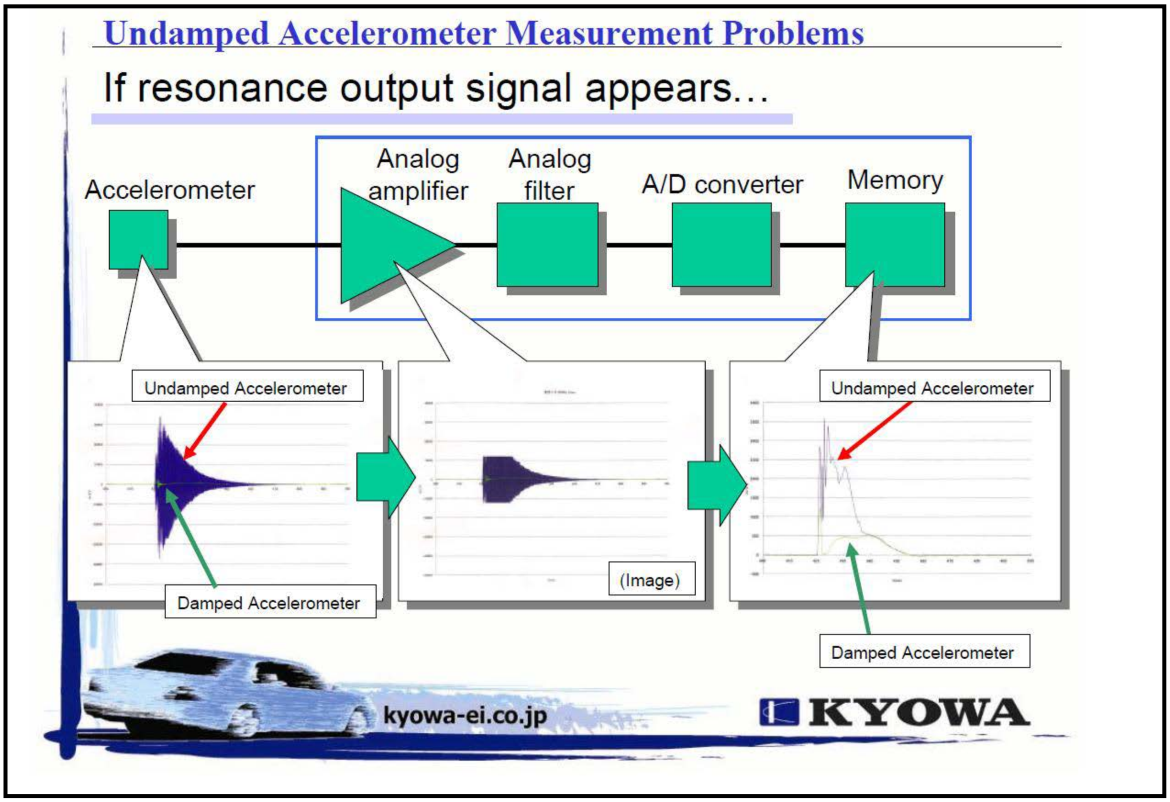


Figure C-6. Kyowa figure.

APPENDIX C. TOP SIX CONCERNS FOR NEW DATA ACQUISTION SYSTEM INSTRUMENTATION.

C.2 OVERSAMPLING RATIO.

a. It turns out that the "oversampling ratio" is a very important factor in evaluating any data acquisition system for ATD use. Errors can range from 1.2 to 69 percent!

b. Using the typical 10:1 oversampling ratio, with a sine wave at the cutoff frequency, we would have 10 points per cycle which equals one point every 36 degrees. The best case scenario is that you sample exactly when the peak amplitude occurs. The worst case is when the peak occurs mid-way between two samples or in this case 18 degrees before and after the peak. See Figure C-7 for additional information.

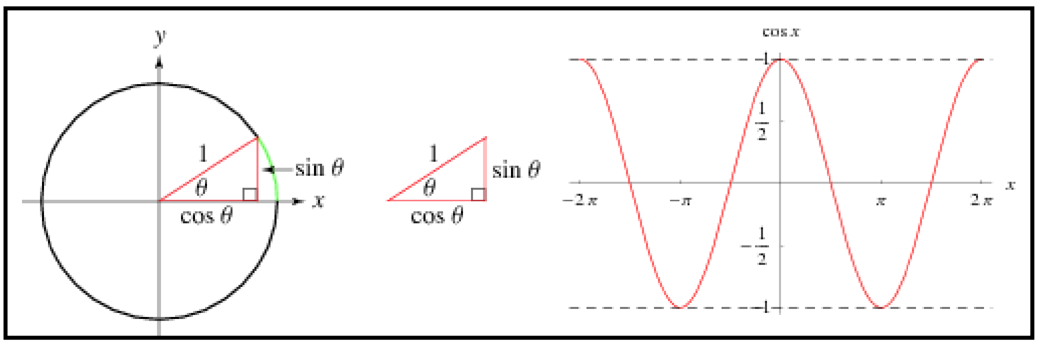


Figure C-7. Oversampling ratio.

c. The error associated with a sample 18 degrres off the peak equals 1- cos(18 degrees) = 0.048 or 4.8 percent which equates to -26 dB. That is a significant reduction in amplitude when the peak value is the most important measurement.

d. Note that compared to -96 dB cross talk, -80 dB common mode, and -50 dB "Total Attenuation of Noise Error Folded Back into the Pass Band", the -26 dB of peak measurement uncertainty due to 10:1 sampling is critical.

e. The worst case peak value measurement uncertainty for several common oversampling ratios are:

(1) 50:1 oversampling = -54 dB = 0.19 percent error (D4DG1).

(2) 40:1 oversampling = -50 dB = 0.3 percent error (D4DG2).

(3) 20:1 oversampling = -38 dB = 1.2 percent error.

APPENDIX C. TOP SIX CONCERNS FOR NEW DATA ACQUISTION SYSTEM INSTRUMENTATION.

(4) 10:1 oversampling = -26 dB = 4.8 percent error.

(5) 5:1 oversampling = -14 dB = 19 percent error.

(6) 4:1 oversampling = -10.7 dB = 29 percent error.

(7) 2.5:1 oversampling = -3.2 dB = 69 percent error.

C.3 SLEW RATE.

a. Slew rate is the rate at which the input amplifier can track the voltage signal. According to the document “A Proposed Validation Test Suite for Data Acquisition Systems used for Pyrotechnic Tests”[7], slew rate is critical if the measurement is contaminated with high frequency energy. The sine-sweep depicted in the graph of Figure C-8 shows slew rate issues starting at 383,877 Hz and beyond. This issue is out of band energy that must be identified to ensure it is not affecting the output results.

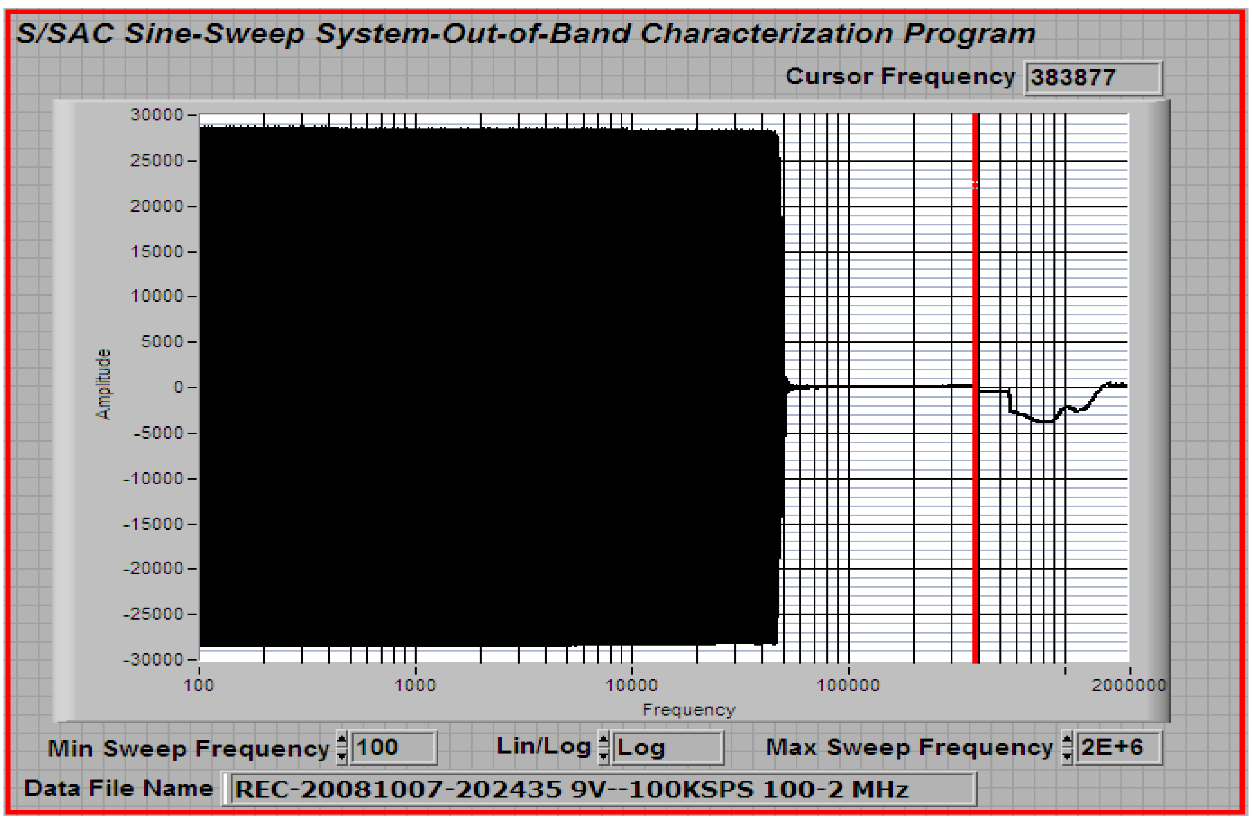


Figure C-8. Sine sweep plot example.

APPENDIX C. TOP SIX CONCERNS FOR NEW DATA ACQUISTION SYSTEM INSTRUMENTATION.

b. The slew rate problem shows up at 383,877 Hz (red cursor). To calculate the slew rate at that frequency use Equation C-2:

SR = 2 * π * Vpeak * problem frequency / 1,000,000 = V/us *(Equation C-2)*

example: 2 * π * 9 V * 383,877 Hz / 1,000,000 = 21.7 V/us

c. There is no fix for a low slew rate. It is a hardware limitation that the operator must be aware of prior to the test.

C.4 FILTER TYPE.

The two most common filters used in data acquisition are the Butterworth and Bessel type filters. A Butterworth is best suited for the frequency domain measurements and the Bessel is best suited for time domain measurements when voltage peaks are critical. When injecting a step pulse into a Butterworth filter the output will overshoot by 7.5 percent, and injecting that same pulse into a Bessel filter the overshoot is only 0.6 percent. The 7.5 percent overshoot is trivial for frequency domain analysis (FFT), but is very significant for time domain analysis (peak load, etc.). An example of overshoot from a Butterworth filter using a step input is shown in Figure C-8.

APPENDIX C. TOP SIX CONCERNS FOR NEW DATA ACQUISTION SYSTEM INSTRUMENTATION.

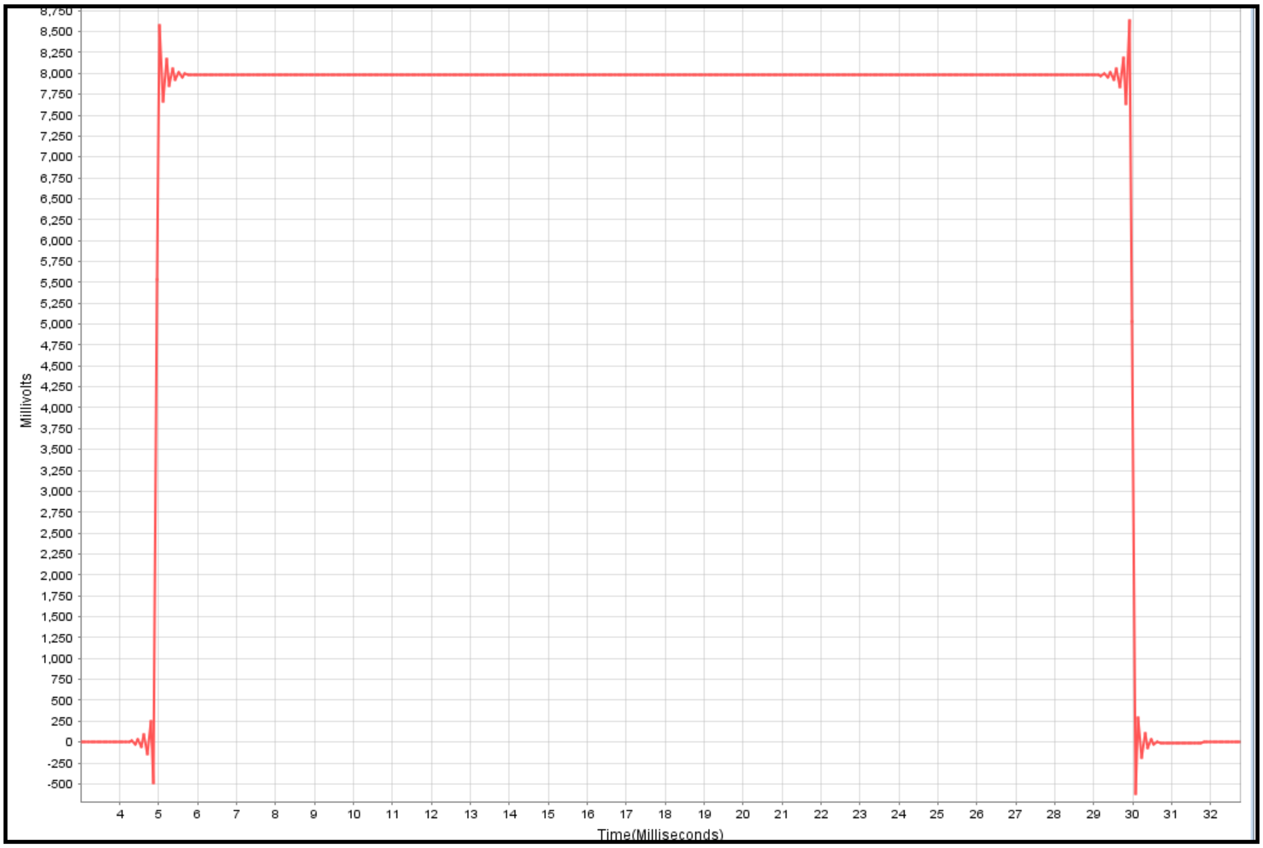


Figure C-9. Example of overshoot from a Butterworth filter using a step input.

C.5 DYNAMIC RANGE.

a. The dynamic range of a DAS device is the ratio of the highest signal level to the smallest signal level a circuit can handle (usually equal to the noise level), normally expressed in dB (Equation C-3):

Dynamic Range (dB) = 20 x log10(Maximum Voltage / Minimum Voltage) *(Equation C-3)*

b. To determine the dynamic range, you must know both the maximum voltage and the noise floor of the device. For example the D4DG1 has an input range of 5 V that converts to 3.53 Vrms: (Input Range 5 V / sqrt(2) = 3.53 Vrms). The noise floor for the D4DG1 at a gain of 1 is 26.4 uVrms so the Dynamic range (dB) = 20 x log10 (3.53 Vrms / 26.4 uVrms) = 102.52 dB.

APPENDIX C. TOP SIX CONCERNS FOR NEW DATA ACQUISTION SYSTEM INSTRUMENTATION.

c. The document "A Proposed Validation Test Suite for Data Acquisition Systems used for Pyrotechnic Tests" indicates for 1 percent accuracy a minimum dynamic range of a 1,000/1 or 60 dB is required and 10,000/1 or 80 dB is desired.

C.6 EFFECTIVE NUMBER OF BITS (ENOB).

ENOB is used to characterize the time-domain accuracy of a digital measurement system. An ENOB test determines the individual point accuracy (worst case) and the RMS accuracy (average error), and will indicate when problems exist but will not pin-point specific instrumentation problems.

APPENDIX D. FILTER GROUP DELAY.

D.1 WHAT IS GROUP DELAY?

The basic idea of group delay is reasonably simple; the negative derivative of phase with respect to frequency. But for most people, this doesn't mean much, which is unfortunate, because group delay is an important way to describe a filter's pass band characteristics. Our purpose here is to show why it is important.

D.2 WHY THE NAME "GROUP DELAY"?

a. We all understand ordinary time delay (phase shift), but what is group delay. Consider a simple example of a square wave, which as you know, is composed of a large group of frequency components. A square wave is square only because its frequency components are in proper phase alignment with one another. If we pass a square wave through a device and expect it to remain square, then we need to ensure that the device doesn't misalign these frequency components. A Group Delay measurement shows us how much a device causes these frequency components to become misaligned.

b. This may sound like a trivial matter, but as we show below, misaligning the phase between a group of frequency components can destroy a signal. In short, we want all frequency components to experience the same amount of delay (in seconds, not phase angle) as they pass through a device.

D.3 WHY DOES A FILTER GENERATE A PHASE SHIFT?

a. Let's start by answering this frequently asked question. To start with, a better question would be, is it possible to construct a device that doesn't generate a phase shift, and the answer is no.

b. Lets consider the simplest device possible, a piece of wire of length L where the signal can travel at the speed of light. Clearly, it takes L/c seconds for the signal to get through this device. The simple fact that time is required for a signal to pass from a device's input to its output means that it generates a phase shift.

c. As compared to other electrical devices however, filters have significant amounts of phase shift, and the longer the filter (i.e., the more poles it has, or the more taps it has) the more delay it has. In the case of digital filters, this delay is usually discussed in terms of samples, not seconds.

APPENDIX D. FILTER GROUP DELAY.

D.4 GROUP DELAY DESCRIBES PHASE SHIFT.

a. Let's start by making it clear that group delay is a measurement of time, so let's compare group delay to ordinary time delay (phase shift).

b. Here we compare the time delay to the group delay of a low pass filter. It turns out that the time delay and the group delay of a filter take on similar values in the pass band where the filter's phase response is linear. For an FIR filter with constant group delay, the time delay and the group delay are equal at all frequencies. For a filter with non-linear phase however, such as the Butterworth filter shown as Figure D-1), the delay is close to the group delay in the pass band.

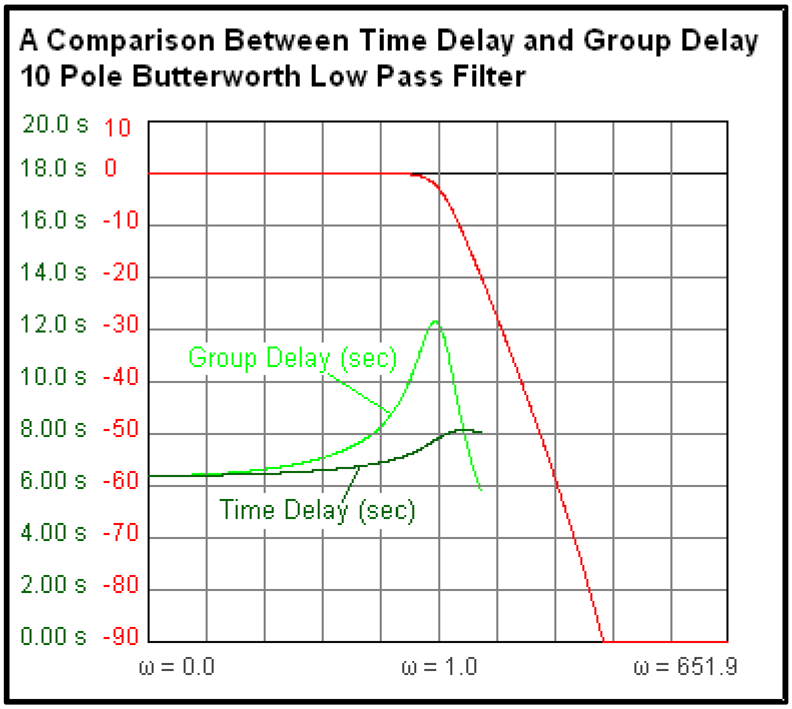


Figure D-1. Butterworth filter with non linear phase.

c. The plot in Figure D-1 makes it obvious that we cannot in general equate time delay and group delay, but this comparison helps to simplify the topic a bit (i.e., Group Delay is a measurement of time, and is similar in value to ordinary time delay in the filter's pass band where the phase is most linear). Figure D-2 shows an example using the more phase linear Gauss filter.

APPENDIX D. FILTER GROUP DELAY.

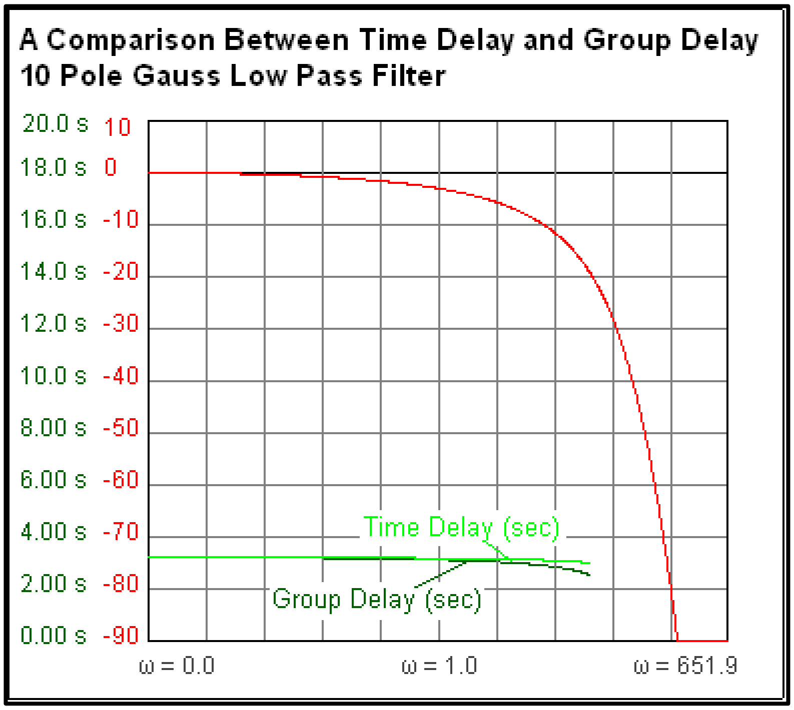


Figure D-2. Phase linear Gauss filter.

d. In loose terms, Group Delay is the amount of time required for a signal to propagate through a device.

e. More importantly however, the group delay curve indicates how much a device will distort a signal. A device with constant group delay (linear phase) equates to minimal distortion, but as we will show with examples below, non linear phase is a contributor to distortion, not the sole reason for it.

D.5 GROUP DELAY VS. SIGNAL PROPAGATION TIME.

a. We said that in loose terms, the group delay is a measurement of the time needed for a signal to propagate through a device. To demonstrate this, we send a square pulse through a low pass filter. This particular filter has a group delay of 40, and as can be seen in Figure D-3, the midpoint of the pulse's leading edge occurs at the output at t=40.

APPENDIX D. FILTER GROUP DELAY.

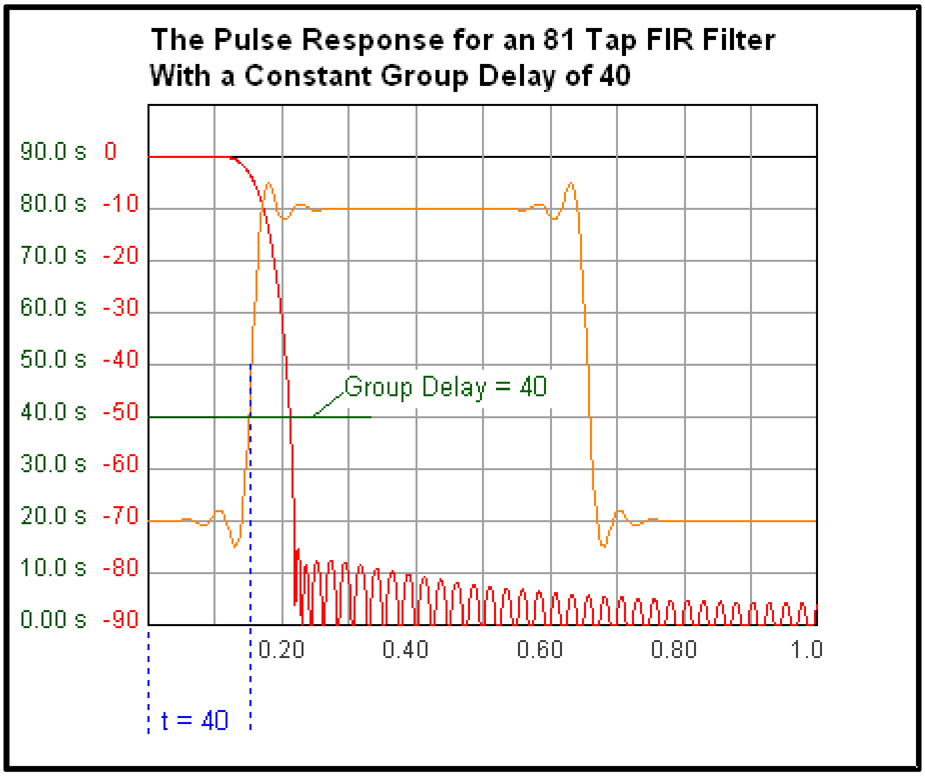


Figure D-3. Example square pulse through a low pass filter plot.

Note: For those not familiar with digital filters, t=40 means 40 sample times. If the filter's clock is running at 1 MHz, t=40 means 40 µs. This signal propagation behavior is the same for analog filters.

b. We used a low pass filter and a square pulse in this example because the effect of group delay is so readily seen, but keep in mind that a sine wave would have the same 40 sample delay. Since this filter has the same group delay at all frequencies, a sine wave at any frequency experiences the same delay time.

D.6 <u>WHY IS THE STEP RESPONSE IMPORTANT</u>?

Please remember that all signals passing through a device will experience the same distortion, but we use a step response to measure distortion for two reasons. First, a step input contains all frequencies, so using it is a bit like doing a frequency sweep, but in the time domain. Second, since you know the exact shape of the input signal, any variations to that shape make the distortion readily apparent. Distortion would be much harder to detect if we used an audio signal, for example.

APPENDIX D. FILTER GROUP DELAY.

D.7 <u>WHY IS GROUP DELAY IMPORTANT</u>?

a. In most cases, we are not particularly concerned with a filter's delay (i.e., the amount of time it takes for a signal to propagate through the filter). We are concerned however, that each of the signal's frequency components experience the same delay so that their phase relative to one another is maintained. Or said a bit differently, we want our signals to maintain their shape as they pass through a device.

b. In principle, the filter shown above has perfect group delay, but the pulse was still distorted by the filter. The filter slowed the pulse's rise time and gave it overshoot. So there is more to be concerned with than just group delay. As you know, the square wave entering the filter had an infinite number of frequency components, and the filter did its job by attenuating the higher frequencies. So, in this respect, there is no way for a low pass filter to not affect a square wave, so we must expect some distortion.

c. Figure D-4 compares the distortion caused by two filters. Both of these FIR filters have the same ideal group delay, but they attenuate the high frequencies differently. This difference has a clear effect on the distortion of the pulse.

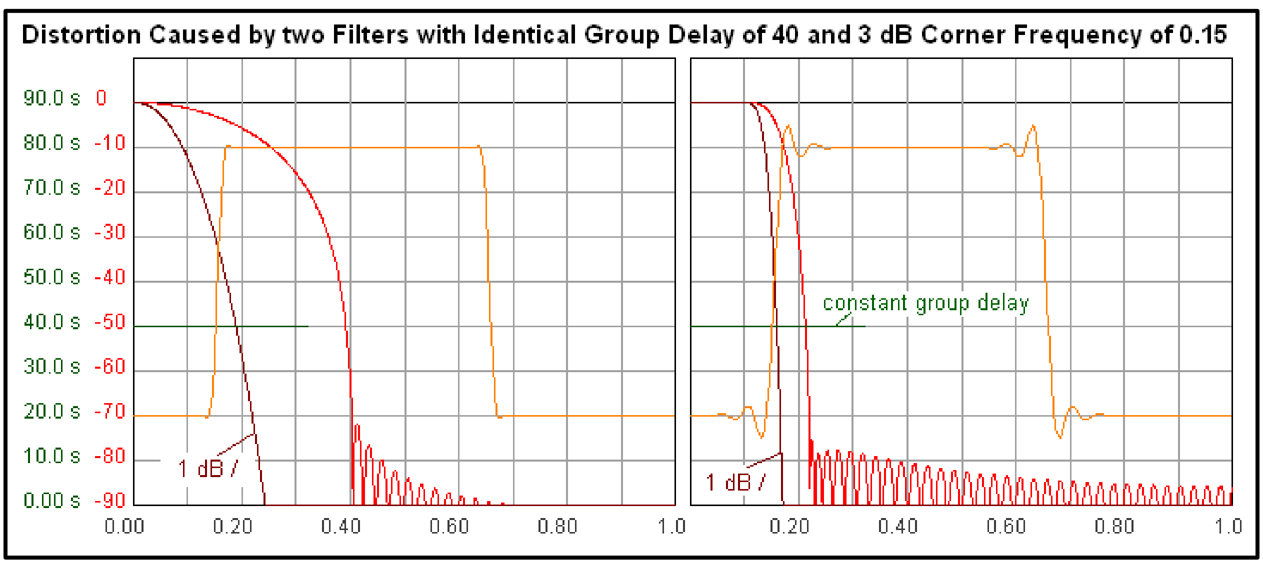


Figure D-4. Example plots of distortion caused by two filters.

APPENDIX D. FILTER GROUP DELAY.

d. Figure D-5 shows the converse of Figure D-4 where two filters have the same magnitude response, but have different group delay responses. The effect of nonlinear phase is clear. The step response for the filter with nonlinear phase has significantly more overshoot and ringing than the filter with constant group delay. Also note the time delay differences, which of course, coincides with the different group delay values.

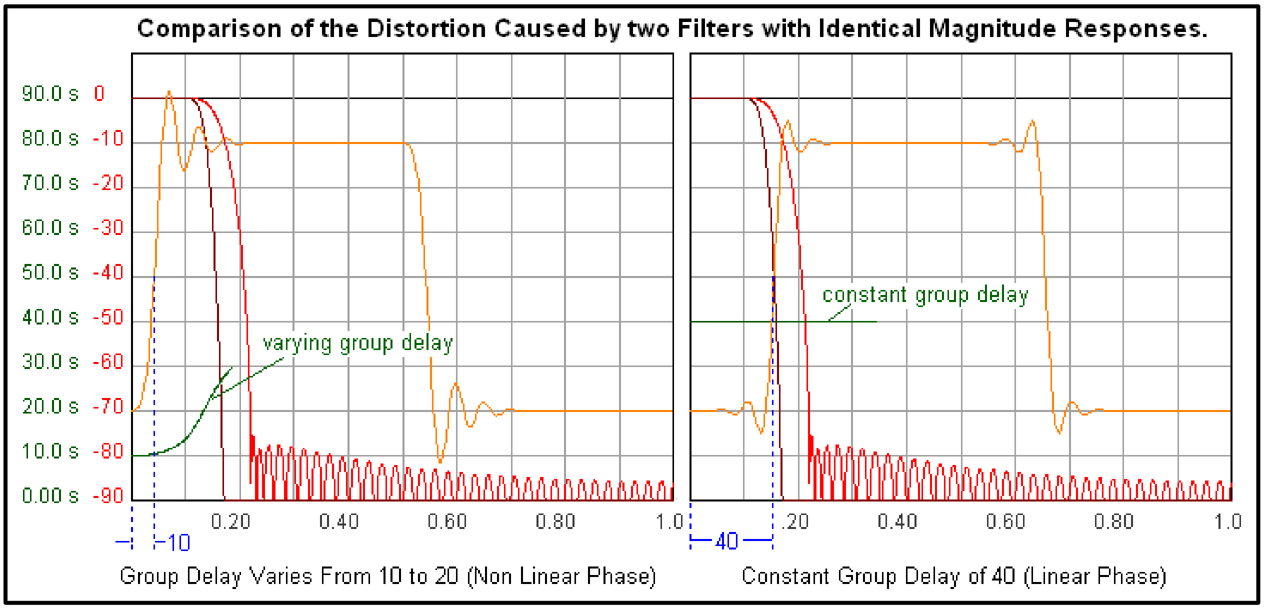


Figure D-5. Distortion caused by two filters with identical magnitude responses.

D.8 AN EXTREME EXAMPLE OF GROUP DELAY DISTORTION.

a. You are probably familiar with the term "all pass filter", and you have probably wondered why a device that passes all frequencies is called a filter.

b. The pass band of an all pass filter is defined by its group delay response, not its magnitude response. The key to using an all pass filter is to make sure that the frequency content of the signal is within the filter's pass band. In this example in Figure D-6, the square wave is virtually destroyed by the filter because it has significant frequency content well beyond the filter's pass band (where its group delay is flat).

APPENDIX D. FILTER GROUP DELAY.

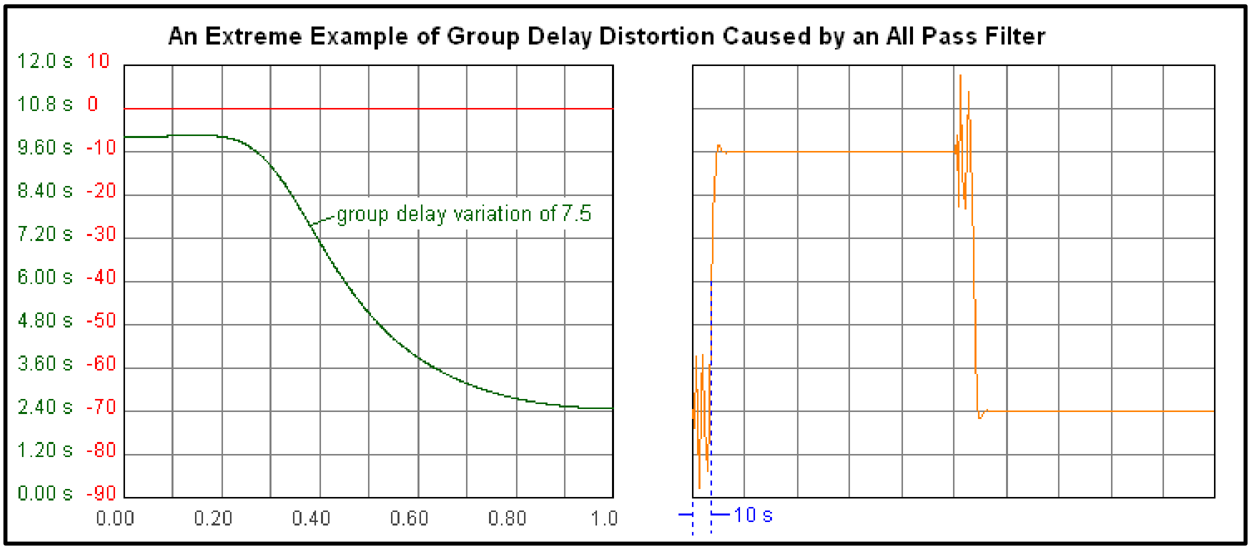


Figure D-6. Example of group delay distortion caused by an all pass filter.

Note: All pass filters are used to delay a signal in order to align it with another signal. This IIR example would delay the signal by 10 samples. If we had used an FIR all pass, which would have constant group delay at all frequencies, there would be no distortion.

D.9 GROUP DELAY AS A MEASURE OF PHASE.

a. Now let's show group delay as it is defined, the negative derivative of the phase.

b. It should be clear that as the tap count is increased for an FIR filter, the group delay increases as well, simply because the filter is getting longer. Similarly, as the pole count is increased for IIR and analog filters, the group delay increases, again, because the filter is getting longer.

c. Or said a bit differently, as the filter gets longer, the slope of the phase curve gets steeper. In Figure D-7 we compare the slope of the phase for two FIR filters with different group delays. The first has 10 taps and the other 14 taps. The 14 tap filter is longer so its phase has more negative slope (more group delay).

APPENDIX D. FILTER GROUP DELAY.

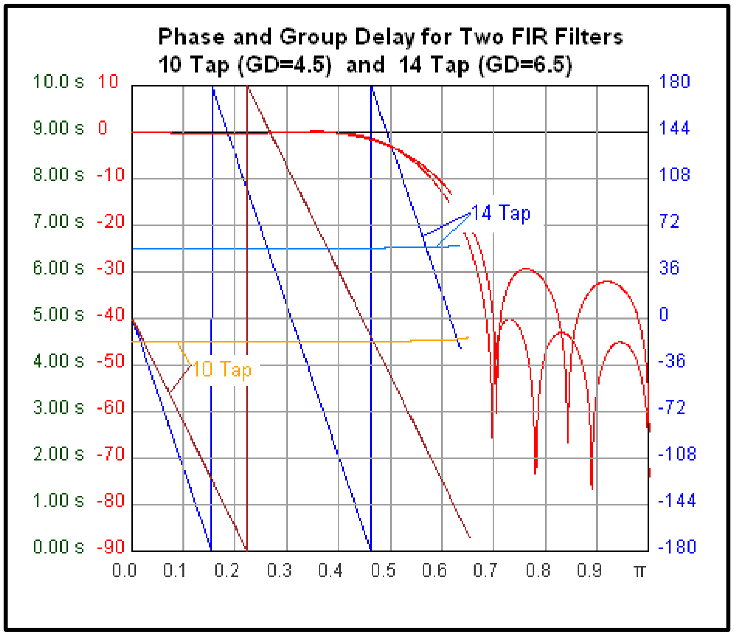


Figure D-7. Example phase slope for two FIR filters with different group delays.

D.10 NEGATIVE GROUP DELAY.

a. We want to make it clear that, in general, the group delay for a physical device (as opposed to a pure mathematical construct) cannot be negative. If it were, the signal would appear at the device's output before it entered the device.

b. It is possible however, to construct an active circuit (not a passive circuit) with negative group delay. One simply needs to a place a pole in the right hand plane, which of course makes the circuit unstable. The circuit will want to oscillate at the pole frequency, which is fine if you are designing an oscillator, but not very useful otherwise.

c. While not negative, the ideal Hilbert Transform has no group delay, because its phase is a constant ± 90 degrees (making the derivative zero), but it cannot be implemented in hardware. Only in mathematics can we construct a filter with constant phase. The phase of a filter implemented in hardware must vary with frequency. Therefore, if we want to implement a Hilbert Transform in hardware, we must give it some delay.

d. Our purpose here was to try to give some meaning to the term Group Delay. The more signal processing experience you get, the more attention you will pay to group delay curves. It is not a complicated subject, but it does take a bit of experience to understand its significance.

APPENDIX E. ABBREVIATIONS.

AC	Alternating Current
A/D	analog/digital
ADC	analog-to-digital converter
ATC	U.S. Army Aberdeen Test Center
ATD	anthropomorphic test dummy
ATEC	U.S. Army Test and Evaluation Command
BW	bandwidth
°C	degrees Celsius
CMRR	common mode rejection ratio
DAS	Data Acquisition System
dB	decibel
DC	Direct Current
DMM	digital multi-meter
DTC	discharge time constant
DVM	digital voltmeter
EMC	electromagnetic compatibility
EMI	electromagnetic interference
ENOB	Effective Number of Bits
ESD	electrostatic discharge
°F	degrees Fahrenheit
f	frequency
fc	corner frequency
FFT	Fast Fourier Transform
FS	full-scale
GPS	Global Positioning System
Hz	Hertz
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IEPE	Integrated Electronic PiezoElectric
IOP	Internal Operating Procedure
kHz	kilohertz
kS/s	kilo Samples per second
kV	kilovolt

APPENDIX E. ABBREVIATIONS.

LCR	Inductance, Capacitance, Resistance
mA	milliamp
MIL-STD	Military Standard
mV	millivolt
NAD	noise and distortion
NIST	National Institute of Standards and Technology
ns	nanosecond
pC	picocoulombs
PCB	printed circuit board
pf	picofarads
PSG	precision signal generator
psi	pounds per square inch
PTP	Precision Time Protocol
RF	radio frequency
rms	root mean square
SFDR	spurious-free dynamic range
SINAD	signal to noise and distortion
SNR	signal to noise ratio
SR	sample rate
TC	time constant
TOP	Test Operations Procedure
V/µs	Volts per microsecond
v	voltage
V	Volts
Vp	peak
Vpp	peak-to-peak

.

APPENDIX F. REFERENCES.

1. IEEE 1057, IEEE Standard for Digitizing Waveform Recorders, 2007.

2. ATEC Reg 73-1, System Test and Evaluation Policy, 13 May 2019.

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7. "A Proposed Validation Test Suite for Data Acquisition Systems used for Pyrotechnic Tests", Strether Smith, October 2009.

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APPENDIX G. APPROVAL AUTHORITY.

CSTE-CI 8 December 2020

MEMORANDUM FOR

Commander, U.S. Army Operational Test Command
Director, U.S. Army Evaluation Center
Commanders, ATEC Test Centers
Technical Directors, ATEC Test Centers

SUBJECT: Test Operations Procedure 02-2-632, Data Acquisition System (DAS) Test Procedures, Approved for Publication

1. Test Operations Procedure (TOP) 02-2-632, Data Acquisition System (DAS) Test Procedures, has been reviewed by the U.S. Army Test and Evaluation Command (ATEC) Test Centers, the U.S. Army Operational Test Command, and the U.S. Army Evaluation Center. All comments received during the formal coordination period have been adjudicated by the preparing agency.

2. Scope of the document. This TOP defines specifications and describes test methods used for measuring the performance of electronic waveform digitizing systems. The TOP is directed toward, but not restricted to, general-purpose waveform recorders and analyzers.

3. This document is approved for publication and has been posted to the Reference Library of the ATEC Vision Digital Library System (VDLS). The VDLS website can be accessed at https://vdls.atc.army.mil/.

4. Comments, suggestions, or questions on this document should be addressed to U.S. Army Test and Evaluation Command (CSTE-CI), 6617 Aberdeen Boulevard-Third Floor, Aberdeen Proving Ground, MD 21005-5001; or e-mailed to usarmy.apg.atec.mbx.atec-standards@mail.mil.

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Forward comments, recommended changes, or any pertinent data which may be of use in improving this publication to the following address: Policy and Standardization Division (CSTE-CI-P), U.S. Army Test and Evaluation Command, 6617 Aberdeen Boulevard, Aberdeen Proving Ground, Maryland 21005-5001. Technical information may be obtained from the preparing activity: Ballistics Instrumentation Division, Survivability Lethality Directorate, U.S. Army Aberdeen Test Center, Aberdeen Proving Ground, MD 21005-5059. Additional copies can be requested through the following website: https://www.atec.army.mil/publications/documents.html, or through the Defense Technical Information Center, 8725 John J. Kingman Rd., STE 0944, Fort Belvoir, VA 22060-6218. This document is identified by the accession number (AD No.) printed on the first page.