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# **Fabrication, Characterization, and Modeling of Monolayer Molybdenum Disulfide Radio Frequency Transistors**

**by Alexander L Mazzoni, Matthew L Chin, Pankaj B Shah, Khamsouk Kingkeo, Madan Dubey, and Robert A Burke**

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# **Fabrication, Characterization, and Modeling of Monolayer Molybdenum Disulfide Radio Frequency Transistors**

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| 14. ABSTRACT<br>Radio frequency (RF) transistors using US Army Combat Capabilities Development Command Army Research Laboratory–grown monolayer molybdenum disulfide (MoS <sub>2</sub> ) were fabricated and tested in the ground-signal-ground configuration. Devices were fabricated and characterized on both hard (silicon dioxide) and flexible (polyimide) substrates. Devices operated with de-embedded $f_T$ and $f_{max}$ over 3 GHz on rigid substrates and 1 GHz on flexible substrates. Standard metal–oxide–semiconductor field-effect transistor current-voltage equations are applied to experimental results of a DEVCOM Army Research Laboratory–fabricated RF transistors that use monolayer MoS <sub>2</sub> as the channel material. A method to accurately extract the key device parameters of threshold voltage, contact resistance, and transconductance is introduced and discussed. The experimental transistor curves deviate from the transistor models in regions of operation with both a high gate and drain bias. According to related literature, significant device self-heating occurs at these operation regimes causing significant velocity saturation/mobility degradation. |                             |                                    |                                      |                                                             |                                                             |
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## Contents

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|                                                                |           |
|----------------------------------------------------------------|-----------|
| <b>List of Figures</b>                                         | <b>v</b>  |
| <b>List of Tables</b>                                          | <b>vi</b> |
| <b>1. Introduction</b>                                         | <b>1</b>  |
| <b>2. Methods</b>                                              | <b>2</b>  |
| 2.1 MoS <sub>2</sub> Growth Process                            | 2         |
| 2.2 Device Substrates                                          | 3         |
| 2.3 MoS <sub>2</sub> Transfer Process                          | 4         |
| 2.4 MoS <sub>2</sub> RF FET Fabrication Process                | 5         |
| 2.4.1 MoS <sub>2</sub> Channel Etch                            | 7         |
| 2.4.2 Source and Drain Contact Metallization                   | 10        |
| 2.4.3 Top-Gate Dielectric Deposition                           | 12        |
| 2.4.4 Top-Gate Metallization                                   | 12        |
| 2.4.5 Polyimide-Specific Fabrication Techniques                | 13        |
| 2.5 DC Electrical Characterization                             | 14        |
| 2.5.1 Back-Gated Measurements                                  | 15        |
| 2.5.2 Top-Gated Measurements                                   | 15        |
| 2.6 RF Electrical Characterization                             | 15        |
| <b>3. Results</b>                                              | <b>16</b> |
| 3.1 DC Electrical Data                                         | 16        |
| 3.1.1 Back-Gated Testing                                       | 16        |
| 3.1.2 Top-Gated Testing                                        | 18        |
| 3.2 RF Electrical Data                                         | 20        |
| 3.2.1 RF Performance on Rigid (SiO <sub>2</sub> ) Substrate    | 21        |
| 3.2.2 RF Performance on Flexible (Polyimide) Substrate         | 22        |
| 3.2.3 Comparison to Monolayer RF FET Performance in Literature | 23        |
| 3.2.4 RF Performance Comparison to Theoretical Limits          | 24        |
| 3.3 Device I-V Modeling                                        | 24        |

|           |                                                         |           |
|-----------|---------------------------------------------------------|-----------|
| 3.3.1     | Simple FET Model with Contact Resistance                | 24        |
| 3.3.2     | FET Model Parameter Extraction                          | 26        |
| 3.3.3     | Parameter Validation and Low-Field Mobility Calculation | 28        |
| 3.3.4     | FET Model Inaccuracies at High Gate and Drain Fields    | 32        |
| <b>4.</b> | <b>Conclusions</b>                                      | <b>37</b> |
| <b>5.</b> | <b>References</b>                                       | <b>38</b> |
|           | <b>List of Symbols, Abbreviations, and Acronyms</b>     | <b>41</b> |
|           | <b>Distribution List</b>                                | <b>43</b> |

## List of Figures

|         |                                                                                                                                                                                                                                                                             |    |
|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| Fig. 1  | Diagram of the MoS <sub>2</sub> growth setup. The MoO <sub>3</sub> powder and the substrates were loaded in the same alumina boat. The samples were placed face down on top of the alumina boat and the MoO <sub>3</sub> powder was spread along the base of the boat. .... | 3  |
| Fig. 2  | Cross-section of the device substrate prior to MoS <sub>2</sub> transfer. The highly doped Si wafer acted as a back-gate contact for the 300-nm SiO <sub>2</sub> dielectric, but the polyimide film is too thick to be operated in a back-gated configuration. ....         | 4  |
| Fig. 3  | Cross-section of the device stack after MoS <sub>2</sub> transfer .....                                                                                                                                                                                                     | 5  |
| Fig. 4  | Optical image of a completed device (left) and corresponding cross-section (right); red line on optical image indicating location of cross-section .....                                                                                                                    | 6  |
| Fig. 5  | CAD drawing of the RF transistor fabricated with important dimensions labeled. The colors correspond to the different layers: green = MoS <sub>2</sub> channel, magenta = drain and source metal contact layer, and cyan = top-gate metal layer. ....                       | 7  |
| Fig. 6  | Optical image of a device after EBL exposure and development to form the MoS <sub>2</sub> channel, but before MoS <sub>2</sub> etching .....                                                                                                                                | 8  |
| Fig. 7  | Channel area after the channel-defining RIE, but before PMMA removal in acetone .....                                                                                                                                                                                       | 9  |
| Fig. 8  | Channel area after RIE and PMMA removal in acetone .....                                                                                                                                                                                                                    | 10 |
| Fig. 9  | Device after metal contact EBL, prior to metal evaporation for the source/drain contacts.....                                                                                                                                                                               | 11 |
| Fig. 10 | Device after source/drain metal contact deposition and liftoff.....                                                                                                                                                                                                         | 12 |
| Fig. 11 | Device after top-gate metal contact deposition and liftoff.....                                                                                                                                                                                                             | 13 |
| Fig. 12 | Completed RF FET on polyimide.....                                                                                                                                                                                                                                          | 14 |
| Fig. 13 | CAD for the short and open test structures fabricated for de-embedding.....                                                                                                                                                                                                 | 16 |
| Fig. 14 | Back-gated $I_{DS}$ vs. $V_{GS}$ example measurement, $V_{DS} = 100$ mV .....                                                                                                                                                                                               | 17 |
| Fig. 15 | Mobility extracted from the back-gated $I_{DS}$ vs. $V_{GS}$ example measurement .....                                                                                                                                                                                      | 18 |
| Fig. 16 | Top-gated $I_{DS}$ vs. $V_{GS}$ example measurement .....                                                                                                                                                                                                                   | 19 |
| Fig. 17 | Top-gated $I_{DS}$ vs. $V_{DS}$ example measurement .....                                                                                                                                                                                                                   | 20 |
| Fig. 18 | Rigid substrate: $f_T \sim 180$ MHz/3.3 GHz (extrinsic/intrinsic).....                                                                                                                                                                                                      | 21 |
| Fig. 19 | Rigid substrate: $f_{max} \sim 2.4$ GHz/3.5 GHz (extrinsic/intrinsic) .....                                                                                                                                                                                                 | 22 |
| Fig. 20 | Polyimide substrate: $f_T \sim 300$ MHz/1 GHz (extrinsic/intrinsic) .....                                                                                                                                                                                                   | 22 |
| Fig. 21 | Polyimide substrate: $f_{max} \sim 1.1$ GHz/1.1 GHz (extrinsic/intrinsic) .....                                                                                                                                                                                             | 23 |

|         |                                                                                                                                                                                                                                                                                                         |    |
|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| Fig. 22 | Simple transistor model including contact resistances .....                                                                                                                                                                                                                                             | 25 |
| Fig. 23 | $I_{DS}$ - $V_{DS}$ curve of an RF FET on the rigid substrate. Dashed green box indicates region used to fit FET parameters. ....                                                                                                                                                                       | 26 |
| Fig. 24 | Total resistance: experimental values compared to the model .....                                                                                                                                                                                                                                       | 27 |
| Fig. 25 | Extrapolation of the total resistance to higher gate voltages, showing the limit of twice the contact resistance as the dashed horizontal line and threshold voltage as the vertical line .....                                                                                                         | 28 |
| Fig. 26 | RF FET $I_{DS}$ - $V_{GS}$ curve (notice the extracted threshold voltage of $-10.45$ from the $I_{DS}$ - $V_{DS}$ curves qualitatively makes sense).....                                                                                                                                                | 29 |
| Fig. 27 | After extracting the contact resistance, we can determine how much of the applied voltage $V_{DD}$ is dropped across the channel vs. the contact resistance. At low gate voltages most of the voltage drops across the channel, but at high gate voltages most drops across the contact resistance..... | 30 |
| Fig. 28 | Field-effect mobility extracted from the RF FET $I_{DS}$ - $V_{GS}$ curve as measured (not considering contact resistance) .....                                                                                                                                                                        | 31 |
| Fig. 29 | Field-effect mobility extracted from the RF FET $I_{DS}$ - $V_{GS}$ curve after incorporating the voltage dropped across the contact resistance .....                                                                                                                                                   | 32 |
| Fig. 30 | $I_{DS}$ - $V_{DS}$ curves plotted using extracted values X2 and X3 .....                                                                                                                                                                                                                               | 33 |
| Fig. 31 | Calculated voltage drops due to contact resistance, X1. The specific contact resistance of this device was $2.56 \text{ k}\Omega\cdot\mu\text{m}$ . ....                                                                                                                                                | 34 |
| Fig. 32 | $I_{DS}$ - $V_{DD}$ curves plotted using extracted values X1, X2, and X3.....                                                                                                                                                                                                                           | 35 |
| Fig. 33 | Experimental results vs. computed $I_{DS}$ - $V_{DD}$ curves plotted using extracted values X1, X2, and X3 .....                                                                                                                                                                                        | 36 |
| Fig. 34 | Experimental results vs. computed $I_{DS}$ - $V_{DD}$ curves plotted using extracted values X1, X2, and X3. Subthreshold current modeling was ignored for simplicity; this explains the low current computed for $V_{GS} < -10 \text{ V}$ . ....                                                        | 37 |

## List of Tables

|         |                                                  |    |
|---------|--------------------------------------------------|----|
| Table 1 | Summary of intrinsic RF device performance ..... | 23 |
|---------|--------------------------------------------------|----|

## 1. Introduction

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In 2004, researchers established the ability to create a 2-D sheet of material only a single-atom thick with the demonstration of graphene, a monolayer of carbon atoms exfoliated from the bulk and layered material graphite.<sup>1</sup> This method to produce 2-D monolayers was then quickly applied to other common layered materials,<sup>2</sup> including molybdenum disulfide ( $\text{MoS}_2$ ). Although back-gated field-effect transistors (FETs) using monolayer  $\text{MoS}_2$  as the semiconducting channel were demonstrated in 2005, the carrier mobility measured many orders of magnitude lower than the mobility in graphene, and research into the electronic properties of 2-D materials focused mainly on graphene. A few factors renewed interest in the electronic properties of  $\text{MoS}_2$  in the early 2010s such as the limitations realized in graphene electronics from its lack of a bandgap, the observation of an indirect-to-direct bandgap transition when  $\text{MoS}_2$  is thinned to a monolayer,<sup>3,4</sup> the demonstration of improved monolayer  $\text{MoS}_2$  transistor performance,<sup>5,6</sup> and the ability to grow large-area  $\text{MoS}_2$  via a chemical vapor deposition (CVD) method.<sup>7</sup>

The emphasis on research and development of  $\text{MoS}_2$  transistors occurred after that of graphene transistors, and that research is often referenced for guidance or comparison. In terms of transistors for RF applications, the high carrier mobility and velocity in graphene excited researchers for the potential of pushing the limits on transistor operating speed. Graphene FETs quickly demonstrated competitive performance with state-of-the-art III-V and silicon (Si) transistors in terms of cutoff frequency,  $f_T$ . However, the lack of a bandgap in graphene prevents the normal transistor saturation needed to have a high output resistance and graphene transistors could not compete in terms of power gain or the maximum frequency of operation metric,  $f_{max}$ .<sup>8</sup>

In a similar manner, although  $\text{MoS}_2$  has a bandgap and shows clear saturating behavior, its carrier mobility is lower and could not compete in either RF performance metric.<sup>9</sup>

Due to the inability of 2-D materials to immediately compete with state-of-the-art devices in traditional digital or RF applications, researchers started looking for niche applications that take advantage of 2-D materials' thinness and the unique deposition methods like inkjet printing or fabrication processes like the polymer-assisted transfer method. Around 2015, one such application space popularly explored was using 2-D materials such as  $\text{MoS}_2$  as candidates for flexible RF electronics due to their high elastic strain limit<sup>10</sup> and ability to transfer to arbitrary surfaces. In this area of flexible or transparent electronics, suggested at least as

early as 2006–2007 as a target area for MoS<sub>2</sub> electronics,<sup>11</sup> transistors made from 2-D materials are often compared in performance to organic semiconductors.

This report documents the work to achieve the following goals derived from the Biennial Program Plan<sup>12</sup> of:

- 1) Monolayer MoS<sub>2</sub> FETs operating in the GHz frequencies (2016)
- 2) Monolayer MoS<sub>2</sub> FETs operating above a GHz on flexible substrates (2017)

Efforts to fabricate transistors out of monolayer MoS<sub>2</sub> using an entirely in-house operation to grow the material, make the device, and test the device are detailed in this report. The performance of the device is then compared to standard transistor models, other monolayer MoS<sub>2</sub> RF FET performance published in literature,<sup>13,14</sup> and to the theoretical maximum performance of phonon-limited transport.<sup>15,16</sup>

## **2. Methods**

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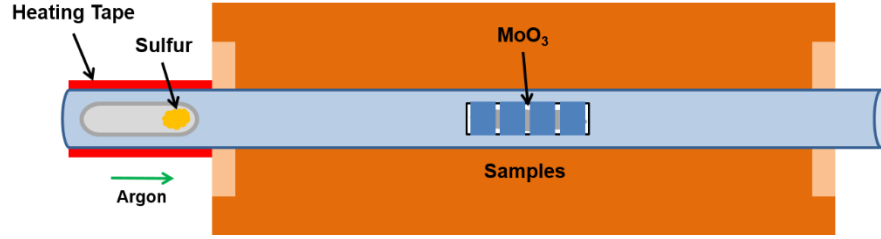
The following steps are covered in detail in this section:

- 1) MoS<sub>2</sub> growth process
- 2) Preparation of the device substrates (rigid and flexible)
- 3) Process used to physically transfer MoS<sub>2</sub> from the growth substrate to the device substrate
- 4) Fabrication of RF FETs after material transfer
- 5) DC testing of the MoS<sub>2</sub> FETs
- 6) RF testing of the MoS<sub>2</sub> FETs

### **2.1 MoS<sub>2</sub> Growth Process**

---

MoS<sub>2</sub> was grown on 15- × 16-mm thermal oxide (220 nm) chips in a tube furnace via powder vaporization using sulfur and molybdenum trioxide (MoO<sub>3</sub>) powder precursors. The growth was performed in a tube furnace with heating tape upstream of the hot zone (Fig. 1). Sulfur powder was located upstream, outside of the furnace heating zone to limit the sulfur vapor pressure, and was instead controlled by the heating tape. Alumina boats were used for holding the MoO<sub>3</sub> powder, sulfur powder, and the substrates for growth. Argon was used as a carrier gas for the growth process. The heating tape was set to 275 °C, while the furnace temperature was set to 650 °C. Before growth, 40 µL of perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt was spin-coated at 2000 rpm on the samples to improve seeding for the growth process.



**Fig. 1** Diagram of the MoS<sub>2</sub> growth setup. The MoO<sub>3</sub> powder and the substrates were loaded in the same alumina boat. The samples were placed face down on top of the alumina boat and the MoO<sub>3</sub> powder was spread along the base of the boat.

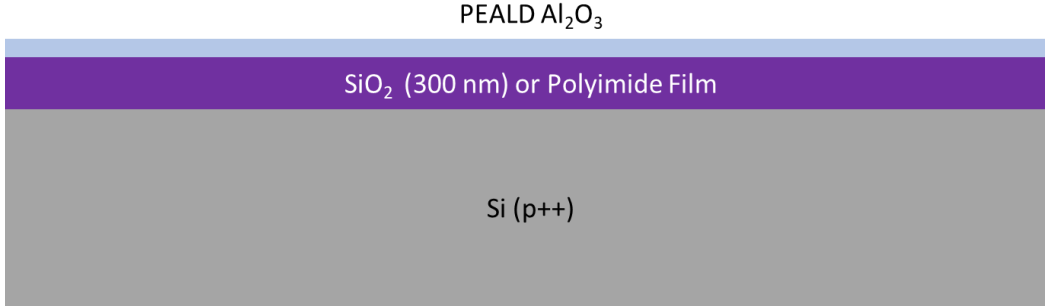
## 2.2 Device Substrates

The RF FETs were fabricated on top of two different substrates. The first was a standard thermal oxide chip (300 nm), the second was a layer of polyimide spun on a Si chip. In both cases, the MoS<sub>2</sub> layer was moved from the growth substrate (220-nm thermal oxide chip) to the device substrate via the transfer method described in Section 2.3.

A spin-on polyimide was chosen to enable standard fabrication on a rigid carrier wafer, with the ability to peel off the flexible device upon completion. The specific polymer chosen was HD Microsystems Polyimide PI 2611. This polyimide has an associated optional adhesion promoter, VM-651. The polyimide was spun onto a Si wafer at 2000 rpm for 60 s and then soft baked on a hot plate at 150 °C for 2 min. This was performed two times to create a thicker layer. To cure the polyimide, the wafer was loaded into a vacuum furnace (IVI Corp.) with controlled heat-ramping rates. The furnace ramped from room temperature to 250 °C over 1 h, stayed at temperature for 2 h, then took 1 h to cool down to room temperature. A slow ramping time for temperature heat-up and cool-down was critical to prevent any delamination. According to the data sheet, the polyimide thickness should be approximately 9 μm after curing.

A layer of aluminum oxide (Al<sub>2</sub>O<sub>3</sub>) was deposited on both substrates to serve as a common bottom interface of the MoS<sub>2</sub> transistor. First, a 1-nm Al seed layer was deposited via electron beam evaporation (CHA Industries) at a pressure of 10<sup>-6</sup> Torr. After the Al seed-layer deposition, the sample sat out in the ambient cleanroom environment to oxidize. A total of 250 cycles of plasma-enhanced atomic layer deposition (PEALD) Al<sub>2</sub>O<sub>3</sub> were then deposited (Kurt J. Lesker Company) at 200 °C using oxygen (O<sub>2</sub>) and trimethylaluminum (TMA) precursors. This PEALD coating was deposited on both substrates to provide a similar interface with the MoS<sub>2</sub> layer, enabling a more direct comparison between the rigid (silicon dioxide [SiO<sub>2</sub>]) and flexible (polyimide) substrate devices.

A cross-section of the device substrates prior to MoS<sub>2</sub> transfer is provided in Fig. 2.



**Fig. 2** Cross-section of the device substrate prior to MoS<sub>2</sub> transfer. The highly doped Si wafer acted as a back-gate contact for the 300-nm SiO<sub>2</sub> dielectric, but the polyimide film is too thick to be operated in a back-gated configuration.

On top of this substrate stack, MoS<sub>2</sub> material was transferred (described in Section 2.3) and then underwent the RF FET fabrication process shown in Section 2.4.

### 2.3 MoS<sub>2</sub> Transfer Process

The transfer process used a polymethyl methacrylate (PMMA) spin-cast layer to protect the MoS<sub>2</sub> and potassium hydroxide (KOH) to separate the MoS<sub>2</sub> from the SiO<sub>2</sub> growth substrate. The specific details for the transfer process are as follows.

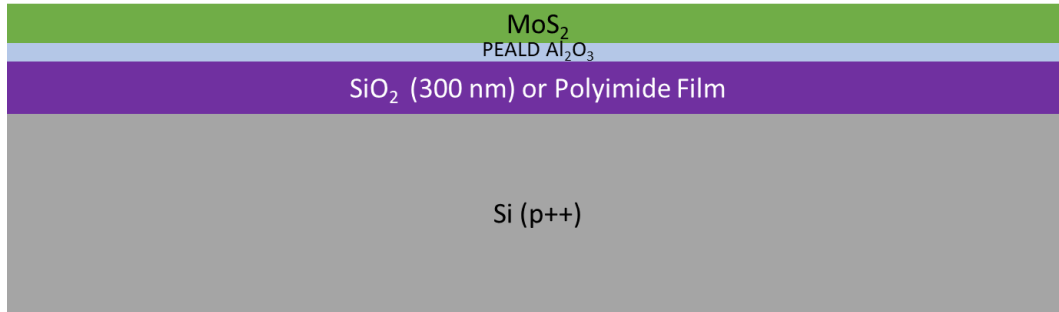
PMMA 950 A9 was spun onto the MoS<sub>2</sub>/SiO<sub>2</sub>/Si growth substrate stack at 2000 rpm for 60 s and then soft baked at 50 °C in air for 30 min. After air-drying in a fume hood for an additional 3 h at room temperature, the PMMA was scraped from the edges of the growth substrate with a razor blade.

A solution of 15% KOH by weight was prepared by dissolving KOH pellets in deionized (DI) water. The PMMA-coated MoS<sub>2</sub> substrate was floated on the KOH solution at room temperature and left in the solution until interfacial interactions between the MoS<sub>2</sub>, SiO<sub>2</sub>, and KOH solution caused the PMMA/MoS<sub>2</sub> layer to release from the SiO<sub>2</sub>/Si substrate.

Upon release, the MoS<sub>2</sub> with the PMMA handling layer was transferred from the KOH solution into a DI water bath, where it was floated for 10 min to disperse any KOH residue still present on the MoS<sub>2</sub>. This PMMA/MoS<sub>2</sub> film stack was transferred again to another DI water bath, where it sat for another 10 min to further dilute any KOH residue. Finally, the PMMA/MoS<sub>2</sub> film stack was transferred onto the target substrate within the DI water bath. Once the transfer was complete, the PMMA/MoS<sub>2</sub> film stack was lightly dried with nitrogen gas (N<sub>2</sub>) to remove any

interfacial water. The sample was then dried at room temperature in a fume hood overnight.

After drying overnight, the PMMA layer was removed from the MoS<sub>2</sub> by immersing the sample in an acetone bath at room temperature for at least 2 h. Afterward, the sample was taken out of the acetone, rinsed with isopropyl alcohol (IPA), and dried using N<sub>2</sub>. Forming gas anneals can help remove any remaining PMMA residue, but for these devices a forming gas anneal was skipped to limit the exposure of the polyimide layer to high temperatures. At this point, the transferred MoS<sub>2</sub> film was ready for processing (Fig. 3).



**Fig. 3** Cross-section of the device stack after MoS<sub>2</sub> transfer

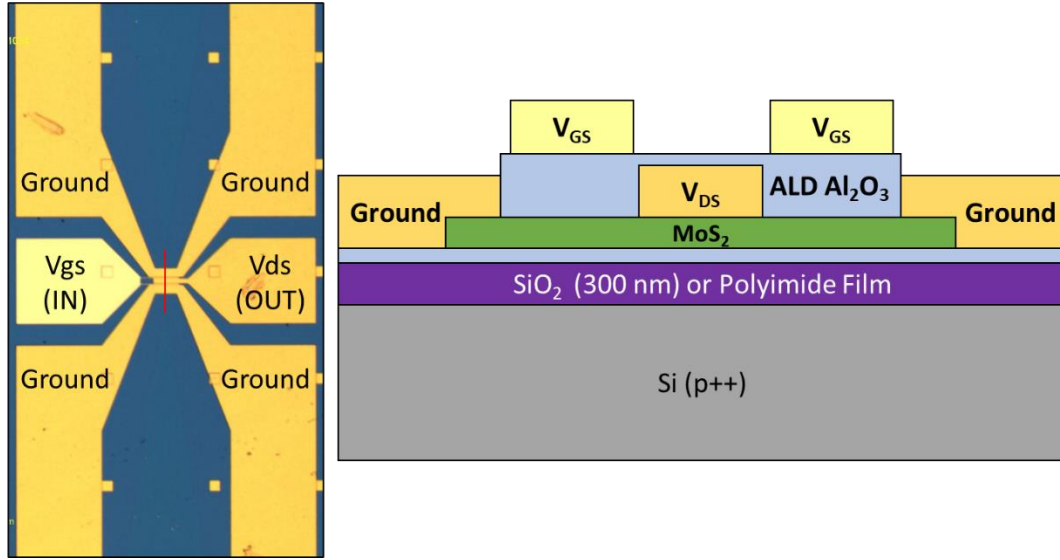
## 2.4 MoS<sub>2</sub> RF FET Fabrication Process

After material transfer, areas of clean, monolayer MoS<sub>2</sub> were identified via optical microscopy (Olympus OLS 4000 LEXT), and the following steps were performed:

- 1) MoS<sub>2</sub> channel etch
- 2) Source and drain contact metallization
- 3) Top-gate dielectric deposition
- 4) Top-gate contact metallization

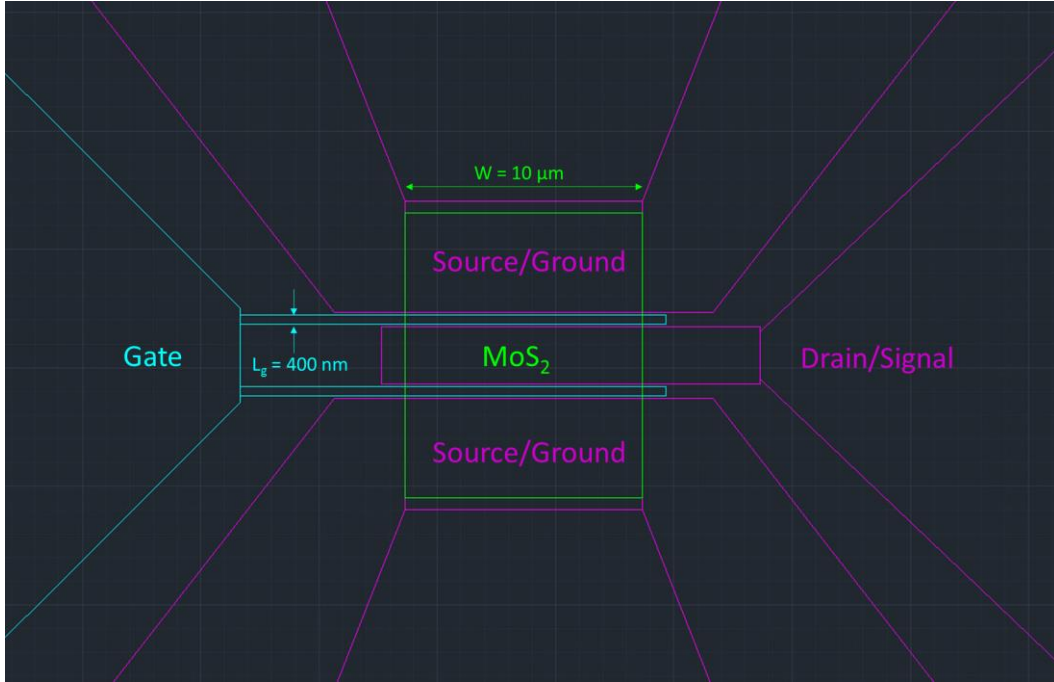
All patterning for etching and deposition steps was performed using a PMMA layer defined by electron beam lithography (EBL). PMMA 950 A4 was spun at 2000 rpm, giving a thickness around 300 nm, and baked on a hotplate at 185 °C for 2 min. The base exposure dose used was 850  $\mu\text{C}/\text{cm}^2$  and development was performed in a 10-mL methyl isobutyl ketone (MIBK): 25-mL IPA solution for 75 s, followed by N<sub>2</sub> drying.

A single RF FET device design was used and around 10 identical devices were fabricated on both substrate types. To understand the device fabricated, in Fig. 4 we first show an example optical image of a completed device on the thermal oxide substrate along with a simplified cross-section of the device.



**Fig. 4** Optical image of a completed device (left) and corresponding cross-section (right); red line on optical image indicating location of cross-section

The device was designed to be tested in the ground-signal-ground (GSG) configuration, accommodating probe pitches of 50–150  $\mu\text{m}$ . A zoomed-in image of the RF FET computer-aided design (CAD) is provided in Fig. 5. The gate length was 400 nm and the drain-source distance was 600 nm, meaning there was a 100-nm gap on either side to allow for some alignment inaccuracy. The transistor channel width was 10  $\mu\text{m}$ .

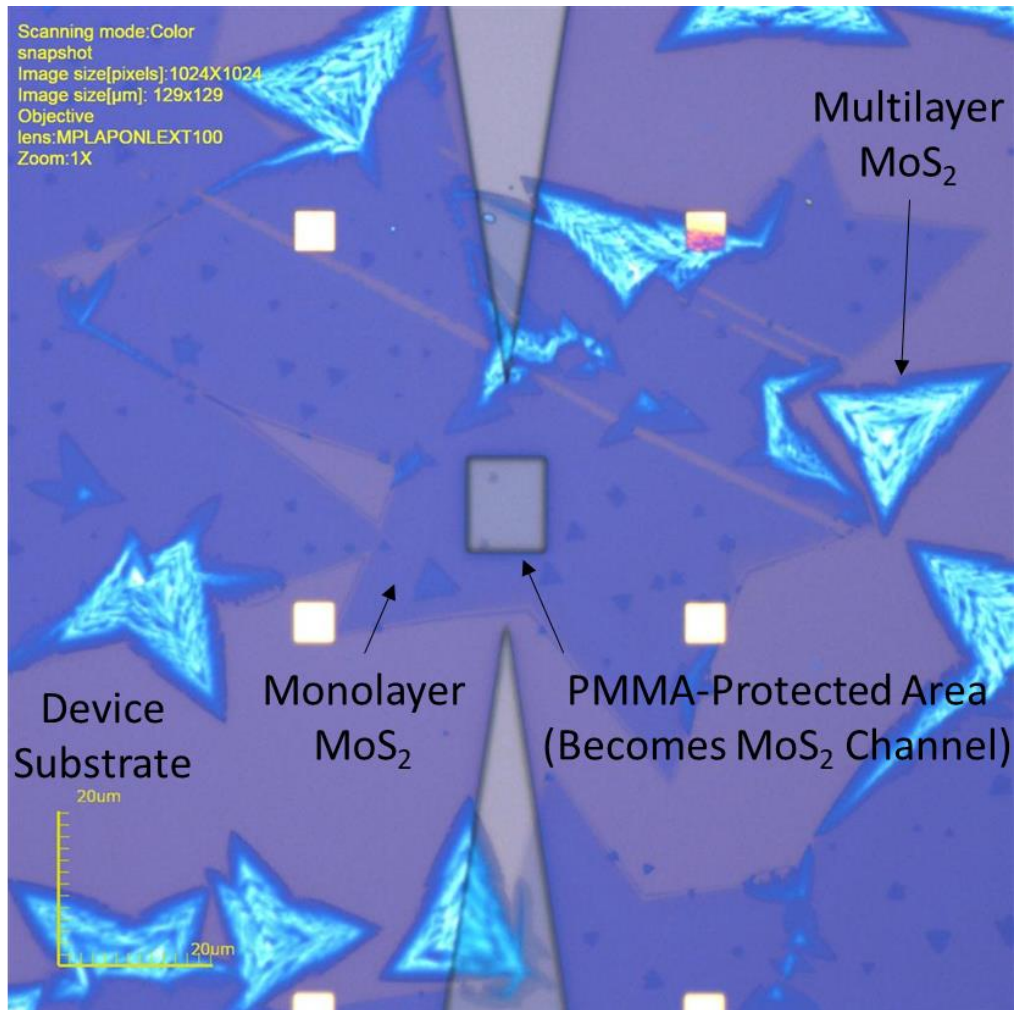


**Fig. 5** CAD drawing of the RF transistor fabricated with important dimensions labeled. The colors correspond to the different layers: green = MoS<sub>2</sub> channel, magenta = drain and source metal contact layer, and cyan = top-gate metal layer.

#### 2.4.1 MoS<sub>2</sub> Channel Etch

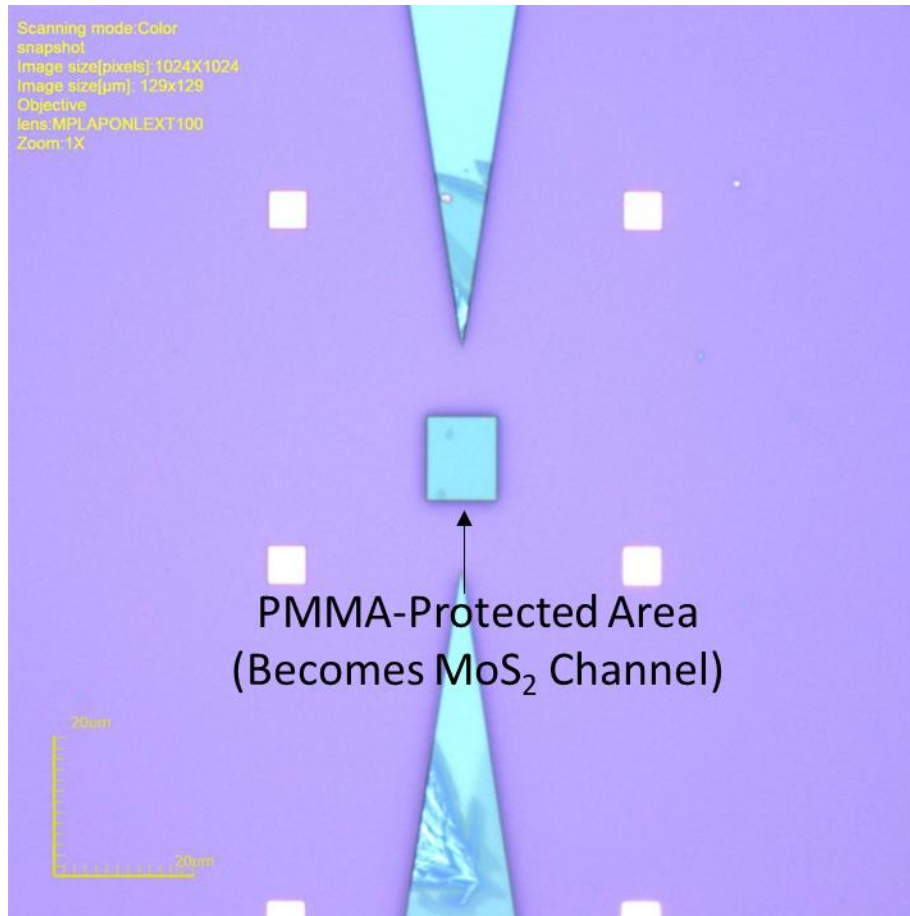
The MoS<sub>2</sub> channel (green section in Figs. 4 and 5) dimensions were formed through 45 s of reactive ion etching (RIE) using 15 sccm of tetrafluoromethane (CF<sub>4</sub>), 5 sccm of O<sub>2</sub>, and 200 W of RF power (Ulvac NE550e Etcher). It should be noted that since these devices were made, we have switched to a dry-etching process based on chlorine (Cl<sub>2</sub>) and O<sub>2</sub>, with a pure O<sub>2</sub> second step to minimize residue.<sup>17</sup>

Figure 6 shows an example device after the channel-defining EBL step, but before the RIE step. The example device shown is on the 300-nm thermal oxide wafer and as can be seen in the optical image, the MoS<sub>2</sub> growth was not uniform and did not cover the whole chip. The gray rectangle represents the area chosen for device fabrication and was protected by PMMA while the rest of the MoS<sub>2</sub> was removed. It should be noted that sometimes, as in this example device, the area of MoS<sub>2</sub> to be covered with metal contacts had small regions of bilayer growth, but the areas that form the transistor channel were always monolayer growth.



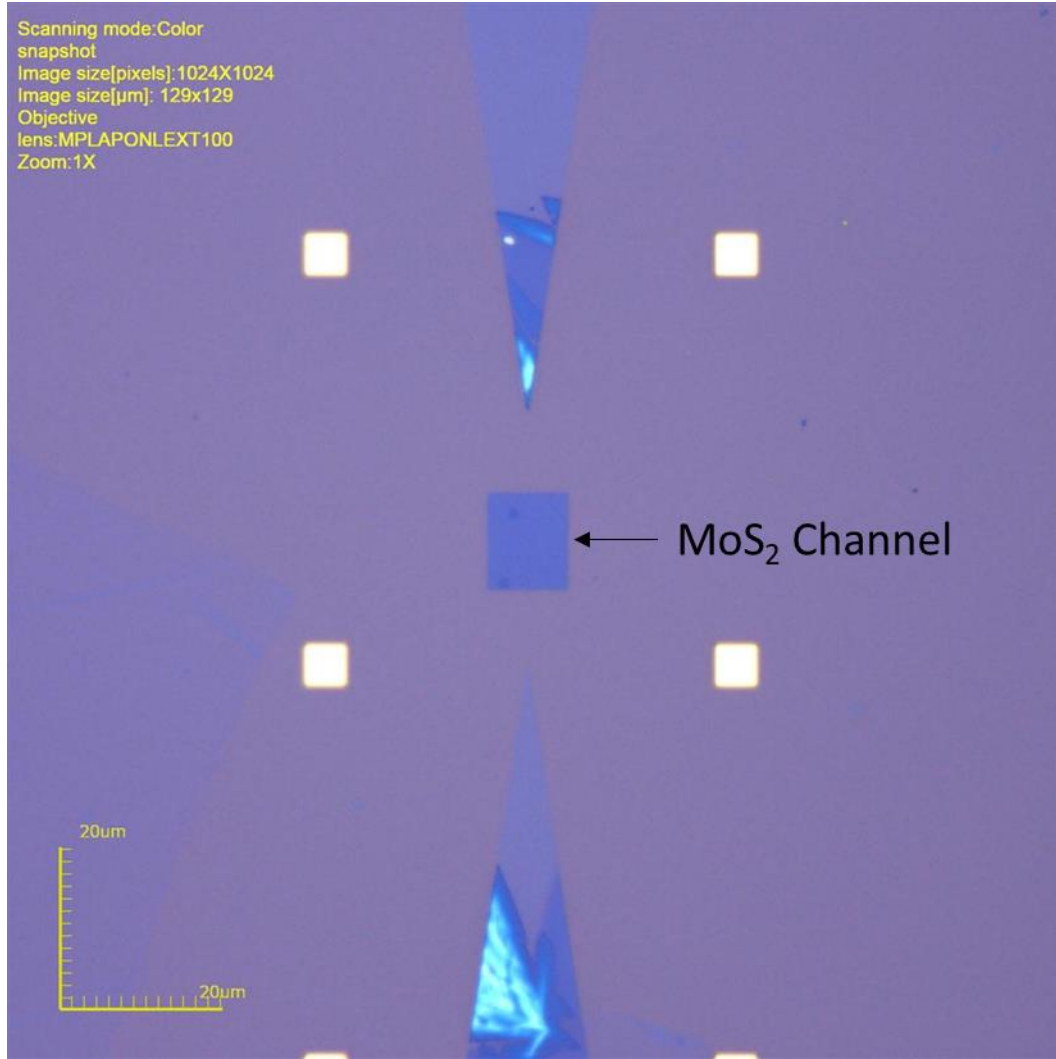
**Fig. 6** Optical image of a device after EBL exposure and development to form the MoS<sub>2</sub> channel, but before MoS<sub>2</sub> etching

Figure 7 shows the same example device after the RIE step was performed to etch away all the MoS<sub>2</sub>, but prior to removal of the PMMA in acetone. Although it is not shown in the image, the boundary of where we performed the RIE step extended past where the metal contact pads will be by around 10 μm in all directions to avoid unwanted conduction pathways across the MoS<sub>2</sub> growth or between devices.



**Fig. 7** Channel area after the channel-defining RIE, but before PMMA removal in acetone

Lastly, Fig. 8 shows the MoS<sub>2</sub> channel after removal of the PMMA layer in acetone.

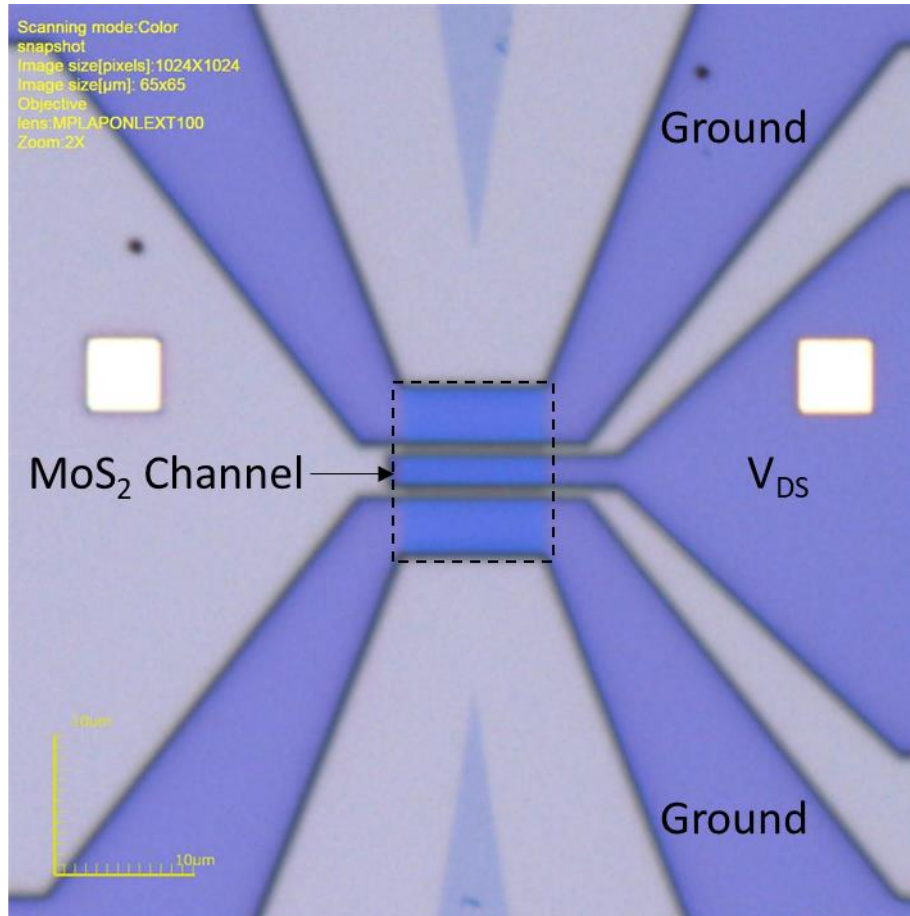


**Fig. 8** Channel area after RIE and PMMA removal in acetone

#### **2.4.2 Source and Drain Contact Metallization**

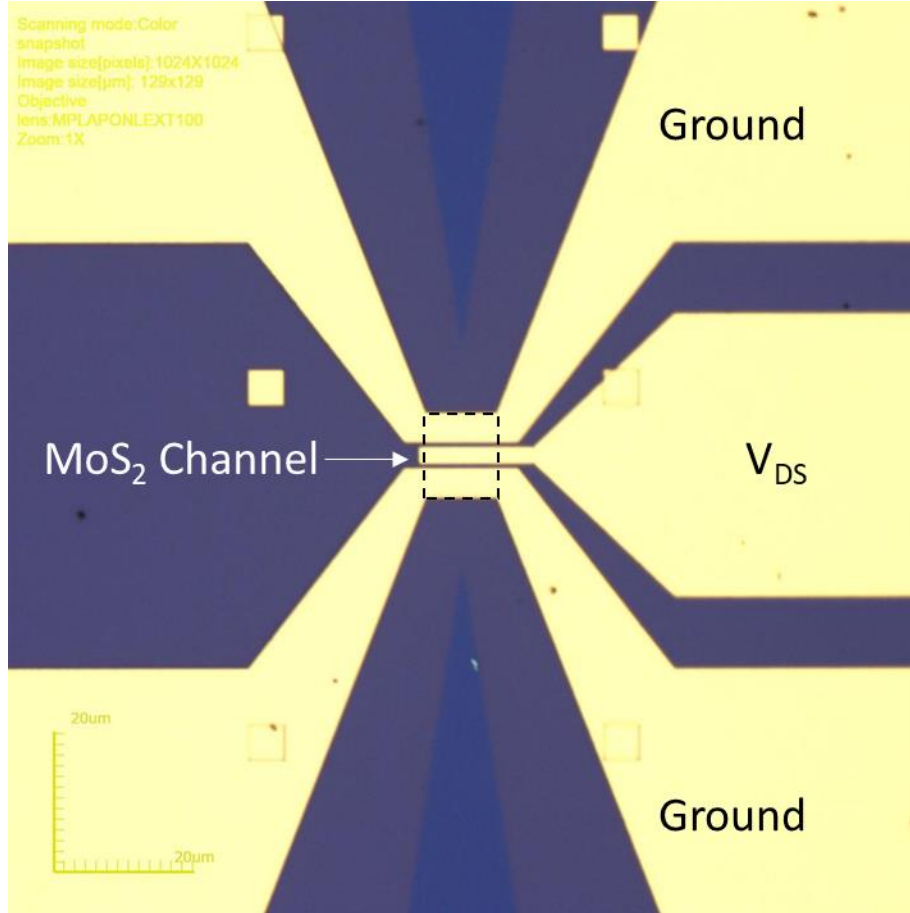
Metal source/drain contacts (darker-gold layer in Fig. 4, magenta in Fig. 5) of silver (Ag)/gold (Au) (30/70 nm) were deposited via electron beam evaporation (CHA Industries) at a pressure of  $1 \times 10^{-6}$  Torr, followed by liftoff in acetone.

Figure 9 shows an example device after the source/drain contact EBL step, but before the metallization step. The MoS<sub>2</sub> channel formed by the previous RIE step is indicated by the dashed rectangle and the electrical nodes to be formed are labeled accordingly with Figs. 4 and 5.



**Fig. 9** Device after metal contact EBL, prior to metal evaporation for the source/drain contacts

After the metal contact layer was deposited, the chips were soaked in acetone for liftoff. The acetone was not heated above 40 °C to avoid bubbling that can lead to delamination of the polyimide layer. Figure 10 shows an example device after metal deposition and liftoff.



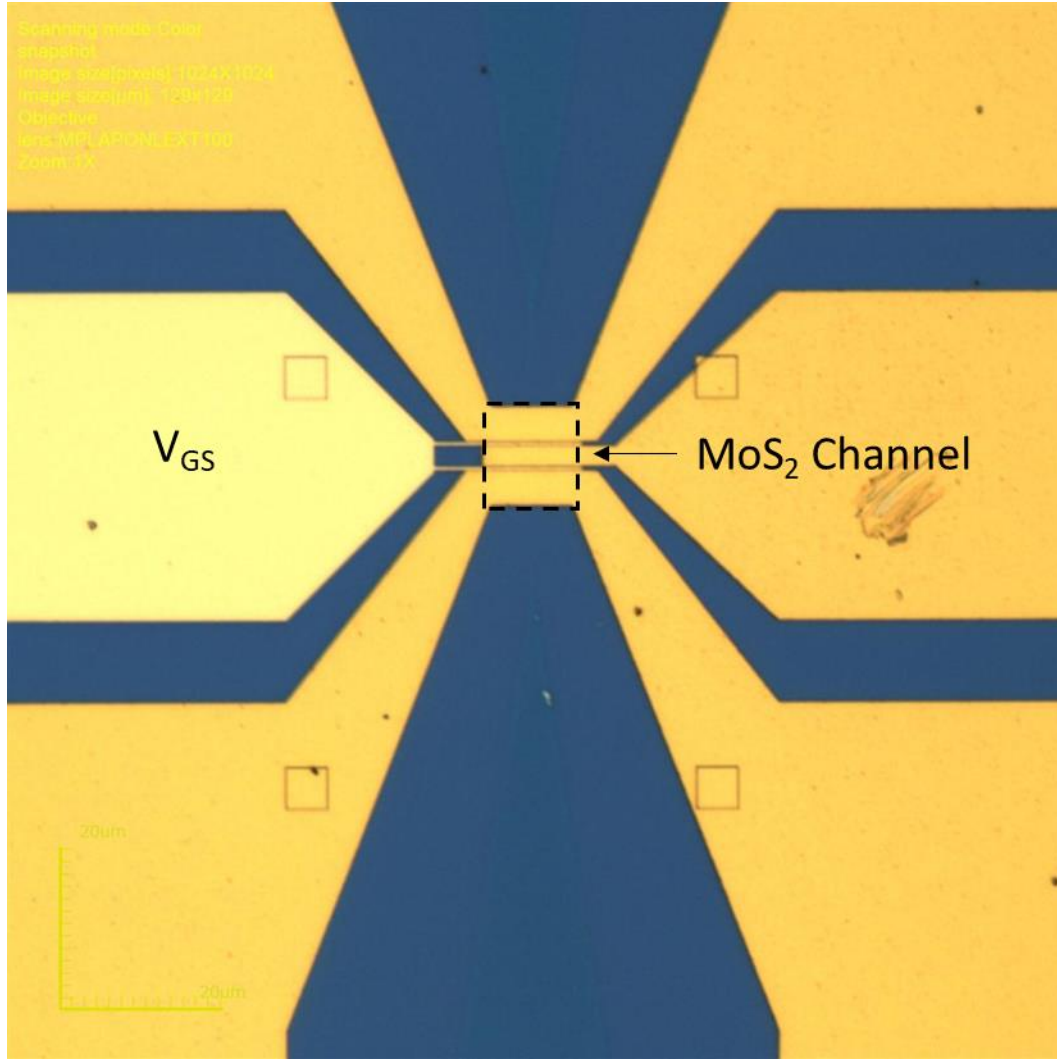
**Fig. 10** Device after source/drain metal contact deposition and liftoff

### 2.4.3 Top-Gate Dielectric Deposition

The top-gate dielectric deposition process was identical to the process used for the bottom dielectric interface described in Section 2.2. Once again, a 1-nm Al seed layer was deposited via e-beam evaporation, allowed to oxidize in air, then 250 cycles of  $\text{Al}_2\text{O}_3$  were deposited via PEALD using  $\text{O}_2$  and TMA precursors.

### 2.4.4 Top-Gate Metallization

The final step in the fabrication process was the deposition of the top-gate metal. This process was identical to the source/drain contact metallization, except the metals deposited were nickel (Ni)/Au (20/80 nm) (Fig. 11).



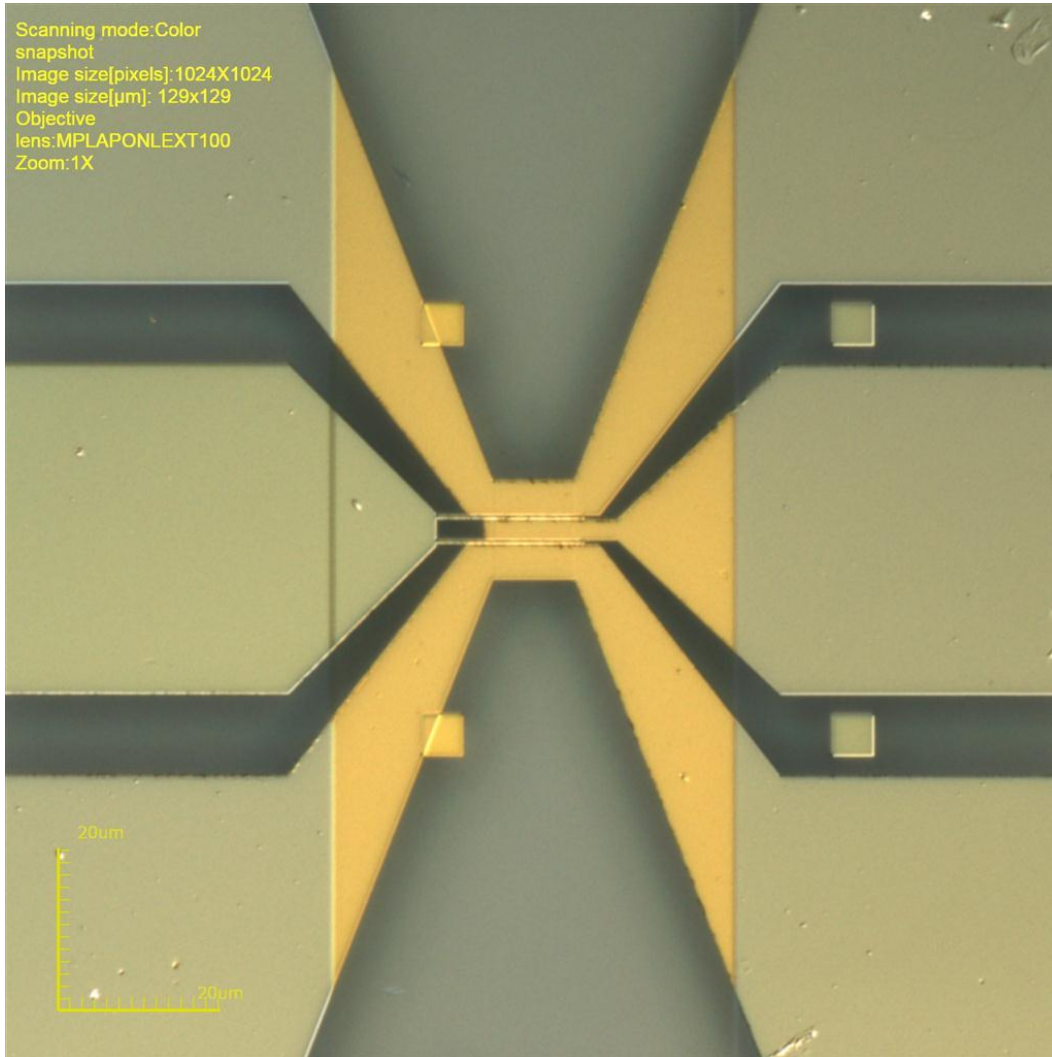
**Fig. 11 Device after top-gate metal contact deposition and liftoff**

We experimented with adding a top-dielectric etch step to get clean access to the metal contact pads but determined that the probes easily scratched through the PEALD layer and had reliable electrical contact.

#### **2.4.5 Polyimide-Specific Fabrication Techniques**

We were apprehensive about performing EBL on a nonconductive surface (polyimide), so we used a conductive layer of poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS), 3% to 4% Sigma Aldrich 655201 to avoid charging artifacts. Sometimes PEDOT:PSS can be difficult to remove after exposing large areas to high-energy electrons. To achieve full removal of the PEDOT:PSS film, the samples were soaked in 80 °C water and lightly agitated until the film lifted off (usually within a minute or two). After removal of the conductive

film, the PMMA was developed as usual in the MIBK and IPA solution. Figure 12 shows an optical image of a completed RF FET on the polyimide substrate.



**Fig. 12 Completed RF FET on polyimide**

## **2.5 DC Electrical Characterization**

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All devices were tested at room temperature in a vacuum probe station at a pressure no higher than  $5 \times 10^{-5}$  Torr. Prior to testing, the devices were annealed overnight at 400 °K in vacuum to drive out water vapor. A Keithley 4200 Semiconductor Characterization System was used to perform the electrical measurements. The viewport was covered with Al foil to block any light from entering the probe station.

### 2.5.1 Back-Gated Measurements

After the source/drain contact metallization step, devices without the polyimide layer were tested to get a baseline measurement using the doped Si substrate as a back-gate electrode. Since the polyimide substrate is insulating, those devices could only be measured after completing the entire top-gate fabrication process.

Devices were tested with a constant drain-source bias ( $V_{DS}$ ) of 100 mV, while sweeping the back-gate voltage ( $V_{GS}$ ) back and forth from  $-30$  to  $+60$  V and measuring the drain-source current ( $I_{DS}$ ).

Calculations in this report for back-gated measurements used a relative permittivity of  $\epsilon_{ox} = 3.9$  for  $\text{SiO}_2$  and a thickness of  $t_{ox} = 300$  nm.

### 2.5.2 Top-Gated Measurements

After finishing the fabrication process, devices were tested to determine proper DC biasing conditions for the RF testing. Devices were tested with a constant  $V_{DS}$  of 100 mV, while sweeping the top-gate voltage back and forth from  $-10$  to  $+10$  V (or sometimes  $-20$  to  $+10$  V when looking for complete turnoff, usually avoided to limit the electric field across the gate oxide).

From the  $I_{DS}$ - $V_{GS}$  measurement, a range of suitable top-gate voltages were chosen to step through, while  $V_{DS}$  was swept from 0 to 5 V. These  $I_{DS}$ - $V_{DS}$  curves provide the information for determining DC biasing conditions during the RF testing.

The calculations in this report for top-gated measurements used a relative permittivity of  $\epsilon_{ox} = 9$  for  $\text{Al}_2\text{O}_3$  and a thickness of  $t_{ox} = 25$  nm.

## 2.6 RF Electrical Characterization

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The devices with the highest transconductance and current saturation were chosen for RF testing. RF measurements were made on a Cascade Summit Probe station using a Keysight PNA-X network analyzer to obtain the small-signal S-parameter data up to 30 GHz. Being small signal, we verified that the RF power was kept quite low to avoid nonlinear effects during the measurements, while also minimizing noise effects. DC bias was provided by a Keysight B1500 parametric analyzer. GGB Industries' GSG coplanar RF probes were used to apply the DC bias and launch the RF signal into the FET. During fabrication mask layout, we verified that a 50-ohm environment existed at the probe pads and through the transition structure to the transistor using the software Keysight ADS Momentum. While RF testing, short-open-load-thru calibration was used to calibrate up to the probe tips, followed by an open-short de-embedding<sup>18</sup> to remove the parasitic effects of the large pads use for landing the probes (Fig. 13). Analysis of the RF data was performed using Keysight ADS software.

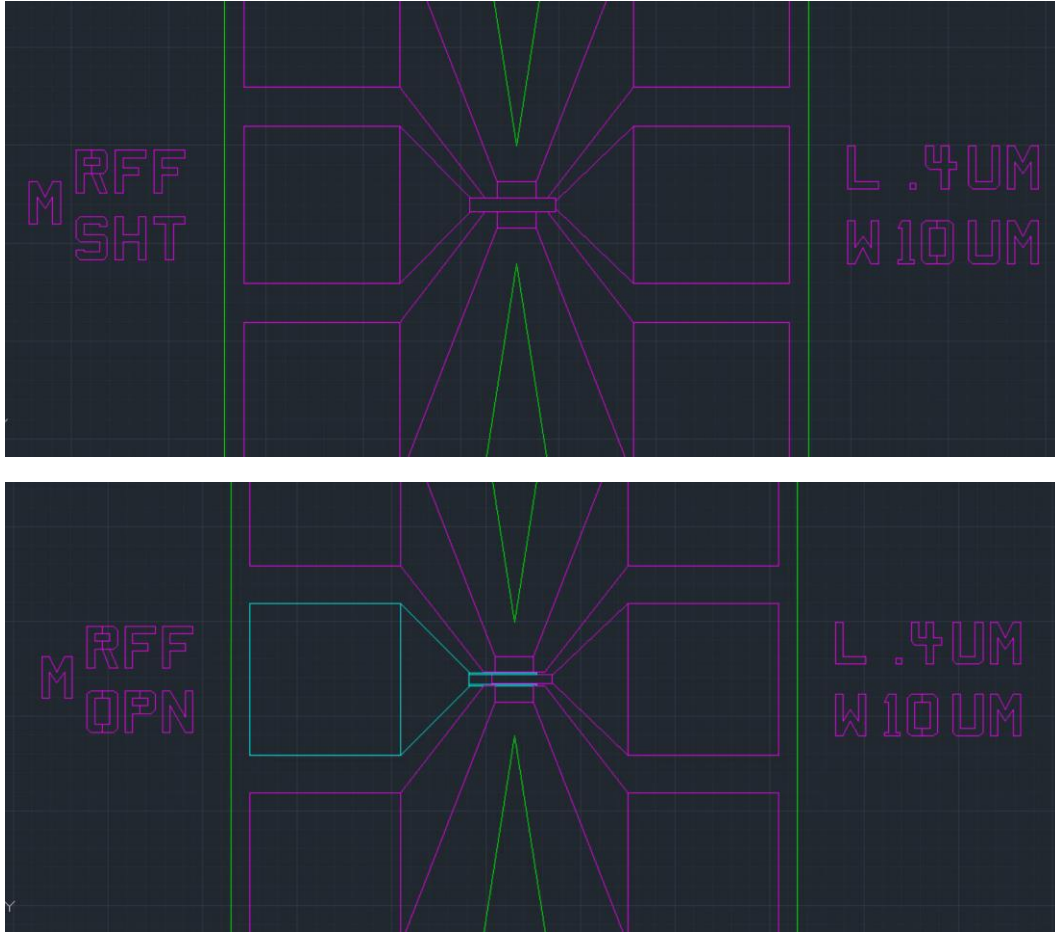


Fig. 13 CAD for the short and open test structures fabricated for de-embedding

### 3. Results

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Section 3.1 provides example current-voltage (I-V) curves from the DC electrical testing.

Section 3.2 compiles the RF performance achieved and compares it to similar devices in the literature and the theoretical limits.

Section 3.3 compares the top-gated transistor I-V curves to standard transistor models and provides a potential explanation for the deviation in behavior.

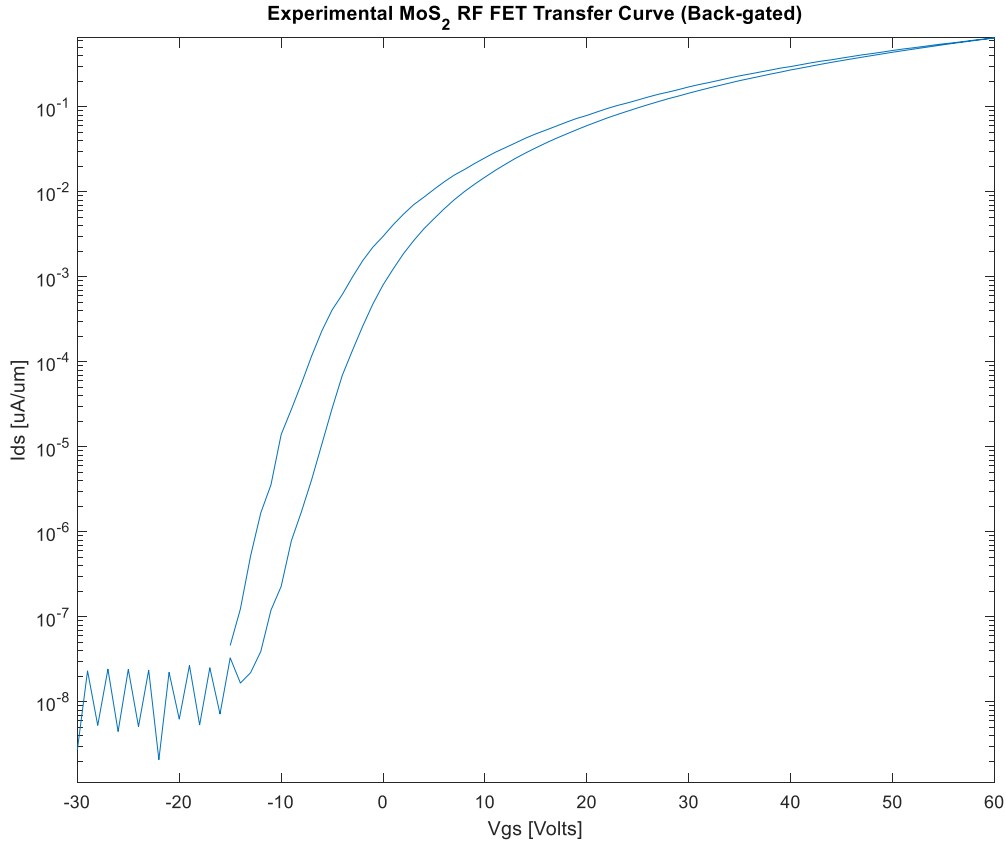
#### 3.1 DC Electrical Data

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##### 3.1.1 Back-Gated Testing

A typical transfer curve obtained from the back-gated testing is shown in Fig. 14. The transistors were completely off at a  $V_{GS}$  of  $-30$  V and had an  $I_{ON}/I_{OFF}$

approximately  $10^7$ – $10^8$ , though this is determined primarily by the capability to accurately measure the off-current.



**Fig. 14 Back-gated  $I_{DS}$  vs.  $V_{GS}$  example measurement,  $V_{DS} = 100$  mV**

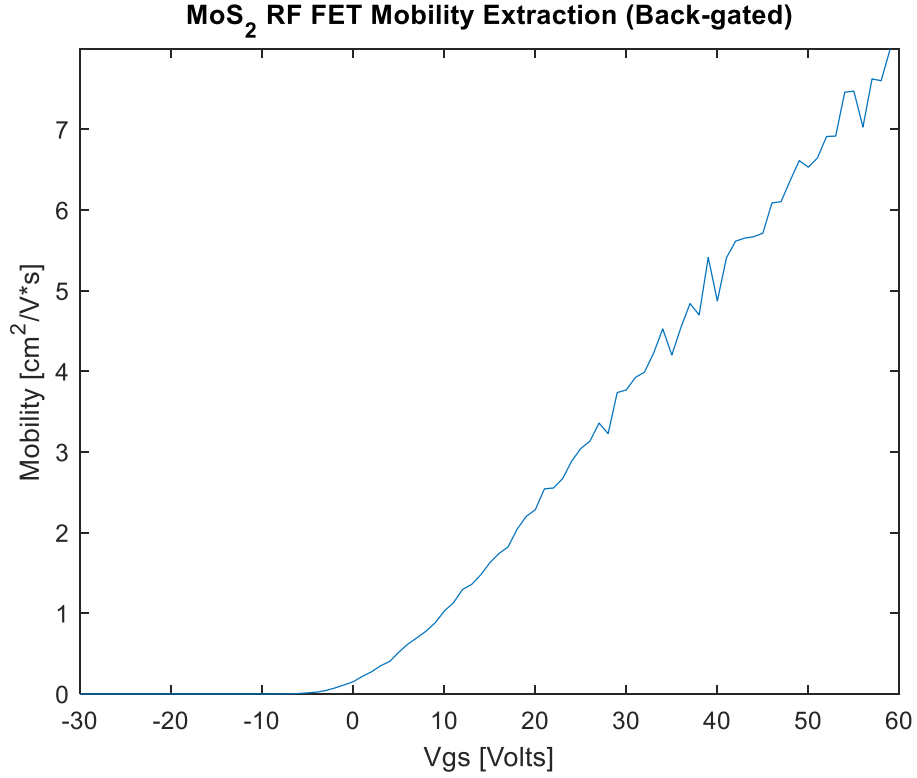
Field-effect mobility was determined from the  $I_{DS}$ – $V_{GS}$  characteristics (Fig. 15) via Eq. 1:

$$\mu_{FE} = \frac{d \frac{I_{DS}}{V_{DS}}}{dV_{GS}} \times \frac{1}{C_{ox}} \times \frac{L}{W}, \quad (1)$$

where  $V_{DS}$  is the applied drain-source voltage,  $I_{DS}$  is the measured drain current,  $V_{GS}$  is the applied gate-source voltage,  $L/W$  is the ratio of channel dimensions, and  $C_{ox}$  is the gate-channel capacitance per unit area:

$$C_{ox} = \frac{\varepsilon_{ox} \varepsilon_0}{t_{ox}}, \quad (2)$$

where  $\varepsilon_{ox}$  is the relative permittivity of the gate dielectric,  $\varepsilon_0$  is the permittivity of free space, and  $t_{ox}$  is the gate dielectric thickness.

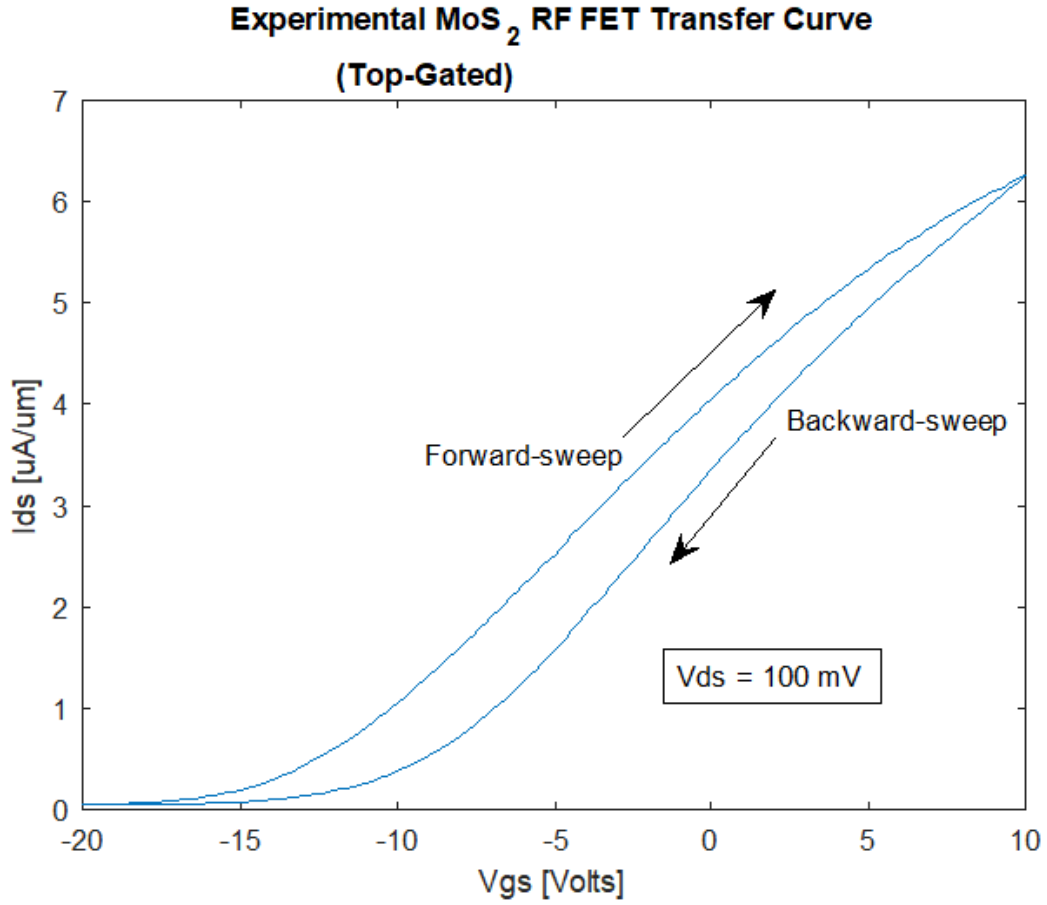


**Fig. 15 Mobility extracted from the back-gated  $I_{DS}$  vs.  $V_{GS}$  example measurement**

This version of mobility extraction is based off a two-point probe measurement, meaning that the actual intrinsic mobility of the material is higher since contact resistance is not considered. This transfer curve and carrier mobility is consistent with devices we have measured previously using monolayer MoS<sub>2</sub> grown in a similar manner.<sup>19</sup>

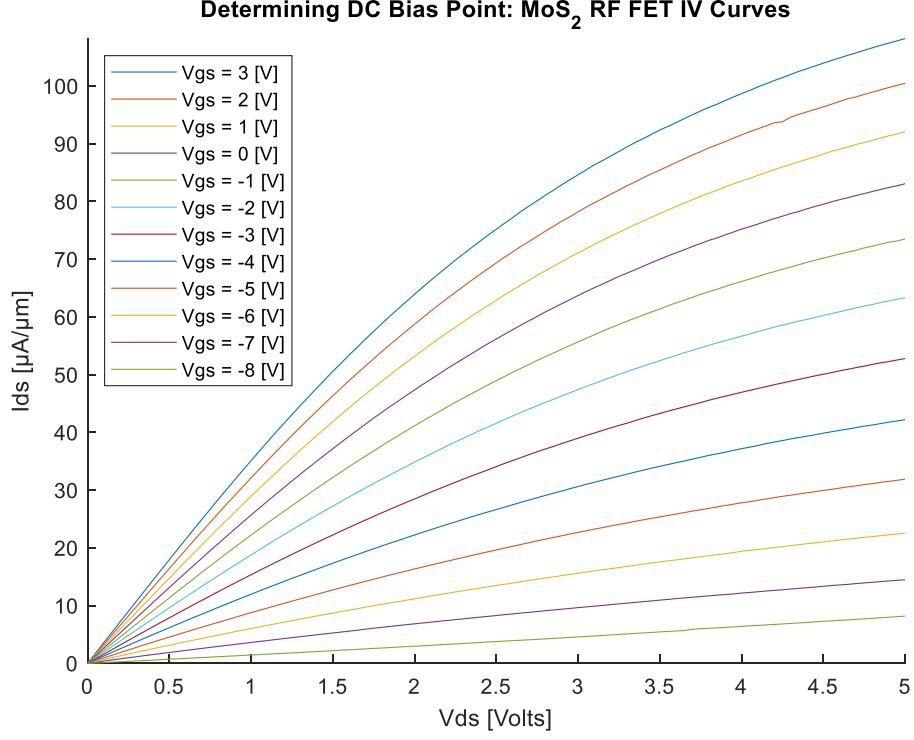
### 3.1.2 Top-Gated Testing

A typical transfer curve obtained from the top-gated testing is shown in Fig. 16. The top-gate fabrication process shifted the threshold voltage, causing the devices to be on at 0 gate voltage. This threshold voltage shift is consistent with results in the literature and other devices fabricated at the US Army Combat Capabilities Development Command Army Research Laboratory.<sup>20,21</sup>



**Fig. 16** Top-gated  $I_{DS}$  vs.  $V_{GS}$  example measurement

When testing the  $I_{DS}$ - $V_{DS}$  characteristics to find the location of maximum transconductance to for RF testing, saturating behavior was observed over a wide range of gate voltages (Fig. 17). These top-gated DC I-V curves will be examined in more detail in Section 3.3.



**Fig. 17 Top-gated  $I_{DS}$  vs.  $V_{DS}$  example measurement**

The electrical data presented in this section came from devices without the polyimide layer. In general, the devices on the polyimide substrate had a lower fabrication yield and required a higher drain bias to push a comparable current through the device.

### 3.2 RF Electrical Data

Common metrics to characterize RF transistors are  $f_T$ , the frequency at which there is unity current gain and  $f_{max}$ , the frequency at which there is unity power gain. These metrics were extracted from the measured S-parameters and are displayed graphically in this section by the frequency at which the curves hit 0 dB gain. These metrics can also be derived using small-signal transistor models and are often approximated as follows.<sup>22,23</sup>

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}, \quad (3)$$

$$f_{max} = \frac{f_T}{2} \sqrt{\frac{r_o}{R_g + R_i}}, \quad (4)$$

where  $g_m$  is the transconductance,  $C_{gs}$  and  $C_{gd}$  are the capacitances between the gate and the source/drain,  $r_o$  is the output resistance,  $R_g$  is the gate resistance, and  $R_i$  is the input resistance.

From the  $f_T$  metric, we calculate the saturation velocity using the formula

$$v_{sat} = 2\pi f_T L_g, \quad (5)$$

where  $L_g$  is the gate length of 400 nm.

### 3.2.1 RF Performance on Rigid (SiO<sub>2</sub>) Substrate

Results from the device with the highest measured  $f_T$  and  $f_{max}$  are plotted in Figs. 18 and 19. The device was biased with  $V_{GS} = -2$  V and  $V_{DS} = 5$  V.

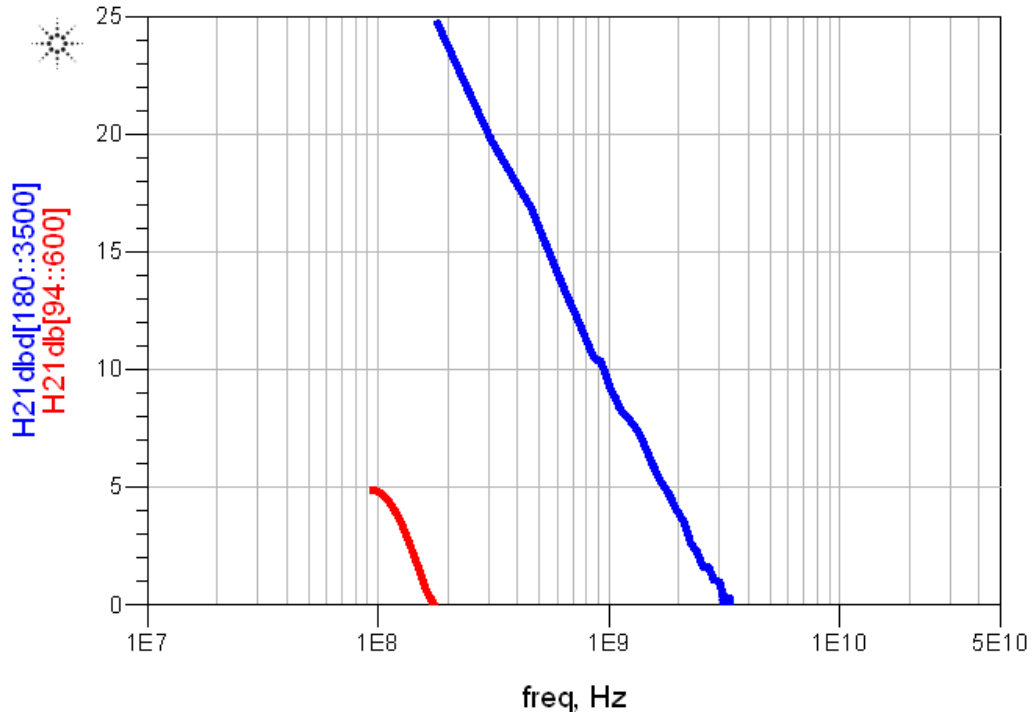


Fig. 18 Rigid substrate:  $f_T \sim 180$  MHz/3.3 GHz (extrinsic/intrinsic)

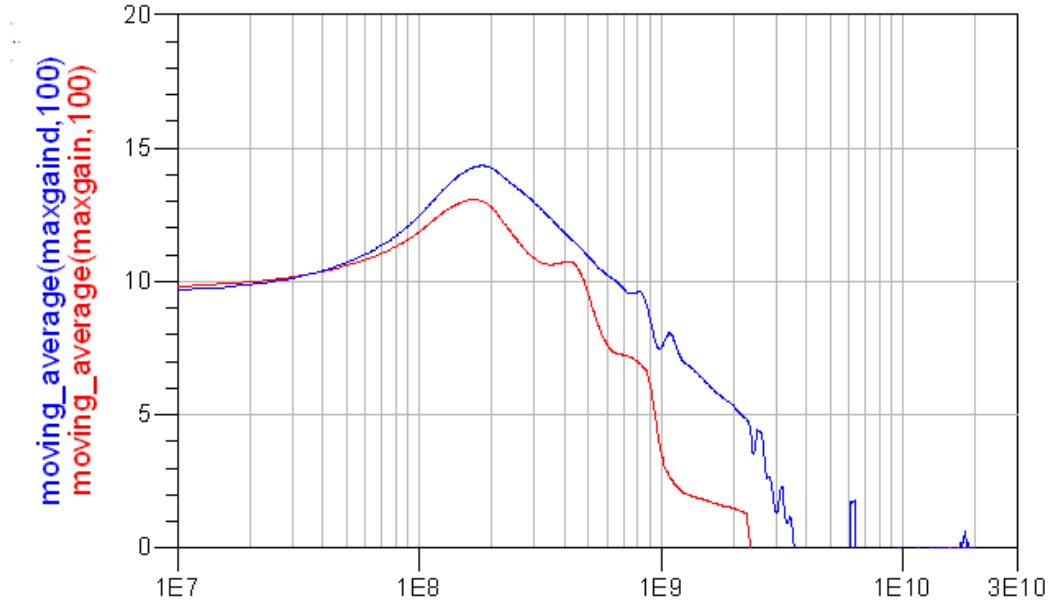


Fig. 19 Rigid substrate:  $f_{max} \sim 2.4$  GHz/3.5 GHz (extrinsic/intrinsic)

### 3.2.2 RF Performance on Flexible (Polyimide) Substrate

Results from the device with the highest measured  $f_T$  and  $f_{max}$  are plotted in Figs. 20 and 21. The device was biased with  $V_{GS} = -5$  V and  $V_{DS} = 7$  V. A summary of the data is presented in Table 1.

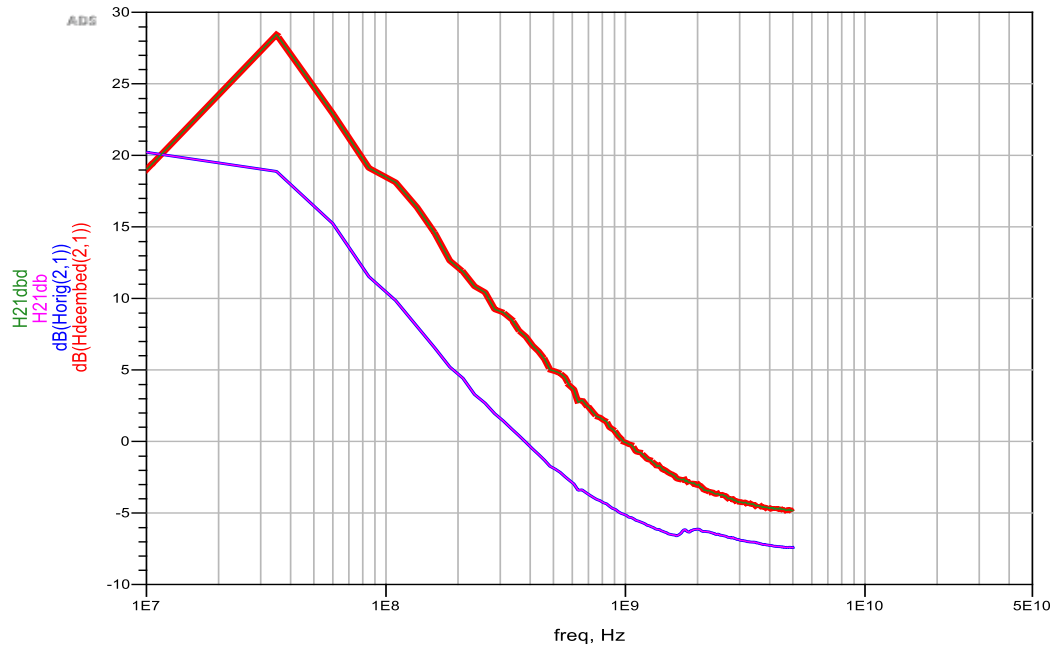


Fig. 20 Polyimide substrate:  $f_T \sim 300$  MHz/1 GHz (extrinsic/intrinsic)

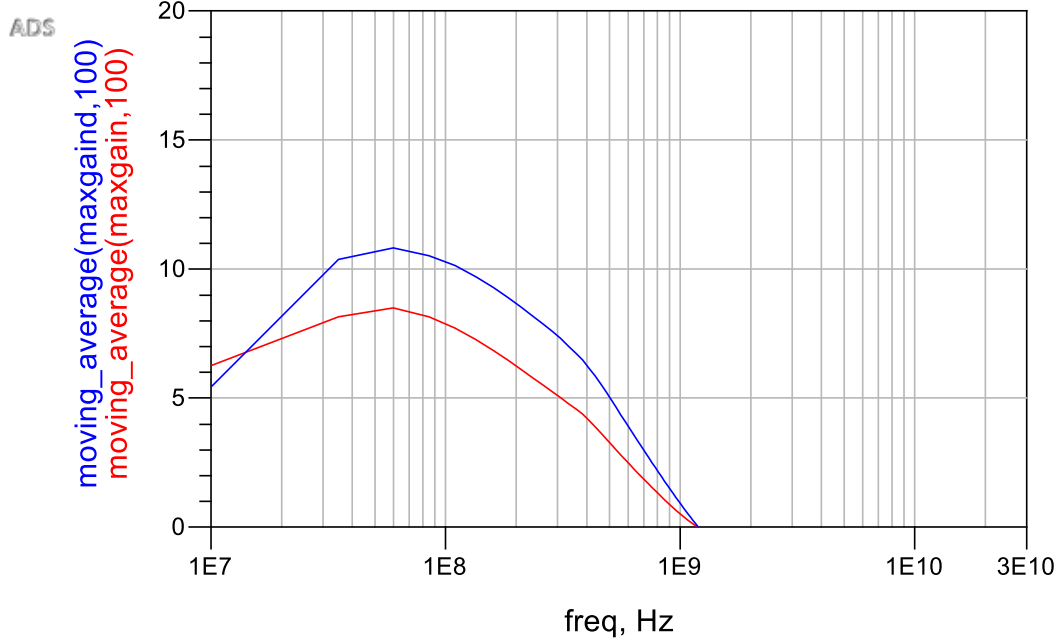


Fig. 21 Polyimide substrate:  $f_{max} \sim 1.1$  GHz/1.1 GHz (extrinsic/intrinsic)

Table 1 Summary of intrinsic RF device performance

| Substrate type            | $f_T$<br>(GHz) | $f_{max}$<br>(GHz) | $v_{sat}$<br>(cm/s) |
|---------------------------|----------------|--------------------|---------------------|
| Rigid (SiO <sub>2</sub> ) | 3.3            | 3.5                | $8.29 \times 10^5$  |
| Flexible (polyimide)      | 1.0            | 1.1                | $2.51 \times 10^5$  |

### 3.2.3 Comparison to Monolayer RF FET Performance in Literature

For monolayer MoS<sub>2</sub> devices with a similar top-gated design to ours, an  $f_T$  of 6.7 GHz,  $f_{max}$  of 5.3 GHz, and  $v_{sat}$  of  $1.1 \times 10^6$  cm/s has been achieved with a 250-nm gate length.<sup>13</sup> Using a combined metric of  $f_T \cdot L_g$  to compare our devices, this device has  $f_T \cdot L_g = 1.68$  GHz· $\mu$ m, whereas ours has  $f_T \cdot L_g = 1.32$  GHz· $\mu$ m.

However, better performance has been achieved by switching to an embedded gate structure.<sup>14</sup> With this gate-first process and a 150-nm  $L_g$ , they achieved  $f_T$  of 20 GHz,  $f_{max}$  of 11.4 GHz, and  $v_{sat}$  of  $1.88 \times 10^6$  cm/s, resulting in  $f_T \cdot L_g = 3.0$  GHz· $\mu$ m.

Section 3.3 of this report goes into detail calculating the mobility and contact resistance of a DEVCOM Army Research Laboratory–fabricated FET. Based on the information provided in Sanne et al. (2015, 2017), the difference in performance appears to be mainly a result of higher electron mobility.

### 3.2.4 RF Performance Comparison to Theoretical Limits

According to Monte Carlo simulations, the room-temperature electron velocity saturation in intrinsic MoS<sub>2</sub> is around  $3.4 \times 10^6$  to  $4.8 \times 10^6$  cm/s, although this value depends on the chosen energy separation between the K and Q valleys.<sup>15,16</sup> This, however, only includes the intrinsic scattering from phonons originating in the MoS<sub>2</sub>; other scatter processes such as from remote phonons and impurities need to be accounted for to get a more complete picture.<sup>24</sup> The velocity measured in our RF FET and the embedded gate design mentioned previously are well below the theoretical phonon-limited value, though measurements of  $v_{sat}$  approaching this limit ( $\sim 3.4 \times 10^6$  cm/s at room temperature) have been measured in monolayer MoS<sub>2</sub> FETs after accounting for device self-heating.<sup>25</sup>

## 3.3 Device I-V Modeling

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While this report focuses on devices made for RF operation, MoS<sub>2</sub> FETs are still a relatively new technology and investigating the DC I-V characteristics can provide useful insights. Only the top-gated devices are investigated here for modeling the I-V characteristics. The back-gated devices have extremely thick gate dielectrics (hundreds of nanometers). This thick oxide requires gate voltages up to  $\pm 100$  V to fully sweep the on/off range of the transistor. This effectively restricts operation of back-gated transistors to the linear regime since reaching the saturation condition ( $V_{DS} > V_{GS} - v_{th}$ ) would require large drain-source biases and cause device destruction. The top-gated devices on the other hand have thin enough gate dielectrics ( $\sim 25$  nm) to enable saturation at feasible drain-source voltages and were tested over the range of 0–5 V  $V_{DS}$ .

### 3.3.1 Simple FET Model with Contact Resistance

Neglecting channel length modulation, the standard metal–oxide–semiconductor field-effect transistor (MOSFET) I-V equations are listed as follows:

Linear Regime ( $V_{GS} > v_{th}$ ,  $V_{DS} < V_{GS} - v_{th}$ ):

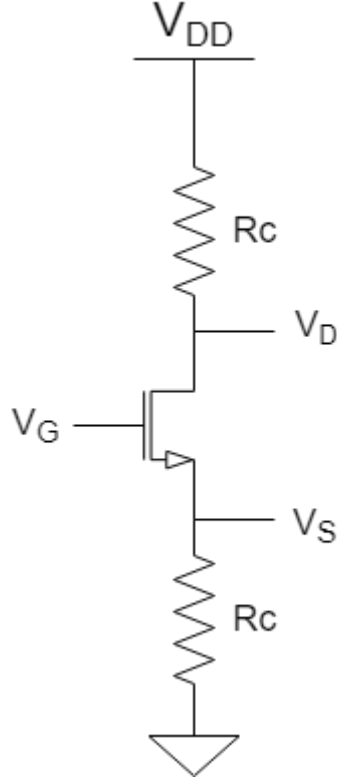
$$I_{DS\ LIN} = \frac{\mu_n C_{OX} W}{L} \left[ [V_{GS} - V_{th}] V_{DS} - \frac{V_{DS}^2}{2} \right]. \quad (6)$$

Saturation Regime ( $V_{GS} > v_{th}$ ,  $V_{DS} > V_{GS} - v_{th}$ ):

$$I_{DS\ SAT} = \frac{\mu_n C_{OX} W}{2L} [V_{GS} - V_{th}]^2. \quad (7)$$

Not included in these equations is the impact of contact resistance,  $R_c$ . The main impact this has is that the applied drain-source voltage is no longer the potential

that is dropped across the channel due to some of the potential being dropped across the contact resistance. This is shown schematically in the circuit diagram provided in Fig. 22.



**Fig. 22 Simple transistor model including contact resistances**

To determine the impact that the contact resistance is having, we first assume the contact resistance does not significantly change with gate voltage since the metal contacts screen the MoS<sub>2</sub> underneath it from the gate electric field (unlike in the back-gated configuration where the MoS<sub>2</sub> under the contacts are not screened and the contact resistance is known to change significantly with gate voltage).<sup>19,26</sup>

The voltage seen across the channel becomes

$$V_{DS} = V_{DD} - I_{DS}2R_c. \quad (8)$$

$$R_{TOTAL} = 2R_c + R_{MoS2}. \quad (9)$$

This means the contact resistance becomes more dominant as  $V_{GS}$  increases since the resistance of the MoS<sub>2</sub> channel will go down as more carriers are drawn into the channel.

### 3.3.2 FET Model Parameter Extraction

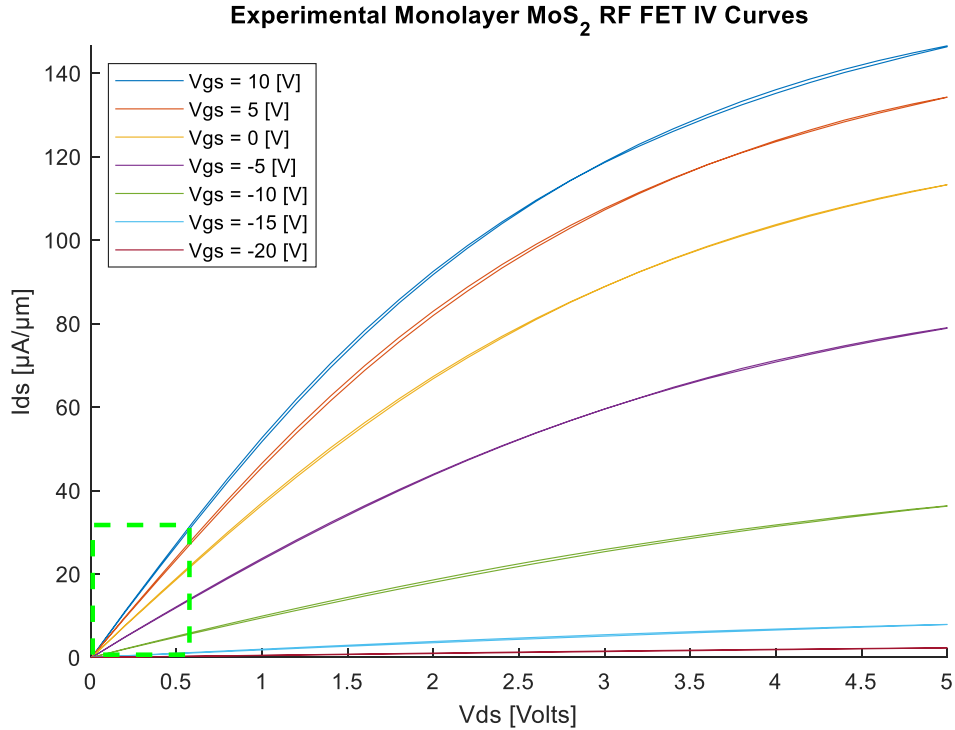
The analysis that follows calculates contact resistance by extrapolating experimental data of  $R_{TOTAL}$  versus  $V_{GS}$  to the limit when  $R_{MoS_2}$  is zero. To quantitatively see how the total resistance changes with  $V_{GS}$ , we can look at the linear regime equation and make some approximations. At low  $V_{DS}$  and higher  $[V_{GS} - V_{th}]$ , the quadratic term can be neglected, and linear regime equation can be approximated as linear:

$$I_{DS\ LIN} = \frac{\mu_n C_{OX} W}{L} [V_{GS} - V_{th}] V_{DS}. \quad (10)$$

This enables straightforward calculation of the resistance of the MoS<sub>2</sub> channel:

$$R_{MoS_2} = \frac{V_{DS}}{I_{DS\ LIN}} = \frac{L}{\mu_n C_{OX} W [V_{GS} - V_{th}]}. \quad (11)$$

Figure 23 shows experimental  $I_{DS} - V_{DS}$  curves obtained from testing a MoS<sub>2</sub> RF FET over a wide range of gate voltages. The total resistance was determined experimentally via Ohm's law for each gate voltage in the region highlighted by the green box ( $V_{DS} < 0.6$  V).



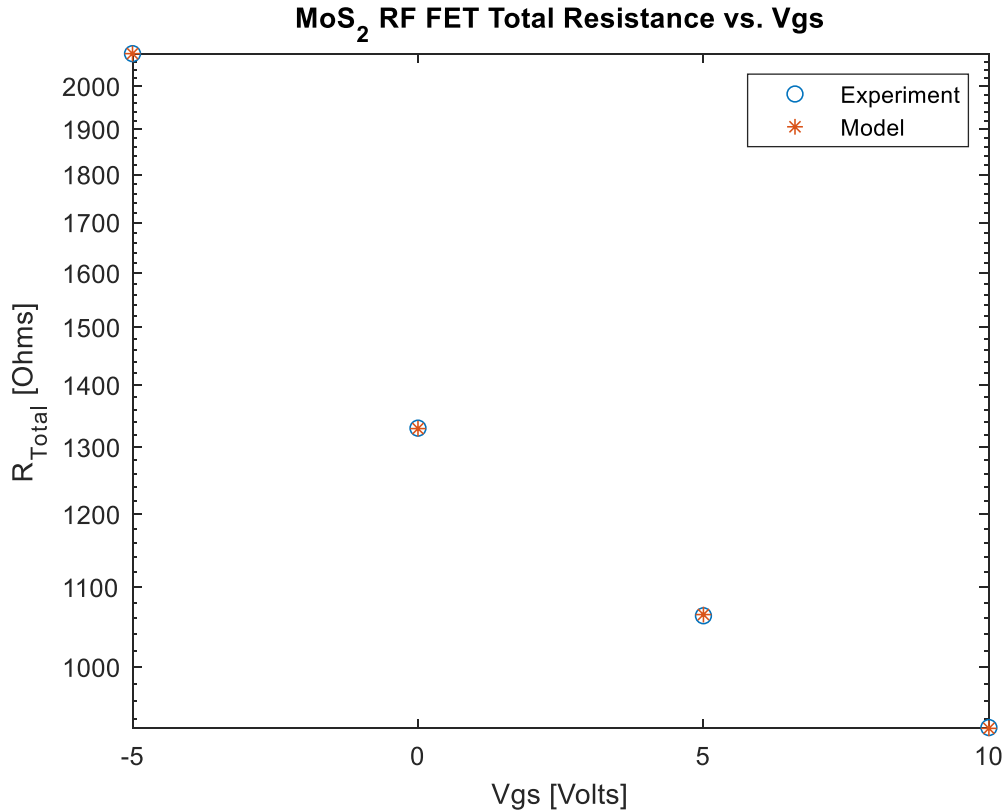
**Fig. 23**  $I_{DS} - V_{DS}$  curve of an RF FET on the rigid substrate. Dashed green box indicates region used to fit FET parameters.

$R_{TOTAL}$  was fitted numerically as a function of  $V_{GS}$  in MATLAB with three unknowns:

$$R_{TOTAL} = X_1 + \frac{X_2}{(V_{GS} - X_3)}, \quad (12)$$

where  $X_1 = 2R_c$ ,  $X_2 = \frac{L}{\mu_n C_{OX} W}$ , and  $X_3 = V_{th}$ . This fitting enabled simultaneous determination of the contact resistance, threshold voltage, and the product of the mobility and gate capacitance. Looking at how well the function fits the raw data, we can determine if our inherent assumptions (such as contact resistance and mobility not depending heavily on  $V_{GS}$ ) are valid.

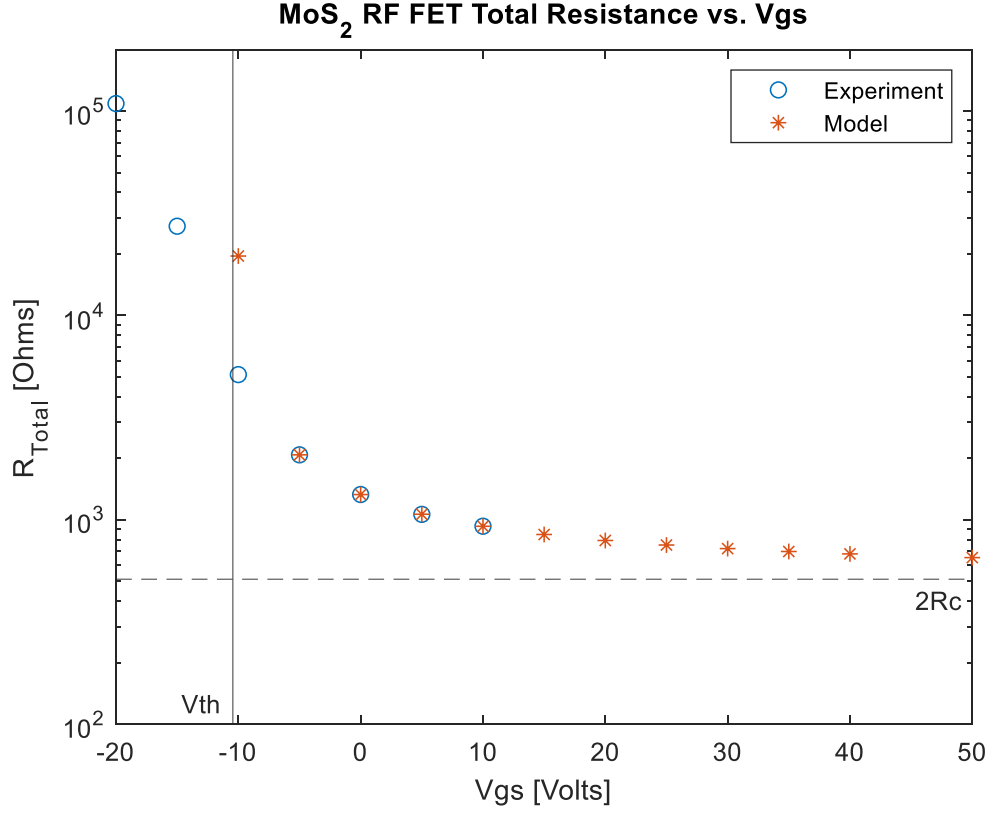
Figure 24 shows the fitting of experimental data with the model, demonstrating the high degree of accuracy, meaning either our assumptions were correct or that they happen to offset each other.



**Fig. 24** Total resistance: experimental values compared to the model

The extracted fitting parameters were  $X_1 = 2R_c = 512 \, \Omega$  ( $2.56 \, \text{k}\Omega \cdot \mu\text{m}$ ),  $X_2 = \frac{L}{\mu_n C_{OX} W} = 8542.6 \, \text{V}^2/\text{A}$ , and  $X_3 = V_{th} = -10.45 \, \text{V}$ . Using  $W = 20 \, \mu\text{m}$ ,  $L = 400 \, \text{nm}$ , and the top-gated parameters listed in Section 2.5,  $\mu_n = 7.345 \, \text{cm}^2/\text{V}\cdot\text{s}$ .

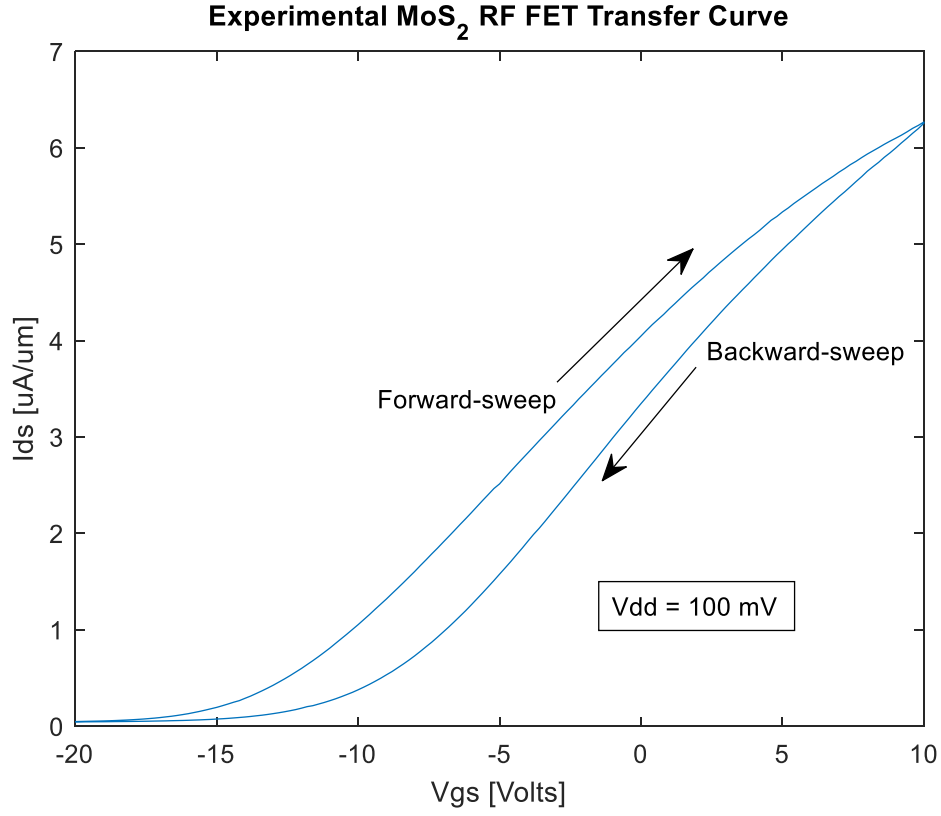
Figure 25 shows an extrapolation of the model to a wider range of gate voltages and the extracted limit of  $2R_c$ , as well as the calculated threshold voltage.



**Fig. 25** Extrapolation of the total resistance to higher gate voltages, showing the limit of twice the contact resistance as the dashed horizontal line and threshold voltage as the vertical line

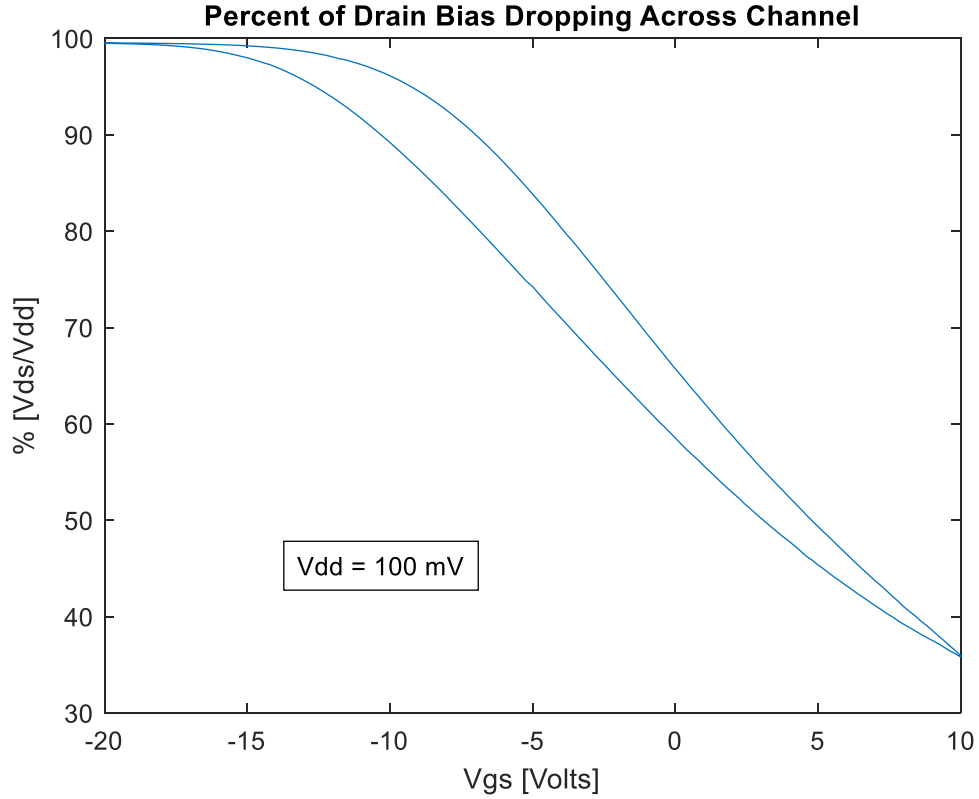
### 3.3.3 Parameter Validation and Low-Field Mobility Calculation

The threshold voltage calculated with this model ( $-10.45 \, \text{V}$ ) agrees with the qualitative behavior of the RF FET's  $I_{DS} - V_{GS}$  curve (Fig. 26).



**Fig. 26** RF FET  $I_{DS}$ - $V_{GS}$  curve (notice the extracted threshold voltage of  $-10.45$  from the  $I_{DS}$ - $V_{DS}$  curves qualitatively makes sense)

After determining  $R_c$ , we calculate the voltage dropping across the contacts ( $2R_c I_{DS}$ ) versus the voltage dropping across the channel ( $V_{DD} - 2R_c I_{DS}$ ) (Fig. 27).



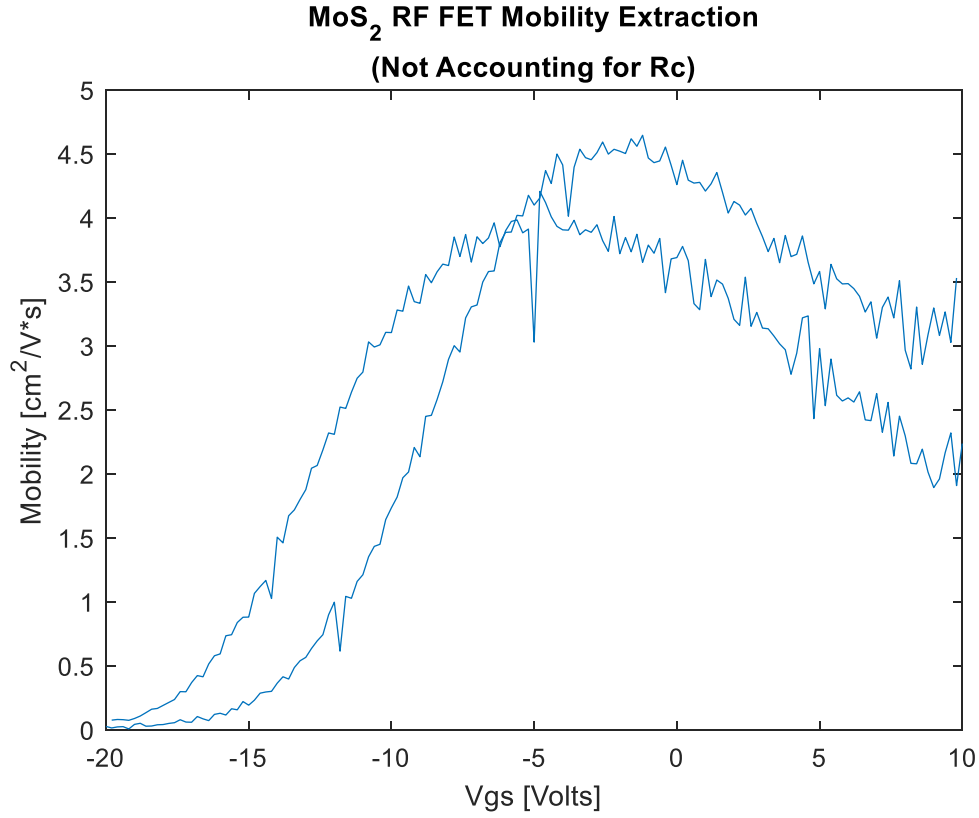
**Fig. 27** After extracting the contact resistance, we can determine how much of the applied voltage  $V_{DD}$  is dropped across the channel vs. the contact resistance. At low gate voltages most of the voltage drops across the channel, but at high gate voltages most drops across the contact resistance.

Based on this result, once the gate voltage is 5 V or higher, most of the applied voltage is dropping across the parasitic contact resistance rather than the MoS<sub>2</sub> channel.

Next we looked at how the contact resistance impacts the extraction of the field-effect mobility from the transfer curve. As mentioned earlier, mobility is normally calculated from the  $I_{DS} - V_{GS}$  curve with the following formula:

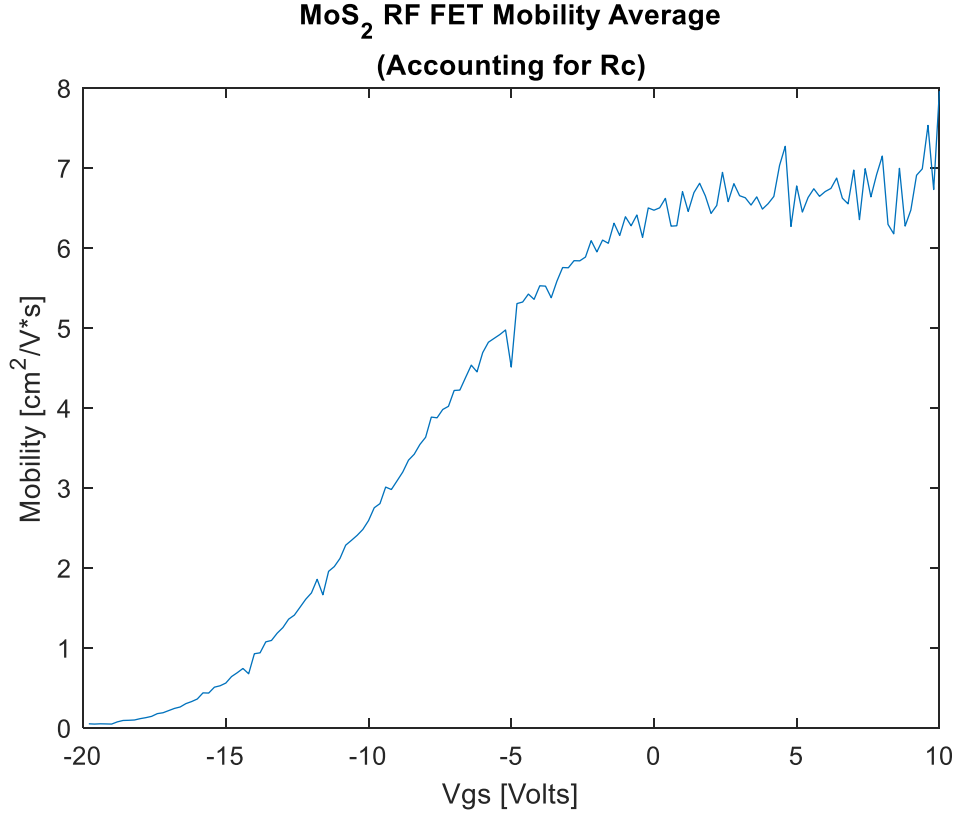
$$\mu_{FE} = \frac{dI_{DS}}{dV_{GS}} \frac{L}{C_{OX}W}. \quad (13)$$

Without considering the impact of contact resistance, the  $V_{DS}$  term is considered to be the same as the applied voltage  $V_{DD}$ . Figure 28 shows the extraction of mobility from the transfer curve without including contact resistance.



**Fig. 28** Field-effect mobility extracted from the RF FET  $I_{DS}$ - $V_{GS}$  curve as measured (not considering contact resistance)

When including the impact of contact resistance, the  $V_{DS}$  term is equal to  $V_{DD} - I_{DS}2R_C$ . Figure 29 shows the extraction of mobility from the transfer curve while including contact resistance and averaging the two sweep directions. Note that extracted field-effect mobility approaches the  $7.345 \text{ cm}^2/\text{V}\cdot\text{s}$  value determined by the total resistance model.



**Fig. 29** Field-effect mobility extracted from the RF FET  $I_{DS}$ - $V_{GS}$  curve after incorporating the voltage dropped across the contact resistance

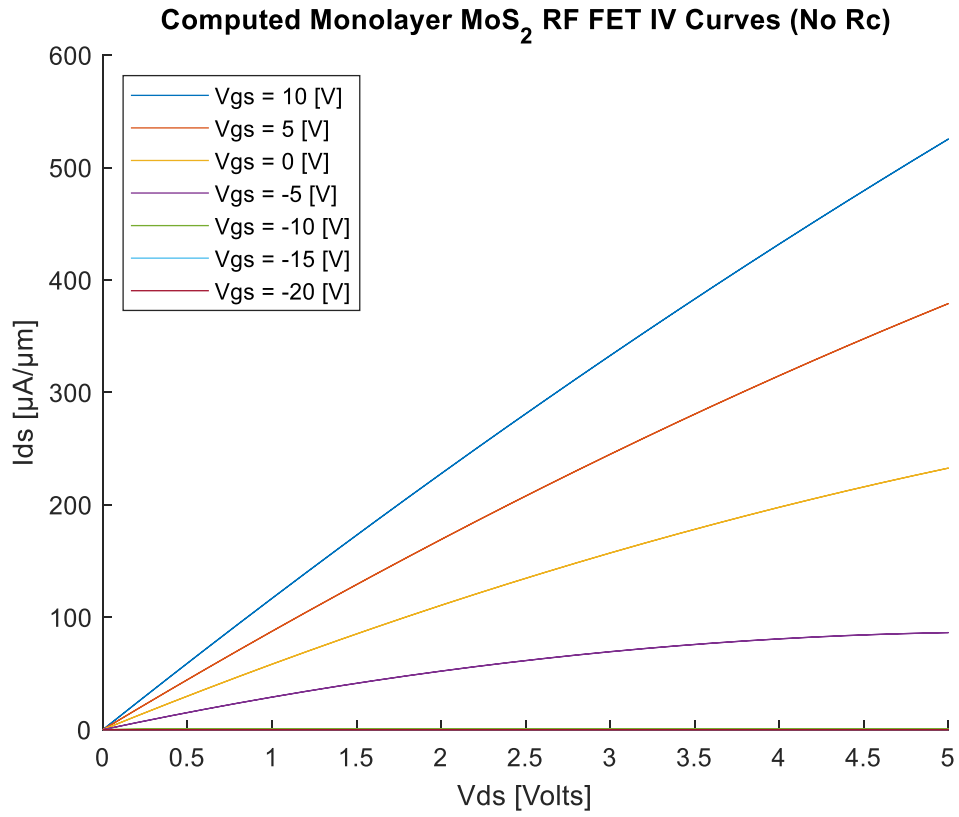
### 3.3.4 FET Model Inaccuracies at High Gate and Drain Fields

After extracting values for electron mobility, contact resistance, and threshold voltage from the low  $V_{DS}$  region of operation, we applied these parameters to the whole range of  $V_{GS}$  and  $V_{DS}$  to determine the accuracy of the simple transistor equations and where the model breaks down.

Looking at the experimental  $I_{DS}$ - $V_{DS}$  data (Fig. 23), and knowing that the threshold voltage is  $-10.45$  V, clearly the device does not follow the transistor equations at high gate biases. Since  $V_{DD}$  is 5 V and the threshold voltage is  $-10.45$  V, the device should be in the linear regime for  $V_{GS} > 0$  V as the saturation condition would not be reached. Additionally, the spacing between the lines at  $V_{DS} = 5$  V should be linear between the gate voltages; however, the spacing clearly is sublinear.

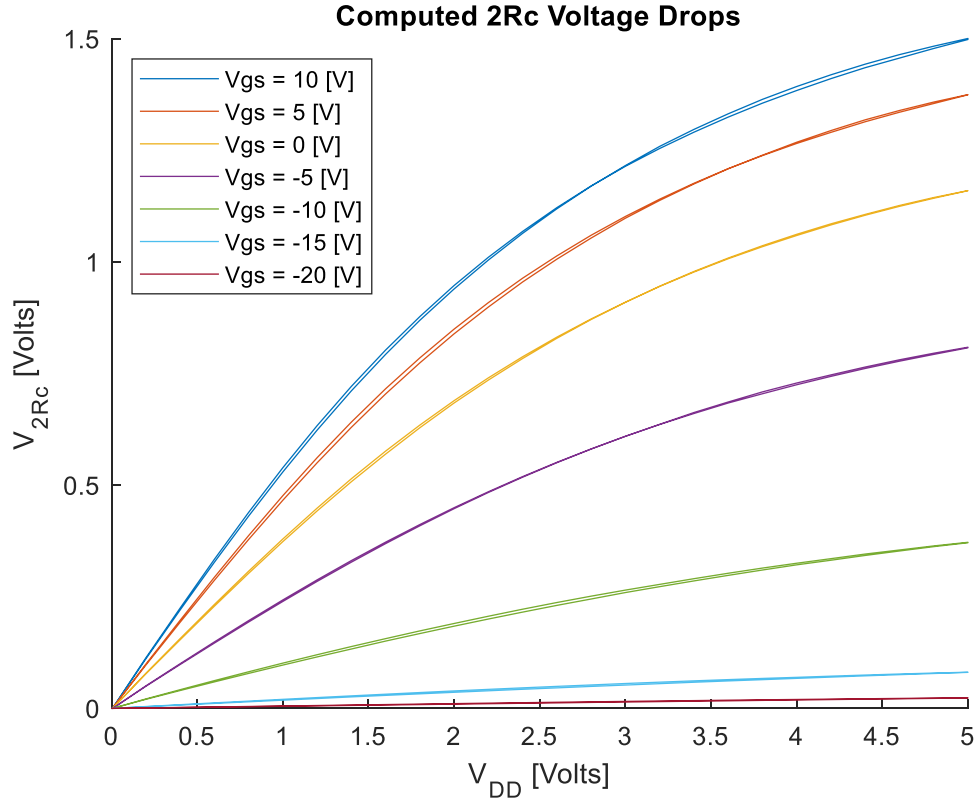
We know that the contact resistance plays an important role in the device performance and that a significant portion of the applied potential drops across the contact resistance instead of the channel. Therefore, the first goal is to determine how the contact affects the  $I_{DS}$ - $V_{DS}$  curves.

We first compute and plot the entire range of  $I_{DS}-V_{DS}$  curves using the extracted parameters and not including contact resistance (Fig. 30).



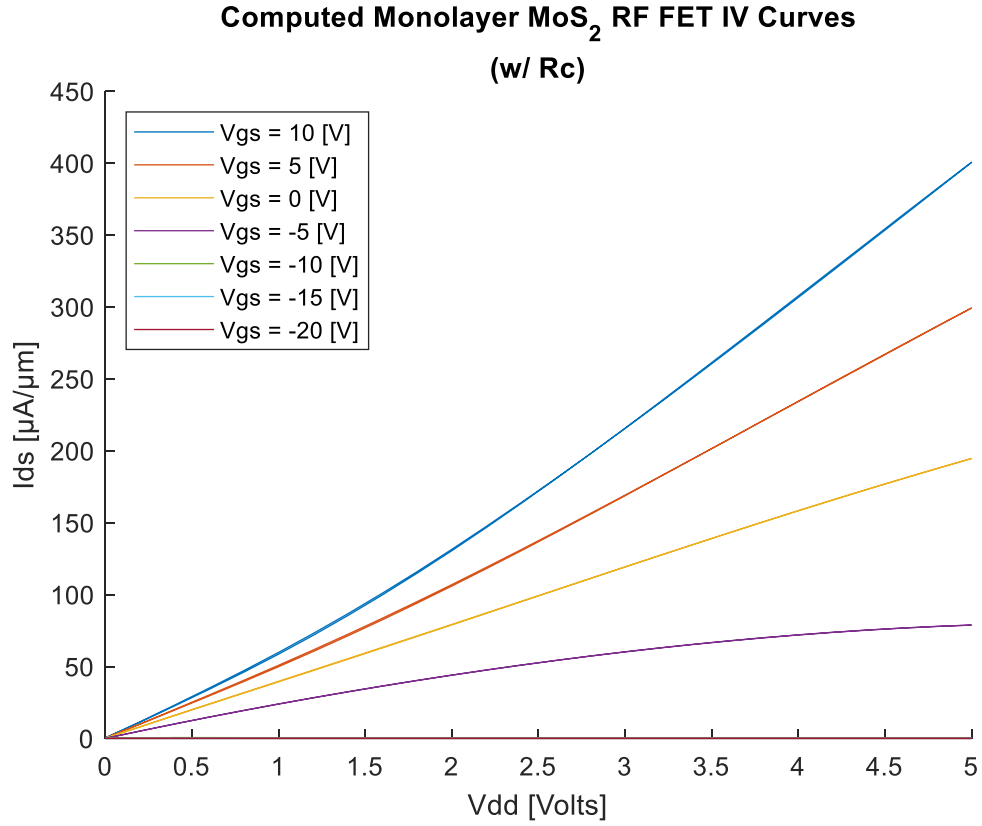
**Fig. 30**  $I_{DS}-V_{DS}$  curves plotted using extracted values X2 and X3

Next, as before, the voltage drop across the contact resistance is calculated as  $I_{DS}2R_C$  (Fig. 31).



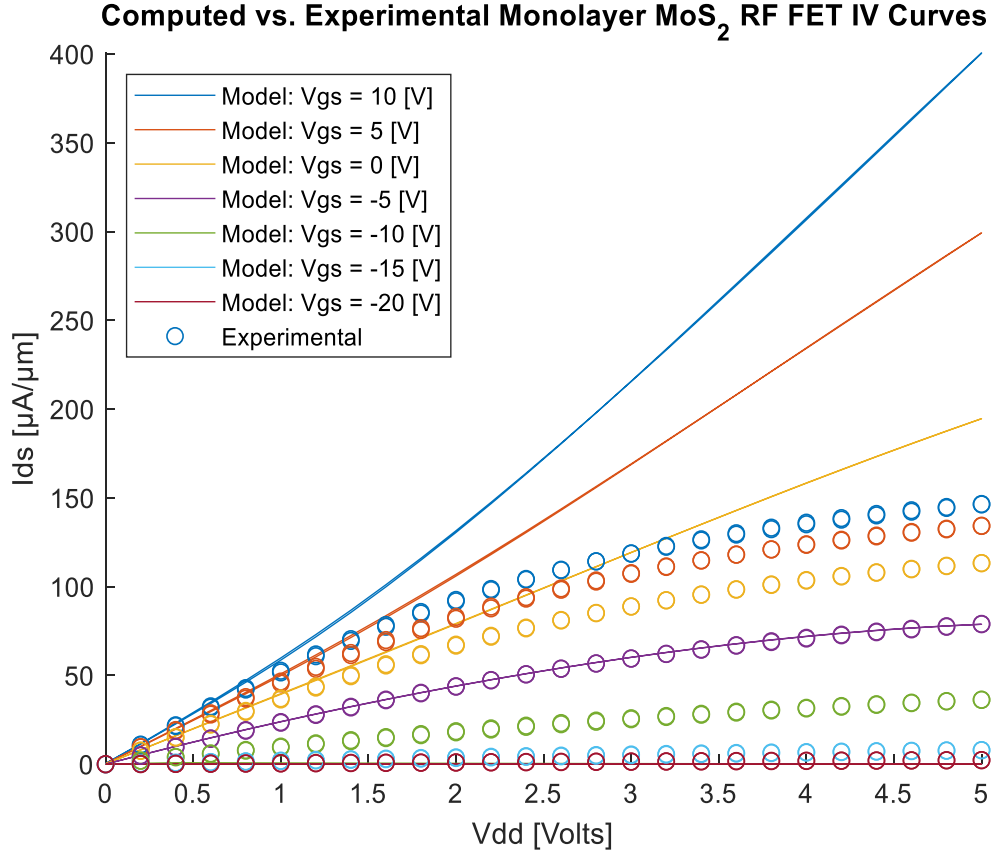
**Fig. 31** Calculated voltage drops due to contact resistance, X1. The specific contact resistance of this device was  $2.56 \text{ k}\Omega\cdot\mu\text{m}$ .

Next, we include the impact of contact resistance by updating the  $V_{DS}$  term and plotting against  $V_{DD}$  instead (Fig. 32).



**Fig. 32**  $I_{DS}$ - $V_{DD}$  curves plotted using extracted values X1, X2, and X3

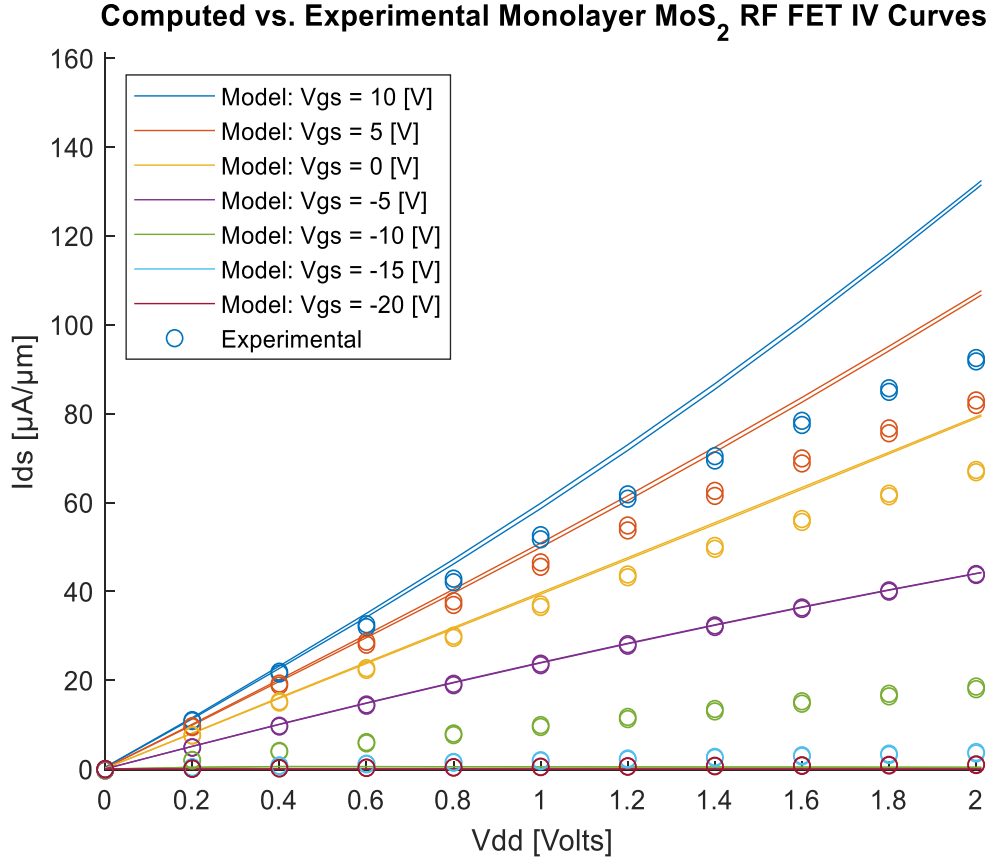
Next, the computed  $I_{DS}$ - $V_{DD}$  curves are plotted alongside the experimental  $I_{DS}$ - $V_{DD}$  curves to determine where the model is no longer accurate (Fig. 33).



**Fig. 33** Experimental results vs. computed  $I_{DS}$ - $V_{DD}$  curves plotted using extracted values X1, X2, and X3

It is worth noting that for smaller gate overdrives ( $V_{GS} = -5$  V), the transistor equations describe the experimental data well after including contact resistance. However, clearly incorporating the impact of contact resistance alone does not accurately recreate the experimental device performance in the regions where there is both a high gate and drain bias. Other groups have noticed this behavior as well, and often attribute it to “velocity saturation”. In the work by Smithe et al., they determine that significant heating occurs at high drain and gate biases.<sup>25</sup>

Zooming in to look at the low drain-bias region ( $V_{DD} < 2$  V), we can see the model is indeed more accurate at lower biasing (Fig. 34).



**Fig. 34** Experimental results vs. computed  $I_{DS}$ - $V_{DD}$  curves plotted using extracted values X1, X2, and X3. Subthreshold current modeling was ignored for simplicity; this explains the low current computed for  $V_{GS} < -10$  V.

## 4. Conclusions

RF FETs using ARL-grown, monolayer MoS<sub>2</sub> as the semiconducting channel were fabricated and tested in the GSG configuration. Devices were fabricated and characterized on both hard (SiO<sub>2</sub>) and flexible (polyimide) substrates. Devices operated with de-embedded  $f_T$  and  $f_{max}$  over 3 GHz on rigid substrates and 1 GHz on flexible substrates. The performance of the devices was compared to other monolayer MoS<sub>2</sub> RF FET performance published in literature<sup>13,14</sup> and to the theoretical maximum performance of phonon-limited transport.<sup>15,16,24</sup> Standard MOSFET current-voltage equations were applied to experimental results of ARL-fabricated RF transistors. A method to accurately extract the key device parameters of threshold voltage, contact resistance, and transconductance was introduced and discussed. The experimental transistor current-voltage curves deviate from the transistor models in regions of operation with both a high gate and drain bias. According to related literature,<sup>25</sup> device self-heating occurs at these operation regimes causing significant velocity saturation and mobility degradation.

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## List of Symbols, Abbreviations, and Acronyms

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|                                |                                                   |
|--------------------------------|---------------------------------------------------|
| 2-D                            | two-dimensional                                   |
| Ag                             | silver                                            |
| Al                             | aluminum                                          |
| Al <sub>2</sub> O <sub>3</sub> | aluminum oxide                                    |
| ARL                            | Army Research Laboratory                          |
| Au                             | gold                                              |
| CAD                            | computer-aided design                             |
| CF <sub>4</sub>                | tetrafluoromethane                                |
| Cl <sub>2</sub>                | chlorine gas                                      |
| CVD                            | chemical vapor deposition                         |
| DC                             | direct current                                    |
| DEVCOM                         | US Army Combat Capabilities Development Command   |
| DI                             | deionized                                         |
| EBL                            | electron beam lithography                         |
| FET                            | field-effect transistor                           |
| GSG                            | ground-signal-ground                              |
| I <sub>DS</sub>                | drain-source current                              |
| I-V                            | current-voltage                                   |
| IPA                            | isopropyl alcohol (isopropanol)                   |
| KOH                            | potassium hydroxide                               |
| MIBK                           | methyl isobutyl ketone                            |
| MoO <sub>3</sub>               | molybdenum trioxide                               |
| MoS <sub>2</sub>               | molybdenum disulfide                              |
| MOSFET                         | metal–oxide–semiconductor field-effect transistor |
| N <sub>2</sub>                 | nitrogen                                          |
| Ni                             | nickel                                            |

|                  |                                                         |
|------------------|---------------------------------------------------------|
| O <sub>2</sub>   | oxygen                                                  |
| PEALD            | plasma-enhanced atomic layer deposition                 |
| PEDOT:PSS        | poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) |
| PMMA             | polymethyl methacrylate                                 |
| RF               | radio frequency                                         |
| RIE              | reactive ion etching                                    |
| rpm              | revolutions per minute                                  |
| Si               | silicon                                                 |
| SiO <sub>2</sub> | silicon dioxide                                         |
| Ti               | titanium                                                |
| TMA              | trimethylaluminum                                       |
| V                | volts                                                   |
| V <sub>DS</sub>  | drain-source voltage                                    |
| V <sub>GS</sub>  | gate-source voltage                                     |

1 DEFENSE TECHNICAL  
(PDF) INFORMATION CTR  
DTIC OCA

1 DEVCOM ARL  
(PDF) FCDD RLD DCI  
TECH LIB

11 DEVCOM ARL  
(PDF) FCDD RLS G  
R BURKE  
FCDD RLS EE  
M CHIN  
M DUBEY  
S NAJMAEI  
FCDD RLS EM  
J PULSKAMP  
A MAZZONI  
C MORRIS  
FCDD RLS ER  
K KINGKEO  
P SHAH  
G BIRDWELL  
T IVANOV