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Gallium Nitride (GaN) RF Challenge: Broadband Power Amplifiers in BAE 0.18-µm GaN Technology

by John E Penn

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Gallium Nitride (GaN) RF Challenge: Broadband Power Amplifiers in BAE 0.18-µm GaN Technology

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14. ABSTRACT

The DOD Gallium Nitride (GaN) RF Challenge is enabling development and fabrication of the best concepts for high-performance efficient broadband Monolithic Microwave Integrated Circuits related to 5G expansion and critical electronic-warfare needs. The circuits documented in this report represent some of the US Army Combat Capabilities Development Command Army Research Laboratory's designs as part of the DOD Design Team for BAE Systems' 0.18-µm GaN multiproject wafer fabrication. When these fabricated designs are returned in 2021, they will be tested, evaluated, and documented in future technical reports.

15. SUBJECT TERMS

MMIC, monolithic microwave integrated circuit, RF, microwave, GaN, gallium nitride, power

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Acknowledgments

I would like to acknowledge and thank the US Army Combat Capabilities Development Command Army Research Laboratory team. These designs were a joint effort of Dr Ali Darwish, Sami Hawasli, and Khamsouk Kingkeo—who will be heavily involved in testing the designs when they come back from fabrication. Thanks to the Gallium Nitride (GaN) RF Challenge team and coordinators, especially to Dave Via of the US Air Force Research Laboratory and Dave Brown and Ed Gacek of BAE Systems, who helped us get the designs submitted and helped with many technical questions.

1. Introduction

With the emergence of 5G wireless networks, DOD systems will have to operate in a crowded and contested environment. The DOD Gallium Nitride (GaN) RF Challenge is enabling development and fabrication of the best competed concepts for high-performance efficient broadband monolithic microwave integrated circuits (MMICs) related to the 5G expansion and critical electronic-warfare (EW) needs. Two different gallium nitride (GaN) foundries, BAE Systems and Qorvo, will fabricate the many competed circuit ideas as part of this effort. The circuits documented in the following sections are part of the DOD Design Teams' fabrication space on the BAE 0.18-µm GaN multiproject wafer fabrication. The US Army Combat Capabilities Development Command Army Research Laboratory was also part of the DOD Design Teams for the Qorvo 0.15-µm GaN multiproject wafer fabrication, and those designs are documented in other technical reports.

2. Design Submissions in BAE 0.18-µm GaN

The DEVCOM Army Research Laboratory design team of Ali Darwish, Sami Hawasli, and John Penn proposed an extremely broadband transmitter architecture that won acceptance for the GAN RF Challenge. Dr Darwish conceived the idea and Hawasli spearheaded the proposal, as well as the overall transmitter design. ARL was allowed two die sites of 9- × 6-mm size. The large die size allowed for a number of parallel subcircuit designs and demonstrations of a number of other design concepts. Figure 1 shows the layout of CHIP1, which includes a number of designs from Penn that will be documented in this technical report. A number of designs in CHIP1 are subcircuits from the full transmitter design by Hawasli in CHIP2. It will be easier to test and verify the subcircuits in parallel before testing the complex, full transmitter architecture. Figure 2 shows the layout of CHIP2, the full broadband transmitter design, which will be documented in other reports. Note that there are a few subcircuits and test high electron mobility transistors (HEMTs) included in available space in CHIP2, and one can see some of the subcircuits designed by Hawasli that are probe testable as individual circuits in CHIP1. Both die layouts (CHIP1 and CHIP2) will be fabricated and tested as part of a multiproject, BAE 0.18-µm GaN prototype wafer fabrication. When the designs are returned sometime in 2021, they will be tested, evaluated, and documented.

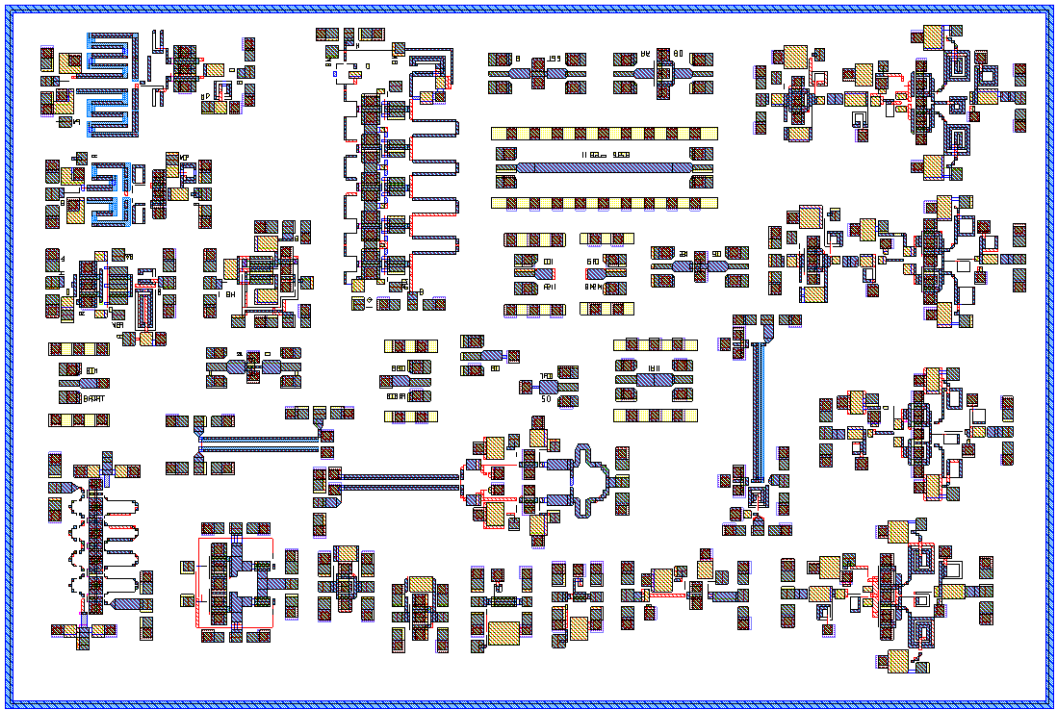

Fig. 1 Layout of CHIP1's 9- × 6-mm die (various circuits and test structures)

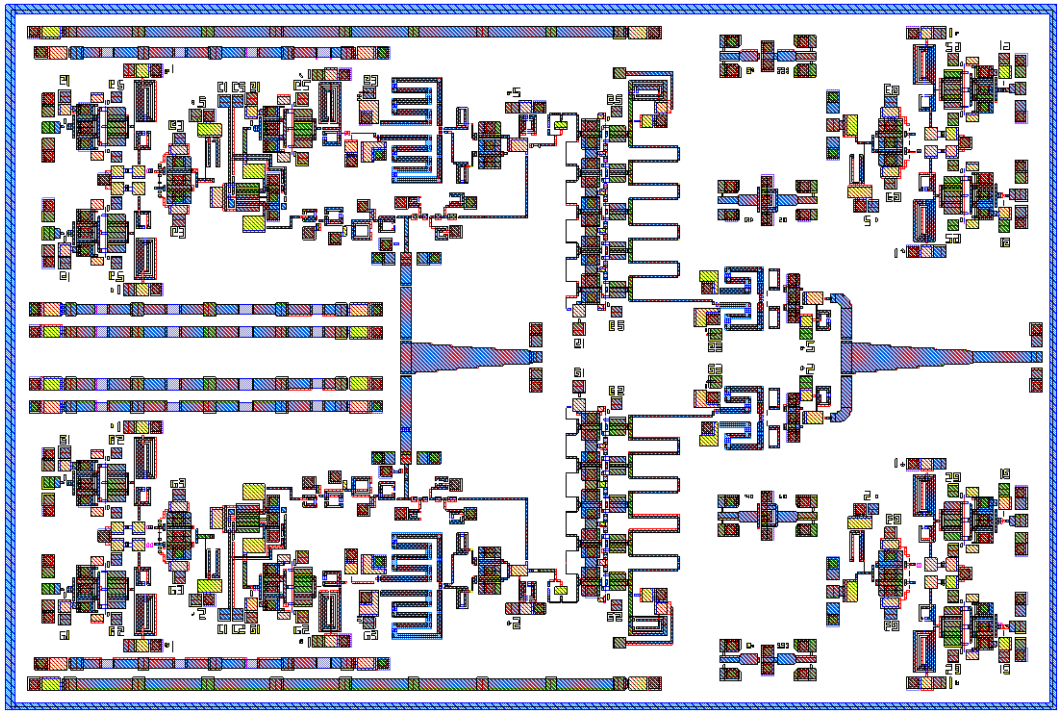

Fig. 2 Layout of CHIP2's 9- × 6-mm die (extremely broadband transmitter)

3. Broadband Distributed Amplifier Design

Broadband amplifiers were needed for the novel transmitter architecture. Distributed amplifiers can achieve decades of bandwidth, so they were explored initially to determine what could be achieved using the BAE process. The basic concept of the distributed amplifier, or traveling wave amplifier, is the input RF signal propagates down a transmission line to a series of amplifiers that have a small amount of gain, but with very broadband gain. Each stage's output then propagates down a transmission line to an output that adds up the gain contributions of multiple broadband gain elements. Figure 3 shows a schematic of an ideal lossless distributed amplifier using five HEMTs, or five stages. Tradeoffs among bandwidth, gain, stability, noise figure, return loss, and DC power consumption can be made early in the design process before committing to a layout and performing design rule checks (DRCs) and other time-consuming tasks of design and verification. Lossless ideal elements are converted to lossy MMIC elements, and the physical design matches the ideal design as much as is feasible. Linear and nonlinear simulations are performed as well as Axiem electromagnetic simulations of the physical layout after correcting all DRC errors. Small signal simulations of the MMIC design versus the ideal design show good gain before rolling off above 30 GHz (see Fig. 4). A picture of the final layout of the distributed amplifier is shown in Fig. 5. DC bias can be supplied at the input (gate) and output (drain) using external bias tees. It should operate well over a range of DC biases, depending on the application requirements for DC power consumption, noise figure, RF output power, or dynamic range.

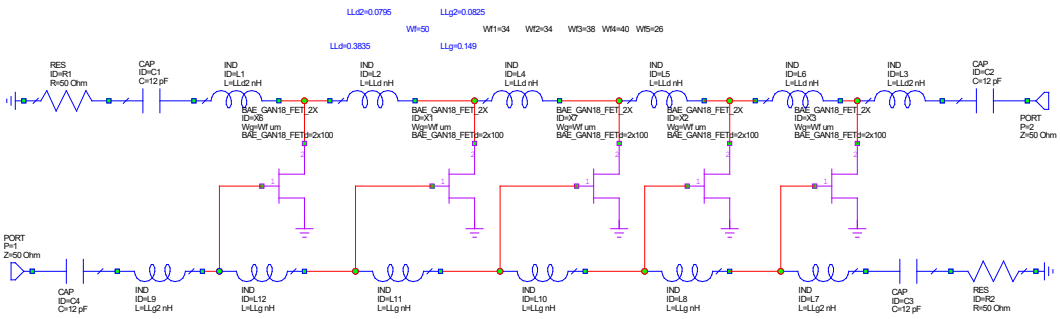

Fig. 3 Schematic of ideal lossless distributed amplifier with five stages (HEMTs)

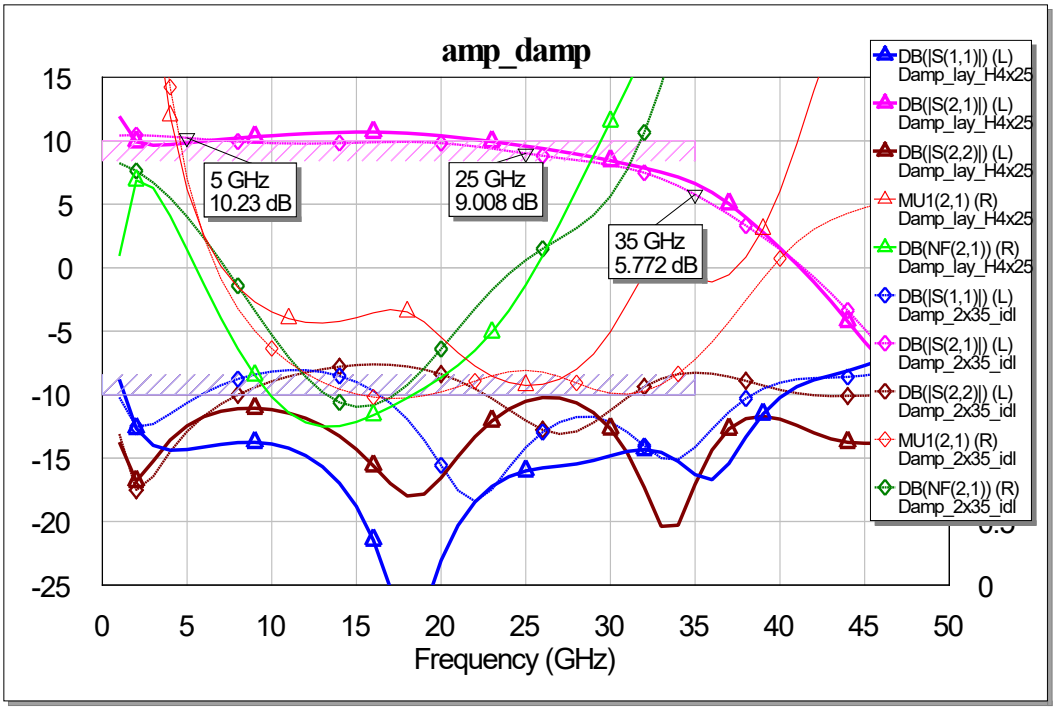

Fig. 4 S-parameter simulation of ideal (dash) vs. MMIC (solid) distributed amplifier

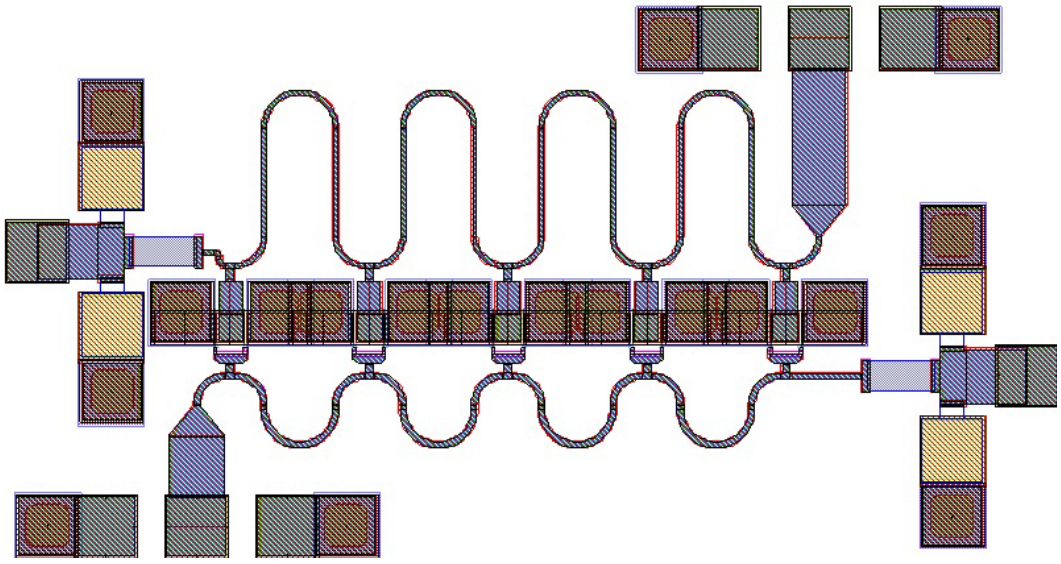

Fig. 5 Final layout of MMIC (solid) distributed amplifier (input gate, bottom left; output drain, upper right)

4. Compact Broadband Amplifier Designs

Another approach to broadband amplifier designs that can be extremely compact uses feedback. A simple resistive feedback design was initially designed using various size HEMTs in the BAE library. Figure 6 shows a schematic of a 4- × 75-µm HEMT broadband amplifier, with its DRC clean layout shown in Fig. 7. There was a problem with the initial process design kit (PDK) for HEMTs with gate finger lengths less than 100 µm, which was fixed over a couple of updates to the BAE PDK. There were still some issues after each update, but this is not unusual for an early version of a PDK that is being released to external customers/designers for the first time.

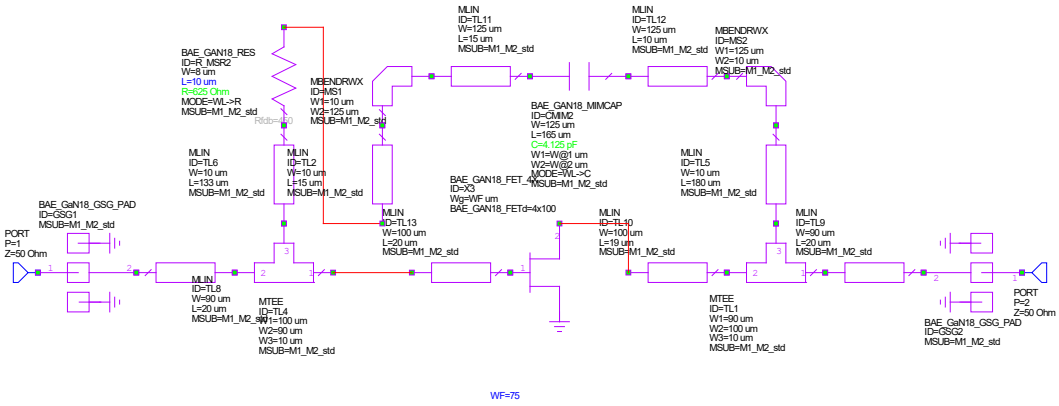

Fig. 6 Schematic of MMIC broadband 4- × 75-µm feedback amplifier

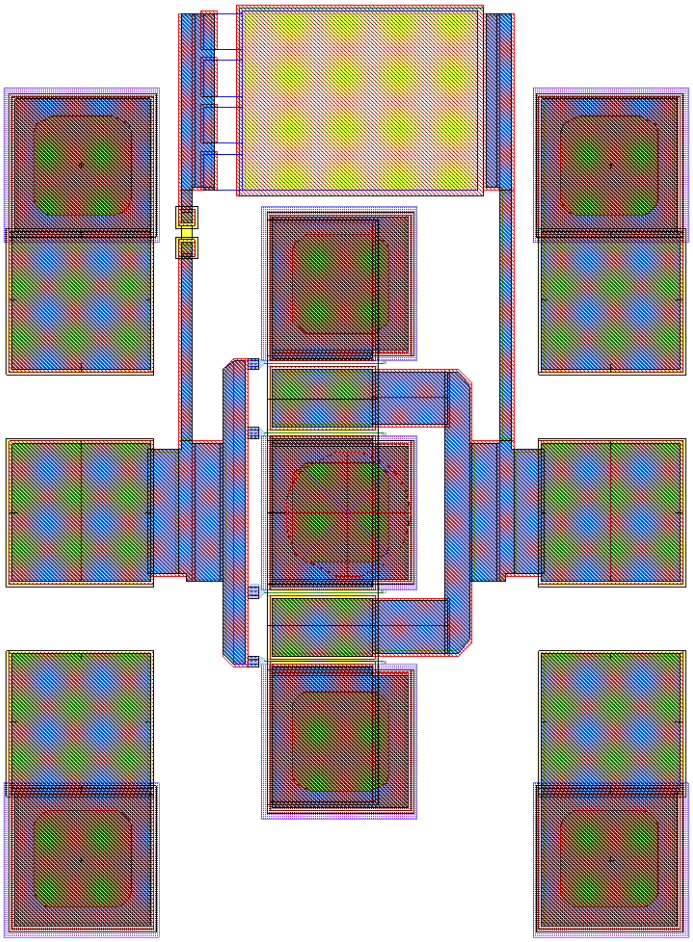

Fig. 7 Compact layout of MMIC broadband 4- × 75-µm feedback amplifier

Broadband s-parameter performance for the amplifier is shown in the s-parameter simulation of Fig. 8. Gain, stability, and return loss are mostly dominated by the HEMT characteristics and device size and by the feedback resistor value. The capacitor in the feedback needs to DC-block the drain and gate voltages and be large enough to pass the RF-resistive feedback of the amplifier. Another version of a DRC-correct layout of a 4- × 120-µm broadband amplifier is shown in Fig. 9. Note the longer gate fingers, though otherwise it looks very similar to the 4- × 75-µm compact design. An s-parameter simulation of the 4- × 120-µm broadband amplifier versus the 4- × 75-µm design (Fig. 10) shows higher gain at lower frequencies, but then rolls off more quickly than the smaller HEMT design.

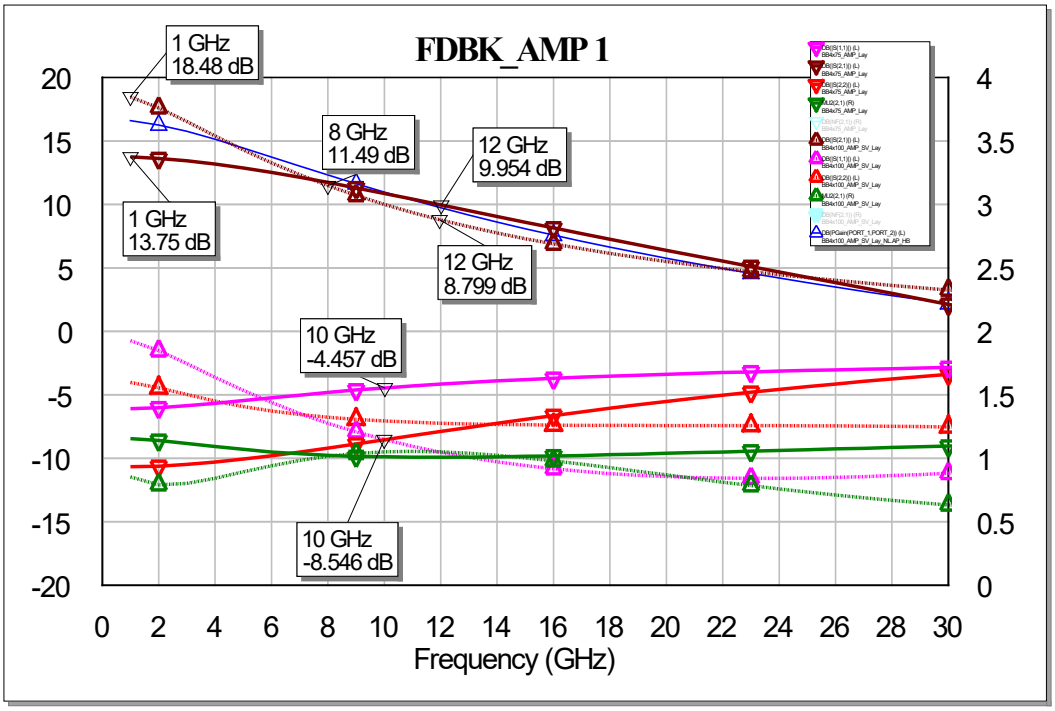

Fig. 8 S-parameters of MMIC broadband 4- × 75-µm (solid) and 4- × 100-µm (dot–dash) feedback amplifiers

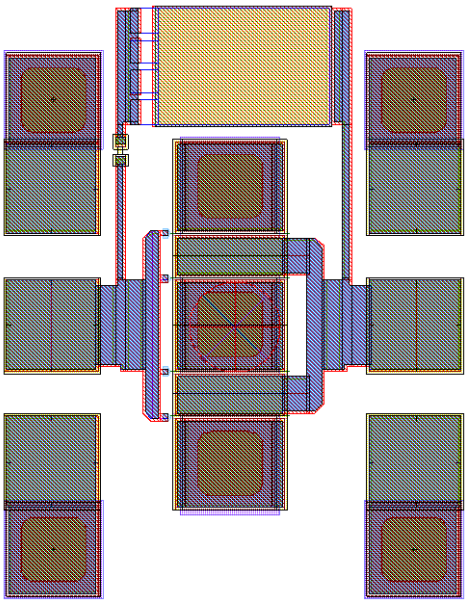

Fig. 9 Compact layout of MMIC broadband 4- × 120-µm feedback amplifier

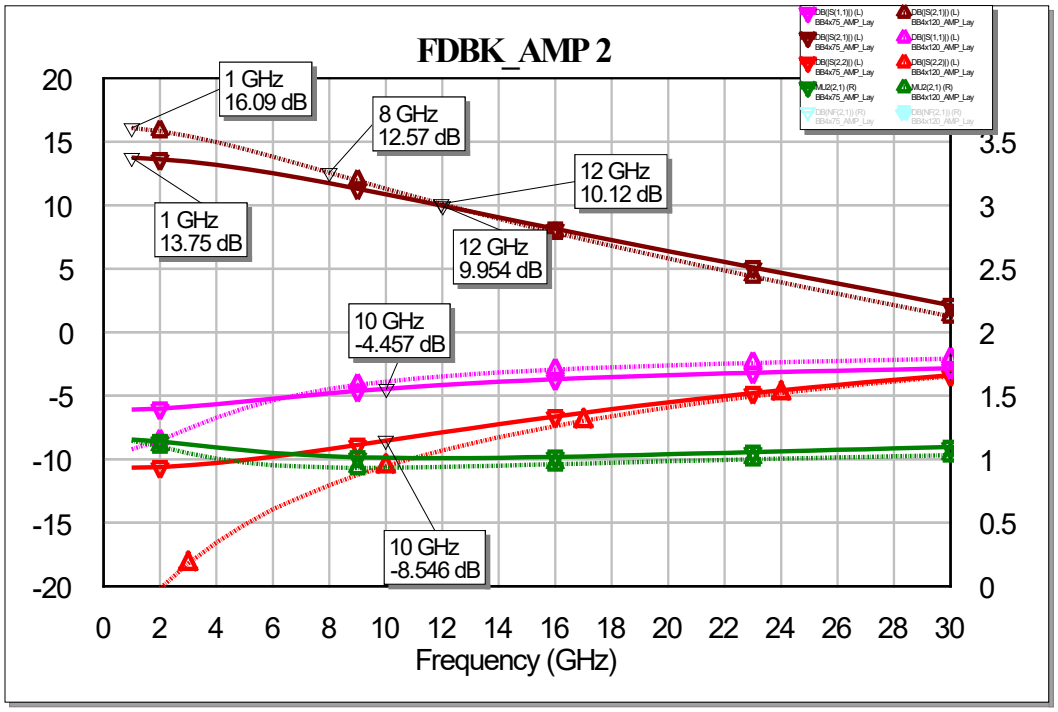

Fig. 10 S-parameters of MMIC broadband 4- × 75-µm (solid) and 4- × 120-µm (dot–dash) feedback amplifiers

Another approach to a broadband feedback amplifier is to use source-inductive feedback. This technique often works well in low noise amplifiers (LNA) with the tradeoff between good noise figure and return loss. There were limitations in using source inductance with the first PDK, as there were no models with "open" sources. The only available HEMTs had grounded sources for both the models and layouts. This first PDK library had both nonlinear and linear HEMT models but were only available in 2- and 4-finger layouts with grounded sources. Another unusual feature of this PDK is that you could not do a linear simulation with a DC-biased nonlinear model, unlike other foundry PDKs. There were built-in restrictions to the types of simulations one could perform with the nonlinear model. In an updated PDK, open-source HEMT models were supplied but without layouts for open-source HEMTs. The open-source HEMT layouts had to be created by the designers, starting from the provided grounded-source layouts. These HEMTs were unusual in that there were no air-bridge connections across alternating source regions. This required additional layout modifications to ensure the multiple source regions were connected. Normally, the alternating source regions are connected by two to three substrate vias for the grounded HEMT layouts. In the following open-source feedback amplifiers, the initial 4-finger HEMT designs were converted to 2-finger HEMTs with double the gate finger length to minimize the number of source connections.

The source inductance is modeled as a single length of microstrip line, which is then replaced with an equivalent rectangular-length spiral inductor that compacts the layout while maintaining the desired source inductance. Linear models in Microwave Office (a CAD tool) allow modification, or access, to the ground reference, but not the nonlinear models. This required an updated PDK with open-source models for nonlinear simulations of these feedback amplifiers.

Figure 11 shows the preliminary layout of a 4- × 50-µm broadband amplifier (left side), which initially created many DRC errors due to the 50-µm gate length, then the final DRC-correct amplifier layout was converted to a 2- × 100-µm HEMT (right side) where the vertical "red" metal-trace underpass connects the two sources, and the horizontal metal trace is an overpass to the drain connection. It would be convenient to have air-bridge connections for the alternating source regions of the HEMT, as in most MMIC processes, but there may be some processing and/or performance tradeoffs for not having air bridges in the BAE process. Broadband performance for the source-feedback amplifier is shown in the s-parameter simulation of Fig. 12. Note the broadband gain with decreasing gain slope. It may look similar to the earlier resistive-feedback amplifier because of this broadband decreasing gain, but note the significantly different return loss. With resistive feedback, the return loss tends to be better at lower frequencies; with source feedback, return loss may be better at higher frequencies.

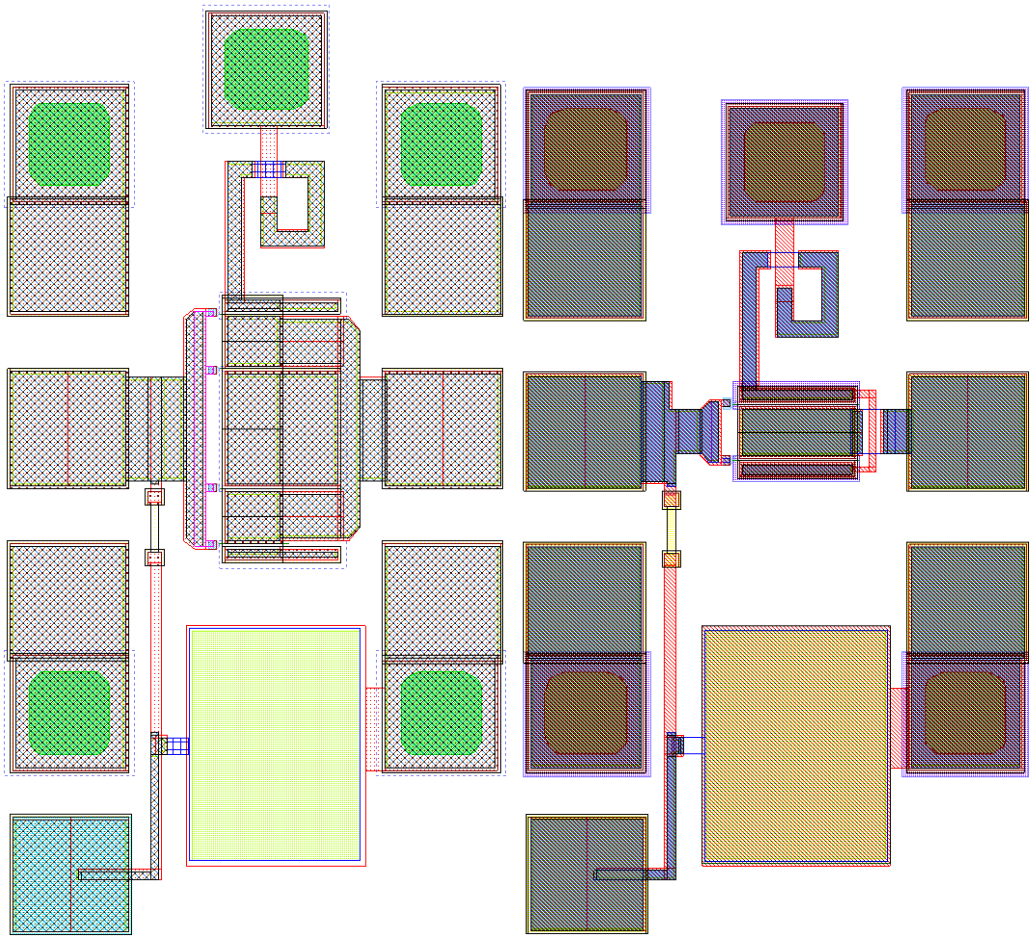

Fig. 11 Preliminary layout (left) for 4- × 50-µm amp and final DRC clean layout (right) of 2- × 100-µm amp

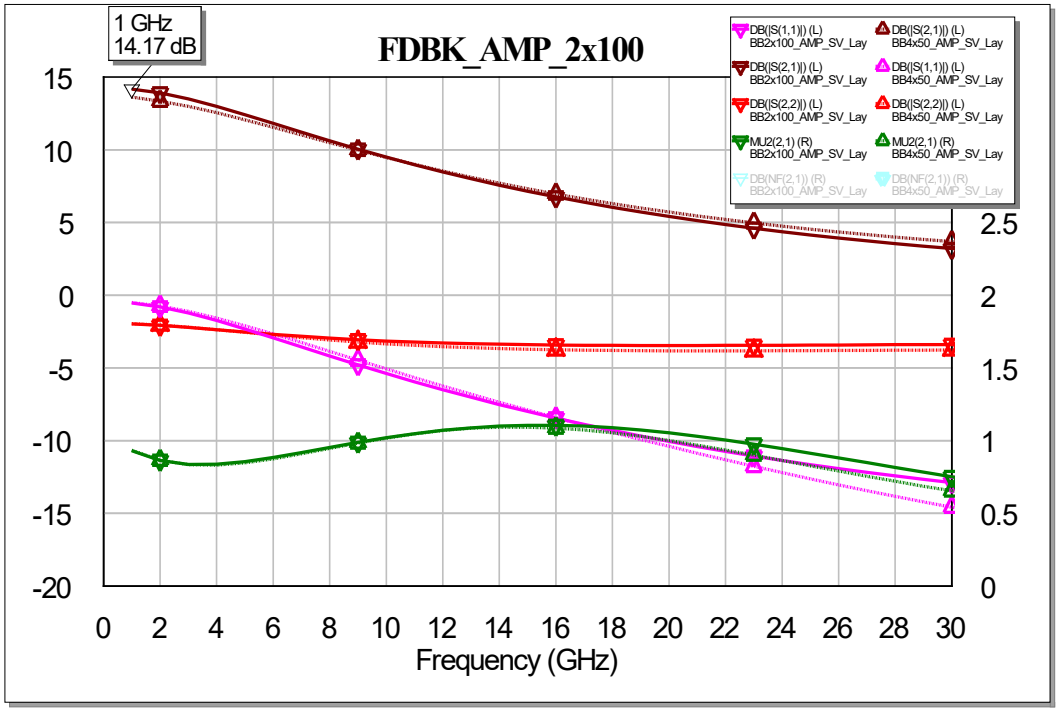

Fig. 12 S-parameters of MMIC broadband 4- × 50-µm (dot-dash) and 2- × 100-µm (solid) source feedback amps

Another source-feedback amplifier was designed, originally using a 4- × 100-µm HEMT that was changed to a 2 × 200 HEMT to make the layout simpler—using overpass and underpass metals for source and drain connections. Figure 13 shows the final DRC-correct layout for the 2- × 200-µm amplifier. Broadband performance for the 2- × 200-µm source-feedback amplifier is shown in the s-parameter simulation of Fig. 14. The larger 2 × 200 HEMT amplifier has more gain at lower frequencies (below 9 GHz) and slightly better output return loss (S22) compared with the smaller 2 × 100 HEMT broadband amplifier.

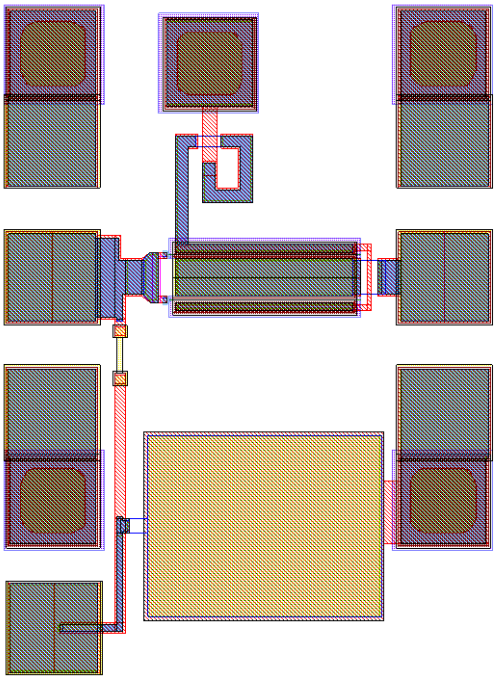

Fig. 13 Layout of MMIC broadband 2- × 200-µm source-feedback amplifier

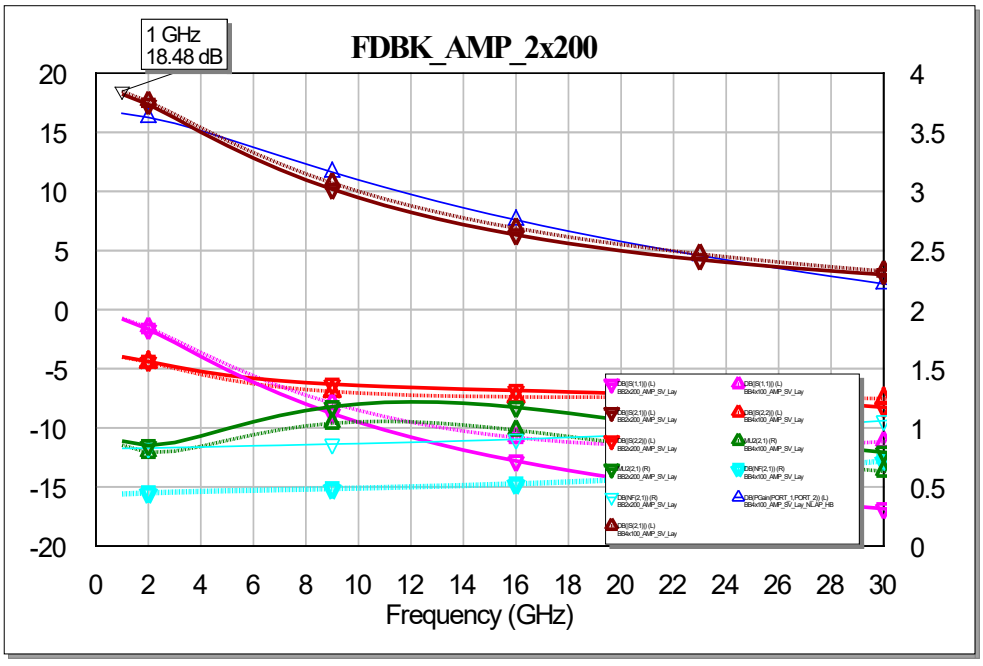

Fig. 14 S-parameters of MMIC broadband 2- × 200-µm source-feedback amplifier

5. Broadband 12–24-GHz 2-W Power Amplifier (PA)

PAs with at least an octave bandwidth were desired, targeting 6–12-GHz and 12–24-GHz operation with 2 W of output power. After estimating that a 0.6-mm

(8- × 75-µm) HEMT would be a good size for 2 W of RF power, load-pull simulations were then run at 10, 20, and 30 GHz. The schematic for the load pull of an 8- × 75-µm HEMT (two parallel 4- × 75-µm HEMTs) is shown in Fig. 15, which results in load-pull contours for peak power and efficiency at 10 and 20 GHz (Figs. 16 and 17). Maximum power-added efficiency (PAE) is an excellent 50% with more than 2 W of output power at 10 GHz, but falls below 2 W with much less PAE at 20 GHz. The HEMT size for the PA was increased about 10% to an 8 × 83 µm to give a margin in achieving 2 W after adding the lossy matching network. This size change scales the ideal resistive load line to a serendipitous 50 ohms at 20 GHz. An equivalent power load is approximately a 50-ohm resistance in parallel with 0.21-pF capacitance.

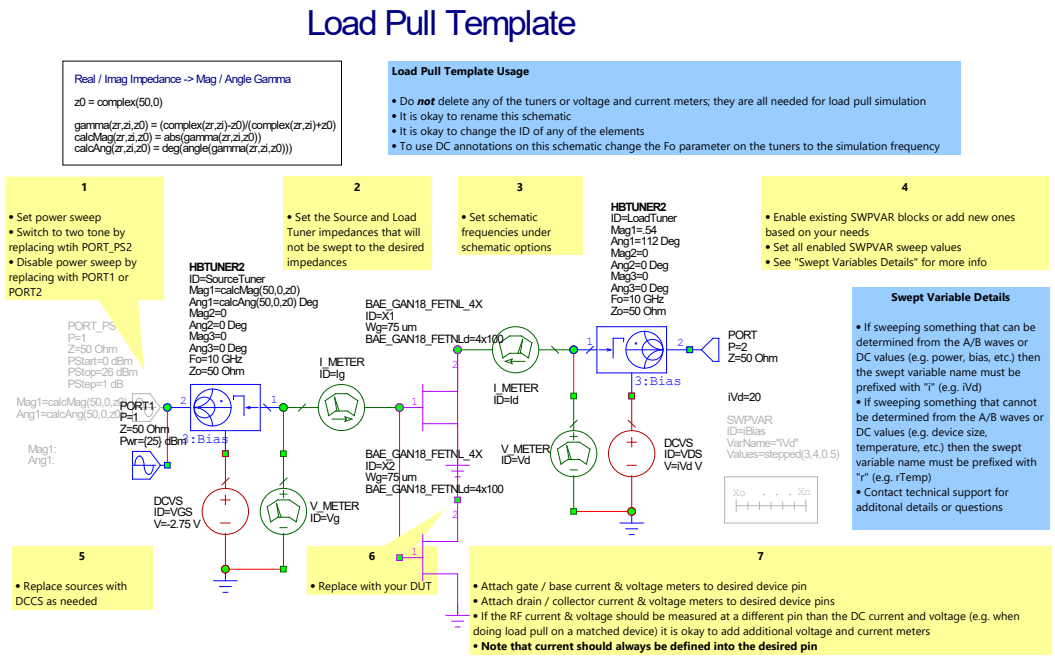

Fig. 15 Load-pull schematic for 8- × 75-µm HEMT (2× the 4 × 75 µm)

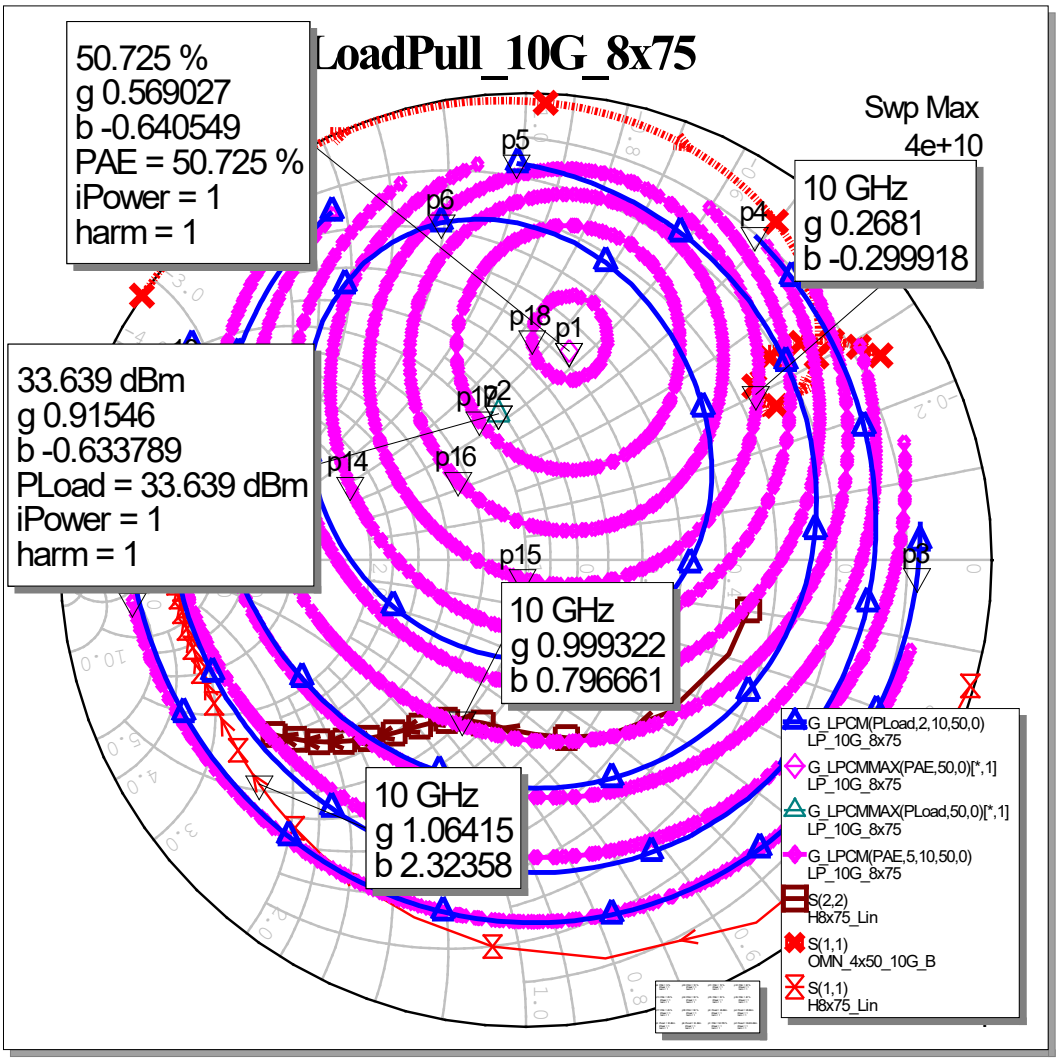

Fig. 16 Load-pull contours for 8- × 75-µm HEMT (10 GHz)

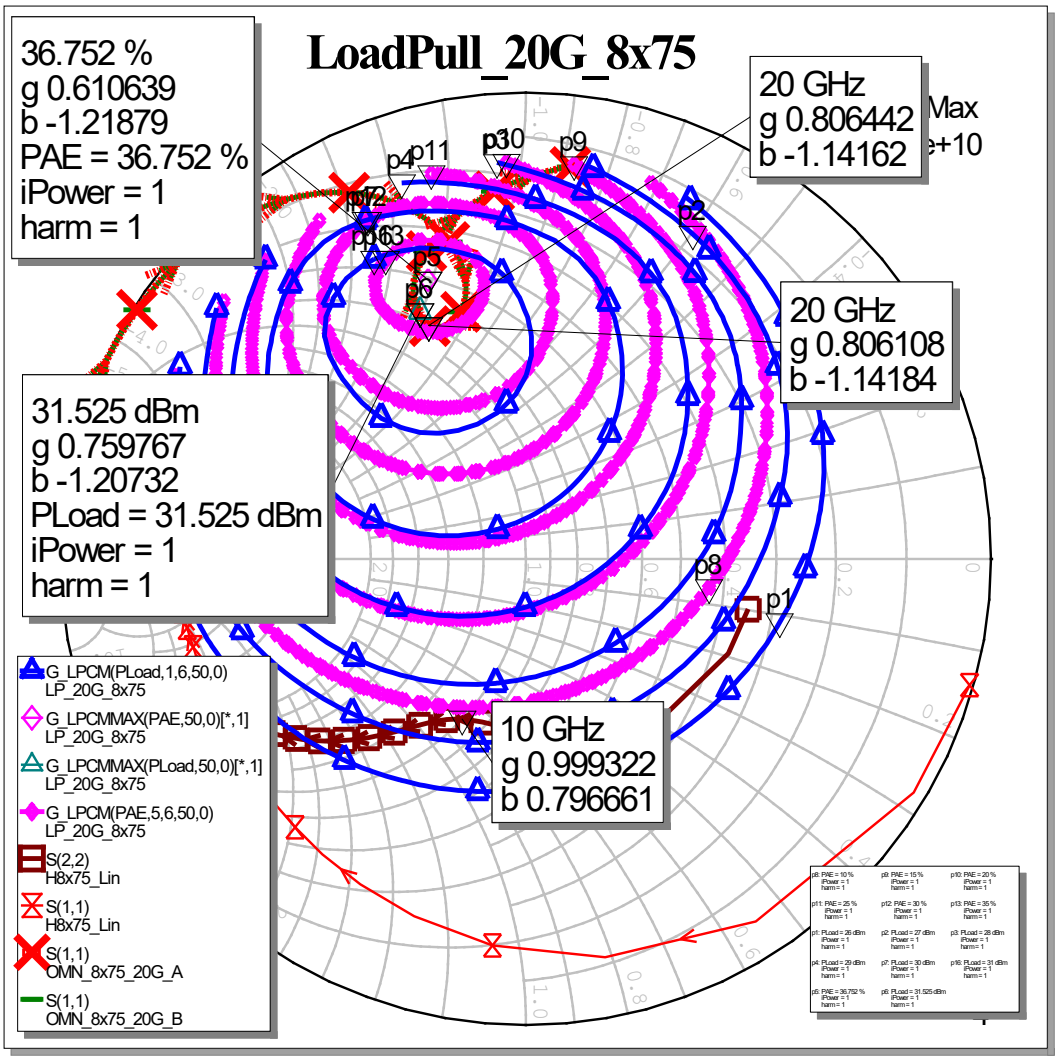

Fig. 17 Load-pull contours for 8- × 75-µm HEMT (20 GHz)

Two simple lossless-output matching circuits were compared, shown in Fig. 18, where the ideal load match is the green trace that touches the narrower band's output match in blue and the alternative wider band's output match in magenta. Note that 17 GHz is the geometric center frequency for the desired 12–24-GHz bandwidth. The physical layout of the output match is created by replacing one ideal element at a time with MMIC elements from the PDK, with retuning at each step. In the MMIC output match design, loss relative to the desired parallel resistor–capacitor (RC) power match is about 1 dB from 10 to 26 GHz, which is shown relative to the lossless ideal match in Fig. 19. A layout of the MMIC output match is shown in Fig. 20. Drain-bias pads need to be added near the shunt capacitor to ground at the top and bottom of the output-match layout. For the input match, the PA is stabilized with a parallel RC intended to help stabilize at lower frequencies where the gain is higher while not reducing gain at higher frequencies where less resistance is required to stabilize the PA.

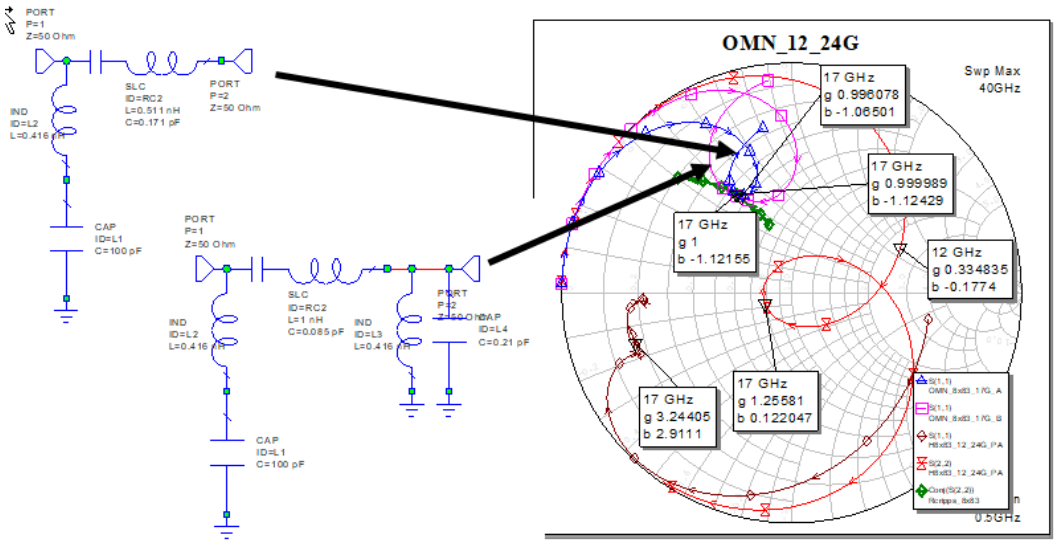

Fig. 18 Ideal lossless-output Matches 1 and 2 for 8- × 83-µm HEMT (17 GHz)

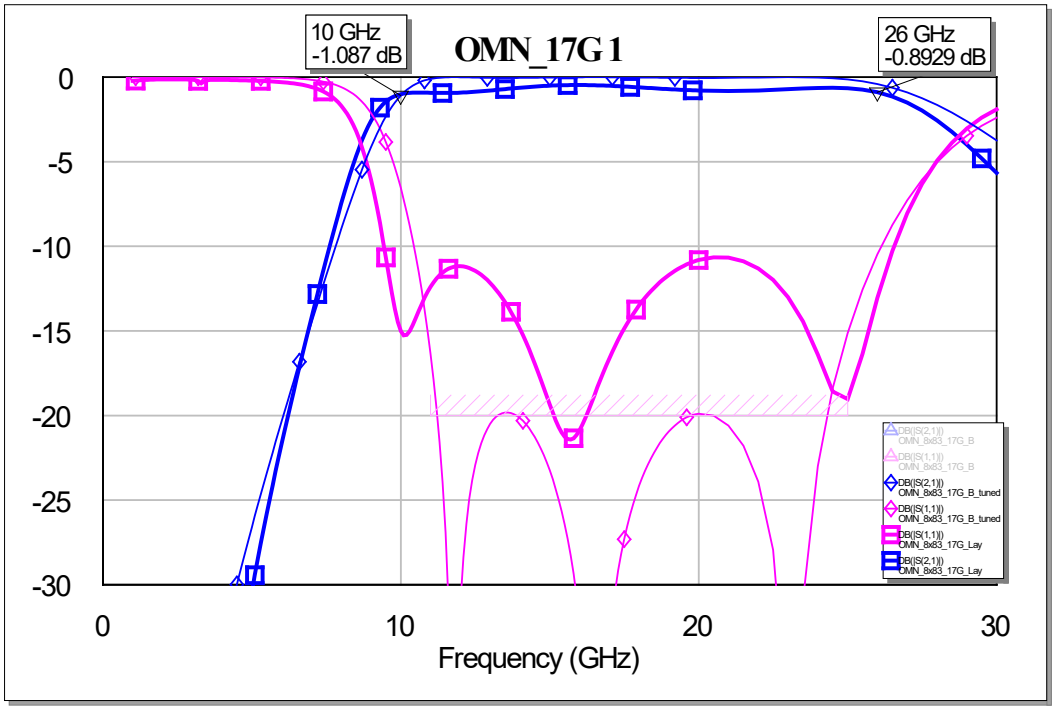

Fig. 19 Lossless-output match (thin) vs. MMIC output-match layout (thick)

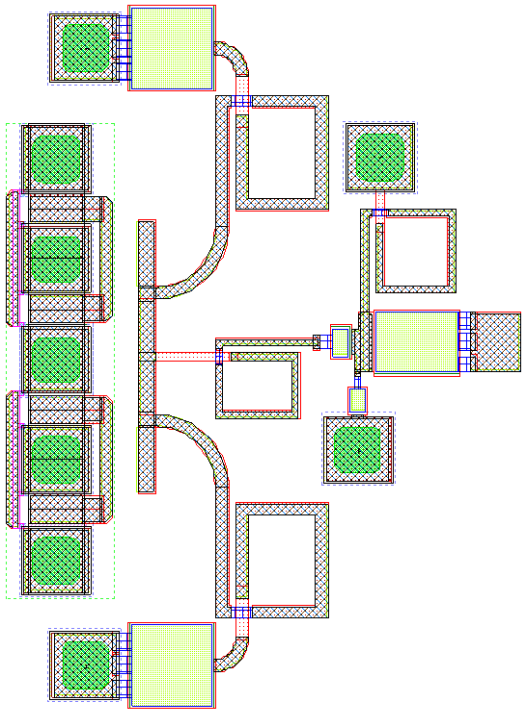

Fig. 20 Preliminary layout of MMIC output match 8 × 83 µm (17 GHz)

Preceding the stabilizing RC, there is a 4-element bandpass match to a 50-ohm input, tuned to maximize gain from about 12 to 24 GHz. A layout of the MMIC

input match is shown in Fig. 21. The small signal gain of the one-stage PA is 11 dB at 12 GHz but drops to 8 dB at 23 GHz, falling sharply before achieving the 24-GHz goal (Fig. 22). A full layout of the one-stage 1–24-GHz PA is shown in Fig. 23, which has a DC pad for gate DC supply voltage (Vgg) at the top left and DC pads for drain DC supply voltage (Vdd) at the top and bottom middle.

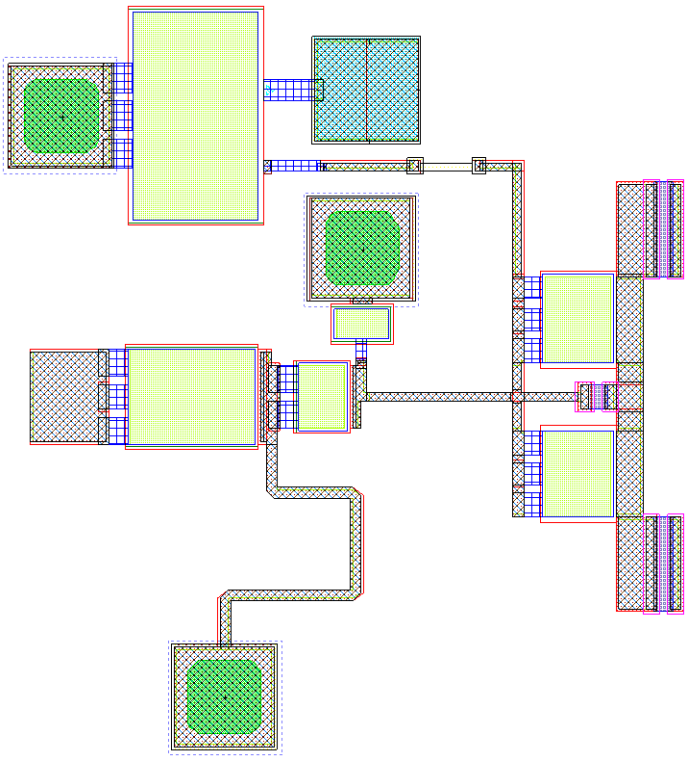

Fig. 21 Layout of MMIC input match 8 × 83 µm (17 GHz)

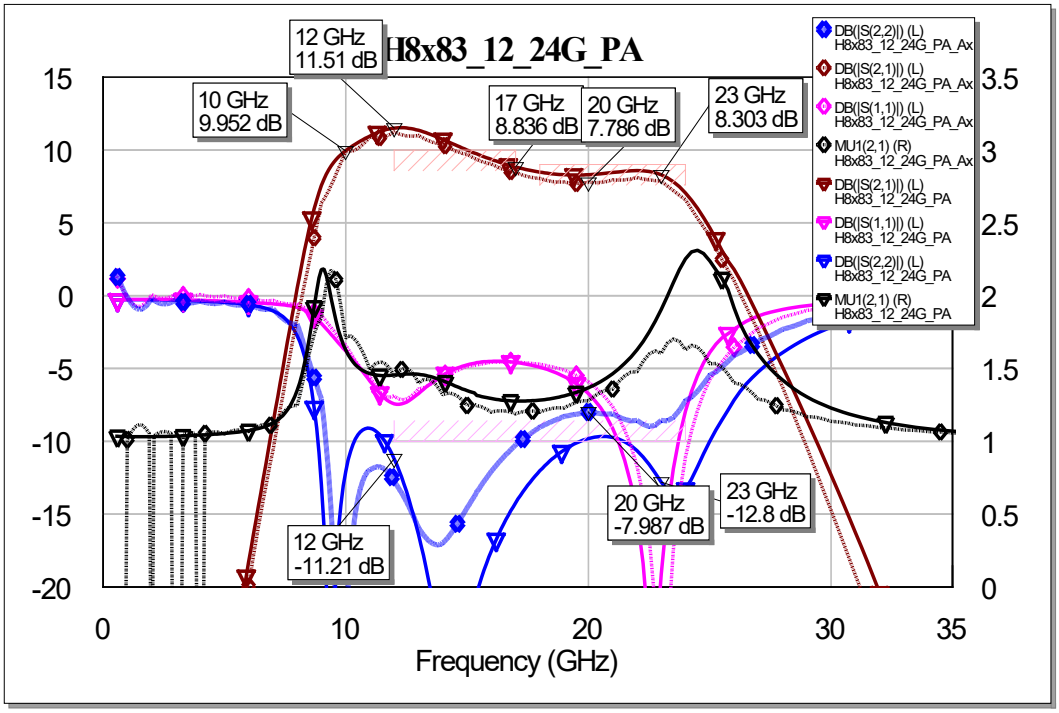

Fig. 22 S-parameter simulation of MMIC 8- × 83-µm 12–24-GHz PA (solid traces)

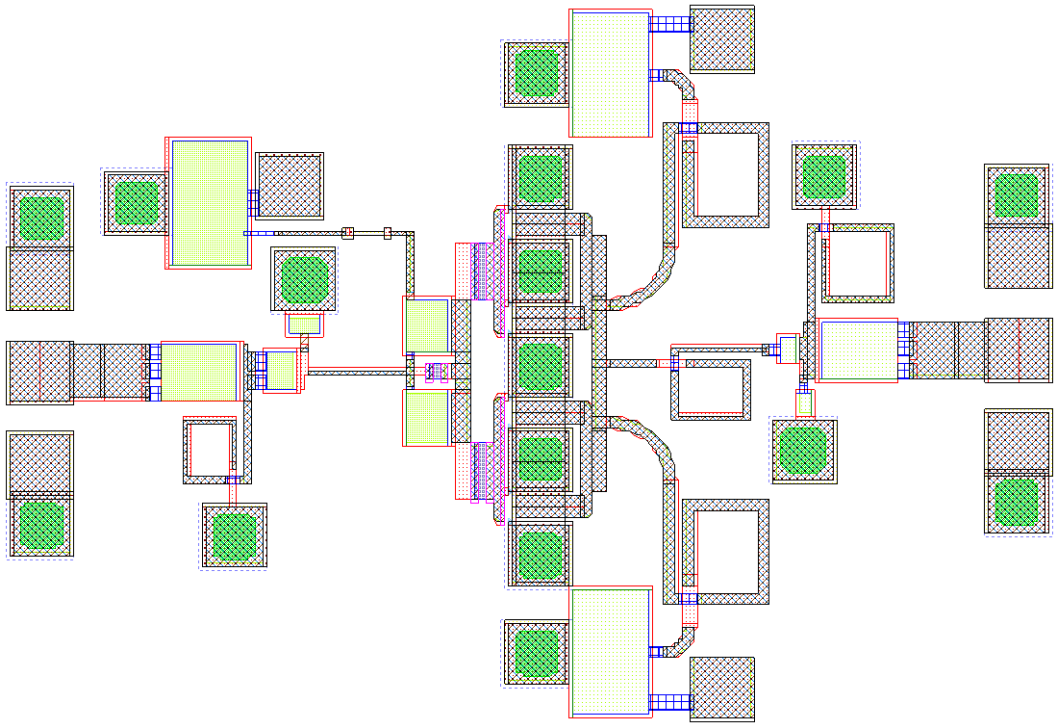

Fig. 23 Layout of one-stage 8- × 83-µm 12–24-GHz PA

Note that the PA load-pull simulations were done at 24 V. There are indications the process can go to 28 V, but the models are fit at 20 V and 24 V, and 24 V seems to be the recommended maximum. Recall that voltage squared is power, so there is a significant power difference between 20 V and 28 V. For now the simulations are done at 20 V, and when the designs are fabricated and tested the performance should be evaluated at 24 V and 28 V as well. Power simulations predict about 2 W of output power (33 dBm) at 20 V from 13 to 23 GHz as shown in Fig. 24. Output power increases to about 2.5 W (34 dBm) at 24 V from 13 to 23 GHz as shown in Fig. 25.

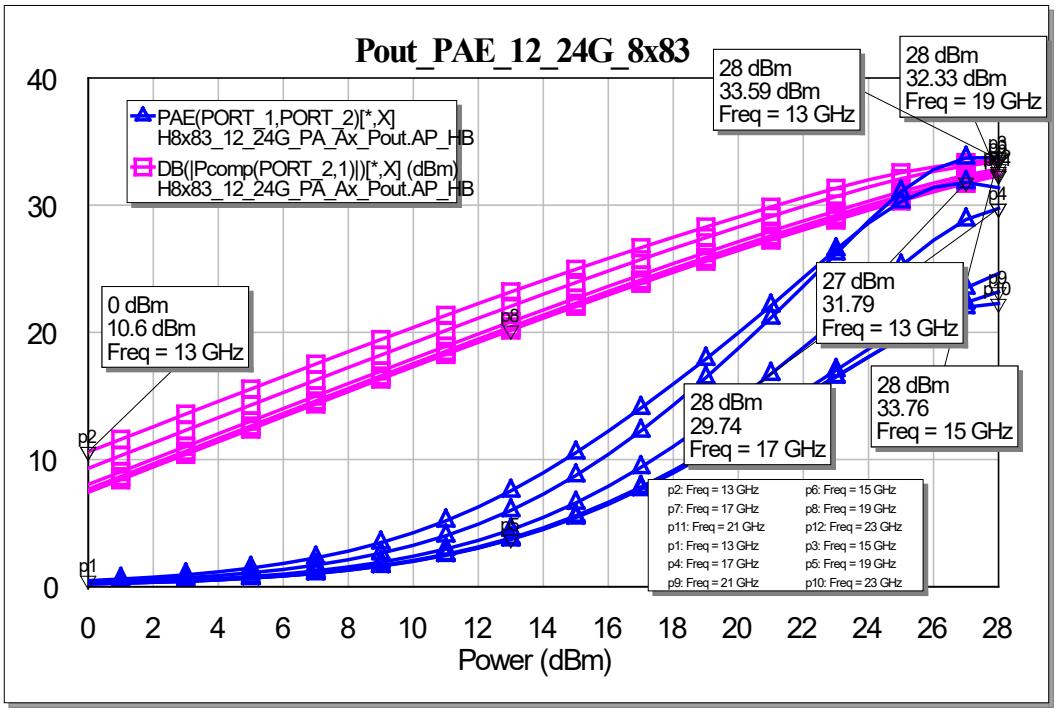

Fig. 24 Output power (magenta) and PAE (blue) vs. input-power one-stage 8- × 83-µm 12–24-GHz PA (20 V)

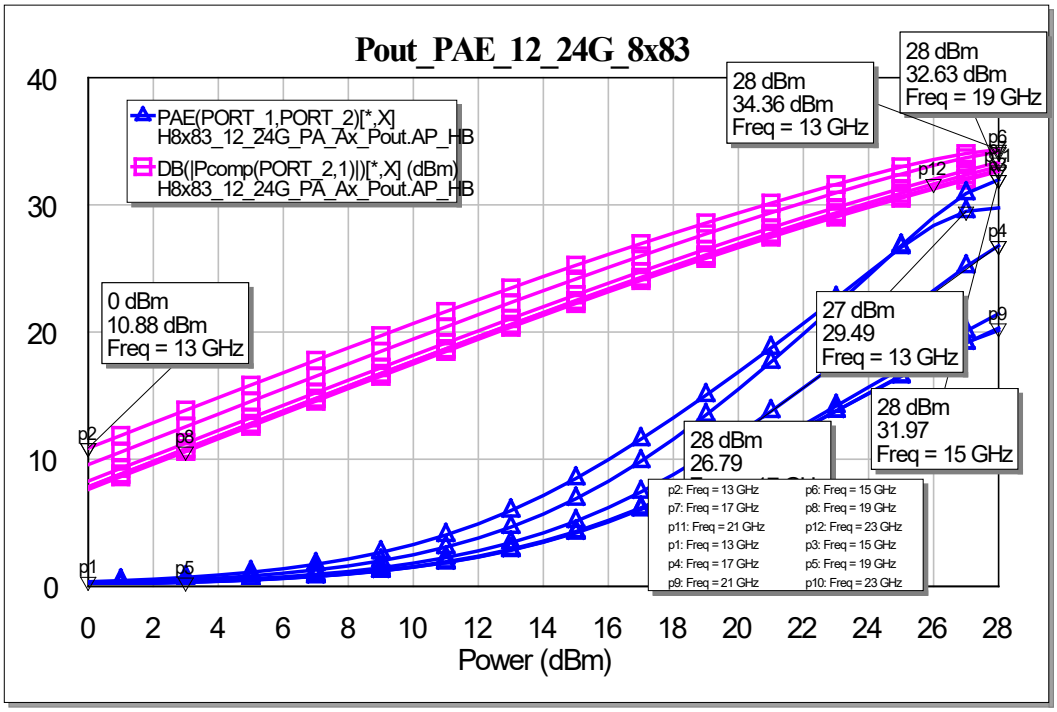

Fig. 25 Output power (magenta) and PAE (blue) vs. input-power one-stage 8- × 83-µm 12–24-GHz PA (24 V)

6. Broadband 6–12-GHz 2-W PA

Using the prior simulations and similar topologies for the input- and output-match circuits, a 6–12-GHz 2-W PA was designed. In the MMIC output-match design, loss relative to the desired parallel RC power match is about 1 dB from 5 to 16 GHz, which is shown relative to the lossless ideal match in Fig. 26. The small signal gain of the one-stage PA is 14 dB at 6 GHz and still above 10 dB at 16 GHz, achieving the 6–12-GHz goal (Fig. 27). Note that the PA load pull simulations were done at 24 V. For now, most of the linear simulations are done at 20 V and when the designs are fabricated and tested, the performance should be evaluated at 24 V and 28 V as well. Power simulations predict about 2 W of output power (33 dBm) at 20 V from 6 to 12 GHz as shown in Fig. 28. Output power increases to about 2.5 W of output power (34 dBm) at 24V from 6 to 12 GHz as shown in Fig. 29.

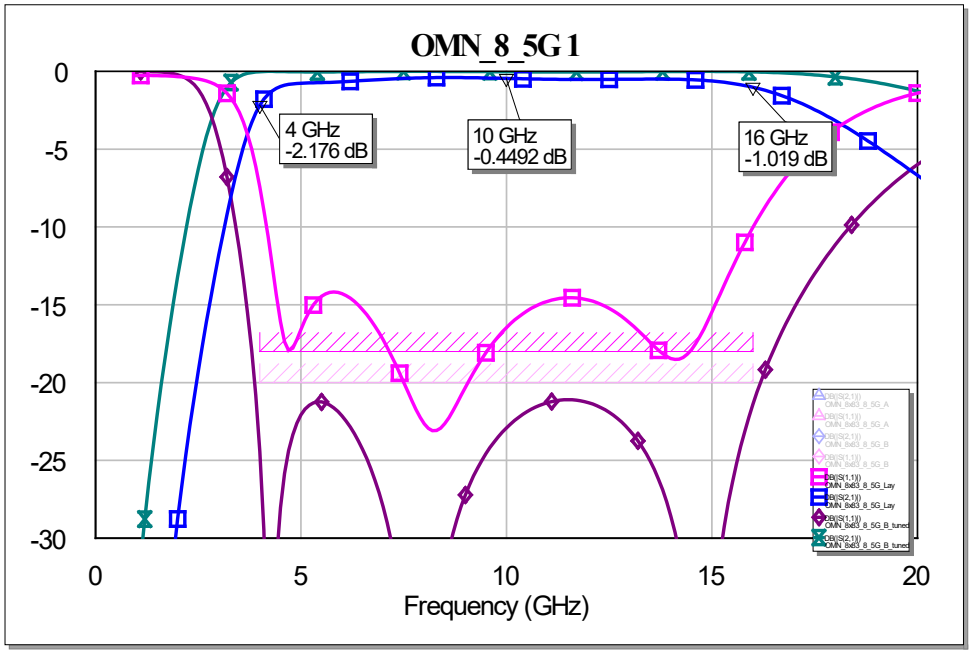

Fig. 26 Lossless-output match (thin) vs. MMIC output-match layout (thick) for 6–12 GHz

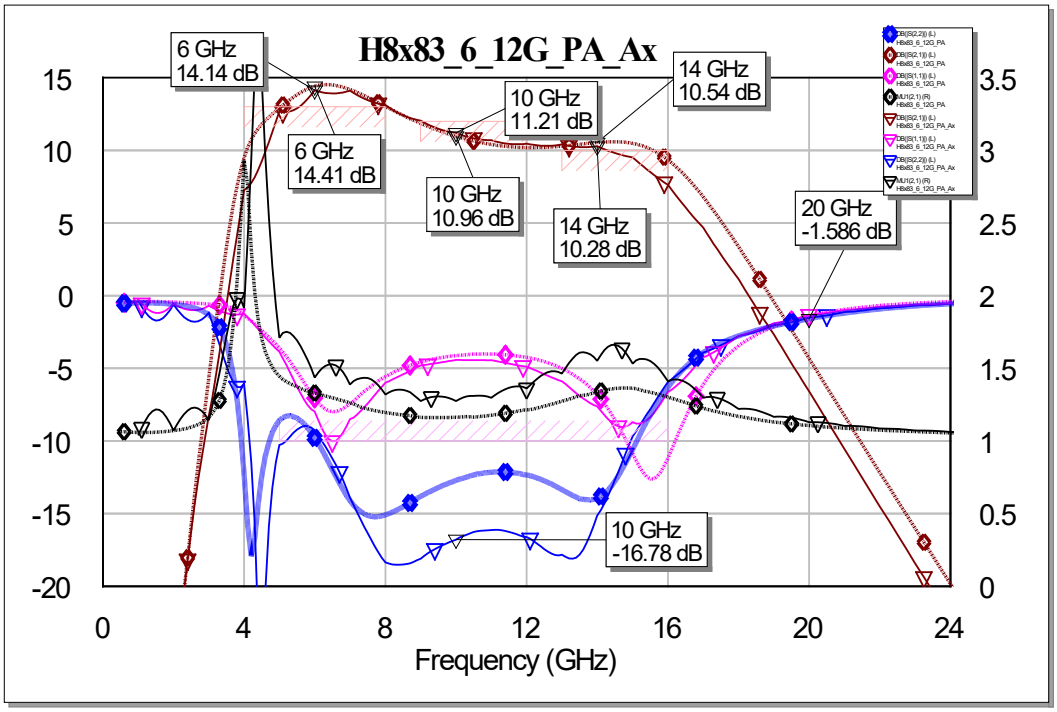

Fig. 27 S-parameter simulation of MMIC 8- × 83-µm 6–12-GHz PA (dot–dash traces)

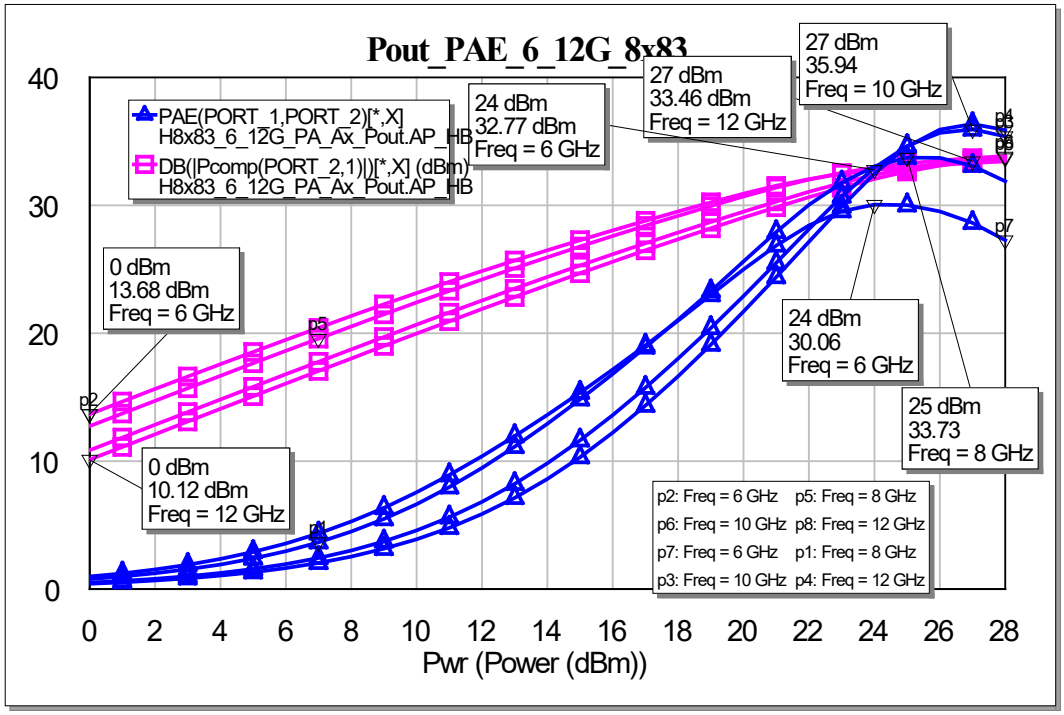

Fig. 28 Output power (magenta) and PAE (blue) vs. input-power one-stage 8- × 83-µm 6–12-GHz PA (20 V)

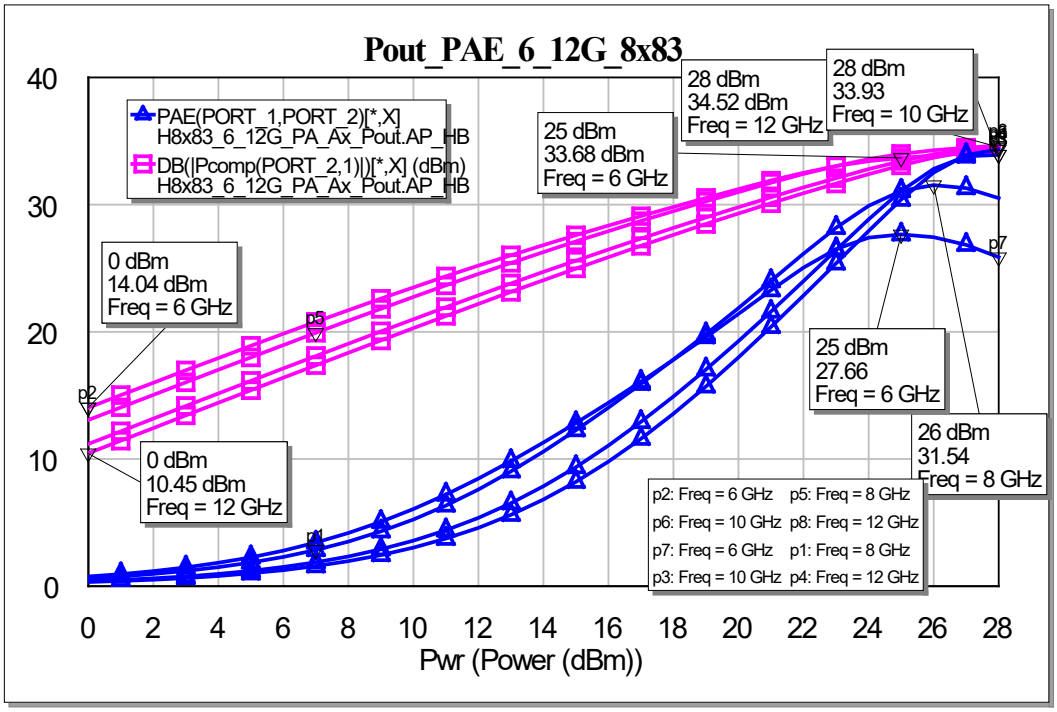

Fig. 29 Output power (magenta) and PAE (blue) vs. input-power one-stage 8- × 83-µm 6–12-GHz PA (24 V)

A full layout of the one-stage 6–12-GHz PA is shown in Fig. 30, which has a DC pad for Vgg at the top left and DC pads for Vdd at the top and bottom middle.

Using one of the broadband feedback amplifiers as a driver stage for the PAs allowed for a quick design of a two-stage 6–12-GHz PA. The simulation and layout of the two-stage 6–12-GHz 2-W PA is shown in Figs. 31 and 32. While the feedback amplifier's gain drops considerably at higher frequencies, it was used to quickly design a two-stage 12–24-GHz PA. Gain drops off above 20 GHz but is increased moderately by the additional compact-driver stage. The simulation and layout of the two-stage 12–24-GHz 2-W PA is shown in Figs. 33 and 34.

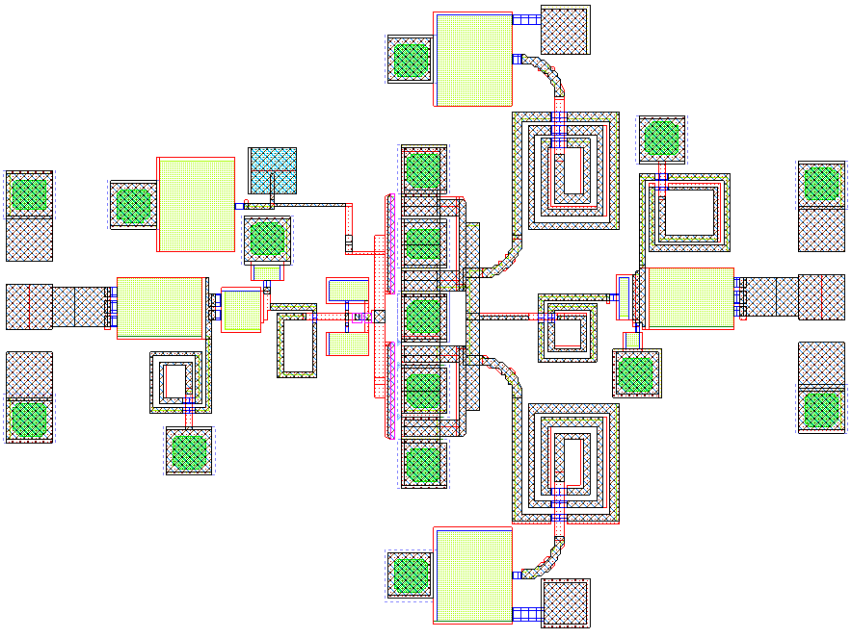

Fig. 30 Layout of one-stage 8- × 83-µm 6–12-GHz PA

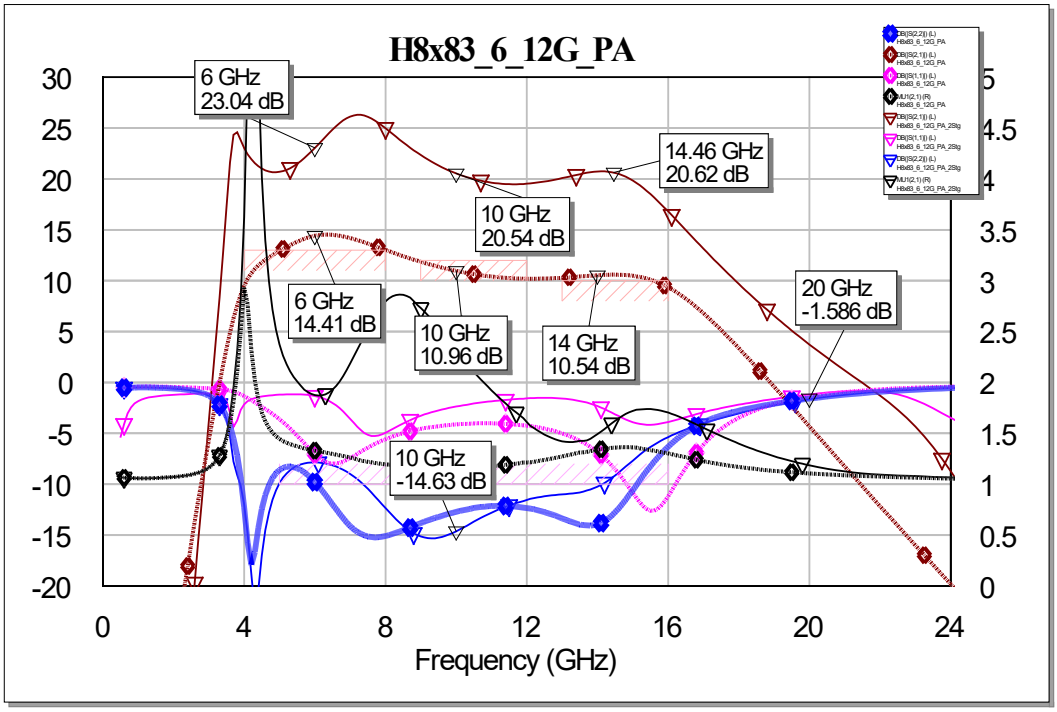

Fig. 31 S-parameter simulation of MMIC one- (dash) and two-stage (solid) 6–12-GHz PAs

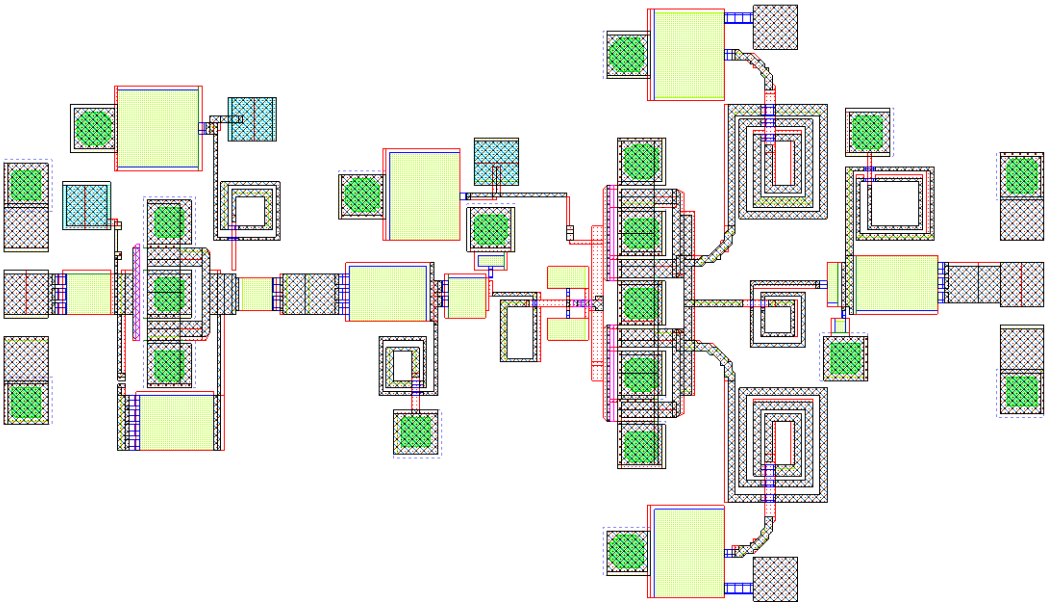

Fig. 32 Layout of MMIC two-stage 6–12-GHz PA

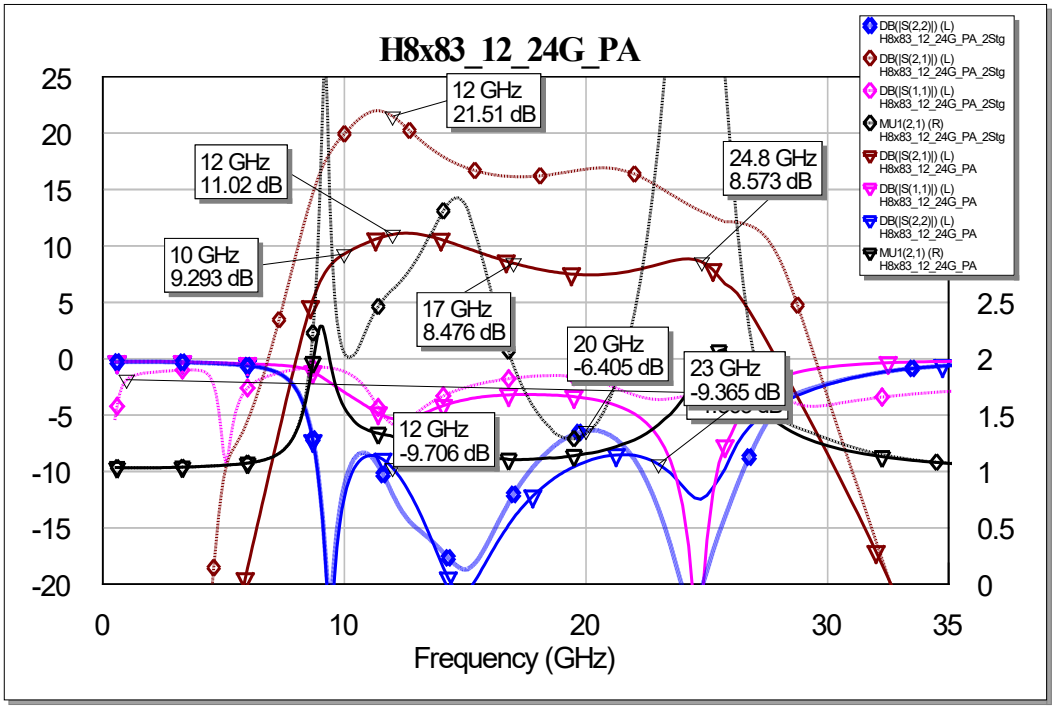

Fig. 33 S-parameter simulation of MMIC one- (solid) and two-stage (dash) 12–24-GHz PAs

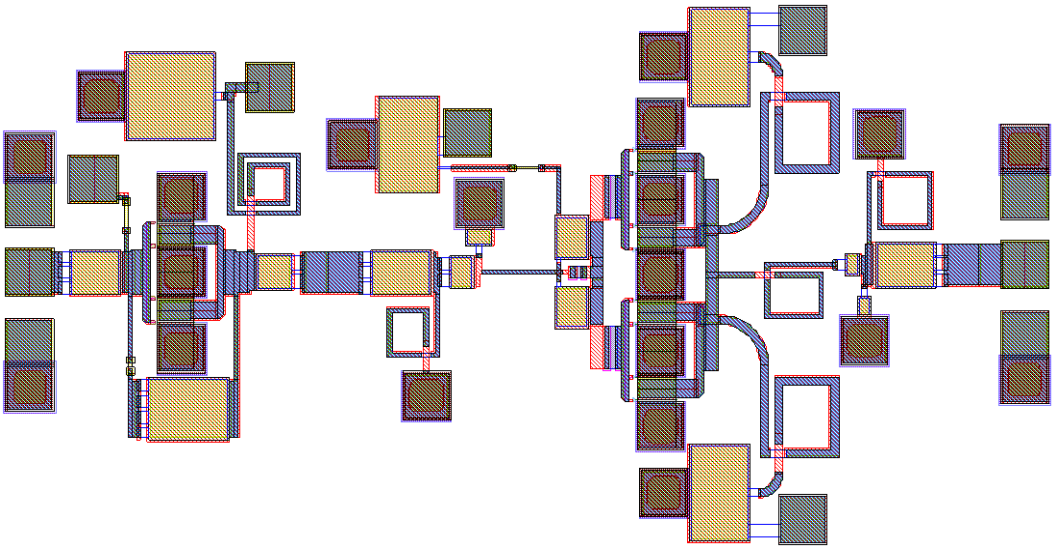

Fig. 34 Layout of MMIC two-stage 12–24-GHz PA

7. Transmit/Receive (TR) Switch

While there were no switch elements in the current PDK, BAE supplied s-parameter measurements of HEMTs at various On and Off DC biases for different-sized HEMTs to use for designing switch circuits. A simple model of an HEMT switch

consists of a resistor for the On state (RON) and a capacitance for the Off state (COFF). The RON scales inversely proportional to the HEMT size, while COFF scales proportional to the size; that is, RON * COFF is a constant for a given process. A simple, scaleable parallel RC model's schematic is shown in Fig. 35. Plots of the provided On and Off switch data, as shown are Figs. 36 and 37, were used to calculate the RON and COFF values. From the plot in Fig. 36, the RON scales as 2.5 ohm/mm while COFF scales as 0.18 pF/mm from the plot in Fig. 37.

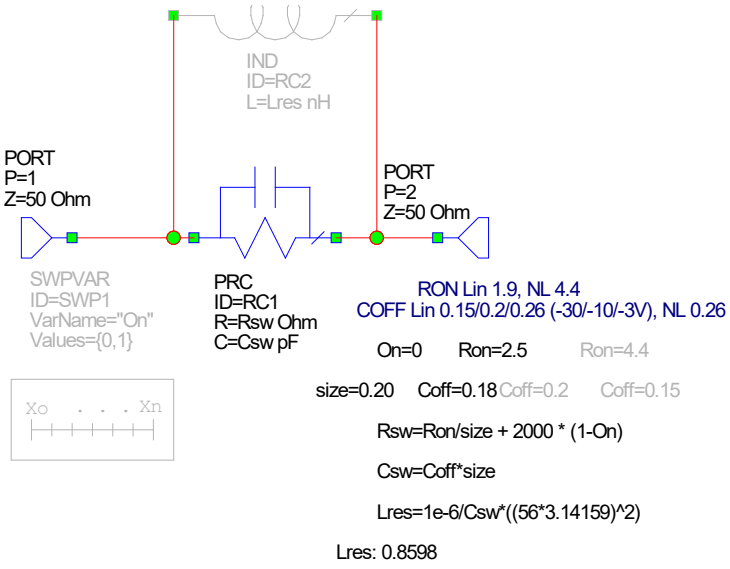

Fig. 35 Simple schematic of switch model (On = 0, 1; size = HEMT in mm)

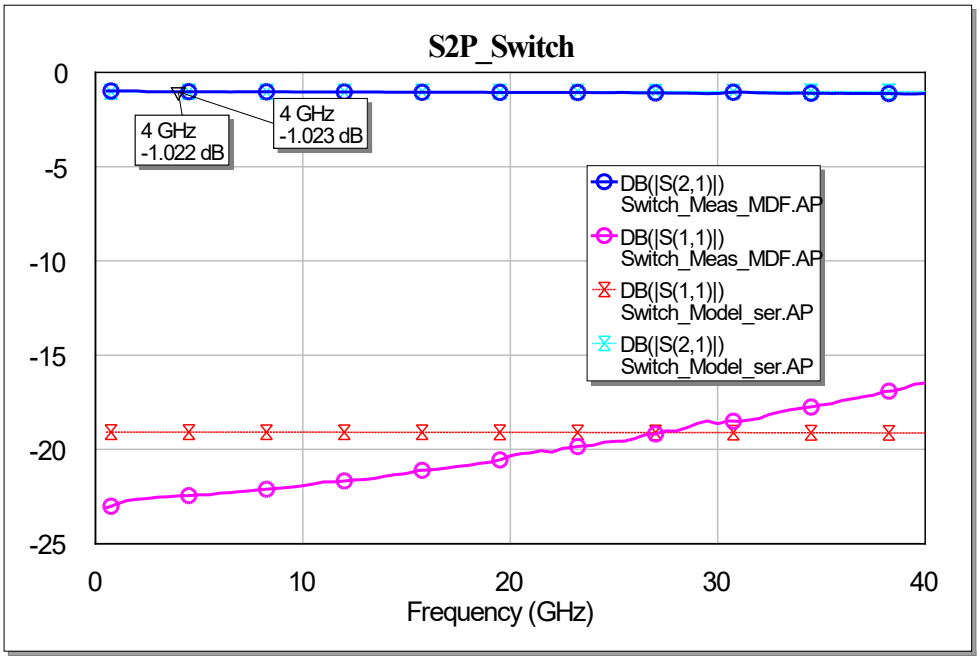

Fig. 36 S-parameters of switch in On state

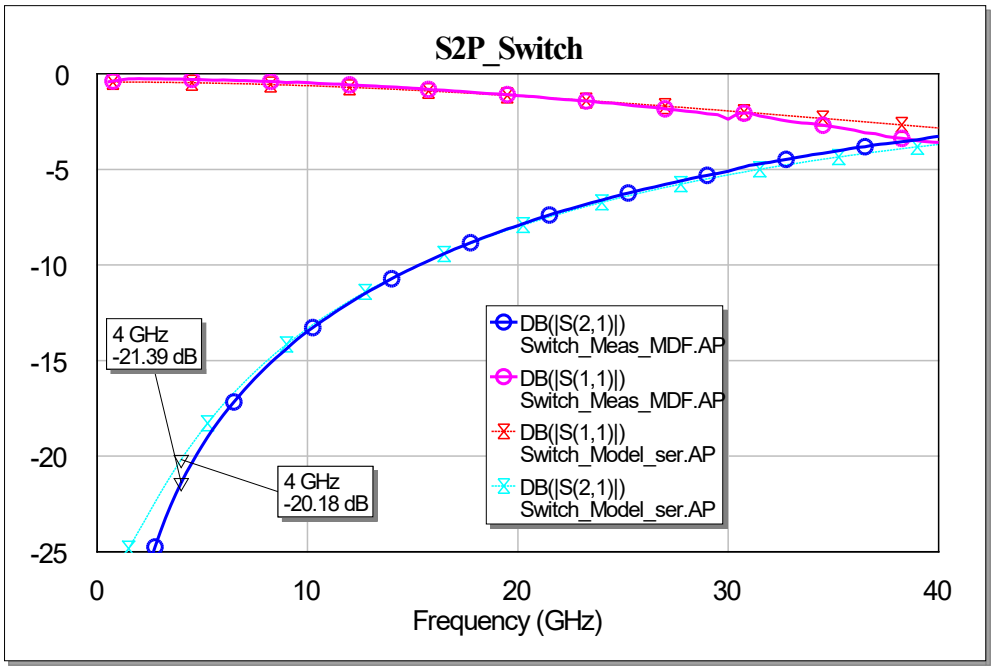

Fig. 37 S-parameters of switch in Off state

A TR switch was designed; an ideal equivalent single pull double throw (SPDT) schematic is shown in Fig. 38. Typically, the common connection is to an antenna, and the DC biases control two series and two shunt switches to connect the antenna to either an LNA or a PA. Figure 39 shows the layout of the TR switch, with the two complementary DC bias pads on the left, the common (antenna) connection is on the right, and top and bottom are the two RF signals for the SPDT switch. A simulation of the small signal performance is shown in Fig. 40 up to 12 GHz.

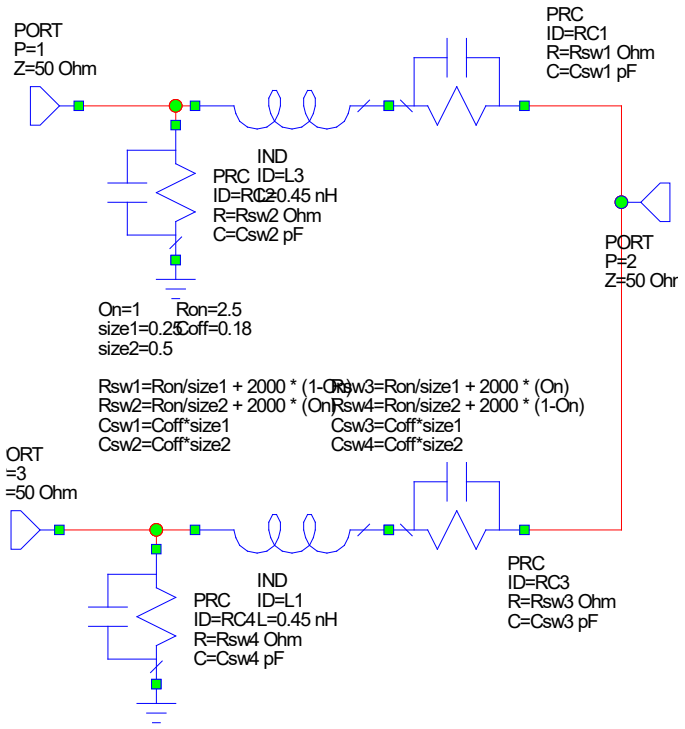

Fig. 38 Schematic of ideal SPDT TR switch

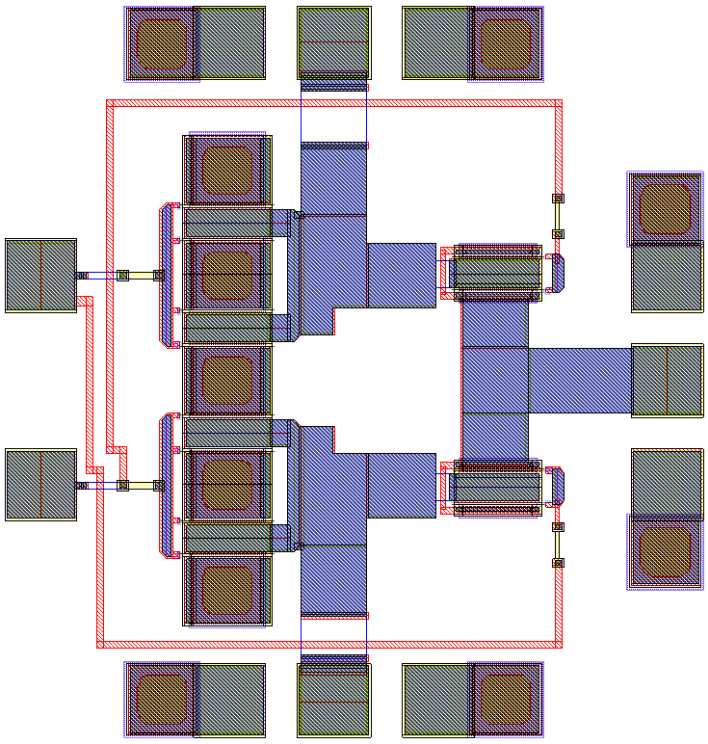

Fig. 39 Layout of TR switch

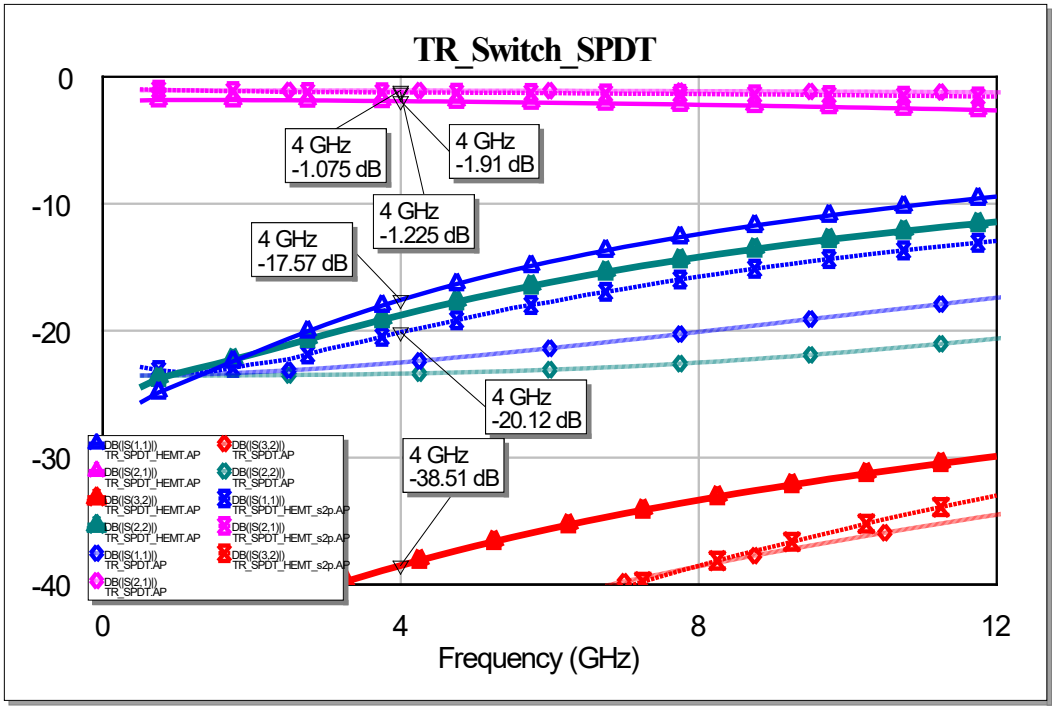

Fig. 40 S-parameter simulation of TR switch

8. Ka-Band Mixer

A Ka-band passive mixer was created using a Lange coupler, two HEMTs as diodes, and a low pass filter (LPF) for the intermediate-frequency (IF) output. The layout is shown in Fig. 41, with two RF connections for local oscillator and RF, and one for the IF at the bottom, near the LPF. Only the Lange coupler was simulated, verifying its broadband performance around 30 GHz (Fig. 42). The nonlinear simulation of the mixer failed and gave an error message. Evaluating the design will have to await testing. Hopefully, future PDKs will have more capability in their nonlinear models for simulating designs other than amplifiers.

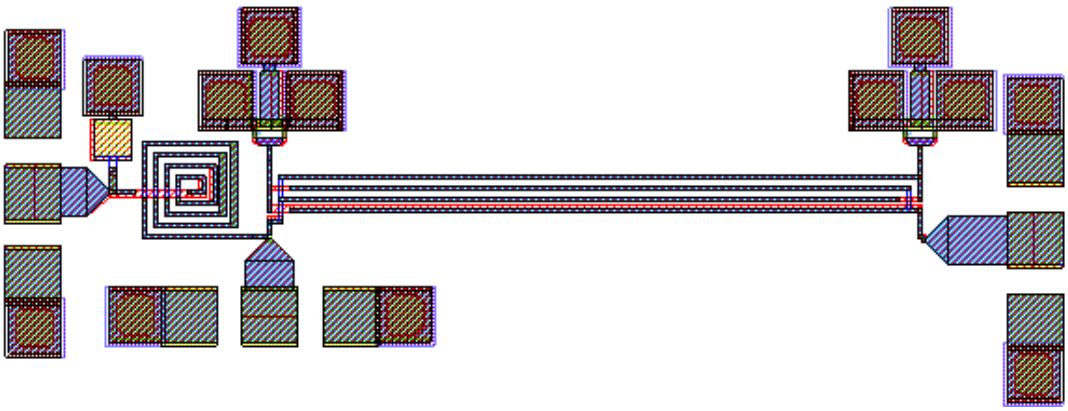

Fig. 41 Layout of Ka-band diode mixer

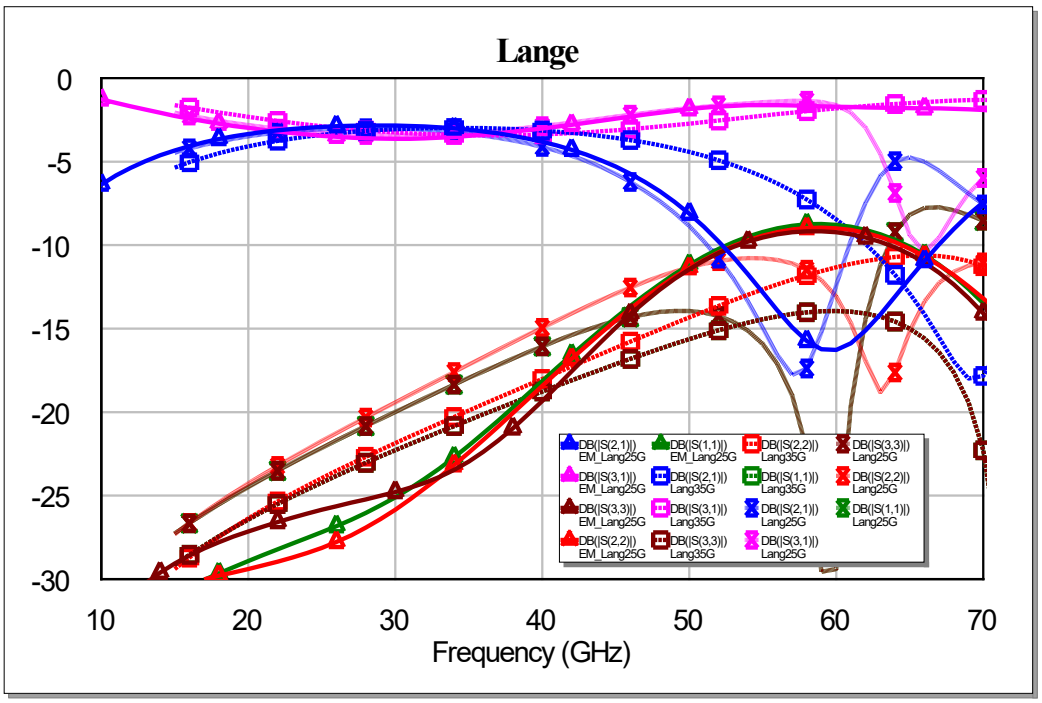

Fig. 42 Simulation of Ka-band Lange coupler (part of diode mixer)

9. Ka-Band Frequency Doubler

The current architecture for an extremely broadband transmitter uses broadband frequency multipliers. A frequency doubler with an input of around 25 GHz (Ka band) was designed in the BAE process using a 2- × 100-µm HEMT as the active nonlinear device. For the input match of the HEMT, a simple conjugate match near 25 GHz is designed, while the output match is a simple conjugate match at twice the frequency, or 50 GHz. Stability must be considered, and the plot of the small signal match on a Smith chart shows unconditional stability over frequency with an excellent input match near 25 GHz and with an excellent output match near twice that frequency at 50 GHz (Fig. 43). A plot of the layout of a single-stage frequency doubler is show in in Fig. 44. (Note the gate bias pad in upper left and the drain bias pad in upper right.) DC bias should be varied under test to determine optimal performance for the frequency multiplier. A nonlinear simulation (Fig. 45), with the HEMT at a moderate gate bias (Vgs = –3 V) and moderate drain voltage (Vdd = 5 V) to enhance nonlinear characteristics, shows a strong second harmonic (magenta), but also creates a large fundamental harmonic (blue) that would typically be filtered out.

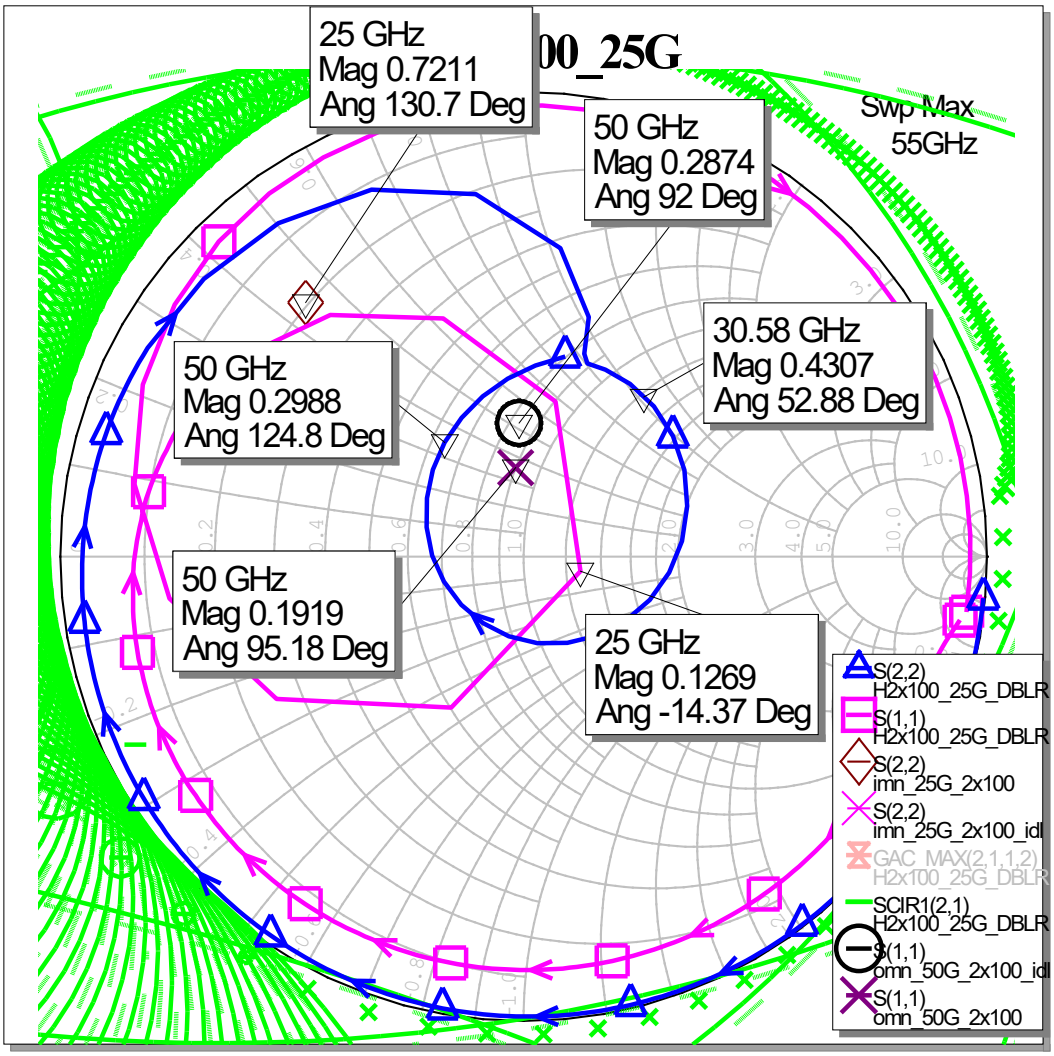

Fig. 43 Small-signal simulation of 25-GHz 2- × 100-µm frequency doubler

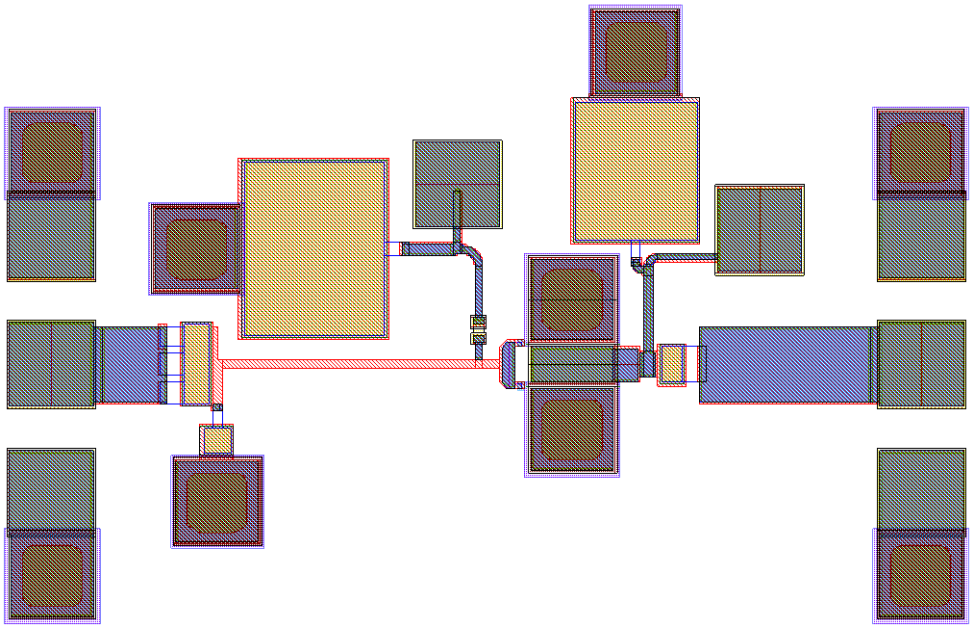

Fig. 44 Final layout of single-stage 25-GHz 2- × 100-µm frequency doubler

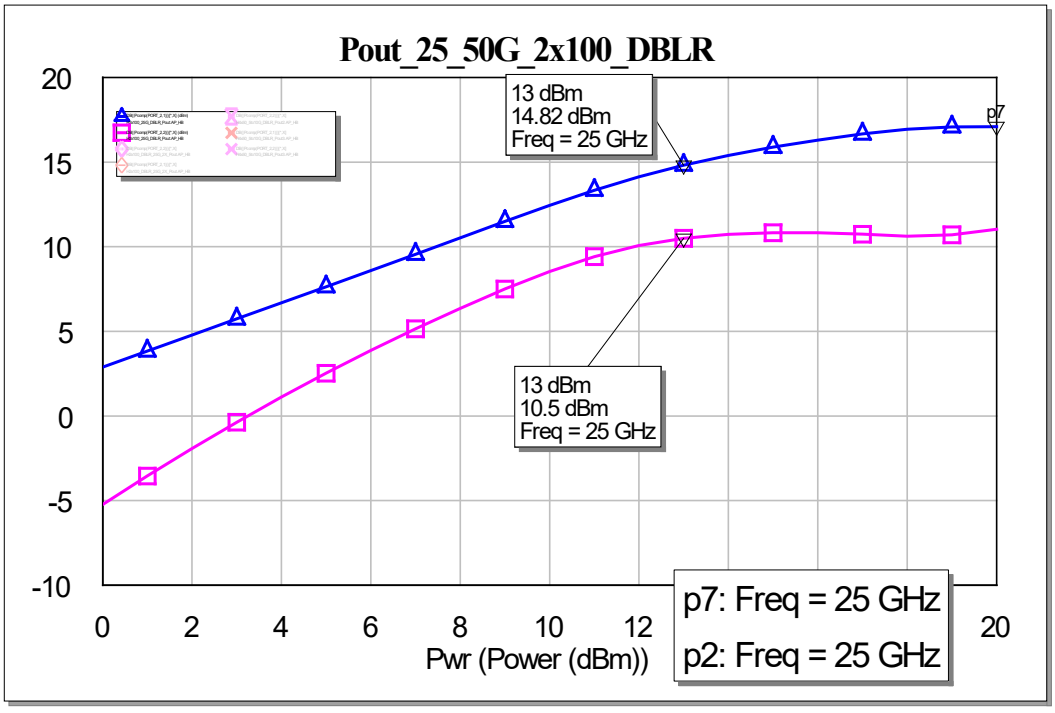

Fig. 45 Nonlinear simulation of 2- × 100-µm frequency doubler (25 GHz out—blue; 50 GHz out—magenta)

Sami Hawasli designed a broadband balun in the BAE process, which takes an input and splits it into two outputs that have a 180° phase difference. Using a variation

of this balun design centered on an input of 25 GHz, a fundamental cancelling-frequency doubler was created by parallel combining two of the previous single-stage doublers. The input uses a balun splitter and an output in-phase Wilkinson combiner to sum the outputs such that the input frequency is highly attenuated while its second harmonic output is added in-phase. A plot of the layout of a fundamental cancelling-frequency doubler is shown in in Fig. 46. A nonlinear simulation (Fig. 47) with the HEMTs at a moderate gate bias (Vgs = –3 V) and moderate drain voltage (Vdd = 5 V) to enhance nonlinear characteristics shows a strong second harmonic (magenta, dot–dash), while cancelling the fundamental harmonic (blue, dot–dash). Note the comparison with the single-stage doubler (solid traces) in the same figure showing the strong—nearly 30 dB—cancellation of the fundamental by using this architecture. Another illustration of the nonlinear operation is the time waveform plot in Fig. 48; note the doubling of the input frequency (25 GHz, magenta) at the output (50 GHz, blue). Both circuits will be tested for comparison with simulations and to evaluate the design approaches.

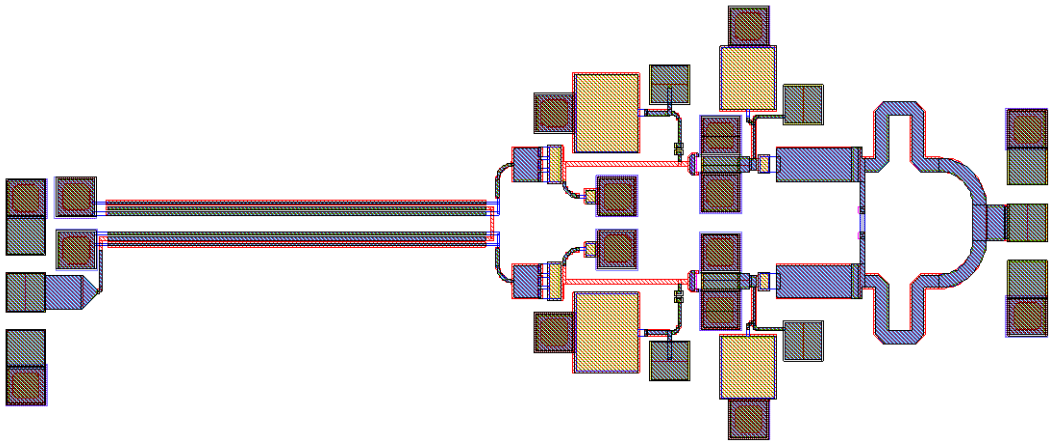

Fig. 46 Final layout of fundamental cancelling 25-GHz 2- × 100-µm frequency doubler (with balun)

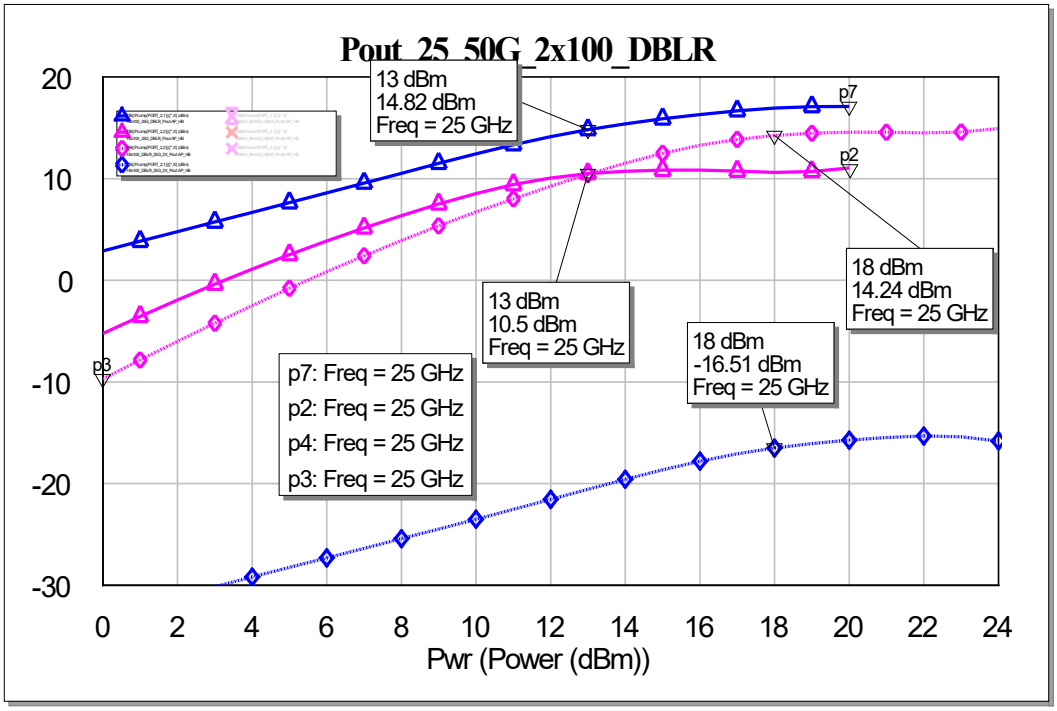

Fig. 47 Nonlinear simulation of fundamental cancelling 25-GHz 2- × 100-µm frequency doubler (dot–dash)

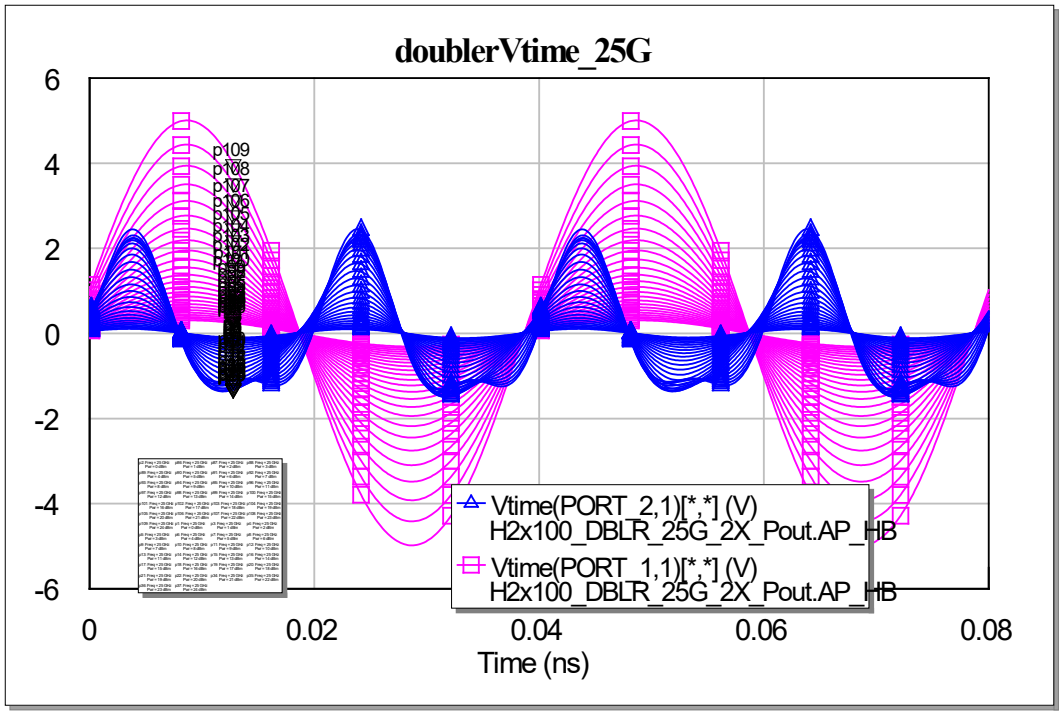

Fig. 48 Time waveforms showing fundamental cancelling 25-GHz 2- × 100-µm frequency doubler

10. Conclusions

The GAN RF Challenge effort included many teams exploring challenges focused on the broadband 5G development and EW needs related to DOD requirements. Parallel fabrication efforts using BAE's 0.18-µm GaN process and Qorvo's 0.15-µm GaN process will consolidate and produce multiple design-team efforts, with die to be returned in 2021 for test. Our ARL III/V Design Team was primarily focused on the BAE design effort; some of those designs are documented in this report. Broadband amplifiers, mixers, frequency multipliers, and other microwave circuits were designed to meet some of the DOD challenges, particularly in EW and future congested and contested RF spectrum as 5G develops. When the designs return, they will be tested, evaluated, and documented for future use and incorporation into DOD needs.

List of Symbols, Abbreviations, and Acronyms

ARL	Army Research Laboratory
CAD	computer-aided design
COFF	capacitance for the Off state
DC	direct current
DEVCOM	US Army Combat Capabilities Development Command
DOD	US Department of Defense
DRC	design rule check
EW	electronic warfare
GaN	gallium nitride
HEMT	high electron mobility transistor
IF	intermediate frequency
LNA	low noise amplifier
LPF	low pass filter
MMIC	monolithic microwave integrated circuit
PA	power amplifier
PAE	power-added efficiency
PDK	process design kit
RC	resistor–capacitor
RF	radio frequency
RON	resistor for the On state
SPDT	single pull double throw
TR	transmit/receive
Vdd	drain DC supply voltage
Vgg	gate DC supply voltage

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