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DEVCOM Army Research Laboratory Specialty Electronic Materials and Sensors Cleanroom (SEMASC) Dry-Etching Capability

by Nelson Mark and Gerard Dang

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14. ABSTRACT

This report presents the dry-etch capabilities at the US Army Combat Capabilities Development Command Army Research Laboratory Specialty Electronic Materials and Sensors Cleanroom research facility. This encompasses plasma- and gaseous-chemical-reaction-based processes for removing a wide range of materials used by internal and external customers. The currently installed tool base for dry etching as well as the processing capabilities for each tool are discussed.

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Contents

List of Figures vi

1. Introduction 1

2. Tools for Deep Silicon Etching 1

2.1 Purpose 1

2.2 PlasmaTherm Versaline Deep Silicon Etcher (DSE1) 2

2.2.1 Model and Specifications 2

2.2.2 Materials and Processing 3

2.2.3 Example Applications 4

2.3 PlasmaTherm Versaline (DSE2) 4

2.3.1 Model and Specifications 4

2.3.2 Materials and Processing 5

2.3.3 Example Applications 5

2.4 PlasmaTherm SLR 700 5

2.4.1 Model and Specifications 5

2.4.2 Materials and Processing 6

2.4.3 Example Applications 7

3. Tools for Etching of III-V Compounds, Metals, and General Materials 8

3.1 Purpose 8

3.2 PlasmaTherm Versalock 700 PM2, Model VLR-702-PM770I-10R 8

3.2.1 Model and Specifications 8

3.2.2 Materials and Processing 9

3.2.3 Example Applications 9

3.3 Oxford PlasmaLab 100 ICP 380 9

3.3.1 Model and Specifications 9

3.3.2 Materials and Processing 10

3.3.3 Example Applications 11

3.4 Ulvac NE-550EXa 11

3.4.1 Model and Specifications 11

3.4.2 Materials and Processing 12
3.4.3 Example Applications 13

4. Tools for Etching Oxides, Nitrides, and Silicon 13

4.1 Purpose 13
4.2 PlasmaTherm Versalock 700 PM3 13
4.2.1 Model and Specifications 13
4.2.2 Materials and Processing 14
4.2.3 Example Applications 14
4.3 Xactix X2B Xenon DiFluoride Etcher 15
4.3.1 Model and Specifications 15
4.3.2 Materials and Processing 15
4.3.3 Example Applications 16
4.4 Primaxx MEMS-CET HF Vapor Etcher 16
4.4.1 Model and Specifications 16
4.4.2 Materials and Processing 17
4.4.3 Example Applications 17

5. Tools for Photoresist Stripping and Wafer Cleaning 18

5.1 Purpose 18
5.2 Axcelis 200ES Downstream Asher 18
5.2.1 Model and Specifications 18
5.2.2 Materials and Processing 18
5.2.3 Example Applications 19
5.3 Anatech SCE1000 Barrel Asher 19
5.3.1 Model and Specifications 19
5.3.2 Materials and Processing 20
5.3.3 Example Applications 20
5.4 UVOCS Ozone Cleaner 21
5.4.1 Model and Specifications 21
5.4.2 Materials and Processing 21
5.4.3 Example Applications 22
5.5 PVA Tepla Ion 40 22
5.5.1 Model and Specifications 22
5.5.2 Materials and Processing 22

5.5.3 Example Applications 23

5.6 PVA Tepla Ion Wave 10 23

5.6.1 Model and Specifications 23

5.6.2 Materials and Processing 24

5.6.3 Example Applications 24

6. Tools for Etching PZT and Metals 25

6.1 Purpose 25

6.2 4Wave Planetary Stage Ion Beam Etcher (PSIBE) 25

6.2.1 Model and Specifications 25

6.2.2 Materials and Processing 26

6.2.3 Example Applications 26

7. 10-Year Plan 26

8. Conclusion 27

9. References 28

List of Symbols, Abbreviations, and Acronyms 29

Distribution List 31

List of Figures

Fig. 1 Bosch process ... 2
Fig. 2 PlasmaTherm Versaline DSE ... 3
Fig. 3 PlasmaTherm SLR 770 DSE ... 6
Fig. 4 PlasmaTherm Versalock 700 etching system ... 8
Fig 5. Oxford Instruments PlasmaLab 100 ICP etcher ... 10
Fig. 6 Ulvac NE-550EXa etcher ... 12
Fig. 7 PlasmaTherm Versalock 700 etching system ... 14
Fig. 8 Xactix X2B XeF2 etching system ... 15
Fig. 9 Primaxx MEMS-CET HF vapor etcher ... 17
Fig. 10 Axcelis 200ES Downstream Asher ... 18
Fig. 11 Anatech SCE1000 Barrel Asher ... 20
Fig. 12 UVOCS ozone cleaner ... 21
Fig. 13 PVA Tepla Ion 40 ... 22
Fig. 14 PVA Tepla Ion Wave 10 ... 24
Fig. 15 4Wave PSIBE ... 25

1. Introduction

The Army Research Laboratory Specialty Electronic Materials and Sensors Cleanroom (SEMASC) is located at the US Army Combat Capabilities Development Command Army Research Laboratory in Adelphi, Maryland, and housed in the Zahl Research Facility (Building 207). It is divided into two sections. One area is 10,000 sq.ft in size and rated Class 100. The second area is 5000 sq.ft in size and rated Class 10. It is a raised floor design, with facilities routed under the floor or above the ceiling tiles. Air is purified by means of high-efficiency particulate-air filters installed in the ceiling tiles. The installed equipment base provides a full suite of semiconductor and micro-electromechanical system (MEMS) processing capabilities. This report concentrates on the dry-etching capabilities available to researchers using DEVCOM Army Research Laboratory's cleanroom.

2. Tools for Deep Silicon Etching

2.1 Purpose

These tools are used for deep (high aspect ratio) etching of silicon (Si). The process chamber utilizes an upper inductively coupled plasma (ICP) section to achieve high-density ionization of process gases and an RF-biased electrode for high anisotropy.

The feature etch is accomplished using the Bosch process (Fig. 1), which employs a scheme of alternating deposition and etch cycles to etch Si. The first step of the cycle is the deposition step, which uses a C4F8-based plasma to deposit a CxFy passivation polymer over all surfaces. The second step is an SF6-based directional plasma that removes material preferentially in the vertical direction. This removes the passivating film from the bottom of the trench while leaving passivation on the sidewalls. The third and last step is an SF6-based isotropic etch, which removes the exposed bottom Si, the remaining sidewall passivation, as well as some of the sidewall (hence the sidewall scalloping).

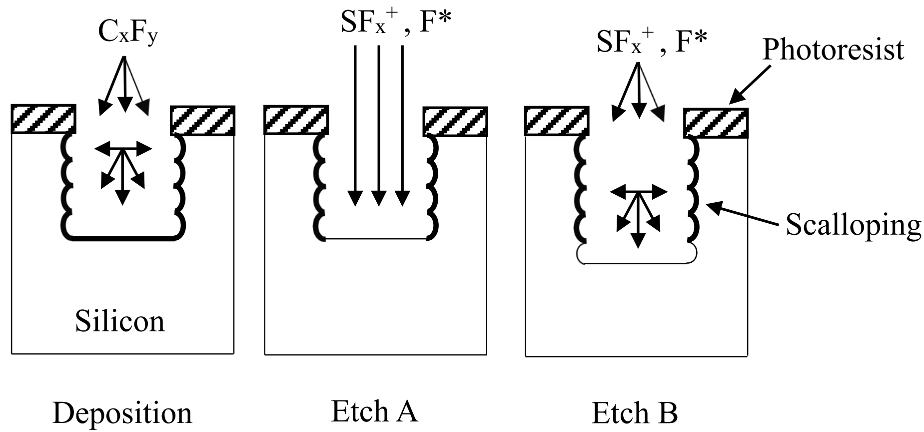

Fig. 1 Bosch process

2.2 PlasmaTherm Versaline Deep Silicon Etcher (DSE1)

2.2.1 Model and Specifications

Model: Versaline DSE PM#1; June 2012 (Fig. 2)

Specifications:

- Electrostatic chuck: 100-mm wafers
- End point: optical emission spectroscopy (OES)
- Process gases: octafluorocyclobutane (C_4F_8), sulfur hexafluoride (SF_6), oxygen (O_2), argon (Ar)
- Fast gas switching for smaller sidewall scalloping
    - Deposition (Dep): 1.5 versus 4 s
    - Etch A: 1.5 versus 2 s
    - Etch B: 2.0 versus 6 s
- Parameter morphing for profile control
- RF1 (reactive ion etching [RIE]): 1–100 kHz
- RF2 (ICP): 1.8–2.17 MHz (frequency tuning)
- Helium (He) backside cooling: 5 °C
- Single-wafer loadlock

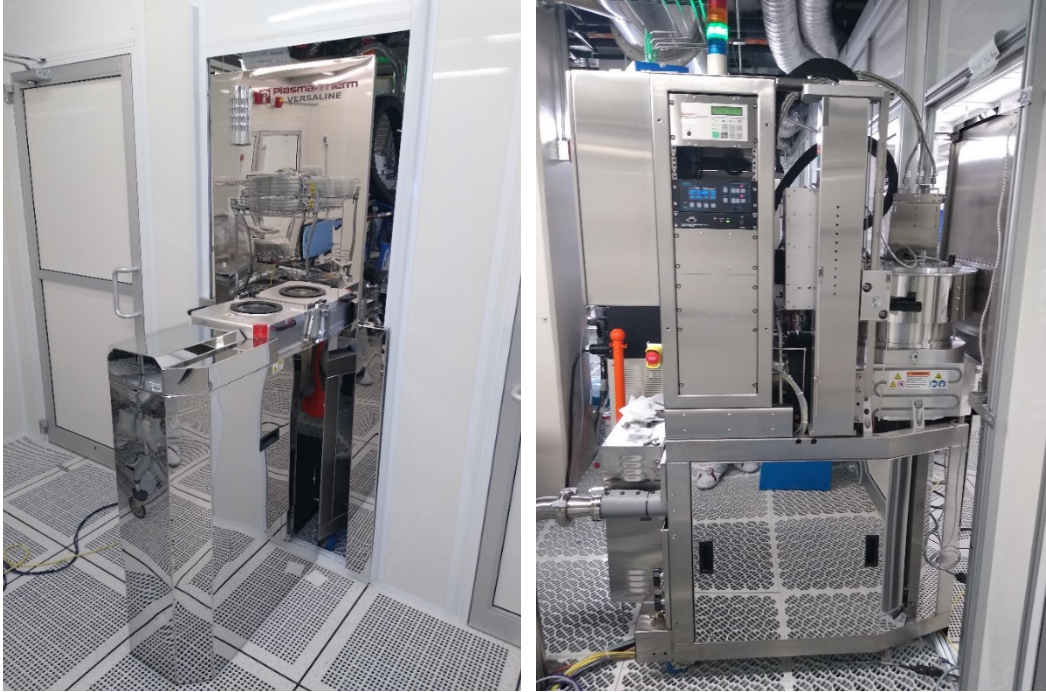

Fig. 2 PlasmaTherm Versaline DSE

2.2.2 Materials and Processing

Materials etched: Si

Mask: Photoresists (AZ 5214, AZ 9260), silicon dioxide (SiO_2), titanium (Ti), nickel (Ni)

Etch rates: up to 6 µm/min, depending on feature size

Selectivity: Si/resist > 70:1, Si/oxide > 100:1

Base recipe:

Dep: Pressure (P) = 25 mT, C4F8/Ar = 150/30 sccm, ICP/Bias = 1500 W/10 V, He = 6 Torr, temperature (T) = 5 °C, time (t) = 1.5 s

Etch A: Pressure (P) = 25 mT, SF6/Ar = 150/30 sccm, ICP/Bias = 1000 W/500 V, He = 6 Torr, T = 5 °C, t = 1.5 s

Etch B: Pressure (P) = 50 mT, SF6/Ar = 200/30 sccm, ICP/Bias = 2000 W/10 V, He = 6 Torr, T = 5 °C, t = 2.0 s

Processing requirements:

1) Backside of wafer must be clean. The 2-mm edge exclusion zone on the backside of the wafer must be clean and free of defects for it to seal properly on the electrostatic chuck (echuck). The wafer must lie flat on the echuck.

Otherwise, the tool will either error-out with an He backside cooling compliance error or the etch will be very nonuniform.

2) Through-wafer or release etches must be mounted to a dummy Si handling wafer. Otherwise, the process will abort due to He compliance errors at breakthrough, and debris will be left on the electrostatic chuck.

2.2.3 Example Applications

- Through-Si-via (TSV) etch
- Silicon etch to a buried SiO_2 layer on a silicon-on-insulator (SOI) wafer
- Release of devices
- CxFy polymer coating
- Fabrication of support module for microshutter array
- Development of lead zirconate titanate (PZT)-based piezoelectric MEMs technology at ARL[1]

2.3 PlasmaTherm Versaline (DSE2)

2.3.1 Model and Specifications

Model: Versaline DSE PM#1

Specifications:

- Echuck: 150-mm wafers
- End point: none
- Process gases: C_4F_8, SF_6, O_2, Ar
- Fast gas switching for smaller sidewall scalloping
- Parameter morphing for profile control
- RF1 (RIE): 1–100 kHz
- RF2 (ICP): 1.8–2.17 MHz (frequency tuning)
- He backside cooling: 5 °C
- Single-wafer loadlock

2.3.2 Materials and Processing

Materials etched: Si

Mask: Photoresists (AZ 5214, AZ 9260), SiO_2, Ti, Ni

Etch rates: up to 6 µm/min depending on feature size

Selectivity: Si/resist > 70:1, Si/oxide > 100:1

Base recipe:

> Dep: P = 25 mT, C4F8/Ar = 150/30 sccm, ICP/Bias = 1500 W/10 V, He = 6T, T = 5 °C, t = 1.5 to 1.2 s
>
> Etch A: P = 25 mT, SF6/Ar = 150/30 sccm, ICP/Bias = 1000 W/500–600 V, He = 6T, T = 5 °C, t = 1.5 s
>
> Etch B: P = 50 mT, SF6/Ar = 200/30 sccm, ICP/Bias = 2000 W/10 V, He = 6T, T = 5 °C, t = 2.0 s

Processing requirements:

1) Backside of wafer must be clean. The 2-mm edge exclusion zone on the backside of the wafer must be clean and free of defects for it to seal properly on the echuck. The wafer must lie flat on the echuck; otherwise, the tool will either error-out with an He backside cooling compliance error or the etch will be very nonuniform.
2) Through-wafer or release etches must be mounted to a dummy Si-handling wafer. Otherwise, the process will abort due to He compliance errors at breakthrough and debris will be left on the echuck.

2.3.3 Example Applications

- TSV etch
- Si etch to a buried SiO_2 layer on an SOI wafer
- Fabrication of scanning electron microscope specimen heaters
- CxFy polymer coating

2.4 PlasmaTherm SLR 700

2.4.1 Model and Specifications

Model: SLR ICP 770 Mn frame; October 9, 1997 (Fig. 3)

Specifications:

- Echuck: 100-/150-mm wafers (easy to switch between form factors)
- Process gases: C_4F_8, SF_6, O_2, Ar
- RF1 (RIE): 13.56 MHz
- RF2 (ICP): 1.72–2.1 MHz
- He backside cooling: 20 °C
- Single-wafer loadlock

Fig. 3 PlasmaTherm SLR 770 DSE

2.4.2 Materials and Processing

Materials etched: Si

Mask: Photoresists (AZ 5214, AZ 9260), SiO_2, Ti, Ni

Etch rate: up to 2.8 µm/min depending on feature size

Selectivity: Si/resist > 50:1, Si/oxide > 70:1

Base recipe:

Dep: P = 25 mT, C4F8/Ar = 70/30 sccm, ICP/Bias = 1500 W/10 W, He = 4T, T = 20 °C, t = 4 s

Etch A: P = 25 mT, SF6/Ar = 50/30 sccm, ICP/Bias = 1000 W/20 W, He = 4T, T = 20 °C, t = 2 s

Etch B: P = 50 mT, SF6/Ar = 100/30 sccm, ICP/Bias = 2000 W / 10 W, He = 4T, T = 20 °C, t = 6 s

Processing requirements

1) Backside of wafer must be clean. The 2-mm edge exclusion zone on the backside of the wafer must be clean and free of defects for it to seal properly on the echuck. The wafer must lie flat on the echuck. Otherwise, the tool will either error-out with an He backside cooling compliance error, or the etch will be very nonuniform.
2) Through-wafer or release etches must be mounted to a dummy Si handling wafer. Otherwise, the process will abort due to He compliance errors at breakthrough and debris will be left on the echuck.

2.4.3 Example Applications

- TSV etch
- Si etch to a buried SiO_2 layer on an SOI wafer
- Release of devices
- CxFy polymer coating
- Shallow alignment marks on Si wafers
- Nitride etch

3. Tools for Etching of III-V Compounds, Metals, and General Materials

3.1 Purpose

These tools are for general plasma etching of a wide variety of materials. The process chamber uses an upper ICP section to achieve high-density ionization of process gases and an RF-biased electrode for high anisotropy. The exception is the Ulvac etcher, in which the process chamber employs an inductively super magnetron (ISM) plasma source to generate a high-density plasma. The electrode is RF-biased for ion energy control (anisotropy).

3.2 PlasmaTherm Versalock 700 PM2, Model VLR-702-PM770I-10R

3.2.1 Model and Specifications

Model: VLR-702-PM770I-10R; March 23, 2000 (Fig. 4)

Specifications:

- Mechanical clamp (alumina ceramic): 100-mm wafers
- Process gases: boron trichloride (BCl_3), chlorine (Cl_2), hydrogen bromide (HBr), SF_6, O_2, hydrogen (H_2), Ar
- RF1 (RIE): 13.56 MHz
- RF2 (ICP): 1.72–2.1 MHz
- He backside cooling: 15 °C
- 25-wafer cassette loadlock

Fig. 4 PlasmaTherm Versalock 700 etching system

3.2.2 Materials and Processing

Materials etched: III-V, II-VI compounds, aluminum (Al), InAlGaAs, gallium nitride (GaN), Si, silicon carbide (SiC)

Mask: Photoresists (AZ 5214, AZ9245, AZ 9260), SiO_2, Ti, Ni

Etch rate: varies, about 200 nm/min

Selectivity: varies, typically 1:1 to 1.5:1

Base recipe:

Etch: P = 2.5 mT, BCl_3/Cl_2 = 12.5/2.5 sccm, ICP/Bias = 500/100 W, He = 4T, T = 15 °C

Processing requirements:

1) Backside of wafer must be clean. The 2-mm edge exclusion zone on the backside of the wafer must be clean and free of defects for it to seal properly on the electrode. The wafer must lie flat on the electrode; otherwise, the tool will either error-out with an He backside cooling compliance error or the etch will be very nonuniform.
2) Through-wafer or release etches must be mounted to a dummy Si-handling wafer; otherwise, the process will abort due to He compliance errors at breakthrough and debris will be left on the electrode.

3.2.3 Example Applications

- Etching of mercury cadium telluride for IR detectors
- Etching of GaAs/Al_xGa_{1-x}As quantum well IR photodector superlattices to fabricate quantum grid IR photodectors[2]

3.3 Oxford PlasmaLab 100 ICP 380

3.3.1 Model and Specifications

Model: 100 ICP 380 (Fig. 5)

Specifications:

- Mechanical clamp (quartz): 100- and 150-mm wafers (easy to switch between form factors)
- Process gases: BCl_3, Cl_2, C_4F_8, SF_6, Trifluoromethane (CHF_3), O_2, H_2, Ar
- RF (RIE): 13.56 MHz

- ICP (ICP): 1.72–2.1 MHz
- He backside cooling
- Cryo electrode: liquid Ni (–110 °C) to 70 °C (cryo DSE capability)
- Single-wafer loadlock

Fig 5. Oxford Instruments PlasmaLab 100 ICP etcher

3.3.2 Materials and Processing

Materials etched: III-V, II-VI compounds, Al, InAlGaAs, GaN, Si, SiO_2, PZT

Mask: Photoresists (AZ 5214, AZ9245, AZ 9260), SiO_2, Ti, Ni

Etch rates: varies, about 200 nm/min

Selectivity: varies, typically 1:1 to 1.5:1

Base recipe:

Etch: P = 10 mT, CHF_3/Ar = 20/10 sccm, ICP/Bias = 800/40 W, He = 10T, T = 25 °C.

Processing requirements:

1) Backside of wafer must be clean. The 2-mm edge exclusion zone on the backside of the wafer must be clean and free of defects for it to seal properly on the electrode. The wafer must lie flat on the electrode; otherwise, the tool will either error-out with an He backside cooling compliance error, or the etch will be very nonuniform.

2) Through-wafer or release etches must be mounted to a dummy Si handling wafer; otherwise, the process will abort due to He compliance errors at breakthrough and debris will be left on the electrode.

3.3.3 Example Applications

- Cryo etching of Si for indium-tin-oxide ring oscillators
- Cryo DSE[3]
- SiO_2 etch for RF MEMS devices
- Hydrogen plasma treatment
- Hollow-core waveguides[4]

3.4 Ulvac NE-550EXa

3.4.1 Model and Specifications

Model: NE-550EXa (Fig. 6)

Specifications:

- Mechanical clamp (alumina ceramic): 100-, 150-, and 200-mm wafers (easy to switch between form factors)
- End point: OES
- Process gases: BCl_3, Cl_2, HBr, C_4F_8, SF_6, CF_4, O_2, Ar
- Bias (RIE): 13.56 MHz
- Antenna (ISM): 13.56 MHz
- Heated electrode: 5–180 °C
- Single-wafer loadlock

Fig. 6 Ulvac NE-550EXa etcher

3.4.2 Materials and Processing

Materials etched: III-V, II-VI compounds, Al, InAlGaAs, GaN, Si, SiO_2, PZT, molybdenum disulfide, SiC

Mask: Photoresists (AZ 5214, AZ9245, AZ 9260), SiO_2, Ti, Ni

Etch rate: varies, about 200 nm/min

Selectivity: varies, typically 1:1 to 1.5:1

Base recipe:

Etch: P = 10 mT, CHF_3/Ar = 20/10 sccm, ICP/Bias = 800/40 W, He = 10 T, T = 25 °C

Processing requirements:

1) Backside of wafer must be clean. The 2-mm edge exclusion zone on the backside of the wafer must be clean and free of defects for it to seal properly on the electrode. The wafer must lie flat on the electrode; otherwise, the tool

will either error-out with an He backside cooling compliance error, or the etch will be very nonuniform.

2) Through-wafer or release etches must be mounted to a dummy Si handling wafer; otherwise, the process will abort due to He compliance errors at breakthrough and debris will be left on the electrode.

3.4.3 Example Applications

- SiC etching for metal–oxide–semiconductor field-effect transistor and insulated-gate bipolar transistor devices
- Etching GaN to form mesas for planar homojunction p-i-n devices for betavoltaic energy conversion[5]

4. Tools for Etching Oxides, Nitrides, and Silicon

4.1 Purpose

These tools are for etching of a limited number of commonly used materials to minimize cross-contamination concerns.

The PlasmaTherm Versalock 700 PM3 is a plasma etcher for Si, SiO_2, quartz, and silicon nitride (SiN). The process chamber uses an upper ICP section to achieve high-density ionization of process gases and an RF-biased electrode for high anisotropy.

The Xactix X2B Xenon DiFluoride Etcher is a vapor phase etcher using xenon difluoride (XeF_2) to etch Si.

The Primaxx MEMS-CET HF Vapor Etcher is a vapor-phase etcher using hydrogen fluoride (HF) to etch SiO_2.

4.2 PlasmaTherm Versalock 700 PM3

4.2.1 Model and Specifications

Model: VLR-702-PM770I-10R; March 23, 2000 (Fig. 7)

Specifications:

- Mechanical clamp (alumina ceramic): 100-mm wafers
- Process gases: SF_6, CF_4, CHF_3, O_2, Ar
- RF1 (RIE): 13.56 MHz

- RF2 (ICP): 1.72–2.1 MHz
- He backside cooling: 15 °C
- 25-wafer cassette loadlock

Fig. 7 PlasmaTherm Versalock 700 etching system

4.2.2 Materials and Processing

Materials etched: Si, SiO_2, SiN

Mask: Photoresists (AZ 5214, AZ9245, AZ 9260), Ti, Ni

Etch rate: varies, about 200 nm/min

Selectivity: varies, typically 1:1 to 1.5:1

Base recipe:

Etch: P = 5 mT, CHF_3/CF_4 = 5/15 sccm, ICP/Bias = 500/50 W, He = 2T, T = 25 °C

Processing requirements:

1) Backside of wafer must be clean. The 2-mm edge exclusion zone on the backside of the wafer must be clean and free of defects for it to seal properly on the electrode. The wafer must lie flat on the electrode; otherwise, the tool will either error-out with an He backside cooling compliance error, or the etch will be very nonuniform.

2) Through-wafer or release etches must be mounted to a dummy Si handling wafer; otherwise, the process will abort due to He compliance errors at breakthrough and debris will be left on the electrode.

4.2.3 Example Applications

- RF MEMS devices

- Etching of SiN_x in the fabrication of surface-enhanced Raman scattering substrates[6]

4.3 Xactix X2B Xenon DiFluoride Etcher

4.3.1 Model and Specifications

Model: X2B (Fig. 8)

Specifications:

- Al plate: 150-mm wafers and smaller samples
- Process gases: XeF_2
- Single wafer, manual loading

Fig. 8 Xactix X2B XeF2 etching system

4.3.2 Materials and Processing

Materials etched: Si

Mask: Photoresists (AZ 5214, AZ9245, AZ 9260), Ti, Ni

Etch rates: up to 1 µm/min

Selectivity: Nearly infinite to photoresist, SiO_2, SiN, Al

Base recipe:

Etch: 2-20-20: 2-Torr sublimation, 20-Torr expansion, 20-s etch

4.3.3 Example Applications

- Release of MEMS canterlevers
- IR bolometer suspended structure release
- Free-standing platinum (Pt) specimens for mechanical testing[7]

4.4 Primaxx MEMS-CET HF Vapor Etcher

4.4.1 Model and Specifications

Model: MEMS-CET (Fig. 9)

Specifications:

- Ceramic pins: 150-mm wafers, pocket handling wafer for smaller substrates
- Process gases: HF, ethanol, N_2
- Three-wafer, manual loading

Fig. 9 Primaxx MEMS-CET HF vapor etcher

4.4.2 Materials and Processing

Materials etched: SiO_2

Mask: Si, Ni

Etch rates: 1500 A/min

Selectivity: typically 200:1

Base recipe:

Undercut etch: P = 125 T, HF/ethanol/N_2 = 600/450/1000 sccm, 900 s

Processing requirements:

No photoresists or polymers. If material cannot withstand aqueous HF, do not put into process chamber.

4.4.3 Example Applications

- Release of MEMS devices: bolometers, cantilevers.
- Buried oxide etch and release of stators for integrated thin-film piezoelectric traveling wave motors at ARL[8]

5. Tools for Photoresist Stripping and Wafer Cleaning

5.1 Purpose

These tools generate a plasma to strip photoresist masks (typically post-etch) and for removing post-develop residues before a deposition or etch.

5.2 Axcelis 200ES Downstream Asher

5.2.1 Model and Specifications

Model: 200ES-US (Fig. 10)

Specifications:

- Quartz pins: 100-mm wafers (left cassette), 150-mm wafers (right cassette)
- End point: OES
- Process gases: O_2, CF_4, N_2H_2
- Microwave: 2450 MHz
- 25-wafer cassette loaded

Fig. 10 Axcelis 200ES Downstream Asher

5.2.2 Materials and Processing

Materials etched: photoresists (AZ 5214, AZ9245, AZ 9260)

Etch rates: varies, about 500 nm/min

Selectivity: N/A

Base recipe:

Etch: P = 1.5 T, O_2/N_2H_2 = 700/300 sccm, microwave = 1500/50 W, T = 270 °C (quartz lamp heated), t = 200 s

Processing requirements:

Backside of wafer must be clean. Wafer is supported on three quartz pins, and thermocouple contacts backside of wafer.

5.2.3 Example Applications

- Photoresist mask removal
- Descum prior to deposition or etch processes

5.3 Anatech SCE1000 Barrel Asher

5.3.1 Model and Specifications

Model: SCE1000 (Fig. 11)

Specifications:

- Quartz tray: 200-mm wafers and smaller
- Process gases: O_2, CF_4, CHF_3
- RF: 13.56 MHz
- Manual loading

Fig. 11 Anatech SCE1000 Barrel Asher

5.3.2 Materials and Processing

Materials etched: SiO_2, photoresists (AZ 5214, AZ9245, AZ 9260)

Etch rates: varies, about 20 nm/min

Selectivity: N/A

Base recipe:

Etch: P = 1T, O_2 = 200 sccm, RF = 200 W

Processing requirements: N/A

5.3.3 Example Applications

- O_2 descum

5.4 UVOCS Ozone Cleaner

5.4.1 Model and Specifications

Model: T10X10-OES (Fig. 12)

Specifications:

- Steel tray: 250 mm
- Process gases: ambient air
- UV lamps

Fig. 12 UVOCS ozone cleaner

5.4.2 Materials and Processing

Materials etched: carbon-based residues

Etch rates: varies, about 2 nm/min

Selectivity: N/A

Base recipe: quartz ozone generator has no user inputs

Etch: t = 60 s

Processing requirements:

No toxic substances

5.4.3 Example Applications

- Descum
- Surface treatment

5.5 PVA Tepla Ion 40

5.5.1 Model and Specifications

Model: IoN 40 (Fig. 13)

Specifications:

- Al trays: five trays, each handles up to 200-mm substrates
- Gases: O_2, CF_4, CHF_3, N_2
- RF: 13.56 MHz

Fig. 13 PVA Tepla Ion 40

5.5.2 Materials and Processing

Materials etched: photoresists (AZ 5214, AZ9245, AZ 9260)

Etch rates: varies, up to 500 nm/min

Selectivity: N/A

Base recipe:

Etch: P = 1T, O_2 = 200 sccm, RF = 500 W, t = 20 min

Processing requirements:

Bottom of wafer must be clean and not leave residues on wafer trays.

5.5.3 Example Applications

- Photoresist strip
- Descum
- Surface activation

5.6 PVA Tepla Ion Wave 10

5.6.1 Model and Specifications

Model: IoN Wave 10 (Fig. 14)

Specifications:

- Al tray (cooled): up to 200-mm substrate
- Gases: O_2, CF_4, CHF_3, N_2
- Microwave: 2450 MHz

Fig. 14 PVA Tepla Ion Wave 10

5.6.2 Materials and Processing

Materials etched: photoresists (AZ 5214, AZ9245, AZ 9260), SU-8

Etch rates: varies, about 200 nm/min

Selectivity: N/A

Base recipe:

Etch: P = 5 mT, CHF_3/CF_4 = 5/15 sccm, ICP/Bias = 500/50 W, He = 2T, T = 25 °C

Processing requirements: N/A

5.6.3 Example Applications

- SU-8 ashing
- Temperature-sensitive device processing

6. Tools for Etching PZT and Metals

6.1 Purpose

This tool removes materials via ion milling, using inert Ar atoms to physically bombard and sputter-off materials. When Ar is used as the source gas, the etch is purely physical as opposed to other etch tools at ARL in which the plasma generated uses both a chemical and physical component to etch various materials. Ion milling is typically used if there is not a plasma gas chemistry available to etch the material. Selectivity between the mask and the material to be etched is typically lower than using plasma etching. Typical masks are photoresist and "hard" metal masks such as Ni or chromium. Because of the physical nature of ion milling, this tool generally creates greater surface damage on the etched surface than an etch using a gas plasma with a chemical etch component.

6.2 4Wave Planetary Stage Ion Beam Etcher (PSIBE)

6.2.1 Model and Specifications

Model: 4W-PSIBE (Fig. 15)

Specifications:

- Mechanical clamp (stainless): 150-mm wafers, with ring inserts for 100-mm wafers
- Three platens, planetary stage
- End point: Hiden mass spectrometer
- Gases: Ar, CF_4, O_2, or N_2

Fig. 15 4Wave PSIBE

6.2.2 Materials and Processing

Materials etched: PZT, BST, Ti, Pt, Ni, gold, ruthenium, chromium, SiO_2 (nonvolatile materials)

Mask: photoresists (AZ 5214, AZ9245, AZ 9260), Ti, Ni

Etch rates: 50–900 A/min (estimate using sputter yield of material)

Selectivity: typically 1:1

Base recipe: Vbeam = 650 V; Ibeam = 700 mA, Vacc = 195 V, Ar = 20.85 sccm, angle = 95°, stage rotation = 5 rpm

6.2.3 Example Applications

- Contact beams in piezoelectric actuators at ARL[9]
- Multilayer films with end-pointing on specific layer

7. 10-Year Plan

The following are recommendations and justifications for future acquisition and expansion of dry-etch processing tools at ARL's SEMASC Cleanroom Research Facility.

- Cross contamination control. Additional tools and/or process chambers to allow dedication of chambers for particular etches. Residues from etching one material can be detrimental to the process for etching another material. The etch used for quantum well IR photodetector devices is one example at ARL. A wet clean of the chamber (exposed to toxic materials) after approximately 10 h of dry etching is required to restore etch rates and selectivity for particular processes.
- Load lock systems. Anytime a chamber is vented to atmosphere, the conditioning of the chamber is affected and will impact process control. In addition, a load lock minimizes user exposure to hazardous materials.
- Integrated process control and diagnostics: OES, residual gas analyzer, and mass spectrometer. These are essential to monitor a process chamber to detect process drifts due to the wide variety of materials introduced to research equipment.
- Additional tools to accommodate the numerous substrate form factors. This will reduce downtimes required to swap fixturing for each user need and variation of process conditioning each time the process chamber is vented.

- Atomic layer etching tools. These will be needed to controllably remove the very thin layers of new devices. Current tooling was designed for high-speed manufacturing and high etch rates. Newer applications require removal rates of atomic layers per second.
- Flexibility and capability. Tools with expanded gas-delivery cabinets provide additional gas-chemistry options for the researchers and extend the usefulness of the tools.

8. Conclusion

A review of the current dry-etching equipment available at ARL's SEMASC cleanroom was presented. For applicability to your particular program or project, you are encouraged to contact the point of contact for the tools. Tool modifications are made on a continuing basis to accommodate the many users of the cleanroom.

9. References

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List of Symbols, Abbreviations, and Acronyms

Al	aluminum
Ar	argon
ARL	Army Research Laboratory
CHF_3	fluoroform or trifluoromethane
Dep	deposition
DEVCOM	US Army Combat Capabilities Development Command
DSE	deep silicon etcher
echuck	electrostatic chuck
GaN	gallium nitride
H_2	hydrogen
HF	hydrogen fluoride
ICP	inductively coupled plasma
IR	infrared
ISM	inductively super magnetron
mT	milliTorr
Ni	nickel
O_2	oxygen
OES	optical emission spectroscopy
PSIBE	planetary stage ion beam etcher
Pt	platinum
PZT	lead zirconate titanate
RF	radio frequency
RIE	reactive ion etching
sccm	standard cubic centimeters per minute
SEMASC	Specialty Electronic Materials and Sensors Cleanroom
SF_6	sulfur hexaflouride
Si	silicon
SiC	silicon carbide

SiO_2	silicon dioxide
SOI	silicon on insulator
Ti	titanium
TSV	through silicon via
UV	ultraviolet
XeF_2	xenon fluoride

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