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MILLIMETER-WAVE DIGITAL ARRAYS TILES OF UNRELEASED CLOCKS FOR HYBRID ELECTRONIC STEERING (MIDAS TOUCHES)

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Purdue University

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14. ABSTRACT
The techniques of beamforming and null-steering using antenna arrays increase the effective radiated energy density at the transmitter, while improving the sensitivity, interference tolerance, spatial selectivity at the receiver through tunable high directivity. Digital Arrays enable efficient simultaneous multiple beams, opening many unique applications. However, digital mm-wave arrays call for (1) per-channel Gbps ADC, (2) full transmit (Tx) and receive (Rx) mm-wave front-ends(FE) per-channel, and (3) need for high-frequency clock at each channel location, each of which makes mm-wave digital arrays prohibitively power hungry. With recent advances in unreleased fin oscillators from Co-PIs lab, we analyzed different topologies of oscillator design using on-chip, high-Q CMOS/MEMS hybrid resonators (resonant fin transistors (RFTs), and resonant body diodes (RBDs)). We analyze the best phase noise performance by aligning the resonances of motional branch and static capacitance compensatory network in the same directions, thereby achieving <-120dBc/Hz phase noise at 10kHz offset (Q of RFT = 10,000) for all the topologies. Among the topologies discussed, design 3 achieves best performance for passive RFT topologies (<-120dBc/Hz phase noise at 10kHz offset, 208dB FOM), while design 6 achieves the best performance for active RFT topologies (<-140dBc/Hz phase noise at 10kHz offset, 220dB FOM).

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1 SUMMARY OF THE PROGRESS

The techniques of beamforming and null-steering using antenna arrays increase the effective radiated energy density at the transmitter, while improving the sensitivity, interference tolerance, spatial selectivity at the receiver through tunable high directivity. Digital Arrays enable efficient simultaneous multiple beams, opening many unique applications. However, digital mm-wave arrays call for (1) per-channel Gbps ADC (2) full transmit (Tx) and receive (Rx) mm-wave front-ends (FE) per- channel and (3) need for high-frequency clock at each channel location, each of which makes mm-wave digital arrays prohibitively power hungry. With recent advances in unreleased fin oscillators from Co-PIs lab, and lowest-power Gbps samplers and mixer-first receivers from PIs lab, the TOUCHES team proposed clock generation circuitry for an mm-wavedigitally-tunable receiver with High-Q hybrid complementary metal-oxide semiconductor- microelectromechanical (CMOS-MEMS) oscillator (HQCO) based per-channel clock generation.

Figure 1 shows the timeline of the TOUCHES program for micro-scale device array structure (MIDAS) phase-1 (Nov 2018 – Mar 2020). Fundamental Design Explorations were performed for oscillators with active and passive versions of resonant fin transistor (RFT) based resonator in GF 14nm technology and resonant body diodes (RBD) in TSMC 65nm technology. The 14nm RFT and 65nm RBD designs were improved for cleaner modes.

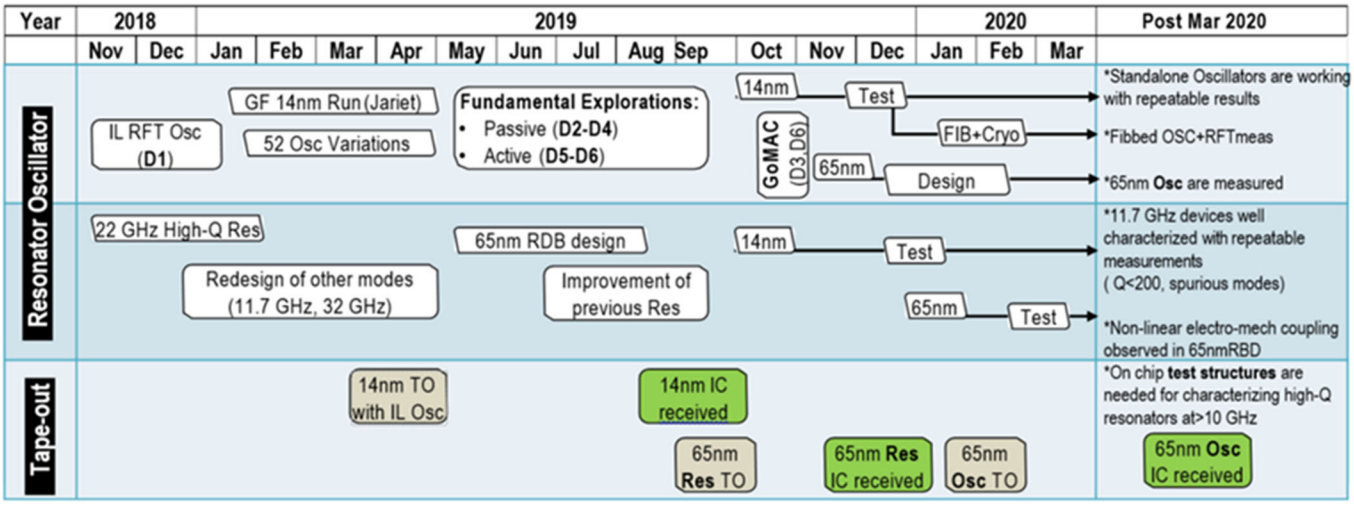


Figure 1: MIDAS TOUCHES Timeline

Nov 2018-Mar 2020: Fundamental Design Explorations were performed for Oscillators with active and passive versions of Resonant Fin Transistor (RFT) based resonator in GF 14nm Technology

1.1 Significant Accomplishments Achieved:

- Analyzed, simulated and designed RFTs using GF 14nm FinFET technology.
- Analyzed, simulated and designed RBDs using TSMC 65nm technology.
- Analyzed, simulated and designed active oscillator circuits using GF 14nm RFTs and

Taiwan semiconductor corporation (TSMC) 65nm RBDs, and analyzed the design trade-offs along with resonator Q requirements to achieve best phase noise.

- Analyzed the best phase noise performance by aligning the resonances of motional branch and static capacitance compensatory network in the same directions, thereby achieving <-120dBc/Hz phase noise at 10kHz offset (Q of RFT = 10,000) for all the Oscillator topologies. Among the topologies discussed, design 3 achieves best performance for passive RFT topologies (<-120dBc/Hz phase noise at 10kHz offset, 208dB FOM), while design 6 achieves the best performance for active RFT topologies (<-140dBc/Hz phase noise at 10kHz offset, 220dB FOM).

1.2 Technical Approach: Design of High-Q RFTs and RBDs

Low phase noise clocks are a critical component to the performance of MIDAS. With array scaling in mind, we propose to replace commonly used Quartz crystal phase-locked-loop (PLL)-based oscillators with monolithically integrated oscillators in standard CMOS. Leveraging the high Q (>1,000) and high frequency (10-40 gigahertz (GHz) of CMOS-MEMS resonators recently demonstrated by PI Weinstein in 14nm FinFET technology, we developed oscillator design methodologies to generate clocks for the system.

1.2.1 High-Q GHz CMOS Resonators

Two different types of CMOS resonators are designed: a) RFTs in GF 14nm FinFET technology, and b) RBDs in TSMC 65nm Bulk CMOS technology.

1.2.2 RFTs in GF 14nm FinFET Technology

Over the past several years, PI Weinstein has developed a class of GHz frequency Microelectromechanical (MEM) resonators embedded seamlessly within CMOS [1]–[5]. These devices use electrostatic (MOSCAP) drive leveraging the gate dielectric to launch acoustic waves within the CMOS stack and sense their vibrations by the time-varying stress induced in a transistor. Transistor sensing is used to internally amplify the acoustic signal over the electrical parasitic floor, improving direct electrical pick-off of the mechanical signature. These so-called RBTs benefit from high Q, high frequency, and seamless integration with CMOS. These devices are unreleased, defined only using the acoustic impedance mismatches of the different layers available in the CMOS stack. Unlike other CMOS-MEMS resonators, there is no post-processing to the standard CMOS process. Recently, Weinstein's group demonstrated the first RBTs in GLOBALFOUNDRIES 14nm FinFET technology, with quality factor (Q~1000), and electromechanical transconductance (g_{mech}~3-6 μS measured).

As can be seen in the simulated phononic dispersion relation for the GF 14LPP CMOS stack in Figure 2, a guided mode exists with excellent vertical confinement and stress localized at the fins. Any disruption or perturbation to the RFT structure (lateral periodicity) induces scattering and reduces the quality factor of the device. For this reason, the gate has to be continuous and common between the driving MOSCAPs and sensing FET. However, we use abrupt termination of the fins at the edges of the device to provide strong reflections along the horizontal waveguide. With a shared gate, the drive and sense signals are accessed through the source and drain of the FinFETs.

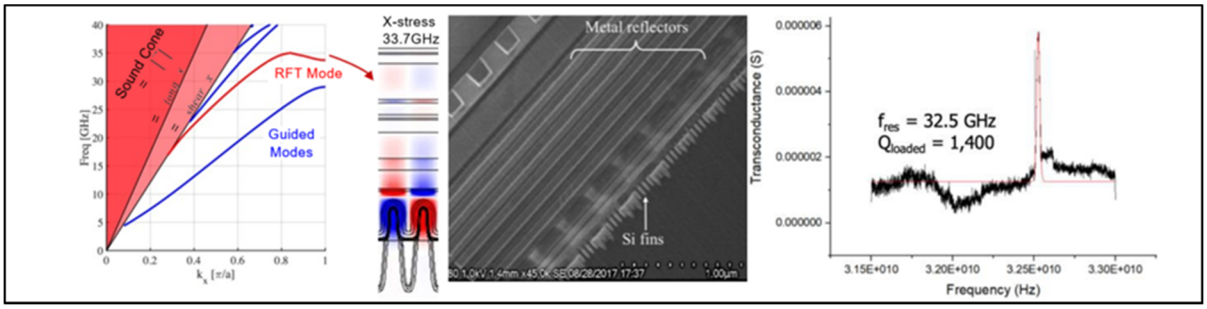


Figure 2: Dispersion Relation and Mode Shape (left), SEM Cross Section (middle), and Measured Frequency Response of Resonant Fin Transistor (RFT)

Though the 32 GHz mode describes the fundamental resonance along the fin width, other high Q modes have also been shown with small modifications to the device design at 10 and 40 GHz. It should be noted that the electro-mechanical transconductance of the 10 GHz mode reaches as high as $g_{mech} = Y_{dd21}-Y_{dd12} = 1.5$ S. Such large output signal translates to lower power, smaller footprint oscillators leveraging the active nature of the RFT.

Measurements of resonators designed to operate around 10 GHz from previous tapeouts revealed that the measured Q-factor was lower and that there was a spurious mode located close to the targeted resonance frequency which causes a broadening of the resonance peak. To alleviate these issues a new generation of devices were designed. The new resonators operating at frequencies ranging from 18 GHz to 21 GHz were designed to obtain a higher Q (Figure 3), suppress the spurious modes and lower the electrical parasitics to the devices. For a gate length of 52 nm, upon performing a 3D FEM based modalanalysis, modes of interest were identified out of which the mode at 21.273 GHz exhibited the highest stress levels in the fin region of the device. As can be seen in Figure 3, the mode 3 exhibits the highest y-stress levels in the fin region and hence this mode is chosen. The targeted mode also shows that no spurious mechanical resonances are located in the vicinity of the main resonance peak. The 21 GHz devices owing to higher stress (hence higher transconductance) as well as higher expected Q-factor were the prime candidates for the oscillator designs. Besides the new design for the 21 GHz resonator, a second design with gate length 16 nm was developed with an operating frequency of 18.4 GHz to assess the effect of back –end-of-line (BEOL) metal PnCs on the spurious modes that were seen in previously designed resonators. The expected maximum Q-factor for this topology was lower (2000) than the high-performance resonators designed at 21 GHz.

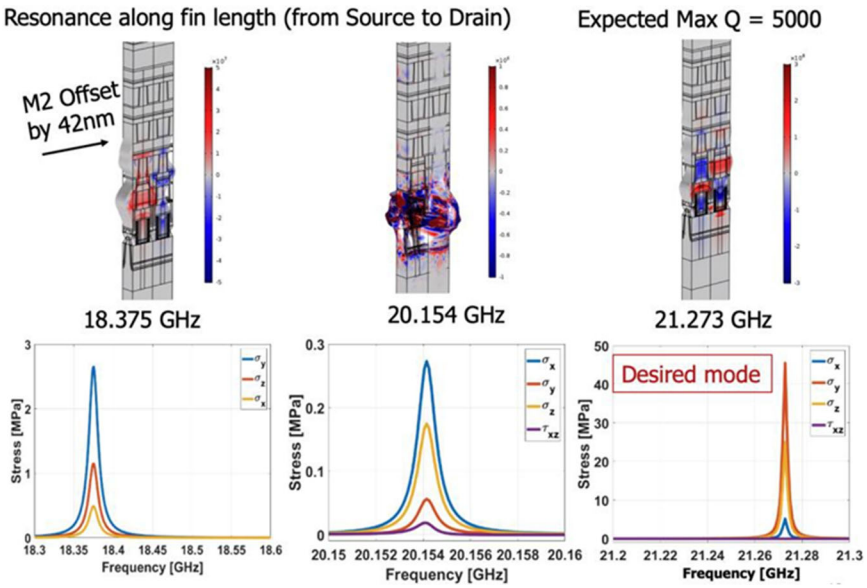


Figure 3: 3D-FEM Simulation Results of Resonators with Gate Length of 52nm showing that the Desired Targeted Mode has a Higher Energy Confinement and Hence Transconductance along with Higher Q-factor

The measurement of the devices was made complicated due the presence of solder bumps which are not amenable to radio frequency (RF) probe landings. In order to conduct reliable measurements on the chips containing the resonators the solder bumps were polished down so as to be able to have a sufficiently flat surface for probe landings. Subsequently 4-port measurements were conducted on the 10 GHz devices on the chip. From the measurements of the resonator transconductance as seen in Figure 4 it can be observed that only the resonators containing the BEOL PnC reflectors exhibit an observable resonance while the ones with plates as reflected show no detectable resonance. Also, the presence of spurious resonance peaks close to the targeted resonance peak can be seen.

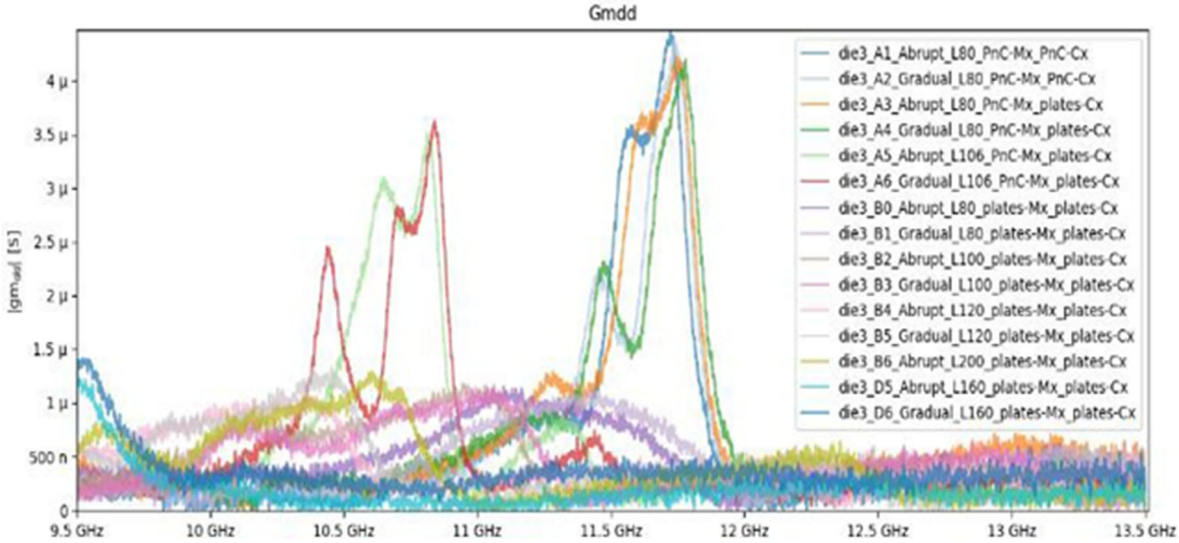


Figure 4: RF-measurement Results of the Transconductance for Resonators Designed to Operate in the Vicinity of 10-11GHz

Measurement of the 21 GHz devices under regular testing conditions showed the presence of a peak but due to the presence of S-parameter measurement inconsistencies and issues with repeatability alternate measurement techniques were considered. Significant effort was dedicated towards detecting the resonance in the 21 GHz resonance mode devices using these alternate methodologies. Mixing measurements were conducted so as to separate the mechanical resonance current from the parasitic current in frequency to make the peak visible. However, mixing measurements at the required high frequencies did not yield satisfactory results and the resonance was not observed. Subsequently, cryogenic measurements were conducted at 78K in a 2-port configuration to enhance the Q-factor of the resonator. From the measured results (Figure 5) it can be seen that a peak at a frequency of 22.59 GHz with a Q of ~860 was observed. This affirms the presence of a mechanical resonance which gets swamped by the presence of parasitic electrical resistances at the room temperature.

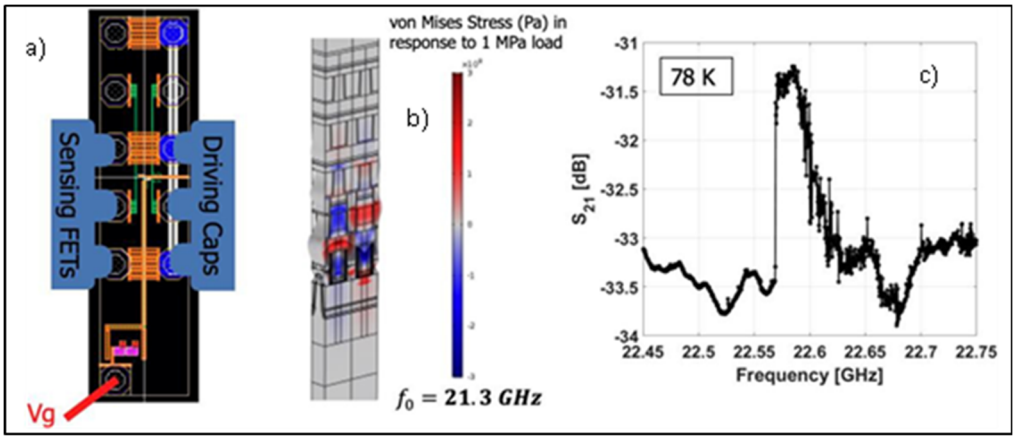


Figure 5: Measurement Scheme for the Two-power cryogenic RF Measurement of the 21 GHz Resonator

Targeted mod shape of the 21 GHz Resonator (a), (b) and (c) Measured S21 for the resonator showing a peak at 22.59 GHz with a Q of ~860

1.2.3 RBDs in TSMC 65nm Technology

As an alternative to the resonators designed in the 14 nm Global foundries process, which have a significantly higher trap-assisted tunneling (TAT), resonators based on P-type/N-type (PN) diode transduction were designed in the TSMC 65 nm process. The main principle behind these devices is to use the force between depletion layer charges of a PN junction to induce vibrations in a resonator structure along with sensing the modulation in diode current due to the induced vibrations.

As can be seen from the 2D simulation of the unit cell in the resonator (Figure 6), the Tungsten via contacting the diode is the region where the maximum stress is localized within the resonator for Mode 1, occurring at 3.214 GHz. The stress in the junction region of the diode is sufficiently high to create an efficient transduction scheme.

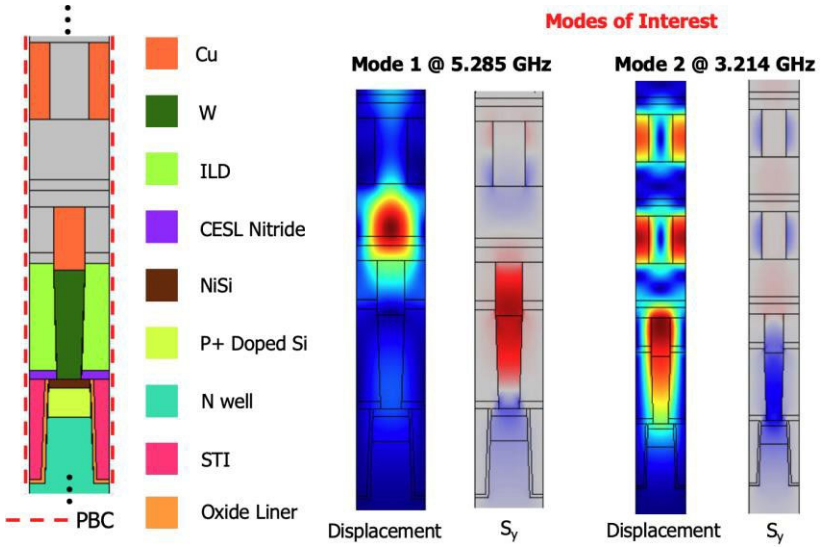


Figure 6: 2D-FEM Simulation Results showing the Targeted Modes of the PN-Diode Resonators Designed in the TSMC 65nm Process

Similarly, Mode 2 occurring at a higher frequency of 5.285 GHz is found that has stress concentration further away from the diode region. To enhance the stress in the region of interest for Mode 1, a staggered PnC having a higher band-gap was designed which is offset from the diode positions. As can be seen in Figure 7, this results in a better confinement of the mode towards the diode region with a low amount of energy percolating into the BEOL metal PnCs. A study of frequency sweep was conducted on a full PN diode resonator model showed high stress levels at the PN junction region (Figure. 7). The phononic crystal constructed out of the BEOL metals from M2 to M7 was designed specifically to confine the vibrations in the diode region.

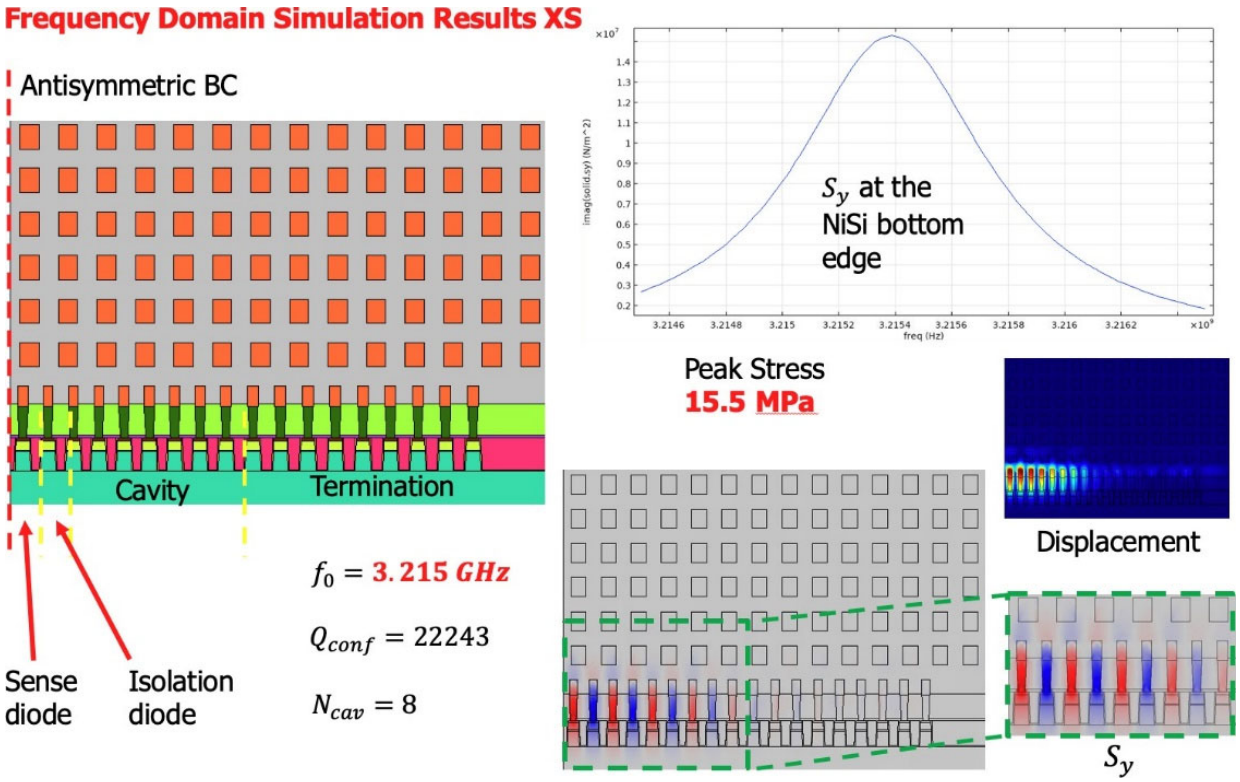


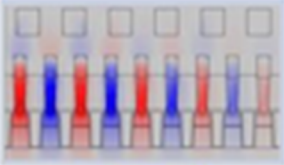
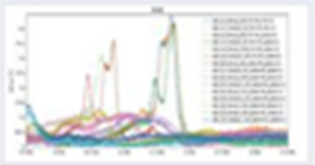
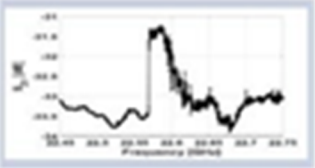
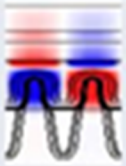
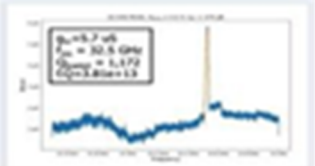
Figure 7: 2D-FEM Frequency Domain Simulation Results showing the Targeted Modes of the PN-Diode Resonator along with the Stress Levels at the PN Diode Junction

In order to create a cavity, unit cells having a lattice constant different from the lattice constant in the cavity are used as terminations. As can be seen in the displacement plot in Figure 7, the mode decays in amplitude inside the termination showing that the termination design is effective.

The measured S-parameter response in Figure 8 for appropriately biased drive and sense diodes shows multiple peaks owing to the coupling of the mechanical resonance to the nonlinear transduction of the diodes. It is also observed that the response of the device is unidirectional which is as expected. The response obtained for the RBD devices is not suitable for the oscillator operation because of the presence of multiple peaks in the spectrum and efforts are required to be made to linearize the transduction.

Table I shows a compilation of the various devices that have been designed as well as measured. RBT devices in 14 nm FinFET technology have been demonstrated that operate at frequencies suitable for mmWave operation. PN diode based RBD devices on the other hand operate at a lower frequency but have a faster TAT. It is possible to attain higher Q values in the RBD devices through the use of adiabatic terminations to minimize radiative losses. More work is required to be done to completely eliminate spurious responses in the RBT devices. Measurement challenges exist due to the presence of substrate and capacitive coupling, electrostatic discharge (ESD) diode loading and transistor mismatch resulting in mode conversion loss. These challenges however do not exist for resonators embedded in-situ with the oscillator circuitry since the measurement fixture is eliminated.

Table 1. Different Resonators Designed in Planar as well as FinFET Processes located in Different Frequency Bands along with the Corresponding Mode Shapes

Technology	Resonance Frequency	Resonance Mode	Measured Response
TSMC 65nm	3.27 GHz		
GF 14LPP	11.7 GHz		
	22.7 GHz		
	32 GHz		

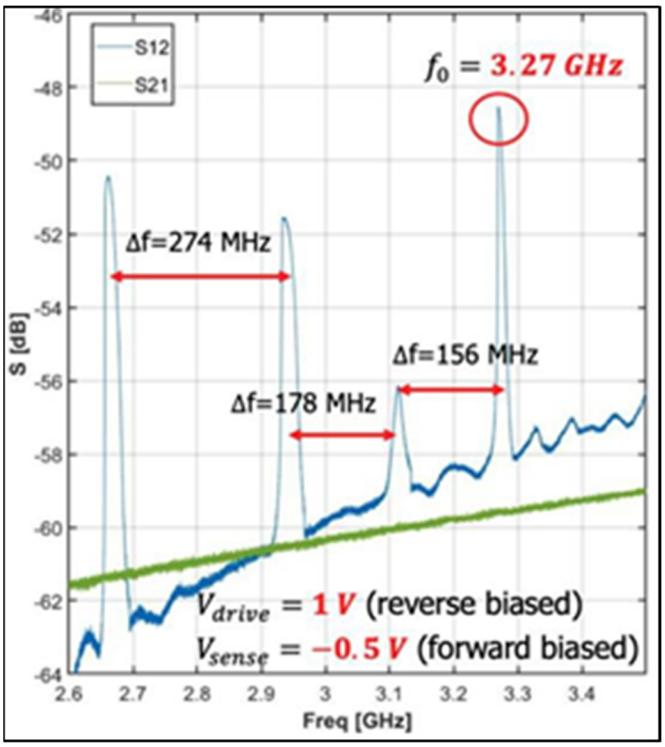


Figure 8: Measured 2-port S-parameters for a PN Diode Resonator showing Multiple Resonance Peaks Arising out of Nonlinear Coupling of the Diode Transduction with the Mechanical Resonance Resulting in Multiple Resonance Peaks along with the Targeted Peak at 3.27 GHz

1.3 Technical Approach: Design of High-Q Oscillators

High-Q CMOS oscillators are designed to generate stable GHz clock references with low-power and low phase noise. The implemented oscillator topologies are shown in Figure 9.

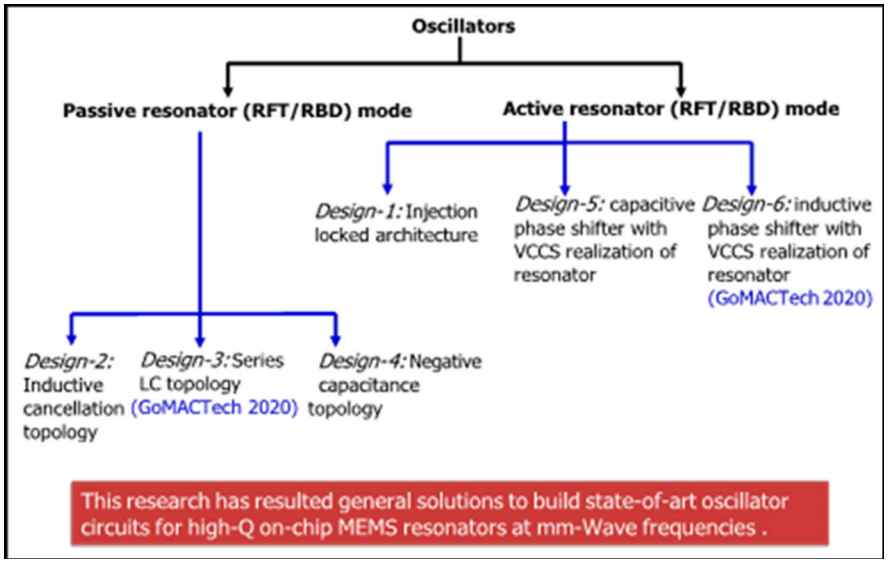


Figure 9: Proposed Oscillator Designs with High Q RFT/RBDs

The designs are divided into passive and active resonator modes based on the type of resonator used. Design 1 is an injection-locked Inductor/Capacitor (LC) cross-coupled (X-coupled) oscillator for which an on-chip LC oscillator drives the on-chip active RFT, the output of which is used to injection-lock the oscillator. Design 2 uses an inductive cancellation topology in which the large parallel capacitance (C_0) for the passive RFT is cancelled using an inductor. Design 3 implements a series LC oscillator topology to leverage the motional inductance and the motional series capacitance in the RFT. A proof-of-concept passive LC oscillator is also designed along with the RFT based design. Design 4 uses a negative-capacitor based cancellation topology in which the large parallel capacitance (C_0) for the passive RFT is cancelled using an active inductor/negative capacitor. Finally, realizing that the RFT/RBD in active mode has a phase shift of 270°, in designs 5 and 6, we implement a capacitive phase shifter and an inductive phase shifter, respectively, to account for an additional 90° phase shift, thereby creating a total phase shift of 360°, creating sustained oscillations in the loop. Table 2 shows the summary of the designs implemented.

Table 2. Summary of the Oscillator Designs

All the designs achieve a PN < -120dBc/Hz at 10kHz offset with RFT's Q assumed to be = 10,000

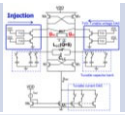
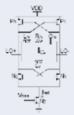
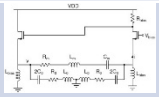
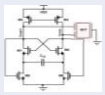
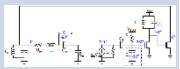
Design	Feature	Snapshot	Frequency	Phase noise@1MHz (dBc/Hz)		Power (mW)	FoM (dB)	
				Q_{RFT}=1K	Q_{RFT}=10K		Q_{RFT}=1K	Q_{RFT}=10K
Design-1 (Active)	Injection locked oscillator for active mode of RFT		21 GHz	-112	-123	9	188	199
Design-2 (Passive)	Inductive cancellation of C_0		21 GHz	-110	-130	8.3	185	205
Design-3 (Passive)	Series LC topology		21 GHz	-115	-130	6.4	193	208
Design-4 (Passive)	Negative capacitance		11.55 GHz	-119	-127	0.9	201	211
Design-5 (Active)	Capacitive phase shifter		21 GHz	<-125	<-140	5.6	204	219
Design-6 (Active)	Inductive phase shifter		21 GHz	<-125	<-140	4.8	205	220

Figure 10 shows the oscillator design 1 in detail. The on-chip LC oscillator drives the on-chip RFT, the output of which is used to injection-lock the LC oscillator. Frequency pulling through injection is observed in the frequency range of 16-30 GHz, with >30dB improvement in phase noise.

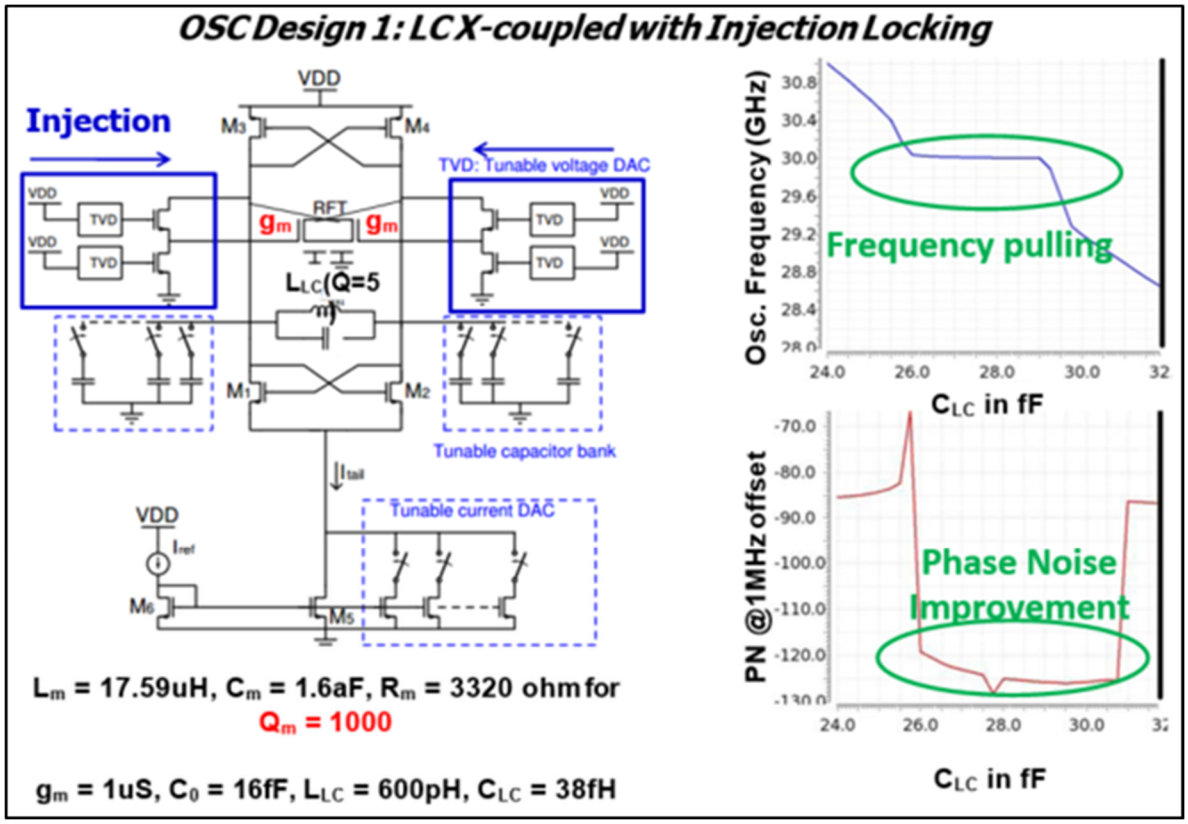


Figure 10: Oscillator Design 1

Active RFT, 10-30GHz LC X-coupled design methodology with injection locking: The on-chip LC oscillator drives the on-chip RFT, the output of which is used to injection-lock the oscillator.

Figure 11 shows the layout of the oscillator in an array of 52 oscillators.

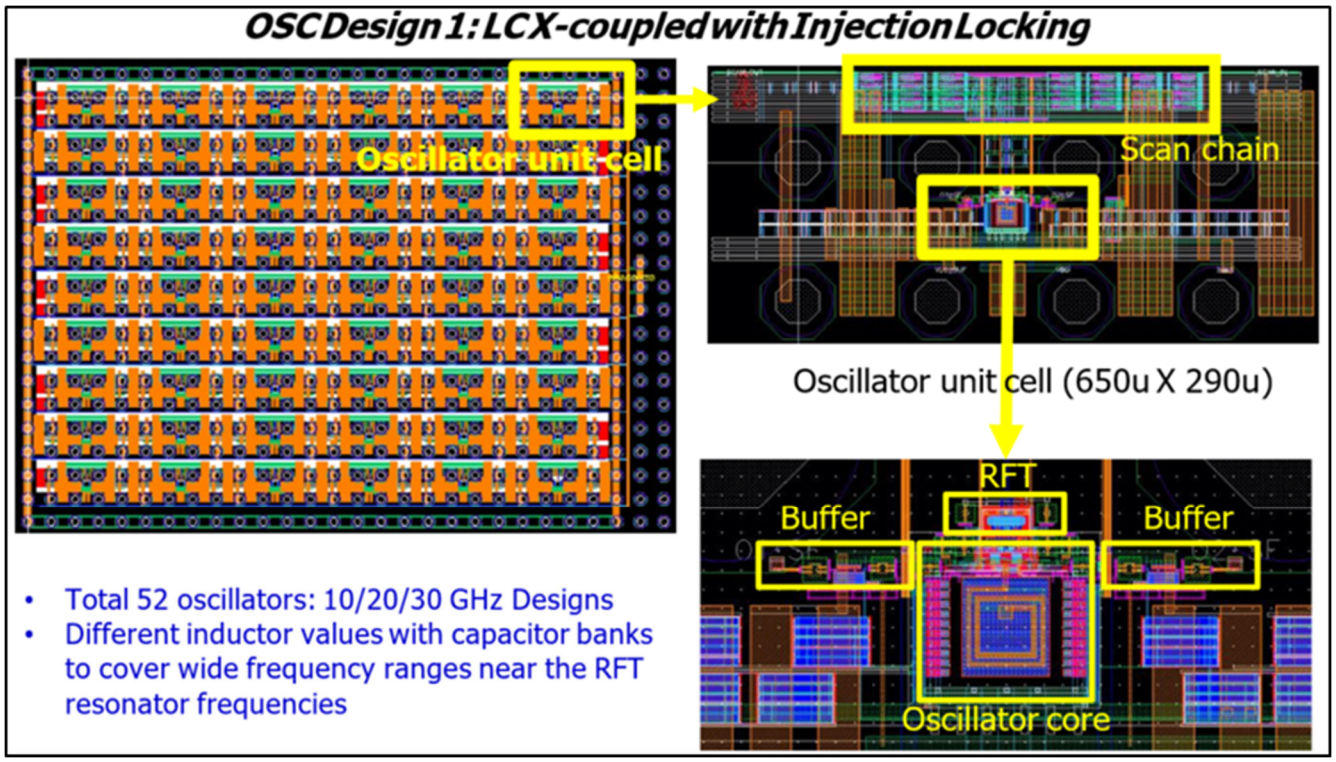


Figure 11: Oscillator Design 1

Active RFT, 10-30GHz LC X-coupled design methodology with injection locking: The on-chip LC oscillator drives the on-chip RFT, the output of which is used to injection-lock the oscillator. The layout with a total of 52 Oscillators is shown.

Figure 12 shows the measurement results for design 1. With a probe-station setup, -76dBc/Hz phase noise is observed at 1MHz offset for a 21GHz oscillator. However, by sweeping the frequency of the LC-oscillator (through an on-chip reconfigurable capacitor bank), no frequency-pulling/improvement in phase noise is observed as it was observed in simulation. Upon further investigation, we found a biasing issue at the input sense/driven ports of the RFT. The AC coupling capacitors used had biased the RFT near 0 voltage. To resolve this issue, we tried shorting the AC coupling capacitors using a focused ion beam (FIB) based etching and metallization in our in-house facility. However, this method of metallization usually results in 100s of ohms to a few kilo- ohms of series resistance between the two points which are shorted. As a result, the effective loaded Q of the RFT is reduced significantly, and we do not observe any significant effect of the injection locking (even in simulation, with a 100 ohm series resistance replacing the capacitors). However, an increase in current from 5mA to 7mA signifies that the RFT starts drawing current because of correct biasing. This biasing issue will be resolved in one of the future tape-outs to understand the effects of RFT better on the LC-oscillator through the injection locking mechanism.

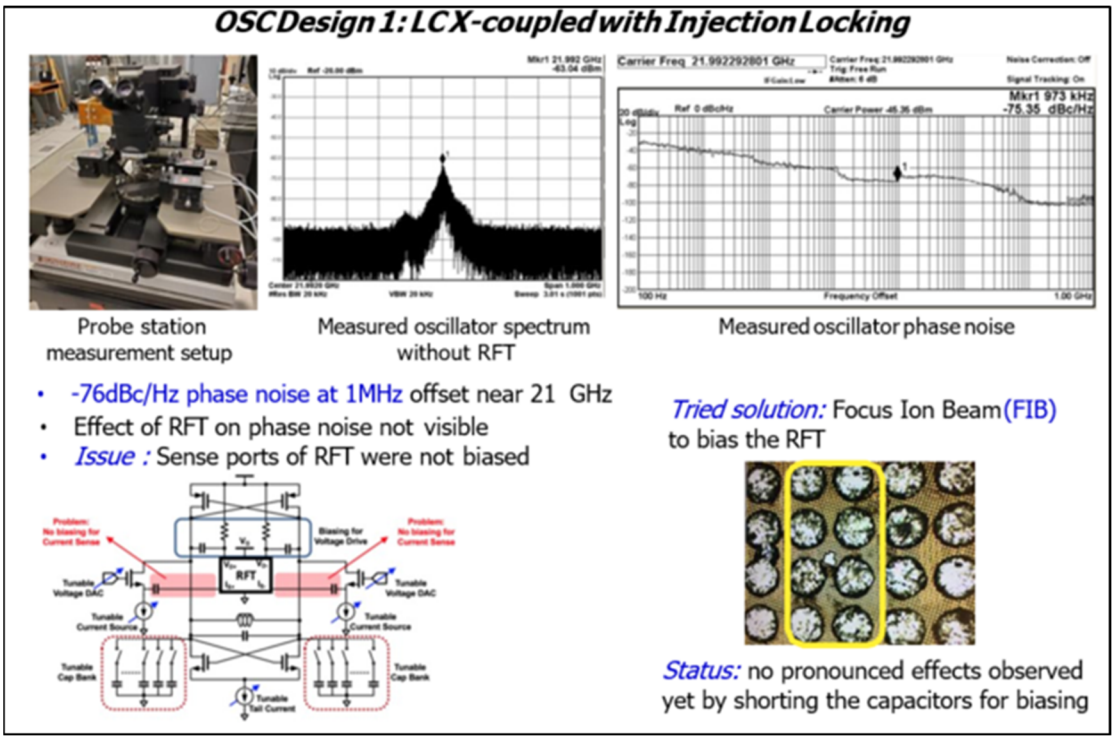


Figure 12: Measurement results for Oscillator Design 1
Active RFT, 10-30GHz: LC X-coupled design methodology with injection

One of the major challenges in the RFT arises due to the large parallel capacitance, C_0 (shown in the equivalent Butterworth- Van Dyke model of the RFT in Figure 13), which provides a low impedance parallel path for the driving current at high frequencies for the RFT. In other words, a significant portion of the driving current takes the parallel path through C_0, instead of taking the motional path. This is described as the 'low X_{C0}/R_m' issue in [6]. To circumvent this issue, we can cancel C_0 either using a parallel inductor (design 2, Figure 13) or a parallel negative capacitor (design 4, Figure 16). From simulation of design 2 (Figure 13), it is observed that the Q of the RFT needs to be > 4000 so that the effect of loading with the additional components is minimized. This signifies the importance of the RFT having a Q of a few thousands or more. Design 4 (Figure 16) shows a method of cancelling C_0 with active inductance, for scenarios when the output swing of the oscillator is low. For large-signal operations, however, active inductance would lead to non-linear effects and cause spurious peaks in the frequency domain. One major drawback in designs 2 and 4 is that Q is maximized at the cost of minimizing the carrier power (since the parallel external LC resonance and the series motional resonance internal to the RFT work in opposite directions). This hurts the overall phase noise. To solve this problem, in design 3 (Figure 14), we propose and implement a series LC-based design which aligns the resonances of the internal and external components of the RFT. However, this design requires a modification in the resonator design (the internal ground needs to be taken out so that external components can be connected). As a proof- of-concept demonstration, the series-LC oscillator (without the RFT, just the positive-feedback gain stages with external components) is taped-out in TSMC 65nm technology and is measured (Figure 15). Excellent conformity between the simulated and measured numbers are observed in terms of the frequency of operation, power consumption and phase noise performance.

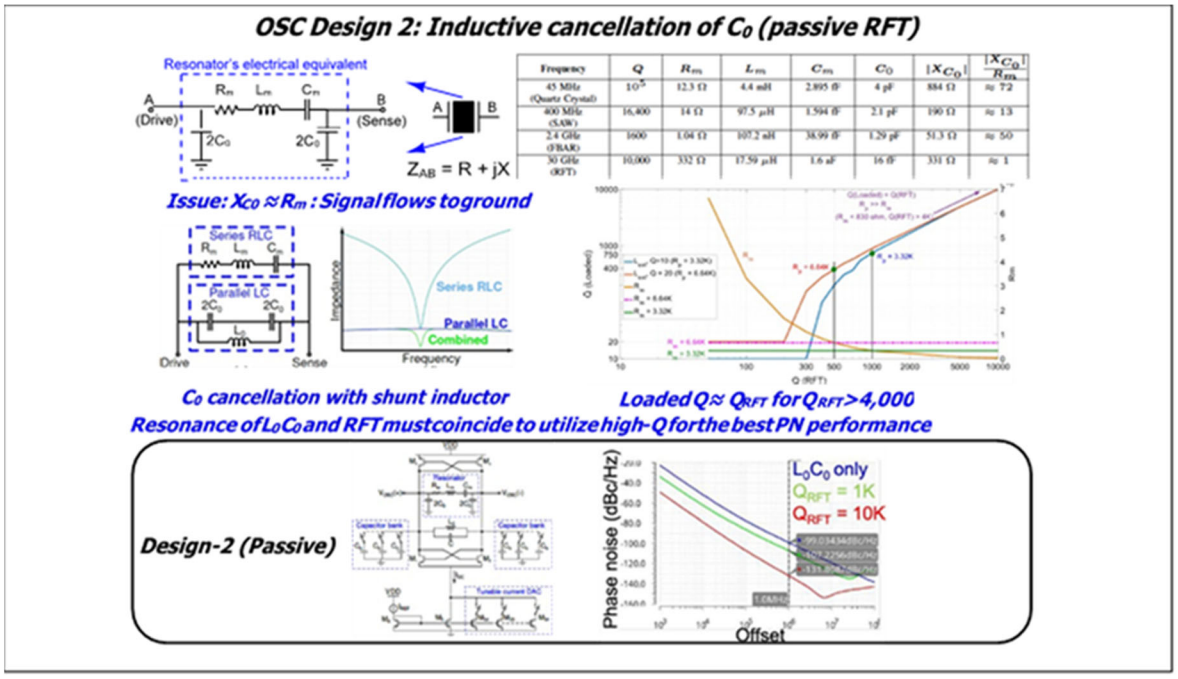


Figure 13: Oscillator Design 2

Passive RFT, 10-30GHz: inductive cancellation of the high C_0, to solve the low X_{C0}/R_m issue.

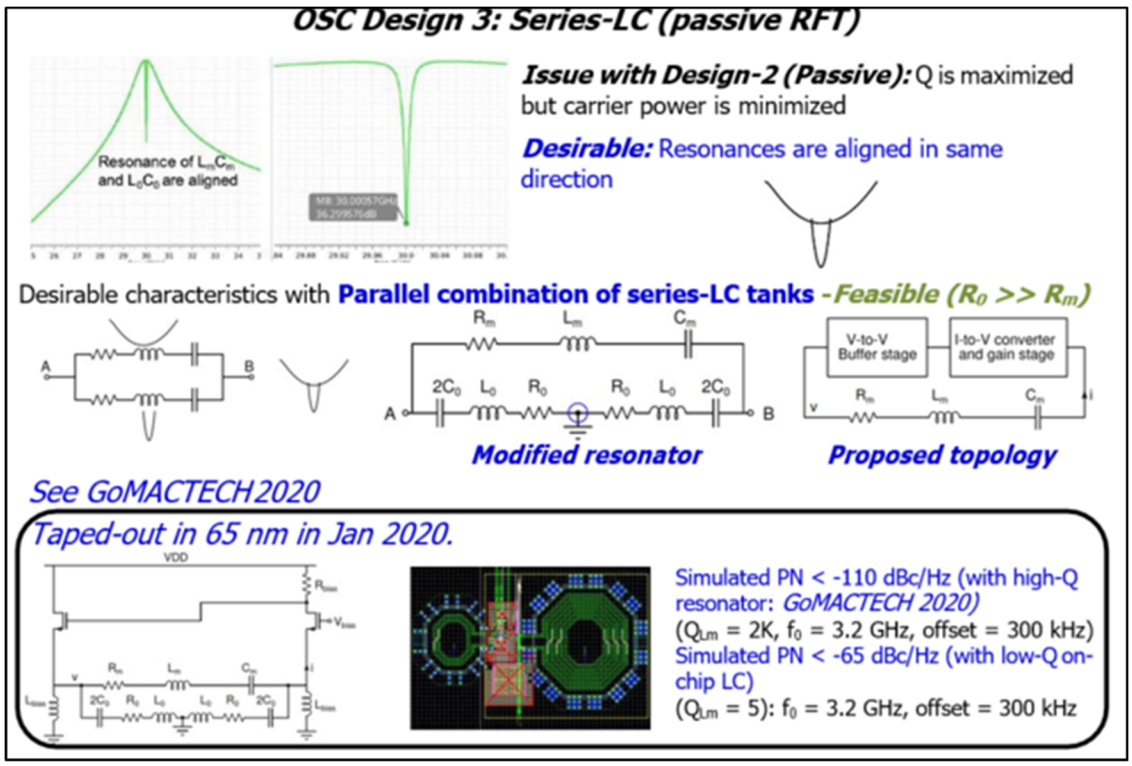


Figure 14: Oscillator Design 3

Passive RFT, 10-30GHz: series LC topology to maximize both Q and carrier power.

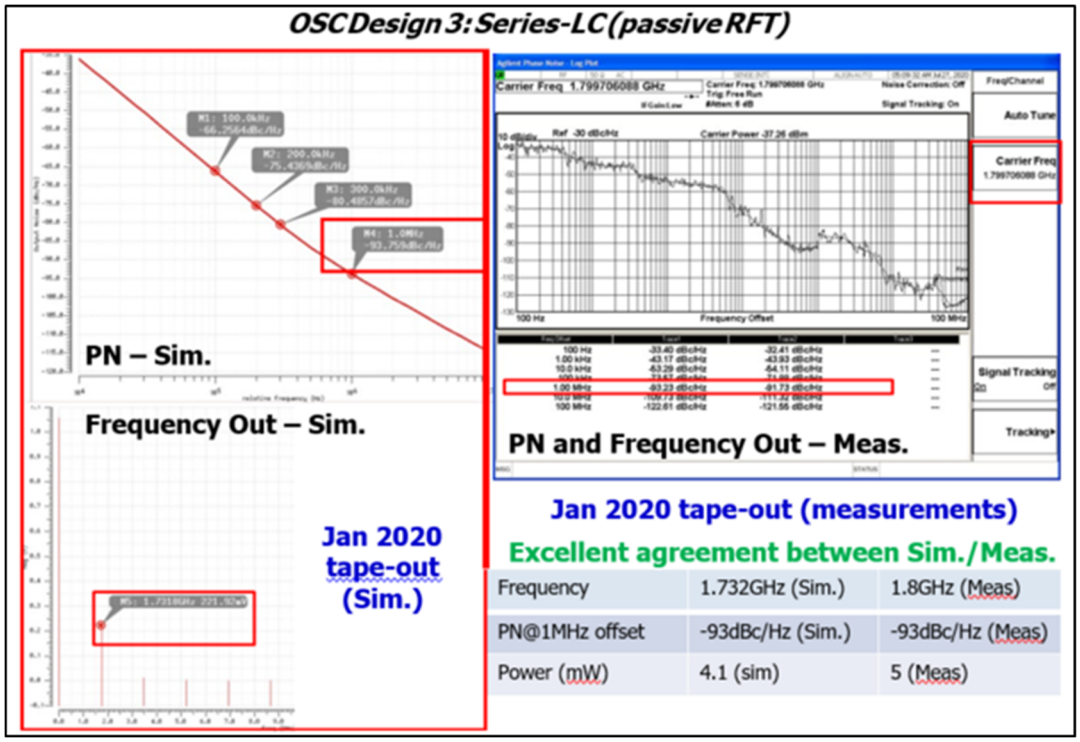


Figure 15: Proof-of-concept Measurement Results of the Series LC Topology (without the RFT) for Oscillator Design

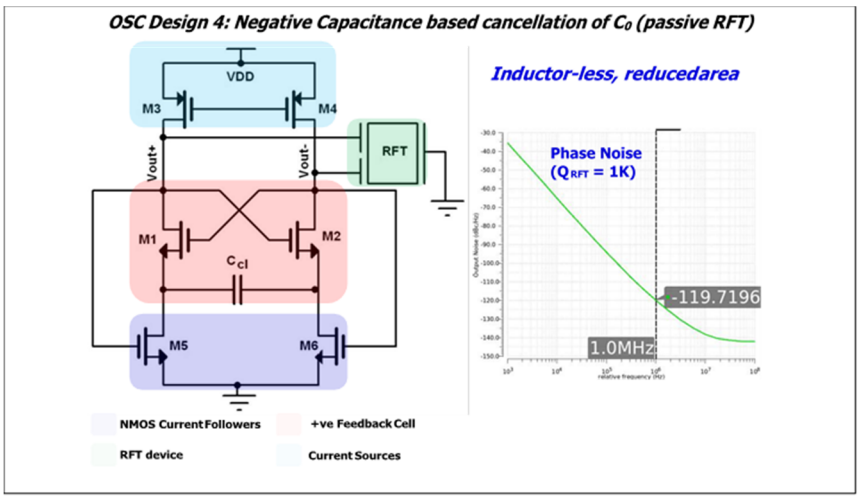


Figure 16: Oscillator Design 4

Passive RFT, 10-30GHz: negative capacitance/active inductance based cancellation of the high C_0, to solve the low X_{C0}/R_m issue.

Next, we have designed the oscillator with maximizing the active RFT benefits. To do this, we first analyzed the equivalent electrical model of the active RFT (Figure 17), which shows that the active RFT is a voltage controlled current source (VCCS) with a 270° phase shift. This is different from the traditional resonators which has an 180° phase shift between the input and the output. Therefore, as shown in Figure 17, the best way to use the active RFT is through a current

to voltage converter and a tuned gain stage which provides the additional phase shift with loop gain > 1. To provide the additional phase shift, wither a capacitor (design 5, Figure 18) or an inductor (design 6, Figure 19) can be used. However, a capacitor would require two gain stages to meet the Barkhausen criteria (please note the phase relations at various nodes in Figure 18), whereas an inductor would require only one gain stage to meet the Barkhausen criteria (please note the phase relations at various nodes in Figure 19).

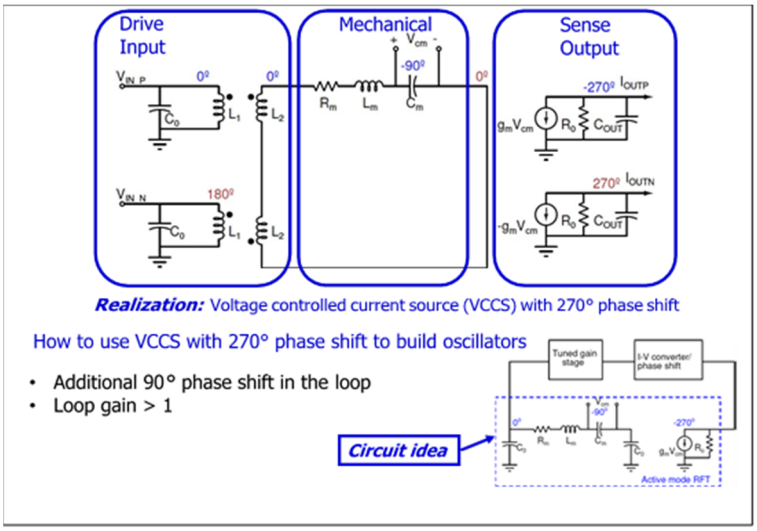


Figure 17: Electrical Equivalent Model of the Active RFT and Circuit Idea to Create an Oscillator

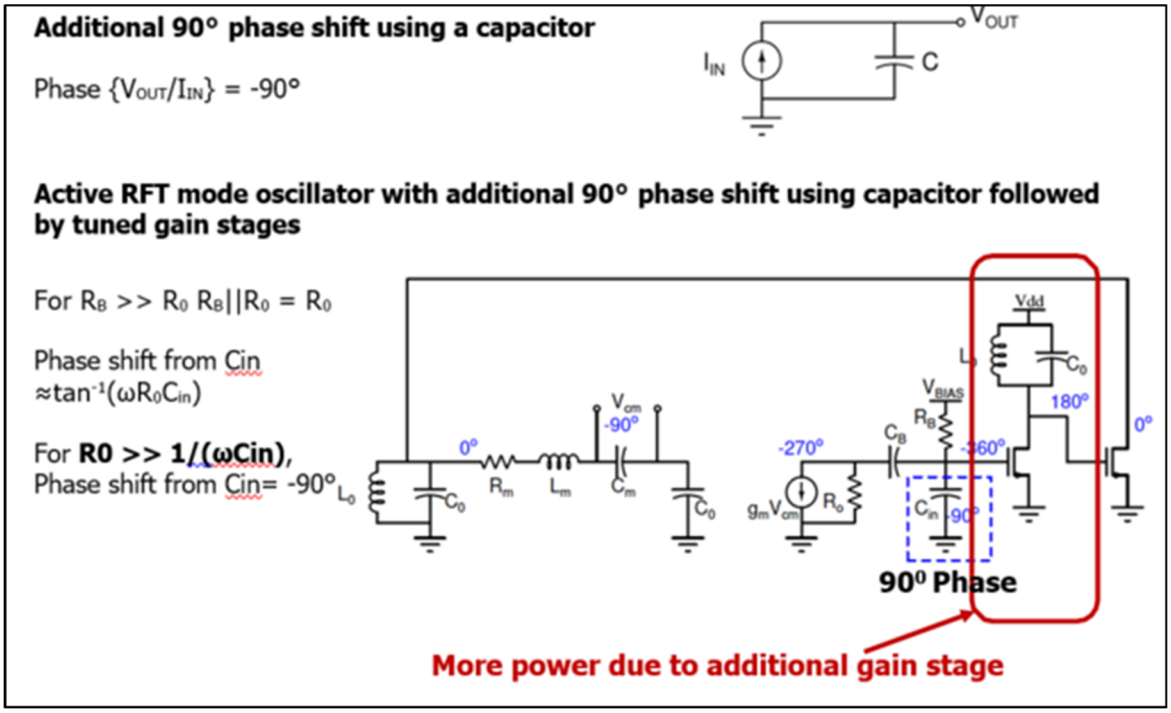


Figure 18: Oscillator Design 5

Active RFT, 10-30GHz: external capacitance provides additional phase.

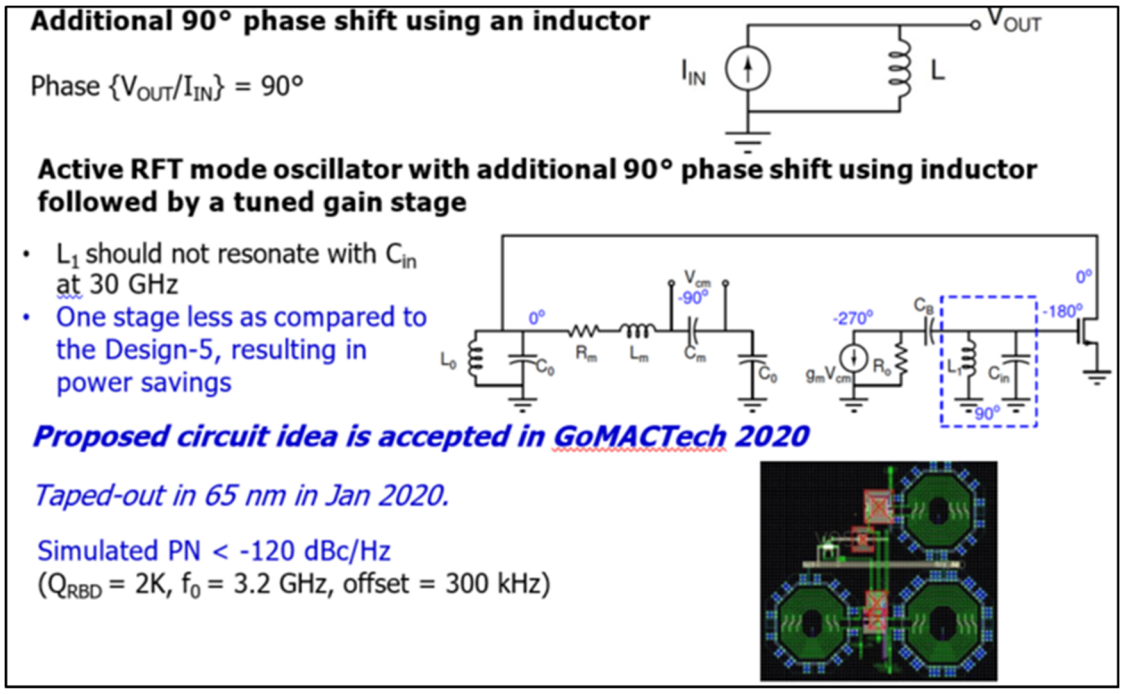


Figure 19: Oscillator Design 5

Active RFT, 10-30GHz: external inductor provides additional phase.

In conclusion, we have analyzed different topologies of oscillator design using on-chip, high-Q CMOS/MEMS hybrid resonators (RFTs/RBDs). We analyze the best phase noise performance by aligning the resonances of motional branch and static capacitance compensatory network in the same directions, thereby achieving <- 120dBc/Hz phase noise at 10kHz offset (Q of RFT = 10,000) for all the topologies. Among the topologies discussed, design 3 achieves best performance for passive RFT topologies (<- 120dBc/Hz phase noise at 10kHz offset, 208dB FOM), while design 6 achieves the best performance for active RFT topologies (<- 140dBc/Hz phase noise at 10kHz offset, 220dB FOM).

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LIST OF SYMBOLS, ABBREVIATIONS, AND ACRONYMS

ACRONYM	DESCRIPTION
AFRL	Air Force Research Lab
BEOL	Back-End-Of-Line
CMOS	Complementary Metal-Oxide Semiconductor
DARPA	Defense Advanced Research Projects Agency
FE	Front-ends
FET	Field Effect Transistor
GHz	Gigahertz
LC	Inductor/Capacitor
MEM	Microelectromechanical
MIDAS	Micro-Scale Device Array Structure
PLL	Phase-Locked-Loop
PN	P-type/N-type
RBD	Resonant Body Diodes
RF	Radio Frequency
RFT	Resonant Fin Transistor
Rx	Receive
SEM	Scanning Electron Microscopy
TAT	Trap-Assisted Tunneling
TSMC	Taiwan Semiconductor Corporation
Tx	Transmit
VCCS	Voltage Controlled Current Source