

**Naval Information
Warfare Center**



PACIFIC

TECHNICAL REPORT 3237
JUNE 2021

Fabrication of 2D Material-Based Devices

Carlos M. Torres Jr.
Brad C. Liu
Teresa Emery
Richard C. Ordonez
Cody K. Hayashi
James R. Adleman
Ryan P. Lu

NIWC Pacific

DISTRIBUTION STATEMENT A: Approved for public release.
Distribution is unlimited.

Naval Information Warfare Center Pacific (NIWC Pacific)
San Diego, CA 92152-5001

This page is intentionally blank.

Fabrication of 2D Material-Based Devices

Carlos M. Torres Jr.
Brad C. Liu
Teresa Emery
Richard C. Ordonez
Cody K. Hayashi
James R. Adleman
Ryan P. Lu

NIWC Pacific

DISTRIBUTION STATEMENT A: Approved for public release.
Distribution is unlimited.

Administrative Notes:

This report was approved through the Release of Scientific and Technical Information (RSTI) process in October 2020 and formally published in the Defense Technical Information Center (DTIC) in June 2021.



NIWC Pacific
San Diego, CA 92152-5001

NIWC Pacific
San Diego, California 92152-5001

A. D. Gainer, CAPT, USN
Commanding Officer

W. R. Bonwit
Executive Director

ADMINISTRATIVE INFORMATION

The work described in this report was performed by the Advanced Photonic Technologies Branch (55360) of the Enterprise Communications and Networks division (55300), Naval Information Warfare Center Pacific (NIWC Pacific), San Diego, CA. The NIWC Pacific Naval Innovative Science and Engineering (NISE) Program provided funding for this Basic and Applied Research project.

Released by
Brent Murray, Division Head
Enterprise Communications and Networks

Under authority of
Susie Hartzog, Department Head
Communications and Networks

ACKNOWLEDGMENTS

This work would not have been possible without the generous financial support from the NIWC Pacific ILIR and NISE Programs during the FY17-20 Basic and Applied Research efforts. The author expresses his sincere gratitude towards Dr. Dave Rees and Dr. Ryan Lu for their unwavering support during these basic research efforts.

This is a work of the United States Government and therefore is not copyrighted. This work may be copied and disseminated without restriction.

The citation of trade names and names of manufacturers is not to be construed as official government endorsement or approval of commercial products or services referenced in this report.

Editor: MRM

EXECUTIVE SUMMARY

This Technical Report summarizes the 2D material-based device fabrication procedures executed during the FY17-19 of the Office of Naval Research (ONR) In-House Laboratory Independent Research (ILIR) funded “Voltage-Tunable Wavelength-Agile 2D Material-Based Light-Emitting Transistors (2D-LETs)” project as well as the first year research effort FY20 Naval Innovative Science and Engineering (NISE) funded “Quantum-Engineered Nanodevices Exploiting Twistronics for EMW and C4ISR (QENETEC)” project. Most of the work was performed in the University of California – San Diego (UCSD) Nano3 cleanroom facility via an Indefinite Delivery/Indefinite Quantity (IDIQ) contract vehicle.

This page is intentionally blank.

ACRONYMS

2D	Two-Dimensional
2D-LETs	Voltage-Tunable Wavelength-Agile 2D Material-Based Light-Emitting
Al ₂ O ₃	Aluminum Oxide
C5ISR	Command, Control, Computers, Communications, Cyber, Intelligence, Surveillance, and Reconnaissance
COTS	Commercial Off The Shelf
CVD	Chemical Vapor Deposition
DON	Department of the Navy
EDL	Electric Dipole Layer
EMW	Electromagnetic Maneuver Warfare
HfO ₂	Hafnium Dioxide
IDIQ	Indefinite Delivery/Indefinite Quantity
ILIR	In-House Laboratory Independent Research
NISE	Naval Innovative Science and Engineering
ONR	Office of Naval Research
QENDL	Quantum-Engineered Nano Devices Laboratory
TMDs	Transition Metal Dichalcogenides
UCSD	University of California – San Diego

This page is intentionally blank.

CONTENTS

EXECUTIVE SUMMARY	v
ACRONYMS	vii
1. INTRODUCTION	1
2. DEVICE DESIGN AND FABRICATION	3
3. CONCLUSIONS	61
REFERENCES	63

FIGURES

1. Conceptual Vision of the Operational Battlespace of 2045.	1
2. (Top) Device Structure and Operation of the 2D-LET. (Bottom) Cross-sectional View of the Active Region of the 2D-LET. Source [3]: C. M. Torres Jr., UCLA PhD Dissertation (2015).	4
3. Isometric View and Cross-Section View of the Active Region of the 2D-LETs. Source [3]: C. M. Torres Jr., UCLA PhD Dissertation (2015).	5
4. Photomask design for the base contact definition step in the fabrication process flow of 2D-LETs.	6
5. Photomask design for the central top-gate contact definition step in the fabrication process flow of 2D-LETs.	7
6. Photomask design for the device isolation (e.g. CVD transferred 2D material etch) definition step in the fabrication process flow of 2D-LETs.	8
7. Photomask design for the dual-side gate top-gate contact definition step in the fabrication process flow of 2D-LETs.	9
8. Generalized steps 1-3 in the fabrication process flow for fabricating 2D-LETs. Source [3]: C. M. Torres Jr., UCLA PhD Dissertation (2015).	10
9. Generalized steps 4-6 in the fabrication process flow for fabricating 2D-LETs. Source [3]: C. M. Torres Jr., UCLA PhD Dissertation (2015).	11
10. Generalized steps 7-9 in the fabrication process flow for fabricating 2D-LETs. Source [3]: C. M. Torres Jr., UCLA PhD Dissertation (2015).	12
11. Generalized steps 10-13 in the fabrication process flow for fabricating 2D-LETs. Source [3]: C. M. Torres Jr., UCLA PhD Dissertation (2015).	13
12. Screenshot of the PI's user page for the UCSD Nano3 cleanroom website. This shows 15 equipment that the PI has been trained and authorized to use at any time.	14

13. (Left) The main corridor of the UCSD Nano3 cleanroom facility. (Right) The PI (Dr. Torres) performing a heated phosphoric acid etching of silicon nitride (Si_3N_4) in the cleanroom.	14
14. Images of seven 4 inch (100mm) wafers right before the device isolation field oxide (FOX, around 550nm SiO_2 expected thickness for WET 1050°C recipe for a growth time of 1 hour, 6 minutes, and 5 seconds) was grown in a thermal oxidation furnace.	15
15. Image of G41. G41 is one of the six 4 inch (100mm) wafers currently being processed in this batch. Its cross section currently consists of n^{++} silicon substrate/83nm SiO_2 pad-buffer oxide/237nm silicon nitride (Si_3N_4) hard mask.....	16
16. Close-up image of various devices on G41 after the FOX (570nm SiO_2) growth via a thermal oxidation furnace.....	16
17. Image of the six 4 inch wafers currently being processed into light-emitting transistors. The top row shows (left to right) G40, G41, and G42, which are all n^{++} silicon substrates.	17
18. Optical image (10x objective lens) of G41 after the first photoresist (AZ 1512) development step. Device cross section consists of n^{++} silicon/83nm SiO_2 pad oxide/237nm Si_3N_4 hard mask/~ 1.2 μm AZ 1512 photoresist).	18
19. Optical image (10x objective lens) of G41 after the first Si_3N_4 etch using an Oxford Instruments P80 RIE (reactive ion etcher).....	19
20. Optical image (10x objective lens) of G41 after the second Si_3N_4 etch using an Oxford Instruments P80 RIE (reactive ion etcher).....	20
21. Optical image (5x objective lens) of G41 after the LOCOS process was complete (that is, the growth of the field oxide (FOX)).	21
22. Optical image (10x objective lens) of G41 after the LOCOS process was complete (that is, the growth of the field oxide (FOX)). Device cross section consists of n^{++} silicon/83nm SiO_2 pad oxide/237nm Si_3N_4 hard mask), each of which is separated from its nearest neighbor device via a around 570nm thick SiO_2 FOX.	21
23. Optical image (20x objective lens) of G41 after the LOCOS process was complete (that is, the growth of the field oxide (FOX)).	22
24. Optical image (50x objective lens) of G41 after the LOCOS process was complete (that is, the growth of the field oxide (FOX)).	22
25. Optical image (50x objective lens) of G41 after the LOCOS process was complete (that is, the growth of the field oxide (FOX)).	23

26. Optical image (50x objective lens) of G41 after the LOCOS process was complete (that is, the growth of the field oxide (FOX)).	24
27. Optical image (50x objective lens) of G41 after the LOCOS process was complete (that is, the growth of the field oxide (FOX)).	24
28. Image of G45, one of the 4 inch (100mm) wafers being processed, that is about to be probed by the DekTak 150 stylus profilometer.	25
29. Image of the monitor (e.g. sample positioning window) connected to the DekTak 150 stylus profilometer. The stylus raster scans the substrate surface based on a defined scan rate, distance, and resolution in order to measure step heights, etc.	25
30. Image of the monitor (e.g. data analysis window) connected to the DekTak 150 stylus profilometer that probes G41.	26
31. Image of a quadrant of G41 after the field oxide (FOX) growth in an oxidation furnace and prior to hot phosphoric acid etching of the silicon nitride hard masks.	26
32. Image of the hot phosphoric acid etching step in the fabrication process. A beaker is filled with 600 mL of phosphoric (H_3PO_4) acid and is placed on a hot plate.	27
33. Image of a quadrant of G41 after the hot phosphoric acid etching of the silicon nitride hard masks.	28
34. Optical image (5X objective lens) of G41_Q3_LET_n ⁺⁺ substrate after etching away the Si_3N_4 masks used in the LOCOS (LOCAl Oxidation of Silicon) process.	28
35. Optical image (10X objective lens) of G41_Q3_LET_n ⁺⁺ substrate after etching away the Si_3N_4 masks used in the LOCOS (LOCAl Oxidation of Silicon) process.	29
36. Optical image (20X objective lens) of G41_Q3_LET_n ⁺⁺ substrate after etching away the Si_3N_4 masks used in the LOCOS (LOCAl Oxidation of Silicon) process.	30
37. Optical image (50X objective lens) of G41_Q3_LET_n ⁺⁺ substrate after etching away the Si_3N_4 masks used in the LOCOS (LOCAl Oxidation of Silicon) process.	31
38. Optical image (50X objective lens) of G41_Q3_LET_n ⁺⁺ substrate after etching away the Si_3N_4 masks used in the LOCOS (LOCAl Oxidation of Silicon) process.	32

39. Optical image (50X objective lens) of G41_Q3_LET_n ⁺⁺ substrate after etching away the Si ₃ N ₄ masks used in the LOCOS (LOCAl Oxidation of Silicon) process.	33
40. Growing a thin tunnel oxide barrier using rapid thermal processing.	34
41. A substrate diced from the G41 quadrant shown in Figure 32 as well as a control silicon substrate (dipped in BOE (6:1) for 30 seconds to remove any native oxide) are placed onto a SiO ₂ loading substrate with K type thermocouple touching the backside of the 4 inch SiO ₂ /Silicon wafer.	35
42. CVD MoS ₂ on sapphire substrate purchased from 2D Semiconductors, Inc.	36
43. Spin coating PMMA polymer onto the CVD 2D material on top of sapphire substrate to assist the 2D material wet transfer onto arbitrary substrates.	37
44. Recipe used to spin coat the PMMA polymer onto the CVD 2D material/sapphire substrate.	38
45. Polypropylene fume hood with secondary container for working with hydrofluoric (HF) acid and buffered oxide etchant (BOE).	38
46. Using the proper personal protective equipment (PPE) to work with HF/BOE (see Figure 13), we prepare our workspace in the fume hood using the secondary container for HF work.....	39
47. Close up view of the CVD 2D material/sapphire substrate floating on the surface of the BOE solution in the beaker shown in Figure 46.	40
48. Close up view of the PMMA/CVD 2D material naturally being delaminated from the sapphire substrate prior to the sapphire substrate sinking into the BOE solution.	41
49. PMMA/CVD 2D material after wet transfer onto a 2D-LET substrate.	42
50. PMMA/CVD 2D material transferred onto a 2D-LET substrate after drying overnight.	42
51. Optical micrograph of a 2D-LET substrate with PMMA/CVD 2D material transferred and dried overnight.	43
52. Optical micrograph of a 2D-LET substrate after the PMMA on top of the CVD 2D material was dissolved in acetone overnight.	44
53. The PI performs metallization on the 2D-LET substrates using a Temescal BJD 1800 e-beam evaporator in the UCSD Nano3 cleanroom.....	45
54. Optical micrograph of a 2D-LET substrate after a 3.5nm Aluminum protection layer was e-beam evaporated using a Temescal BJD 1800 e-beam evaporator	

to protect the CVD 2D material from directly contacting photoresist in the future fabrication processing steps. Scale bar is 500 μ m.	46
55. Optical micrograph of a 2D-LET substrate after the second photolithography step was completed to define circular masks to protect the CVD 2D material from being etched away in a future fabrication processing step. Scale bar is 500 μ m.....	47
56. We next use an AJA Orion Series Argon Ion Mill at the NIWC Pacific Battery Ashburn cleanroom facility to test the etching of monolayer CVD MoS ₂ on sapphire substrates.	48
57. Optical micrograph of a 2D-LET device after the photoresist masks shown in Figure 55 were stripped in acetone.	49
58. Optical micrograph of 2D-LET devices after 20nm Titanium adhesion layer/100nm Gold contacts were deposited using a Temescal BJD 1800 e-beam evaporator.	50
59. Beneq TFS 200 Atomic Layer Deposition.	51
60. G41_Q4_S3 substrate with 6nm HfO ₂ top-gate dielectric during CVD graphene transfer for top-gate fabrication. G41_Q4_S3 with PMMA/CVD Graphene pieces transferred onto at least two matrices (with 20 devices covered per matrix).....	52
61. G41_Q4_S3 with CVD graphene after PMMA was dissolved in acetone. The presence of CVD graphene is not visible to the eye but is confirmed via Raman spectroscopy.	53
62. Raman spectrum of COTS monolayer CVD graphene transferred onto G41_Q4_S3 substrate via an electrolysis and scooping method to serve as a top-gate electrode upon further device fabrication.	54
63. Image through the viewport of the Plasma Etch PE100 oxygen plasma etcher in UCSD Nano3 cleanroom. The 2D material-based substrate is located near the center.....	55
64. Optical micrograph of device G41_Q4_S3_B33_MoS ₂ _GTG (Graphene-Top-Gate) LET (Light Emitting Transistor) after the oxygen plasma etching step.....	56
65. Optical micrograph of device (left) G41_Q4_S3_B33_MoS ₂ _GTG (Graphene-Top-Gate) LET (Light Emitting Transistor) after the 5 th photolithography step to define the side metal gates that make contact to the central CVD graphene.	57
66. Image of the device substrate G41_Q4_S3 with CVD graphene top-gate contact after the fifth and final photolithography step prior to metallization of the side metallic contacts to the central CVD graphene top-gate.	58

67. Optical micrograph of device (left) G41_Q4_S3_B33_MoS ₂ _GTG (Graphene-Top-Gate) LET (Light Emitting Transistor) after the metallization step (50nm Au/150nm Al) to define the side gates that contact the graphene top-gate region.....	59
68. Image of the device substrate G41_Q4_S3 with CVD graphene top-gate contact after metallization of the side metallic contacts to the central CVD graphene top-gate.	60

1. INTRODUCTION

The Conceptual Vision of the Operational Battlespace of 2045 in the 2017 Department of the Navy (DON)’s 30 Year Research and Development Plan predicts quantum-base sensing, nanotechnology, and photonics as Key Programs and Technology Investments [1]. The DON identifies Advanced Materials and Manufacturing Technologies and Advanced Computing and Sensing as core technology areas that must be built and sustained. Furthermore, the EMW Focus Area in the 2015 ONR Naval Science and Technology Strategy seeks to “enable the warfighter to have complete control over the electromagnetic spectrum...” [2]. For these reasons, NIWC Pacific invested via an FY18 NISE Laboratory Recapitalization effort in establishing a novel laboratory, the “Quantum-Engineered Nano Devices Laboratory (QENDL)”, that emphasizes various modalities of characterization of advanced materials and devices. QENDL’s mission is to explore and exploit the exotic properties of atomic-layered (2D) materials, quantum materials, and their heterostructures for the benefit of the future Warfighter in terms of C5ISR, Electromagnetic Maneuver Warfare (EMW), and Spectrum Dominance.

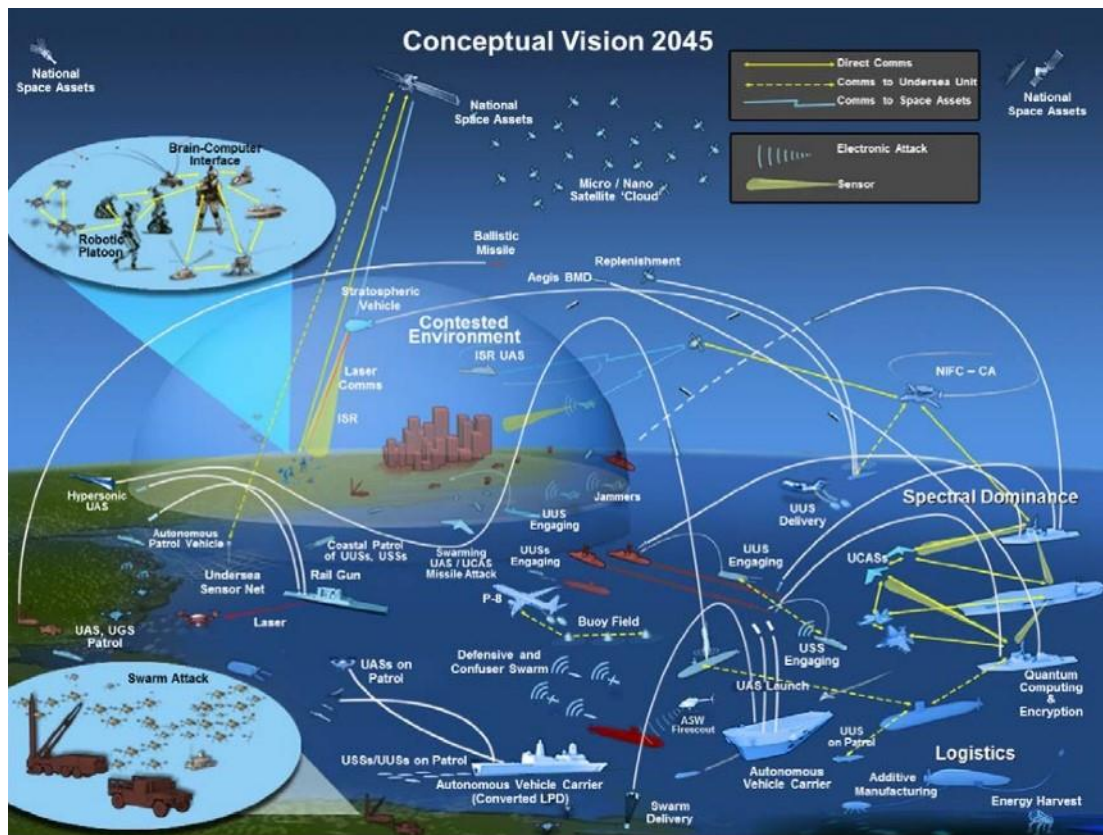


Figure 1. Conceptual Vision of the Operational Battlespace of 2045.

Source: [1] <https://blog.spawar.navy.mil/command/2017/03/don-30-year-rd-plan.html>

This Technical Report focuses on the device fabrication efforts undertaken at the UCSD Nano3 cleanroom facility towards the fabrication of 2D material-based devices utilizing large-area COTS CVD 2D materials that will subsequently be optically and electrically characterized in the QENDL lab at NIWC Pacific

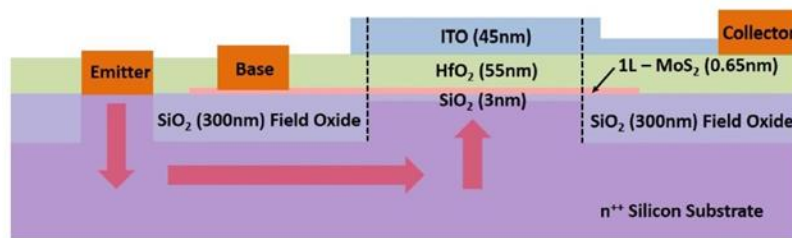
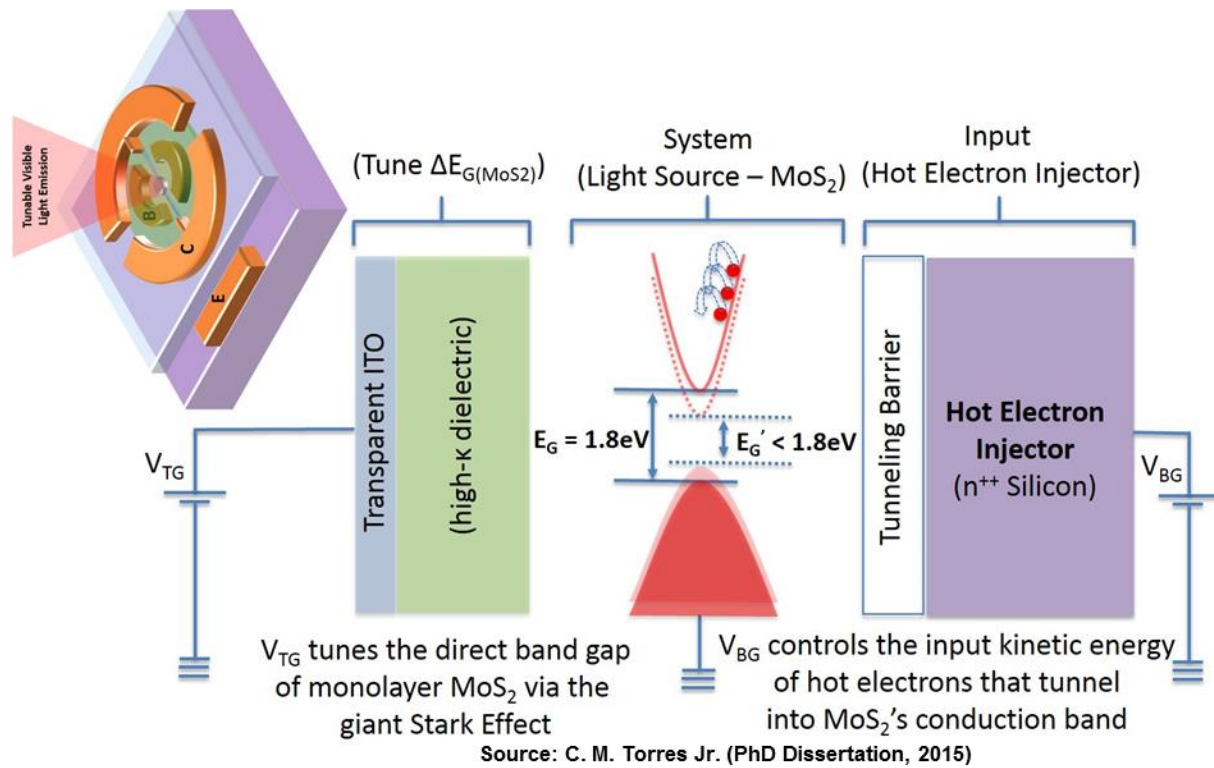
This page is intentionally blank.

2. DEVICE DESIGN AND FABRICATION

2.1 DEVICE OPERATION

Our approach is to design, fabricate, and characterize a novel dual-gated vertical tunneling injection device structure utilizing 2D materials and an ion-gel top-gate dielectric that relies on the injection electroluminescence (EL) of hot electrons that quantum mechanically tunnel from the underlying substrate into the conduction band of a particular 2D material such as (1) graphene and (2) monolayer transition metal dichalcogenides (TMDs) (e.g. MoS₂, MoSe₂, WS₂, or WSe₂) that feature direct bandgaps in the visible to infrared spectrum. The first variant of the 2D-LET, the GBILET (Graphene Broadband Infrared Light-Emitting Transistor), relies on monolayer graphene as the active region for light emission [3-8]. A large-area CVD-grown monolayer graphene will be transferred onto a highly-doped silicon substrate with an ultra-thin (around 2-3nm) tunnel oxide. Base contacts will be patterned onto the graphene. Afterwards, an ion-gel will be prepared and dispersed onto the CVD graphene active area to serve as a top-gate dielectric with exceptionally high carrier doping capability (e.g. $n > 10^{14} \text{ cm}^{-2}$ carrier concentration (holes or electrons) can be induced in the graphene and other TMDs -- an order of magnitude larger than what is currently possible with other top-gate dielectrics [9]).

The ion-gel top-gate dielectric enables the possibility of two practical features: (1) a larger Fermi-level shift or equivalently a larger accessible spectral range in graphene and (2) the capability for flexible optoelectronics with minimal electrical performance degradation under high flexure. The second variant of the 2D-LET, the TMD-LET, features a similar device structure except that a large area monolayer TMD (e.g. MoS₂, MoSe₂, WS₂, or WSe₂) is used instead of graphene. For the TMD-LET, the ion-gel top-gate serves to greatly reduce the direct bandgap via the giant Stark Effect due to the exceptionally large perpendicular electric fields made possible by the ion-gel top-gate dielectric [3-9]. Demonstration of an enhanced Stark Effect via ion-gel gating at room temperature will spawn new avenues of research in material science focused on the in-situ voltage-induced modulation of energy bandstructures from plethora of 2D materials.



Source: C. M. Torres Jr. (PhD Dissertation, 2015)

Figure 2. (Top) Device Structure and Operation of the 2D-LET. (Bottom) Cross-sectional View of the Active Region of the 2D-LET. Source [3]: C. M. Torres Jr., UCLA PhD Dissertation (2015).

Figure 2 shows the device structure and operation of the 2D-LET (top) and the cross-sectional view of the active region of a 2D-LET (bottom). The device operation of the 2D-LET involves the following mechanisms. First, a hot electron distribution is injected from a degenerately doped n^{++} silicon substrate through an ultrathin tunnel barrier (e.g. around 2nm SiO_2) and into the conduction band of a direct bandgap monolayer 2D semiconductor (e.g. MoS_2 , WS_2 , WSe_2 , etc.) via a back-gate voltage bias. As the hot electrons relax to the conduction band edge, they will eventually recombine with holes in the valence band and emit photons with a wavelength near the direct bandgap energy. Furthermore, application of a top-gate voltage bias across the top-gate dielectric (e.g. ion-gel, ionic liquid, hexagonal boron nitride (hBN), hafnium dioxide (HfO_2), aluminum oxide (Al_2O_3), etc.) will generate an electric field perpendicular to the 2D material in the active (e.g. base) region of the 2D-LET [3-5].

As the top-gate voltage increases, the bandgap of the 2D material will reduce due to the giant Stark Effect [3,5]. Thus, the top-gate of the 2D-LET can tune the frequency (or wavelength) of the emitted photons from the 2D material. Note that the top-gate can consist of optically transparent materials

such as: indium tin oxide (ITO), ion-gel, ionic-liquid, large-area CVD transferred graphene, or a semi-transparent metallic contact (e.g. 1nm Ti/5nm Pt) [3-5, 9].

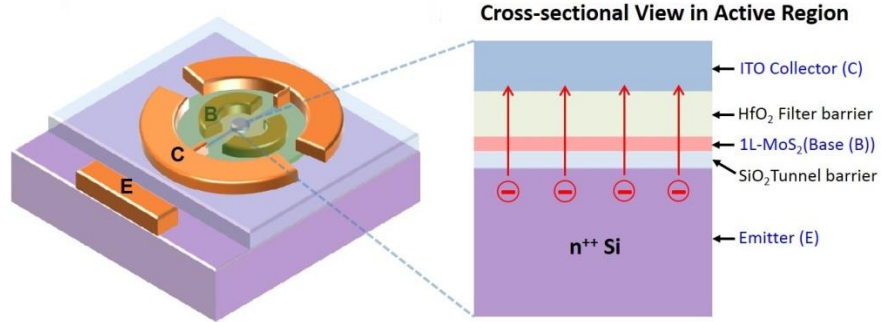


Figure 3. Isometric View and Cross-Sectional View of the Active Region of the 2D-LETs. Source [3]: C. M. Torres Jr., UCLA PhD Dissertation (2015).

Figure 3 shows an isometric view and cross-section of the active region in one variant of our 2D-LET device structure. The hot electrons are vertically injected from the n^{++} silicon emitter, quantum mechanically tunnel through the 2-3nm SiO_2 tunnel barrier and into the 2D material of choice (e.g. monolayer MoS_2 in this case (0.65nm thick)). A top-gate voltage bias applied between the collector and the base (e.g. 2D material) will induce a perpendicular electric field to the surface of the 2D material, which will induce a reduction in the direct bandgap of the monolayer TMD in the base region due to the giant Stark effect [3,5]. We expect a much more pronounced Stark shift by implementing an ion-gel or ionic liquid as the composite top-gate dielectric and collector [3-5, 9].

2.2 PHOTOMASK DESIGN

The following masks were designed using the Tanner L-Edit (Layout Editor) software and the .gds files were provided to Toppan Photomasks, Inc. for the procurement and fabrication of the photomasks.

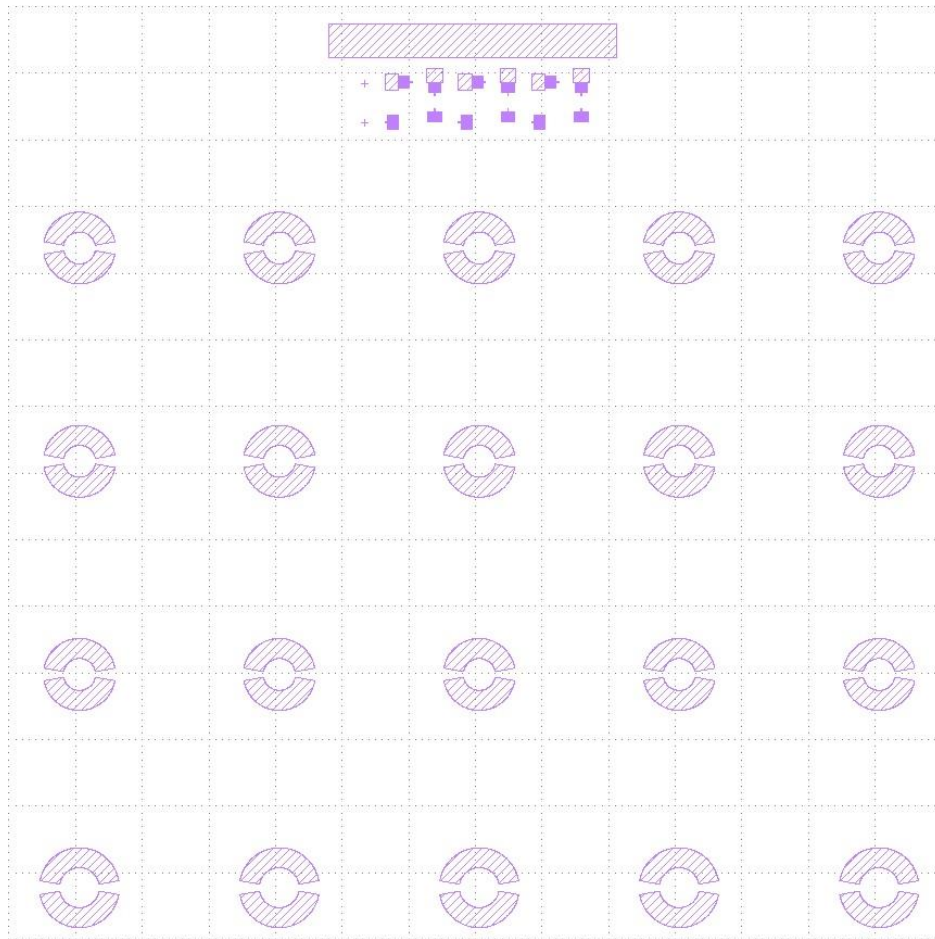


Figure 4. Photomask design for the base contact definition step in the fabrication process flow of 2D-LETs.

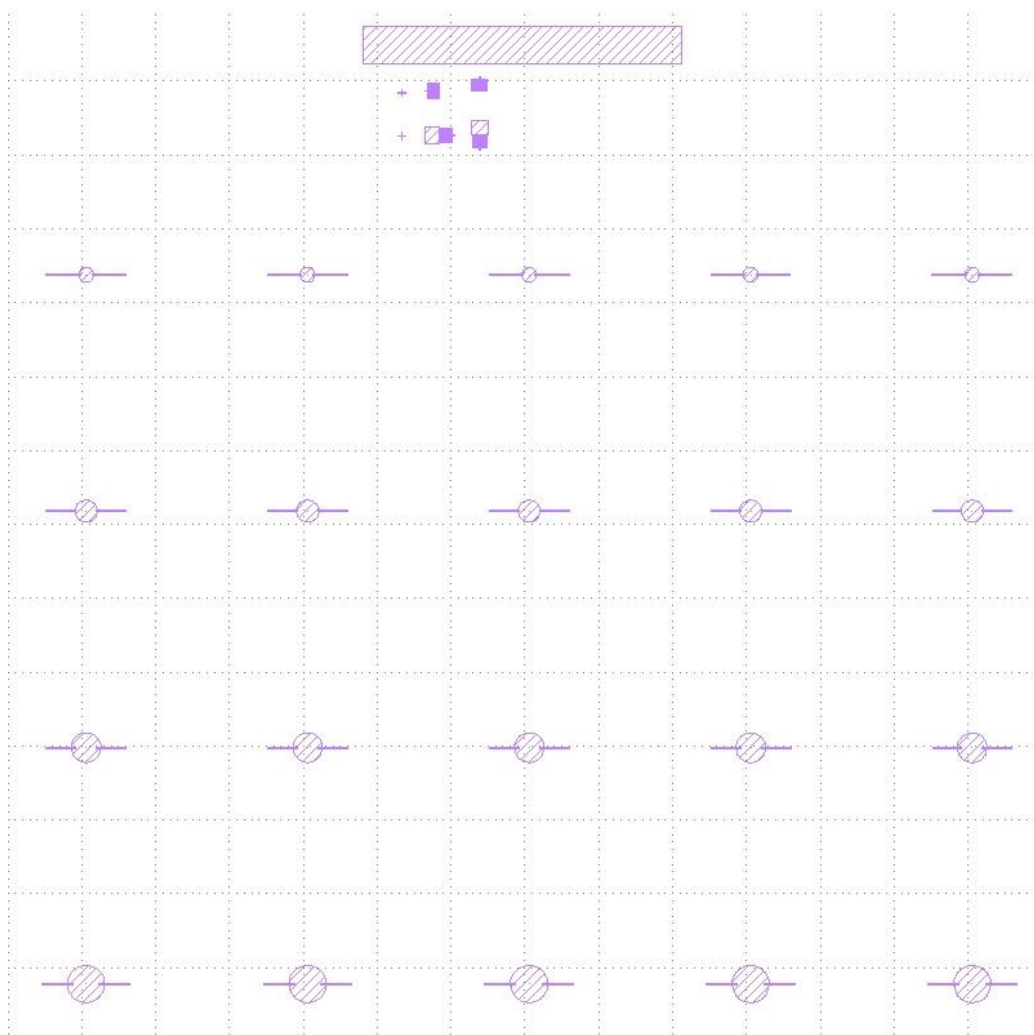


Figure 5. Photomask design for the central top-gate contact definition step in the fabrication process flow of 2D-LETs.

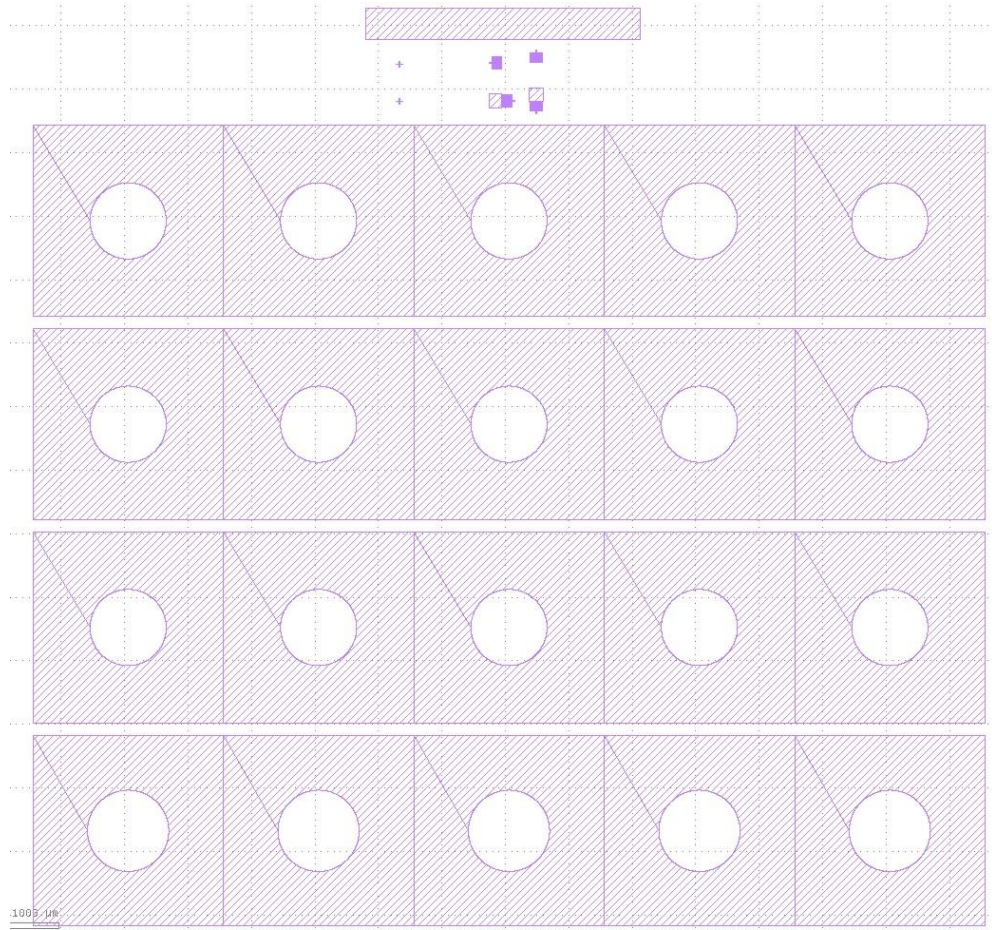


Figure 6. Photomask design for the device isolation (e.g. CVD transferred 2D material etch) definition step in the fabrication process flow of 2D-LETs.

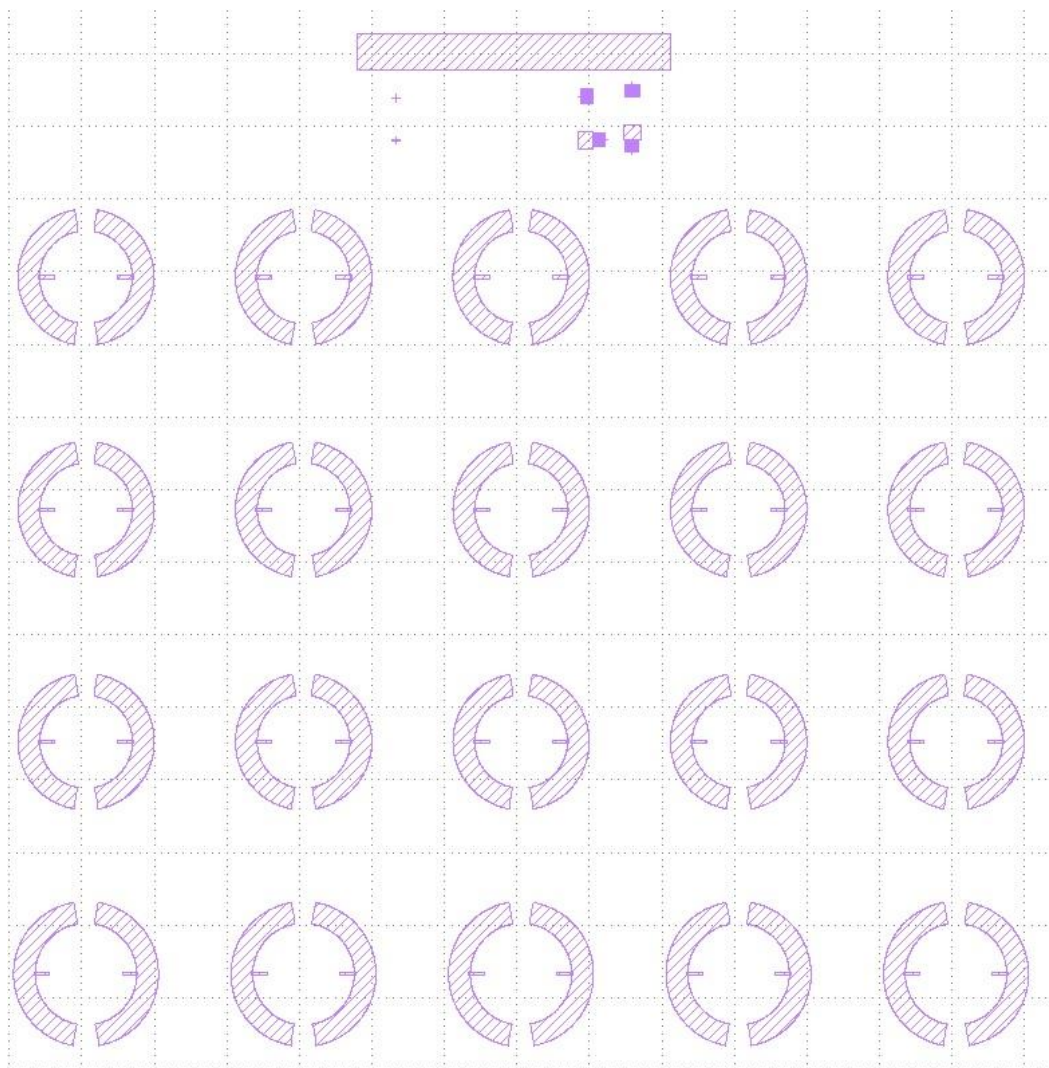
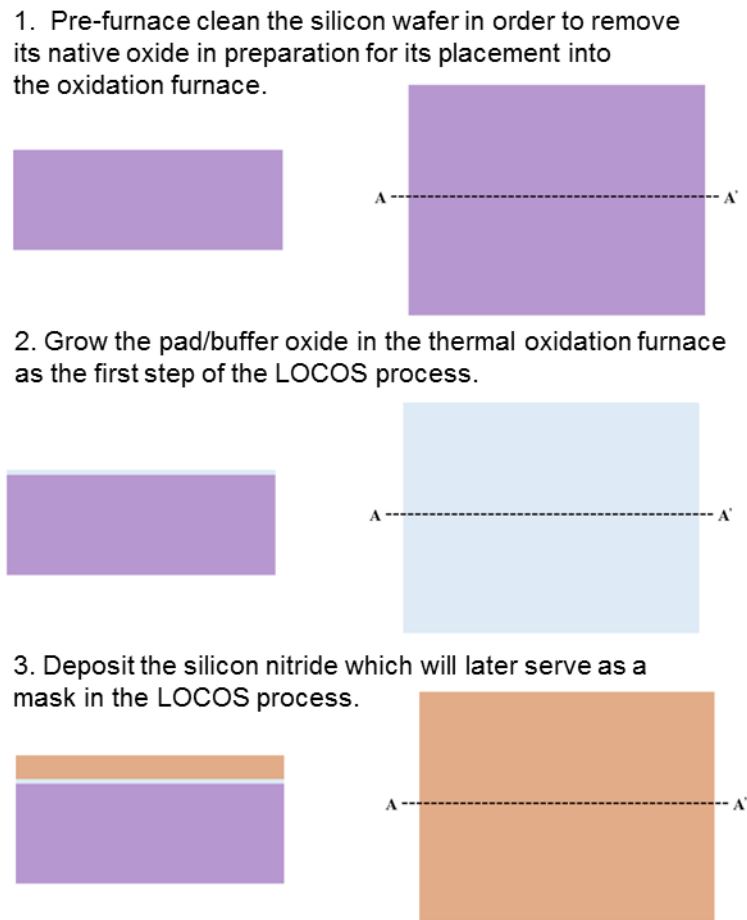


Figure 7. Photomask design for the dual-side gate top-gate contact definition step in the fabrication process flow of 2D-LETs.

2.3 FABRICATION PROCESS FLOW

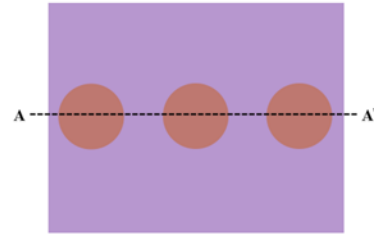
The following images show the fabrication process flow developed for the 2D-LETs that utilize a conventional high-k dielectric such as hafnium dioxide (HfO_2) or aluminum oxide (Al_2O_3). These 13 steps are quite generalized and further details and discussions can be found in the PI's (Dr. Torres) UCLA PhD dissertation from 2015 [3]. For the 2D-LETs utilizing an ion-gel, fabrication steps 1-10 are exactly the same as for the conventional high-k dielectric variety of 2D-LETs. However, after step 10, the ion-gel is spin-coated across the entire substrate with the 2D materials exposed in the active regions of the back-gated 2D-LETs. Finally, a probe can serve as a non-local probe to bias the 2D materials in the active regions via the manifestation of an electric dipole layer (EDL) in the proximity of the 2D material's surface. Also note that simply drop-casting an ionic liquid after fabrication process step 10 and piercing the surface of the ionic liquid with a probe can allow for a similar EDL gating effect and functionality [5].



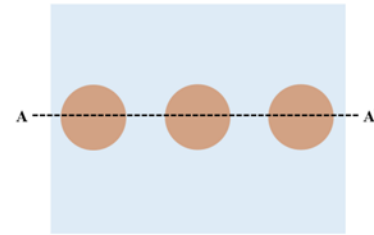
Source: C. M. Torres Jr., PhD Dissertation (2015).

Figure 8. Generalized steps 1-3 in the fabrication process flow for fabricating 2D-LETs. Source [3]: C. M. Torres Jr., UCLA PhD Dissertation (2015).

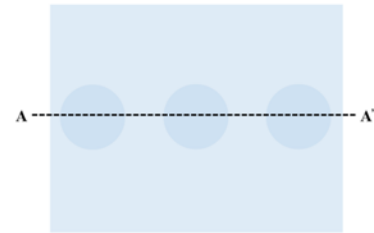
4. Dry etch through the silicon nitride, the pad oxide, and into the silicon substrate for the regions of the silicon nitride which are not covered by the photoresist masks (not shown) which were defined during the 1st photolithography step.



5. Grow the field oxide (FOX) in the thermal oxidation furnace to complete the LOCOS process.



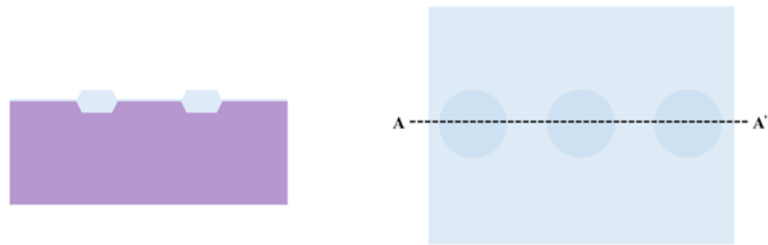
6. Selectively wet etch the silicon nitride masks in a heated solution of phosphoric acid.



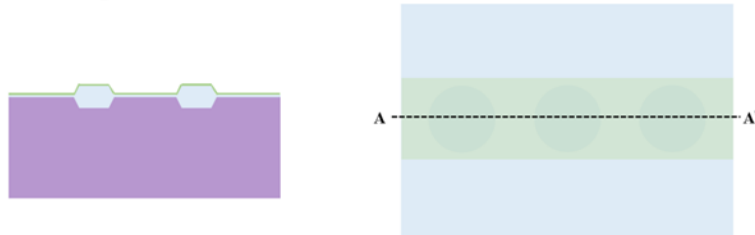
Source: C. M. Torres Jr., PhD Dissertation (2015).

Figure 9. Generalized steps 4-6 in the fabrication process flow for fabricating 2D-LETs. Source [3]: C. M. Torres Jr., UCLA PhD Dissertation (2015).

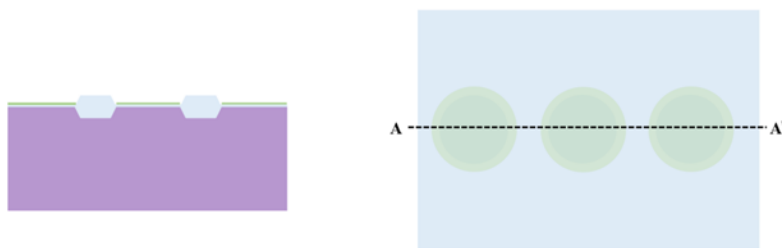
7. Grow the tunnel oxide via the rapid thermal oxidation furnace.



8. Transfer the CVD grown 2D material of choice onto the active regions of the substrate.



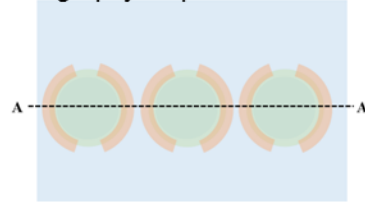
9. Etch the 2D material which are not covered by the photoresist masks that were defined during the 2nd photolithography step via oxygen plasma in order to isolate the various devices.



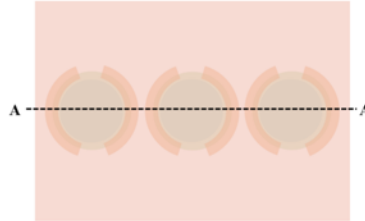
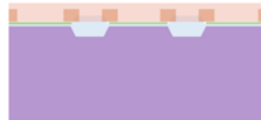
Source: C. M. Torres Jr., PhD Dissertation (2015).

Figure 10. Generalized steps 7-9 in the fabrication process flow for fabricating 2D-LETs. Source [3]: C. M. Torres Jr., UCLA PhD Dissertation (2015).

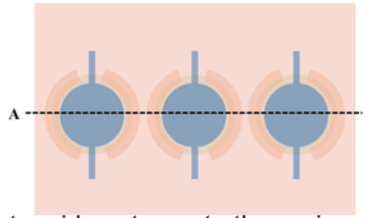
10. Pattern and deposit the base contacts onto the regions which were defined during the 3rd photolithography step via the e-beam evaporator.



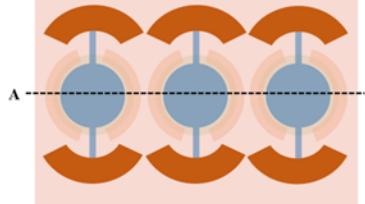
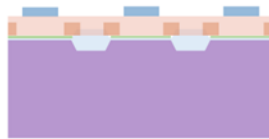
11. Deposit the top-gate dielectric (e.g. Al_2O_3 or HfO_2) via atomic layer deposition.



12. Sputter the ITO onto the top-gate central circular regions which were defined during the 4th photolithography step.



13. Pattern and deposit the collector side gates onto the regions defined during the 5th photolithography step via the e-beam evaporator.



Source: C. M. Torres Jr., PhD Dissertation (2015).

Figure 11. Generalized steps 10-13 in the fabrication process flow for fabricating 2D-LETs. Source [3]: C. M. Torres Jr., UCLA PhD Dissertation (2015).

2.4 UCSD NANO3 CLEANROOM FACILITY FABRICATION PROCESS FLOW

The screenshot shows the user interface of the UCSD Nano3 website. At the top, the header reads 'CALIFORNIA INSTITUTE FOR TELECOMMUNICATIONS AND INFORMATION TECHNOLOGY' above the 'nano3' logo, which also includes 'SCIENCE ENGINEERING MEDICINE' and an 'it²' logo. A navigation bar contains links for Facilities, Equipment, Access, Safety, and Services. Below this, the user is logged in as 'Carlos Torres Jr.' with a 'Logout' button. A sidebar menu on the left lists categories: User Account (Home, Access Requirements, View Graded Exams), Equipment (My Equipment, Reservations, Reserve Equipment, My Equipment Authorizations, Equipment Schedule, Authorized User Lists), and Training. The main content area, titled 'My Equipment Authorizations', states 'You are authorized to use the following equipment' and lists 15 items with their respective counts in parentheses: AG Associates Heat Pulse 610 (1), Beneg TFS200 Atomic Layer Deposition, Dektak 150, Denton Discovery 18 Sputter System, Denton Discovery 635 Sputter System, Filmetrics F20, Karl Suss MA6 Mask Aligner, Oxford Plasmalab 100 RIE/ICP, Oxford Plasmalab 80+ PECVD, Oxford Plasmalab 80+ RIE, Plasma Etch PE100, PVA TePla PS100, Rudolph Auto EL Ellipsometer, Temescal BJD 1800 Ebeam Evaporator (2), and Veeco NT1100 Optical Profiling System.

Figure 12. Screenshot of the PI's user page for the UCSD Nano3 cleanroom website. This shows 15 equipment that the PI has been trained and authorized to use at any time.

- There are an additional 3 authorizations that are not shown in this image. Each equipment requires about 30 minutes to 2 hours for a one-on-one on-site training with the super user, followed by another 30 minutes to 2 hours for authorization. The PI has developed good relations and rapport with the Nano3 on-site equipment engineers and staff.



Figure 13. (Left) The main corridor of the UCSD Nano3 cleanroom facility. (Right) The PI (Dr. Torres) performing a heated phosphoric acid etching of silicon nitride (Si_3N_4) in the cleanroom.

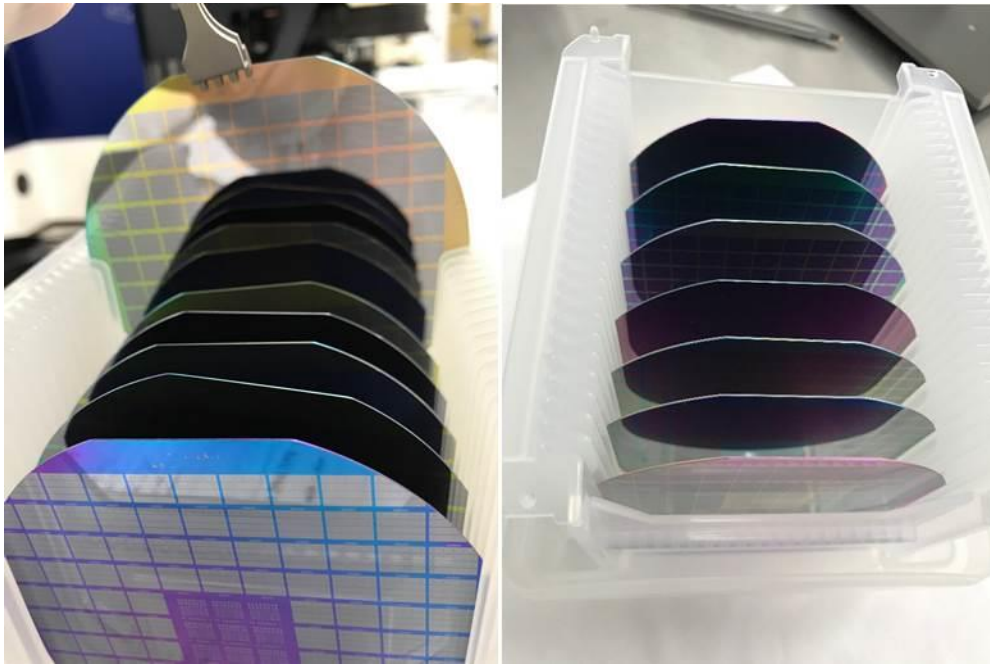


Figure 14. Images of seven 4 inch (100mm) wafers right before the device isolation field oxide (FOX, around 550nm SiO_2 expected thickness for WET 1050°C recipe for a growth time of 1 hour, 6 minutes, and 5 seconds) was grown in a thermal oxidation furnace.

- The central substrate (right figure) is a bare n^{++} silicon wafer that serves as a control substrate in order to measure the SiO_2 thickness and uniformity across the 4 inch wafer after the thermal oxidation furnace step.

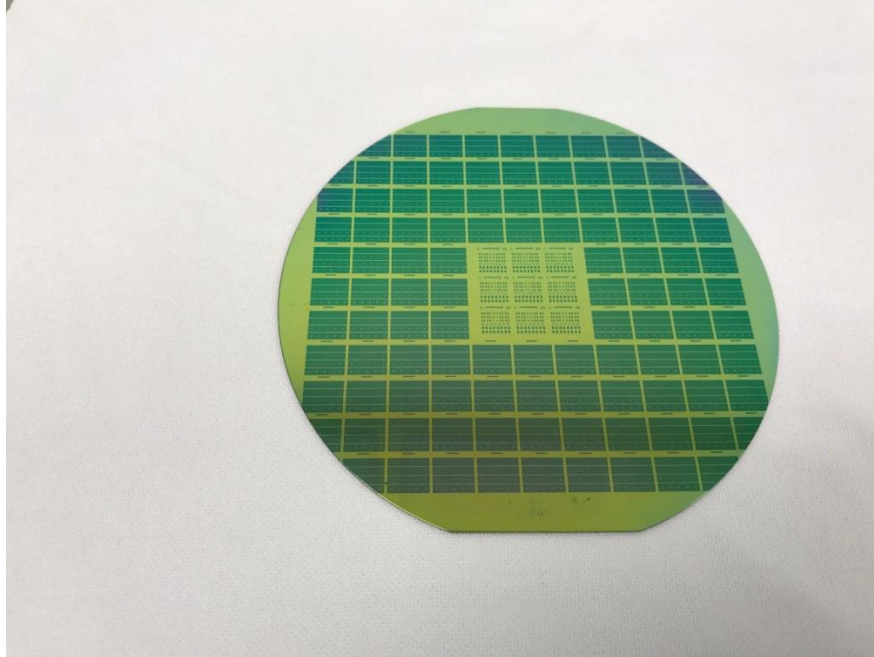


Figure 15. Image of G41. G41 is one of the six 4 inch (100mm) wafers currently being processed in this batch. Its cross section currently consists of n⁺⁺ silicon substrate/83nm SiO₂ pad-buffer oxide/237nm silicon nitride (Si₃N₄) hard mask.

- This image shows the condition of G41 after the LOCOS (LOCAl Oxidation of Silicon) process was complete. A field oxide (FOX) of around 570nm SiO₂ isolates the various Si₃N₄ hard masks that are located at the active regions of the future light-emitting transistors (LETs).
- Each dark green array/square features 20 devices (4x5 matrix). The dark green areas are around 570nm thick SiO₂ device isolating FOX. The lighter green areas are the Si₃N₄ hard masks.

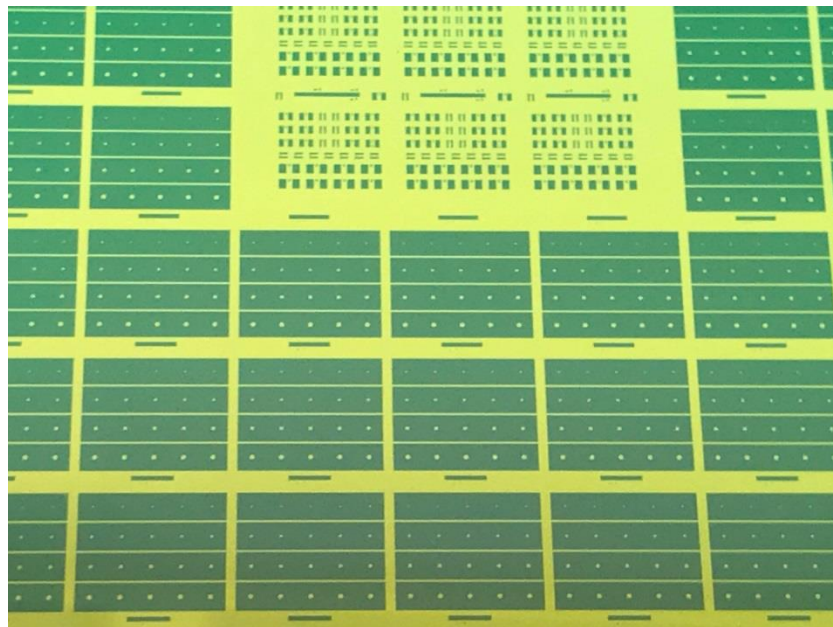


Figure 16. Close-up image of various devices on G41 after the FOX (570nm SiO₂) growth via a thermal oxidation furnace.

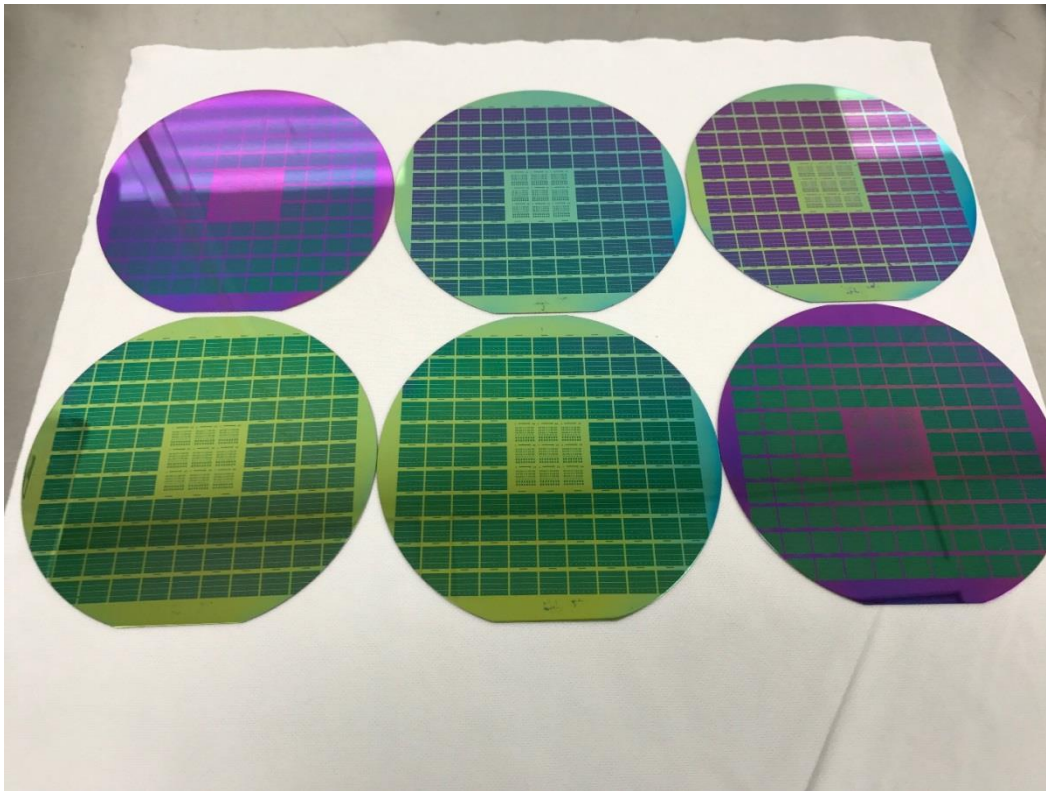


Figure 17. Image of the six 4 inch wafers currently being processed into light-emitting transistors. The top row shows (left to right) G40, G41, and G42, which are all n^{++} silicon substrates.

- The bottom row shows (left to right) G43, G44, and G45, which are all p^{++} silicon substrates. We are processing both n-type and p-type wafers in order to explore future device characteristics as we inject either hot electrons into p-type 2D semiconductors in the base region or hot holes into the n-type 2D semiconductors in the base region.

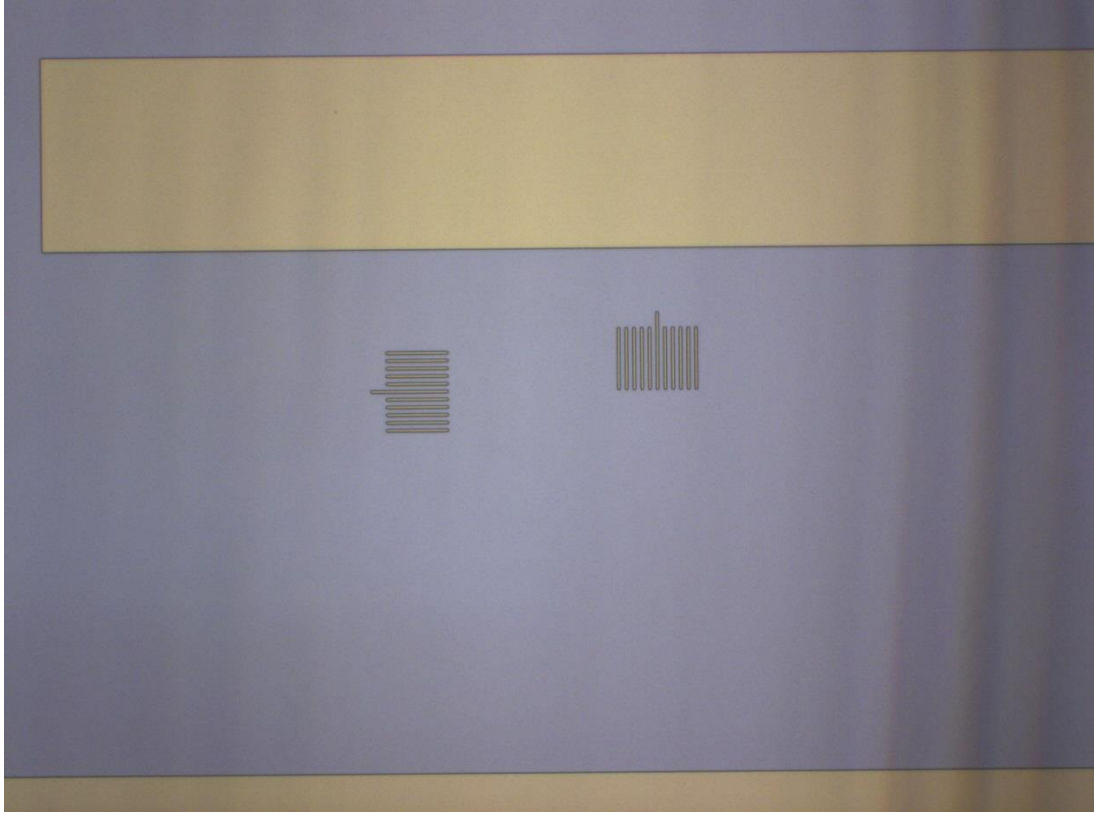


Figure 18. Optical image (10x objective lens) of G41 after the first photoresist (AZ 1512) development step. Device cross section consists of n^{++} silicon/83nm SiO_2 pad oxide/237nm Si_3N_4 hard mask/ $\sim 1.2\mu\text{m}$ AZ 1512 photoresist).

- The AZ 1512 photoresist was exposed with 11mWcm^{-2} UV light for 12 seconds using a Karl Suss MA6 photomask aligner. The AZ 1512 photoresist was developed for 15 seconds in AZ 300MIF Developer.

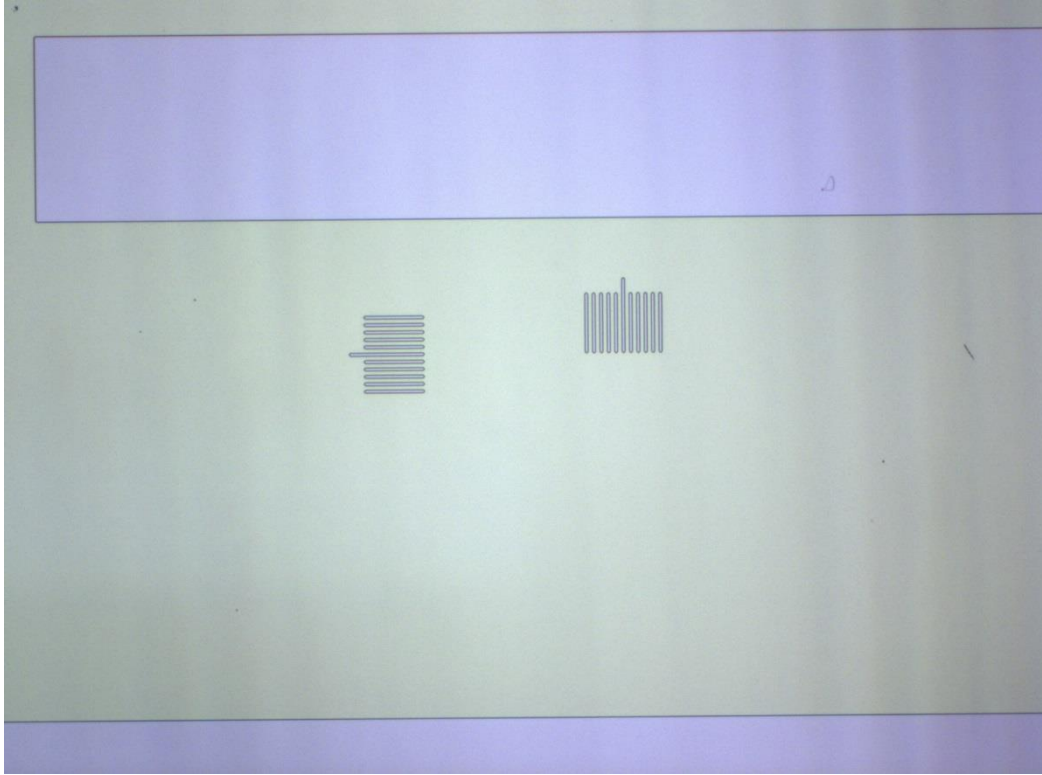


Figure 19. Optical image (10x objective lens) of G41 after the first Si_3N_4 etch using an Oxford Instruments P80 RIE (reactive ion etcher).

- The recipe used was "OPT – Basic Si_3N_4 Etch" for an etch time of 5 minutes and 11 seconds. The etch rate was tested for using control substrates prior to etching and was found to be $\sim 1.2\text{nm}$ per second. Device cross section consists of n^{++} silicon/83nm SiO_2 pad oxide/237nm Si_3N_4 hard mask/ $\sim 1.2\mu\text{m}$ AZ 1512 photoresist.

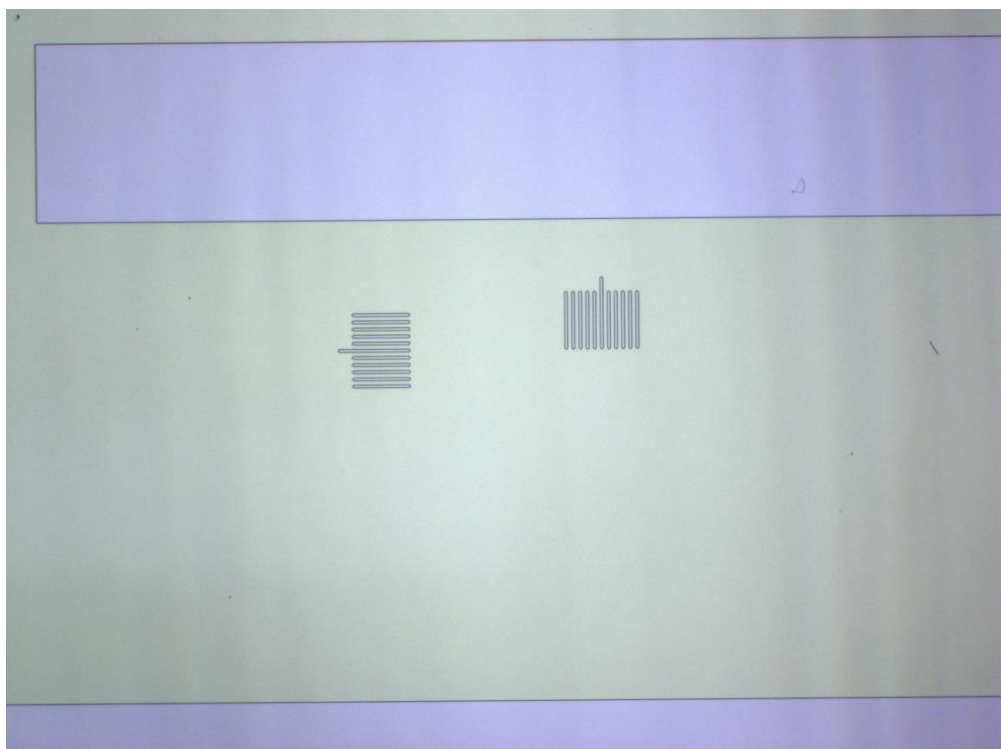


Figure 20. Optical image (10x objective lens) of G41 after the second Si_3N_4 etch using an Oxford Instruments P80 RIE (reactive ion etcher).

- The recipe used was "OPT – Basic Si_3N_4 Etch" for an etch time of 5 minutes and 11 seconds. The etch rate was tested for using control substrates prior to etching and was found to be $\sim 1.2\text{nm}$ per second. Device cross section consists of n^{++} silicon/83nm SiO_2 pad oxide/237nm Si_3N_4 hard mask.
- A second run was performed in order to make sure that we etched all the way through the device structure and into the n^{++} silicon surface. This image shows G41 after the AZ 1512 photoresist was stripped (soak G41 in a petri dish) in acetone overnight.

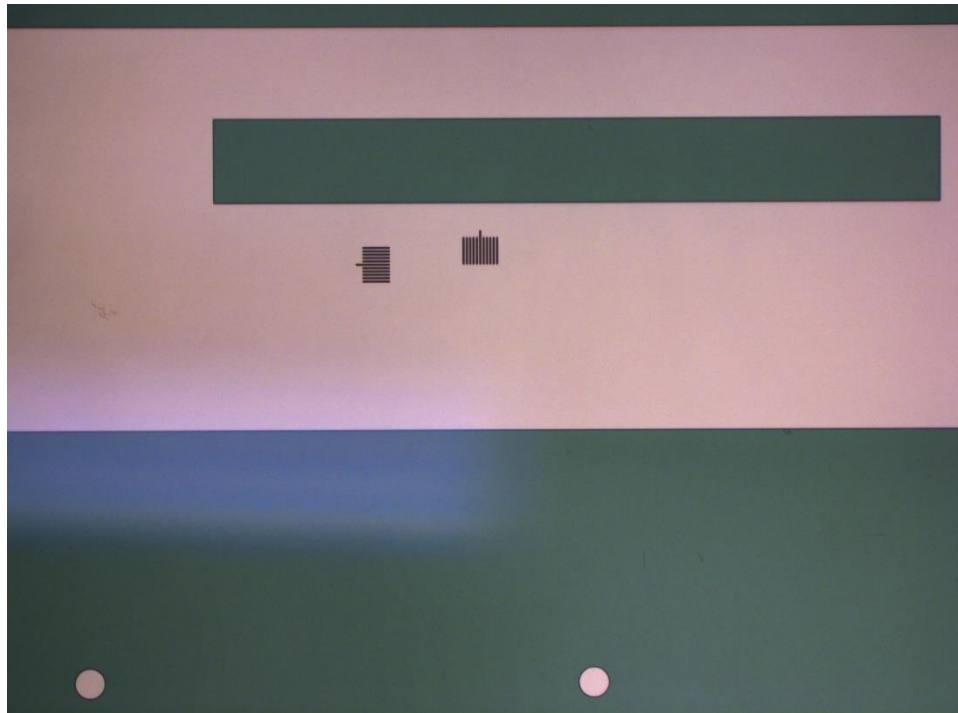


Figure 21. Optical image (5x objective lens) of G41 after the LOCOS process was complete (that is, the growth of the field oxide (FOX)).

- Device cross section consists of n^{++} silicon/83nm SiO_2 pad oxide/237nm Si_3N_4 hard mask), each of which is separated from its nearest neighbor device via a around 570nm thick SiO_2 FOX.

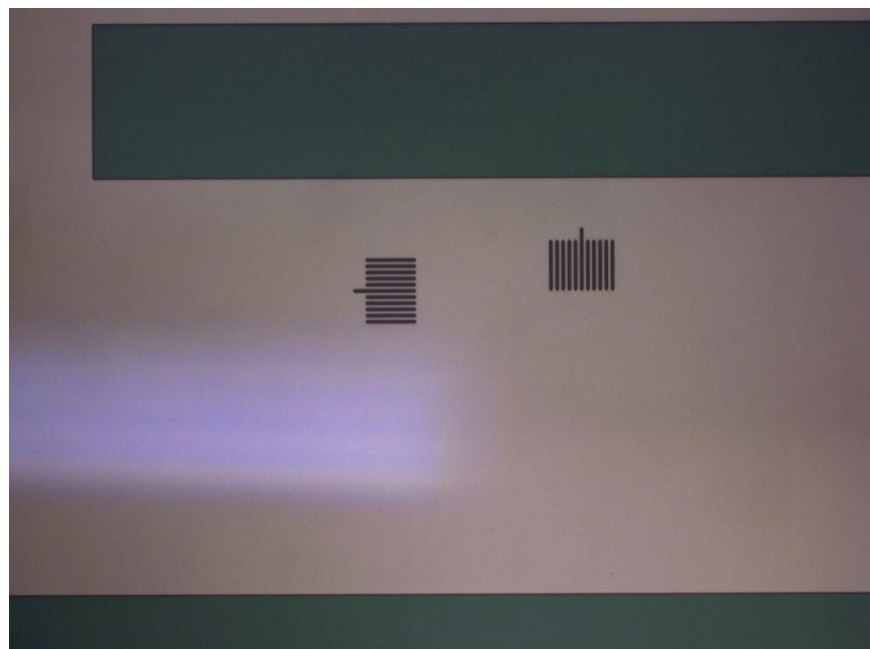


Figure 22. Optical image (10x objective lens) of G41 after the LOCOS process was complete (that is, the growth of the field oxide (FOX)). Device cross section consists of n^{++} silicon/83nm SiO_2 pad oxide/237nm Si_3N_4 hard mask), each of which is separated from its nearest neighbor device via a around 570nm thick SiO_2 FOX.

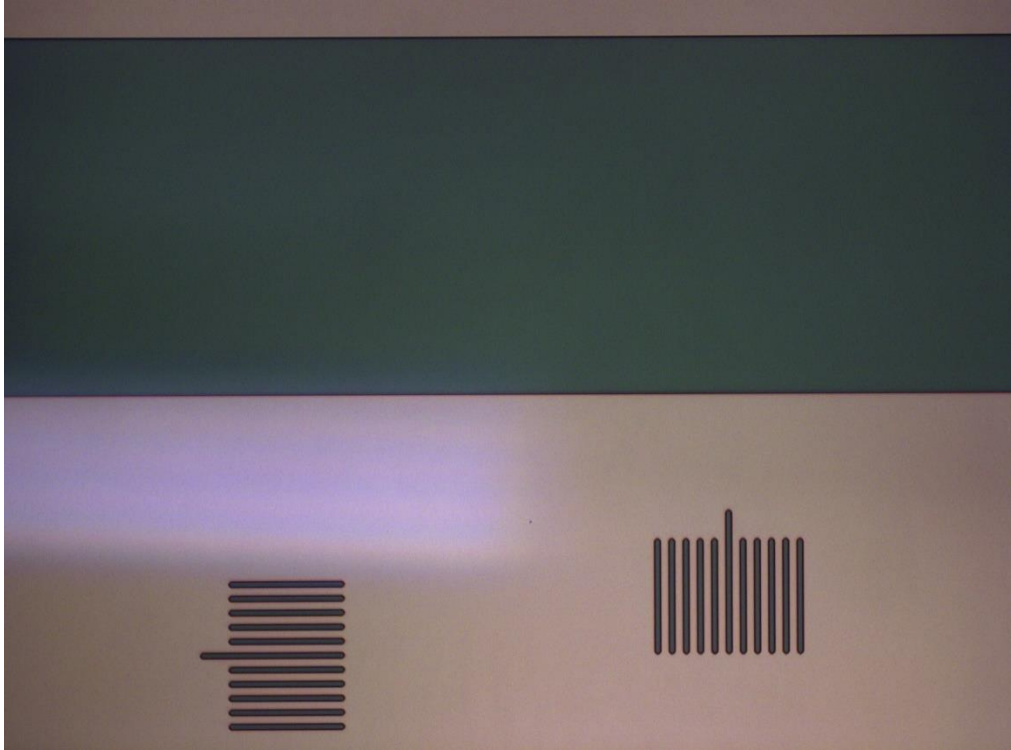


Figure 23. Optical image (20x objective lens) of G41 after the LOCOS process was complete (that is, the growth of the field oxide (FOX)).

- Device cross section consists of n^{++} silicon/83nm SiO_2 pad oxide/237nm Si_3N_4 hard mask), each of which is separated from its nearest neighbor device via a around 570nm thick SiO_2 FOX.

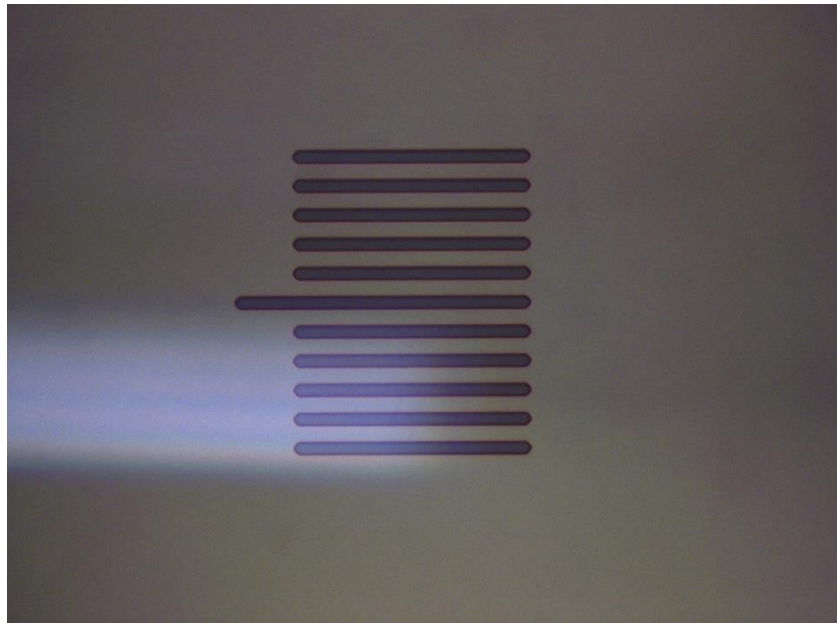


Figure 24. Optical image (50x objective lens) of G41 after the LOCOS process was complete (that is, the growth of the field oxide (FOX)).

- Device cross section consists of n^{++} silicon/83nm SiO_2 pad oxide/237nm Si_3N_4 hard mask), each of which is separated from its nearest neighbor device via a around 570nm thick SiO_2 FOX. Note that this image shows an alignment marker which will be used in the subsequent 4 remaining photolithography steps for the fabrication of the LETs. The linewidth of a single line is $3\mu\text{m}$.

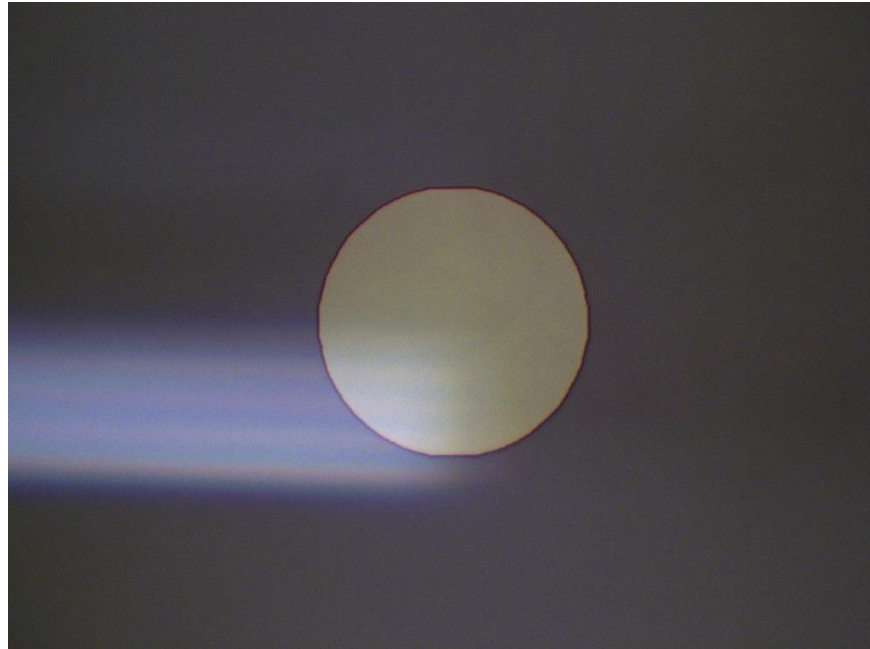


Figure 25. Optical image (50x objective lens) of G41 after the LOCOS process was complete (that is, the growth of the field oxide (FOX)).

- Device cross section consists of n^{++} silicon/83nm SiO_2 pad oxide/237nm Si_3N_4 hard mask), each of which is separated from its nearest neighbor device via a around 570nm thick SiO_2 FOX. Note that this image shows the Si_3N_4 hard mask covering the device active region for a device in Row 1 of the 4x5 matrix (top-most row). The diameter of this Si_3N_4 hard mask is $90\mu\text{m}$.

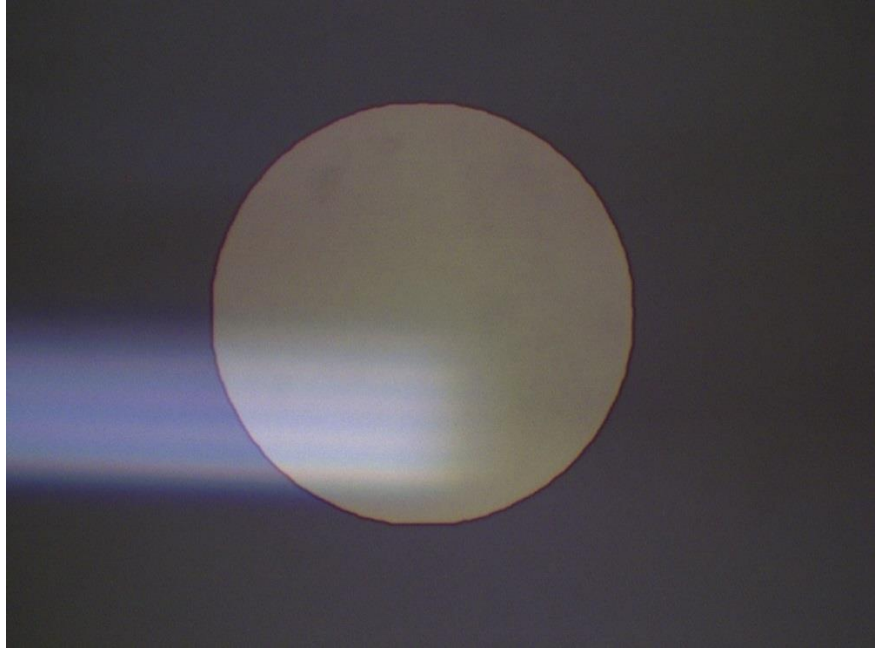


Figure 26. Optical image (50x objective lens) of G41 after the LOCOS process was complete (that is, the growth of the field oxide (FOX)).

- Device cross section consists of n^{++} silicon/83nm SiO_2 pad oxide/237nm Si_3N_4 hard mask), each of which is separated from its nearest neighbor device via a around 570nm thick SiO_2 FOX. Note that this image shows the Si_3N_4 hard mask covering the device active region for a device in Row 2 of the 4x5 matrix (second row from the top). The diameter of this Si_3N_4 hard mask is 140 μm .

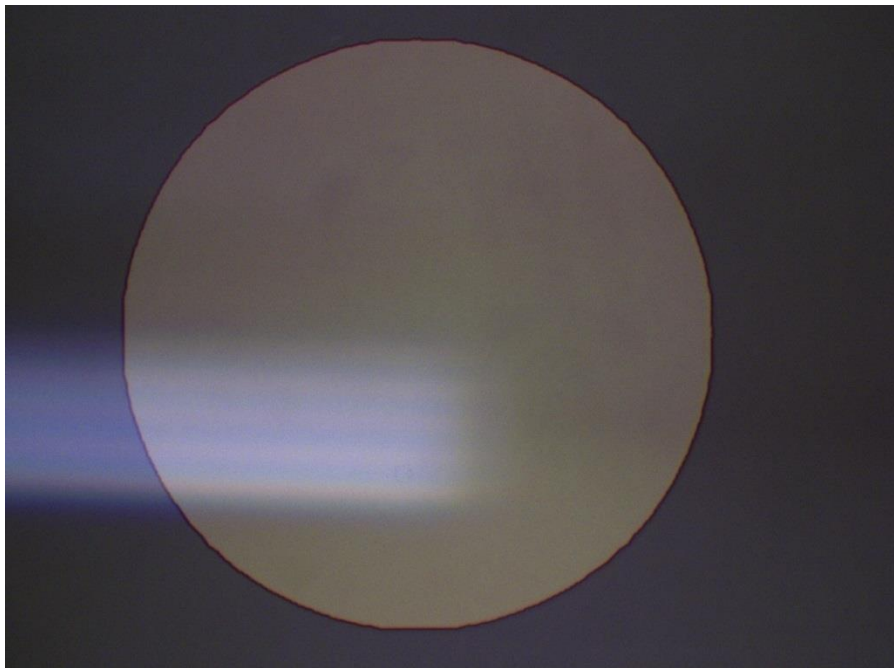


Figure 27. Optical image (50x objective lens) of G41 after the LOCOS process was complete (that is, the growth of the field oxide (FOX)).

- Device cross section consists of n^{++} silicon/83nm SiO_2 pad oxide/237nm Si_3N_4 hard mask), each of which is separated from its nearest neighbor device via a around 570nm thick SiO_2 FOX. Note that this image shows the Si_3N_4 hard mask covering the device active region for a device in Row 3 of the 4x5 matrix (third row from the top). The diameter of this Si_3N_4 hard mask is 190 μm .

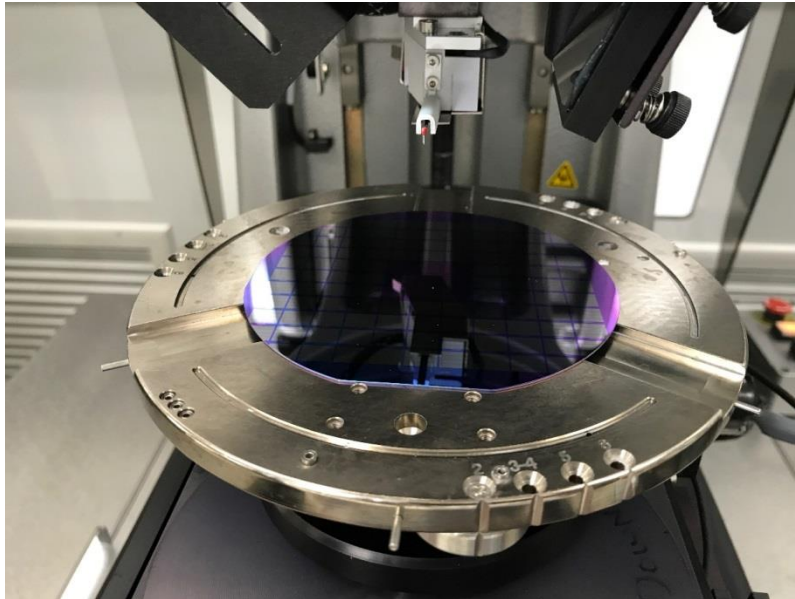


Figure 28. Image of G45, one of the 4 inch (100mm) wafers being processed, that is about to be probed by the DekTak 150 stylus profilometer.

- The stylus raster scans the substrate surface based on a defined scan rate, distance, and resolution in order to measure step heights, etc.

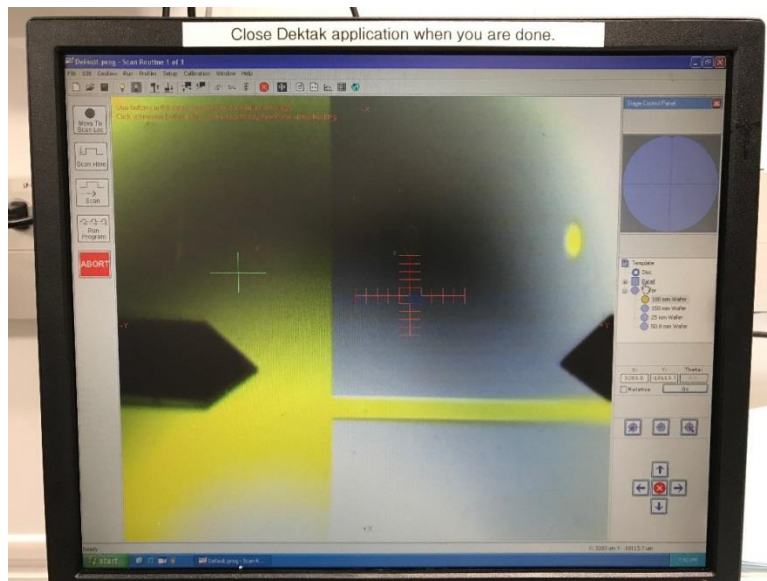


Figure 29. Image of the monitor (e.g. sample positioning window) connected to the DekTak 150 stylus profilometer. The stylus raster scans the substrate surface based on a defined scan rate, distance, and resolution in order to measure step heights, etc.

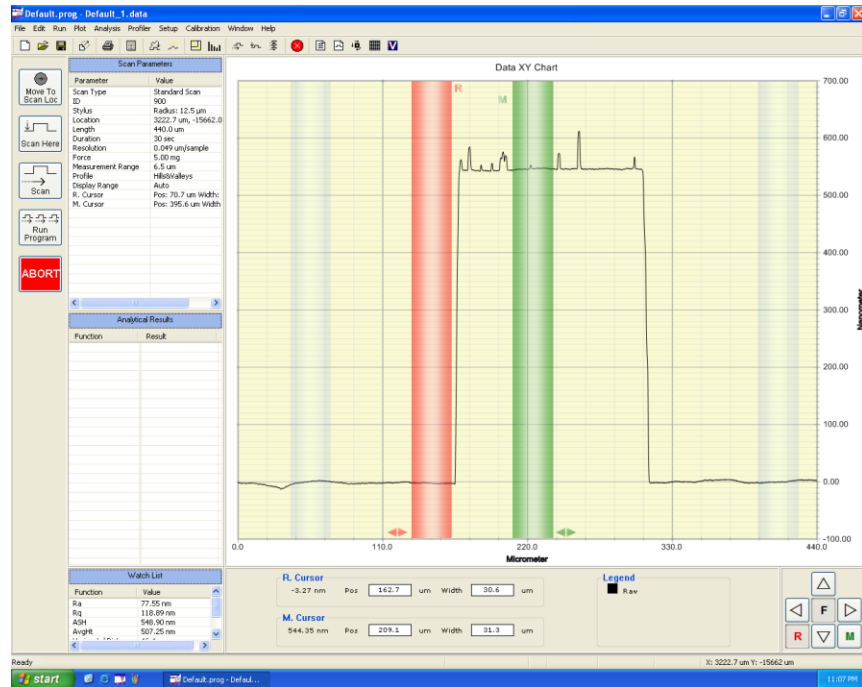


Figure 30. Image of the monitor (e.g. data analysis window) connected to the DekTak 150 stylus profilometer that probes G41.

- This shows an average step height (ASH) of around 549nm between the n^{++} silicon surface and the top surface of the Si_3N_4 hard mask for a particular device just after the photoresist was stripped in acetone overnight. The step after this was to grow the field oxide in the thermal oxidation furnace (around 550nm SiO_2 expected thickness for WET 1050°C recipe for a growth time of 1 hour, 6 minutes, and 5 seconds).

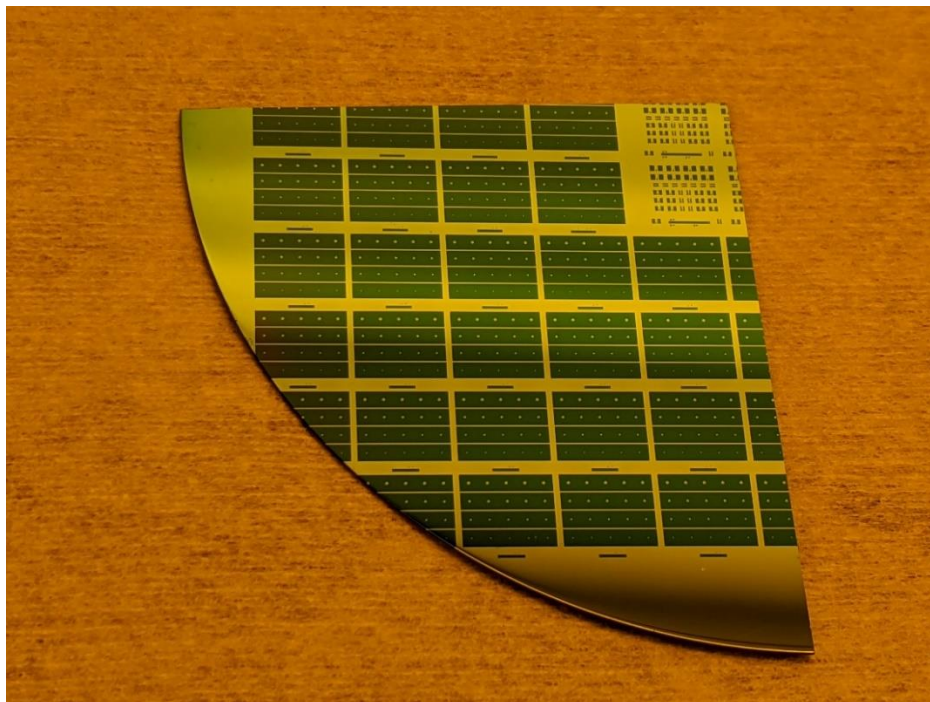


Figure 31. Image of a quadrant of G41 after the field oxide (FOX) growth in an oxidation furnace and prior to hot phosphoric acid etching of the silicon nitride hard masks.



Figure 32. Image of the hot phosphoric acid etching step in the fabrication process. A beaker is filled with 600 mL of phosphoric (H_3PO_4) acid and is placed on a hot plate.

- The phosphoric acid is ramped up to 170°C . Once this setpoint has been reached, the Si_3N_4 etching step is timed for 1 hour at this steady state temperature. Afterwards, the hot plate is turned off and the phosphoric acid is cooled down to room temperature.

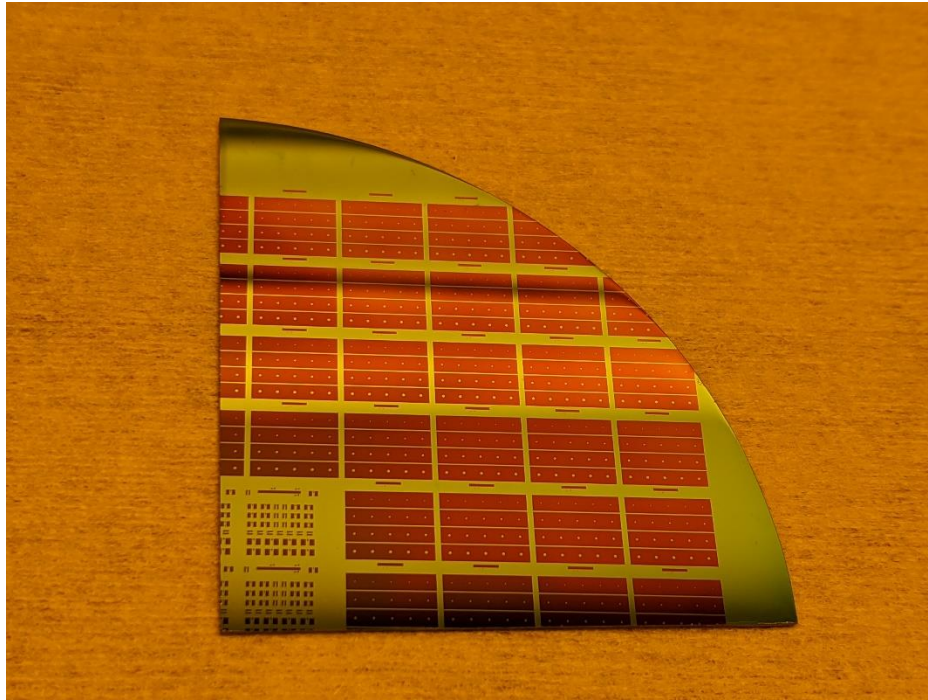


Figure 33. Image of a quadrant of G41 after the hot phosphoric acid etching of the silicon nitride hard masks.

- Note that we eventually dice this quadrant into several smaller substrates to serve as the platform for future 2D-LETs with different 2D materials transferred onto them. The next step will be to grow the tunnel oxide barrier for the hot electron injection via a rapid thermal annealer.

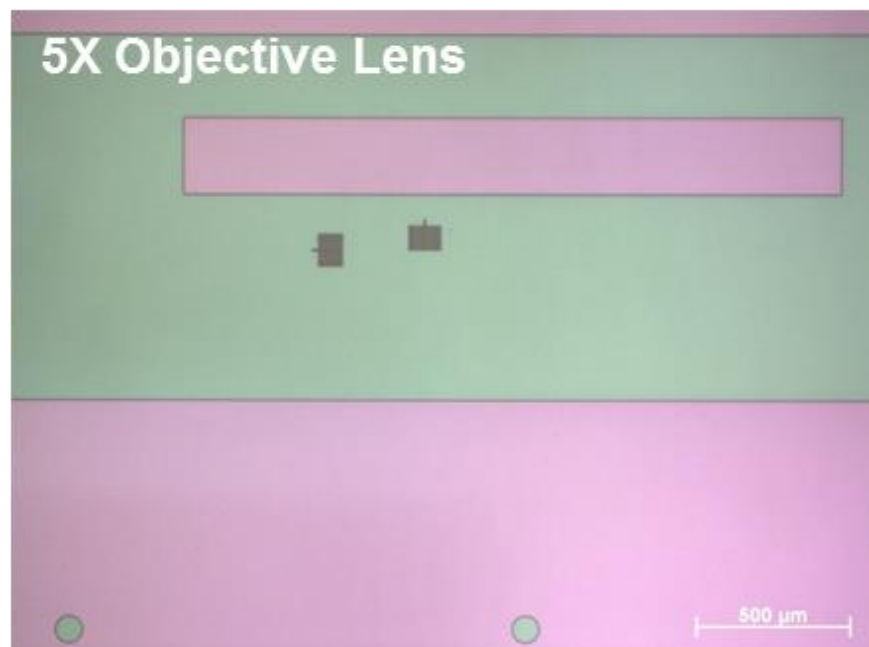


Figure 34. Optical image (5X objective lens) of G41_Q3_LET_n⁺⁺ substrate after etching away the Si₃N₄ masks used in the LOCOS (LOCAl Oxidation of Silicon) process.

- The etching was performed in hot phosphoric acid (around 170°C for 1 hour steady state). The scale bar is 500µm. The few green colored circles near the bottom of the image are device active regions that lie on the first row of the 4x5 matrix.

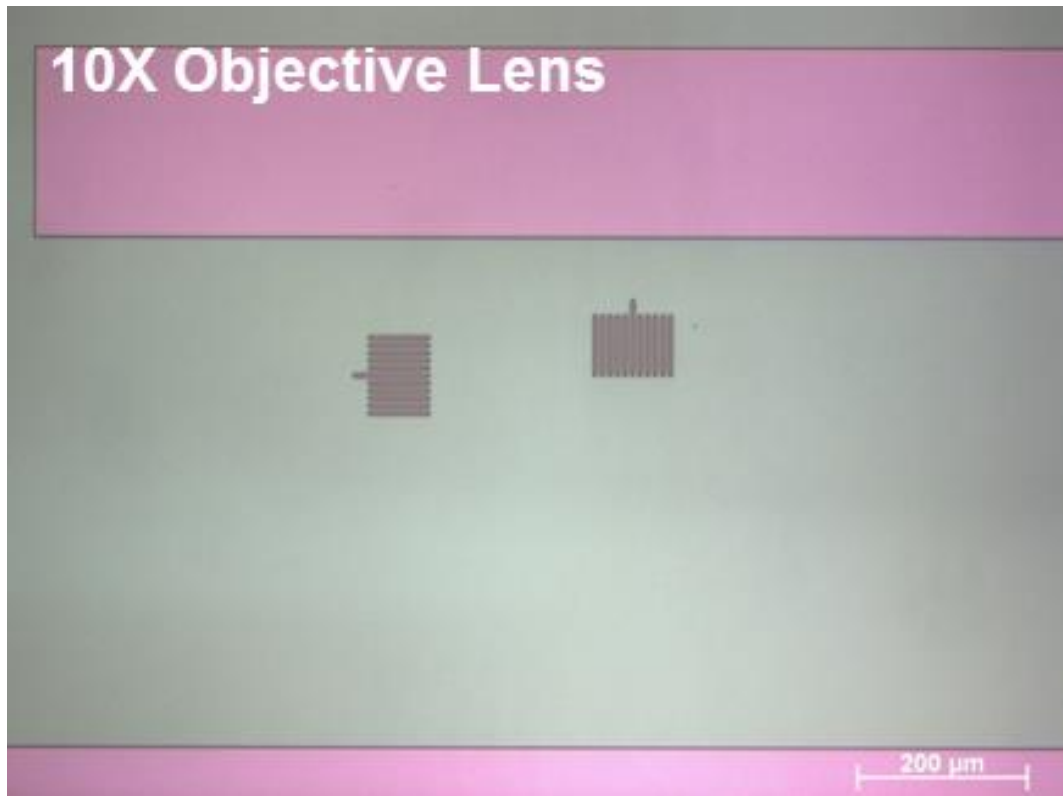


Figure 35. Optical image (10X objective lens) of G41_Q3_LET_n⁺⁺ substrate after etching away the Si₃N₄ masks used in the LOCOS (LOCal Oxidation of Silicon) process.

- The etching was performed in hot phosphoric acid (around 170°C for 1 hour steady state). The scale bar is 200µm.

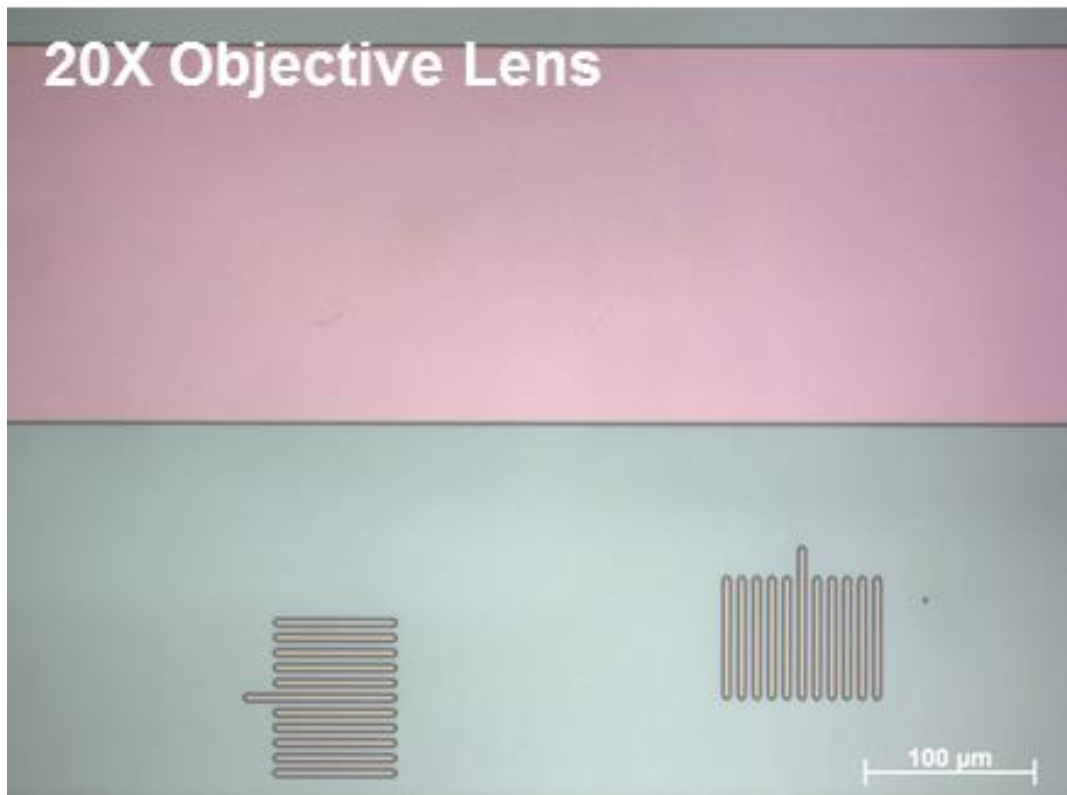


Figure 36. Optical image (20X objective lens) of G41_Q3_LET_n⁺⁺ substrate after etching away the Si₃N₄ masks used in the LOCOS (LOCAl Oxidation of Silicon) process.

- The etching was performed in hot phosphoric acid (around 170°C for 1 hour steady state). The scale bar is 100μm.

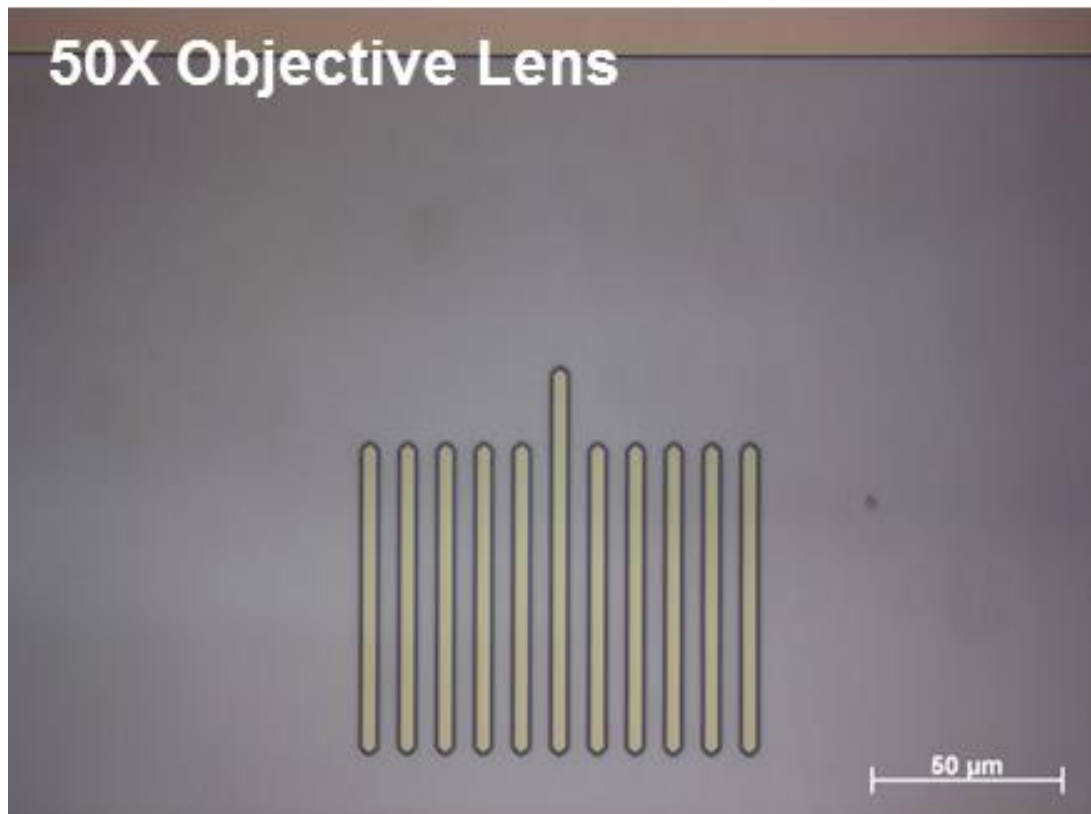


Figure 37. Optical image (50X objective lens) of G41_Q3_LET_n⁺⁺ substrate after etching away the Si₃N₄ masks used in the LOCOS (LOCal Oxidation of Silicon) process.

- The etching was performed in hot phosphoric acid (around 170°C for 1 hour steady state). The scale bar is 50μm. This image focuses on the alignment markers which will be used as a reference in the subsequent 4 remaining photolithography steps. The linewidth of each line is 3μm (e.g. minimum feature size of our LETs).

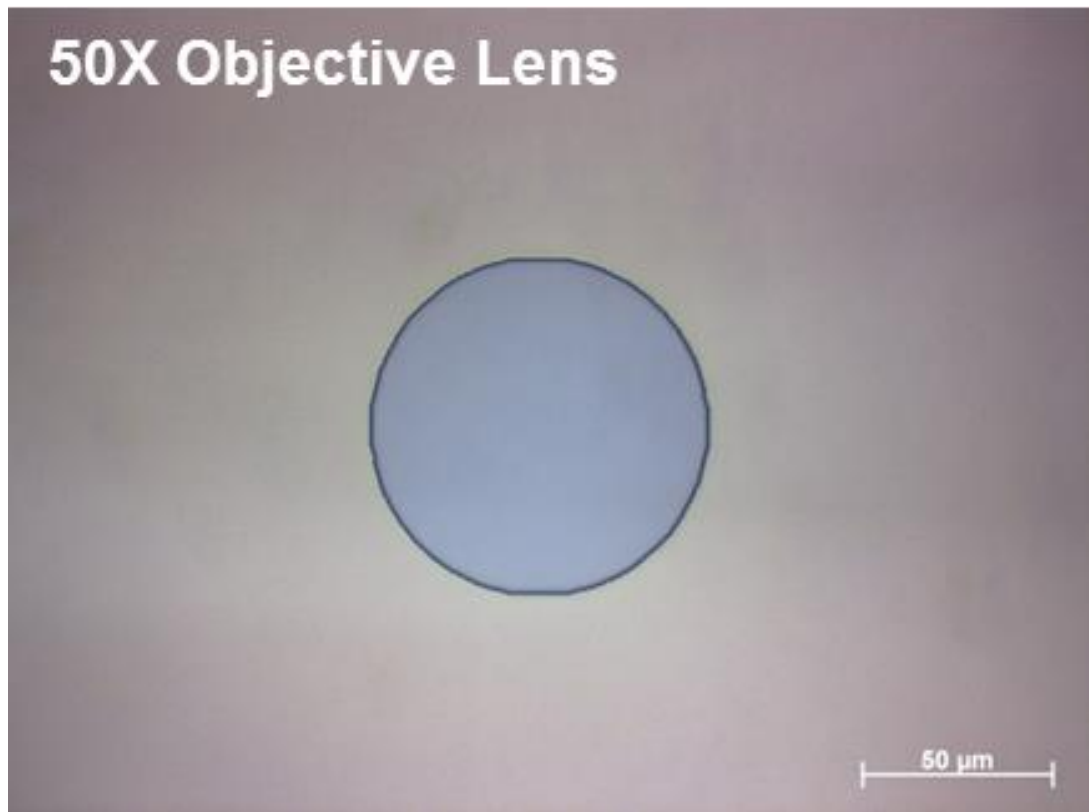


Figure 38. Optical image (50X objective lens) of G41_Q3_LET_n⁺⁺ substrate after etching away the Si₃N₄ masks used in the LOCOS (LOCal Oxidation of Silicon) process.

- The etching was performed in hot phosphoric acid (around 170°C for 1 hour steady state). The scale bar is 50μm. This image focuses on the active region (e.g. hot electron injection region) of a particular device located in the first row from the top of the 4x5 matrix. It features a diameter of 90μm.

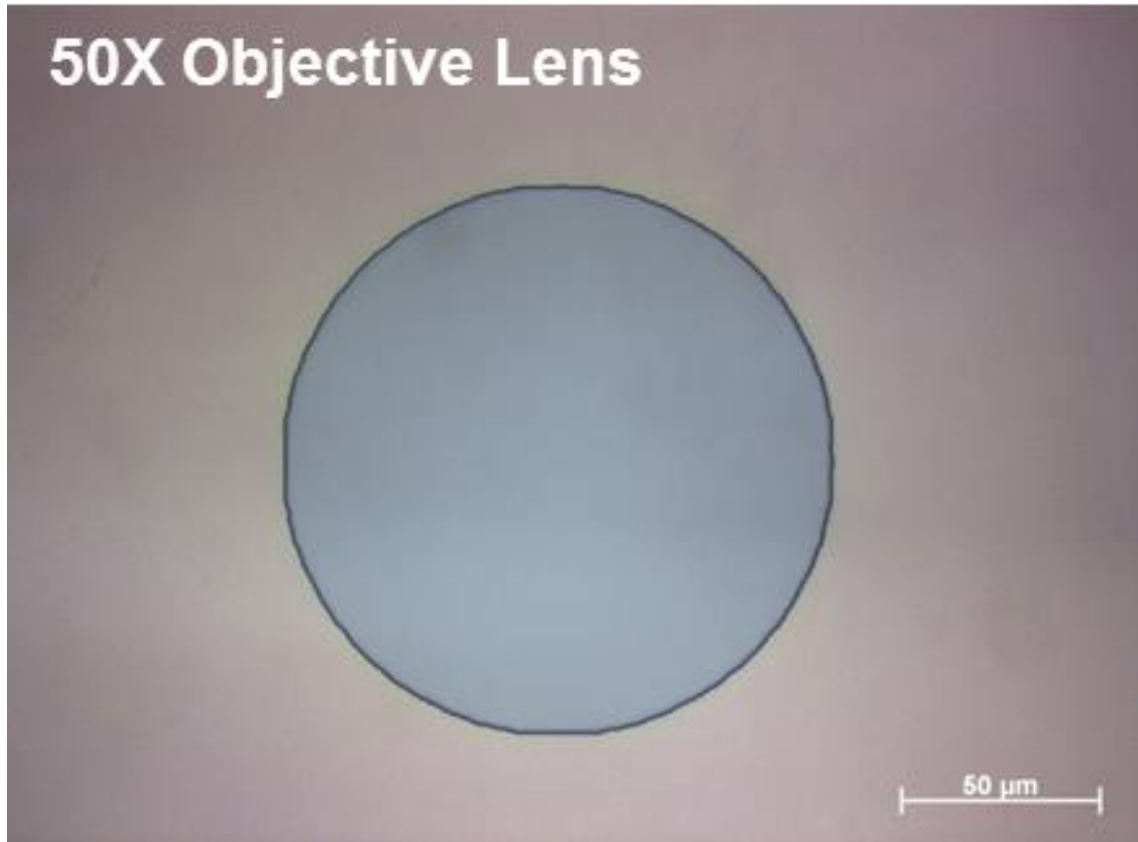


Figure 39. Optical image (50X objective lens) of G41_Q3_LET_n⁺⁺ substrate after etching away the Si₃N₄ masks used in the LOCOS (LOCal Oxidation of Silicon) process.

- The etching was performed in hot phosphoric acid (around 170°C for 1 hour steady state). The scale bar is 50μm. This image focuses on the active region (e.g. hot electron injection region) of a particular device located in the second row from the top of the 4x5 matrix. It features a diameter of 140μm.

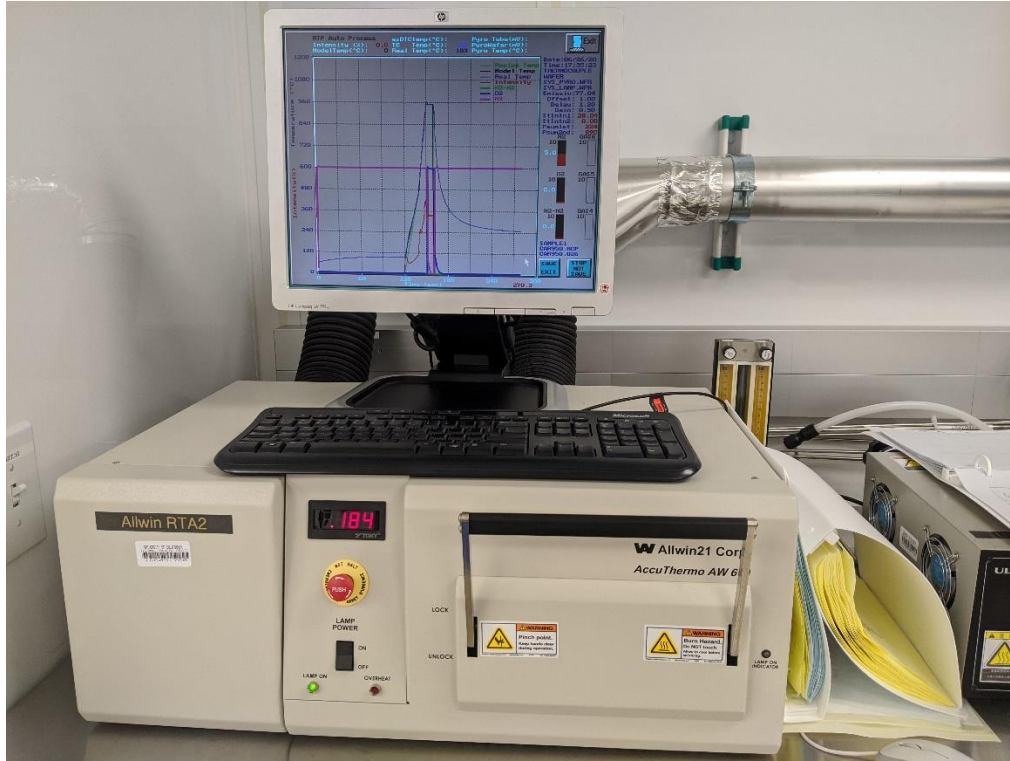


Figure 40. Growing a thin tunnel oxide barrier using rapid thermal processing.

- An Allwin21 AccuThermo AW600 rapid thermal annealer is utilized to grow a thin 2-3nm thick SiO_2 tunnel barrier on top of the exposed degenerately doped silicon surfaces located at the active regions of the devices.
- This procedure involves rapidly heating the substrate to a desired temperature and keeping it steady state for a short duration while introducing oxygen to grow the tunnel barrier. The particular recipe used was:
- DELAY 120 sec at 5 SLPM N_2 gas, RAMP to 475°C within 20 sec at 5 SLPM N_2 gas, RAMP to 950°C within 10 sec at 5 SLPM N_2 gas, STEADY at 950°C for 10 sec at 5 SLPM O_2 gas, and DELAY 120 sec at 5 SLPM N_2 gas.
- Note that prior to this step, the quadrant substrate was diced into several substrates for different device processing parameters (e.g. different 2D materials transferred onto them, different thicknesses of tunnel barriers, etc.).
- We also had to dip each of the substrates into buffered oxide etchant (BOE (6:1)) for 30 seconds to etch away any SiO_2 pad oxide that remained after the Si_3N_4 hard masks were etched away in order to expose the fresh surface of degenerately doped silicon for tunnel barrier growth.

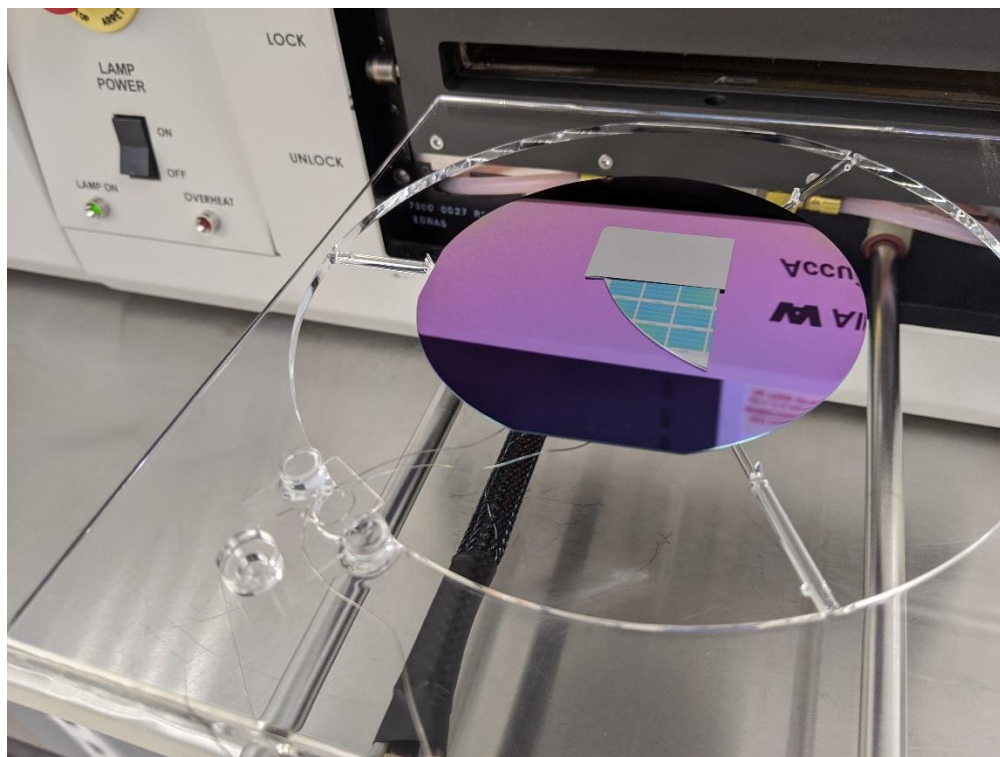


Figure 41. A substrate diced from the G41 quadrant shown in Figure 32 as well as a control silicon substrate (dipped in BOE (6:1) for 30 seconds to remove any native oxide) are placed onto a SiO_2 loading substrate with K type thermocouple touching the backside of the 4 inch SiO_2 /Silicon wafer.

- These substrates are loaded into the rapid thermal annealer shown in Figure 40 in order to grow the tunnel barriers. Note that the control substrate will serve as a reference during ellipsometer measurements (e.g. to ascertain the SiO_2 thickness) and will be fabricated into a metal-insulator-semiconductor (MIS) capacitor structure to perform I-V, C-V, and small-bias resistance versus temperature (R vs T) measurements to confirm negligible pinholes in the tunnel oxide barriers.

Now that we have grown the tunnel barriers at the various active regions of our 2D-LET substrate (these active device regions are surrounded by the thick SiO_2 field oxide), we are ready to transfer the chemical vapor deposited (CVD) large-area 2D materials onto the 2D-LET substrate.



Figure 42. CVD MoS₂ on sapphire substrate purchased from 2D Semiconductors, Inc.

- The sapphire substrate with the CVD MoS₂ is shown to the right of the sample case and on top of a large microscope slide. Note that we purchased various transition metal dichalcogenides (MoS₂, MoSe₂, WS₂, WSe₂) from the vendor to make various types of TMD-LETs.



Figure 43. Spin coating PMMA polymer onto the CVD 2D material on top of sapphire substrate to assist the 2D material wet transfer onto arbitrary substrates.

- We place the CVD MoS_2 /sapphire substrate onto the spin coater and drop cast 950 PMMA C4 to cover the entire substrate. We then run the recipe shown in Figure 44. Afterwards, we place the sapphire substrate onto a hotplate heated to 100°C for 1 minute. We then let the substrate cool and use a sharp tweezer to scratch off the top edge perimeter of the PMMA/2D material to allow for future intercalation of BOE or water to delaminate the PMMA/2D material from the underlying sapphire substrate.

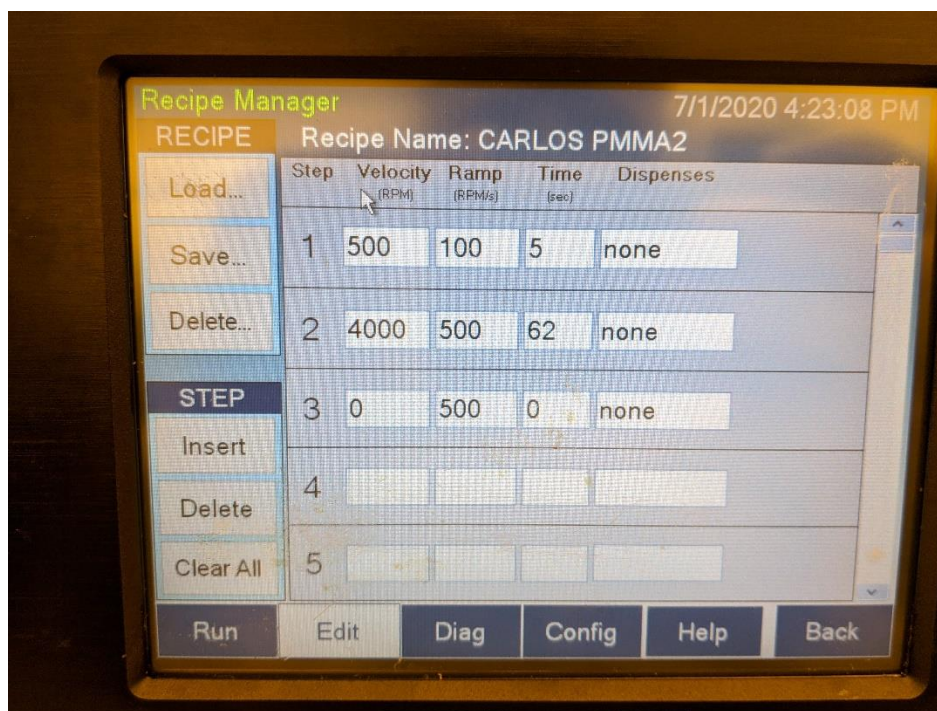


Figure 44. Recipe used to spin coat the PMMA polymer onto the CVD 2D material/sapphire substrate.

- The 4000 rpm for 1 minute spin coat should result in about 500nm thick PMMA which will serve as a support for the CVD 2D material during the wet transfer onto arbitrary substrates.



Figure 45. Polypropylene fume hood with secondary container for working with hydrofluoric (HF) acid and buffered oxide etchant (BOE).

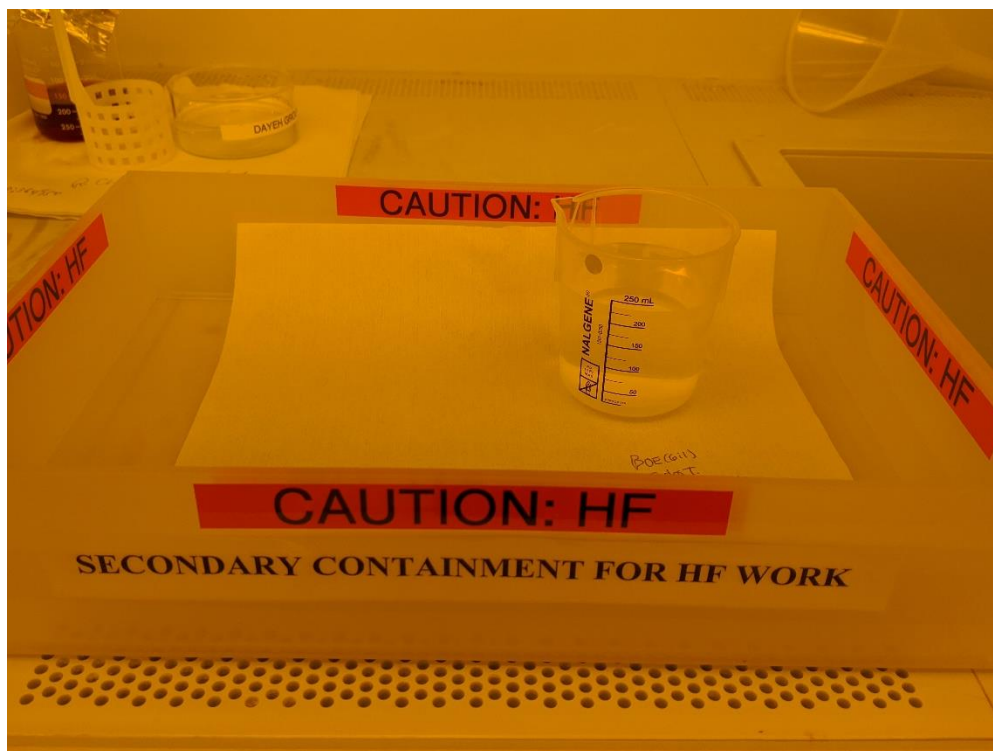


Figure 46. Using the proper personal protective equipment (PPE) to work with HF/BOE (see Figure 13), we prepare our workspace in the fume hood using the secondary container for HF work.

- We pour some BOE (6:1) into a plastic beaker (e.g. HF/BOE etches glassware) and use a tweezer to grab the CVD MoS₂/sapphire substrate and place it floating on top of the BOE solution inside this beaker. We gently push the sapphire substrate into the BOE solution along the various edges so that some BOE can accumulate at the top surface edges of the sapphire substrate (e.g. the perimeter of PMMA that we previously scratched away).



Figure 47. Close up view of the CVD 2D material/sapphire substrate floating on the surface of the BOE solution in the beaker shown in Figure 46.

- Eventually, the BOE solution starts to intercalate between the interface of the 2D material and the sapphire substrate in order to delaminate the 2D material and allow the sapphire substrate to sink in the BOE, while the PMMA/2D material floats on the surface of the BOE.



Figure 48. Close up view of the PMMA/CVD 2D material naturally being delaminated from the sapphire substrate prior to the sapphire substrate sinking into the BOE solution.

- Afterwards, we scoop up the PMMA/2D material from the BOE surface using a fresh silicon substrate and place it onto the surface of deionized water in a petri dish to clean away the BOE residue. Eventually, we will scoop up the PMMA/2D material onto our target substrate, which is the 2D-LET substrate shown in Figure 49.

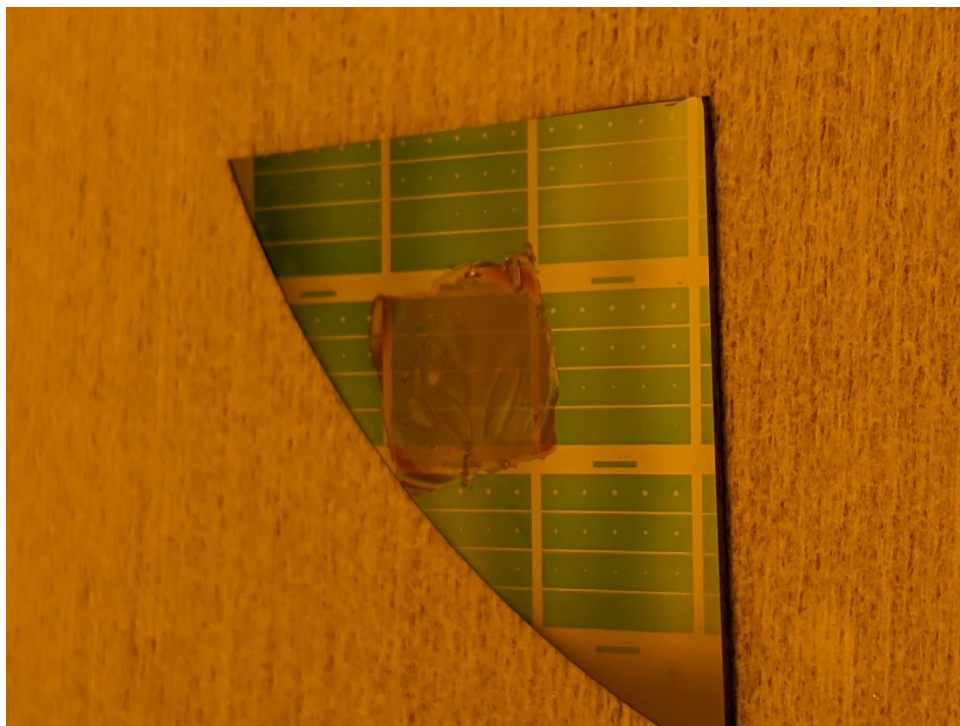


Figure 49. PMMA/CVD 2D material after wet transfer onto a 2D-LET substrate.

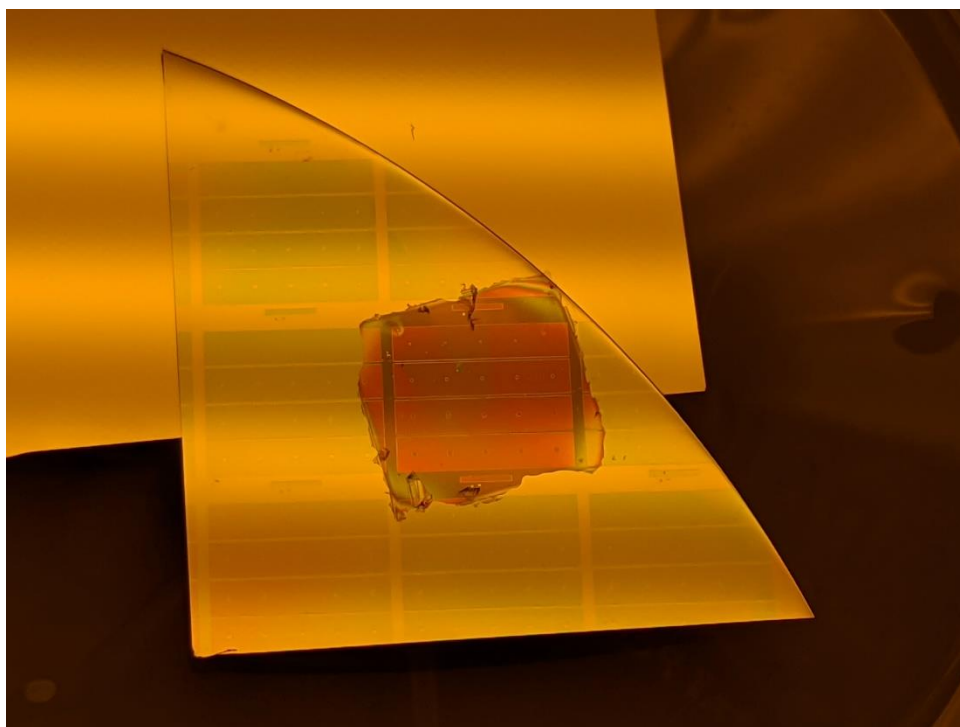


Figure 50. PMMA/CVD 2D material transferred onto a 2D-LET substrate after drying overnight.

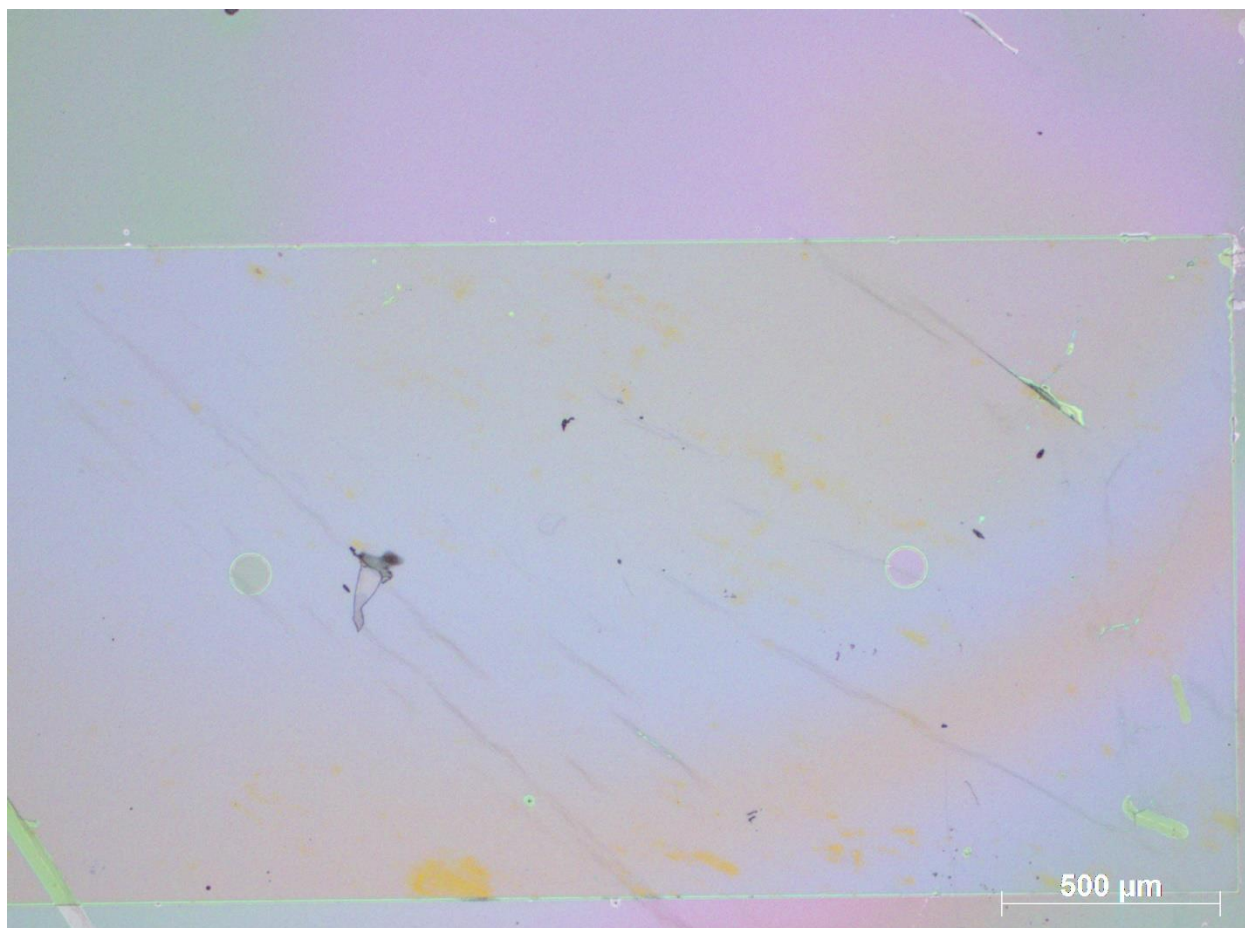


Figure 51. Optical micrograph of a 2D-LET substrate with PMMA/CVD 2D material transferred and dried overnight.

- The figure shows two active device regions (circles) covered by the PMMA/CVD 2D material. Scale bar is 500μm.



Figure 52. Optical micrograph of a 2D-LET substrate after the PMMA on top of the CVD 2D material was dissolved in acetone overnight.

- The figure shows two active device regions (circles) covered by the CVD 2D material. Scale bar is 500μm.



Figure 53. The PI performs metallization on the 2D-LET substrates using a Temescal BJD 1800 e-beam evaporator in the UCSD Nano3 cleanroom.

- The 3.5nm Aluminum protection layer deposited in Figure 54 is performed at a deposition pressure of $\sim 7 \times 10^{-7}$ Torr and at a deposition rate of ~ 0.3 Angstroms/second.

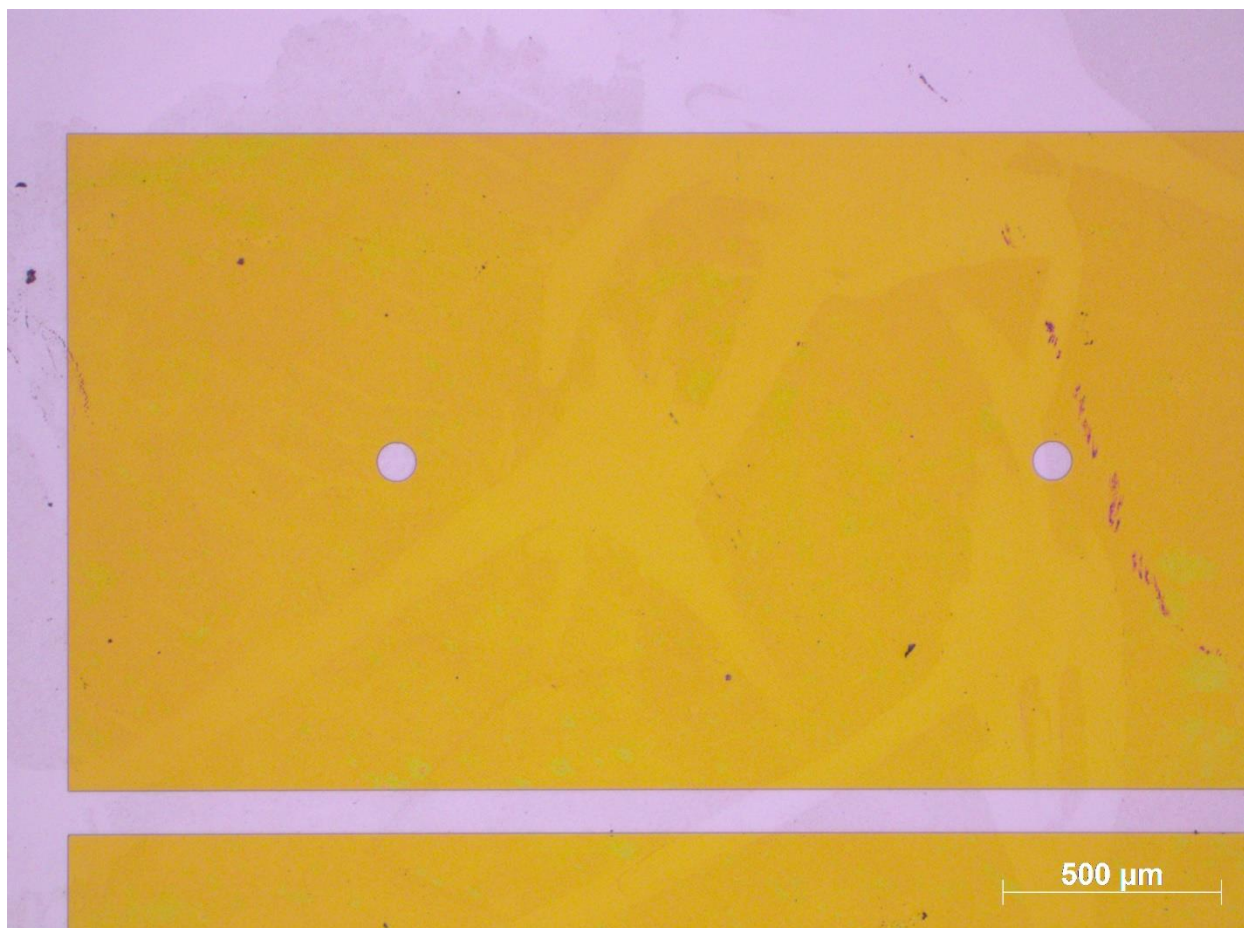


Figure 54. Optical micrograph of a 2D-LET substrate after a 3.5nm Aluminum protection layer was e-beam evaporated using a Temescal BJD 1800 e-beam evaporator to protect the CVD 2D material from directly contacting photoresist in the future fabrication processing steps. Scale bar is 500μm.

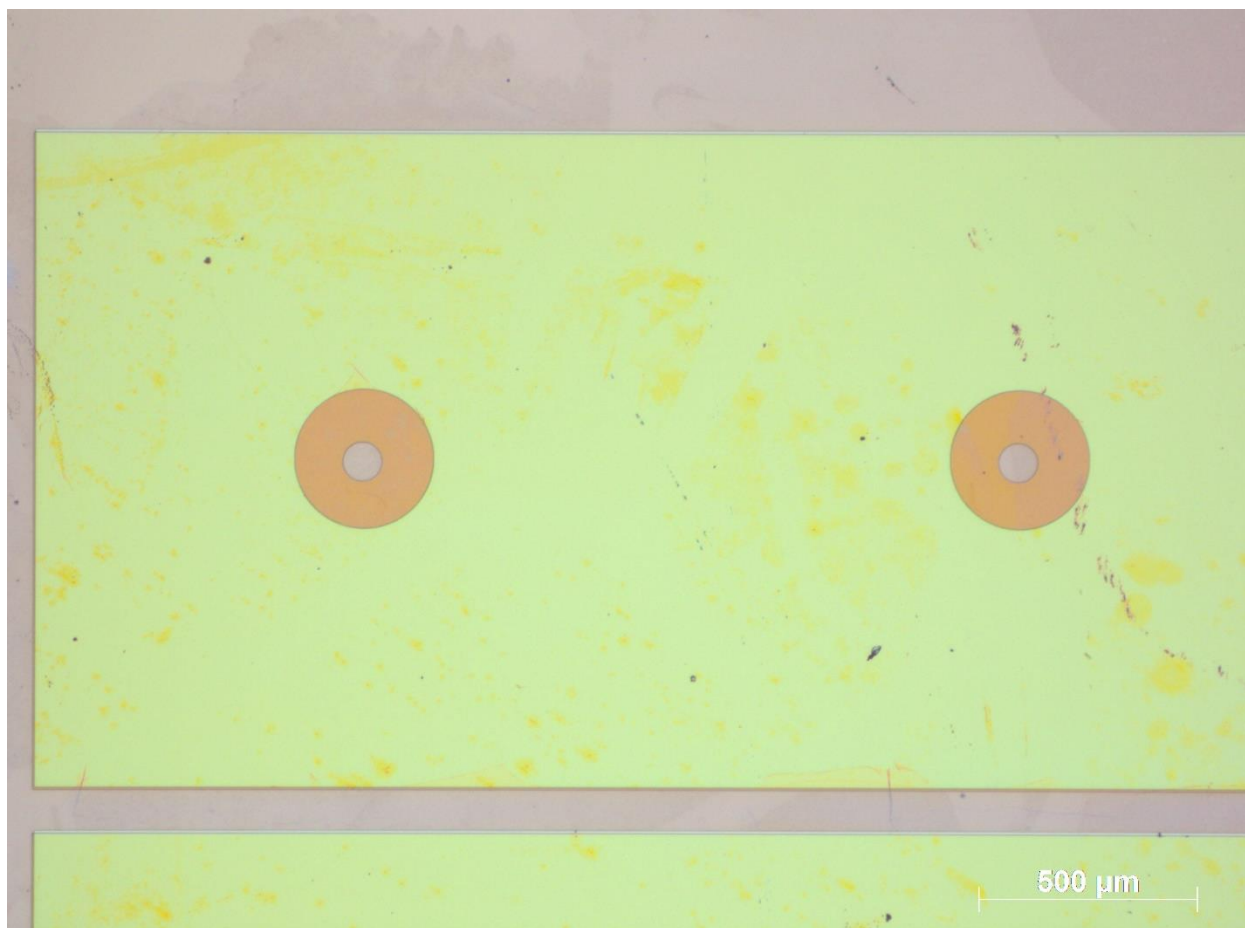


Figure 55. Optical micrograph of a 2D-LET substrate after the second photolithography step was completed to define circular masks to protect the CVD 2D material from being etched away in a future fabrication processing step. Scale bar is 500μm.

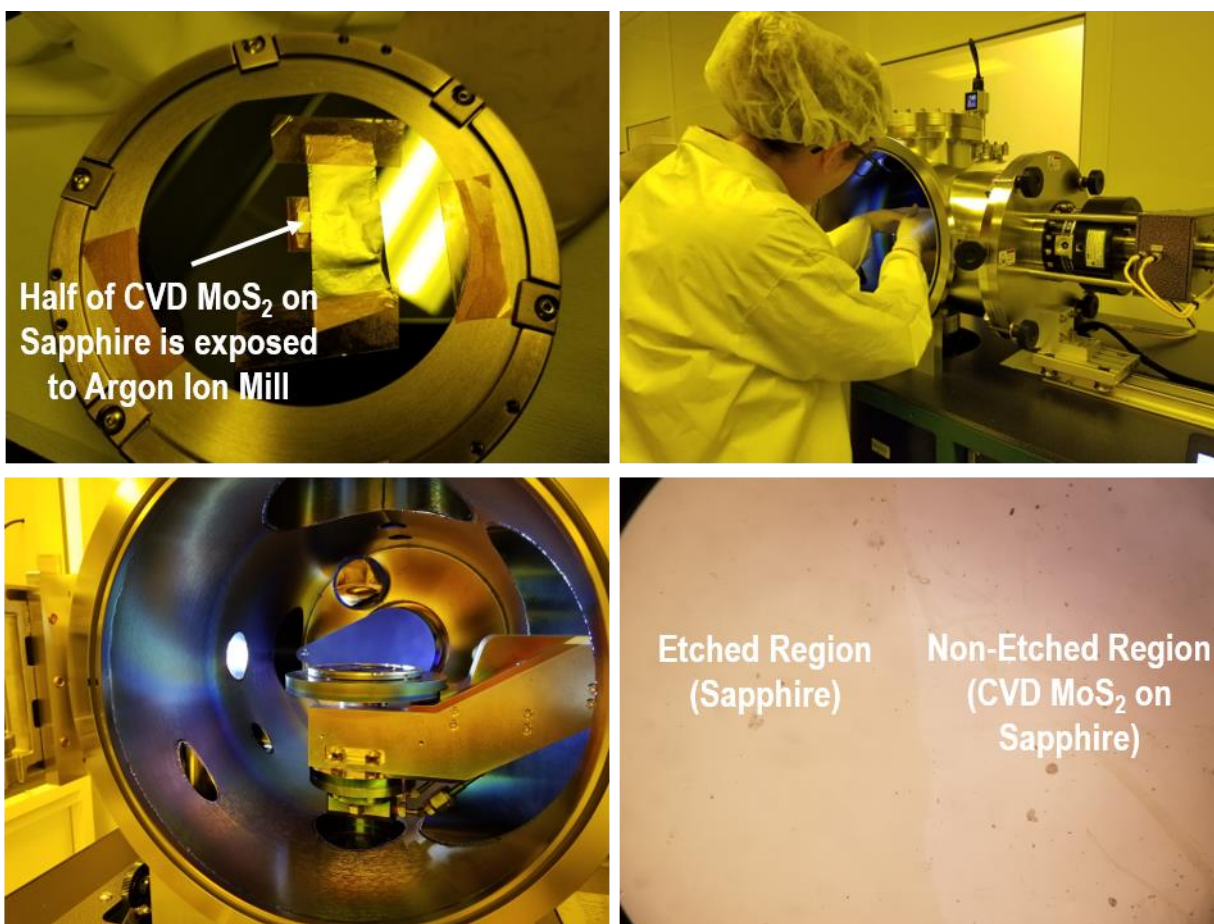


Figure 56. We next use an AJA Orion Series Argon Ion Mill at the NIWC Pacific Battery Ashburn cleanroom facility to test the etching of monolayer CVD MoS₂ on sapphire substrates.

- An optical image taken with a cell phone camera as seen through the objective lens is shown on the bottom right figure.
- The parameters used during the etching were: Argon gas flow at 10sccm at a chamber pressure of 12mTorr during milling for 30 seconds.
- Since we know that the argon ion mill etches the CVD 2D material, we then use it to etch away the regions of the CVD 2D material that are not covered by the circular masks defined in the second photolithography step shown in Figure 55.

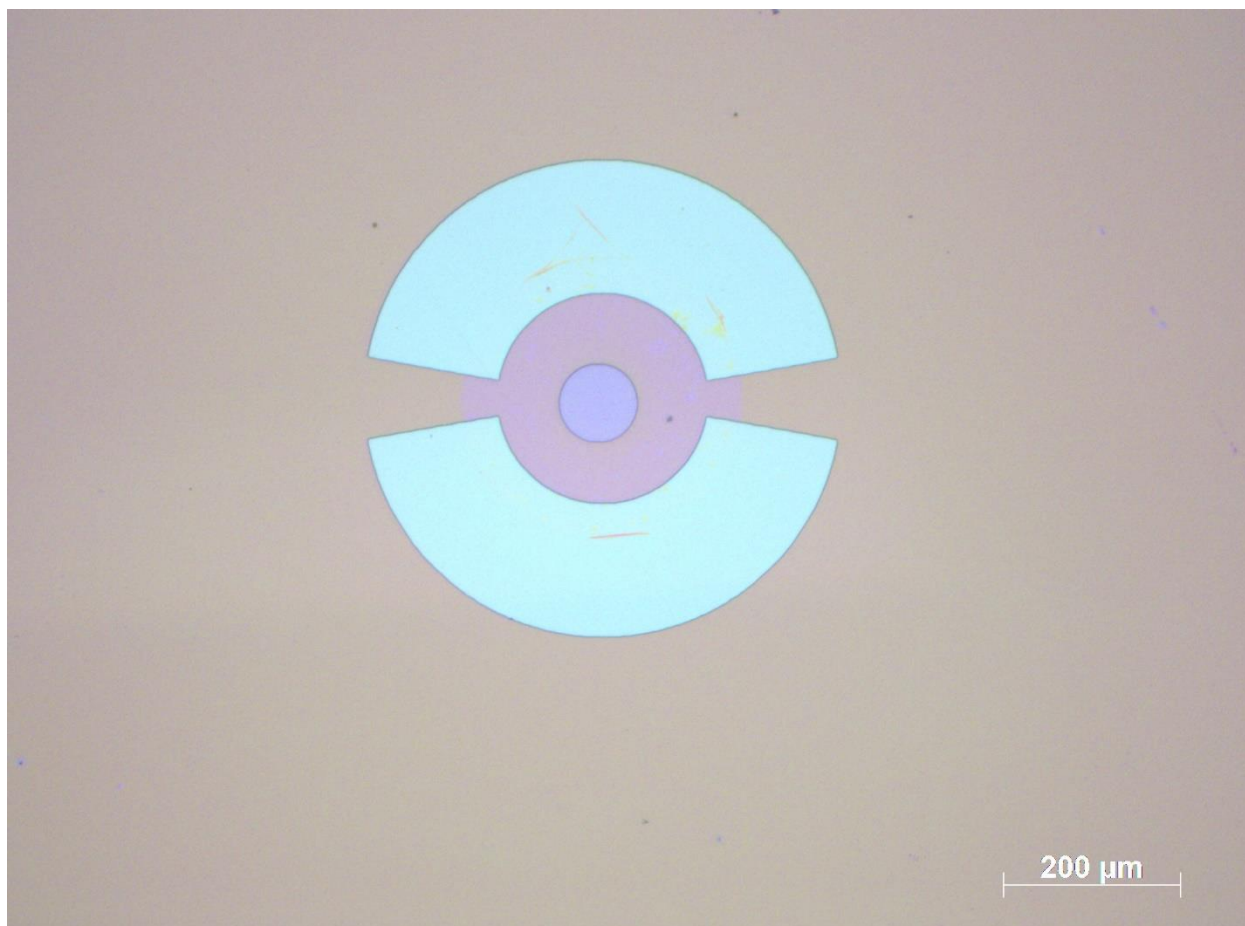


Figure 57. Optical micrograph of a 2D-LET device after the photoresist masks shown in Figure 55 were stripped in acetone.

- Followed by another 3.5nm Aluminum protection layer deposition using the Temescal BJD 1800 e-beam evaporator, and followed by a third photolithography step to define the base contact regions on the CVD 2D material (central circular pink region). Scale bar is 200μm.

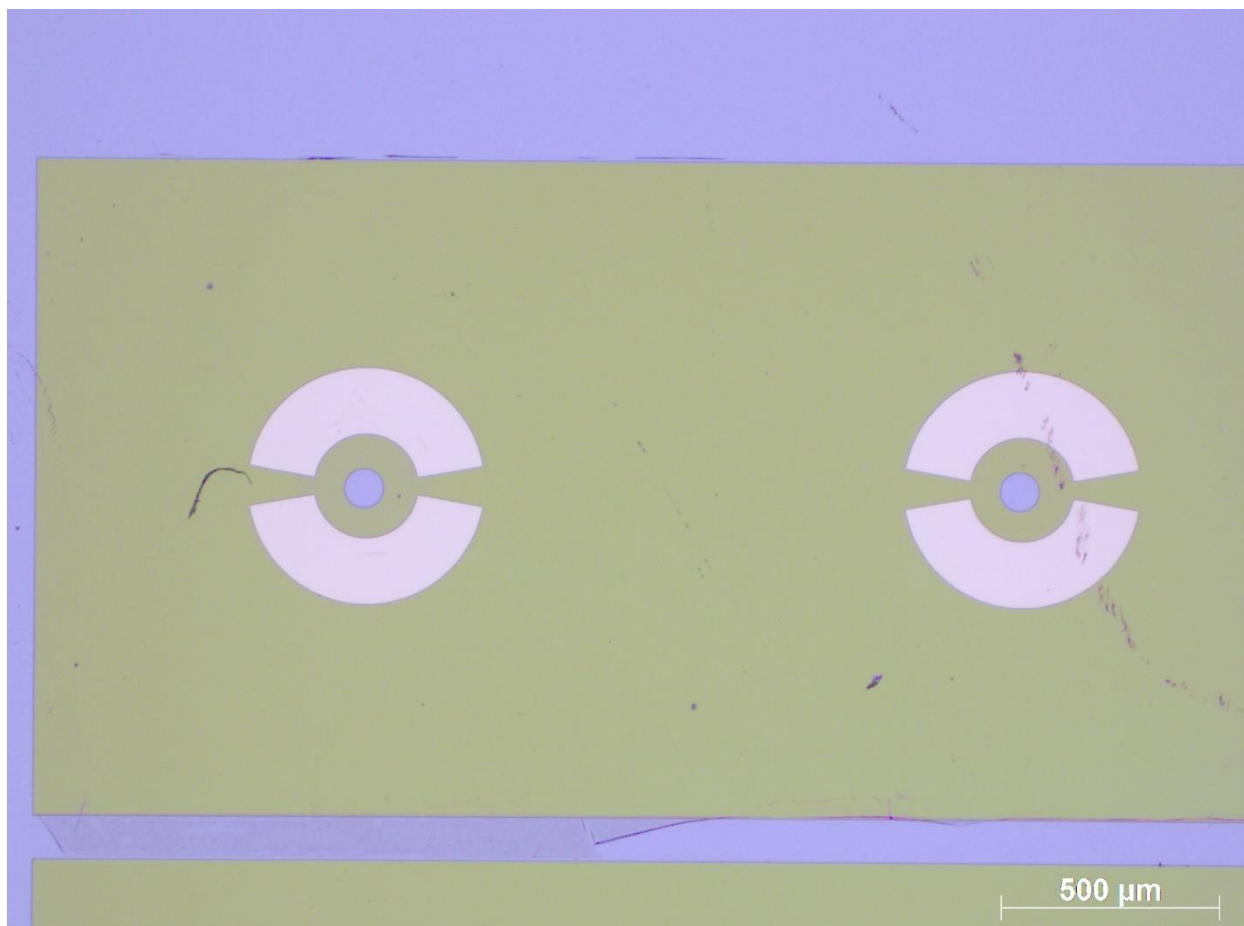


Figure 58. Optical micrograph of 2D-LET devices after 20nm Titanium adhesion layer/100nm Gold contacts were deposited using a Temescal BJD 1800 e-beam evaporator.

- The 20nm Titanium adhesion layer was deposited at a pressure of $\sim 4 \times 10^{-7}$ Torr at a deposition rate of ~ 0.7 Angstrom/second. The 100nm Gold contacts were deposited at a pressure of $\sim 9.5 \times 10^{-7}$ Torr at a deposition rate of ~ 1.27 Angstrom/second. Scale bar is 500 μ m.

We then etch away the 3.5nm Aluminum protection layer by soaking the device in AZ400K (1:4) for 2 minutes followed by rinsing it in deionized water and nitrogen gun drying it. Next, we deposit a 1.1nm Titanium seed layer on top of the exposed CVD 2D material using a Temescal BJD 1800 e-beam evaporator at a deposition rate of ~ 0.1 Angstrom/second and let it oxidize overnight.



Figure 59. Beneq TFS 200 Atomic Layer Deposition.

- After we deposit the Titanium seed layer onto the CVD 2D material and let it oxidize overnight, we then use atomic layer deposition (ALD) to deposit a thin top-gate dielectric of HfO_2 .
- As an example, for one of our 2D-LET substrates (G41_Q4_S3), we grew a 6nm HfO_2 top-gate dielectric using the ALD with the recipe "01 HfO_2 Thermal TDMAH H_2O ": 200°C, HfO_2 Thermal, 50 cycles.
- This dielectric thickness was confirmed using a control substrate placed right beside the actual 2D-LET substrate during ALD and measured using a Woollam M-2000 Ellipsometer.

We then proceed to transfer CVD graphene onto this substrate for top-gate device fabrication using CVD graphene as a transparent and electrically conductive top-gate contact/collector electrode. We grow our CVD graphene on copper foils at NIWC Pacific (or purchase it from a commercial vendor) and then use an electrolysis method to delaminate the PMMA/CVD Graphene from the underlying copper foil substrate and let it float on deionized water in a petri dish. We then scoop up the PMMA/CVD graphene using our target 2D-LET substrate shown in Figure 60.

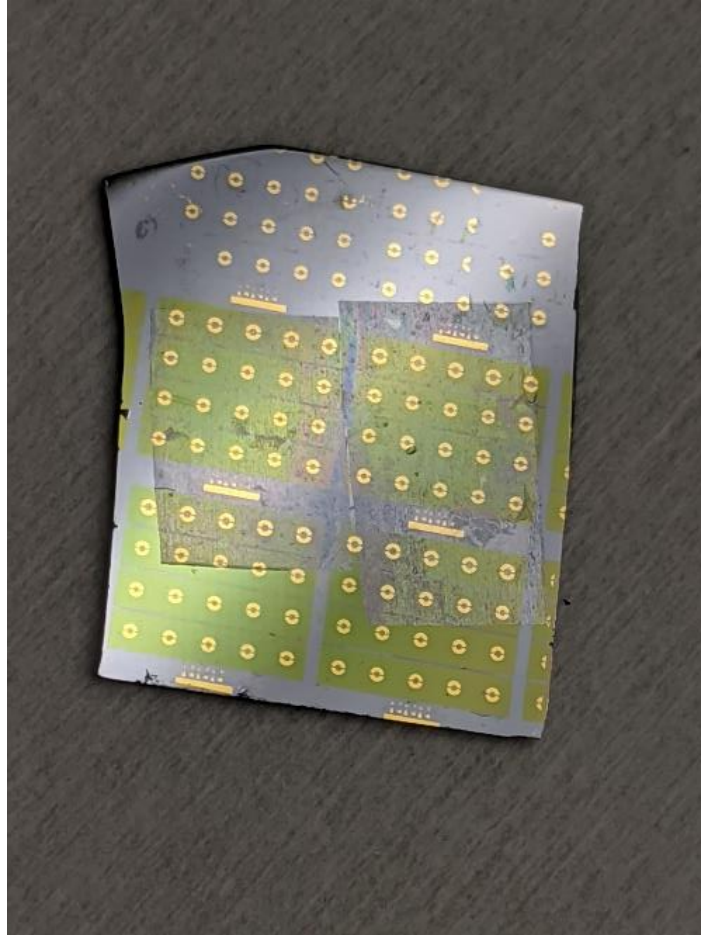


Figure 60. G41_Q4_S3 substrate with 6nm HfO₂ top-gate dielectric during CVD graphene transfer for top-gate fabrication. G41_Q4_S3 with PMMA/CVD Graphene pieces transferred onto at least two matrices (with 20 devices covered per matrix).

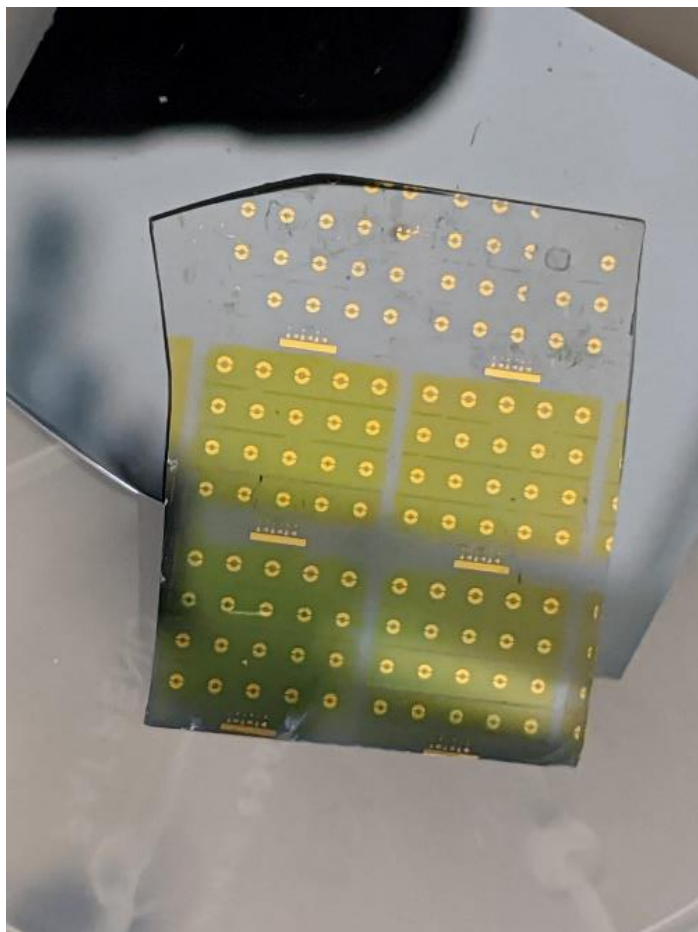


Figure 61. G41_Q4_S3 with CVD graphene after PMMA was dissolved in acetone. The presence of CVD graphene is not visible to the eye but is confirmed via Raman spectroscopy.

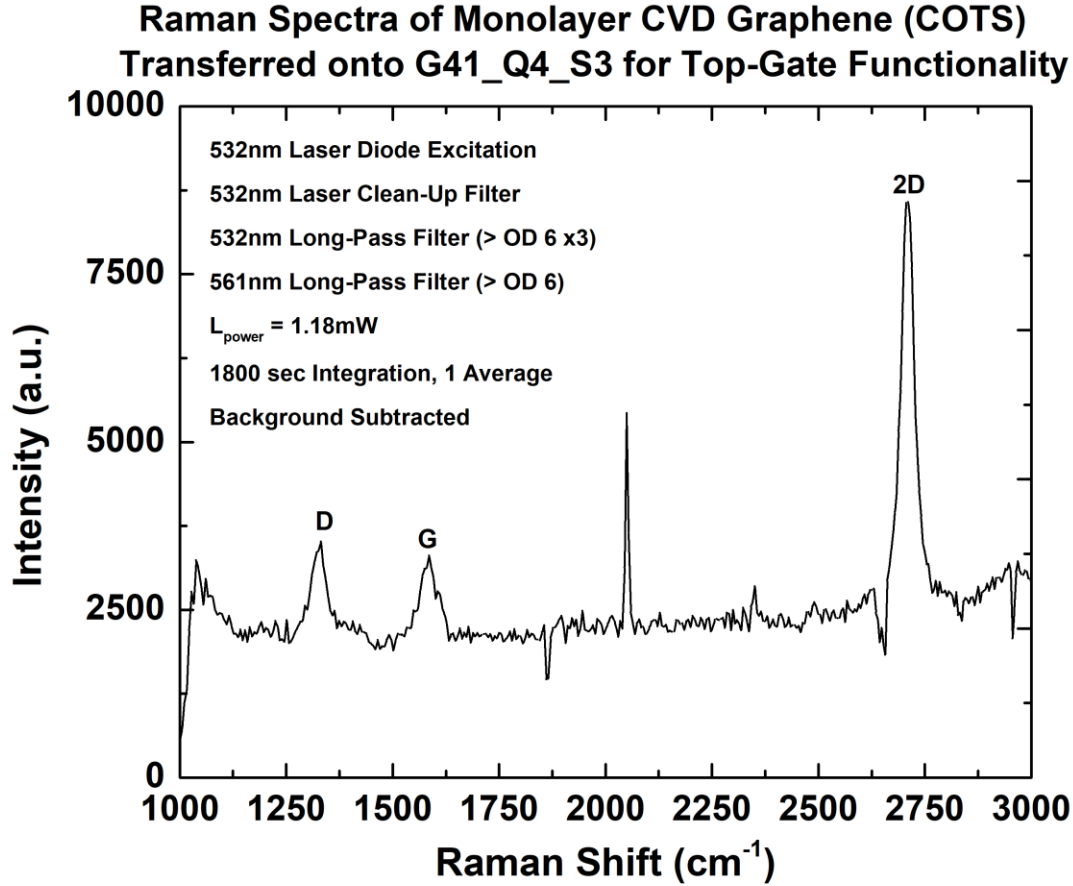


Figure 62. Raman spectrum of COTS monolayer CVD graphene transferred onto G41_Q4_S3 substrate via an electrolysis and scooping method to serve as a top-gate electrode upon further device fabrication.

- The D peak of graphene is centered near 1,350cm⁻¹. The G peak of graphene is centered near 1600cm⁻¹ and the 2D peak of graphene is centered near 2,750cm⁻¹. The inset lists the data acquisition parameters used during measurement.

We next perform a fourth photolithography step to define the central top-gate contact definition (shown in Figure 5) which will consist of CVD graphene. During this step, we first drop-cast NR9-1500PY negative photoresist onto our CVD graphene/2D-LET substrate. We then spin-coat the resist at 4500rpm for 1 minute. Afterwards, we place the substrate on a hotplate at 150°C for 1 minute (soft bake). The photoresist is then exposed for 13 seconds using a photomask aligner with emission at 365nm. Afterwards, we place the substrate onto a hotplate at 100°C for 1 minute (post-exposure bake). We then develop the resist in resist developer RD6 for 15 seconds and rinse the resist in de-ionized water and dry it with a nitrogen gun. Afterwards, we use an oxygen plasma etcher to etch away the exposed CVD graphene that is not covered by the photoresist.

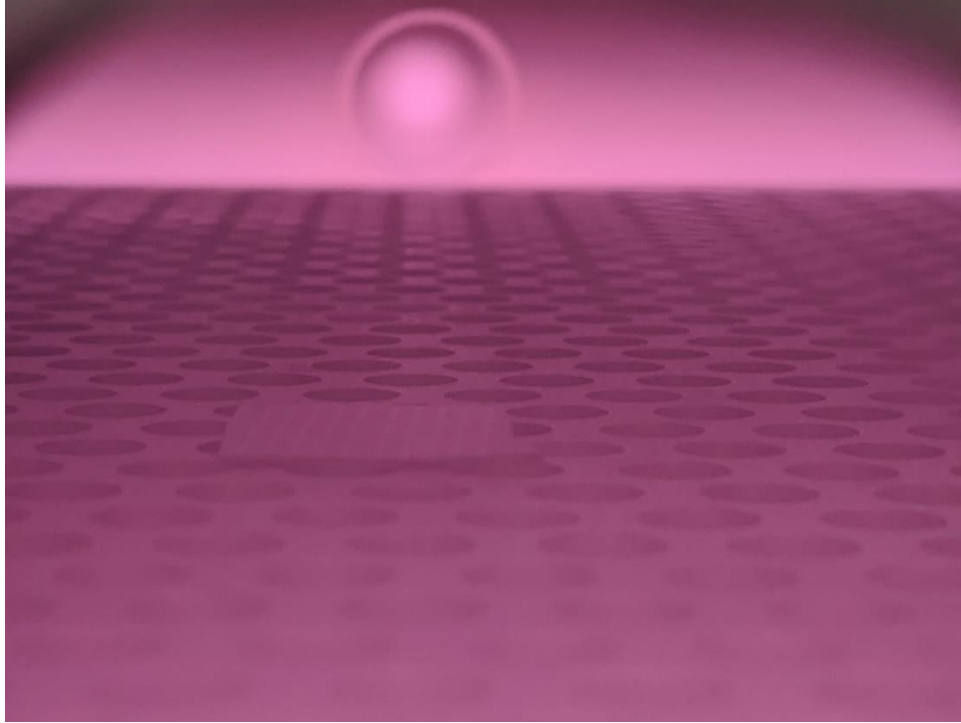


Figure 63. Image through the viewport of the Plasma Etch PE100 oxygen plasma etcher in UCSD Nano3 cleanroom. The 2D material-based substrate is located near the center.

- The PE100 is used to etch away the exposed CVD graphene for future top-gate contact of the TMD-based LET. Recipe used to etch the exposed CVD graphene: 150W RF plasma at 5sccm (O_2 flow) at 42mTorr process pressure for 1 minute.

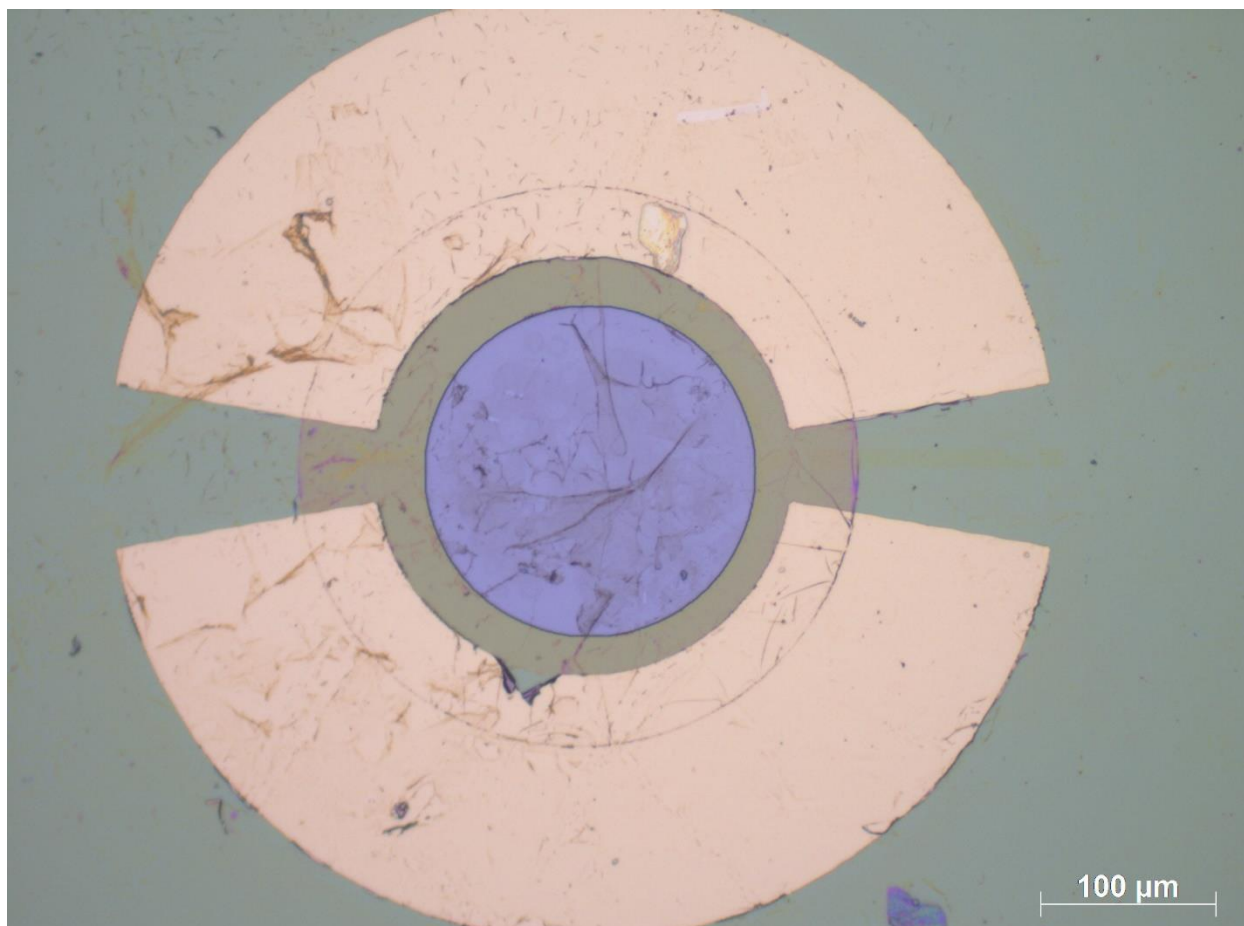


Figure 64. Optical micrograph of device G41_Q4_S3_B33_MoS₂_GTG (Graphene-Top-Gate) LET (Light Emitting Transistor) after the oxygen plasma etching step.

- Notice the barely visible graphene in between the large base metal contact pads on the right side. The final metallization step will make contact to this graphene region.

We then perform a fifth and final photolithography step to define the side contacts to the central top-gate region defined in the fourth photolithography step (see Figure 64).

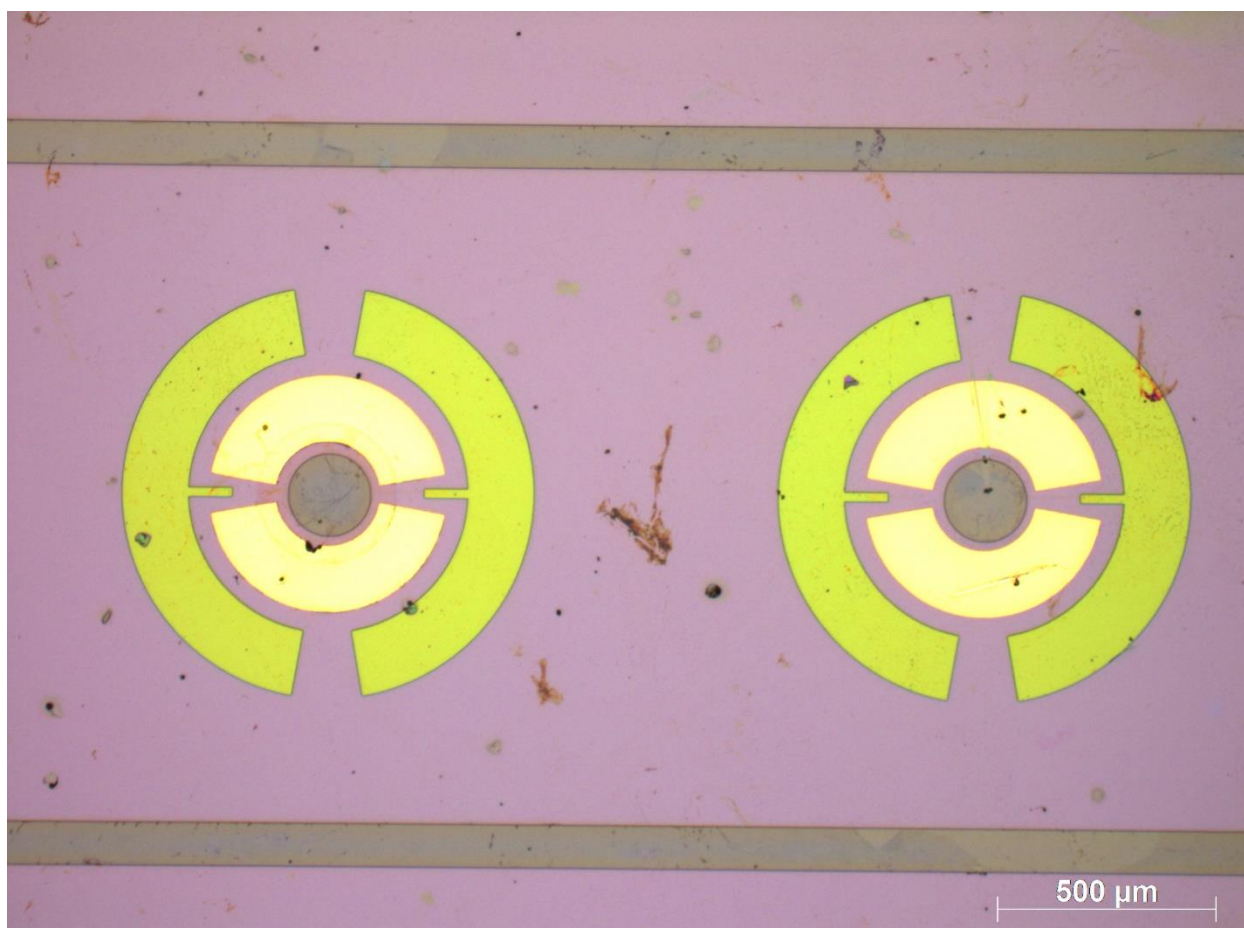


Figure 65. Optical micrograph of device (left) G41_Q4_S3_B33_MoS₂_GTG (Graphene-Top-Gate) LET (Light Emitting Transistor) after the 5th photolithography step to define the side metal gates that make contact to the central CVD graphene.

- The final metallization step will make contact to this graphene region.

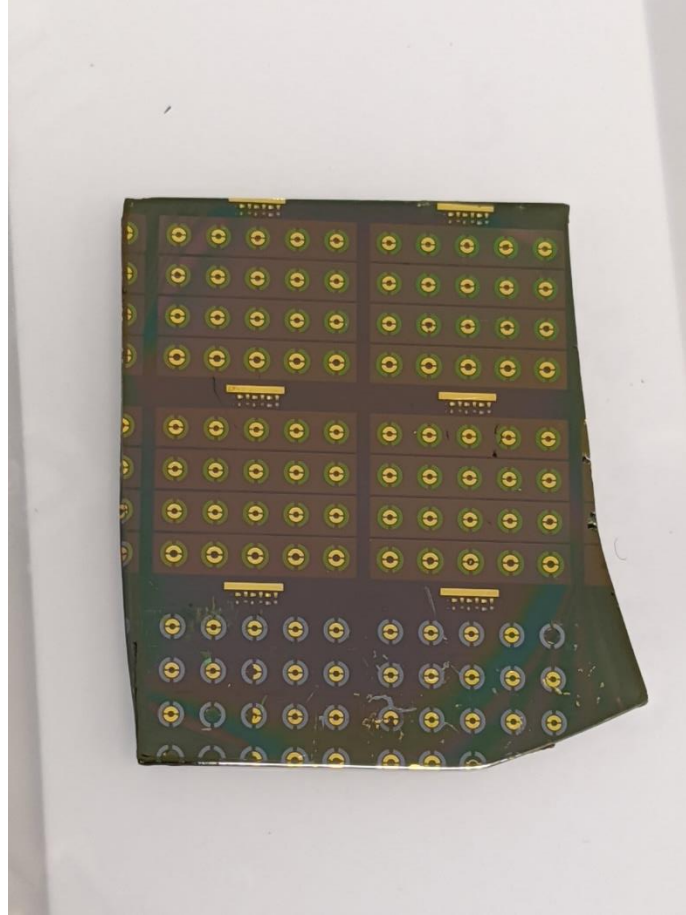


Figure 66. Image of the device substrate G41_Q4_S3 with CVD graphene top-gate contact after the fifth and final photolithography step prior to metallization of the side metallic contacts to the central CVD graphene top-gate.

We then use a diamond scribe to scratch deeply into the n^{++} degenerately doped silicon to deposit metal into the scratches, which will serve as emitter contacts (see Figure 68). Then, we use a Temescal BJD 1800 e-beam evaporator to deposit 150nm Aluminum (deposition rate: ~ 1.1 Angstrom/second at deposition pressure of $\sim 8 \times 10^{-7}$ Torr)/50nm Gold (deposition rate: ~ 1.2 Angstrom/second at deposition pressure of $\sim 9.9 \times 10^{-7}$ Torr) side contacts to the central top-gate collector consisting of CVD graphene.

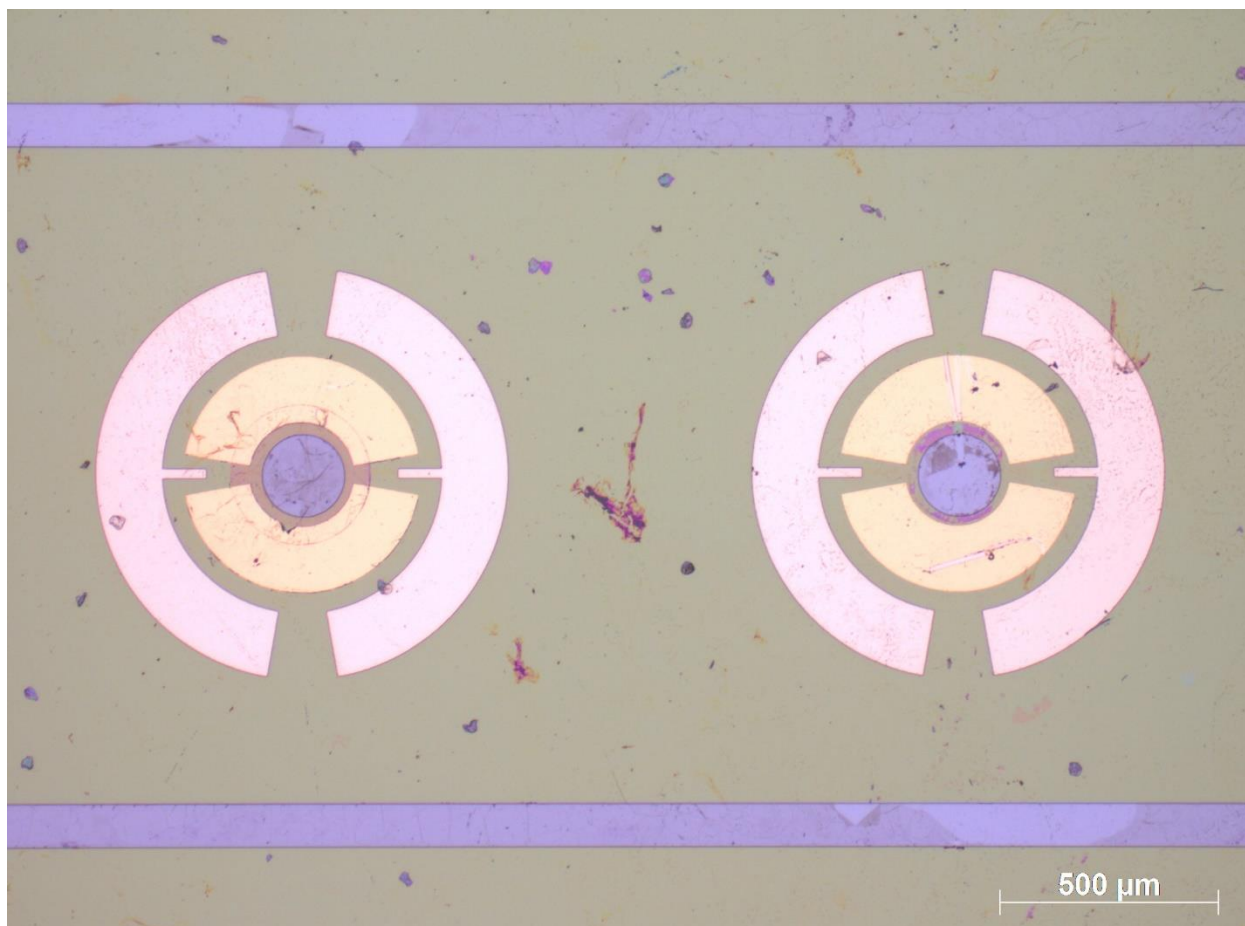


Figure 67. Optical micrograph of device (left) G41_Q4_S3_B33_MoS₂_GTG (Graphene-Top-Gate) LET (Light Emitting Transistor) after the metallization step (50nm Au/150nm Al) to define the side gates that contact the graphene top-gate region.

- The device fabrication is complete at this point and the substrate looks like as shown in Figure 68.

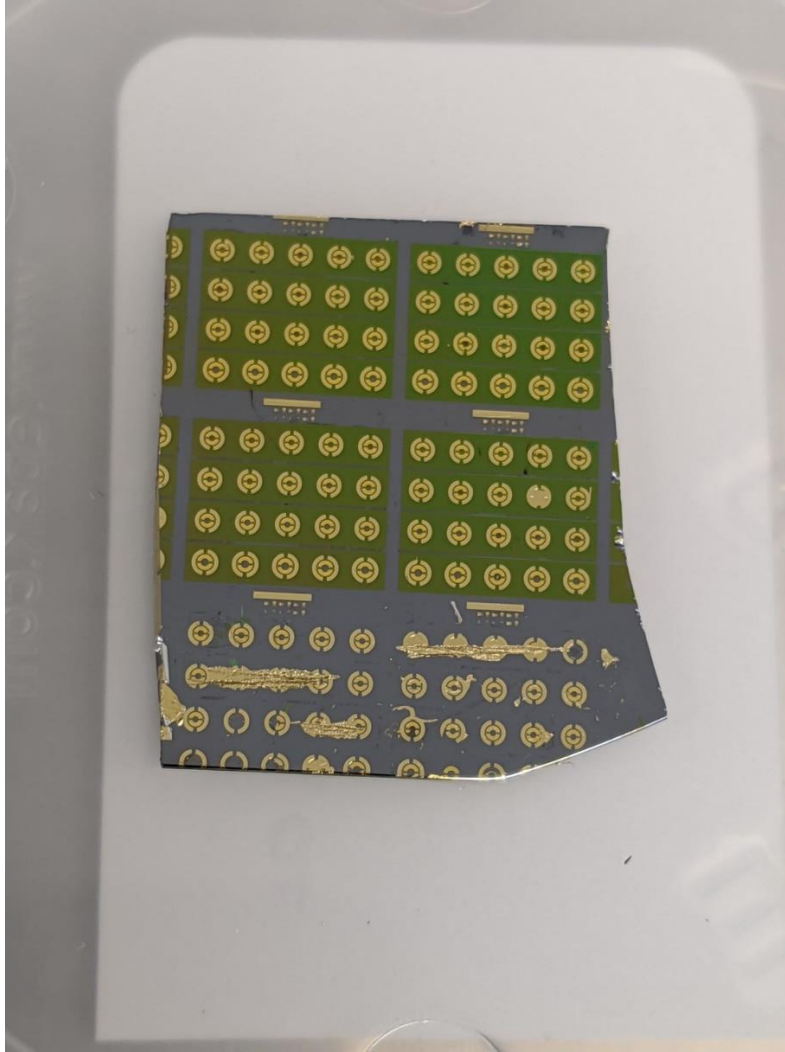


Figure 68. Image of the device substrate G41_Q4_S3 with CVD graphene top-gate contact after metallization of the side metallic contacts to the central CVD graphene top-gate.

- The deep scratches to the n^{++} silicon allow for metallization of the emitter contact region (e.g. hot electron injection).

This concludes the dual-gated 2D material-based device fabrication procedure.

3. CONCLUSIONS

This Technical Report summarized the 2D material-based device fabrication procedures executed at the UCSD Nano3 cleanroom facility and the NIWC Pacific Battery Ashburn cleanroom. We now have several 2D material-based devices (both back-gated and top-gated devices) that we will proceed to electrically and optically characterize using the facilities at the QENDL lab at NIWC Pacific.

This page is intentionally blank.

REFERENCES

- 1 Department of the Navy 30 Year RDT+E 30 Year Research and Development Plan (2017); https://blog.spawar.navy.mil/command/DON%2030%20Year%20R%26D%20Plan%20FINAL_5Jan2017C.PDF
- 2 ONR Naval Science and Technology (S+T) Strategy (2015); http://www.defenseinnovationmarketplace.mil/resources/NavalS&TStrategy2015_Final_01-26-15.pdf
- 3 C. M. Torres Jr., “Vertical Tunneling Hot Carrier Transport in 2D van der Waals Material-Based Devices for Optoelectronic Applications,” UCLA PhD Dissertation (2015); <https://escholarship.org/uc/item/179395wb>
- 4 C. M. Torres Jr. *et al.*, “Tunable Graphene Light-Emitting Device,” US Patent 10,121,932B1 (2018).
- 5 C. M. Torres Jr. *et al.*, “Voltage-Tunable Wavelength-Agile 2D Material-Based Light-Emitting Transistors,” US Patent 10,381,506B1 (2019).
- 6 Chen, C.-F. *et al.*, “Controlling Inelastic Light Scattering Quantum Pathways in Graphene,” *Nature*, 471, 617–620 (2011).
- 7 R. Beams *et al.*, “Electroluminescence from Graphene Excited by Electron Tunneling,” *Nanotechnology*, 25, 055206 (2014).
- 8 M. Parzefall *et al.*, “Light from van der Waals Quantum Tunneling Devices,” *Nature Communications*, 10, 292 (2019).
- 9 S. Z. Bisri *et al.*, “Endeavor of Iontronics: From Fundamentals to Applications of Ion-Controlled Electronics,” *Advanced Materials*, Vol. 29, Issue 25, 1607054 (2017).

This page is intentionally blank.

INITIAL DISTRIBUTION

84310	Technical Library/Archives	(1)
55360	C. Torres Jr.	(1)
71730	B. Liu	(1)
71780	T. Emery	(1)
H56H0	R. Ordonez	(1)
H56H0	C. Hayashi	(1)
55360	J. Adleman	(1)
72110	R. Lu	(1)

Defense Technical Information Center
Fort Belvoir, VA 22060–6218 (1)

In-House Laboratory Independent
Research (1)

Naval Innovative Science and Engineering (1)

This page is intentionally blank.

REPORT DOCUMENTATION PAGE				Form Approved OMB No. 0704-01-0188		
The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing the burden to Department of Defense, Washington Headquarters Services Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.						
PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.						
1. REPORT DATE (DD-MM-YYYY)		2. REPORT TYPE		3. DATES COVERED (From - To)		
June 2021		Final				
4. TITLE AND SUBTITLE				5a. CONTRACT NUMBER		
Fabrication of 2D Material-Based Devices				5b. GRANT NUMBER		
				5c. PROGRAM ELEMENT NUMBER		
				5d. PROJECT NUMBER		
6. AUTHORS				5e. TASK NUMBER		
Carlos M. Torres Jr. Cody K. Hayashi Brad C. Liu James R. Adleman Teresa Emery Ryan P. Lu Richard C. Ordonez				5f. WORK UNIT NUMBER		
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)				8. PERFORMING ORGANIZATION REPORT NUMBER		
NIWC Pacific 53560 Hull Street San Diego, CA 92152-5001				TR 3237		
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)				10. SPONSOR/MONITOR'S ACRONYM(S)		
Naval Innovative Science and Engineering, NIWC Pacific 53560 Hull Street San Diego, CA 92152-5001				ILIR and NISE		
12. DISTRIBUTION/AVAILABILITY STATEMENT				11. SPONSOR/MONITOR'S REPORT NUMBER(S)		
DISTRIBUTION STATEMENT A: Approved for public release. Distribution is unlimited.						
13. SUPPLEMENTARY NOTES						
14. ABSTRACT						
This Technical Report summarizes the 2D material-based device fabrication procedures executed during the FY17-19 of the Office of Naval Research (ONR) In-House Laboratory Independent Research (ILIR) funded "Voltage-Tunable Wavelength-Agile 2D Material-Based Light-Emitting Transistors (2D-LETs)" project as well as the first year research effort FY20 Naval Innovative Science and Engineering (NISE) funded "Quantum-Engineered Nanodevices Exploiting Twistronics for EMW and C4ISR (QENETEC)" project. Most of the work was performed in the University of California – San Diego (UCSD) Nano3 cleanroom facility via an Indefinite Delivery/Indefinite Quantity (IDIQ) contract vehicle.						
15. SUBJECT TERMS						
Naval Innovative Science and Engineering (NISE); In-House Laboratory Independent Research (ILIR); quantum; nanotechnology; semiconductors; graphene; 2D materials; device fabrication; hot electron transistors.						
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON	
a. REPORT	b. ABSTRACT	c. THIS PAGE			Carlos Torres Jr.	
U	U	U	SAR	84	19b. TELEPHONE NUMBER (Include area code)	
(619) 553-1614						

This page is intentionally blank.

This page is intentionally blank.

DISTRIBUTION STATEMENT A: Approved for public release.
Distribution is unlimited.



Naval Information Warfare Center Pacific (NIWC Pacific)
San Diego, CA 92152-5001