A 112 GS/s Switched-Capacitor DAC in 16 nm FinFET CMOS

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***Abstract*—This paper describes ongoing work toward a FinFET-friendly implementation of high-speed D/A converters for mm-wave arrays. The proposed architecture is based on time-interleaved charge redistribution and separates level generation, pulse timing and output power generation. This approach aims to leverage the advantages of 16 nm FinFET technology (transistor speed and density) and simultaneously mitigate its main shortcomings (poor interconnect delay and current handling). Following our proof-of-concept work on 8-bit, 14 GS/s and 28 GS/s prototypes, the current work looks at extending the update rate to 112 GS/s using a data and hold interleaving topology. We present preliminary simulation results of the DAC's core circuitry, which exhibits interleaving spurs at -50 dB relative to the signal level.**

Keywords—digital-to-analog converter; mm-wave; transmitter; switched-capacitor circuits.

I. Introduction

DARPA's Millimeter-Wave Digital Arrays (MIDAS) program pushes the frontiers of digital mm-wave transceiver technology by leveraging the integration density and speed of advanced CMOS process technology. Among the key challenges of this program are the data converters that bridge the digital signal processing modules with the mm-wave transmit/receive circuitry. This work tackles the digital-to-analog converter (DAC) problem, and specifically investigates circuit architectures that leverage the strengths of FinFET CMOS technology.

Our prior work has resulted in 8-bit prototype designs operating at 14 GS/s [1] and 28 GS/s [2]. The highlight of these designs is their very small area, measuring only 0.011 and 0.03 mm^2, respectively. As an exploratory extension, we are now designing a prototype for 112 GS/s operation, which will potentially enable direct and frequency-agile mm-wave synthesis up to ~30 GHz outputs with approximately 2× oversampling for proper image filtering.

Our design approach is a departure from traditional current steering into 50 Ω, which is arguably not the best match for FinFET processes with ultra-thin metal layers [2]. Instead, we deploy time-interleaved switched-capacitor (SC) DACs that are buffered into the 50 Ω loads using inverter-based drivers. Using sub-femtofarad unit capacitors, this leads to compact layouts that help mitigate timing errors that are difficult to manage in distributed current steering circuitry.

The remainder of this paper is structured as follows. Section II describes the proposed DAC architecture for 112 GS/s operation. The planned prototype IC is discussed in Section III, while initial simulation results are presented in Section IV.

II. Technical Approach

To achieve 112 GS/s, we employ a "data and hold interleaving" scheme [3] that enables output updates every 8.3 ps, which is not possible using conventional multiplexing. The resulting architecture and its timing are depicted in Fig. 1. It is composed of four sub-DACs, each operating on one phase φ_i of a 28 GHz quarter-rate quadrature clock.

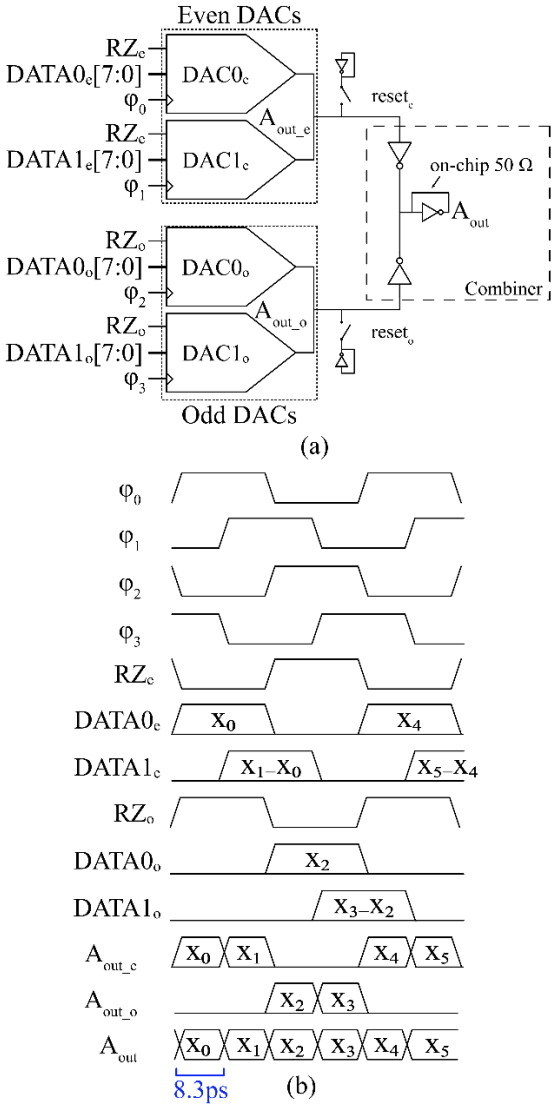

Fig. 1. Data and hold interleaved SC DAC. (a) Architecture and b) timing diagram.

The sub-DAC outputs hierarchically combine in groups of two and withing each group, the DAC0 output is directly proportional to the input code DATA0, while the DAC1 output adds/subtracts only the difference x_{i+1}-x_i between consecutive DATA1 and DATA0 codes. The sub-DAC outputs are returned to zero by asserting the signal $RZ_{e/o}$. An inverter-based combiner forms the full-rate output. During the reset phase ($reset_{e/o}$), a diode-connected inverter sets the sub-DAC's output common-mode voltage around mid-supply. The reset circuit is a replica of the input stage of the inverter-based combiner to match its midpoint-voltage over process, voltage, and temperature (PVT).

The DAC levels are generated using SC circuits, which can be scaled down to the sub-femtofarad level without affecting the linearity and noise performance at the 8-bit target resolution. The SC core contains a binary-weighted capacitor array composed of 256 unit-cells as shown in Fig. 2(a). Each cell contains the logic to perform the return-to-zero (RZ) operation and data re-timing, an inverter driver and a 0.5 fF metal-oxide-metal (MOM) capacitor [Fig. 2(b)-(c)]. During the RZ phase, the sub-DAC word is set to mid-code by using a complementary structure in the unit-cell logic for the MSB and LSBs.

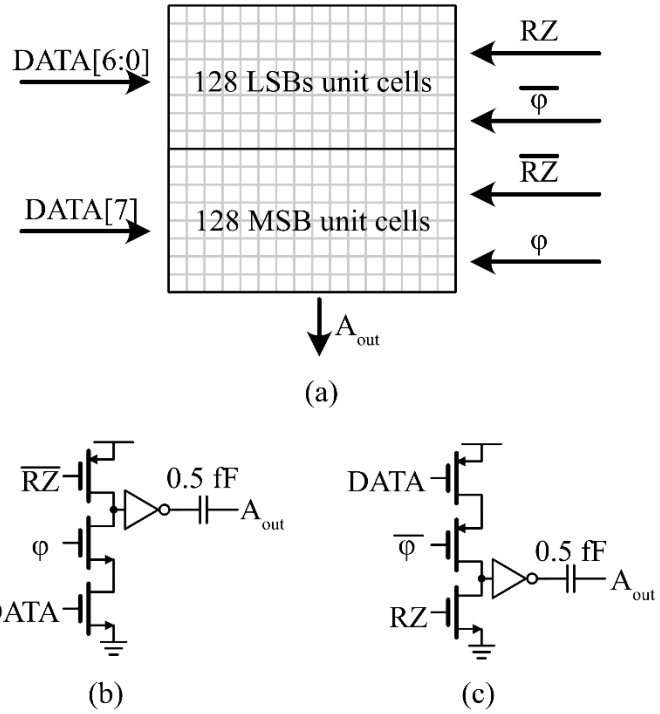

Fig. 2. SC DAC (a) floorplan, unit cells for (b) MSB and (c) LSBs.

The layout of a single-ended sub-DAC has a footprint of only 10 µm x 12 µm as shown in Fig. 3. It achieves a significant area reduction over our prior work thanks to a reduction of the number of transistors in the unit-cell, and the use of higher metal levels for the implementation of the MOM cap that allows to position it on top of the logic.

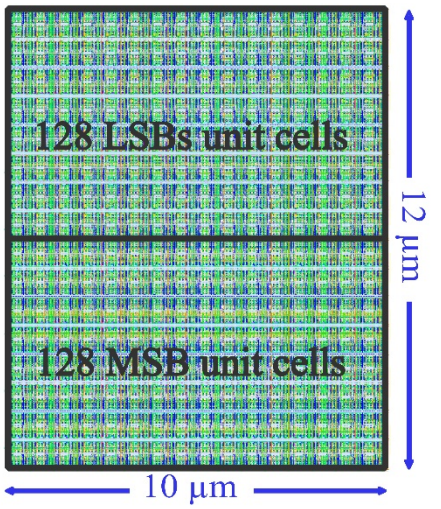

Fig. 3. Switched capacitor sub-DAC layout.

The half-circuit schematic of the inverter-based combiner is shown in Fig. 4. The actual implementation is pseudo-differential. It is composed of two inverter-based drivers and an inverter-based on-chip 50 Ω termination. The combiner's voltage gain is about 1.2, set by the relative size (K) of the drivers and load transistors.

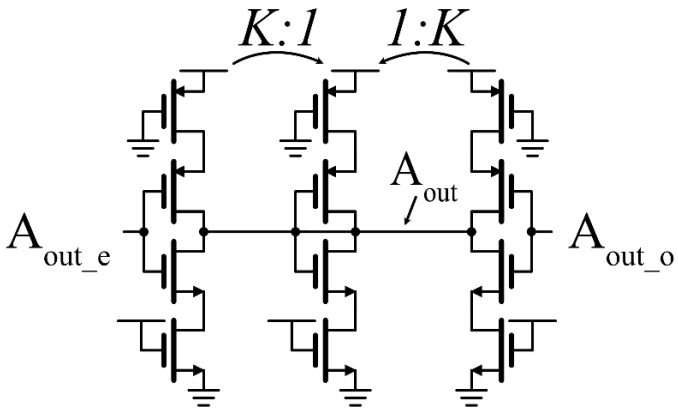

Fig. 4. Inverter-based combiner.

Our previous design achieved 34 dB SFDR with a signal swing of 320 $mV_{pp,diff}$ at the balun input, limited by the two-stage output buffer nonlinearity [2]. In this paper's design we are similarly limited by the output combiner nonlinearity, and aim to improve it through digital predistortion (DPD). Contrary to current-steering DACs, one of the main advantages of the proposed SC DAC architecture is that the digital predistorter can be simple (a memoryless polynomial may suffice), as the output buffer does not have high-speed switching nodes that produce high-order nonlinear dynamics. Moreover, we expect to achieve up to 30 GHz bandwidth due to the simplified signal path and the small load at the output pad of our test chip.

III. Prototype IC

A prototype IC is being designed in TSMC's 16 nm FinFET CMOS process. The die floorplan is shown in Fig. 5. It operates on a DSP-compatible, single 0.8 V supply, and it contains the DAC, the inverter-based clock receivers, an on-chip memory, and SPI interface. The RF interfaces follow a GSGSG format to maximize signal integrity during wafer probing. The power/ground and all the control signals are wire-bonded and placed at the top/bottom of the IO ring to meet the required clearance constraints for the probe tips.

The clock phases ($\phi_{0..3}$) are derived from a single-ended 28 GHz quadrature clock that is generated off-chip (Clk In I/Q) and have adjustable skew and duty-cycle achieved by dedicated on-chip tunable delay-lines. Tunability is needed to reduce the amplitude of the interleaving spurs. The effectiveness of this approach is illustrated in the next section. The tuning of these knobs can be handled at the system level, using transceiver loopback during idle periods.

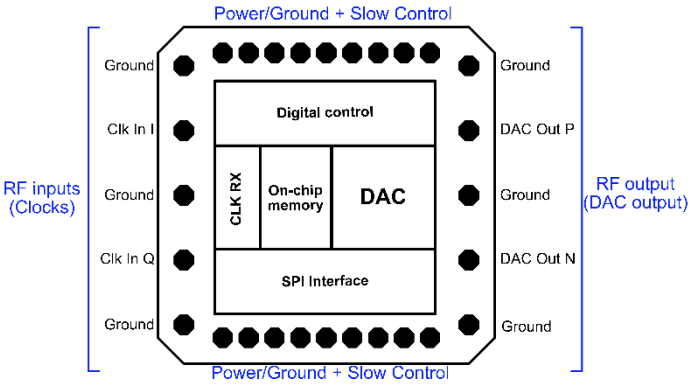

Fig. 5. Die floorplan.

IV. Simulation Results

Fig. 6 shows simulation results with pre-layout estimated parasitics of the proposed DAC operating at 112 GS/s, for a single-tone output signal at a frequency of 2.5 GHz. The combined output has an amplitude of 320 mV_{ppdiff} when terminated on an external 50 Ω load.

The imperfect overlap of the odd/even DAC output causes ripples in the transient waveform of the combined output (red-dashed line shown in Fig. 6) and an interleaving spur at $f_s/2$-f_{in} as seen if Fig. 7. The imperfect overlap is caused by the unit-cell duty-cycle distortion of the RZ signal which can be calibrated by adjusting the duty-cycle of the RZ and clock signal provided to the unit-cells. Fig. 7 shows the spectra for a single-tone low- and high-frequency output signal.

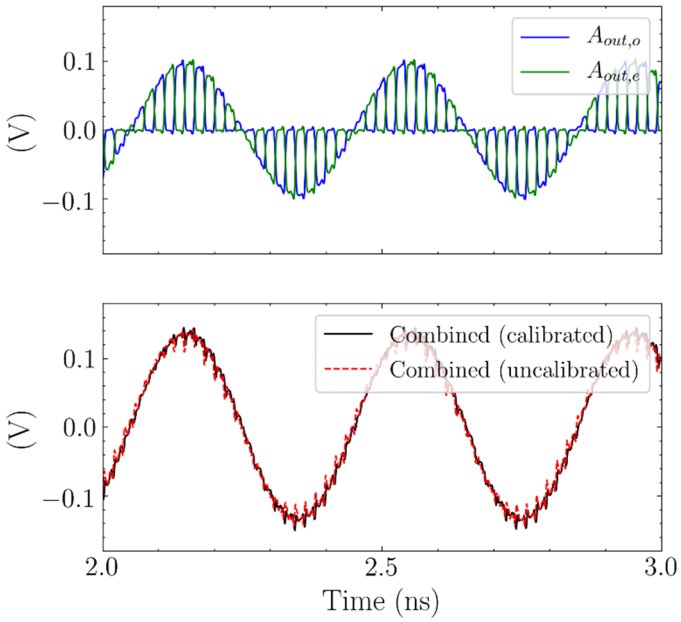

Fig. 6. SC DAC time-domain output waveforms.

Without calibration, the interleaving spur amplitude increases as the output frequency increases, degrading the spurious-free dynamic range (SFDR) due to the interleaving spurs alone ($SFDR_{IS}$). By using calibration, the $SFDR_{IS}$ is nearly constant, as shown in Fig. 8.

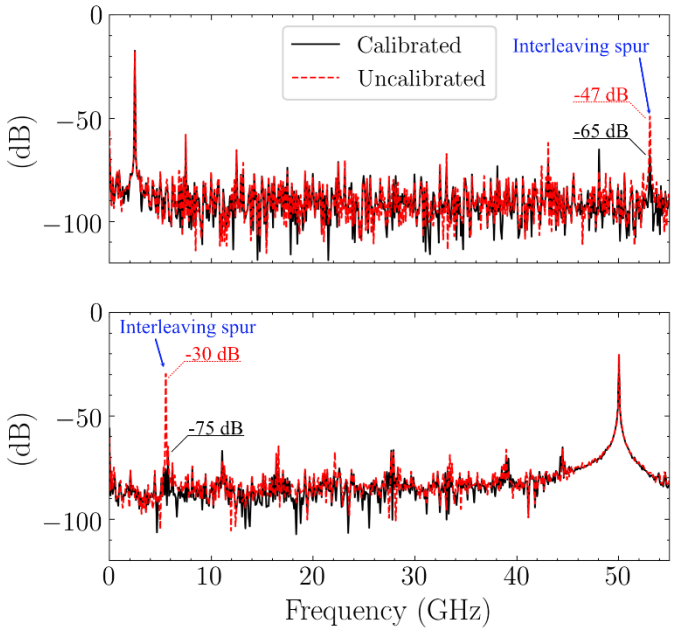

Fig. 7. SC DAC combined output spectrum (first Nyquist zone).

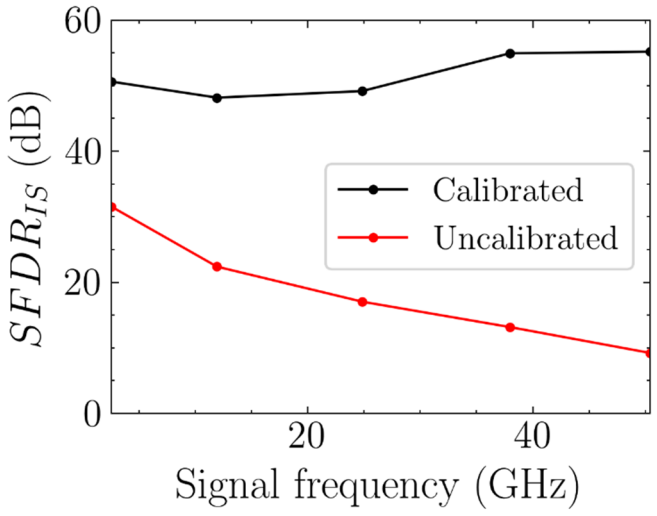

Fig. 8. $SFDR_{IS}$ vs. signal frequency.

DPD performance improvement is verified in terms of individual harmonic distortion components and SFDR at the combiner's output, for varying input signal amplitude and DPD polynomial order. SPICE schematic simulation results are shown in Fig. 9 for an output frequency of 800 MHz. A DPD of polynomial order M = 5 enables the combiner input signal amplitude to increase to 700 $mV_{pp,diff}$ while maintaining SFDR better than 34 dB. The DPD improvement in linearity across the first Nyquist zone is under investigation.

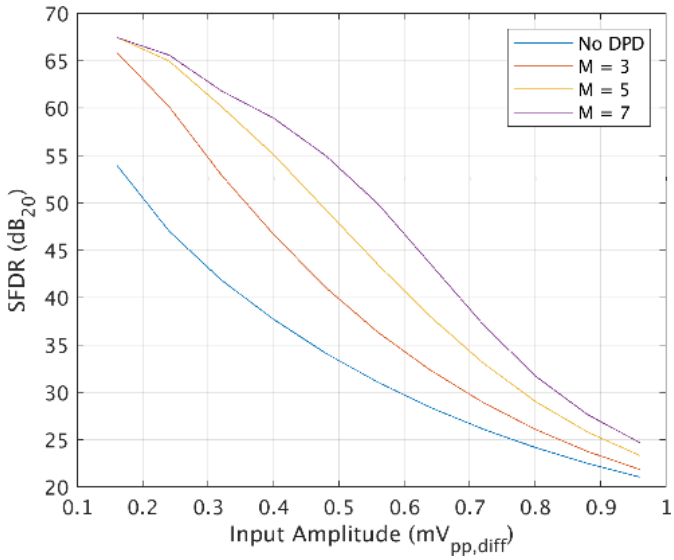

Fig. 9. Combiner SFDR improvement for different DPD orders.

ACKNOWLEDGMENTS

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