# A Study on Printed Circuit Board Backdoor Coupling and Stackup Considerations

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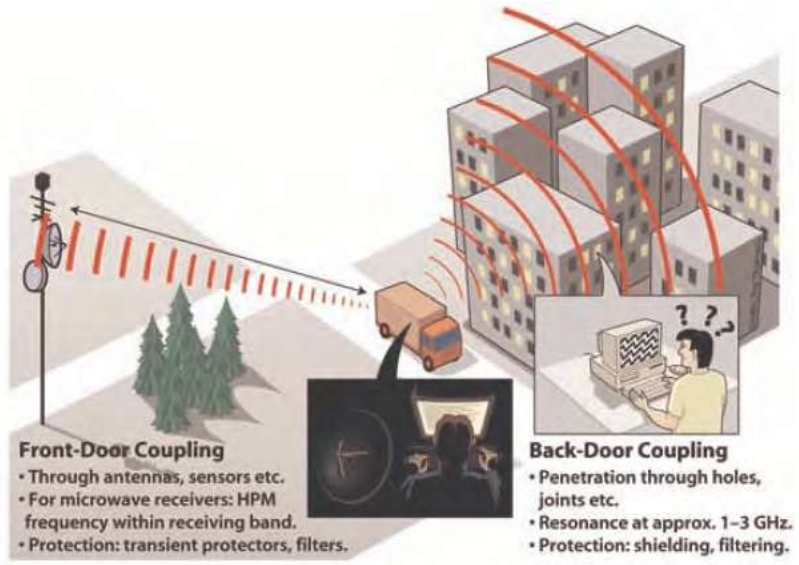
RADIANCE TECHNOLOGIES



LSU

# Background and Motivation

- Much of the existing literature on HPM effects attempts to link field parameters to component or system level effects
- Limited literature on coupling
  - Front door coupling: coupling to an intentional antenna
  - Backdoor coupling: coupling to an unintentional antenna
- Existing literature includes:
  - Microstrip and cable coupling models based on transmission line theory and electromagnetic topology
  - Model development for PCB coupling in complex enclosures
  - System level investigations involving backdoor cable coupling




Swedish Defense Research Agency

# Objective

- Pursuing a better understanding the following:
  - Which design parameters affect PCB coupling
  - How much can a given parameter reduce coupling
  - Under what conditions does a given parameter reduce coupling
- Better understanding enables informed HPM hardening techniques

- Out of scope
  - Coupling prediction
  - Efficient coupling model development

# Methodology: Modeling

- Custom PCBs design in Altium Designer to enable full control over the layout and access to the design files
- 3D full-wave modeling using Ansys High Frequency Structure Simulator (HFSS)
  - Frequency domain simulation using finite element method (FEM)
  - Port assignments, incident field, and absorbing boundary condition are added to the model
- Port voltages are calculated and plotted across frequency

**Simulation Parameters**

Port Impedance: 50 Ω

Field Strength: 1 V/m

Absorbing Boundary Condition: PML

ALTIUM DESIGNER

Ansys HFSS

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- 3D ful… …ys High Frequ… …HFSS)
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**Voltage Scaling**

| Induced Voltage | Field Strength |
|---|---|
| 1 mV | 1 V/m |

**Simulation Parameters**

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ALTIUM DESIGNER

Ansys HFSS

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**Voltage Scaling**

| Induced Voltage | Field Strength |
|---|---|
| 1 mV | 1 V/m |
| 1 V | 1 kV/m |

**Simulation Parameters**

Port Impedance: 50 Ω

Field Strength: 1 V/m

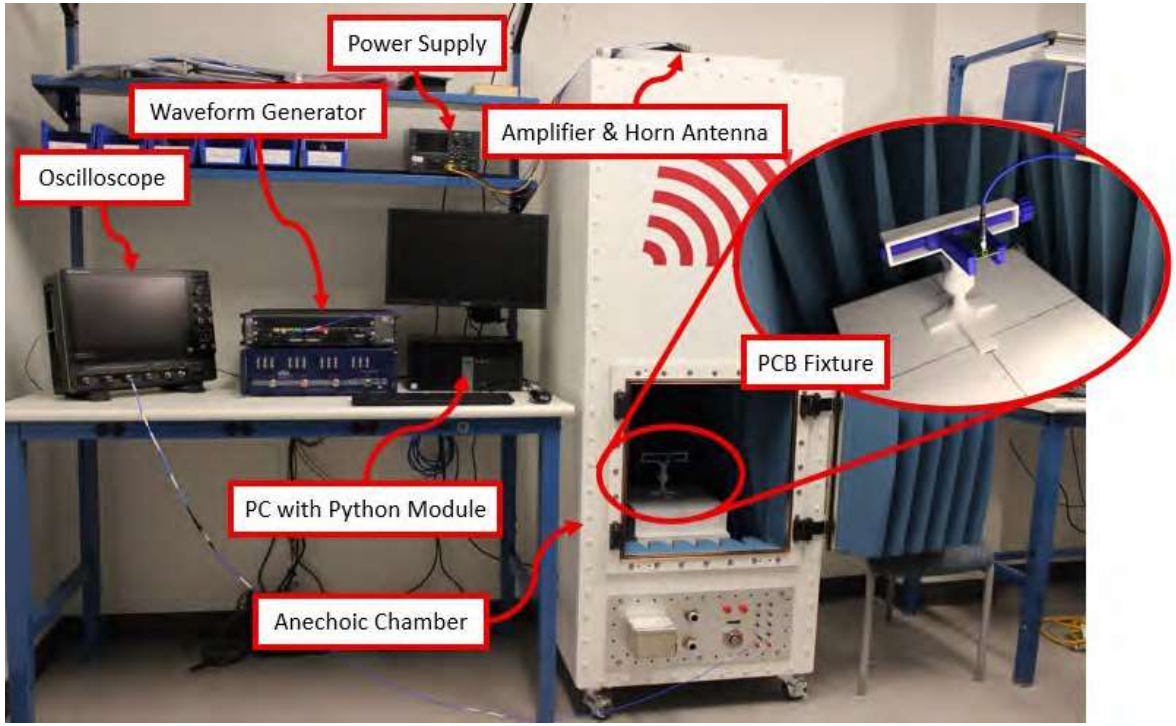
Absorbing Boundary Condition: PML

ALTIUM DESIGNER

Ansys HFSS

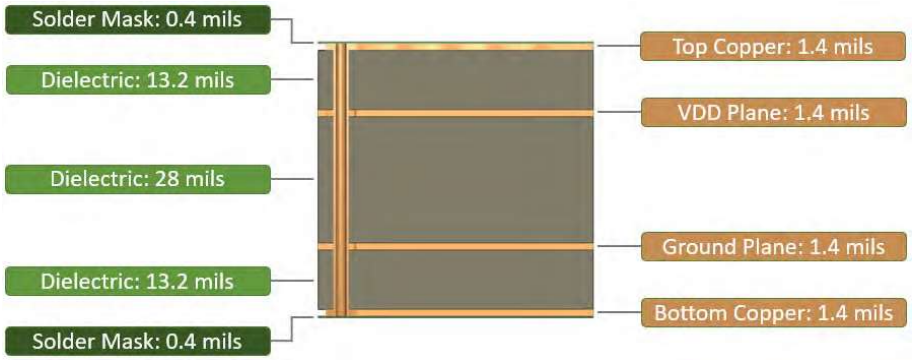
# Methodology: Experimental Testing

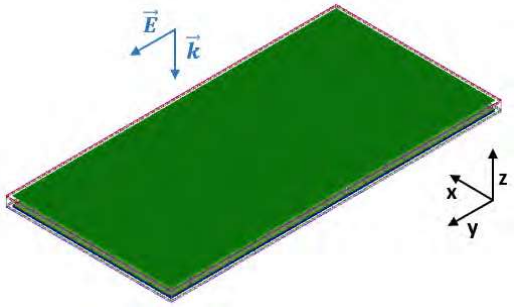
- Model validation performed using an anechoic chamber and high frequency lab equipment
- VNA used to characterize the testing loop and map signal amplitude to field strength at the DUT platform
  - Enables direct comparison to simulation conditions
- Scripting was used to automate measurements which are normalized in post-processing



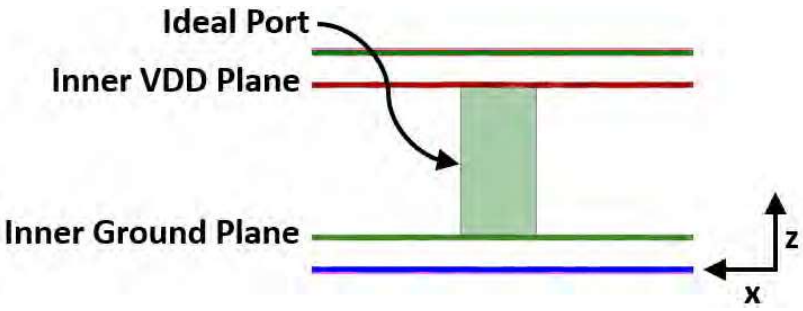
# Effects of Via Fencing on an Ideal PCB

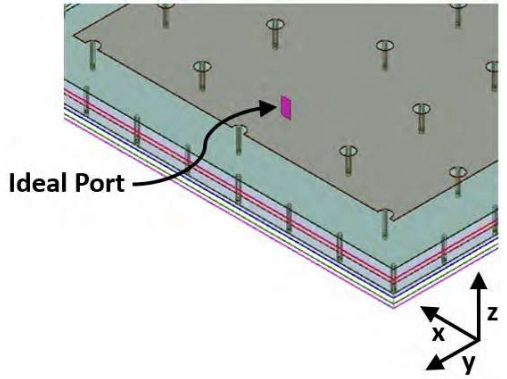
- Numerous investigations on via fencing and emissions
  - Focused on ideal PCB stackups without component footprints and traces




- PCB model
  - 4 layers
  - 1” x 2”
  - Ideal port between inner planes



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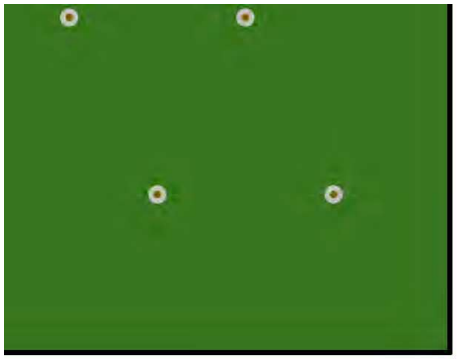
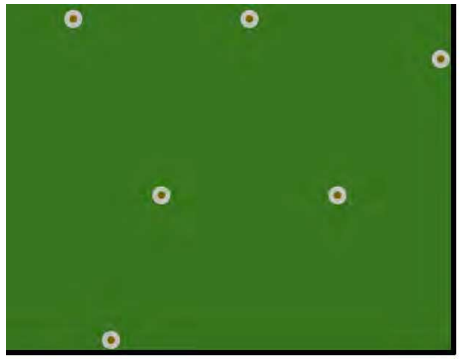
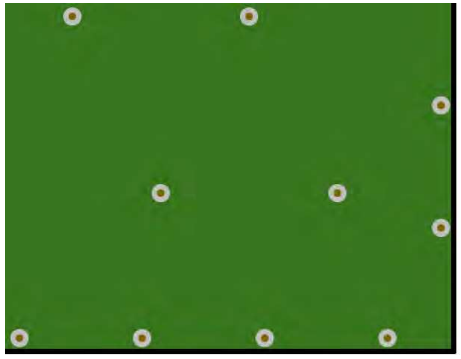


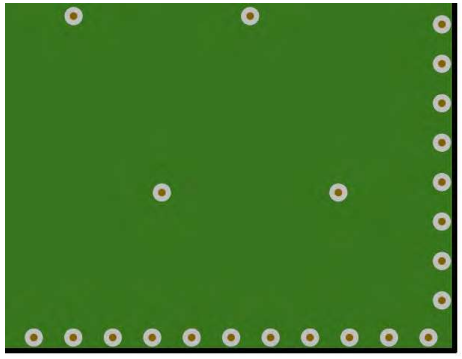
No Fence



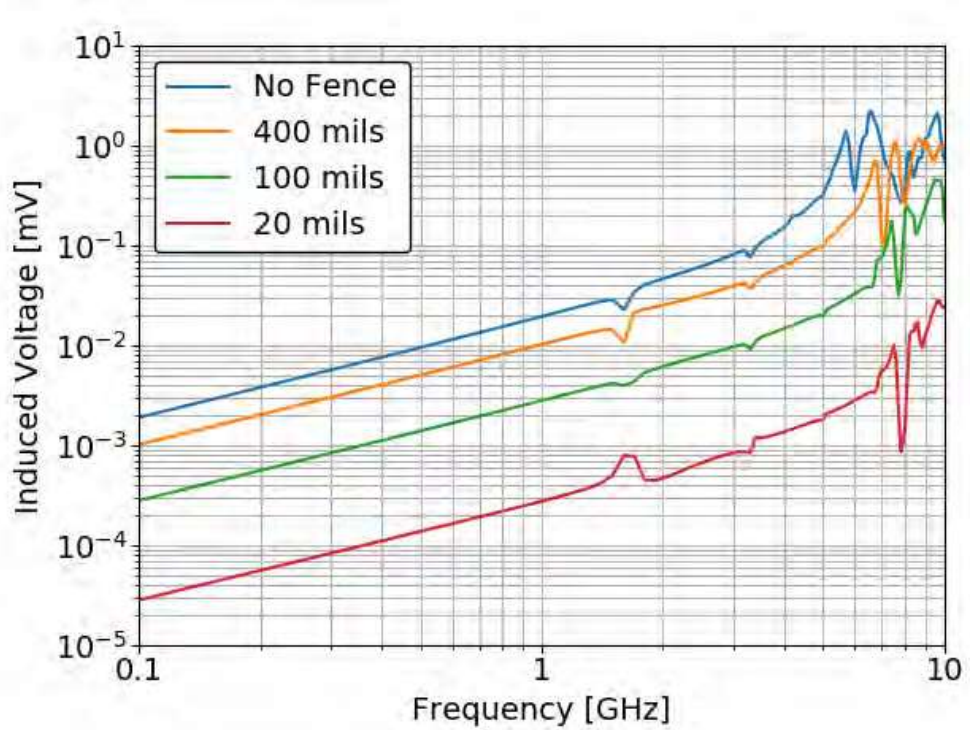
400 mil Fence



100 mil Fence



20 mil Fence

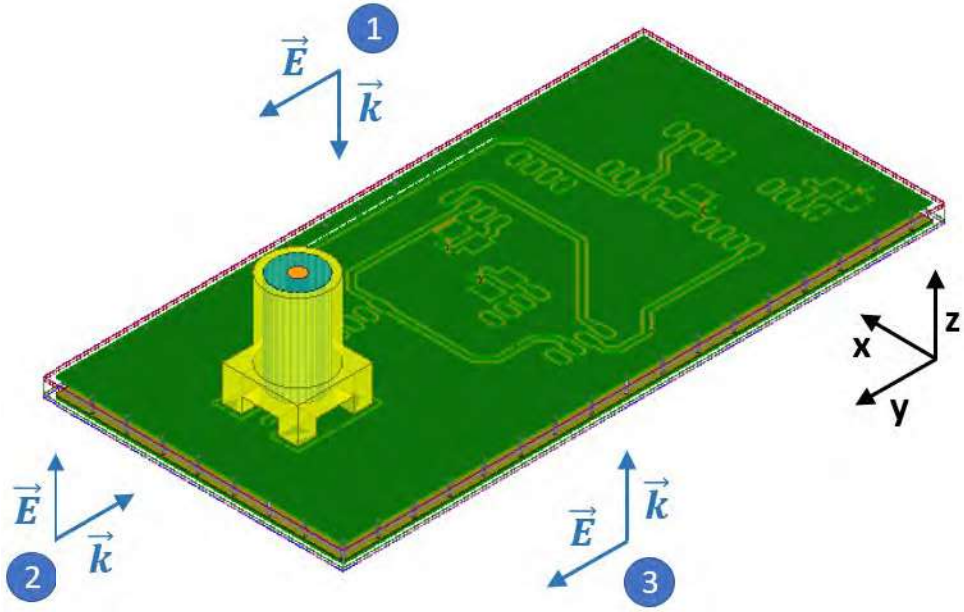



Simulated Induced Voltage (Ideal PCB)

Tortorich, Ryan P., et al. "A Study on the Radiated Susceptibility of Printed Circuit Boards and the Effects of Via Fencing." *Electronics* 10.5 (2021): 539.

# Effects of Via Fencing on a Practical PCB

- Component footprints and pads are incorporated on the top layer
- A surface mount SMA is also included to facilitate experimental testing
- Practical model includes three incident field cases
  - **Case 1**: wave propagates in the negative z direction (**-z**) with the E-field polarized along the **y** axis
  - **Case 2**: wave propagates in the negative y direction (**-y**) with the ~E-field polarized along the **z** axis
  - **Case 3**: wave propagates in the positive z direction (**+z**) with the E-field polarized along the **y** axis

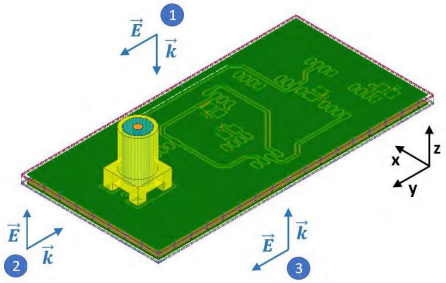


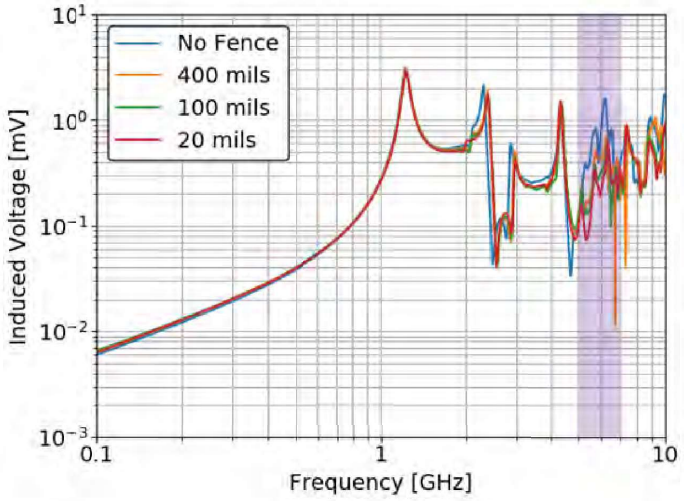

**Practical PCB Model**

Tortorich, Ryan P., et al. "A Study on the Radiated Susceptibility of Printed Circuit Boards and the Effects of Via Fencing." *Electronics* 10.5 (2021): 539.

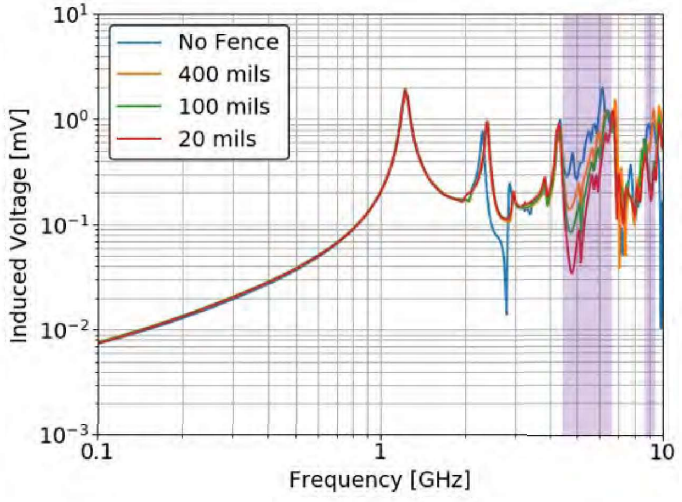
# Effects of Via Fencing on a Practical PCB

- Noticeably different compared to ideal scenario
- Much higher induced voltage
- Via fencing reduces coupling but not as much as expected
  - 5 dB to 20 dB reduction at some frequencies

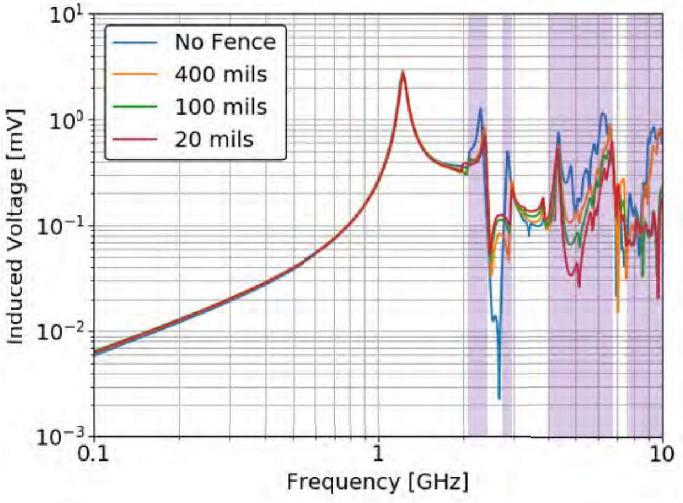



Effects of Via Fencing: Case 1




Effects of Via Fencing: Case 2

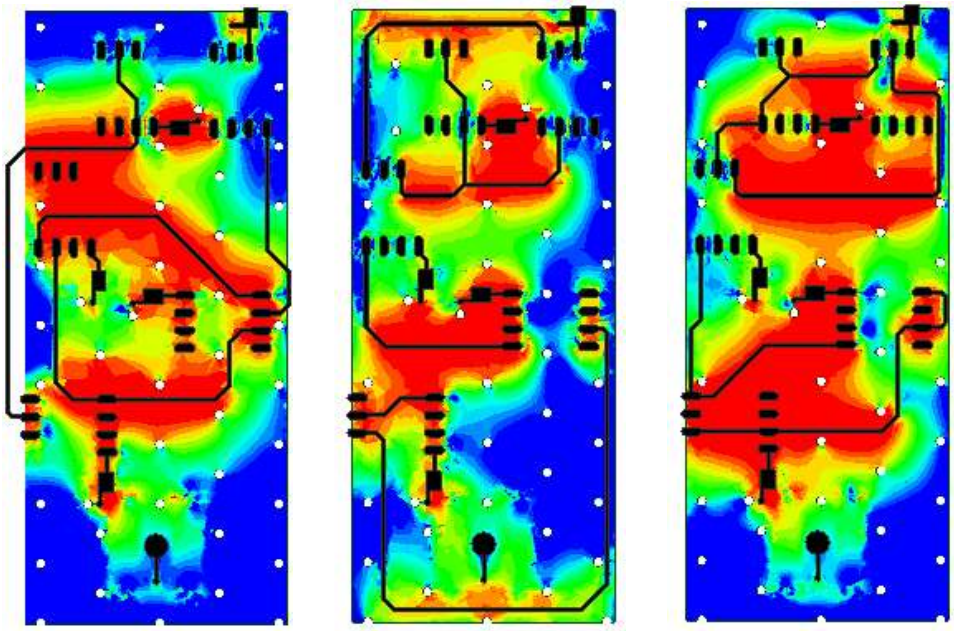



Effects of Via Fencing: Case 3

Tortorich, Ryan P., et al. "A Study on the Radiated Susceptibility of Printed Circuit Boards and the Effects of Via Fencing." *Electronics* 10.5 (2021): 539.

# Surface Current Density

- Data suggests that top layer gaps are the dominant coupling mechanism
  - In fact, ideal edge plating with PEC layers around the PCB perimeter shows minimal reduction in coupling
- Hypothesis is further confirmed by observing surface current density plots for different layouts
  - Surface currents are initially excited at trace locations as opposed to PCB edges



Layout 1 Layout 2 Layout 3

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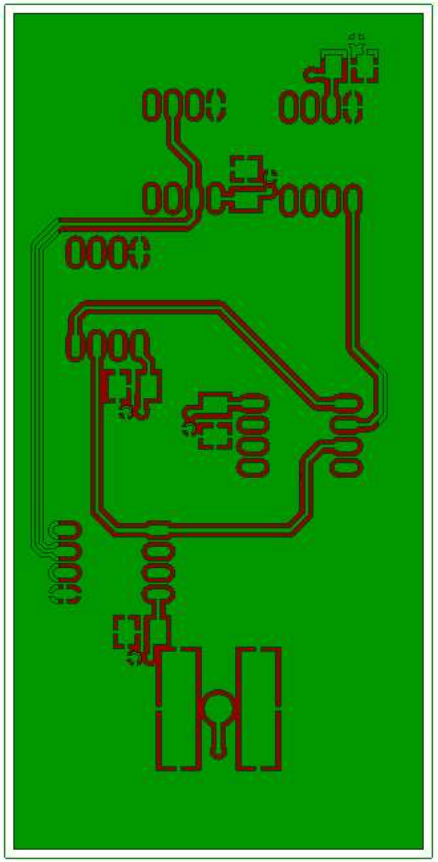
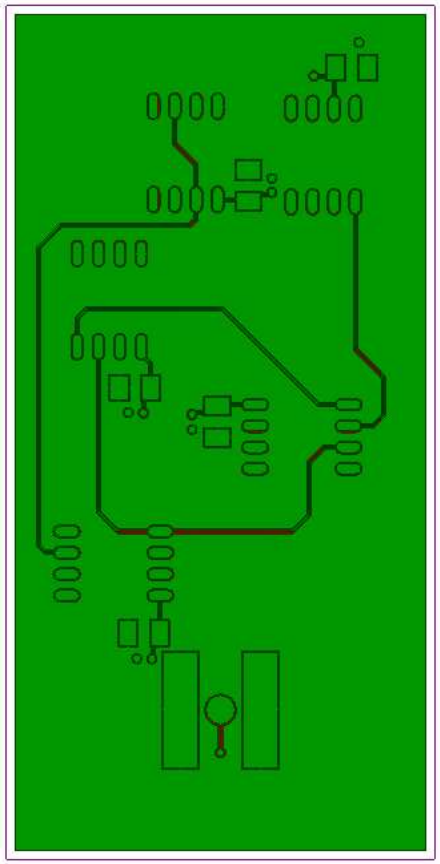
# Effects of Gap Size Variation

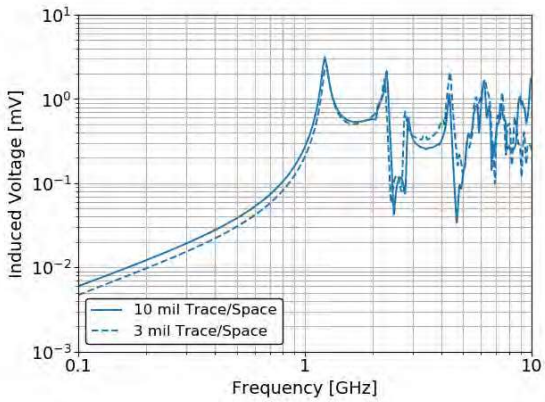


10 mil Trace/Space

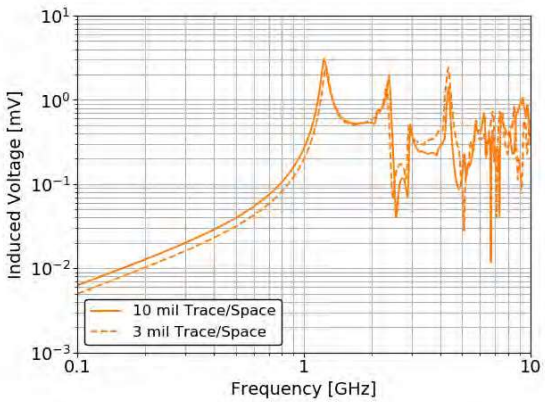


3 mil Trace/Space

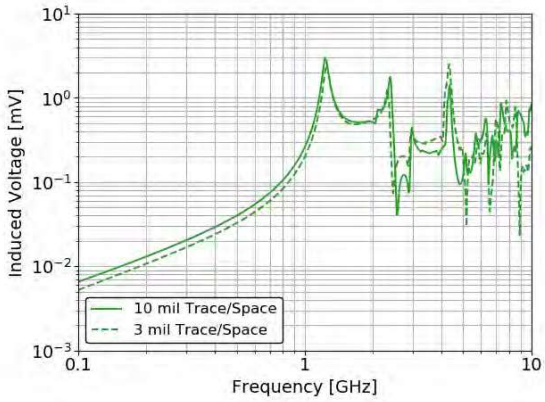
# Effects of Gap Size Variation




No Fence




400 mil Fence

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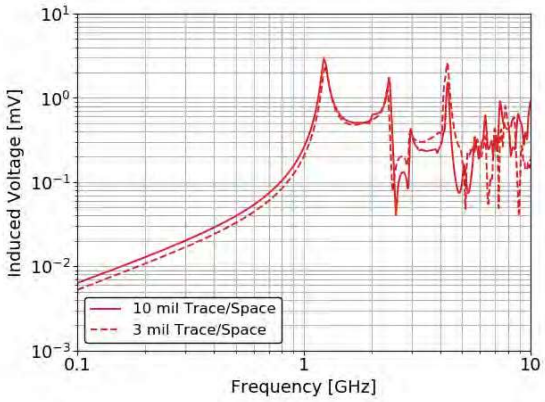


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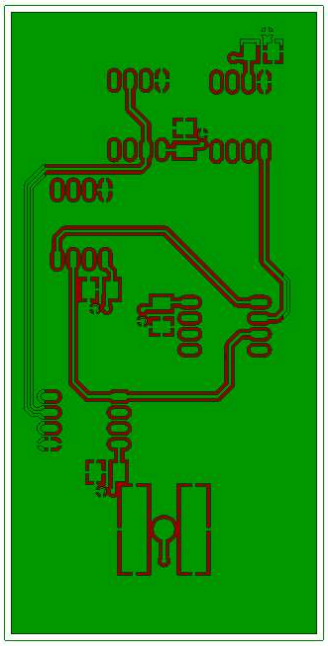

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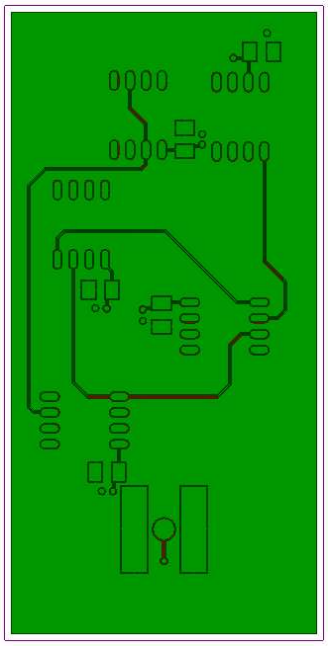
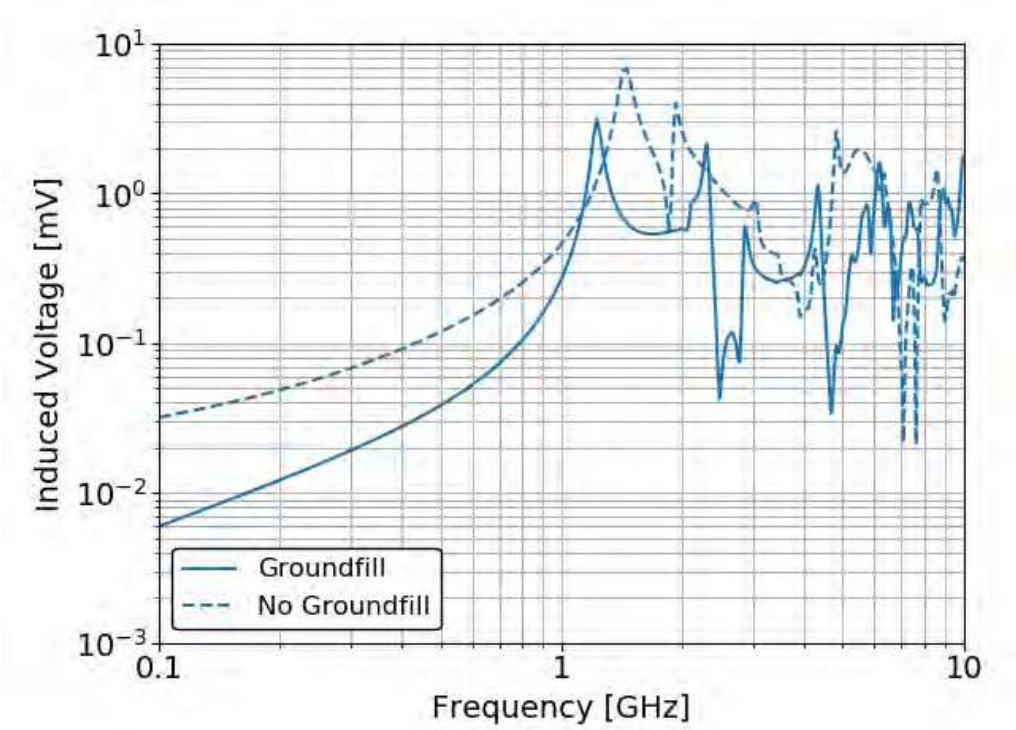
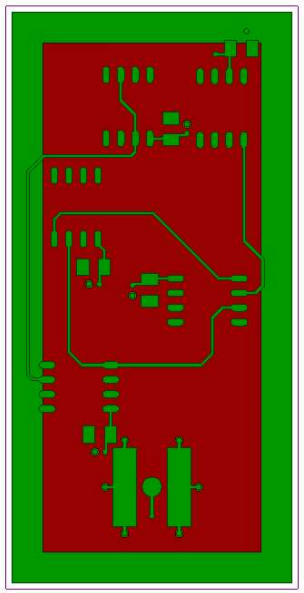


3 mil Trace/Space

# Effects of Groundfill



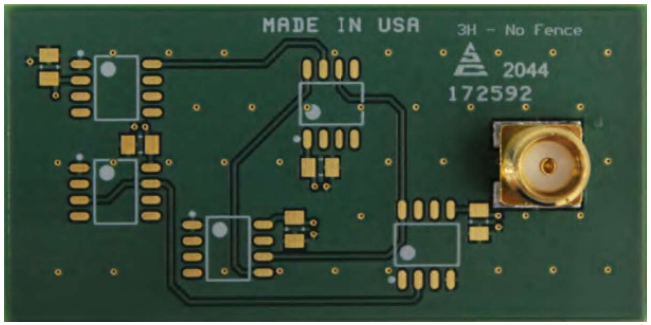

Induced Voltage with and without Groundfill



PCB without Groundfill

# Experimental Testing for Model Validation

Fabricated identical PCBs to enable direct comparison to simulations

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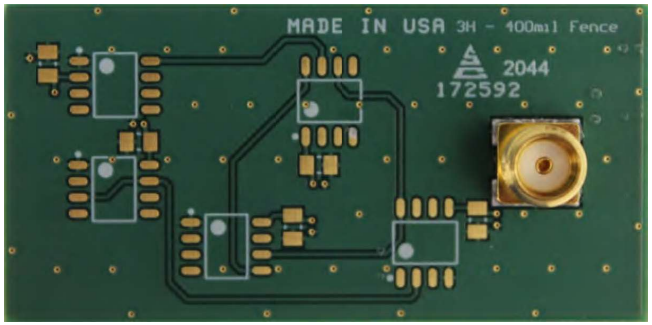


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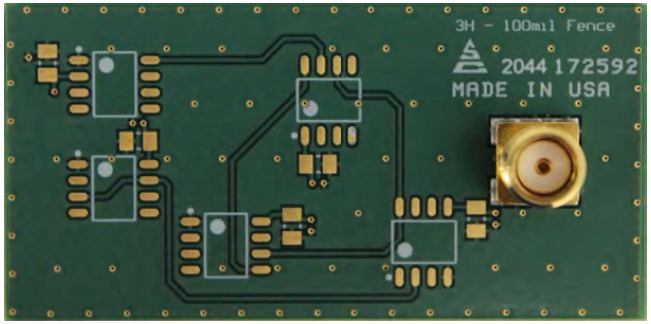


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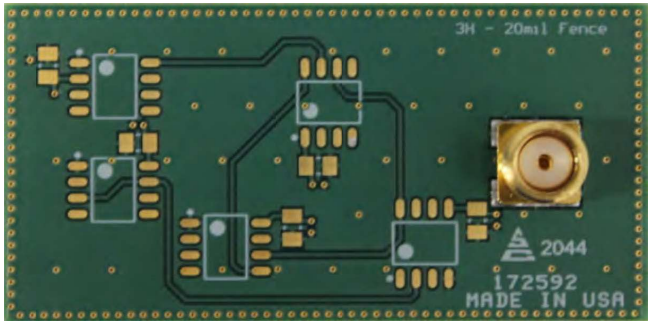
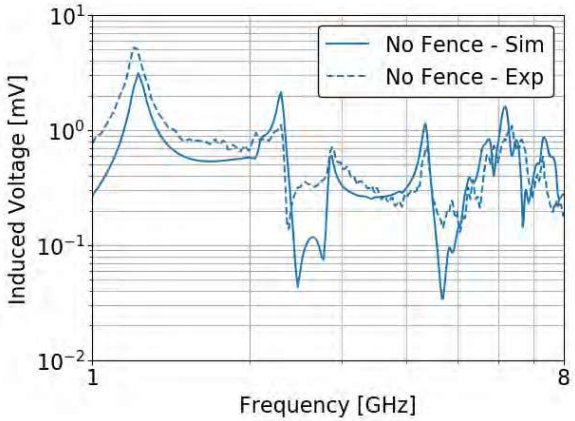



20 mil Fence

# Experimental Testing: Via Fencing

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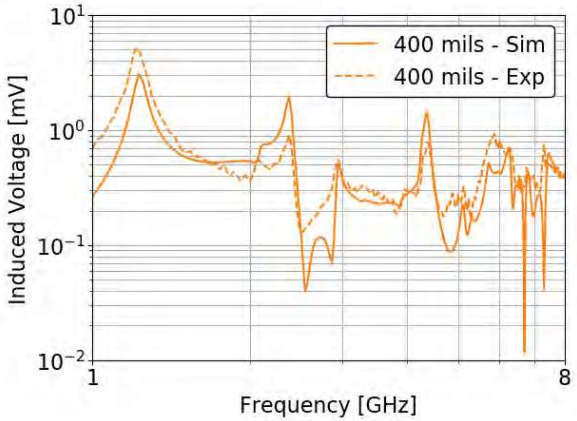


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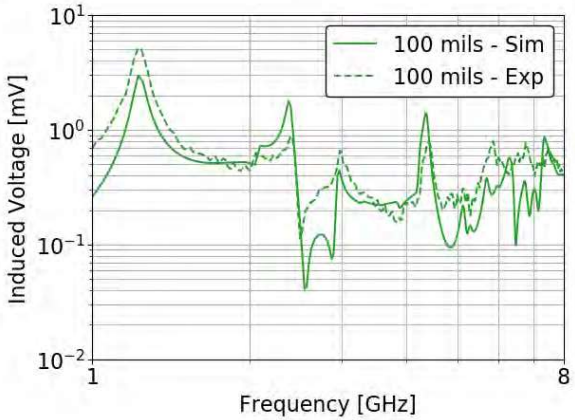


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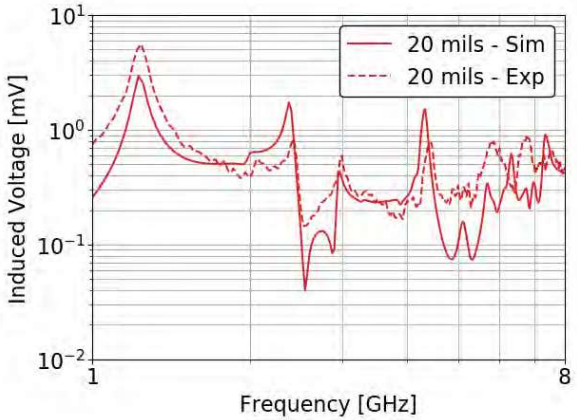


20 mil Fence

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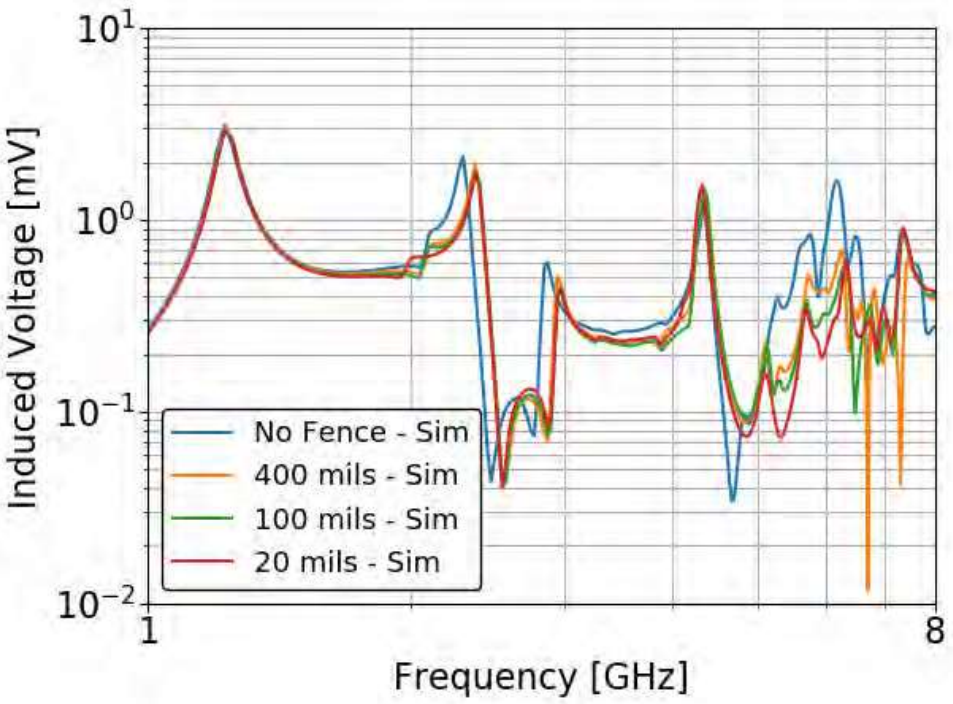
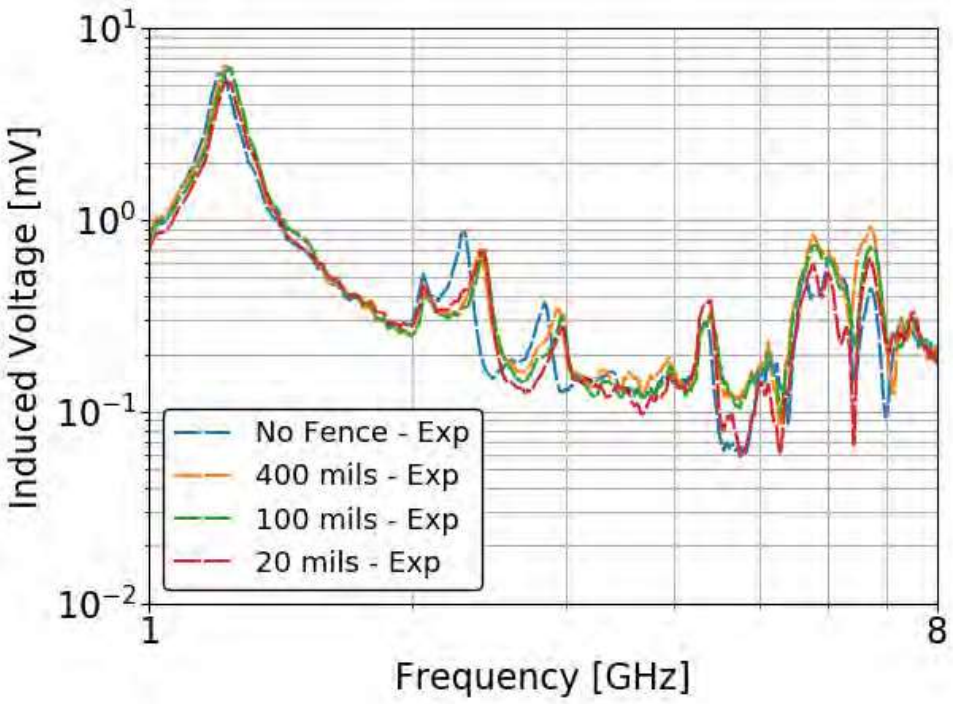



Induced Voltage: Simulation




Induced Voltage: Experiment

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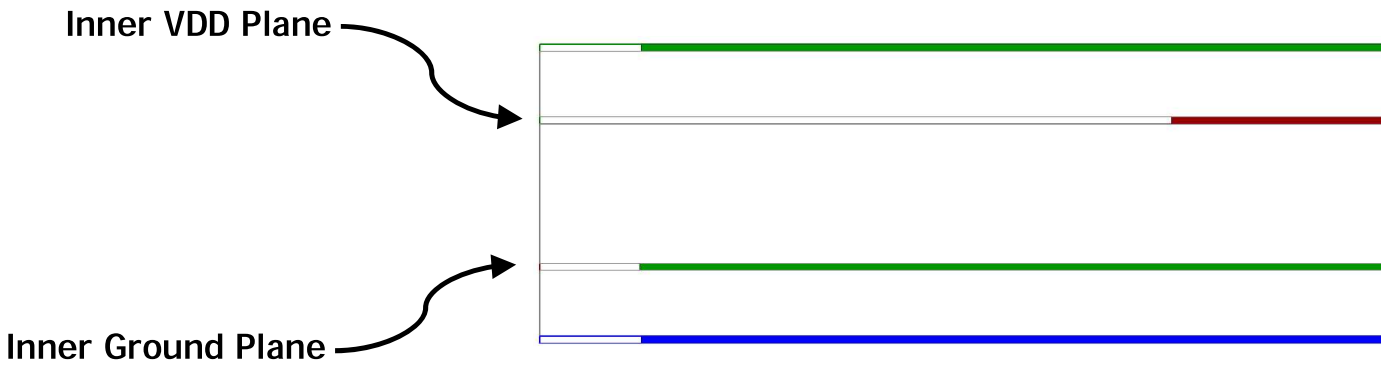
# Buried VDD Plane

- Coupling can be mitigated by burying the VDD plane between solid ground planes



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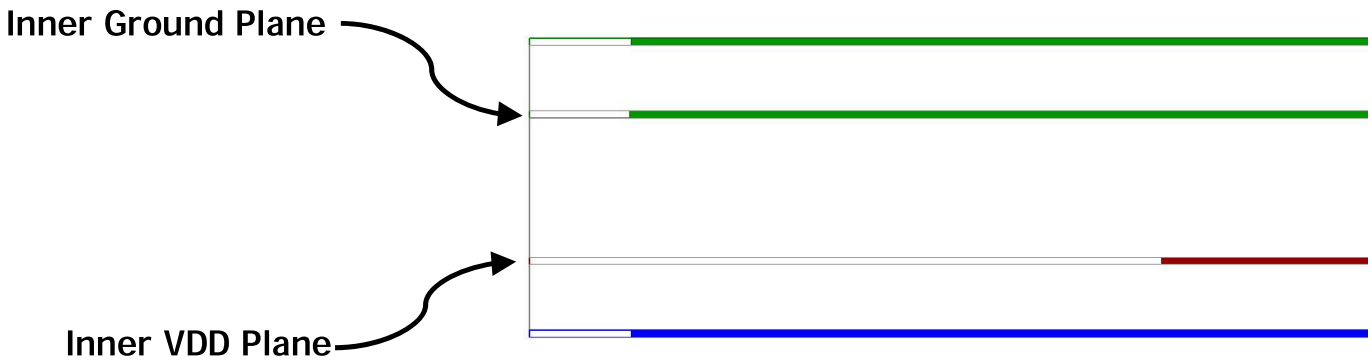

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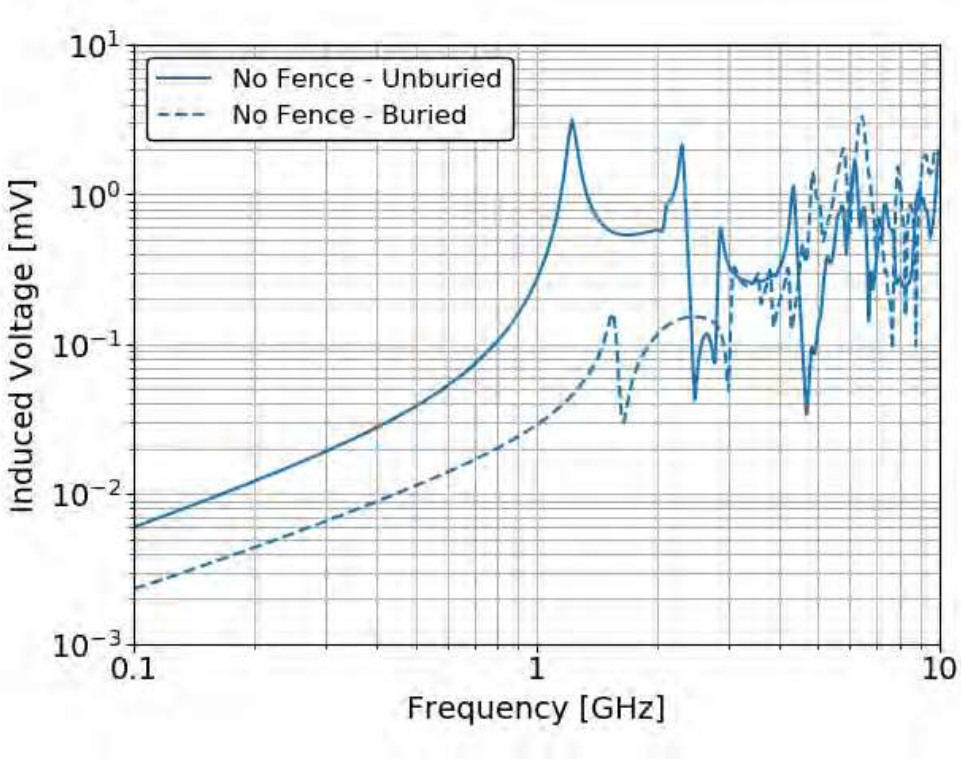
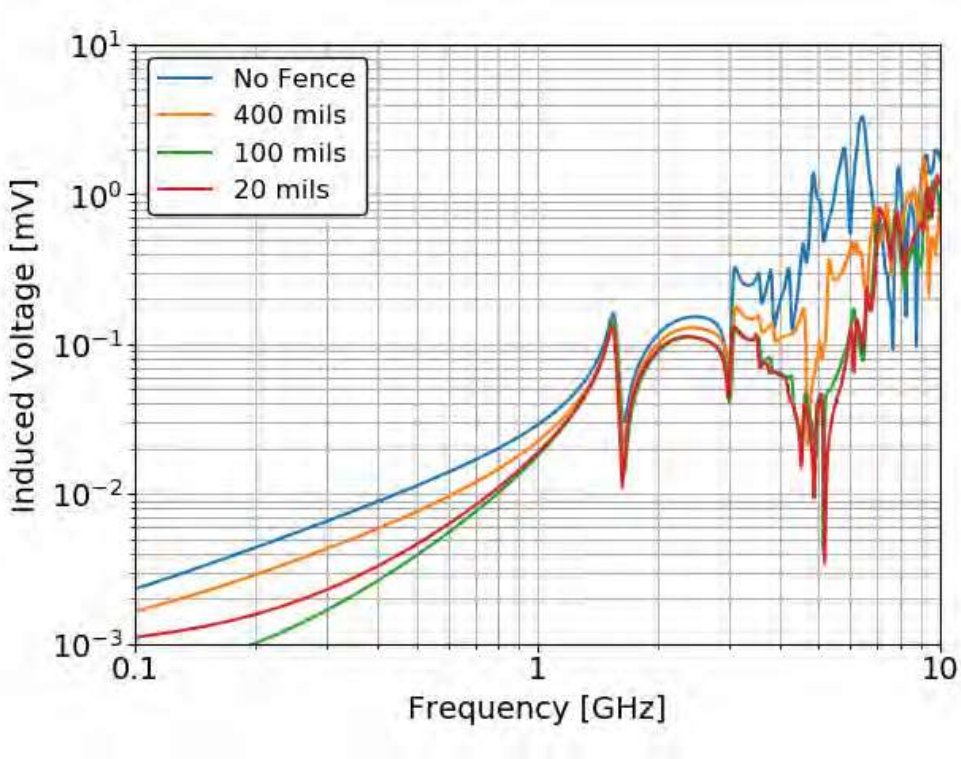
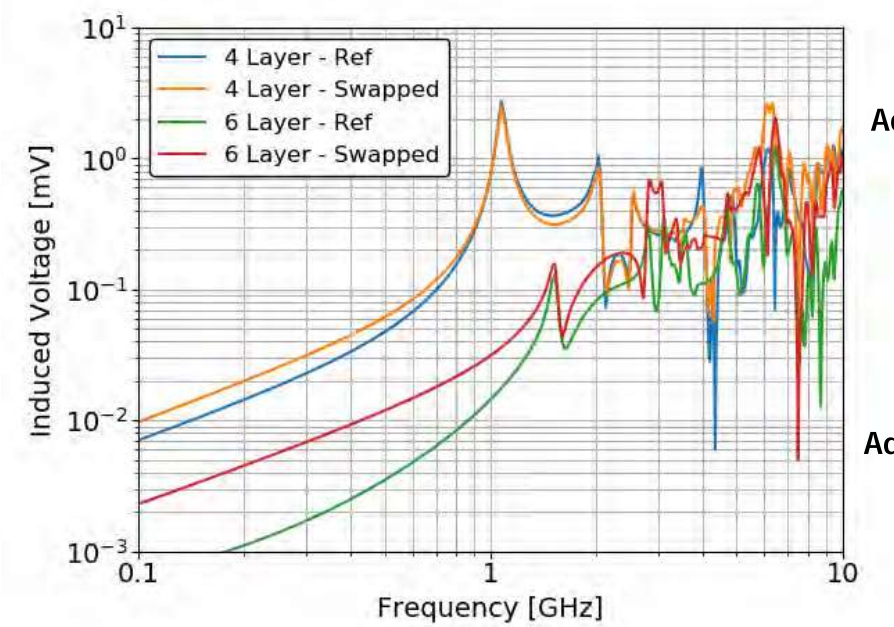


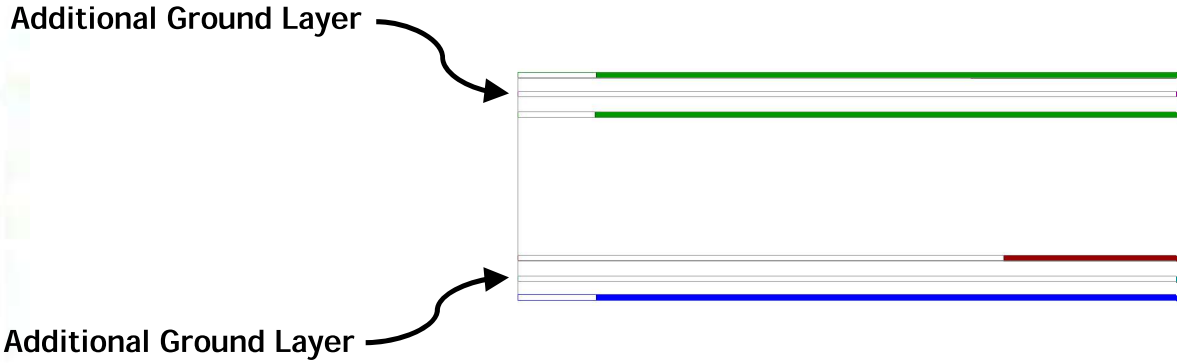




**Buried VDD Plane** **Buried VDD Plane with Via Fencing**

# Buried VDD Plane for 2 Sided Boards

- Buried VDD plane is only possible for single sided 4 layer PCBs
- Double sided 4 layer PCBs still expose the VDD plane
- 6 layer PCB enables buried VDD plane



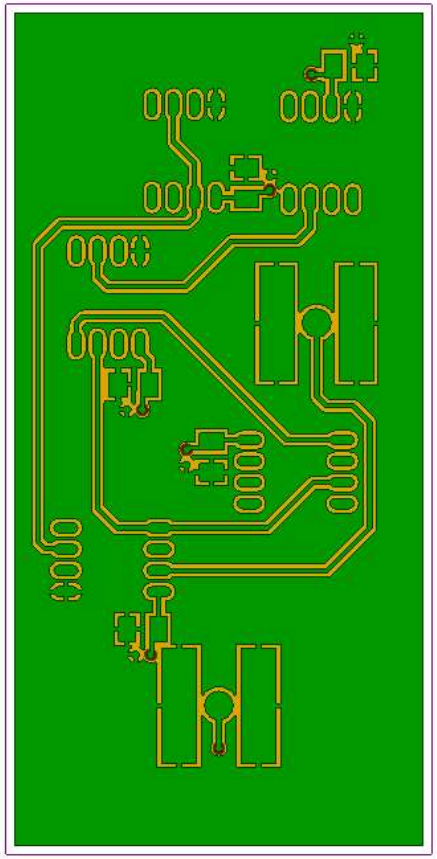




4 Layer vs. 6 Layer - Double Sided PCB

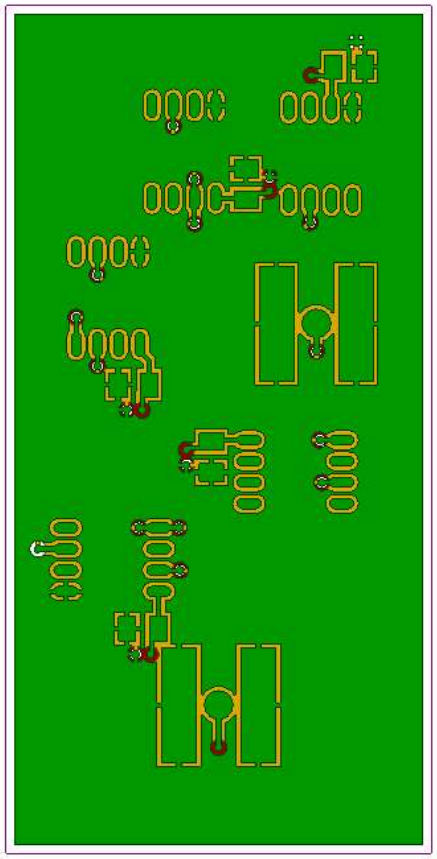
4 Layer – Double Sided PCB

# Buried Traces

- Do buried traces exhibit similar behavior?
- Loaded both ends of each trace
- Compared induced voltage for each trace with and without burying
  - Used a buried VDD plane in both cases to avoid breaking up the power plane with buried traces



Top Traces



Buried Traces

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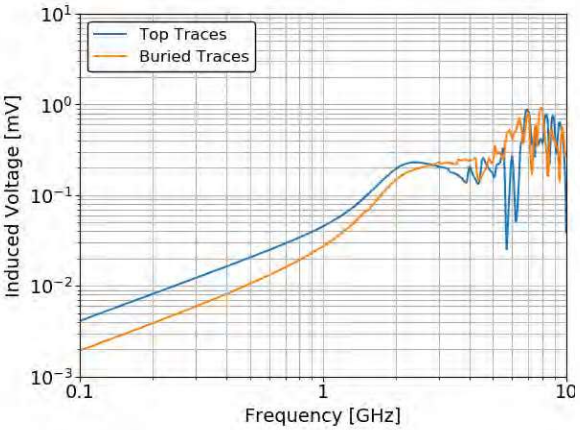
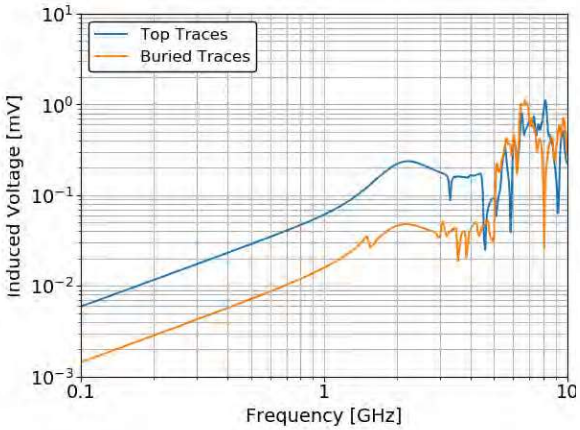
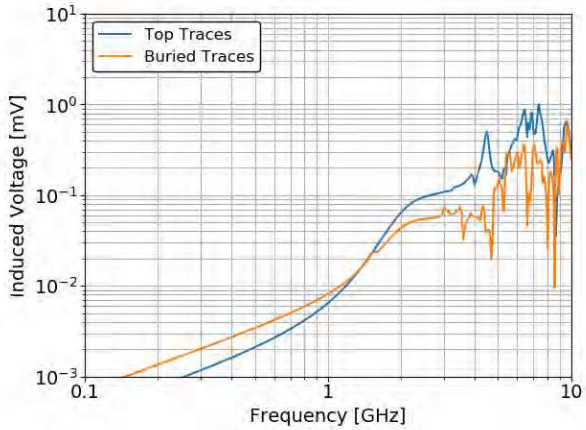



Trace 1




Trace 2

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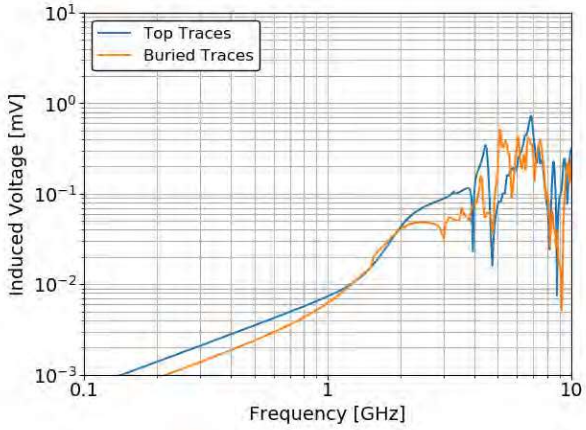


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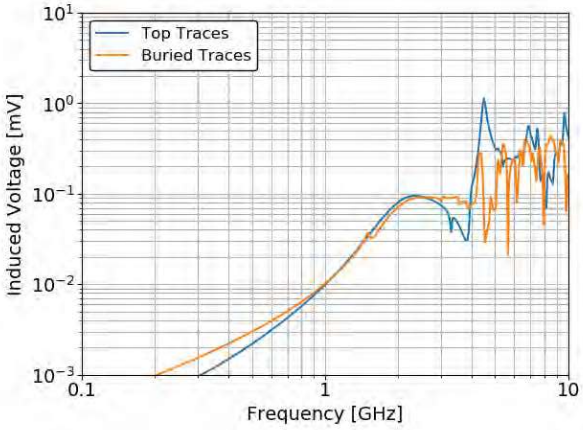
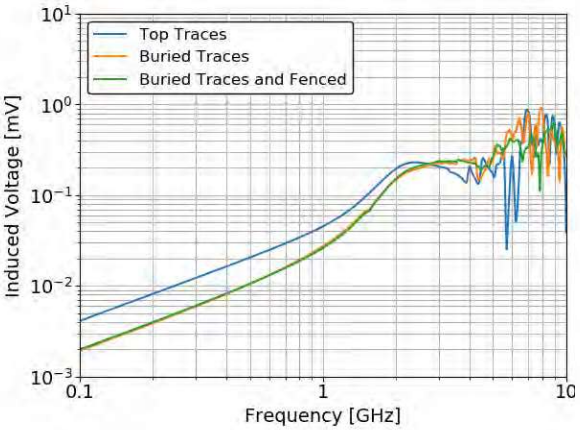



Trace 5

# Buried Traces

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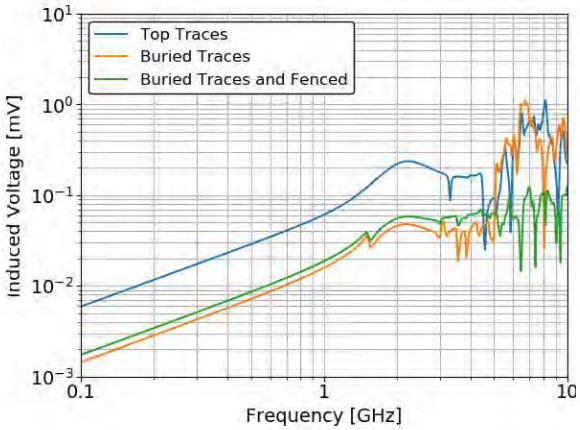


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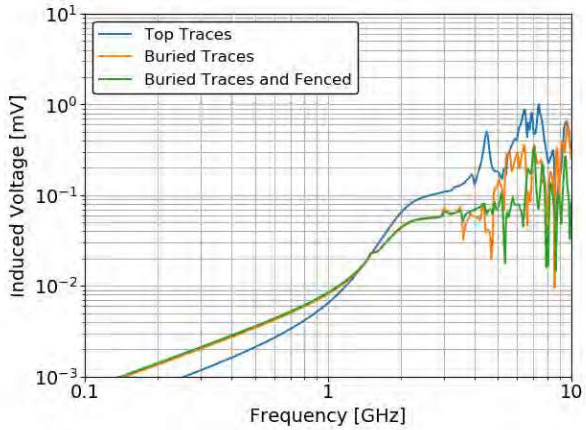


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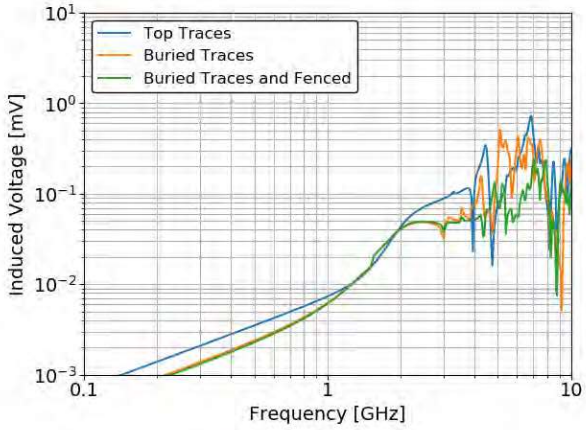


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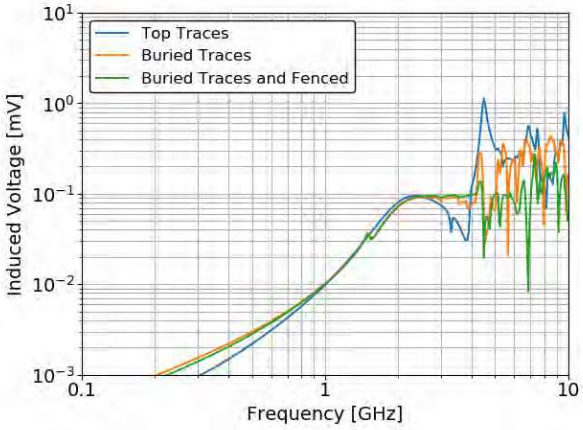
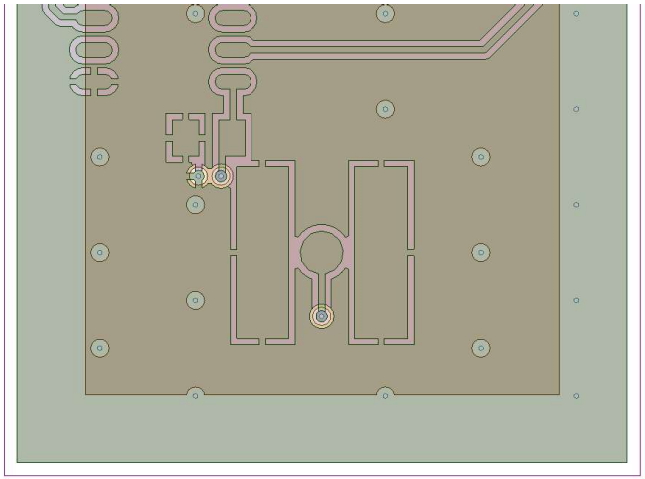


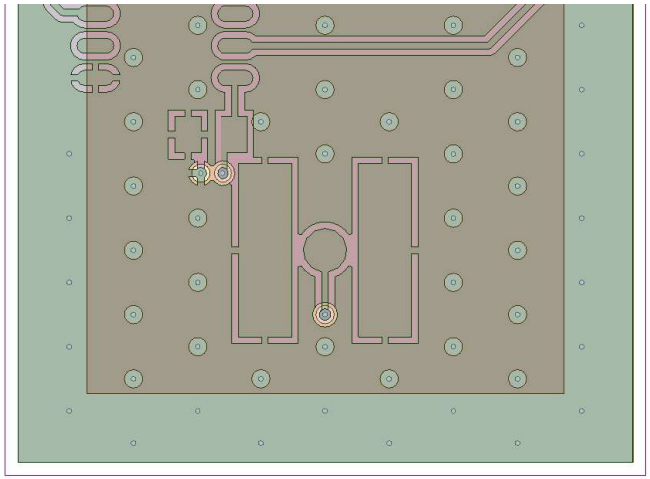

Trace 5

# Via Stitching

- High density via stitching is used to mitigate emissions
  - Ground plane patches may radiate if not tied together well
- Via stitching may also mitigate coupling

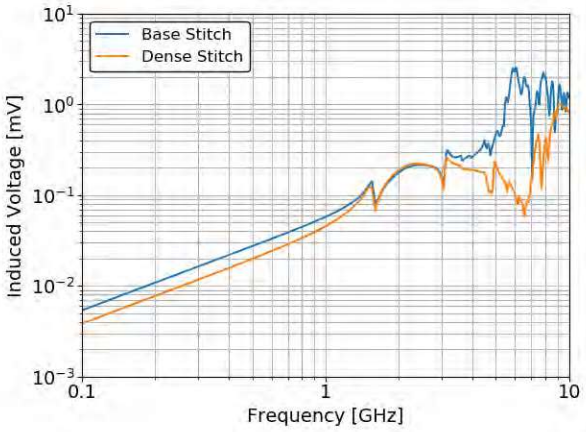


**Base Stitching**

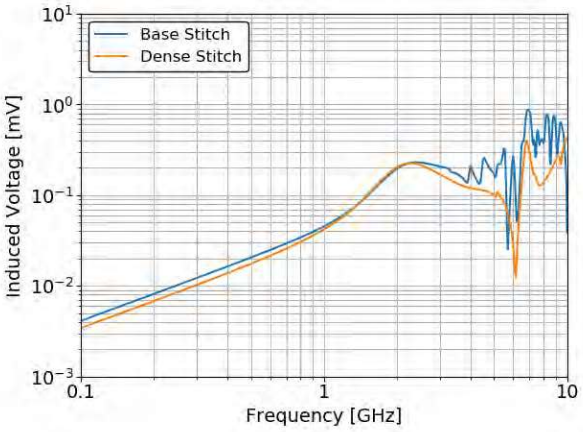


**Dense Stitching**

# Via Stitching




VDD Plane

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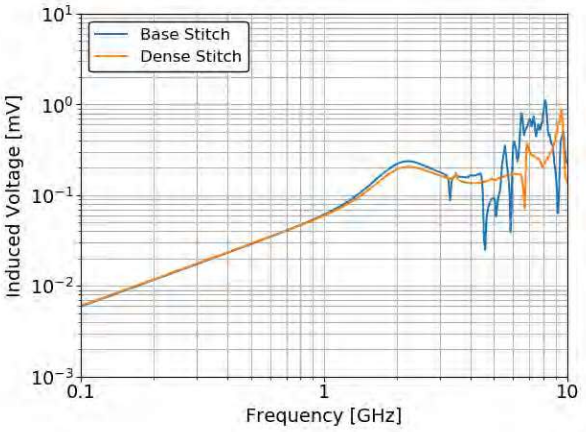


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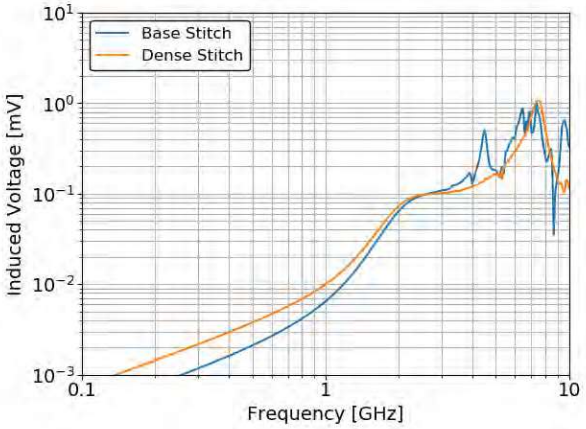


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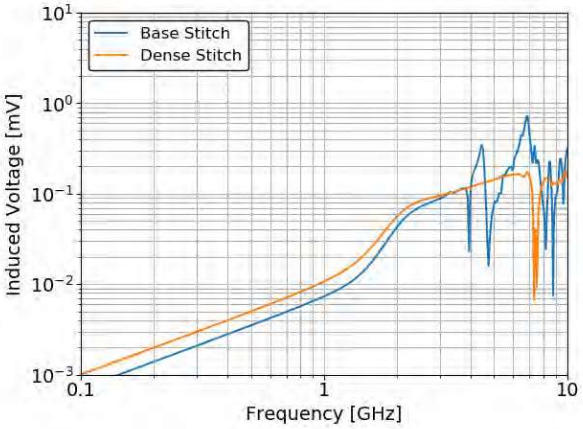


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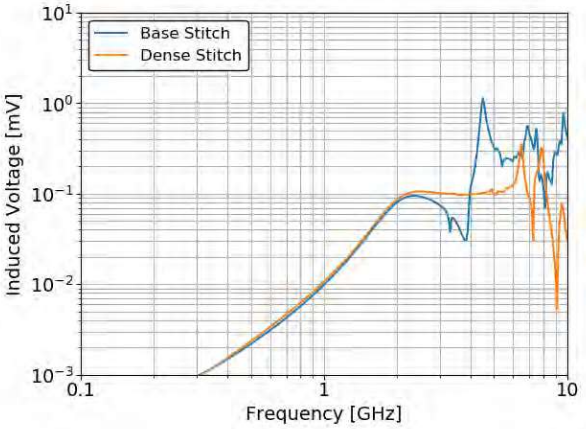


Trace 5

# Conclusions

- PCB design parameters can be adjusted to reduce backdoor coupling
  - Via fencing
  - Buried power plane
  - Buried traces
  - Via stitching
- Combining multiple design techniques can noticeably reduce backdoor coupling
- Backdoor coupling mitigation has potential to reduce probability of effect

# Future Plans

## Broadly Applicable Conclusions

- Rigorous investigation into PCB variations
- Rigorous angle of incidence and polarization variations

## Model Validation

- Ongoing experimental testing with some of the recent layouts shown here
- Will enable greater reliance on additional simulation data for conclusions

## Additional Parameters

- Signal vias
- Power plane pullback
- Electromagnetic bandgap structures
- Realistic component port

## Coupling Prediction

- Machine learning approach to predict backdoor coupling
- Current and planned datasets will provide a realistic set of coupling data for training