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High Voltage Vertical GAN Diodes for Shipboard Power Conversion

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14. ABSTRACT

A major objective of the Naval Power and Energy Systems Technology Development Roadmap is to develop efficient power distribution architectures for improved power handling on U.S. warships, enabling new capabilities requiring high power consumption. Wide bandgap semiconductor technology will help enable this goal. In particular, GaN MOSFET devices can theoretically handle 20 kV; however, this technology is difficult to realize since GaN substrate technology is still immature. This project used long-range, non-destructive optical techniques to study the defects and determine which ones would cause device failure with the aim of helping manufacturers produce vertical device suitable for commercial use. It discovered that Raman spectroscopy and optical profilometry are effective tools for this application.

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HIGH VOLTAGE VERTICAL GAN DIODES FOR SHIPBOARD POWER CONVERSION

1. INTRODUCTION

High powered device based on wide bandgap semiconductors will assist with the goals of the Naval Power and Energy Systems Technology Development Roadmap. Present power conversion technology is mostly Si based with new state the art power converters being based on SiC. However, GaN based power distribution is expected to increase the shipboard power conversion by a factor of 14.5 enabling future payloads requiring higher power such as laser weapons, rail guns, and over the horizon radar. This is due to GaN theoretically being able to handle voltages of 20 kV; however, the inconsistency of GaN wafer technology and non-optimized fabrication process prevents the GaN power technology from being realized to its full potential.

Present GaN technology, used in LED lighting, is derived from lateral 2 dimensional high mobility electron transistors (HEMT). They are excellent for lower power applications; however, since they are lateral devices in a 2D area, the critical electric field factor of 3 lower than a vertical device could have, and since they are typically grown on a non-native substrate such as AlN or Al_2O_3, they have a dislocation density 3 orders of magnitude larger. Vertical devices would require a high quality substrate, though it is important we improve the yield of GaN technology. Diagrams of lateral and vertical GaN devices is shown in **Fig. 1.**

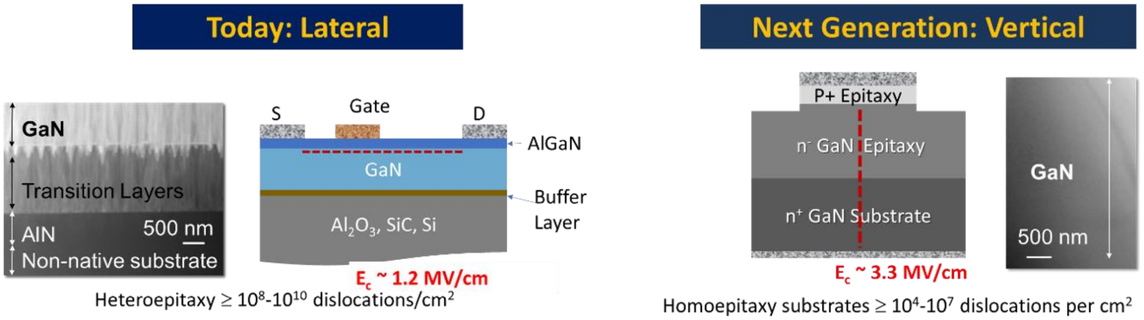

Fig 1. Transmission Electron Microscopy Image and cross section of a Lateral GaN device (Left) and a Vertical Gan Device (Right).

Vertical SiC technology had this same challenges until it was discovered that defects could be quickly detected with ultraviolet photoluminescence imaging [1], [2]. Feedback from this measurement enabled wafer manufacturers to have a cost effective quality control measures enabling commercial quality SiC devices to be manufactured. There has yet to be a standard technique developed for GaN.

The main objective of this study was to probe defects using long-range, non-destructive techniques, and correlate the results to device performance of vertical diodes on a wafer. These techniques included Raman spectroscopy, photoluminescence spectroscopy, and optical profilometry, which previous NRL research has proposed [3]. This program has successful correlated these two techniques to device performance resulting in multiple NRL patents and publications.

2. DEVICE FABRICATION

Two methods were used for diodes fabrication in this research. The first was a simple MESA isolation test, and the second was a more complicated foundry process developed planar foundry-type process developed at NRL under a recent ARPA-E program. The first step in this process involves growth of a low-doped N-type layer fabricated using Si doping to obtain an n-type carrier concentration of $1x10^{16}$ cm^{-3}. A P-type layer is grown using Mg doping with 500 nm [Mg] $>10^{19}$ cm^{-3} and acceptor concentration

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~4x10^{17} cm^{-3}. The p-type layer is capped with a 15 nm [Mg] > 10^{20} cm^{-3} layer to allow an ohmic p-type metal contact. Samples were electrically isolated though either a MESA isolation created from a Cl_2 etch through the anode layer (see **Fig. 2**) or a deep implant isolation (see **Fig. 3**). Since high powered devices do not work well with sharp corners, a more advanced fabrication technique avoids this with an implant isolation layer instead of a MESA isolation layer,and the foundry-type process also includes an edge termination region used to improve the breakdown voltage by spreading the electric field. These layers are fabricated using a N_2 ion implant source. The injected N creates a compensator making the region insulating. Though the implant isolated diodes perform better, it requires two additional steps of implant isolation and edge termination. These processes cannot be performed on site.

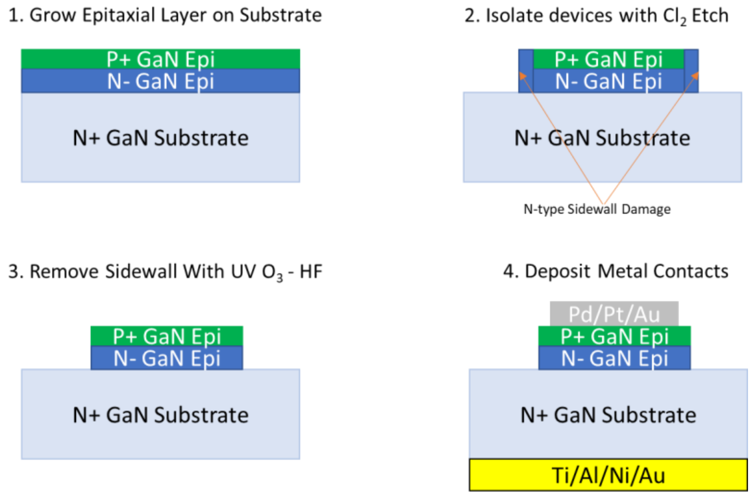

Fig 2. An illustration of the process flow for vertical diode fabrication using a simple MESA isolation techniques [5].

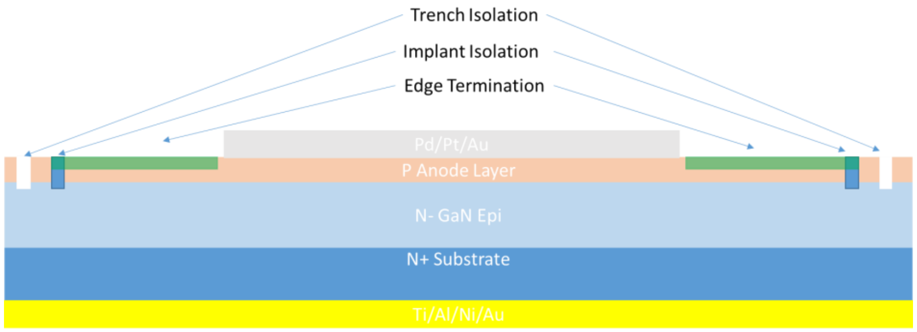

Fig. 3. Design of an implant isolated diode.

3. OVERIEW OF LONG-RANGE TECHNIQUES

Raman spectroscopy peaks are used to detect phonon modes. The phonon properties change if there is a change in stress, quality, or carrier concentration of the crystal. Particularly for GaN, two peaks are used: the E_2 peak at 567 cm^{-1} shifts and broadens when the crystal stress or quality changes, and the A_1 (LO) peak at 730-900 cm^{-1} can be used to determine the carrier concentration using graph in **Fig. 4** [6]. Research from this fellowship has shown that points of high carrier concentration can lead to larger leakage currents [7]–[9]. However the regions of high crystal stress represent a difference of about 0.2 cm^{-1}, In the E_2 peak. The subtle shift can be difficult to detect; however, the changes in crystal stress correspond to large changes in the A_1 peak position that are easy to detect. Using lithography, arrays of vertical diodes can be aligned to these regions of crystal stress. Creating a Raman map of the position of these peaks can be useful in determining the uniformity of the sample and pin point defective areas of the sample. Samples are typically classified into one of three categories after a Raman map shown in **Fig. 5** Wafers with a uniform Raman map are called type I samples. They are usually synthesized by more expensive techniques such as the ammonothermal method. Type IIa samples have defects in regular patterns. They are often created using the dot-core technique. This techniques has crystals seeded on a sapphire wafer, which when grown regions of crystal stress are typically at the points where the coalescence occurred [10]. This method is less expensive, and can produce high yield results by avoiding the defects. Type IIb samples have an irregular pattern of defects, making it difficult to predict if a fabricated device will be on a defect, thus are not ideal for vertical device applications.

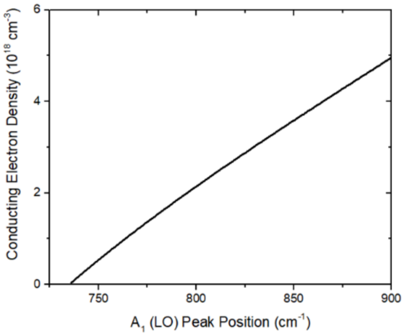

Fig. 4. A_1 peak position vs carrier concentration using the formulas in reference [6].

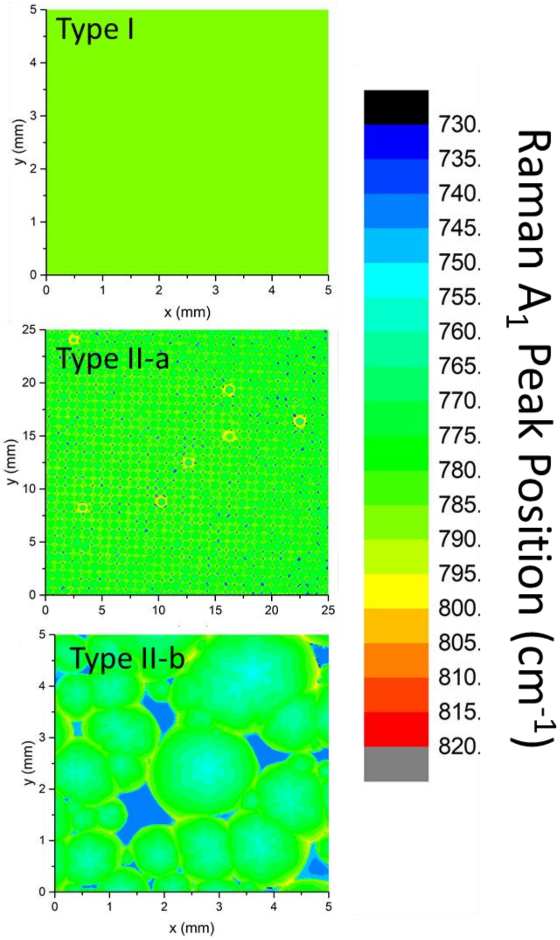

Figure 5. Raman maps of type I (uniform), type II-a (patterned), and type II-b (irregular) wafers [5].

Optical profilometry can be taken using the Zygo^{TM} Optical profilometer in the Nanoscience Institute. This techniques can detect changes in surface morphology, which is often indicative of a defect under the surface, such as threading dislocation and substrate non-uniformities (illustrated in **Fig. 6**), both of which can decrease diode performance.

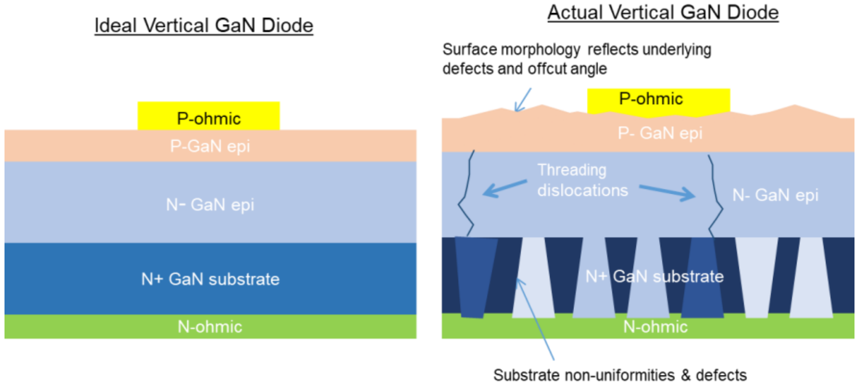

Fig. 6. (Left) An illustration of an ideal vertical diode. (Right) A real diode has defects that are under the surface that cause changes in surface morphology, which can be detected with optical profilometry.

One advantage of optical profilometry is its capability of mapping full 2 inch wafers in a few hours. This makes it useful for predicting the device yield rate and quickly screening wafers. **Fig. 7** highlights a process for doing this. Since defects in the sample manifest as bumps, pits or rough regions on the surface, a way to estimate yield is to calculate the probability that a sample will be on an abnormal region. This can be done by dividing the samples into unit cells of size equal to a devices size of interest. The RMS roughness can be calculated after a polynomial subtraction and a Generalized ESD test is used to calculate the number of bumps and pits present in each area. Previous research has shown that devices fail at RMS roughness > 25 nm [11] or a failure can occur if a single defect is present, thus these are used as the failure criteria in **Fig. 7c**.

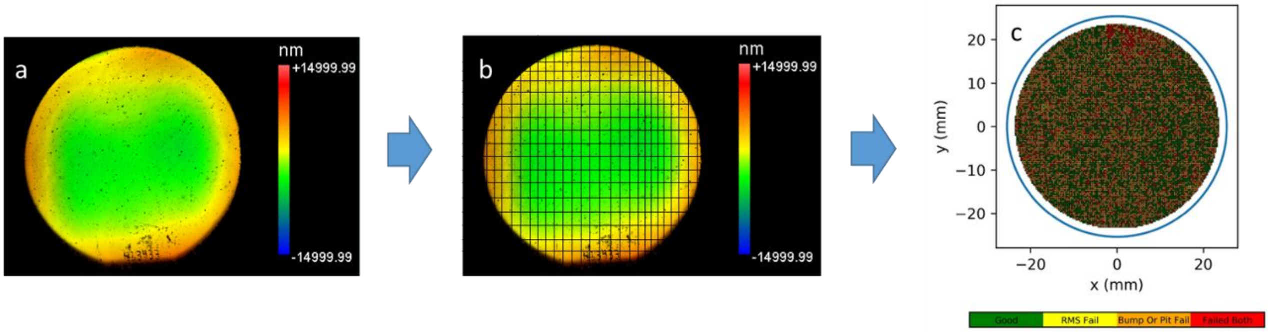

Figure 7. An illustration of using Optical Profilometry to predict the quality of the devices. (a) A Optical Profilometry map of a full 2 inch wafer. To calculate the number of failed devices, the wafer is divided into unit cells as illustrated in part (b). (c) Example of real data results on 325x325 µm cells. Unit cells are highlighted in green if they pass, yellow if the RMS is too large (> 25 nm), orange is a bump or pit is in the cell, and red if both fail criteria are met.

4. EXPERIMENTAL RESULTS

Since diodes are expected to block large leakage currents in power devices, the abnormalities detected using Raman and Optical profilometry were compared to the reverse bias. To test the effect of Raman devices on the quality of the sample, the devices were fabricated in square arrays on samples with a regular pattern of defects spaced 800 µm apart. The diodes were aligned so that the corner devices were on the defects. A Raman map of a wafer with devices is shown in **Fig. 8**.

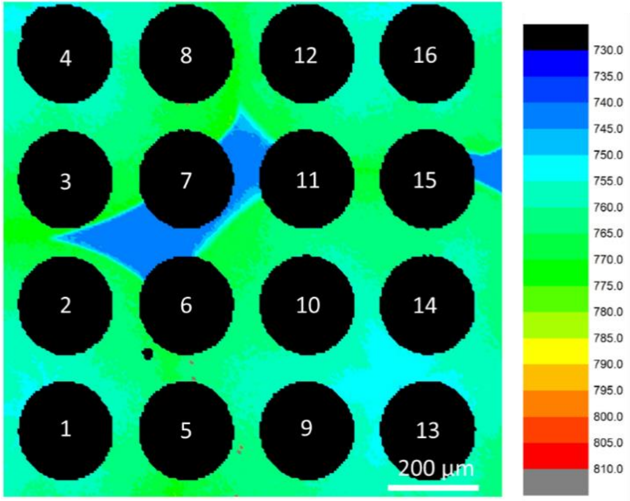

Fig. 8. A Raman map of the A_1 peak over a 4x4 grid of devices with a 200 µm diameter. The black numbered regions are the location of the devices. The defects are on devices 1,4,13, and 16 and are on the points with high crystal stress.

To test the stability of the diodes a 200 V reverse bias IV curve was taken on the samples (results in **Fig. 9**). The dislocation on the defects caused by high crystal stress have leakage currents around 10^{-6} A. While those off defects are typically 10^{-12}-10^{-8} yielding at least 4 orders of magnitude improvement obtained by avoiding the defects.

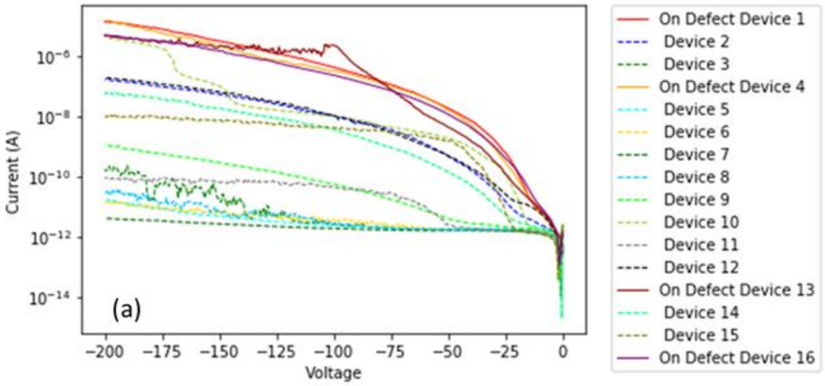

Fig. 9. 200 V reverse bias diode IV curve. The device numbers corresponds the labels in Figure 8 [8].

This project developed a technique using optical profilometry to predict the percentage of high-quality diodes. This was accomplished by mapping full 2 inch GaN wafers the dividing the wafers into regions equal to the device size of interests. A Generalized Extreme Studentized Deviant Test (ESD) can be used to determine spots which are bump and pits. The probability of a device landing on a defect can then be calculated. This method was tested experimentally with the results shown in **Fig. 10**. This method was found to be accurate for low quality wafers; however, for higher quality wafers the predicted yield is typically lower than the experimental yield due to several of the defects detected being benign. Machine learning algorithms may be useful for determining which defects are benign and which cause failures making this process more accurate.

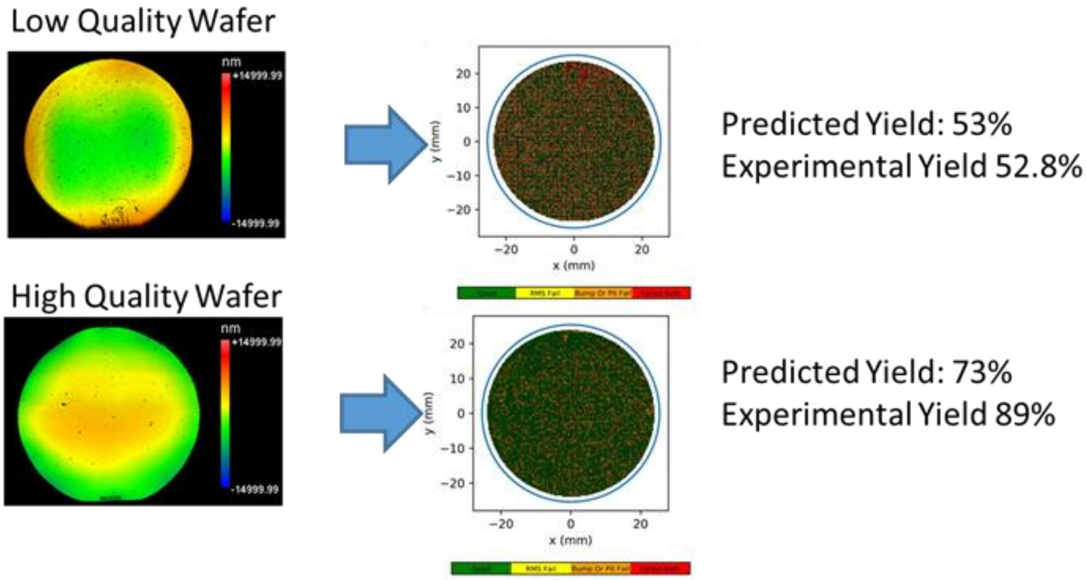

Figure 10. The model described in NRL provisional patent "Surface Profile Mapping Techniques for Evaluating III-N Device Performance and Yield [2]" The left contains a raw surface profile map for two wafers. The right contains a map predicting the regions of the sample that will produce a high-quality diode in green. The predicted yield is determined from the probability that a randomly placed diode will be on a defect.

5. CONCLUSIONS

The purpose of this Karles fellowship was to study the reliability of non-destructive wafer scale techniques to predict the quality of vertical devices to work towards the development of 15 kV DC needed for the power conversion technology specified in the Naval Power and Energy Systems Technology Development Roadmap. Specifically Raman spectroscopy and Optical profilometry were studied. It was discovered that Raman spectroscopy is useful at identifying defects over short ranges, specifically looking for regions of high crystal stress. Optical profilometry is effective at predicting the probability of devices failing on a full wafer at long ranges; however, the presence of benign defects trigger false positives in higher quality wafers. The optical profilometry test could be more accurate if a machine learning algorithm was developed to distinguish between benign and catastrophic defects. This will be studied as part of current NISE project "Developing Computational Algorithms to Predict the Quality of High Voltage GaN Diodes Using Data Science and Machine Learning."

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