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Thermal-Mechanical Stress Limitations for Through-Wafer Vias and Implications for Wafer-Level Packaging

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14. ABSTRACT

Solid copper through-silicon vias (TSVs) fabricated in silicon (Si)-on-insulator wafers failed during subsequent thermal processing. A study of stress, induced by coefficient of thermal expansion (CTE) mismatch with the surrounding Si, was conducted as a cause of failure mechanisms for the TSVs. Three-dimensional thermal-mechanical models of via structures under the thermal conditions of die-attach (200–300 °C) were simulated in ANSYS to gain a better understanding of the thermal stresses seen within the vias and surrounding silicon. Models show that the stress in the copper TSV (>800 MPa) can be well over the yield strength of the material (210 MPa). Further studies were conducted using tungsten (lower CTE, higher yield strength) and hollow-via geometries to find more robust fabrication solutions capable of withstanding higher thermal budgets.

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through-silicon via, TSV, TSV robustness, microfabrication, wafer-level packaging

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1. Introduction

Quadrupole mass gyroscopes (QMG) are resonant microelectromechanical system sensors used to monitor position by detecting changes in Coriolis acceleration. QMGs require ultra-low vacuum packaging to achieve high Qs at their resonance frequency. State-of-the-art technology at the US Army Combat Capabilities Development Command Army Research Laboratory is capable of packaging QMGs at the die-level with less than 1-µTorr internal pressure.[1] Unfortunately, drawbacks of this method include long turnaround times and low-volume production, which means important information on device yield and uniformity across the wafer is difficult to collect. Packaging these devices at the wafer scale would increase the throughput from four devices to 150 devices in a fabrication run. Wafer mapping of device performance would be possible and not only would the pace of research increase, but having a fully packaged product would increase the likelihood of technology transition to Department of Defense contractors. A final benefit is the form of device/package co-design as package requirements (dimensions, design rules, materials, etc.) can limit the performance of the QMG—and vice versa.

2. Wafer-Level Packaging Fabrication Process

There are many different ways to package at the wafer scale (multiple); this work utilizes a through-silicon via (TSV) placed in the cap (Fig. 1) as it minimizes device footprint to QMG die size, and the cap and device wafers can be built in parallel, reducing fabrication time. QMGs are defined lithographically and etched out of a 100-µm thick device layer of a silicon-on-insulator (SOI) wafer. Cap wafers are also built using a SOI wafer. A deep reactive ion etch (DRIE) is used to create the vias in the 100-µm-thick high-resistivity (>10k Ωcm) device layer (Fig. 1b). The wafer is then thermally oxidized to grow a 2-µm silicon dioxide diffusion barrier followed by a reactive ion etch to punch through the buried oxide (BOX) layer (Fig. 1c). A titanium/copper (0.02/3 µm) seed layer is sputtered over the wafer and the vias are filled with copper by electroplating (Fig. 1d). The copper is annealed at 300 °C for 24 h to drive out contaminants, promote grain growth, and improve the conductivity of the material. The vias are then chemical mechanical polished (CMP) to remove the excess copper around the vias (Fig. 1e). Titanium/gold (0.02/0.730 µm) contact pads and routing traces are deposited for gold-tin eutectic bonding to the QMG wafer (Fig. 1f), and optional cavities can be formed using DRIE and getters deposited to keep package pressure stable can be deposited into the cavities (Fig. 1g). At this point, the cap wafer is flipped over and aligned with the device wafer and the two are placed in a vacuum chamber and bonded together

(Fig. 1h). The handle of the cap SOI wafer is removed (Fig. 1i) and subsequent metallization can be deposited (Fig. 1j).

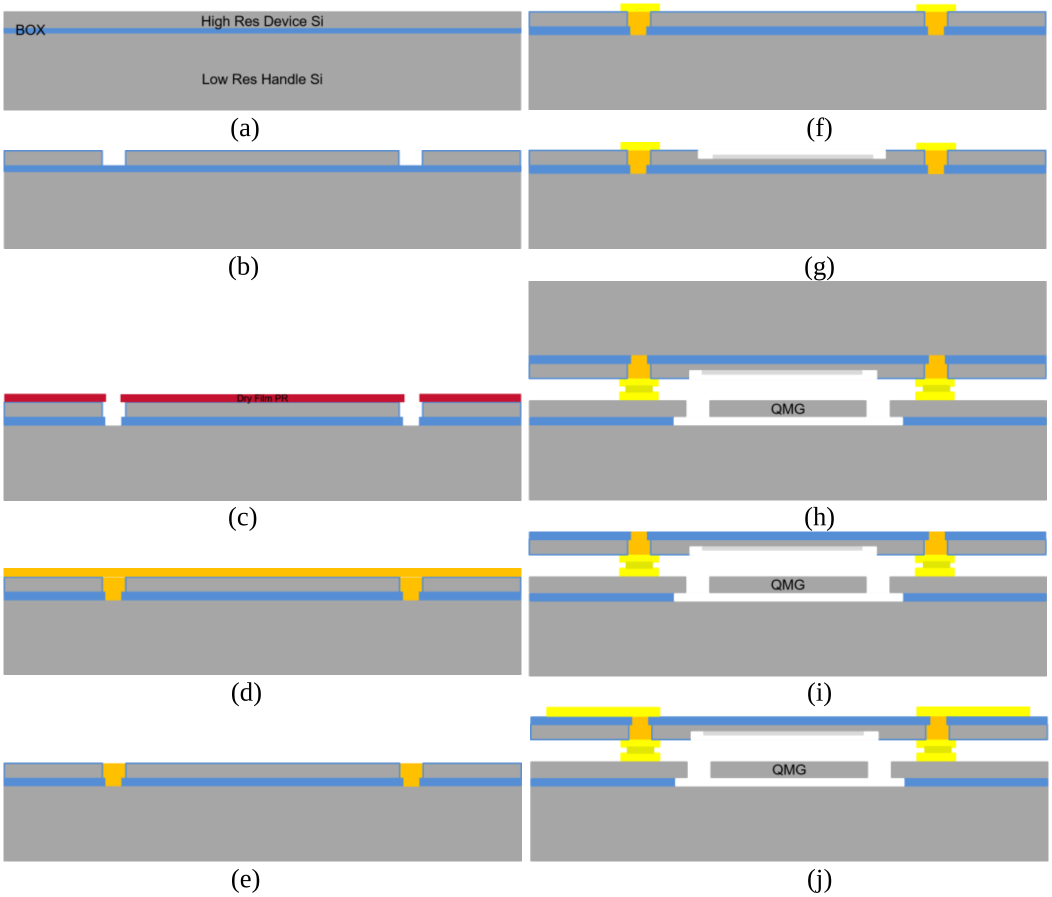

Fig. 1 **Cross section of via fabrication and QMG packaging processes (not to scale)**

3. Via Fabrication Issues

Cap wafers were fabricated up through step (e) of Fig. 1, but work was halted when the wafers were damaged after the CMP step (Fig. 1e). Inspection of a sacrificial wafer (Fig. 2) prior to annealing and CMP showed that vias were completely filled with no voids. After wafers came back from CMP, large regions of the device layer were delaminated around vias and many vias had significant voiding (Fig. 3). It was hypothesized that stress generated during the 300 °C anneal due to coefficient of thermal expansion (CTE) mismatch is what caused the voiding and the delamination of the SOI device layer.

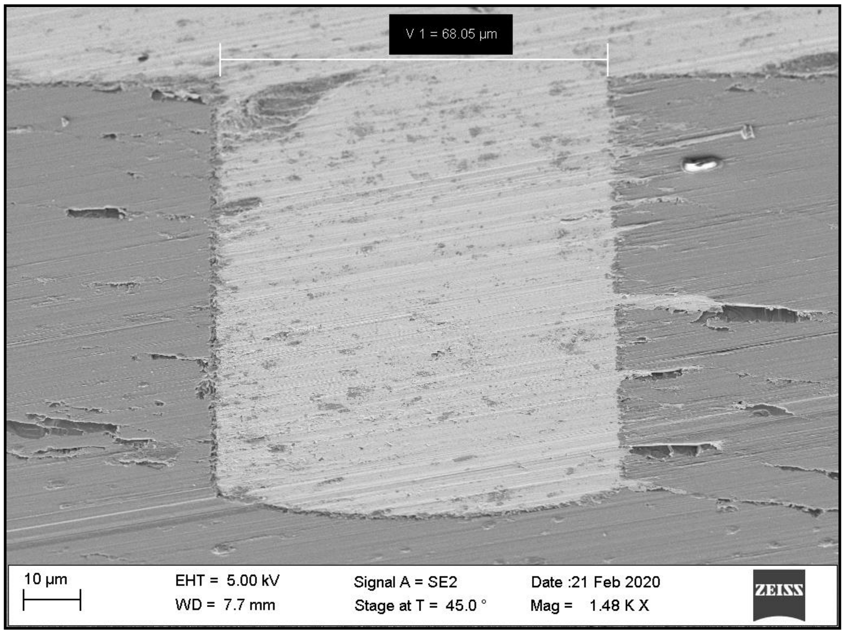

Fig. 2 Scanning electron microscopy (SEM) cross section of filled via before CMP. The protrusions on the right side of the via are where copper smeared across the cross section of the wafer during dicing and not fabrication related.

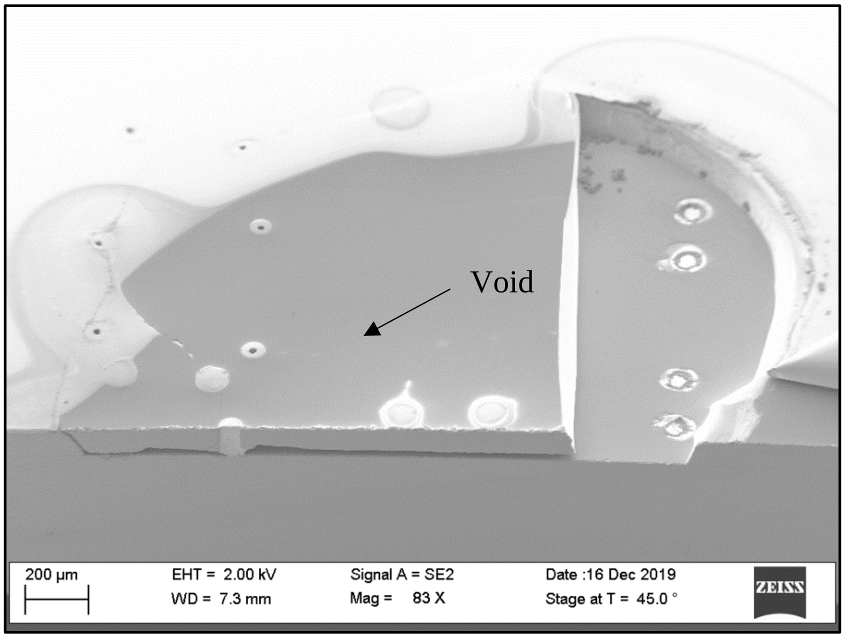

Fig. 3 SEM of damaged wafer after CMP. Voids formed and device layer is partially delaminated.

4. Thermal Stress Simulations

Stresses due to thermal expansion are a major area of concern for packaged QMG devices as elevated temperatures are routinely reached during fabrication and assembly. Typical die attach solder reflow temperatures can reach as high as 285 °C. To try to understand this issue, 3-D models of circular via structures were created using SolidWorks. These models consisted of filled and hollow vias with diameters of 10, 25, 50, and 70 µm. The hollow vias had a sidewall/bottom thickness ranging from 1 to 5 µm at 0.2-µm intervals. To reduce computation time, the 3-D model was divided symmetrically into a quarter model and symmetry planes were used as boundary conditions. The models were meshed (Table 1) and simulated using ANSYS Mechanical (finite element analysis). The analysis was steady-state cooling from various thermal conditions the devices could see during fabrication or soldering (200, 250, or 300 °C) to room temperature (25 °C). This gave us a large quantity of data points allowing us to approximate the max stresses and understand where they occur. The vias were also simulated using two different metals: copper (CTE = 16.7 ppm/C at 25 °C) and tungsten (4.3 ppm/C at 25 °C). The surrounding silicon was treated using the orthorhombic model developed by Hopcroft et al.[2] Changes in the CTE of the materials with temperature was also taken into account and the material models are listed in the Appendix.

Table 1 Table of mesh settings used for finite element analysis. Tetrahedral elements were used for all simulations. A mesh refinement = 1 was carried out on the sidewalls of the vias.

	Via diameter (µm)	10	25	50	70
Filled vias	Via element size (µm)	2	2.5	5	5
	Via contact element size (µm)	2.5	2.5	5	5
	Si element size (µm)	25	25	25	25
Hollow vias	Via element size (µm)	2	2	2	5
	Via contact element size (µm)	4	5	5	5
	Si element size (µm)	25	25	30	25

As seen in Fig. 4, the stress in the copper-filled vias exceeded copper's yield strength (~100 MPa) in every simulation. This explains how the delamination of the SOI device layer (Fig. 3) occurred as stress is generated at the bottom corner of the via (Fig. 5a) during copper annealing. The copper expands more than the surrounding silicon, causing cracks to propagate from the vias along the device layer–BOX interface, resulting in the device layer delamination. It is believed that the plastic deformation of the via causes the material to void while cooling. However, copper can still be considered as an option for via fill due to its available processing methods such as directional electroplating—but thermal budgets must be carefully set to prevent destructive yielding of the vias. In fact, copper is used throughout the microelectronics industry for vias and interconnects in advanced packaging processes.[3] Tungsten-filled vias were also investigated in this study because the CTE of tungsten is closer to that of Si (2.6 ppm/C at 25 °C), which will result in lower stresses due to thermal effects. In both solid and hollow via simulations, the maximum stress inside the tungsten via was approximately 3× lower (Fig. 4) than copper and did not exceed tungsten's yield strength (980 MPa).

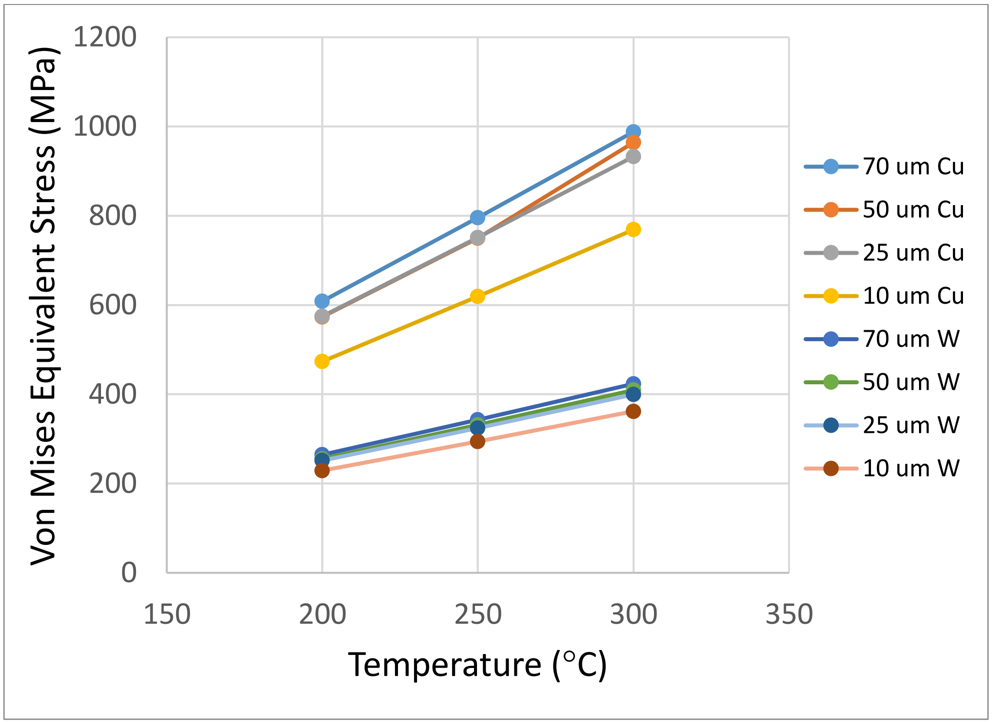

Fig. 4 Simulated maximum stress in the solid via material as a function of temperature

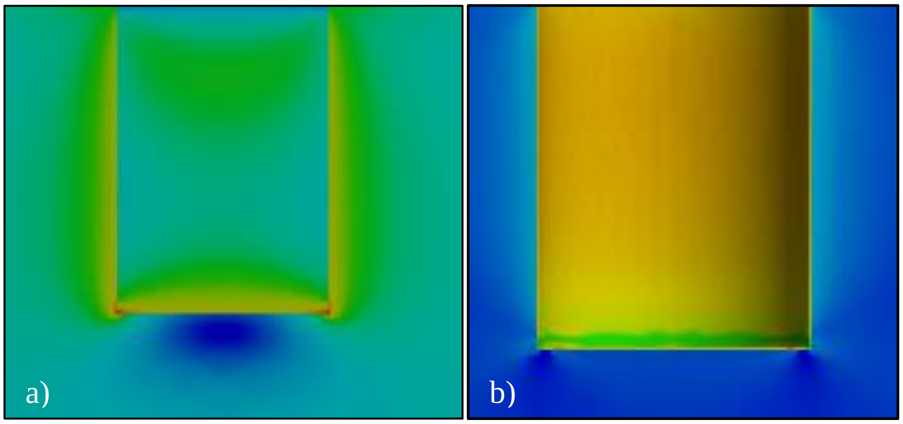

Fig. 5 Cross-sectional image of typical results from ANSYS simulations of (a) solid via and (b) hollow via simulations

Both filled and hollow vias had a positive linear trend for maximum stress within the via as temperature increases, as would be expected. Maximum stress within the hollow copper vias also exceeds the yield strength of copper; however, this simulation does not take into account plastic deformation of the copper in this hollow via simulation. In actuality, the hollow via has space that allows expansion of the copper during plastic deformation at higher temperature anneals, and still might be a viable alternative fabrication process. The hollow vias also returned an interesting trend where the maximum stress decreased as the via wall thickness increased (Fig. 6) but the mechanisms for this trend are unclear at this time.

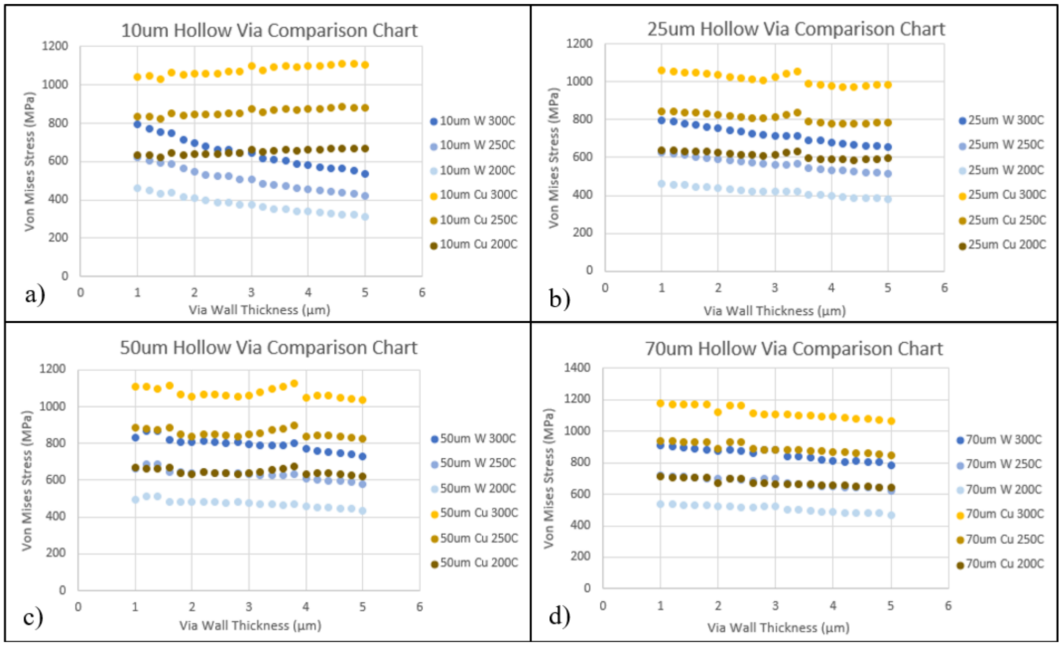

Fig. 6 **ANSYS simulation results for the maximum stress vs. via wall thickness for various via diameters**

5. Conclusion

An experimental microfabrication process for copper TSVs resulted in catastrophic failure of the SOI substrates with the embedded vias. Thermal-mechanical simulations in ANSYS suggest failures are caused by stress generated from the CTE mismatch between the copper and surrounding silicon during a 300 °C anneal. This stress causes cracks and macro-scale delamination in the SOI device layer containing the vias. Simulations show that annealing the copper at a lower temperature might still generate stress to cause failures and the fabrication process development was abandoned. Additional simulations suggest that using another material, such as tungsten, might be a better approach for this type of TSV fabrication.

6. References

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2. Hopcroft MA, Nix WD, Kenny TW. What is the Young's modulus of silicon? J MEMS. 2019;19(2):229–238. doi: 10.1109/JMEMS.2009.2039697.

3. Lau JH, Lee CK, Premachandran CS, Aibin Y**.** Advanced MEMS packaging. McGraw Hill Companies, Inc; 2010. ISBN: 978-0-07-162623-1.

Appendix. Material Properties

Copper:

Density	8933 kg/m^3
Young’s modulus	128 GPa
Poisson’s ratio	0.33
CTE @ temp (C)	α (1/C)
25	1.676E-05
75	1.714E-05
125	1.756E-05
175	1.793E-05
225	1.827E-05
275	1.859E-05
325	1.891E-05

Silicon:

Density	2330 kg/m^3
Young’s modulus	1.65 GPa
Poisson’s ratio	0.1
CTE @ temp (C)	α (1/C)
20	2.57E-06
25	2.63E-06
75	2.97E-06
125	3.24E-06
175	3.44E-06
225	3.6E-06
275	3.73E-06
325	3.84E-06

Tungsten:

Density	19300 kg/m^3
Young’s modulus	400 GPa
Poisson’s ratio	0.28
CTE @ temp (C)	α (1/C)
0	4.3E-06
25	4.3E-06
75	4.4E-06
150	4.5E-06
250	4.6E-06
300	4.7E-06

List of Symbols, Abbreviations, and Acronyms

3-D	3-dimensional
ARL	Army Research Laboratory
BOX	buried oxide
CMP	chemical mechanical polished
CTE	coefficient of thermal expansion
DEVCOM	US Army Combat Capabilities Development Command
DRIE	deep reactive ion etch
QMG	quadrupole mass gyroscope
SEM	scanning electron microscopy
SOI	silicon-on-insulator
TSV	through-silicon via

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