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DEVCOM ARMY RESEARCH LABORATORY

Gallium Nitride (GAN) RF Challenge; BAE Design Testing

by John Penn, Sami Hawasli, Khamsouk Kingkeo, and Ali Darwish

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John Penn, Sami Hawasli, Khamsouk Kingkeo, and Ali Darwish
Sensors and Electron Devices Directorate, DEVCOM Army Research Laboratory

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14. ABSTRACT
The US Department of Defense (DOD) Gallium Nitride (GAN) RF Challenge is enabling development and fabrication of the best concepts for high-performance, efficient, broadband monolithic microwave integrated circuits (MMICs) related to the 5G expansion and to critical electronic warfare needs. The circuits documented in this report represent some of the US Combat Capabilities Development Command Army Research Laboratory designs as part of the DOD Design Team for the BAE Systems 0.18-µm GAN multi-project wafer fabrication. When these fabricated designs are returned in 2021, they will be tested, evaluated, and documented in future technical reports.

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Contents

List of Figures iv

List of Tables vi

Acknowledgments vii

1. Introduction 1

2. Fabricated Die in BAE 0.18-µm GAN 1

3. Broadband Distributed Amplifier (DA) Design 3

4. Compact Broadband Amplifier Designs 6

5. Broadband 6- to 12-GHz and 12- to 24-GHz 2-W Power Amplifiers (PAs) 13

6. Transmit/Receive (TR) Switch 27

7. Ka-Band Mixer 30

8. Frequency Doublers 31

9. Test HEMTs and Calibration Circuits 36

10. Conclusions 41

11. References 42

List of Symbols, Abbreviations, and Acronyms 43

Distribution List 44

List of Figures

Fig. 1 Die photo of CHIP1 9- × 6-mm die (various circuits and test structures)..... 2

Fig. 2 Die photo of CHIP2 9- × 6-mm die (extremely broadband transmitter) 2

Fig. 3 Final layout of MMIC DA #1 (input-gate bottom left, output-drain upper right)..... 3

Fig. 4 S-parameter measurements of MMIC DA #1 (28 V) 4

Fig. 5 S-parameter measurements (solid) vs. simulation (dotted) of MMIC DA #1 (28 V) 4

Fig. 6 Final layout of cascode MMIC DA #2 5

Fig. 7 Measured s-parameters of cascode MMIC DA #2 (10-20V)..... 5

Fig. 8 S-parameter measurements (solid) vs. simulation (dotted) of 4- × 75-µm broadband amplifier (10–20 V)..... 7

Fig. 9 S-parameter measurements (solid) vs. simulation (dotted) of 4- × 120-µm broadband amplifier (10–20 V)..... 8

Fig. 10 S-parameter measurements (solid) vs. simulation (dotted) of 2- × 100-µm broadband amplifier (10–20 V)..... 9

Fig. 11 S-parameter measurements (solid) vs. simulation (dotted) of 2- × 100-µm broadband amplifier (10–20 V)..... 10

Fig. 12 Layout 2- × 100-µm, 2- × 200-µm, and 4- × 75-µm broadband amplifiers 11

Fig. 13 Layout 4- × 120-µm broadband amplifier and cascode 3- to 8-GHz amplifier..... 12

Fig. 14 Measured s-parameters of cascode 3- to 8-GHz amplifier (10–20 V)..... 13

Fig. 15 Layouts of 6- to 12-GHz (left) and 12- to 24-GHz (right) one-stage PA (8 × 83 µm) 14

Fig. 16 S-parameter measurements (solid) vs. simulation (dot) of 6- to 12-GHz PA (20 V)..... 15

Fig. 17 S-parameter measurements (solid) vs. simulation (dot) of 6- to 12-GHz two-stage PA (20 V) 16

Fig. 18 S-parameter measurements (solid) vs. simulation (dot) of 12- to 24-GHz PA (20 V) 17

Fig. 19 S-parameter measurements (solid) vs. simulation (dot) of 12- to 24-GHz two-stage PA (20 V)..... 18

Fig. 20 Performance measurements (solid) vs. simulation (dot) of Pout (blue) and PAE (magenta) for one-stage 6- to 12-GHz PA (24 V)..... 19

Fig. 21 Performance measurements (solid) vs. simulation (dot) of Pout (blue) and PAE (magenta) for one-stage 6- to 12-GHz PA (20V) 20
Fig. 22 Performance measurements (solid) vs. simulation (dot) of Pout (blue) and PAE (magenta) for one-stage 6- to 12-GHz PA (28 V) 21
Fig. 23 Performance measurements (solid) vs. simulation (dot) of Pout (blue) and PAE (magenta) for one-stage 6- to 12-GHz PA (10 V) 22
Fig. 24 Performance measurements (solid) vs. simulation (dot) of Pout (blue) and PAE (magenta) for two-stage 6- to 12-GHz PA (24 V) 23
Fig. 25 Performance measurements (solid) vs. simulation (dot) of Pout (blue) and PAE (magenta) for one-stage 12- to 24-GHz PA (24 V) 24
Fig. 26 Performance measurements (solid) vs. simulation (dot) of Pout (blue) and PAE (magenta) for one-stage 12- to 24-GHz PA (20 V) 25
Fig. 27 Performance measurements (solid) vs. simulation (dot) of Pout (blue) and PAE (magenta) for one-stage 12- to 24-GHz PA (28 V) 26
Fig. 28 Layouts of TR switches 28
Fig. 29 S-parameter measurements (solid) vs. simulation (dot) of single-pull double-throw (SPDT) TR switch 29
Fig. 30 S-parameter measurements (solid) of SPDT TR Switch #2 29
Fig. 31 Layout of diode mixer 30
Fig. 32 Conversion loss of diode mixer vs. LO Pin 31
Fig. 33 Final layout of single-stage 25-GHz 2- × 100-µm frequency doubler 32
Fig. 34 Final layout of fundamental cancelling 25-GHz 2- × 100-µm frequency doubler (with balun) 33
Fig. 35 S-parameter measurements (solid) vs. simulation (dot) of single-stage 25-GHz frequency doubler 33
Fig. 36 Final layout of the 6- to 12-GHz frequency doubler 35
Fig. 37 Final layout of 12- to 24-GHz frequency doubler 35
Fig. 38 EM simulations of open, short, and load (50 Ω) test circuits 37
Fig. 39 S-parameter measurements (solid) vs. simulation (dot) of open, short, and load (50 Ω) 37
Fig. 40 EM simulation of Thru test circuits 38
Fig. 41 S-parameter measurements (solid) vs. simulation (dot) of Thru and 1200-µm line 38
Fig. 42 S-parameter measurements vs. linear simulation of 2- × 50-µm HEMT (Smith chart) 39
Fig. 43 S-parameter measurements vs. linear simulation of 2- × 50-µm HEMT (rectangular plot) 40

Fig. 44 S-parameter measurements vs. linear simulation of 2- × 100-µm HEMT (Smith chart) 40
Fig. 45 S-parameter measurements vs. linear simulation of 2- × 100-µm HEMT (rectangular plot) 41

List of Tables

Table 1 Testing of diode mixer 31
Table 2 Single doubler Pin, doubled Pout, and conversion loss (43–49 GHz) 33
Table 3 Doubler with balun Pin, fundamental Pout, doubled Pout, conversion loss, and isolation (43–47 GHz) 34
Table 4 6- to 12-GHz doubler with input frequency, doubled conversion loss, and isolation 35
Table 5 12- to 24-GHz doubler with Pin, fundamental Pout, doubled Pout, conversion loss, and isolation (24 GHz) 36

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1. Introduction

The Gallium Nitride (GAN) RF Challenge is a US Department of Defense (DOD) program to develop critical technology, with a first phase focused on addressing two major areas in wireless communication needs. First, due to the emerging and evolving 5G wireless networks, DOD systems will have to operate in increasingly crowded and contested RF environments. Second, electronic warfare (EW) is a rapidly developing and changing arena critical to DOD applications and users. Winners of the first phase of the GAN RF Challenge focused on concepts for high-performance, efficient, broadband monolithic microwave integrated circuits (MMICs) related to the 5G expansion, and to critical EW needs. There was also design space and fabrication of DOD designs, where the US Army Combat Capabilities Development Command Army Research Laboratory was one of the design teams. This technical report describes the testing and analysis of the DEVCOM Army Research Laboratory design submissions for the BAE Systems fabrication from the first phase of the GAN RF Challenge.

2. Fabricated Die in BAE 0.18-µm GAN

The DEVCOM ARL design team of Ali Darwish, Sami Hawasli, and John Penn proposed an extremely broadband transmitter architecture that won acceptance for the GAN RF Challenge. Figure 1 shows a picture of the CHIP1 die, which includes a number of smaller designs, some of which make up the larger broadband transmitter. Figure 2 shows a picture of the CHIP2 die, the full broadband transmitter design.

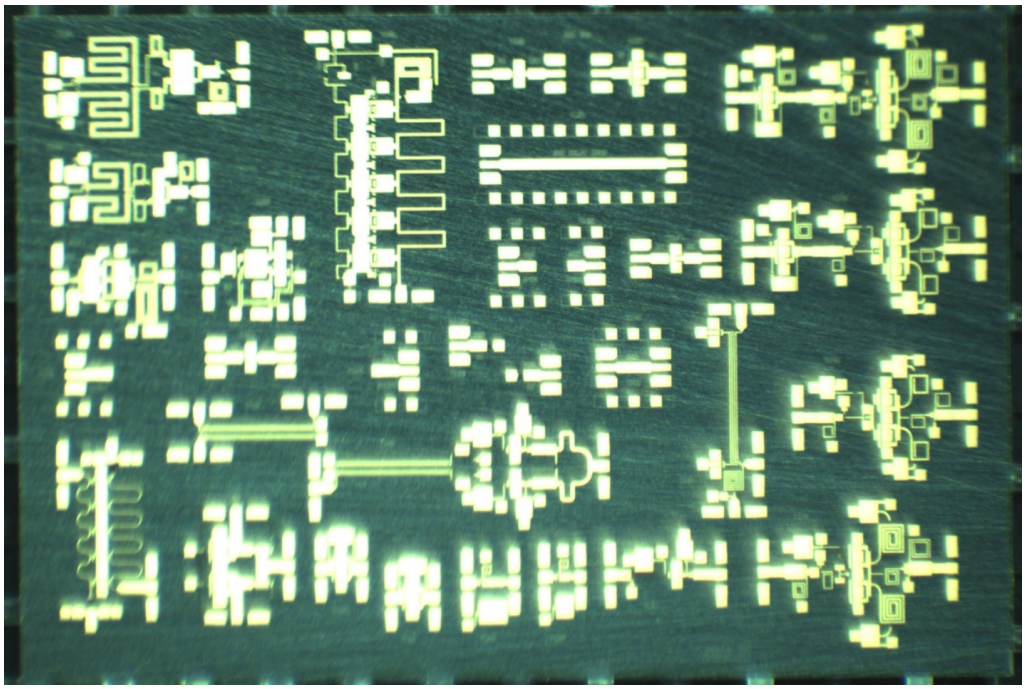

Fig. 1 Die photo of CHIP1 9- × 6-mm die (various circuits and test structures)

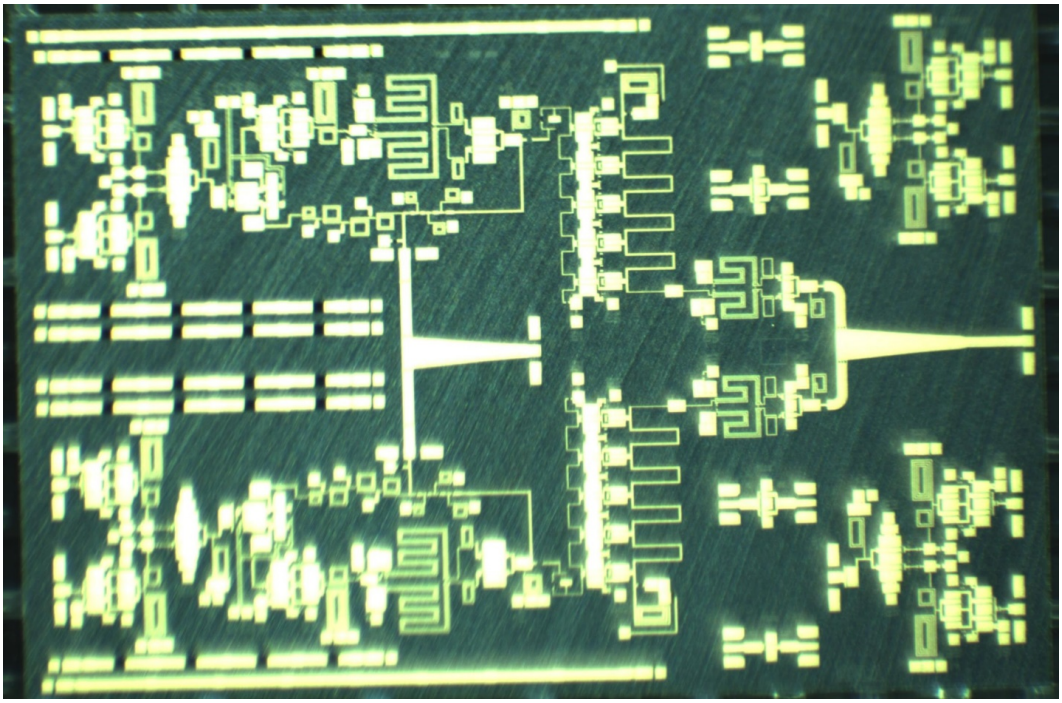

Fig. 2 Die photo of CHIP2 9- × 6-mm die (extremely broadband transmitter)

3. Broadband Distributed Amplifier (DA) Design

Broadband amplifiers were needed for the novel transmitter architecture. Distributed amplifiers can achieve decades of bandwidth, and a couple of design approaches were included in this fabrication. Figure 3 shows a plot of a common source DA. Small signal measurements of the DA show good gain before rolling off above 40 GHz (Fig. 4). Simulations of the broadband amplifier compare well with actual measurements at 28 V (Fig. 5), though at low voltages (10–20 V) the amplifier exhibited some potential high-frequency stability issues (>40 GHz). Another DA in a cascode arrangement showed good broadband gain from below 4 GHz to above 20 GHz. Some marginal high-frequency stability issues (~26 GHz) started to appear at higher bias voltages and currents. Figure 6 shows a plot of the cascode DA and its measured s-parameters from 10- to 20-V biases are shown in Fig. 7.

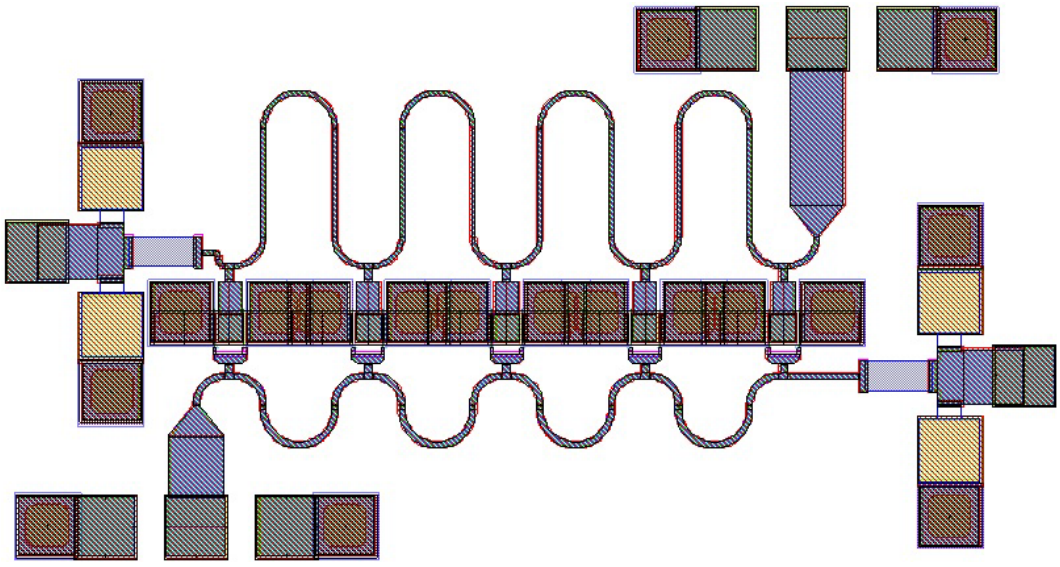

Fig. 3 Final layout of MMIC DA #1 (input-gate bottom left, output-drain upper right)

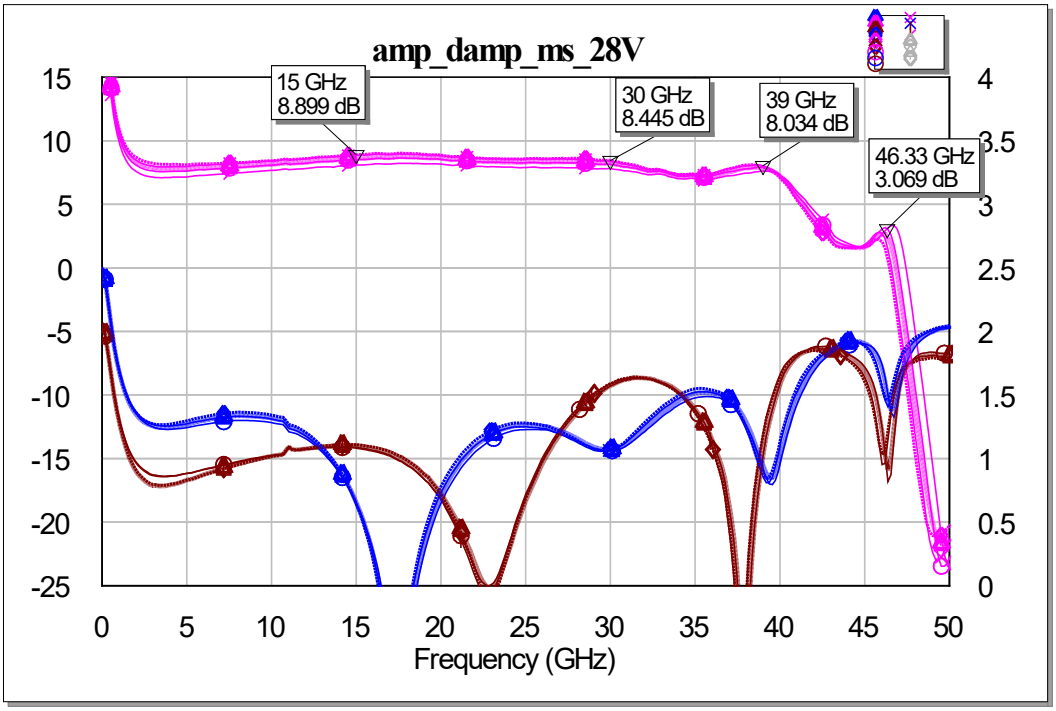

Fig. 4 S-parameter measurements of MMIC DA #1 (28 V)

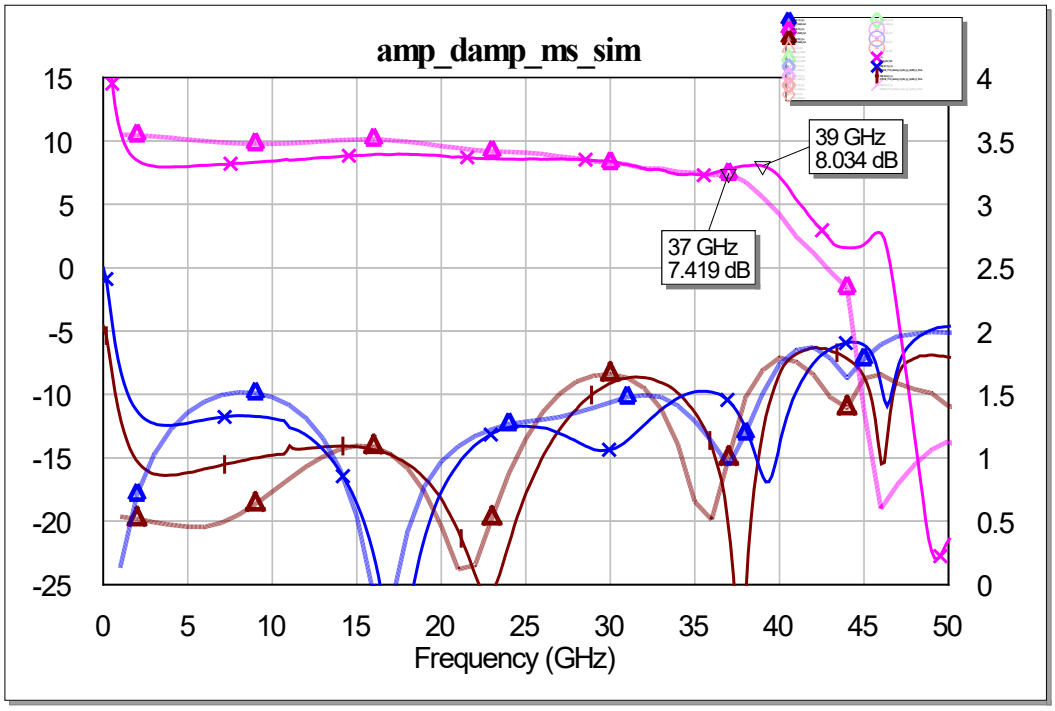

Fig. 5 S-parameter measurements (solid) vs. simulation (dotted) of MMIC DA #1 (28 V)

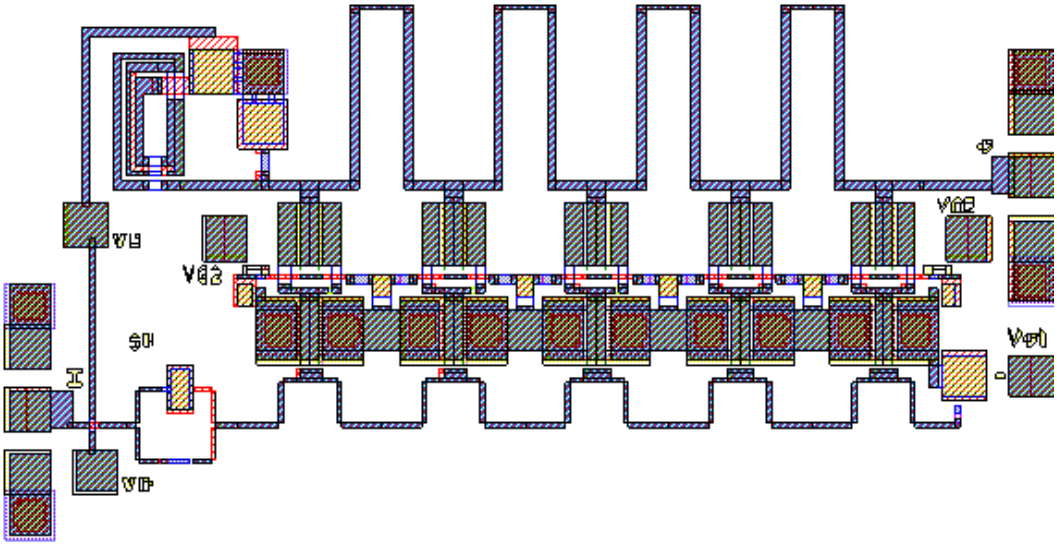

Fig. 6 Final layout of cascode MMIC DA #2

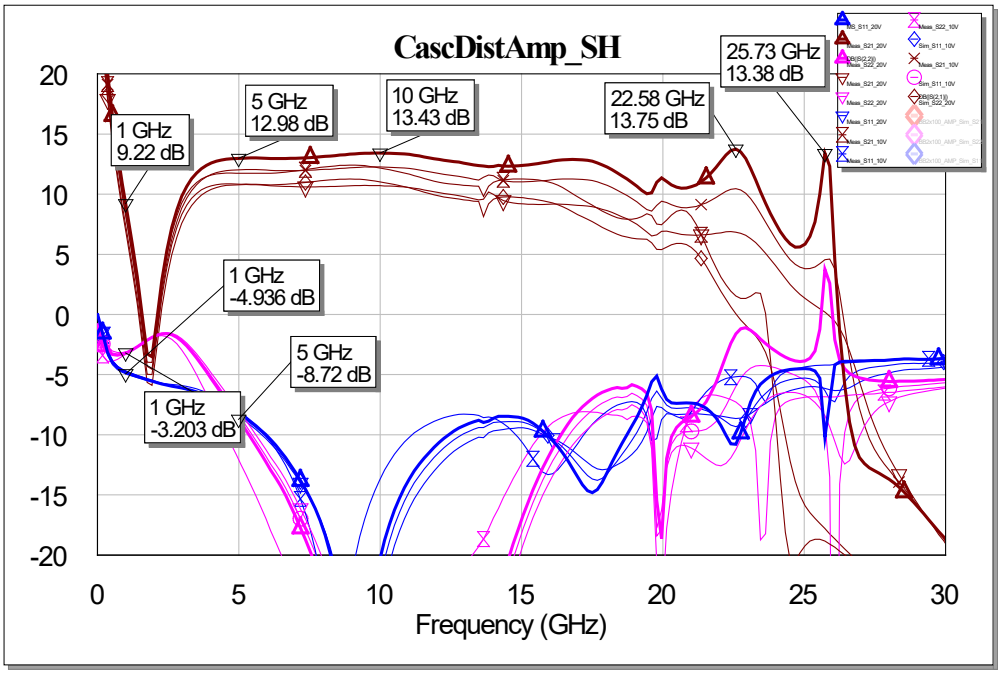

Fig. 7 Measured s-parameters of cascode MMIC DA #2 (10-20V)

4. Compact Broadband Amplifier Designs

Several very broadband, very compact, feedback amplifier designs were fabricated and tested. Two designs used resistive feedback with two different sized high-electron-mobility transistors (HEMTs), while two more used source feedback with two different sized HEMTs. Figure 8 shows measured (solid) versus simulated (dotted) s-parameters of the 4- × 75-µm HEMT broadband amplifier with 10- and 20-V biases at 30- and 60-mA biases (100–200 mA/mm). A slightly larger 4- × 120-µm HEMT broadband amplifier at similar 10- to 20-V biases shows measured (solid) versus simulated (dotted) s-parameters in Fig. 9. For the source feedback amplifier, Fig. 10 shows measured (solid) versus simulated (dotted) s-parameters of the 2- × 100-µm HEMT broadband amplifier with 10- to 20-V biases at 20- and 40-mA biases (100–200 mA/mm). A larger 2- × 200-µm HEMT broadband amplifier at similar 10- to 20-V biases shows measured (solid) versus simulated (dotted) s-parameters in Fig. 11. Generally, the larger HEMT designs have higher gain at lower frequencies, but gain drops off more at higher frequencies relative to the smaller HEMTs. The return loss of the resistive feedback designs tends to be better at lower frequencies, while the source feedback designs have poor return loss at lower frequencies, which improves at higher frequencies. Layouts of these four broadband amplifiers and another 3- to 8-GHz cascode broadband amplifier are shown in Figs. 12 and 13. Small-signal s-parameter measurements of the 3- to 8-GHz cascode amplifier are shown in Fig. 14. It has very good gain but the return loss is low.

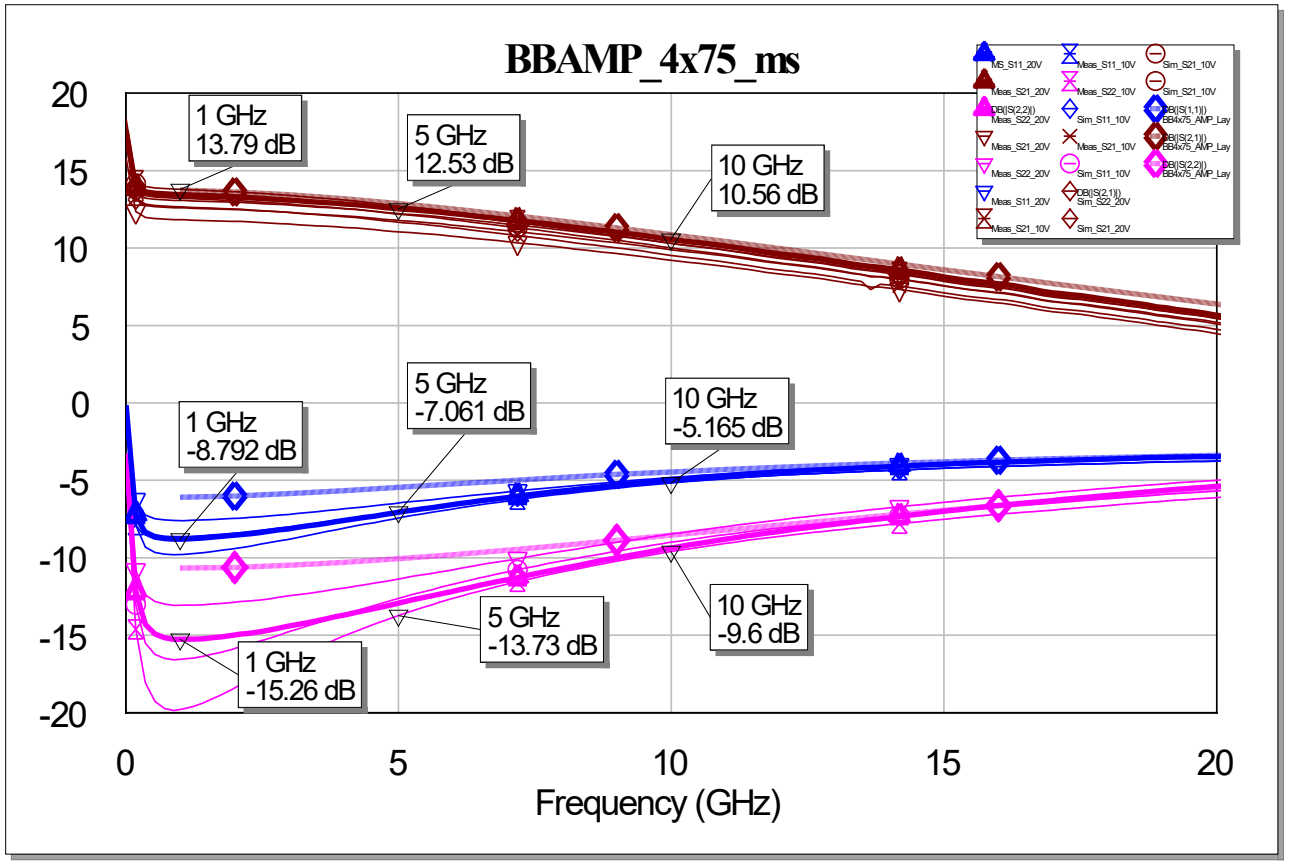

Fig. 8 S-parameter measurements (solid) vs. simulation (dotted) of 4- × 75-µm broadband amplifier (10–20 V)

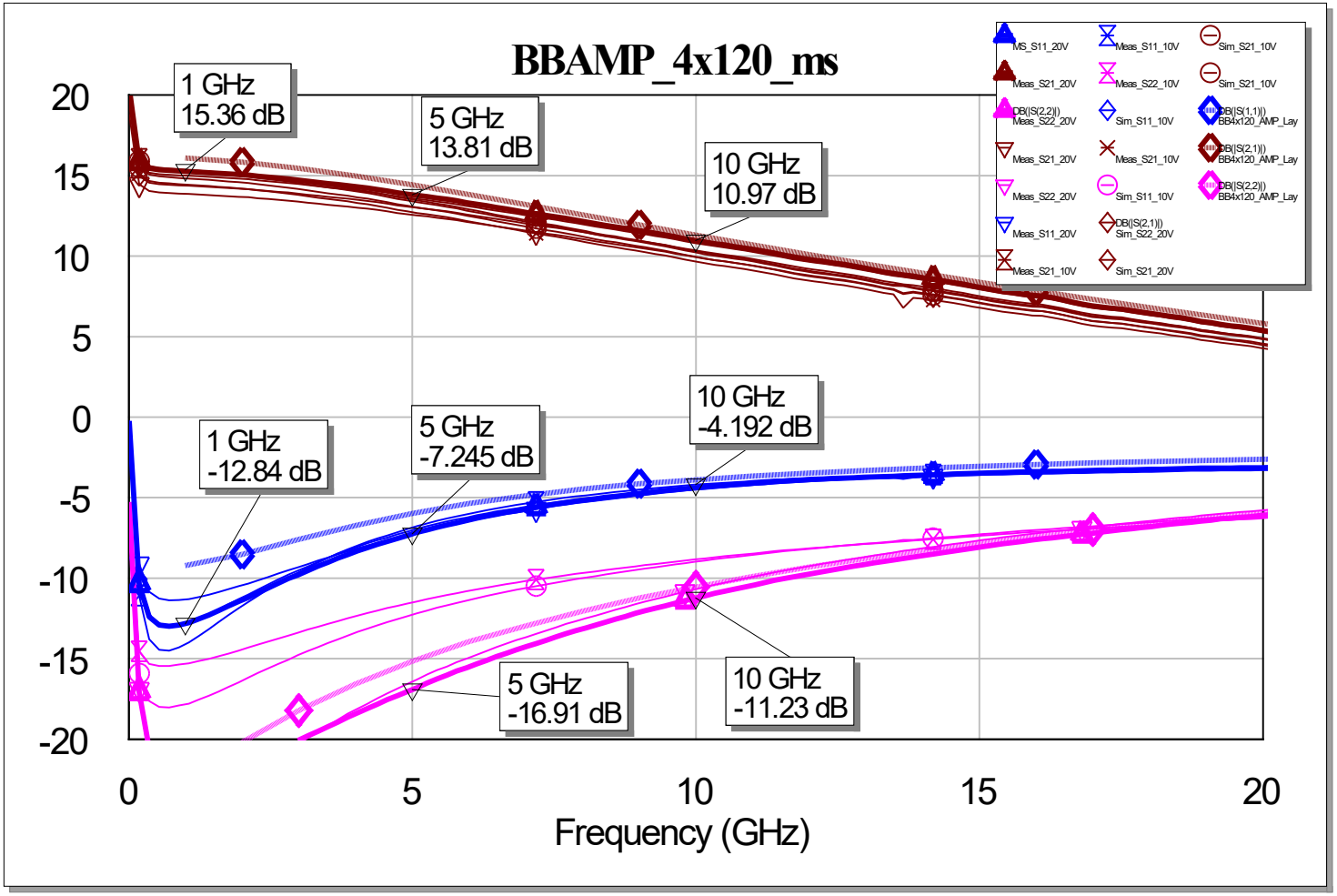

Fig. 9 S-parameter measurements (solid) vs. simulation (dotted) of 4- × 120-µm broadband amplifier (10–20 V)

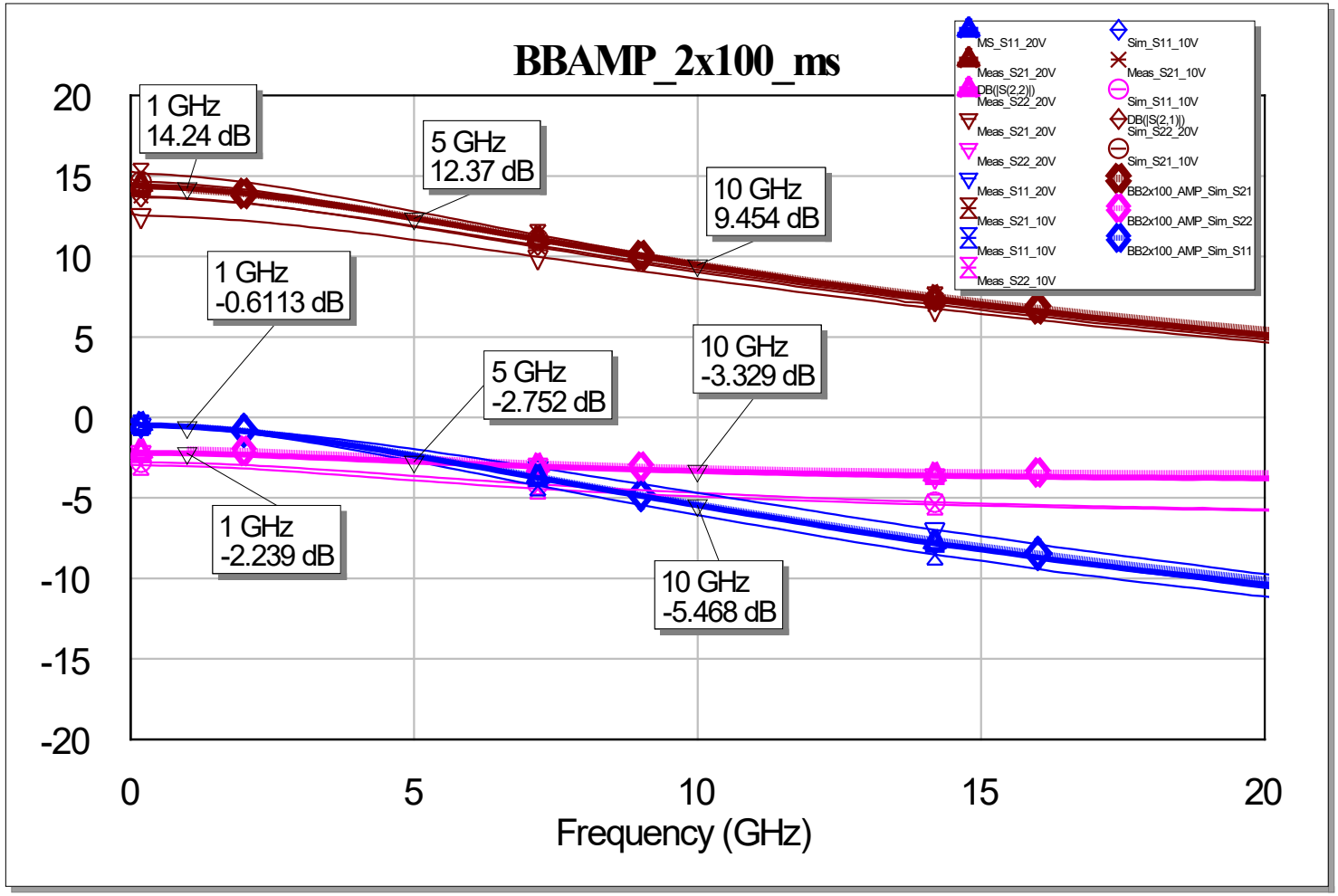

Fig. 10 S-parameter measurements (solid) vs. simulation (dotted) of 2- × 100-µm broadband amplifier (10–20 V)

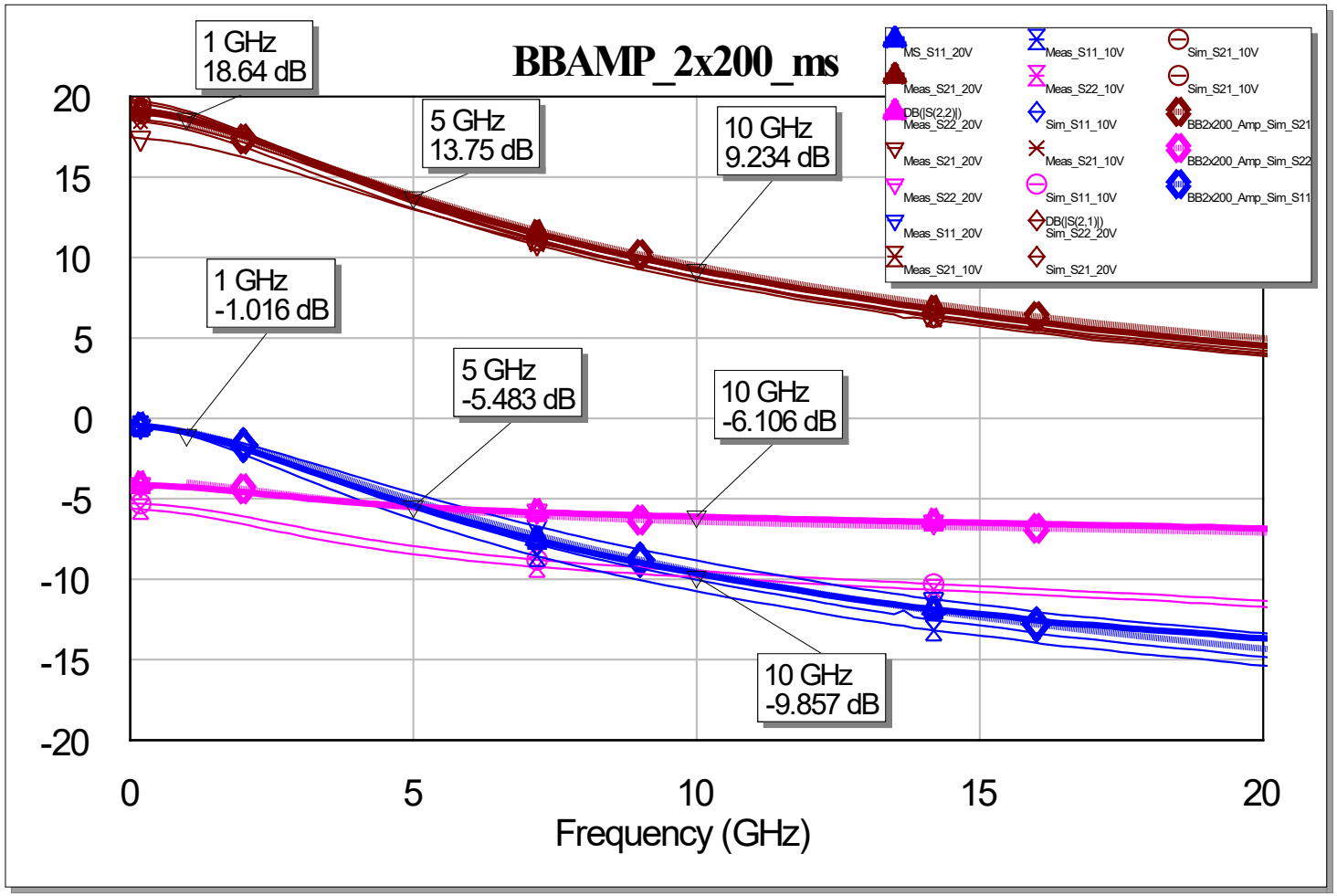

Fig. 11 S-parameter measurements (solid) vs. simulation (dotted) of 2- × 100-µm broadband amplifier (10–20 V)

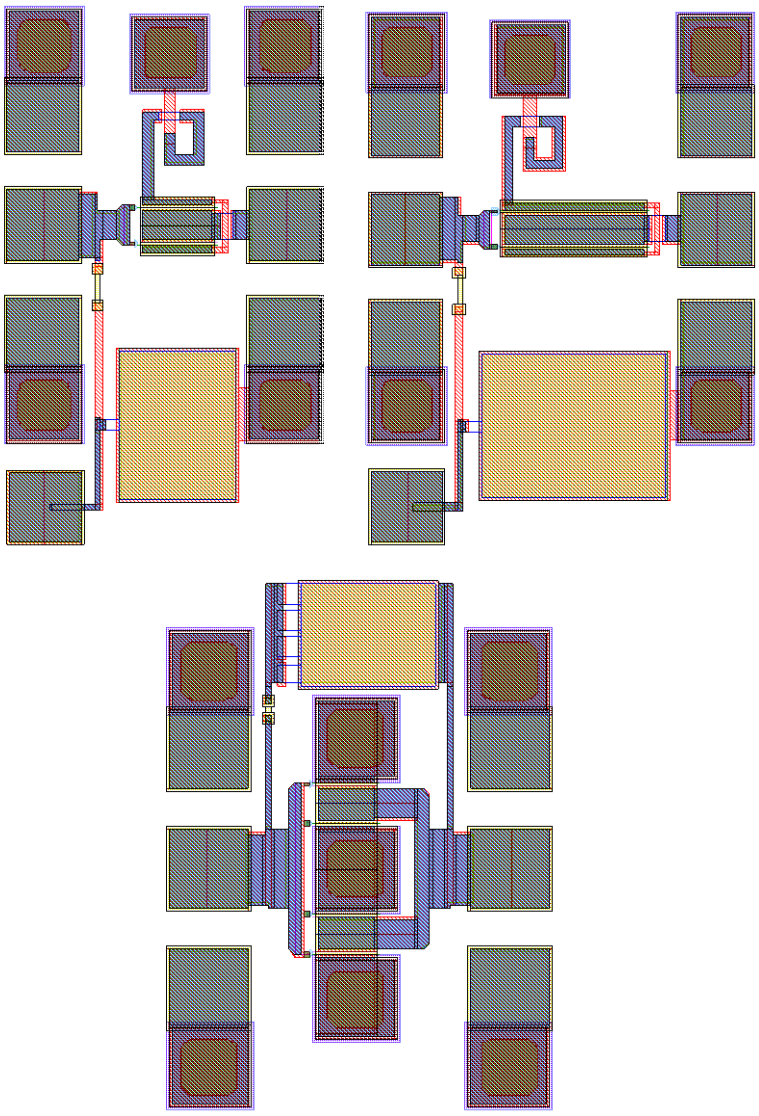

Fig. 12 Layout 2- × 100-µm, 2- × 200-µm, and 4- × 75-µm broadband amplifiers

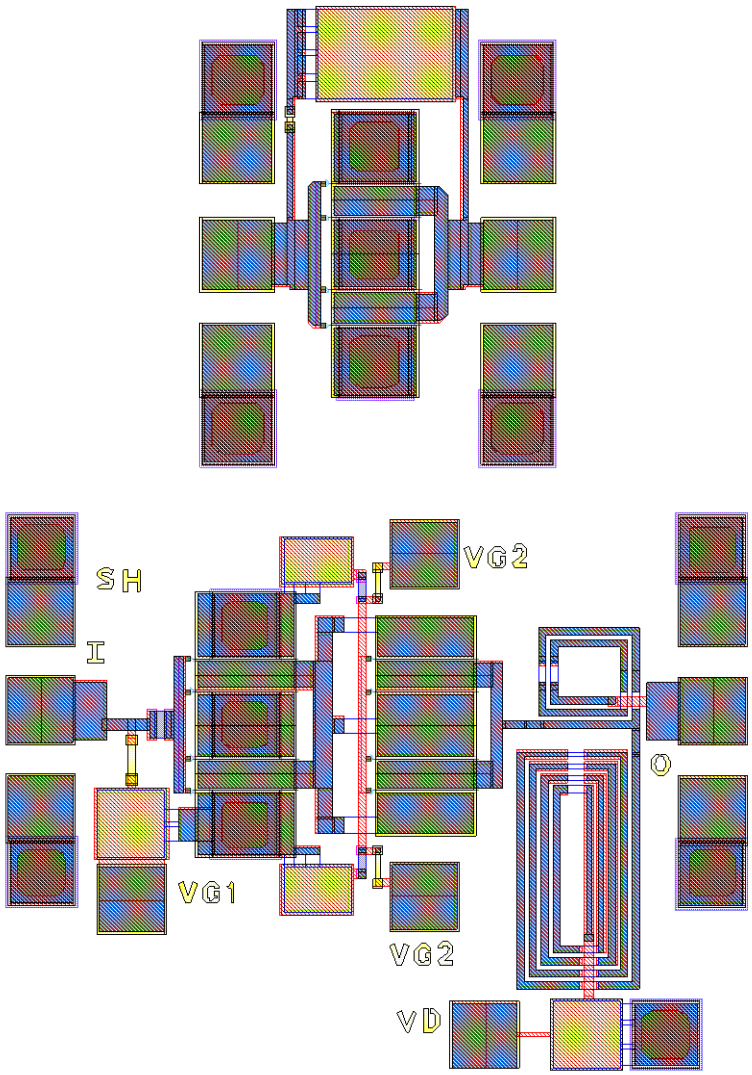

Fig. 13 Layout 4- × 120-µm broadband amplifier and cascode 3- to 8-GHz amplifier

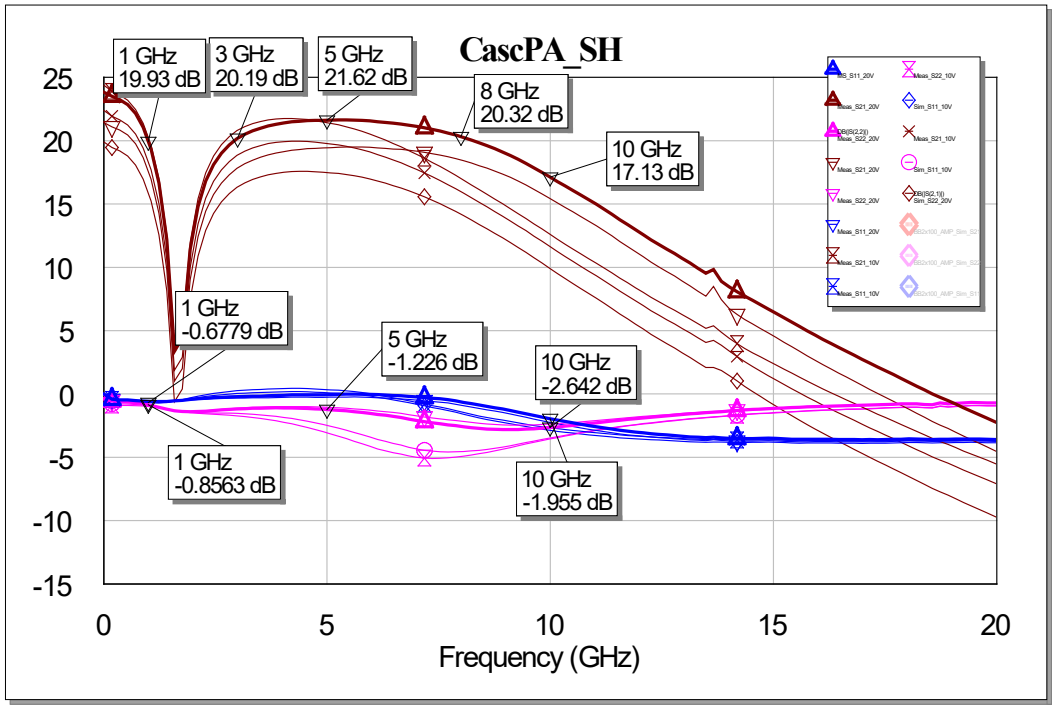

Fig. 14 Measured s-parameters of cascode 3- to 8-GHz amplifier (10–20 V)

5. Broadband 6- to 12-GHz and 12- to 24-GHz 2-W Power Amplifiers (PAs)

Power amplifiers (PAs) with at least an octave bandwidth were desired, targeting 6- to 12-GHz and 12- to 24-GHz operation with 2 W of output power. A two-stage version was created based on the prior 4- × 75-µm feedback amplifier as the first-stage driver to an 8- × 83-µm output stage. Gain of the driver stage is falling off dramatically for the 12- to 24-GHz two-stage amplifier, but there was not sufficient time to design a higher frequency driver. Small signal results matched very well to measurements for all four versions of the PA, where Axiem electromagnetic (EM) simulation was performed on the final layouts for best comparisons. Figure 15 shows the layouts of the one-stage 6- to 12-GHz and 12- to 24-GHz PAs. Simulations compare very well to measurements, with dotted lines for simulations and solid lines for measurements. Figures 16–19 show measured versus simulated s-parameters for the one- and two-stage 6- to 12-GHz PAs, and one- and two-stage 12- to 24-GHz PAs. Small-signal measurements were taken at 10, 20, 24, and 28 V with similar performance. For the small signal plots, 20 V was the bias used for comparison with the models. Large-signal measurements were also taken at 20, 24, 28, and sometimes 10 V. The amplifiers were designed for 20- to 24-V operation because it was not clear if 28 V was within operating limits; still, measurements were taken at 28 and 10 V for comparison with the model outside of its optimal fit.

Many frequencies in the band of operation were measured but only some are plotted as representative. At 6 GHZ and 24 V for the one-stage PA, Fig. 20 shows the measured output power (Pout) and power-added efficiency (PAE) as solid lines versus simulations as dotted lines with input power (Pin) as the x-axis. Note the 2-W (33-dBm) power achieved with a good efficiency of almost 30% by the broadband amplifier. With higher voltages, more Pout could be achieved, while at lower voltages, generally efficiency could improve. A similar power plot at 6 GHZ, but at 20 V for the one-stage PA (Fig. 21), shows the measured Pout and PAE as solid lines versus simulations as dotted lines with Pin as the x-axis. Pout drops by a little more than 1 dB, but efficiency improves to a peak of 32% PAE. Similarly for 28 V in Fig. 22, Pout increases about 1 dB to 34 dBm, while efficiency drops to 28% peak PAE. As expected for the lower 10-V bias (Fig. 23), output power drops and efficiency increases. Note how well the simulations match the measured results at the lower voltage.

For the two-stage amplifier, it is important that the driver stage generates sufficient Pout so that only the final stage is compressing. The simple broadband feedback driver stage was designed more for gain than optimal power performance, so it was expected that it might compress at higher voltages of 24 or 28 V. Measurements at 20, 24, 28, and some 10 V were taken at various frequencies for the two-stage PA. A typical plot is shown in Fig. 24 at 24 V showing 2 W of Pout (33 dBm) and decent PAE of 22% for the two-stage PA.

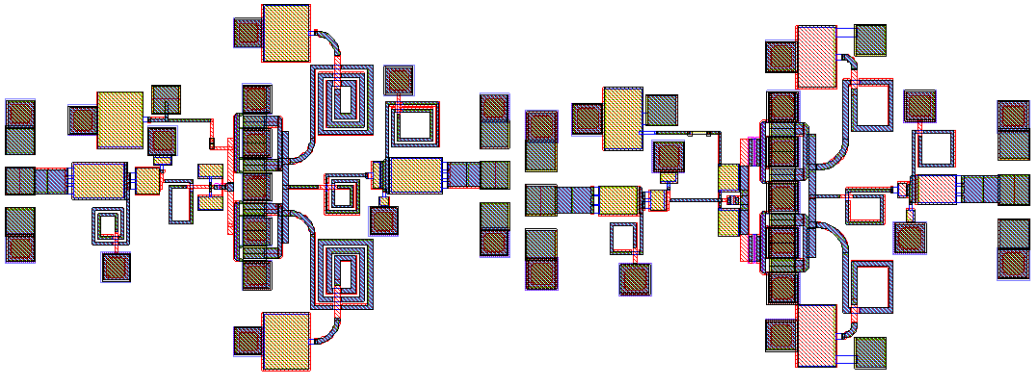

Fig. 15 Layouts of 6- to 12-GHz (left) and 12- to 24-GHz (right) one-stage PA (8 × 83 µm)

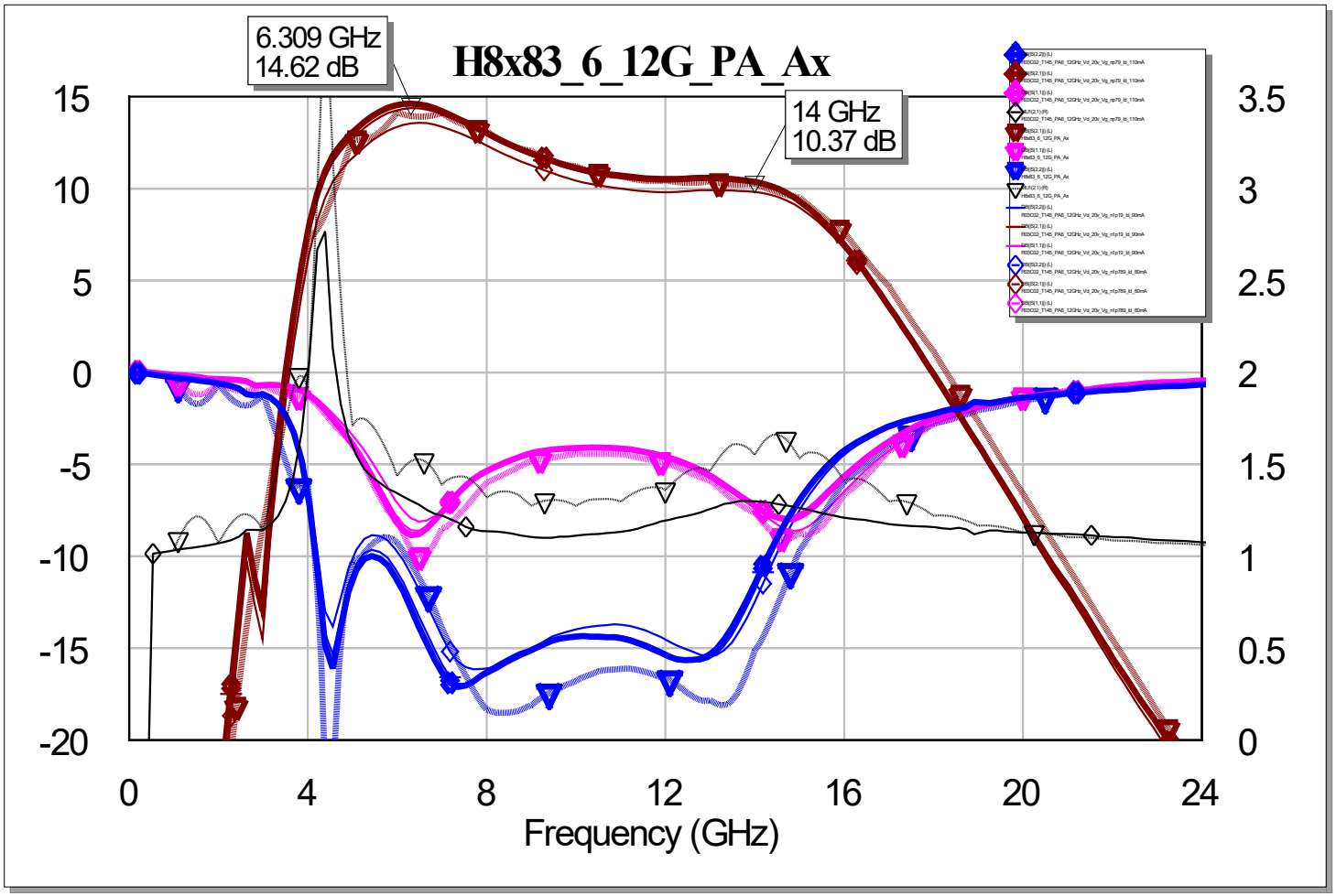

Fig. 16 S-parameter measurements (solid) vs. simulation (dot) of 6- to 12-GHz PA (20 V)

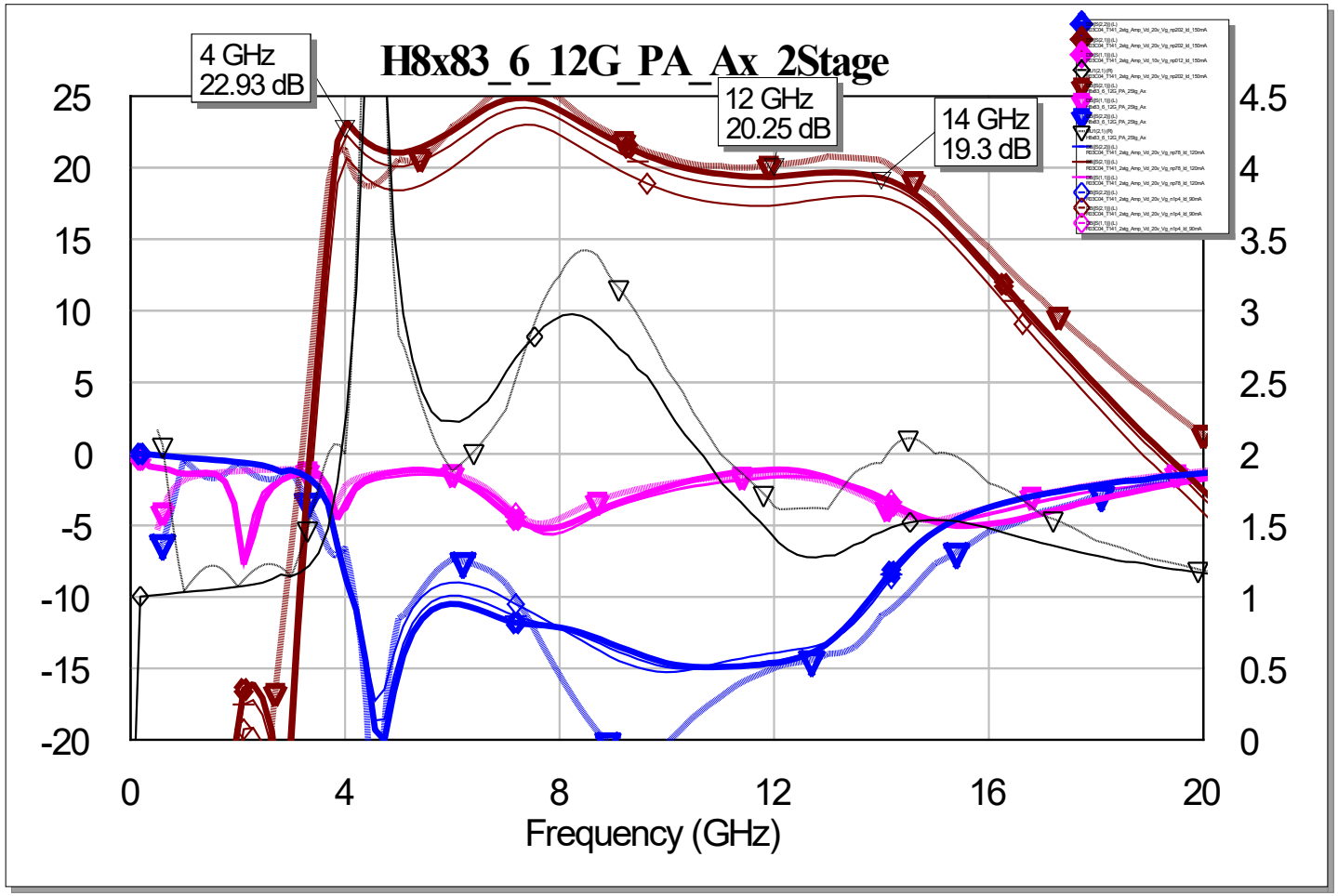

Fig. 17 S-parameter measurements (solid) vs. simulation (dot) of 6- to 12-GHz two-stage PA (20 V)

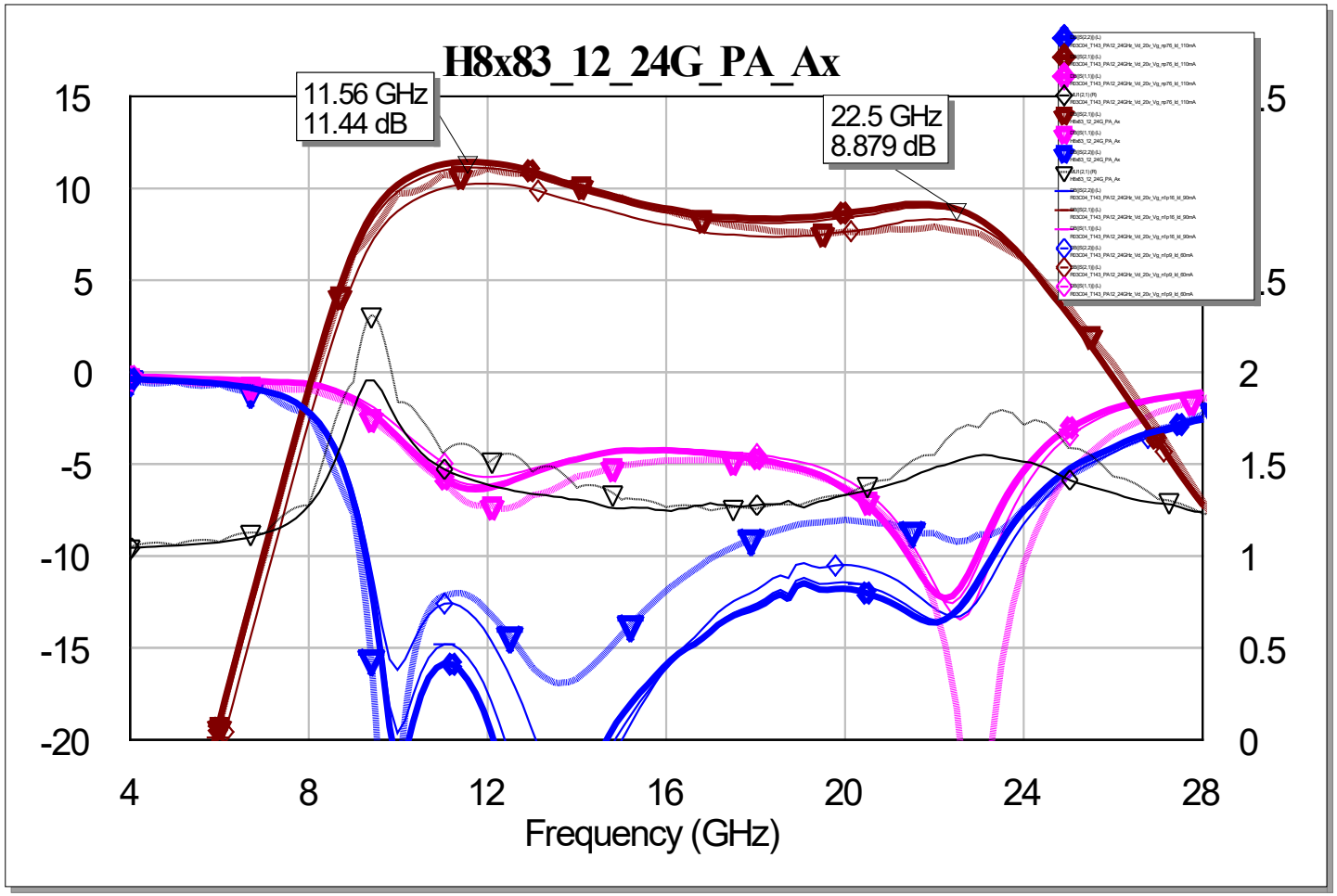

Fig. 18 S-parameter measurements (solid) vs. simulation (dot) of 12- to 24-GHz PA (20 V)

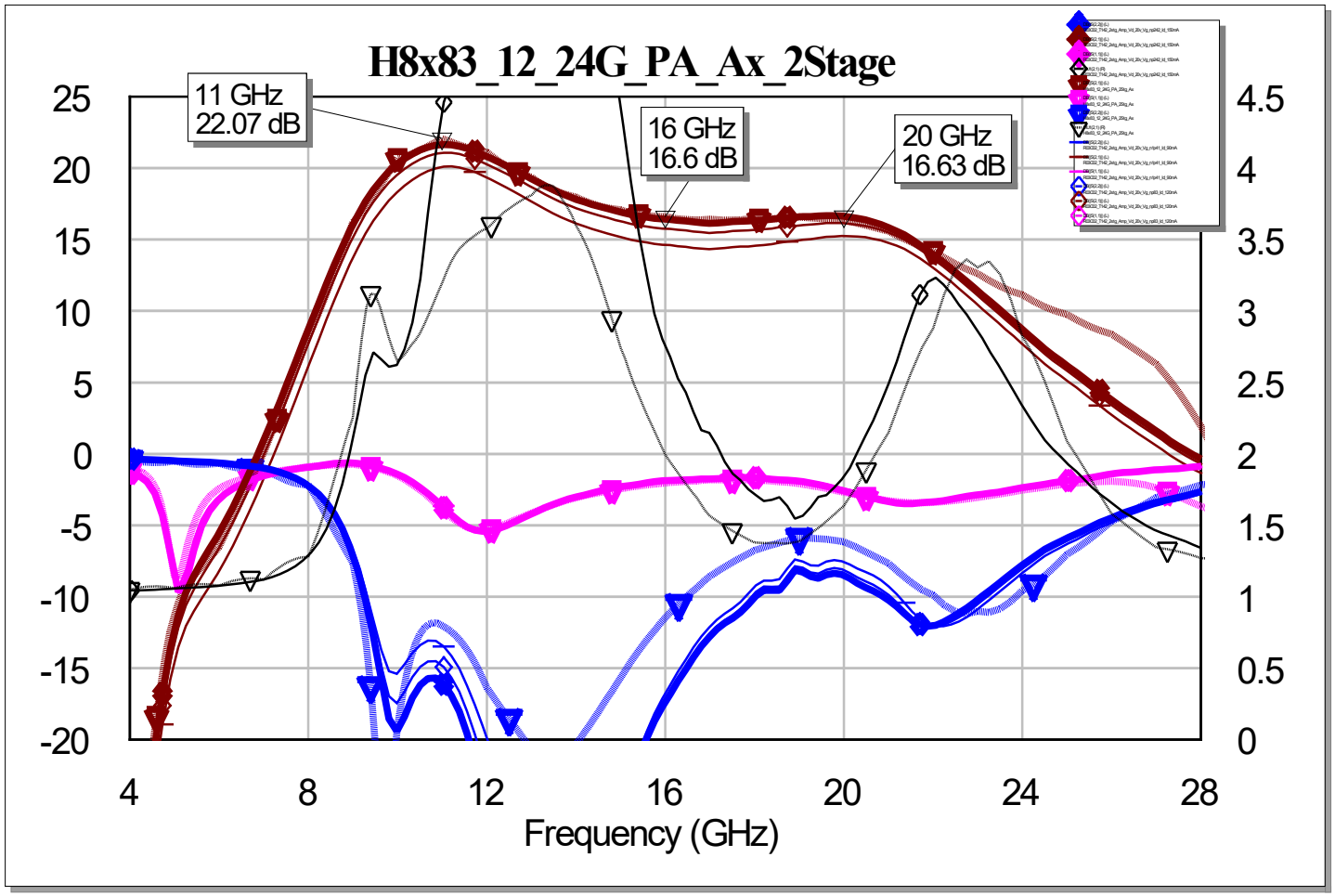

Fig. 19 S-parameter measurements (solid) vs. simulation (dot) of 12- to 24-GHz two-stage PA (20 V)

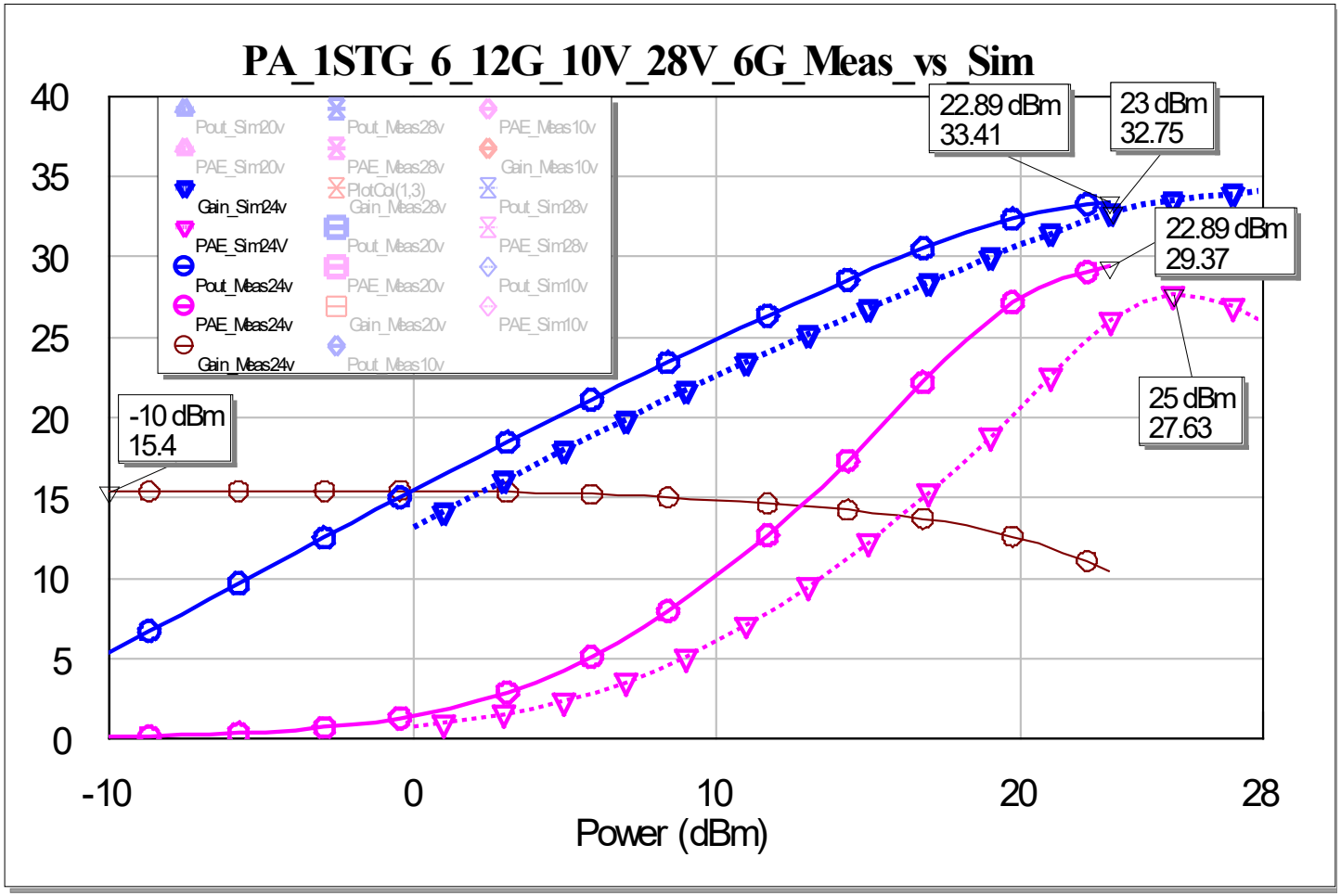

Fig. 20 Performance measurements (solid) vs. simulation (dot) of Pout (blue) and PAE (magenta) for one-stage 6- to 12-GHz PA (24 V)

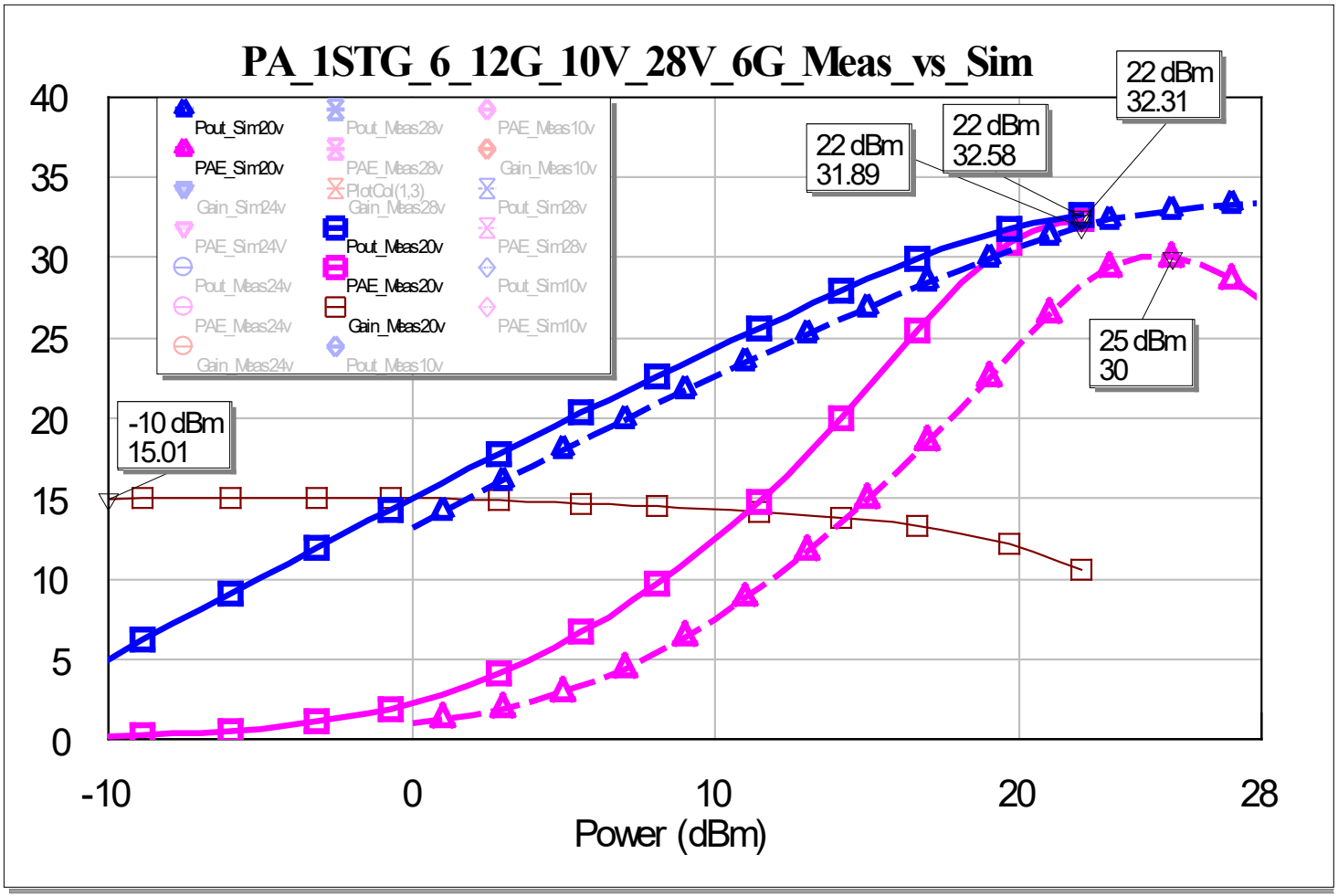

Fig. 21 Performance measurements (solid) vs. simulation (dot) of Pout (blue) and PAE (magenta) for one-stage 6- to 12-GHz PA (20V)

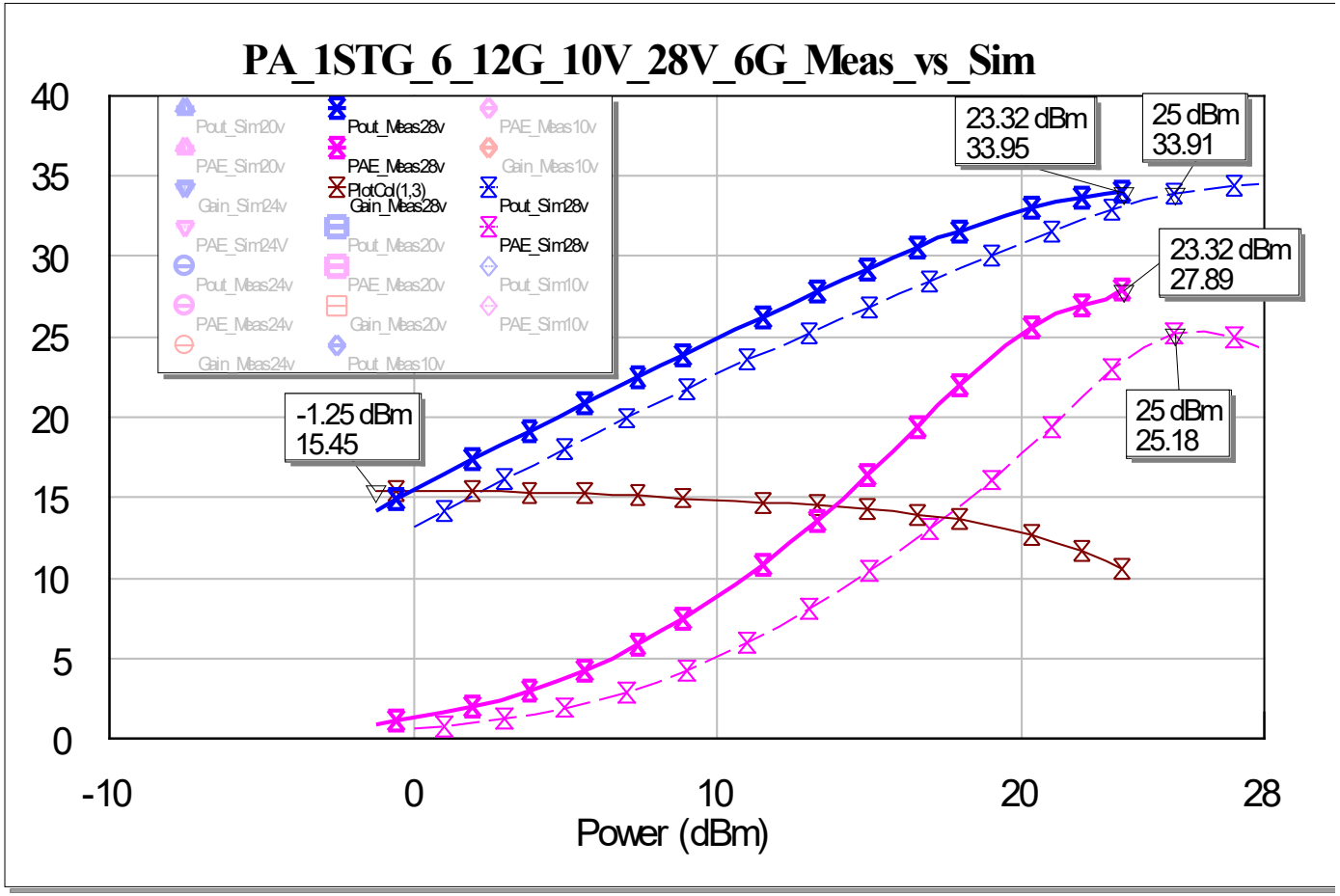

Fig. 22 Performance measurements (solid) vs. simulation (dot) of Pout (blue) and PAE (magenta) for one-stage 6- to 12-GHz PA (28 V)

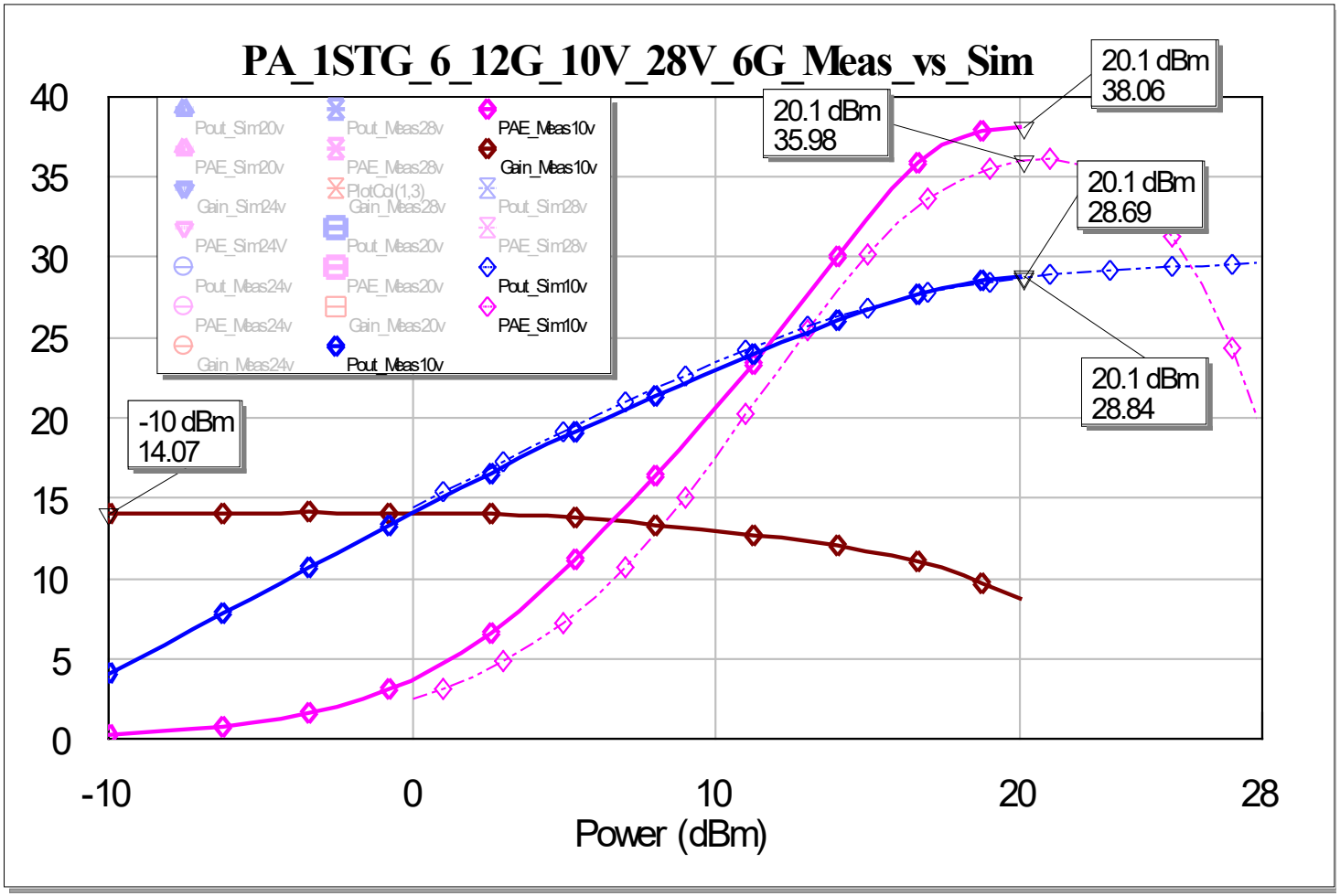

Fig. 23 Performance measurements (solid) vs. simulation (dot) of Pout (blue) and PAE (magenta) for one-stage 6- to 12-GHz PA (10 V)

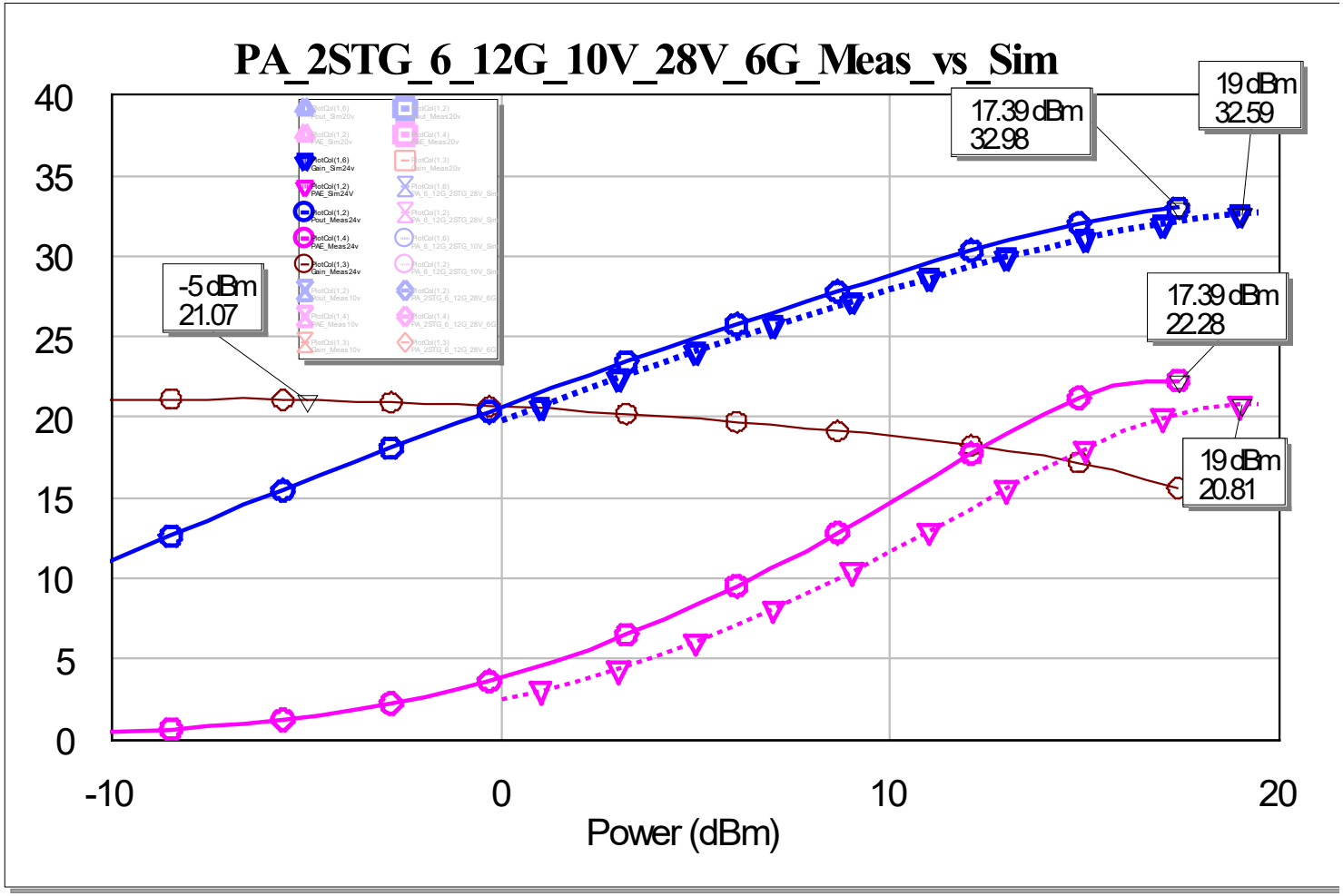

Fig. 24 Performance measurements (solid) vs. simulation (dot) of Pout (blue) and PAE (magenta) for two-stage 6- to 12-GHz PA (24 V)

Power performance measurements for the 12- to 24-GHz amplifier were taken from 11–18 GHz at 20, 24, and 28 V. At 15 GHZ and 24 V for the one-stage PA, Fig. 25 shows the measured Pout and PAE as solid lines versus simulations as dotted lines with Pin as the x-axis. Note the 2-W power is almost achieved, but the efficiency is lower than predicated for the broadband amplifier. With higher voltages, more Pout could be achieved and at lower voltages, generally, efficiency could improve. A similar power plot at 15 GHZ and 20 V for the one-stage PA, Fig. 26 shows the measured Pout and PAE as solid lines versus simulations as dotted lines with Pin as the x-axis. Output power drops very slightly with a very slight efficiency increase. Similarly for 28 V in Fig. 27, Pout increases very slightly and efficiency drops slightly. Power measurements were also taken of the two-stage 12- to 24-GHz PA, but the driver stage is likely compressing causing lower power and PAE performance. A better driver stage would be desired for this higher frequency multi-stage PA.

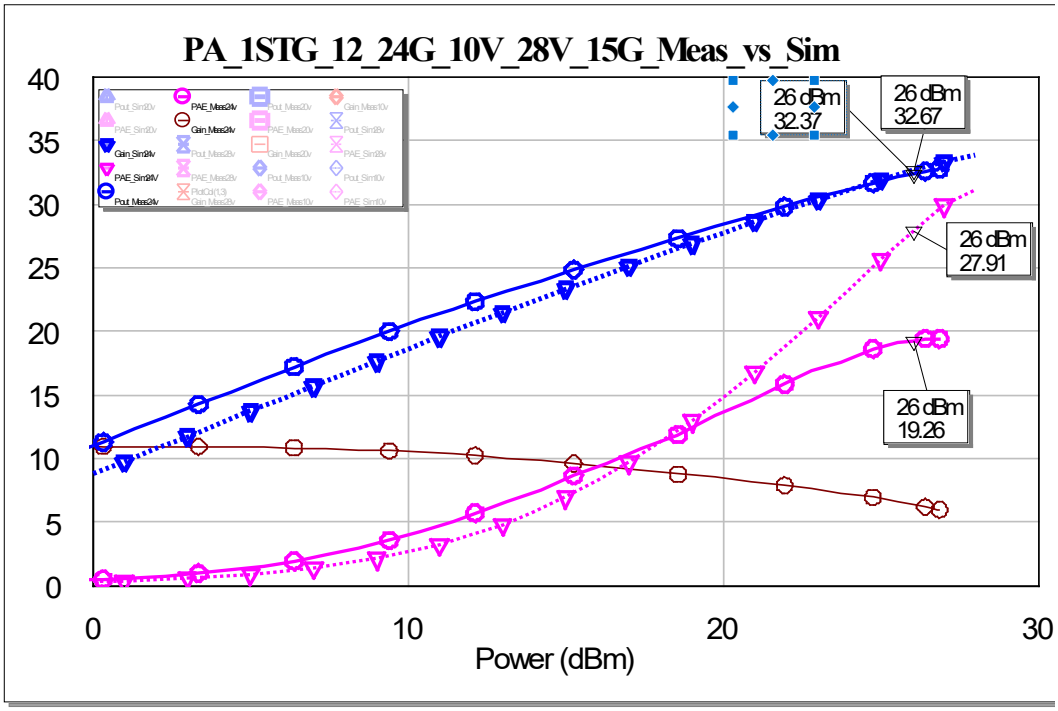

Fig. 25 Performance measurements (solid) vs. simulation (dot) of Pout (blue) and PAE (magenta) for one-stage 12- to 24-GHz PA (24 V)

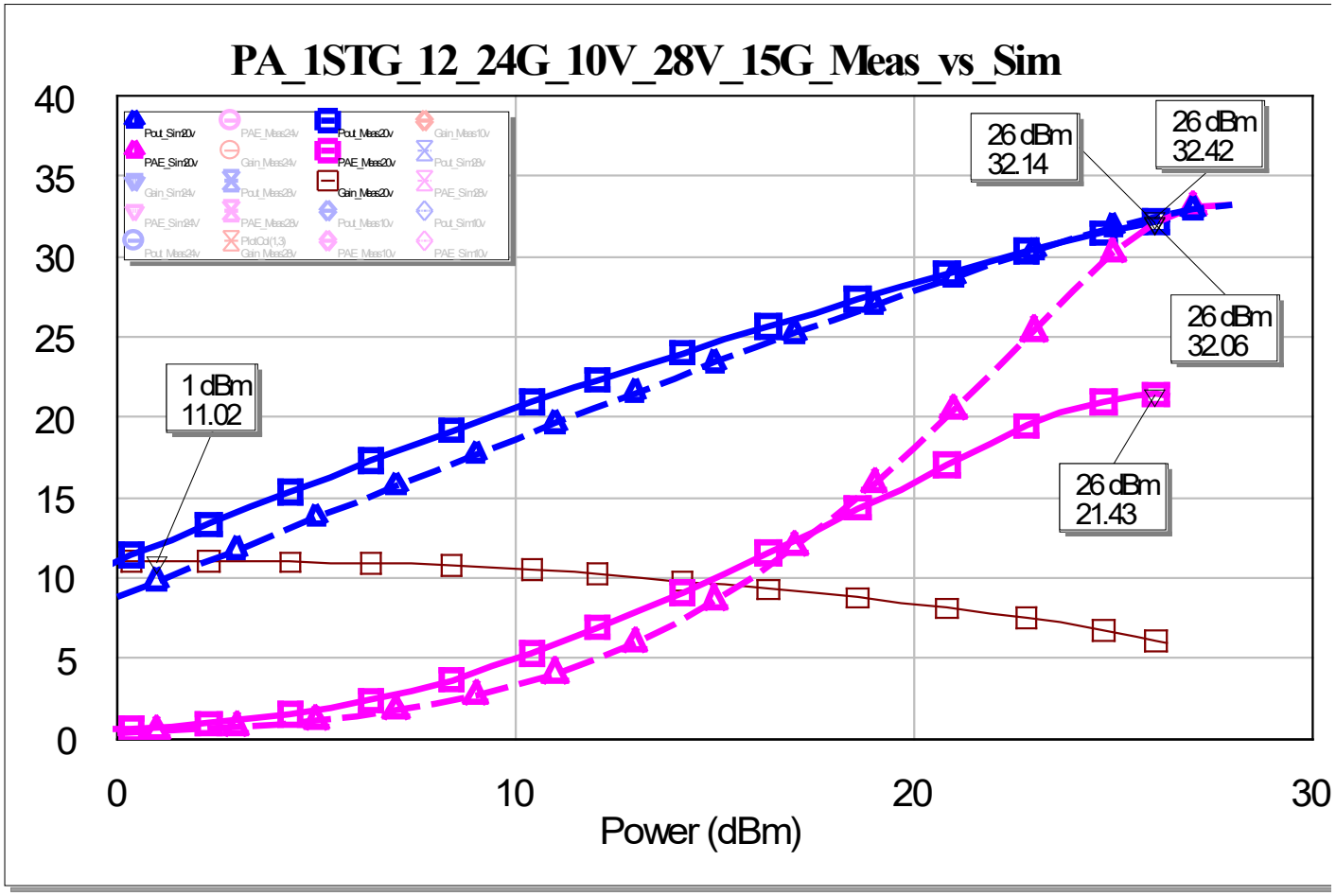

Fig. 26 Performance measurements (solid) vs. simulation (dot) of Pout (blue) and PAE (magenta) for one-stage 12- to 24-GHz PA (20 V)

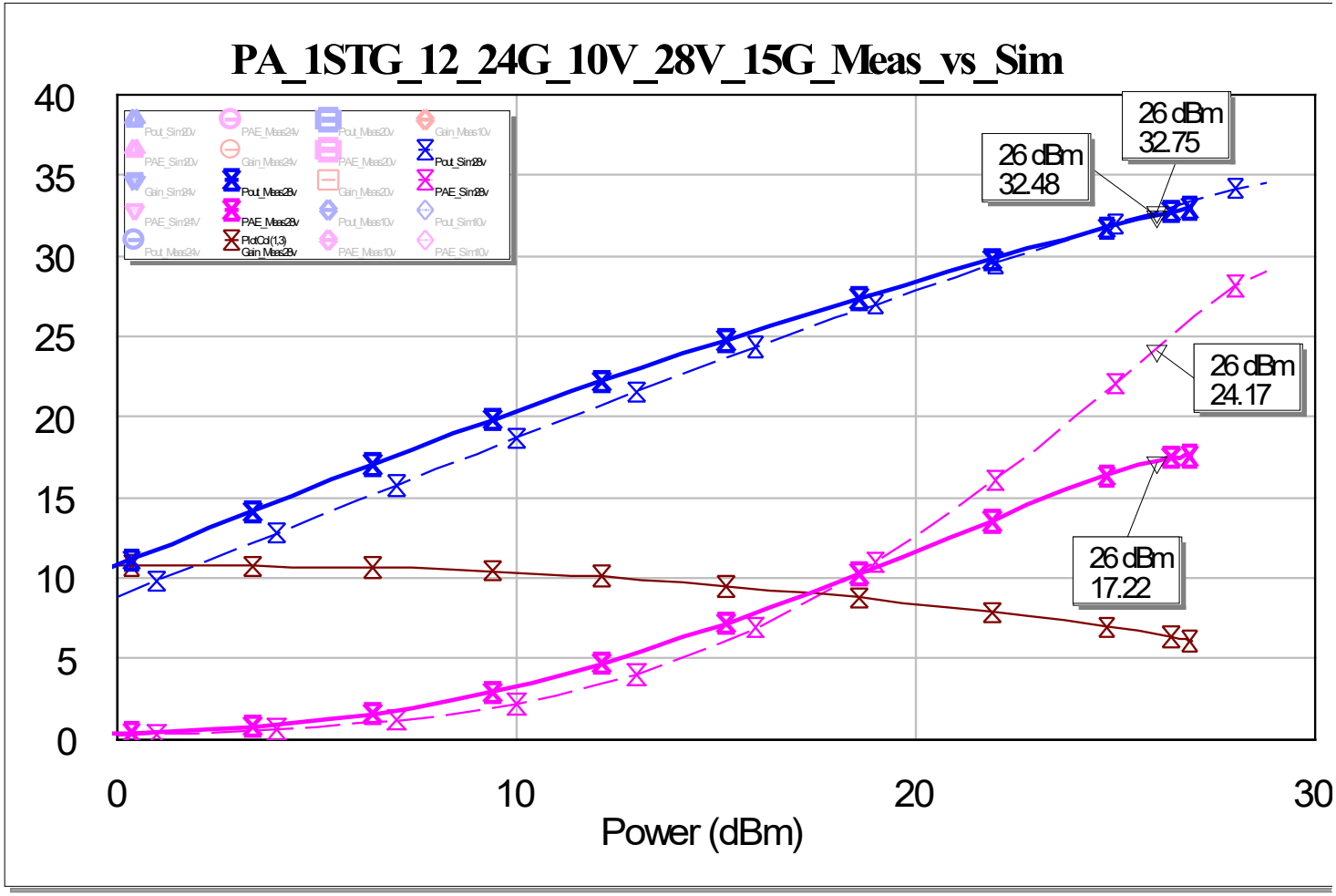

Fig. 27 Performance measurements (solid) vs. simulation (dot) of Pout (blue) and PAE (magenta) for one-stage 12- to 24-GHz PA (28 V)

6. Transmit/Receive (TR) Switch

While there were no switch elements in the design process design kit (PDK), BAE supplied s-parameter measurements of HEMTs at various ON and OFF DC biases for different size HEMTs to use for designing switch circuits. This was used to design two similar TR switches whose layouts are shown in Fig. 28. Typically, the common connection is to an antenna, with the DC biases controlling two series and two shunt switches to connect the antenna to either a low-noise amplifier or a PA. Figure 29 shows measured (solid) versus simulated (dotted) for one TR switch showing good insertion loss of 1 dB at 5 GHz and very good agreement for insertion loss and isolation. Measured return loss was slightly worse than predicted, though quite good given the design was based on preliminary switch measurements. Figure 30 shows the measurement of the other TR switch, which has good insertion loss of 1.2 dB at 5 GHz. Note the low-frequency drop off due to a size-limited series blocking capacitor at the input of the common input for the second TR switch design.

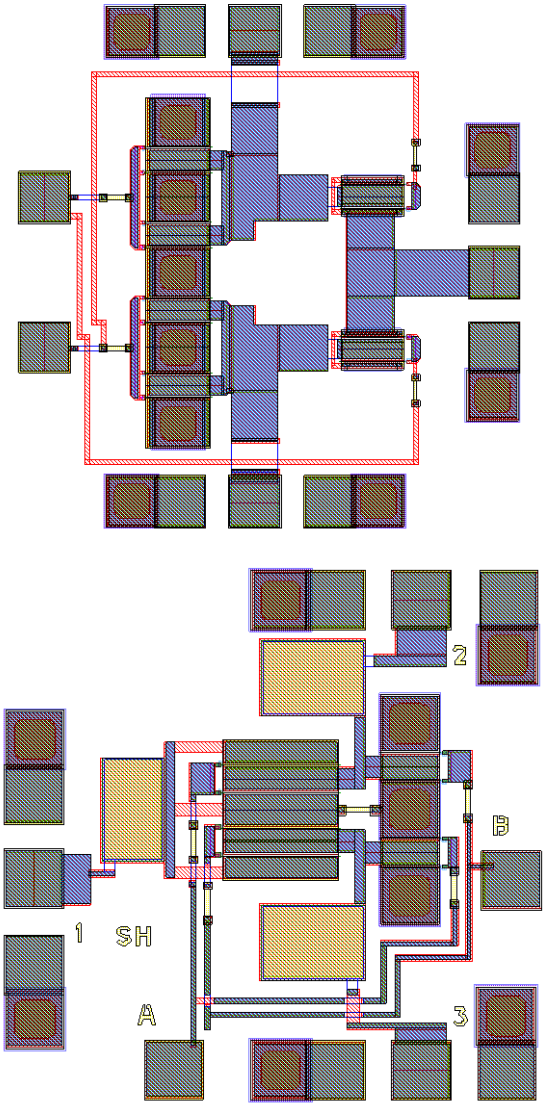

Fig. 28 Layouts of TR switches

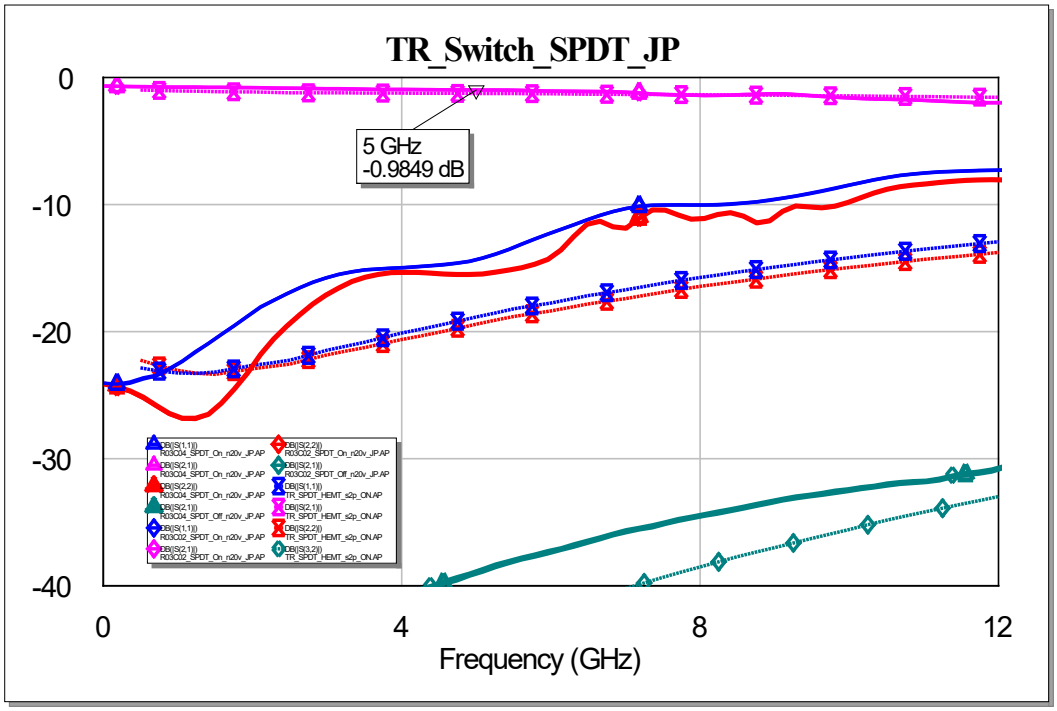

Fig. 29 S-parameter measurements (solid) vs. simulation (dot) of single-pull double-throw (SPDT) TR switch

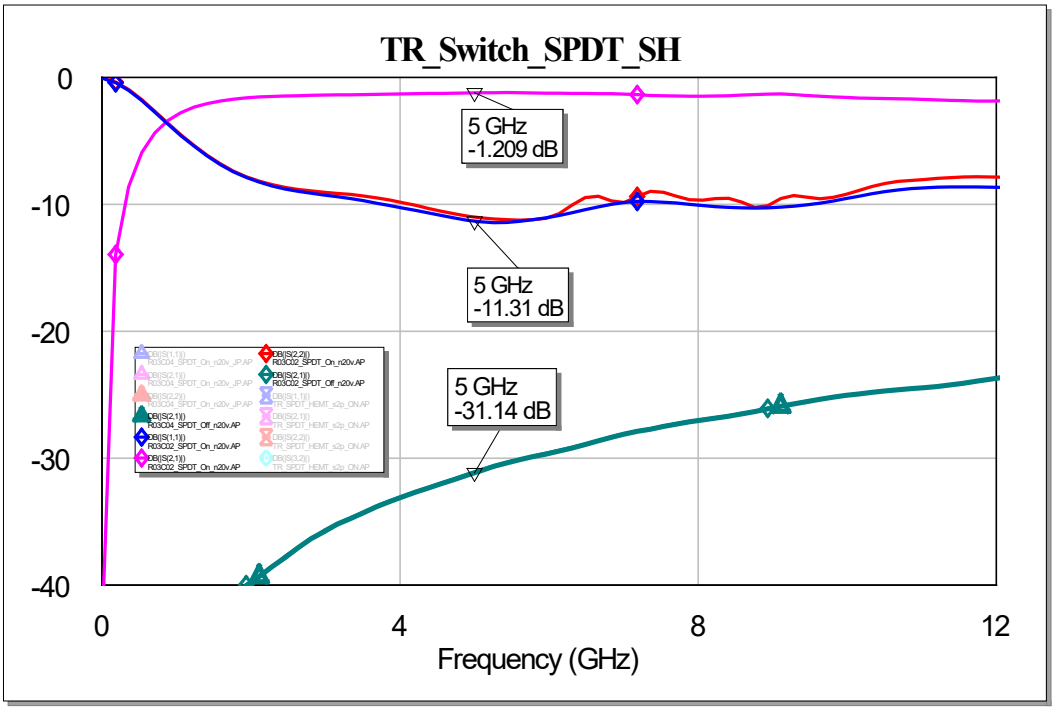

Fig. 30 S-parameter measurements (solid) of SPDT TR Switch #2

7. Ka-Band Mixer

A Ka-band passive mixer was created using a Lange coupler, two HEMTs as diodes, and a low-pass filter (LPF) for the intermediate frequency (IF) output. The layout is shown in Fig. 31, with two RF connections for local oscillator (LO) and RF, and one connection for the IF at the left, next to the LPF. Nonlinear simulations of the mixer failed and gave an error message, possibly due to limitations in the current design PDK. Hopefully, future PDKs will have more capability in their nonlinear models for simulating designs other than amplifiers. Testing was successful, though it appears that more LO power is needed, especially at higher frequencies where the input losses were higher. An IF frequency of 1 GHz was chosen, and the LO was tested at 21, 25, and 28 GHz with an RF signal of –15-dBm offset at 22, 26, and 29 GHz. Table 1 shows the measured data with corrections for 1 dB loss at IF (1 GHz) and 5- to 6.4-dB loss offsets with increasing LO frequency. A reasonable, though still increasing, conversion loss was measured as 14 dB for the 21-GHz LO when 15-dBm power was supplied (20 dBm at the signal generator). At the other two test frequencies the conversion loss was still increasing, as the LO power was limited. A retest with an amplifier after the signal generator should help determine the best LO drive and conversion loss. Ideally, the LO power should be increased until the conversion loss peaked. It was expected that the higher voltage of the GaN diodes would require a significant LO power; still, the mixer worked well over a broad band even at lower than desired LO drive levels. Figure 32 shows a plot of conversion loss versus LO input power with a peak of –14 dB for the 21-GHz LO case.

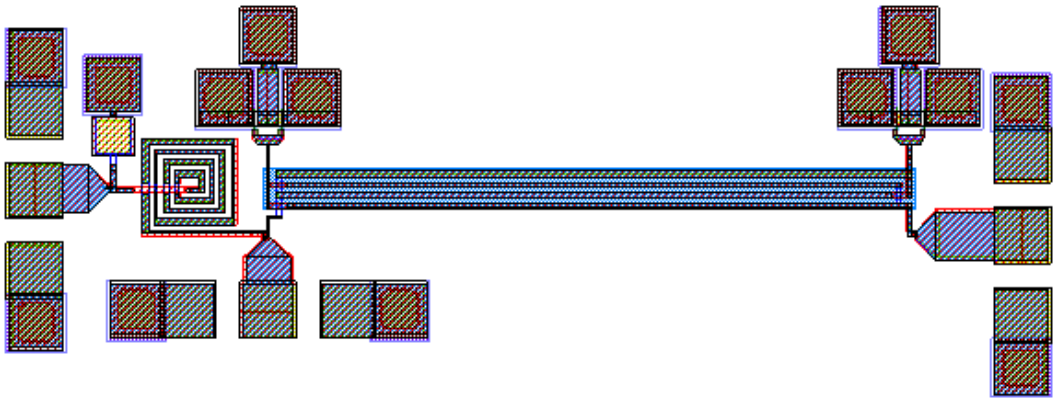

Fig. 31 Layout of diode mixer

Table 1 Testing of diode mixer

	LO = 21 GHz	LO = 25 GH:	LO = 28 GHz		21		25		28	
SG	RF = 22GHz	RF = 26GHz	RF = 29GHz		5		5.75		6.4	
LO Pwr (ms)	IF(1GHz)	IF(1GHz)	IF(1GHz)		LO Pwr (c	Conv(Ls)	LO Pwr (c	Conv(Ls)	LO Pwr (c	Conv(Ls)
16	-52.5	-62	-68		11	-31.5	10.25	-40.25	9.6	-45.6
17	-44.2	-57	-59.8		12	-23.2	11.25	-35.25	10.6	-37.4
18	-39	-51.8	-55.2		13	-18	12.25	-30.05	11.6	-32.8
19	-36.6	-42.4			14	-15.6	13.25	-20.65	12.6	
20	-35.1				15	-14.1	14.25		13.6	

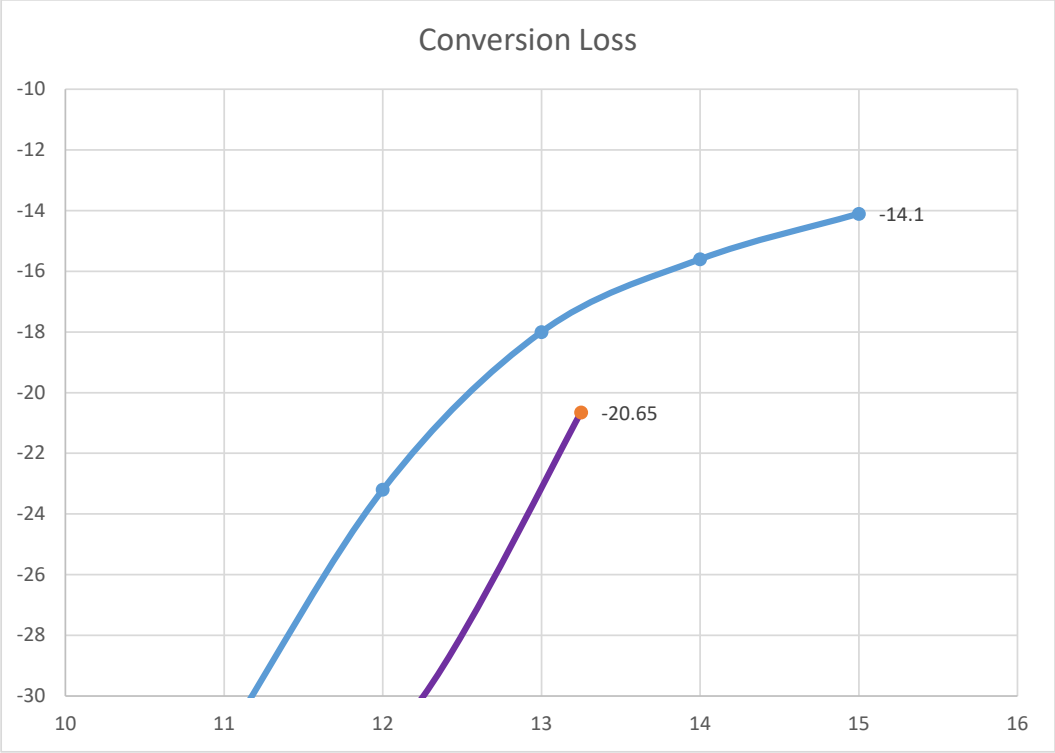

Fig. 32 Conversion loss of diode mixer vs. LO Pin

8. Frequency Doublers

The current architecture for an extremely broadband transmitter makes use of broadband frequency multipliers. Some broadband doublers were designed using baluns to provide fundamental cancellation over an octave bandwidth. Another high-frequency doubler used a narrowband doubler circuit with an input designed for around 25 GHz and an output at twice that frequency. A balun was used to provide broadband fundamental cancellation. The layout of the subcircuit for this doubler is shown in Fig. 33 along with the full doubler including balun in Fig. 34. Small signal measurements of the doubler subcircuit were performed to verify that the input match was good around 25 GHz and the output match was sufficient

around 50 GHz. Figure 35 shows simulated (dot) and measured (solid) small signal performance for the doubler subcircuit. For nonlinear performance, a signal generator supplied sufficient Pin to peak the doubling over a frequency range just below 25 GHz so that the fundamental and second harmonic-doubled frequency could be seen simultaneously on a 50-GHz spectrum analyzer. An input of 4–8 dBm was sufficient at 21.5, 22.5, 23.5, and 24.5 GHz to provide 10- to 13-dB conversion loss for the single-stage doubler. Shown in Table 2 is a summary of the corrected Pin, doubled output power at 43, 45, 47, and 49 GHz, and the conversion loss with a 2-V drain bias and –3.2-V gate bias. The larger doubler was also tested over the same frequency range at the same 2-V drain bias and –3.2-V gate bias. Since the input is divided to two of the single subcircuits, a higher input power of about 12–15 dBm is needed at 21.5, 22.5, 23.5, and 24.5 GHz to provide 12- to 15-dB conversion loss with excellent fundamental cancellation. A summary of the corrected Pin, fundamental leakage Pout, doubled output power at 43, 45, and 47 GHz, and the conversion loss is shown in Table 3. The balun provided excellent cancellation of the fundamental input by 30 dB, a factor of 1000 in power. For a 24.5-GHz input and 49-GHz output, the mixer yielded 12-dB conversion loss with 27 dB of fundamental cancellation.

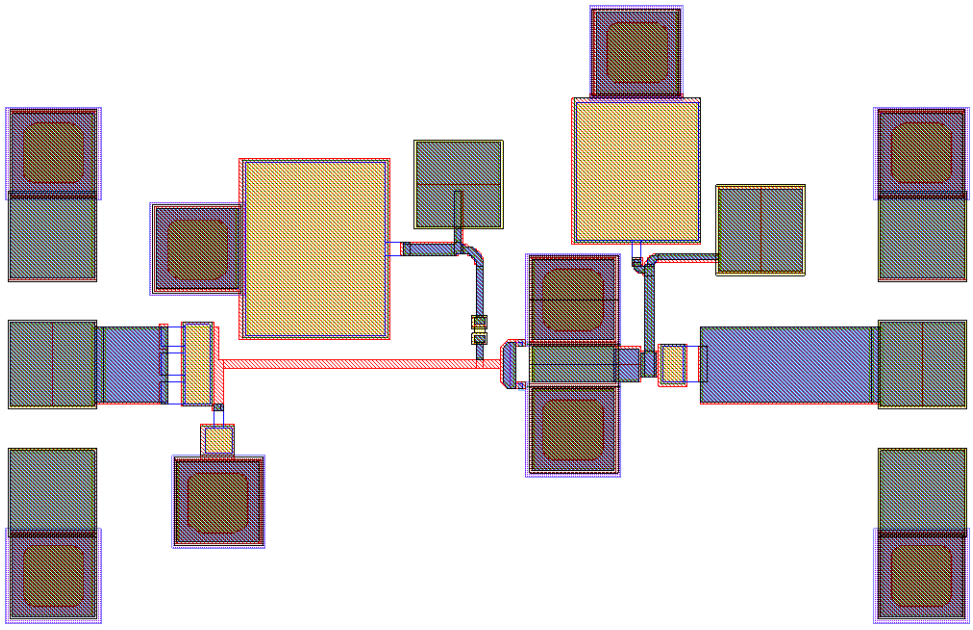

Fig. 33 Final layout of single-stage 25-GHz 2- × 100-µm frequency doubler

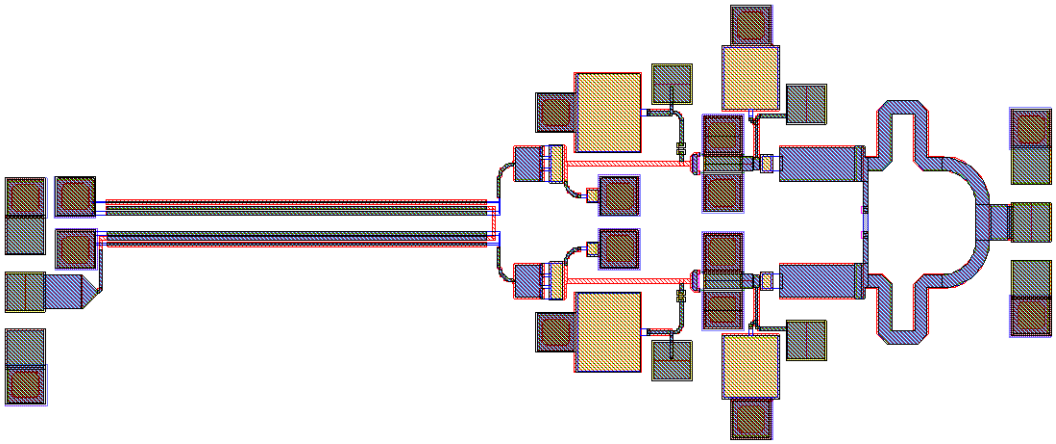

Fig. 34 Final layout of fundamental cancelling 25-GHz 2- × 100-µm frequency doubler (with balun)

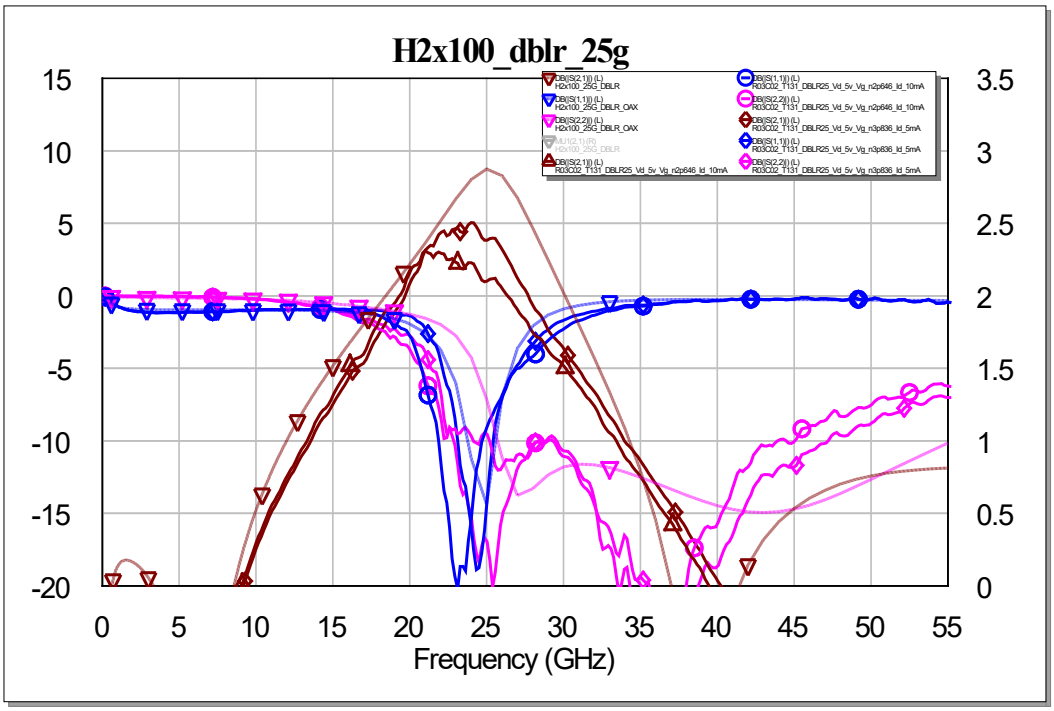

Fig. 35 S-parameter measurements (solid) vs. simulation (dot) of single-stage 25-GHz frequency doubler

Table 2 Single doubler Pin, doubled Pout, and conversion loss (43–49 GHz)

Pin(21.5G)	X2(43G)	convLos	Pin(22.5G)	X2(45G)	convLos	Pin(23.5G)	X2(47G)	convLos	Pin(24.5G)	X2(49G)	convLos
7	-6.4	-13.4	5.8	-4.4	-10.15	**6.5**	**-4.9**	**-11.4**	**4.3**	**-8.9**	**-13.2**
8	**-4.1**	**-12.1**	**6.8**	**-3.1**	**-9.85**	7.5	-4.5	-12	5.3	-7.9	-13.2
9	-2.9	-11.9	7.8	-2.3	-10.1	8.5	-4.6	-13.1	6.3	-7.2	-13.45

Table 3 Doubler with balun Pin, fundamental Pout, doubled Pout, conversion loss, and isolation (43–47 GHz)

Pin(21.5G)	X1(21.5G)	X2(43G)	convLos	Pin(22.5G)	X1(22.5G)	X2(45G)	convLos	Pin(23.5G	X1(23.5G)	X2(47G)	convLos
15	**-20.4**	**0.1**	**-14.9**	**12.8**	**-19.2**	**-0.1**	**-12.9**	**12.5**	**-17.5**	**-0.1**	**-12.6**
IsolationX1	**35.4**				**32**				**30**		

The other two doubler designs tested were a 6- to 12-GHz doubler and 12- to 24-GHz doubler. Figure 36 shows a plot of the 6- to 12-GHz doubler with a compact balun at the input. The circuit was tested over 6 to 12 GHz with a signal generator set at 16 dBm or higher which was actually a few dB lower at the circuit under test due to cable losses. From 6 to 9 GHz, the doubler bias was –2 V on the drain and –3.5 V on the gate. To overcome some stability issues, the bias was lowered to 0.6 V on the drain, which lowers the doubled output. Output power may be lower than expected, as this layout was pulled from the larger CHIP2 design and was intended to have two parallel output connections, while in the breakout test circuit the output is connected through a single output of a resistor in series with the 50-ohm output. Isolation from the input signal to leakage at the output was excellent, with Table 4 showing the conversion loss from input signal to doubled output followed by the isolation of the input from 6–12 GHz. Note the output conversion loss is much better at the 2-V biases from 6–9 GHz. Figure 37 shows a plot of the smaller 12- to 24-GHz doubler with a compact balun at the input. The higher-frequency doubler was tested at 12-, 14-, 16-, 18-, 19-, and 20-GHz steps, with excellent fundamental cancellation from the balun measured at 12, 16, and 19 GHz as 32–28 dB. A typical measurement of the corrected Pin at 12 GHz, fundamental output power, doubled output power at 24 GHz, the conversion loss, and isolation is shown in Table 5. Conversion loss was lowest at about 2 dB at 12 GHz and increased to 10 dB at 19 GHz, with a drop to 20-dB conversion loss at 20 GHz. While it still doubled at 20 GHz and above, the efficiency dropped significantly above 19 GHz. An analysis of these results can be used for a possible future redesign to improve the performance at the higher end of the band.

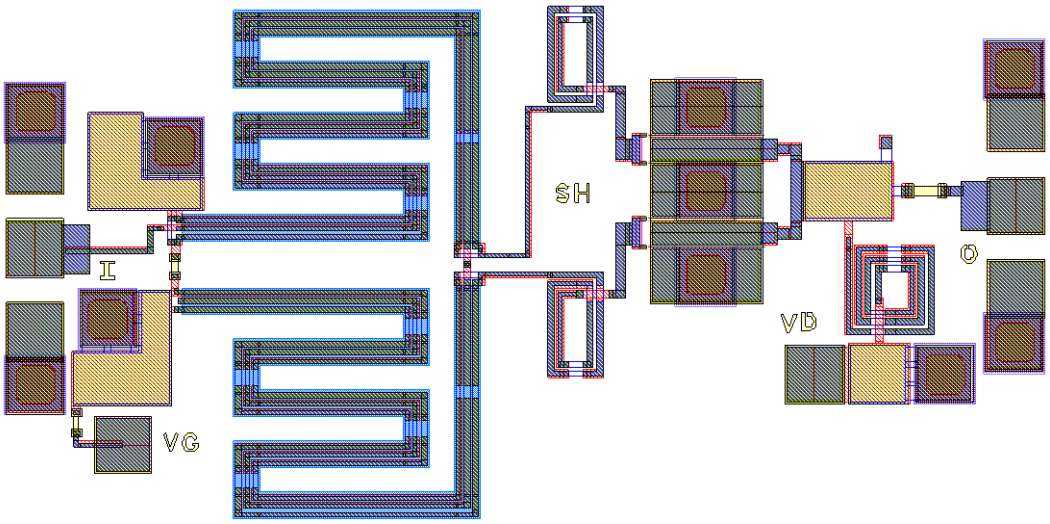

Fig. 36 Final layout of the 6- to 12-GHz frequency doubler

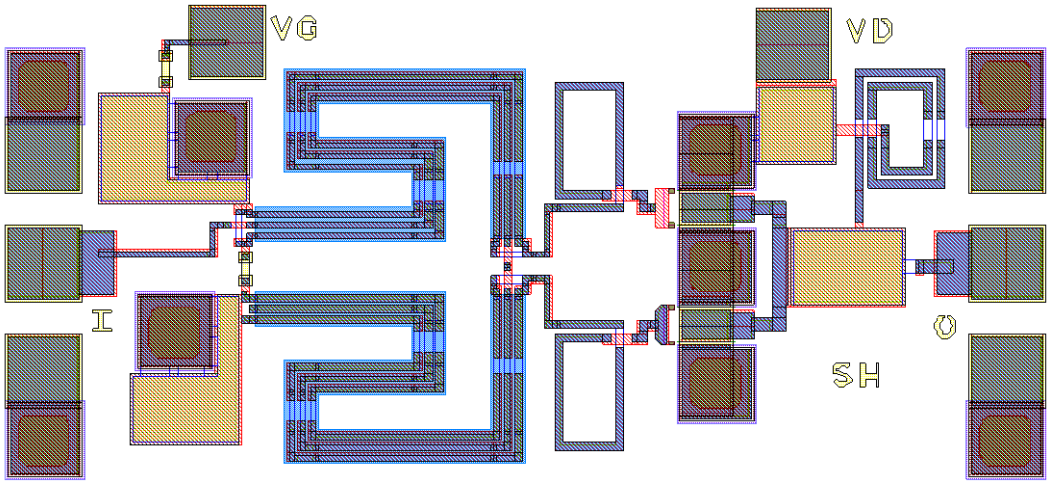

Fig. 37 Final layout of 12- to 24-GHz frequency doubler

Table 4 6- to 12-GHz doubler with input frequency, doubled conversion loss, and isolation

Fin(GHz)	Converion	Isolation
6	-25.5	-53.8
7	-27.4	-53.9
8	-29.2	-51.8
9	-27.0	-52.7
10	-40.4	-63.5
11	-41.9	-68.3
12	-35.9	-62.6

Table 5 12- to 24-GHz doubler with Pin, fundamental Pout, doubled Pout, conversion loss, and isolation (24 GHz)

Pin(12G)	X1(12G)	X2(24G)	convLoss	isolation
-4.6	-35.4	-9.3	-4.7	30.8
-2.6	-34.6	-6.2	-3.6	32
-0.6	-33.4	-3.3	-2.7	32.8
1.4	**-31.4**	**-0.7**	**-2.1**	**32.8**
3.4	-28.9	1.6	-1.9	32.3

9. Test HEMTs and Calibration Circuits

Using available space on the 9- × 6-mm die, several HEMTs were included for comparison with the PDK models and for analyzing overall circuit performance. Calibration structures were also included and were compared with Axiem EM simulations of the physical layouts. A TRL calibration could be performed to move the device reference plane to remove the ground–signal–ground (GSG) launches, or an alternative would be to Axiem EM simulate the GSG launch layouts and use CAD tools to shift the reference plane.

Test HEMTs included on the fabrication were 2 × 50 µm, 4 × 50 µm, and 2 × 100 µm, whose measurements matched well to the circuit models, except for the gain of a nonlinear model for the 2 × 50 µm. There may be an issue with that particular 2- × 50-µm nonlinear model; however, the linear 2 × 50-µm model matched very well. HEMTs were tested at 10, 20, 24, and 28 V. Calibration structures of open, short, match (50 Ω), and varying line lengths were also tested and compared well to simulations of those test circuits. Figure 38 shows the EM structures where the simulation de-embeds to approximately where the GSG probes would touch the test structure. Note the EM simulation uses a simple microstrip port (S), not a coplanar port (GSG), though both are modes are matched to 50 ohm. Measurements to 70 GHz of the open, short, and load compare very well to simulations, as shown in Fig. 39, with slightly more loss in the measured “open”. Likewise, the Thru line was EM simulated (Fig. 40) and compared with measurements to 70 GHz with good agreement (Fig. 41). Measurements of the 1200-µm line are also plotted and agree with linecalc calculations of this microstrip line used for TRL calibrations.

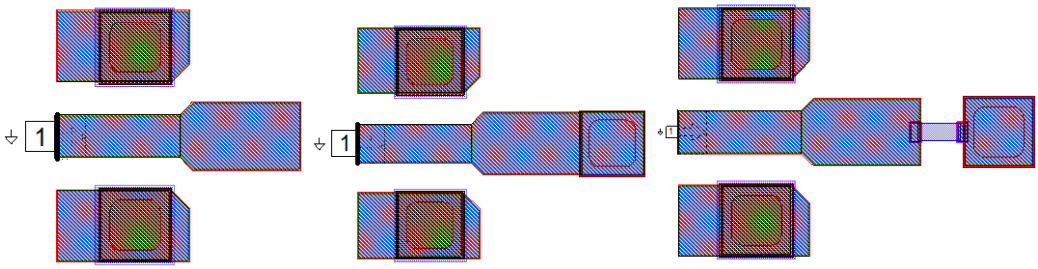

Fig. 38 EM simulations of open, short, and load (50 Ω) test circuits

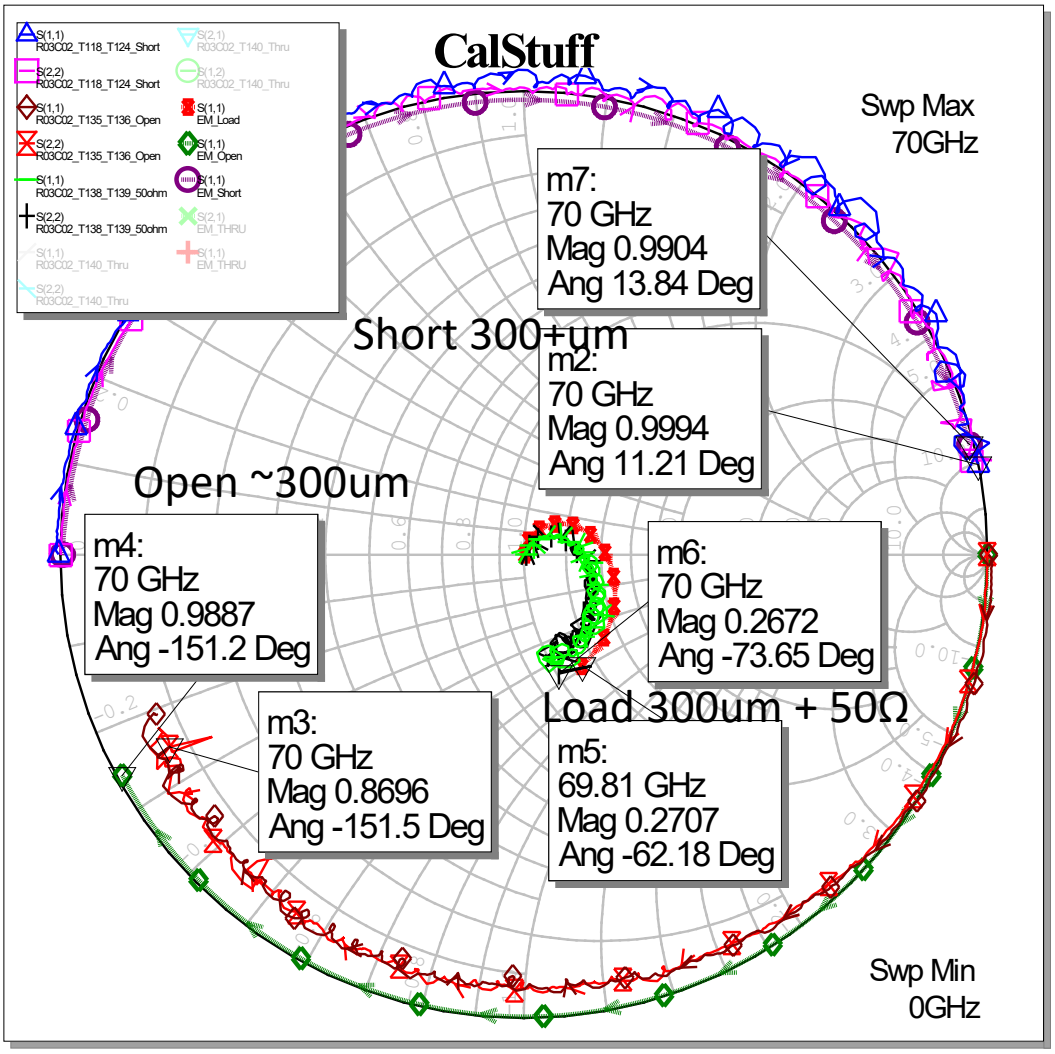

Fig. 39 S-parameter measurements (solid) vs. simulation (dot) of open, short, and load (50 Ω)

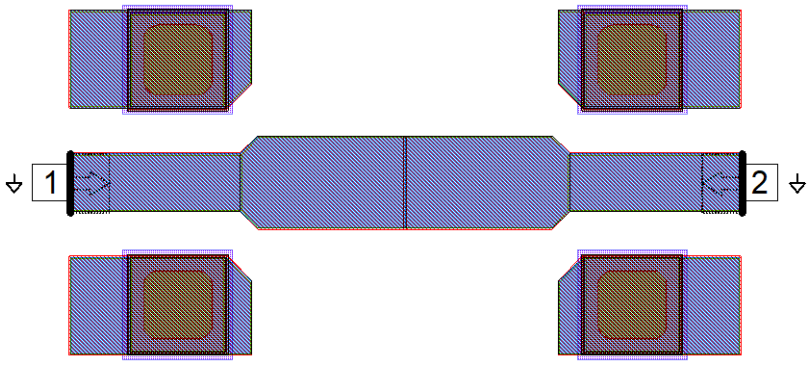

Fig. 40 EM simulation of Thru test circuits

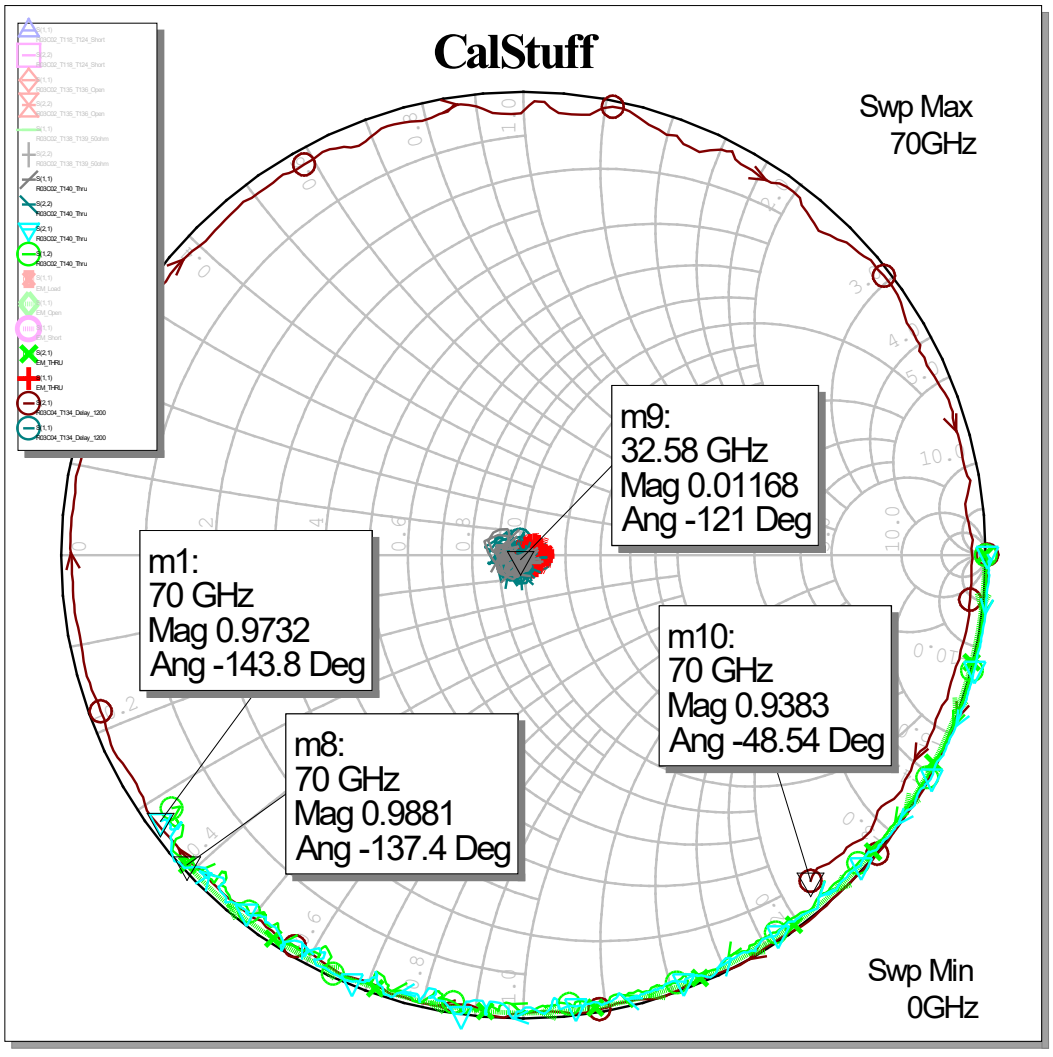

Fig. 41 S-parameter measurements (solid) vs. simulation (dot) of Thru and 1200-µm line

Shown are measured versus linear model simulations for the 2- × 50-µm and 2- × 100- µm test HEMTs at comparable biases, with S11 and S22 plotted on Smith

charts and then S21, S11, and S22 plotted on rectangular plots. Linear and nonlinear models matched very well to 70 GHz for these two device sizes and were nearly as well matched for the 4 × 50-µm HEMT, which is not shown but is very similar to the 2 × 100-µm HEMT. Figures 42 and 43 show the 2- × 50-µm Smith and rectangular plots, while Figs. 44 and 45 show the 2- × 100-µm small signal Smith and rectangular plots. Measurements were taken at 10, 20, 24, and 28 V, but comparisons are plotted at around 20 V. There are some measureable changes with bias, particularly at the low end at 10 V.

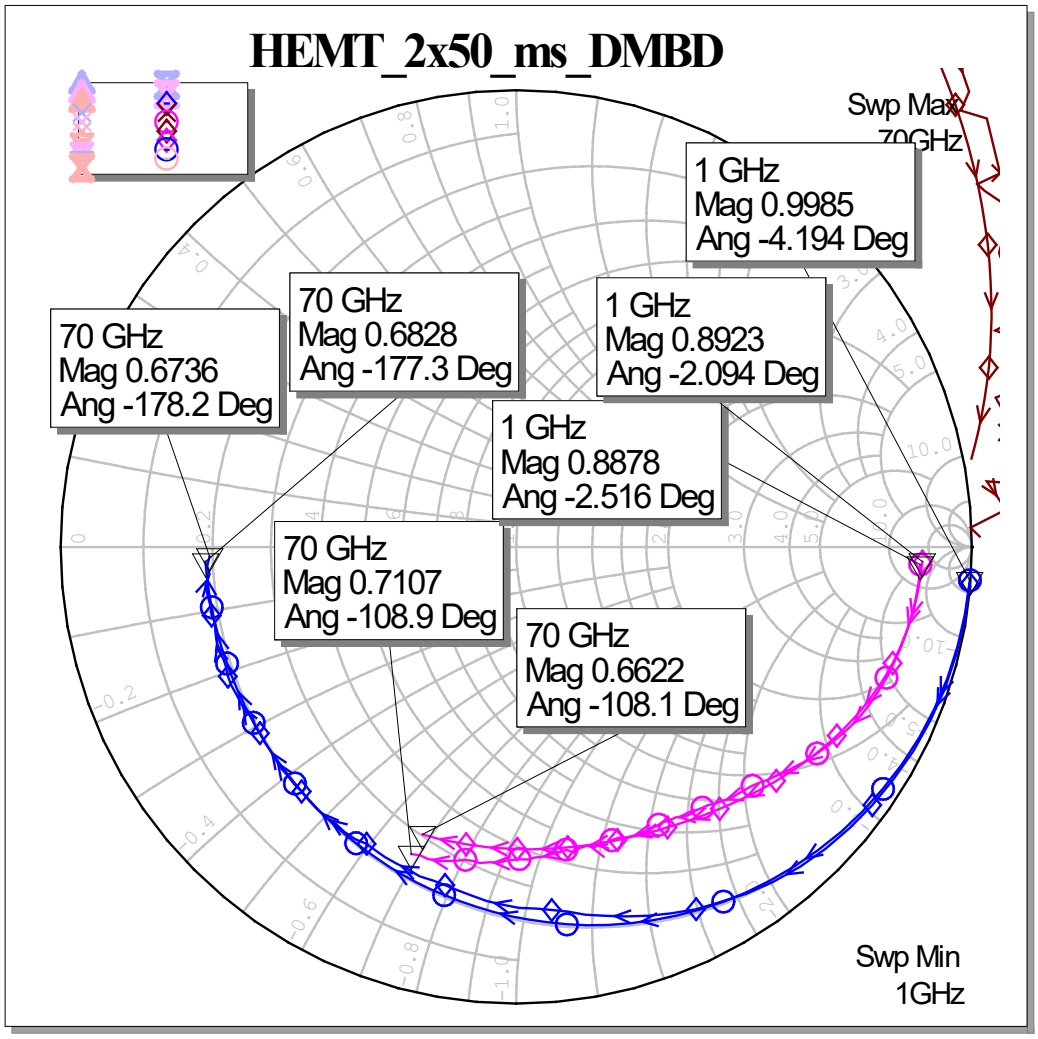

Fig. 42 S-parameter measurements vs. linear simulation of 2- × 50-µm HEMT (Smith chart)

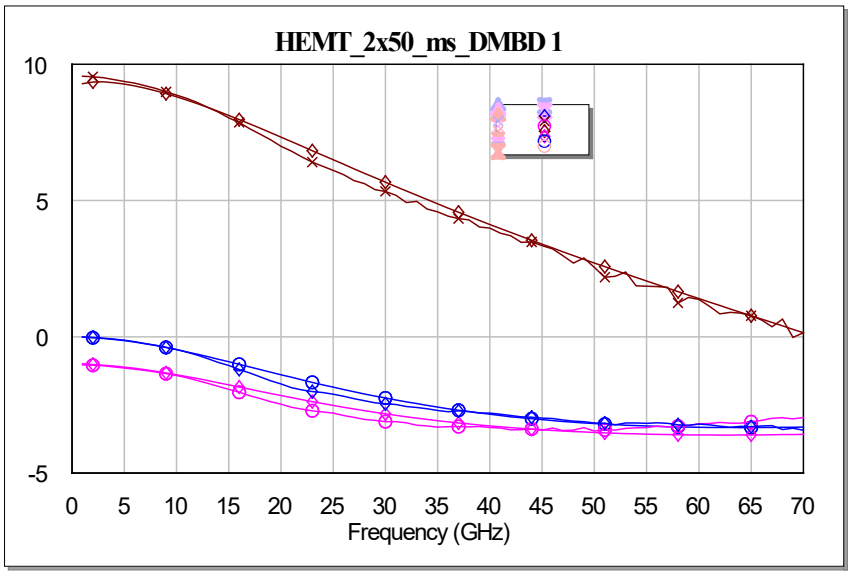

Fig. 43 S-parameter measurements vs. linear simulation of 2- × 50-µm HEMT (rectangular plot)

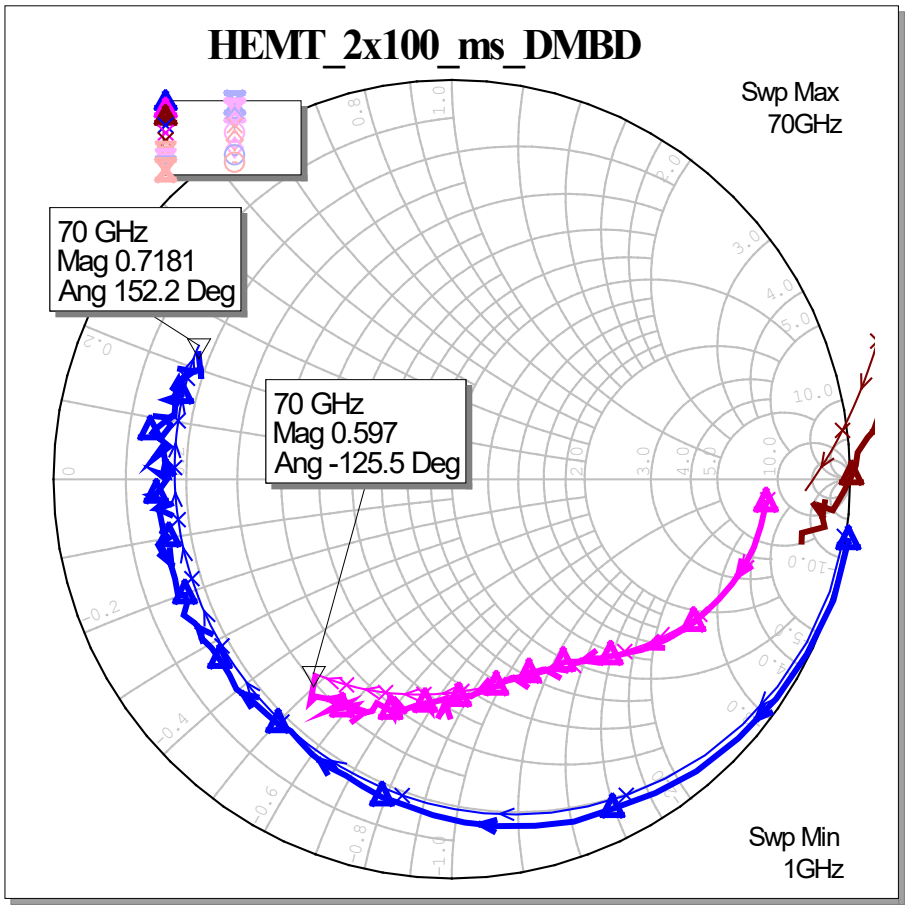

Fig. 44 S-parameter measurements vs. linear simulation of 2- × 100-µm HEMT (Smith chart)

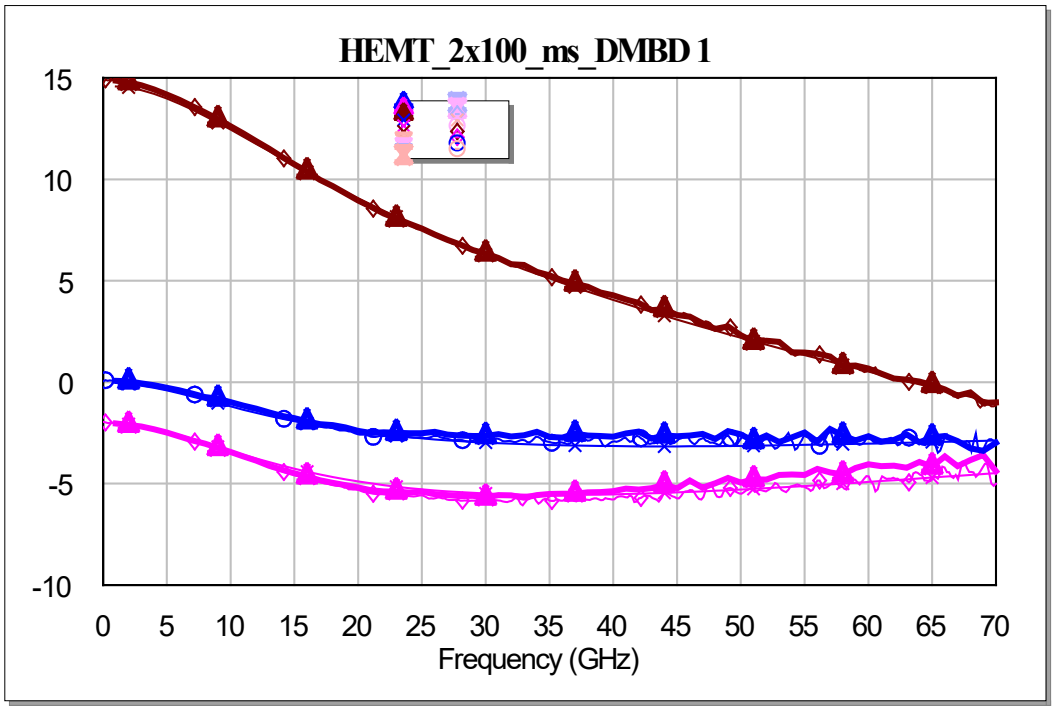

Fig. 45 S-parameter measurements vs. linear simulation of 2- × 100-µm HEMT (rectangular plot)

10. Conclusions

The first phase of the GAN RF Challenge effort included many teams exploring challenges focused on the broadband 5G development and EW needs related to DOD needs. Our DEVCOM ARL III/V Team was primarily focused on a very broadband transmitter fabricated in the BAE 0.18-µm GaN process. The larger transmitter Chip #2 has many of its designs fabricated as stand-alone test subcircuits on Chip #1, making it easier to evaluate and debug design issues and interactions at the larger integration level. Broadband amplifiers, mixers, frequency multipliers, test HEMTs, calibration structures, and other microwave circuits were designed, fabricated, and tested to meet some of the DOD challenges, particularly EW and future congested and contested RF spectrum as 5G develops. Additional test results for the larger circuits may be included in future test reports. Prior technical reports on this effort are listed in the references.[1,2]

11. References

1. Penn J, Darwish A, Hawasli S. Gallium nitride (GaN) RF challenge: BAE Systems and Qorvo submissions. Army Research Laboratory (US); 2021 Feb. Report No.: ARL-TN-1047.

2. Penn J. Gallium nitride (GaN) RF challenge: broadband power amplifiers in BAE 0.18-µm GaN technology. Army Research Laboratory (US); 2021 Feb. Report No.: ARL-TR-9147.

List of Symbols, Abbreviations, and Acronyms

ARL	Army Research Laboratory
CAD	computer-aided design
DA	distributed amplifier
DC	direct current
DEVCOM	US Army Combat Capabilities Development Command
DOD	Department of Defense
EM	electromagnetic
EW	electronic warfare
GaN	gallium nitride
GSG	ground–signal–ground
HEMT	high-electron-mobility transistor
IF	intermediate frequency
LO	local oscillator
LPF	low-pass filter
MMIC	monolithic microwave integrated circuit
PA	power amplifier
PAE	power-added efficiency
PDK	process design kit
Pin	input power
Pout	output power
RF	radio frequency
SPDT	single-pull double-throw
TR	transmit, receive
TRL	through-reflect-line

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	S HAWASLI
	T IVANOV
	P GADFORT
	K KINGKEO
	J PENN (HC)
	E VIVEIROS