Carnegie Mellon University
Software Engineering Institute

## Research Review 2021

# Using All Processor Cores While Being Confident about Timing

**November 2021**

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This material is based upon work funded and supported by the Department of Defense under Contract No. FA8702-15-D-0002 with Carnegie Mellon University for the operation of the Software Engineering Institute, a federally funded research and development center.



DM21-0810

Complex, cyber-physical DoD systems depend on correct timing—any timing failure could be disastrous. What's more, while these systems drive demand for use of multicore processors, concern about timing has led to disabling all processor cores except one—limiting system capability.

We aim to develop a solution to overcome this obstacle.

# DoD Systems Interact with Their Physical Environment






# DoD Systems Include Software






# DoD Systems Include Software That Interacts with the Physical Environment

# DoD Systems Include Software That Has Real-Time Requirements

# Satisfying Real-Time Requirements Is a Challenge for the DoD in General

# Satisfying Real-Time Requirements Is Challenging for Upgrading the Blackhawk UH-60 Helicopter

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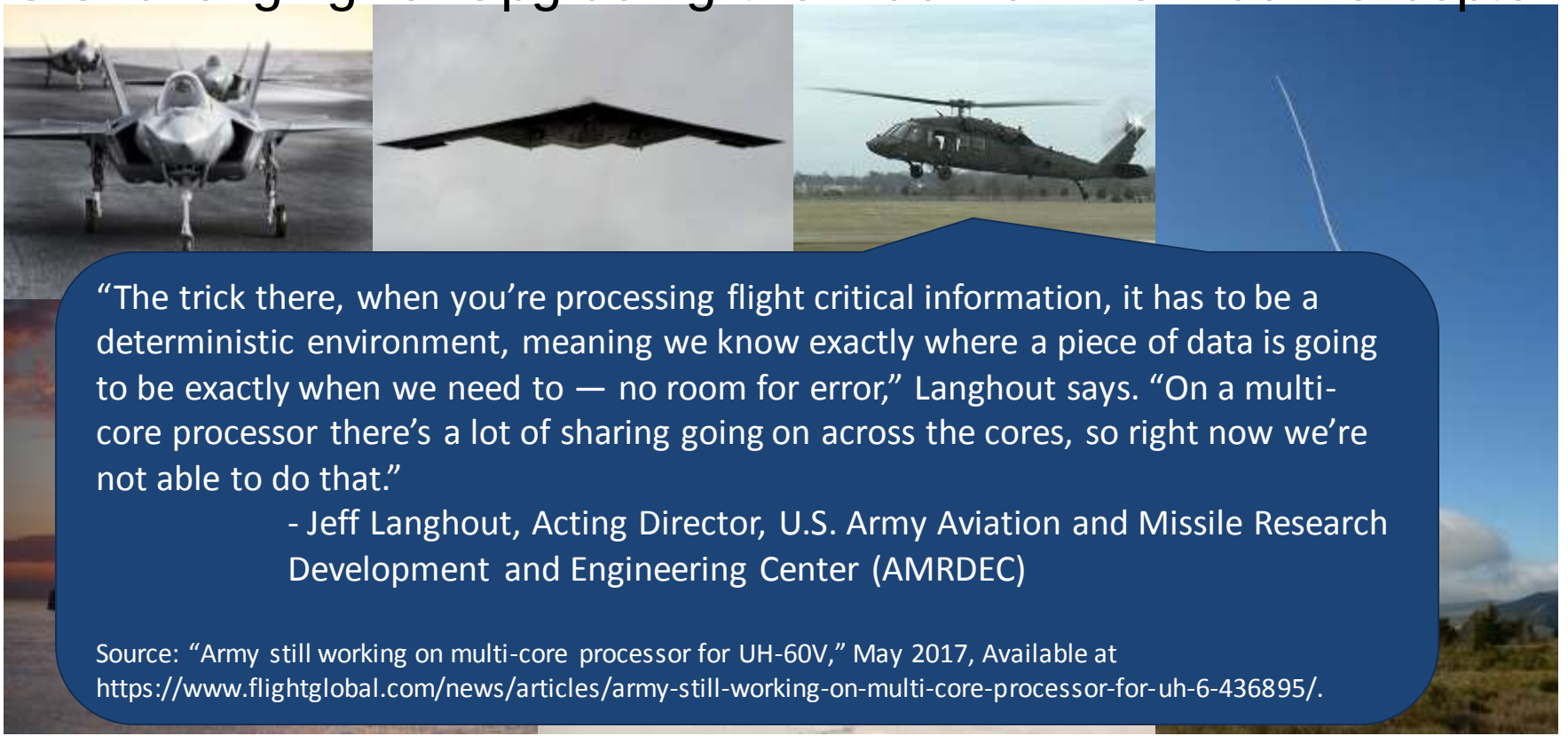
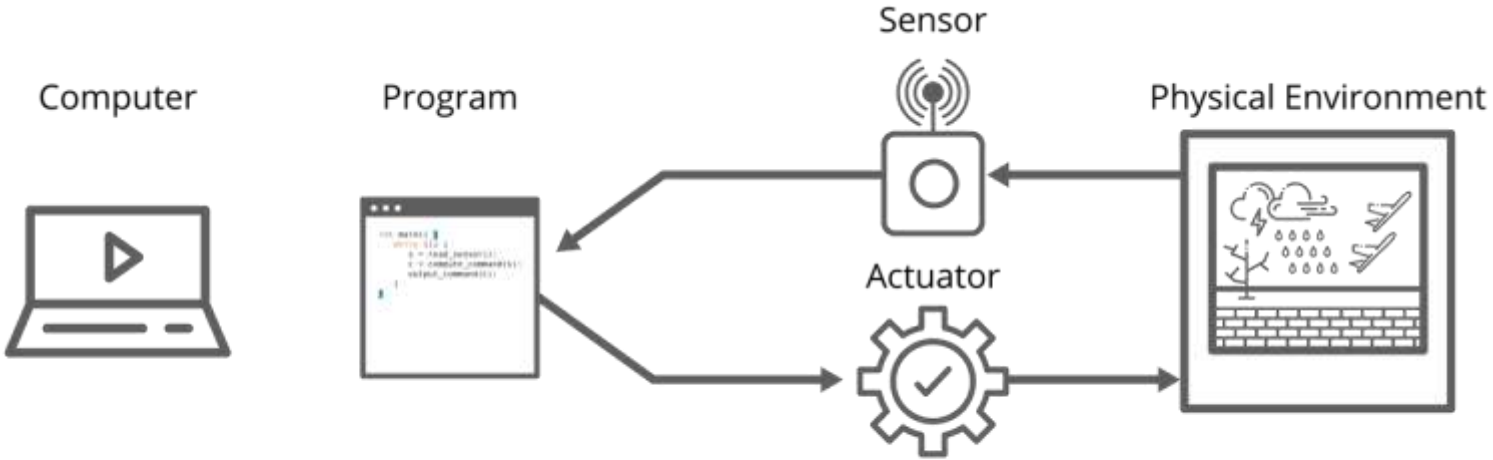


"The trick there, when you're processing flight critical information, it has to be a deterministic environment, meaning we know exactly where a piece of data is going to be exactly when we need to — no room for error," Langhout says. "On a multi-core processor there's a lot of sharing going on across the cores, so right now we're not able to do that."

- Jeff Langhout, Acting Director, U.S. Army Aviation and Missile Research Development and Engineering Center (AMRDEC)

Source: "Army still working on multi-core processor for UH-60V," May 2017, Available at https://www.flightglobal.com/news/articles/army-still-working-on-multi-core-processor-for-uh-6-436895/.

# Commonality of DoD Systems



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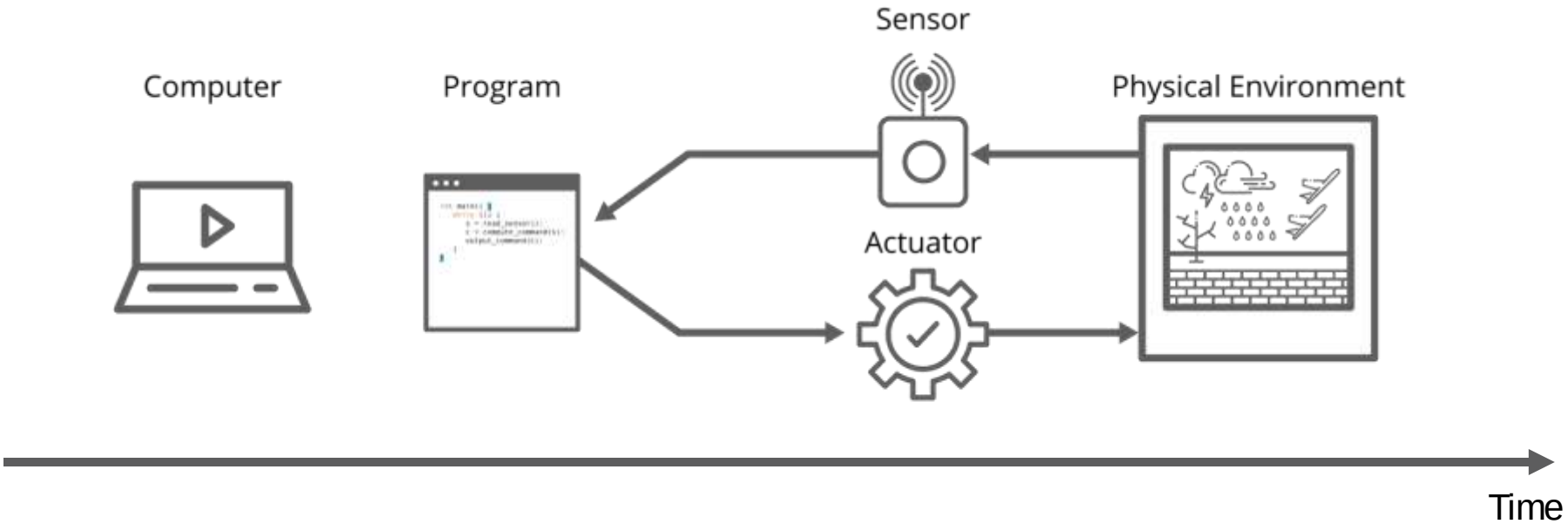

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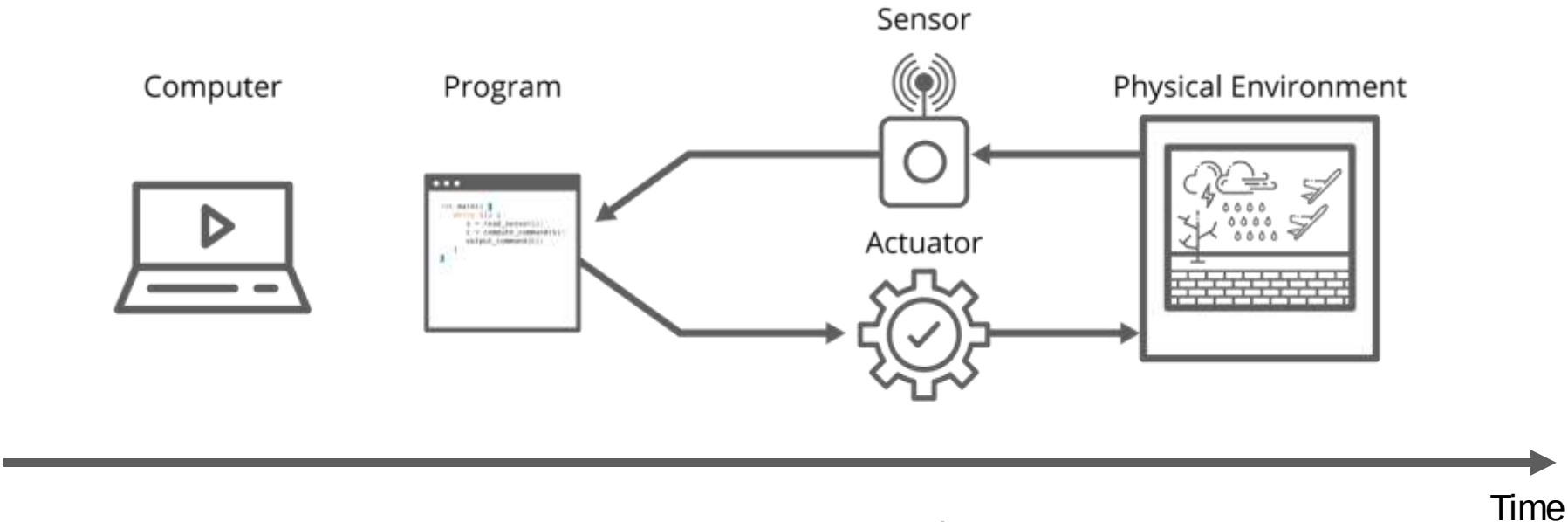

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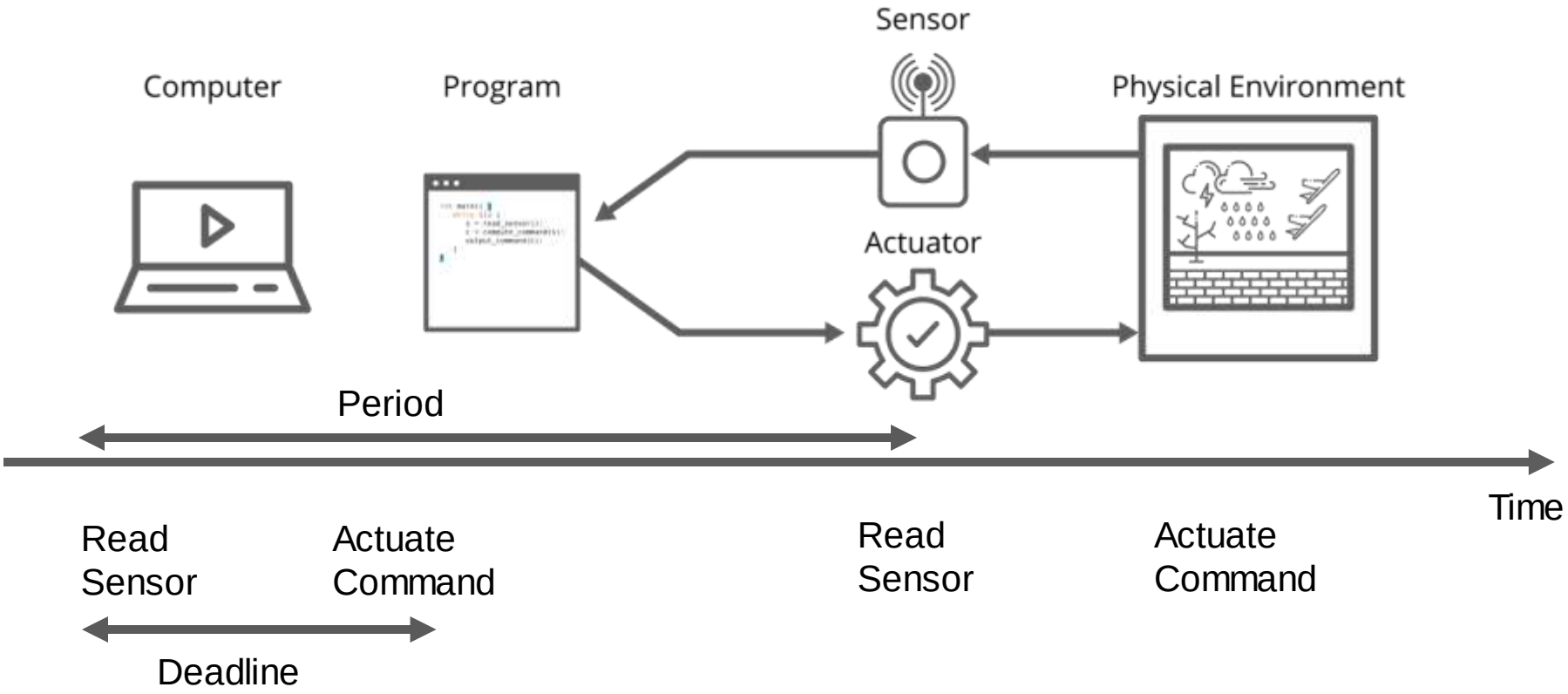

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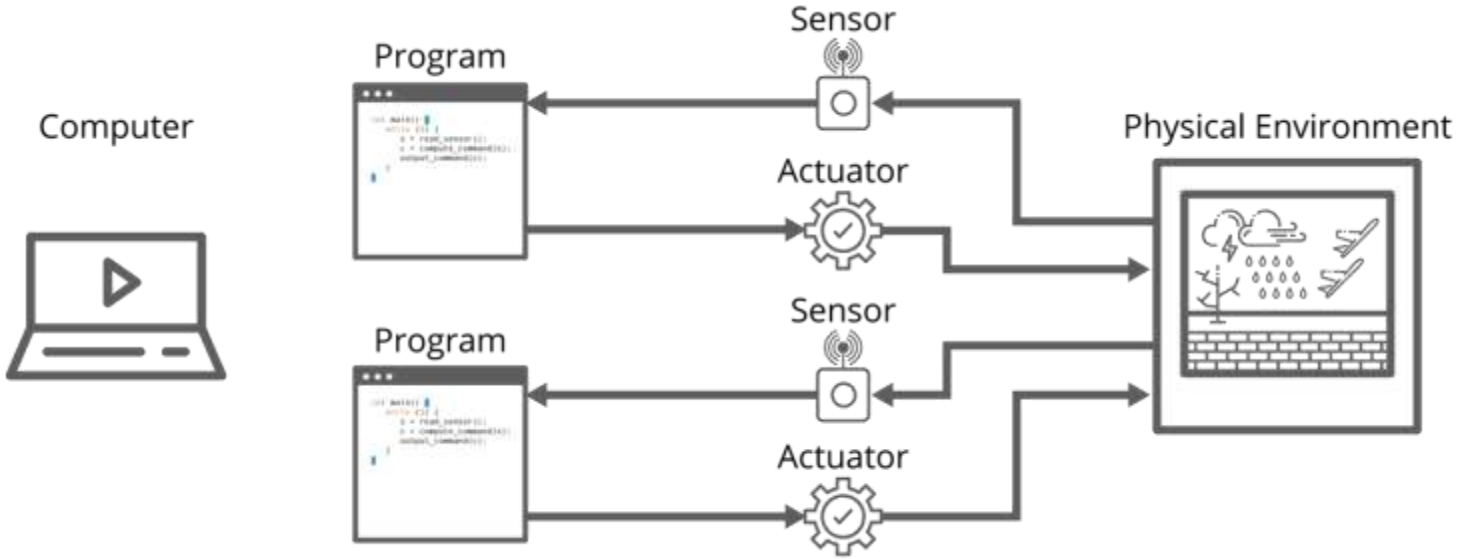

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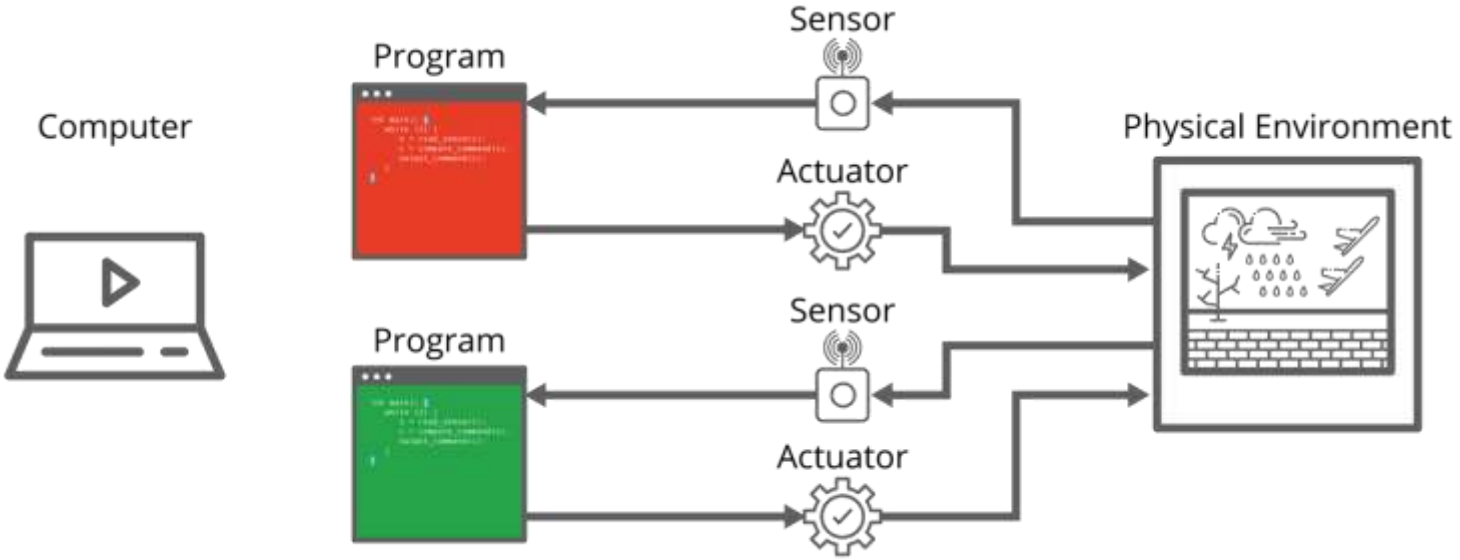


Read Sensor

Actuate Command

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# What Makes it Challenging to Satisfy Real-Time Requirements?

# What Causes Delay of Software?

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Time when one thread in the software system arrives

Deadline Time

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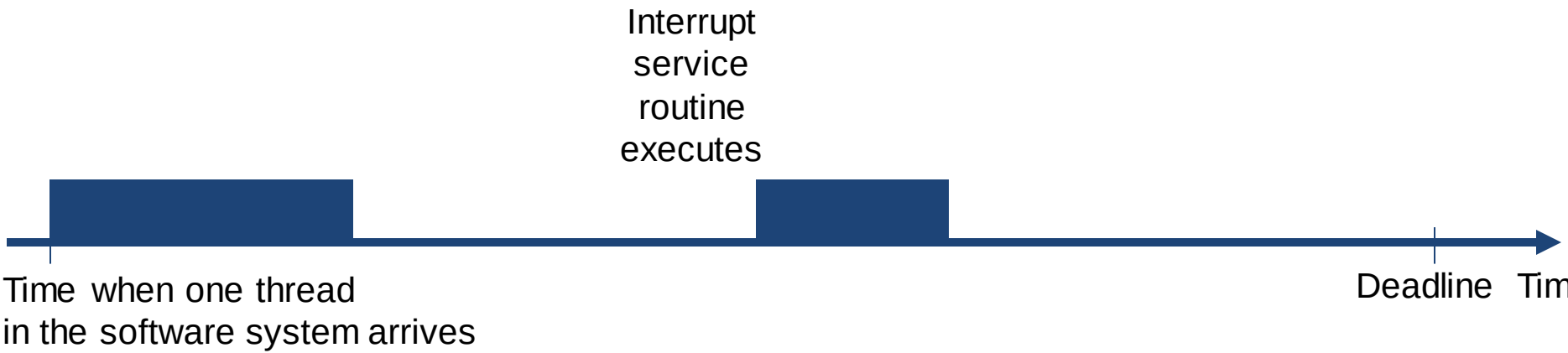

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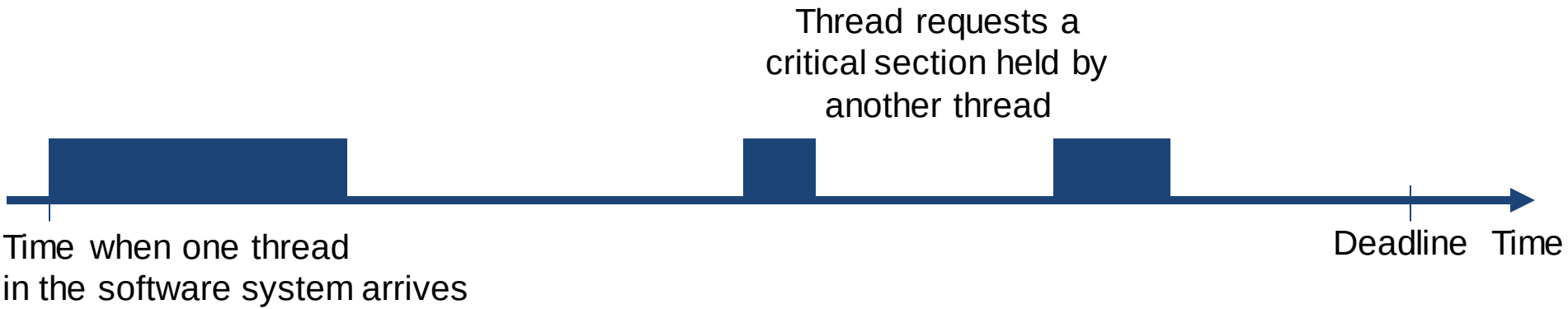
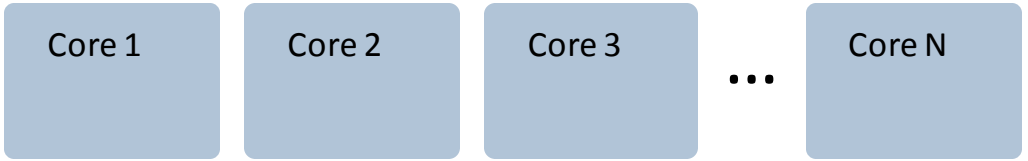


# What Causes Delay of Software?

# Real-Time Requirements of Software Executing on a Multicore Processor

## Hardware Trends

- *All computers are multicores.*



# Real-Time Requirements of Software Executing on a Multicore Processor

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- *All computers are multicores.*
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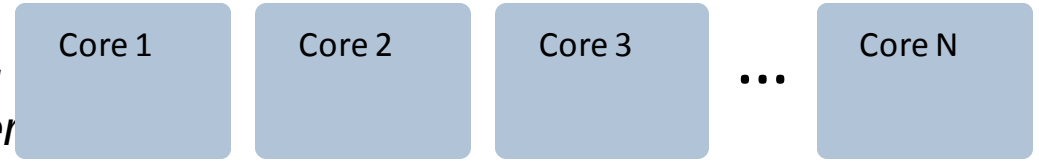
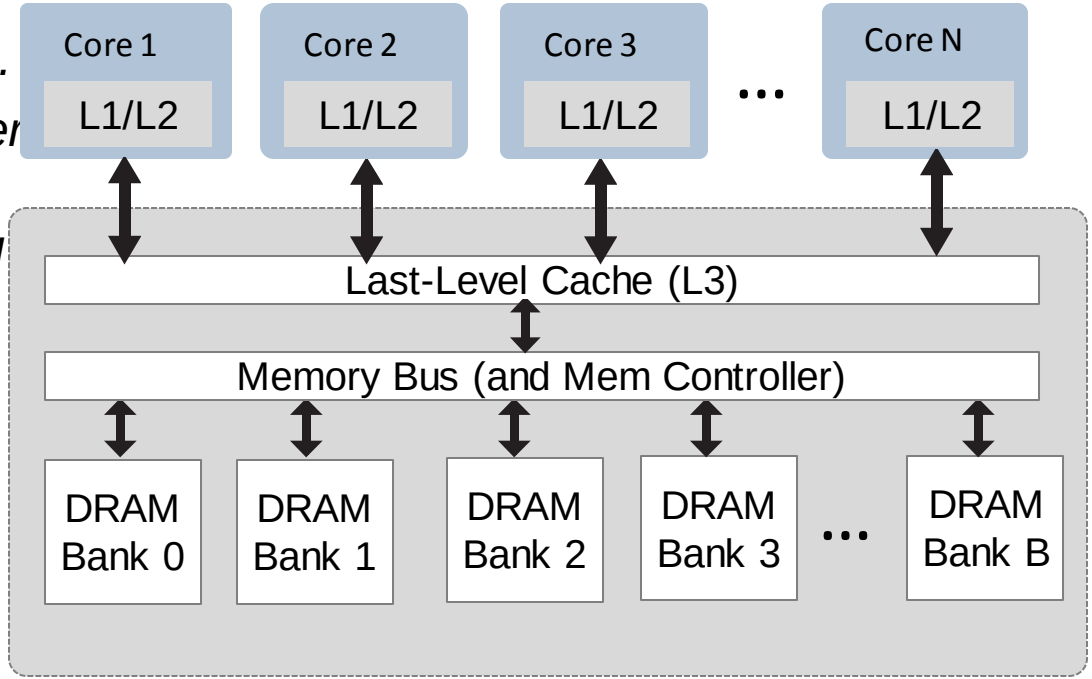


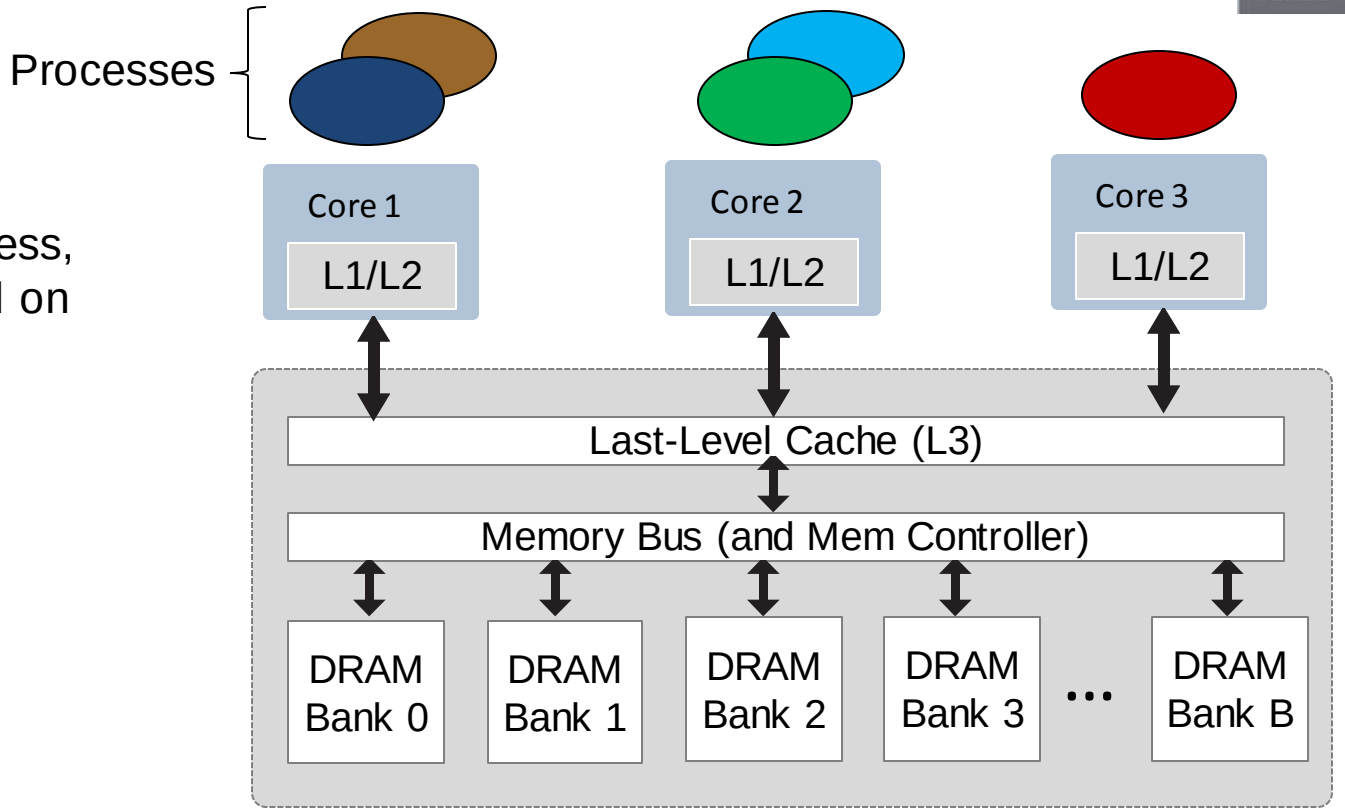
# Real-Time Requirements of Software Executing on a Multicore Processor

## Hardware Trends

- *All computers are multicores.*
- *Most chip makers do not offer single core.*
- *Most multicores have shared memory.*



**Problem:** For each process, compute an upper bound on its response time.



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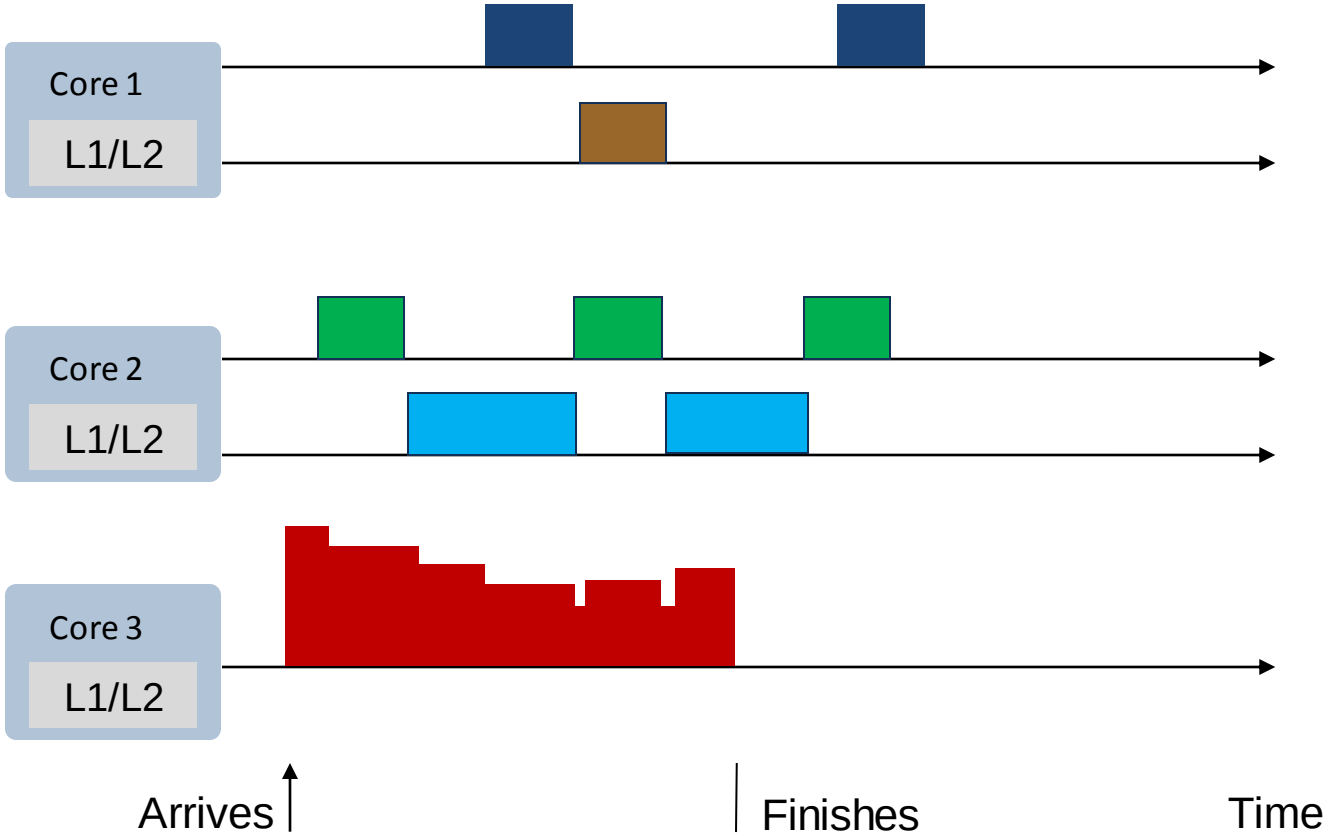

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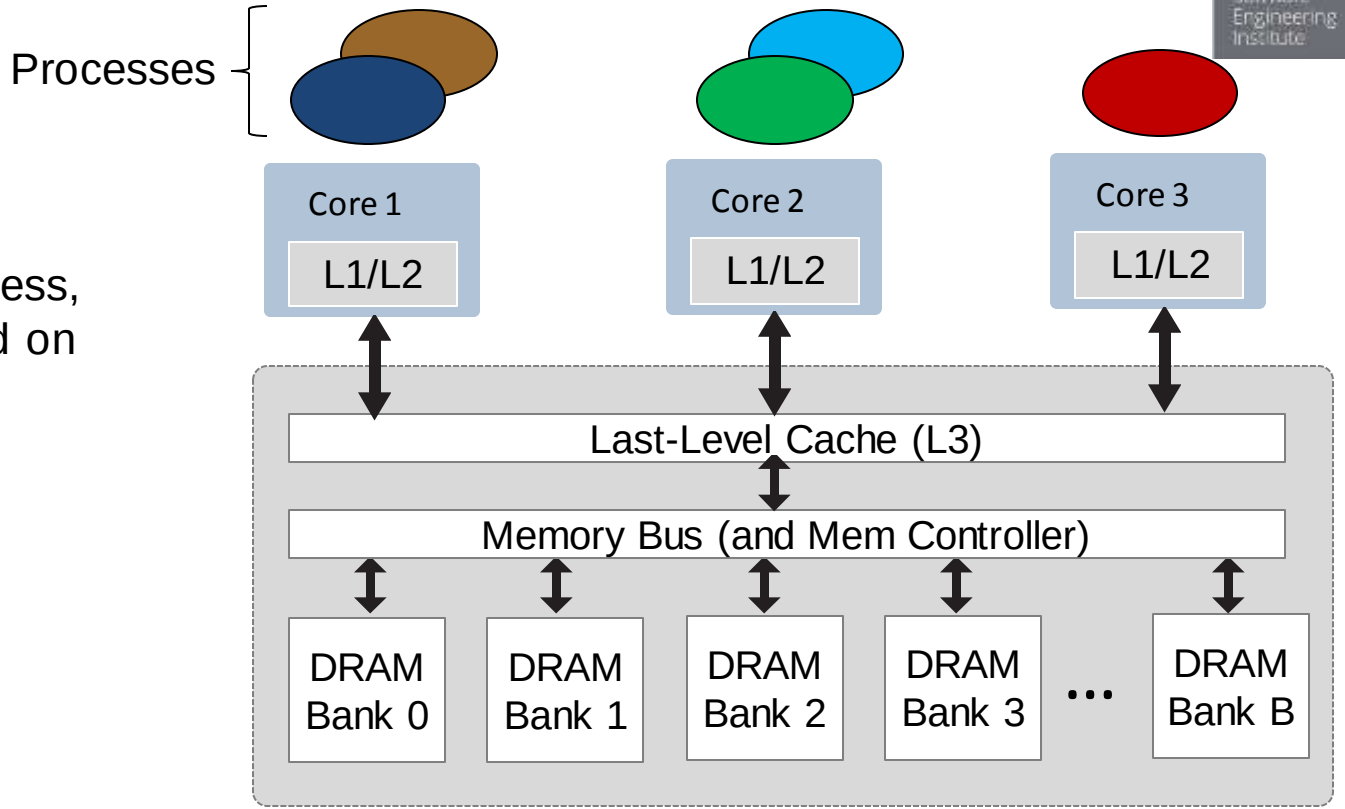
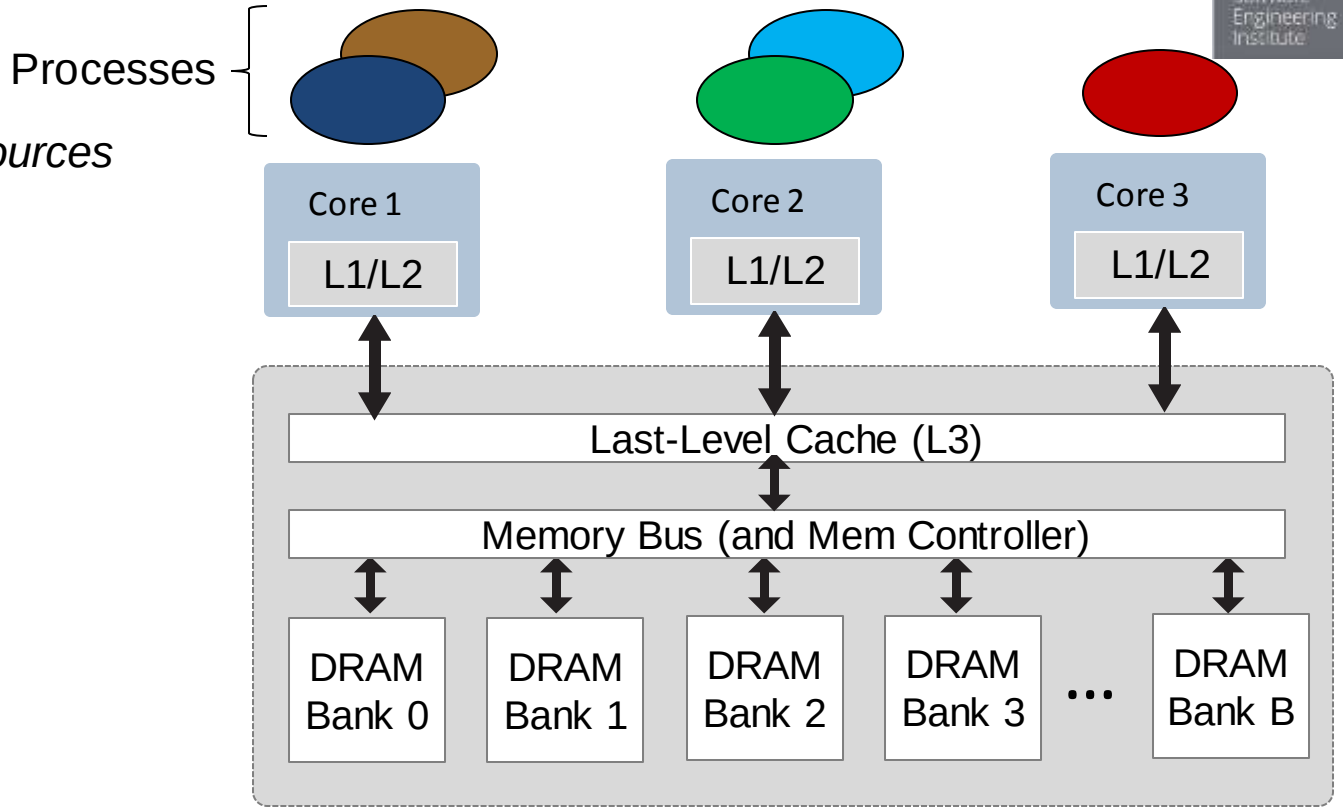


Issues

- *Shared hardware resources impact timing.*



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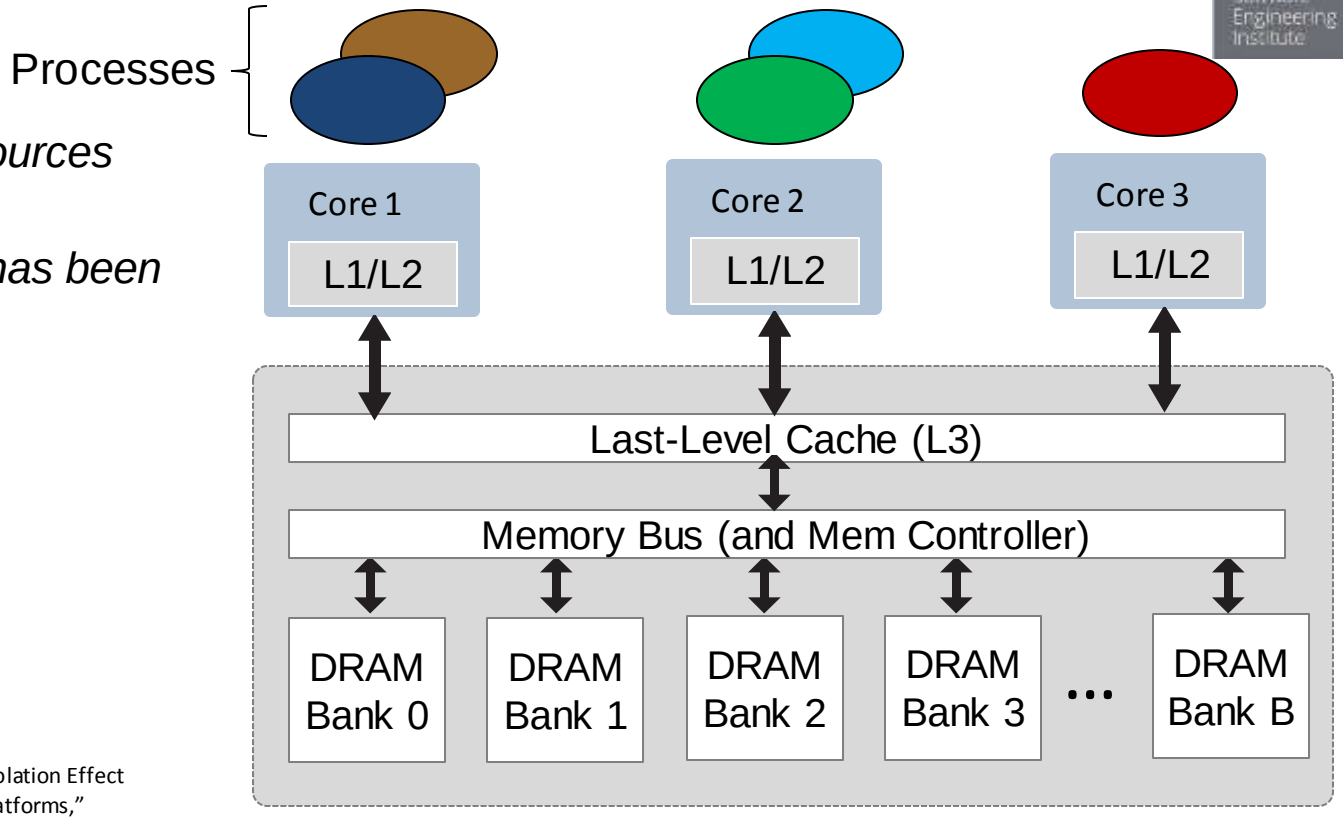
## Issues

- *Shared hardware resources impact timing.*
- *103 times slowdown has been observed.**




*H. Yun and P. K. Valsan, "Evaluating the Isolation Effect of Cache Partitioning on COTS Multicore Platforms," OSPERT, 2015.

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- *Shared hardware resources impact timing.*
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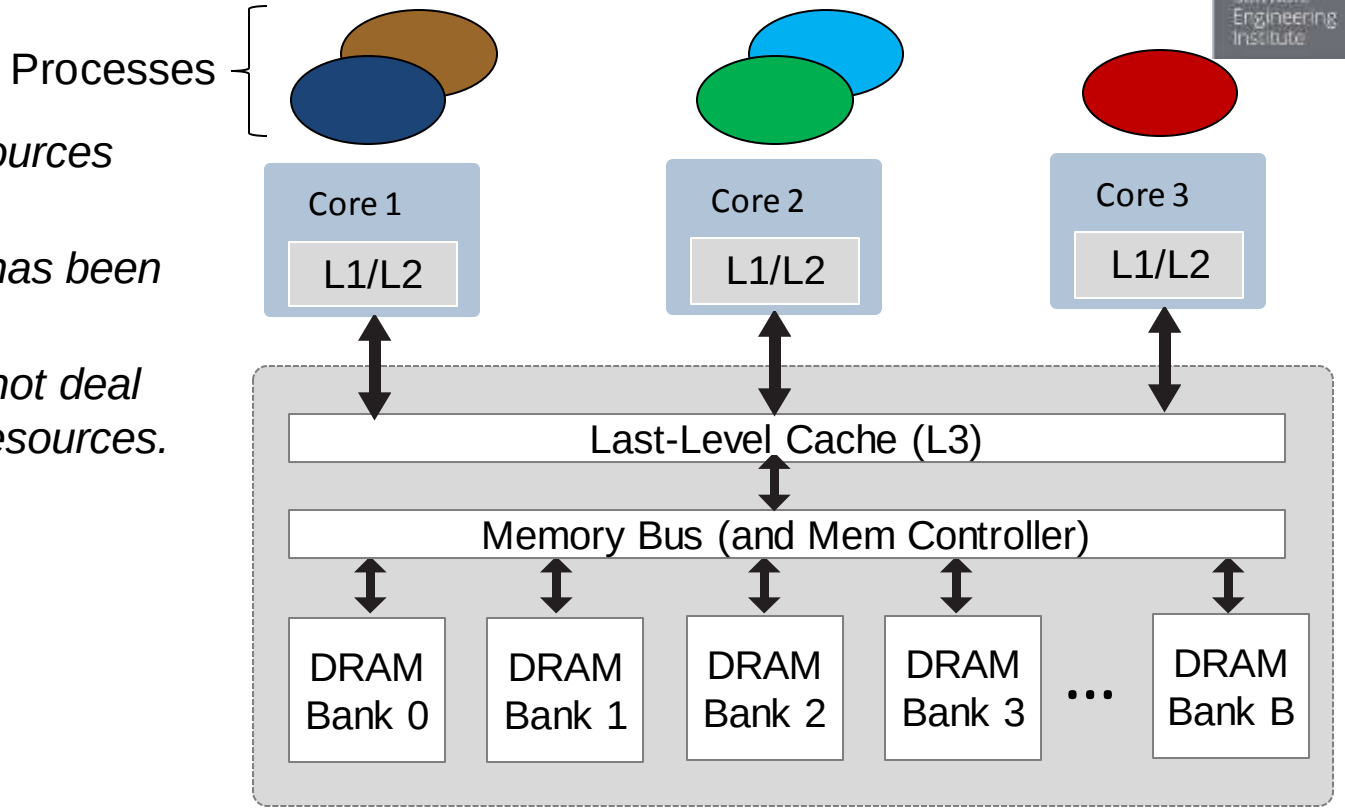
- *Current methods cannot deal with undocumented resources.*



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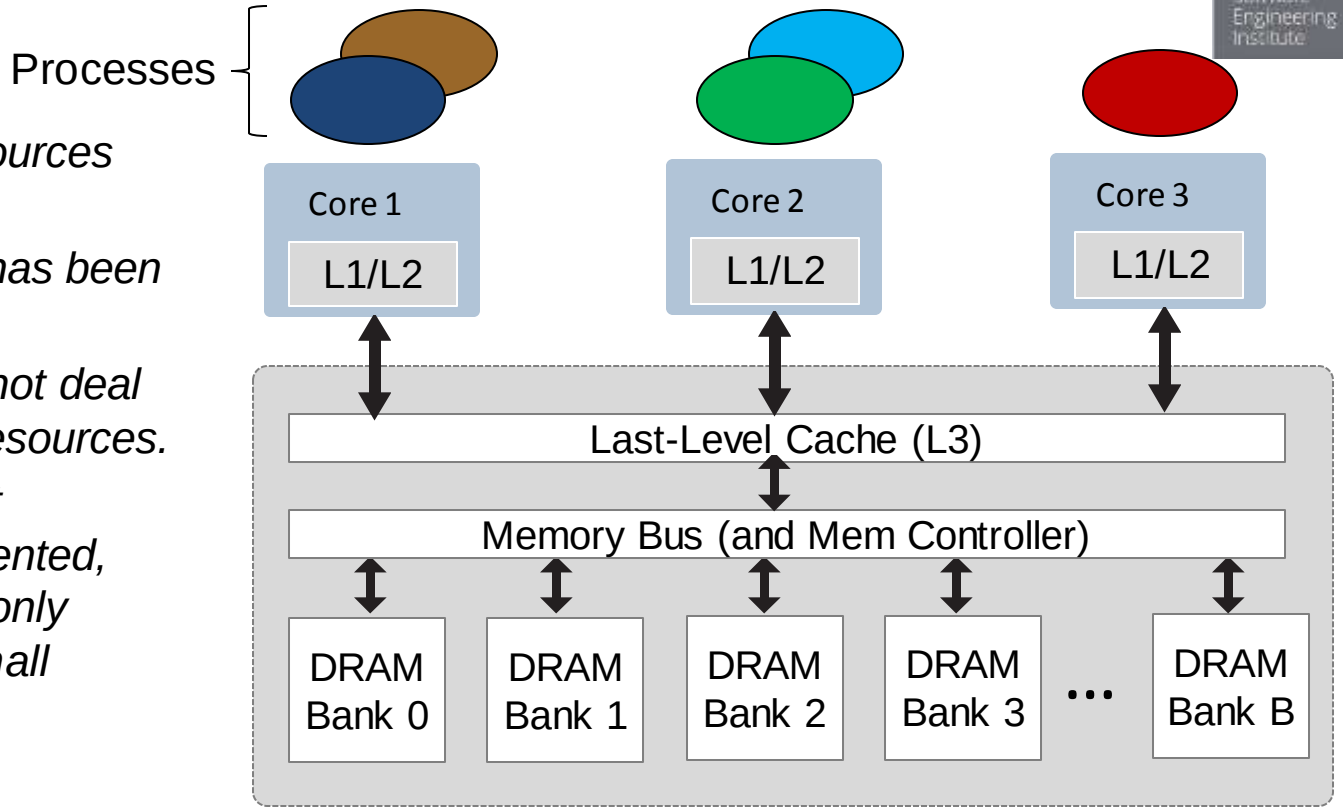

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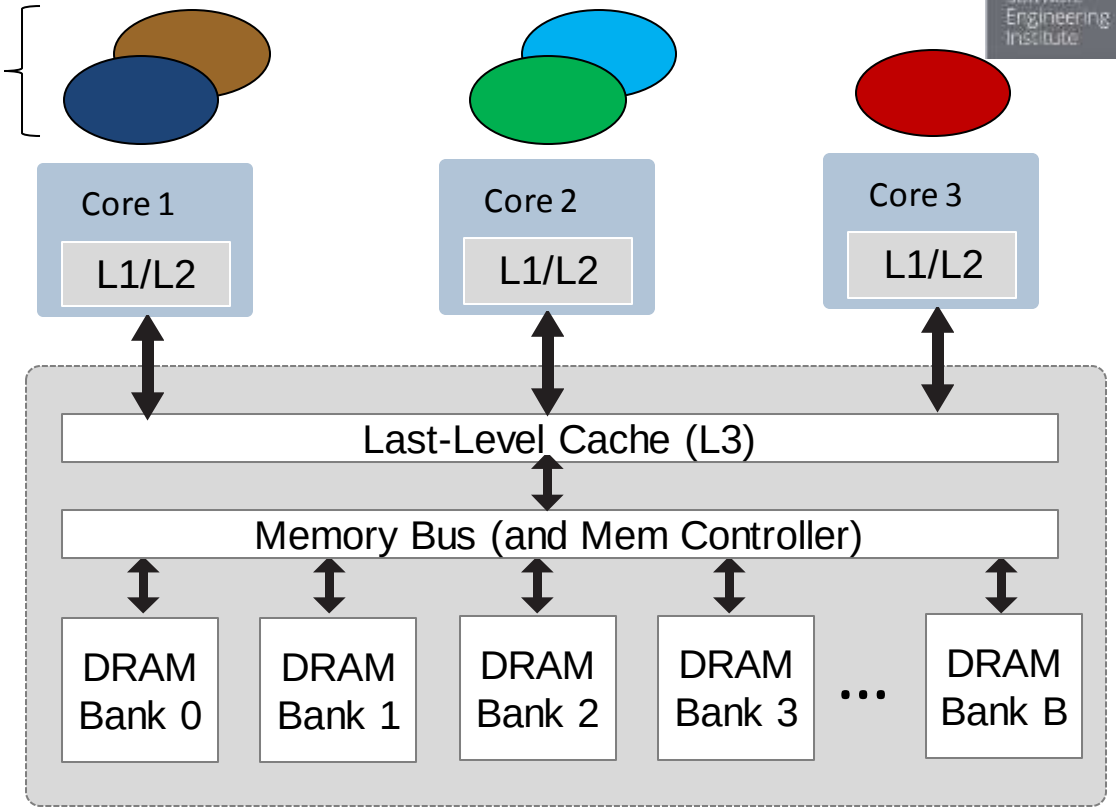

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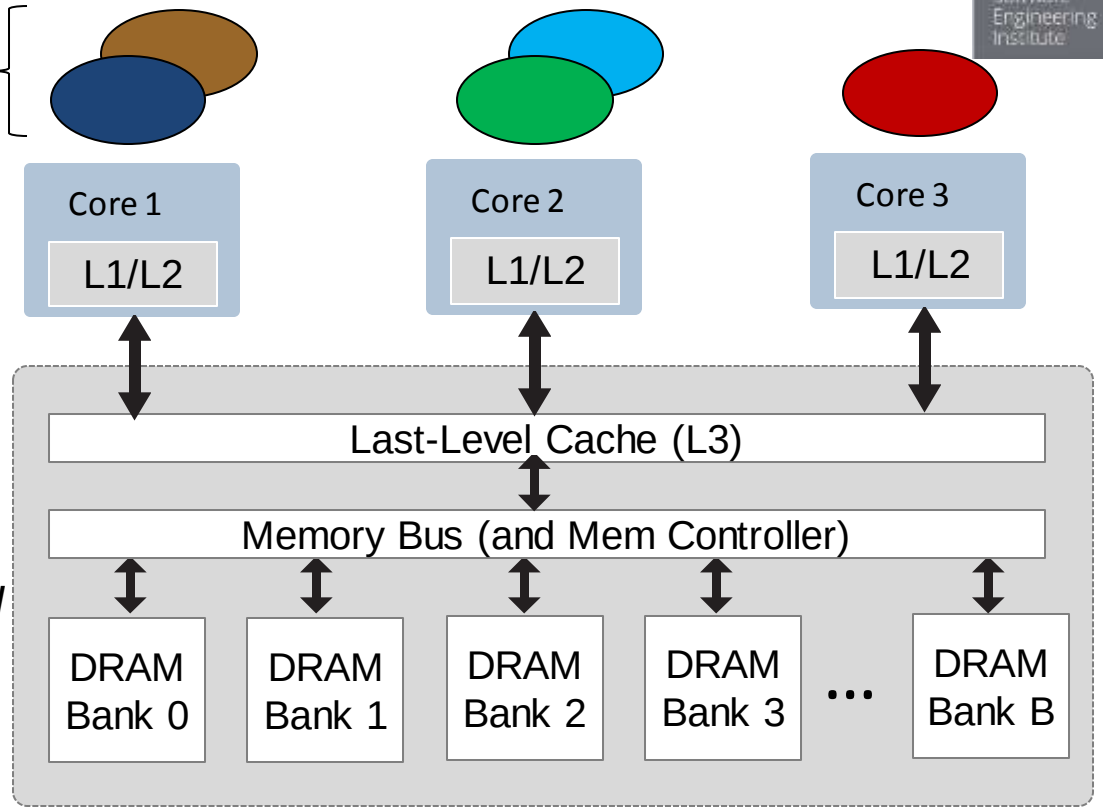


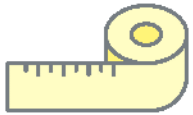

We need a new method to compute response times of processes.

# Project Objective

Many real-time systems within the DoD have all processor cores except one disabled in order to be confident about timing.

Therefore, the objective of this project is to develop a solution to overcome this obstacle.

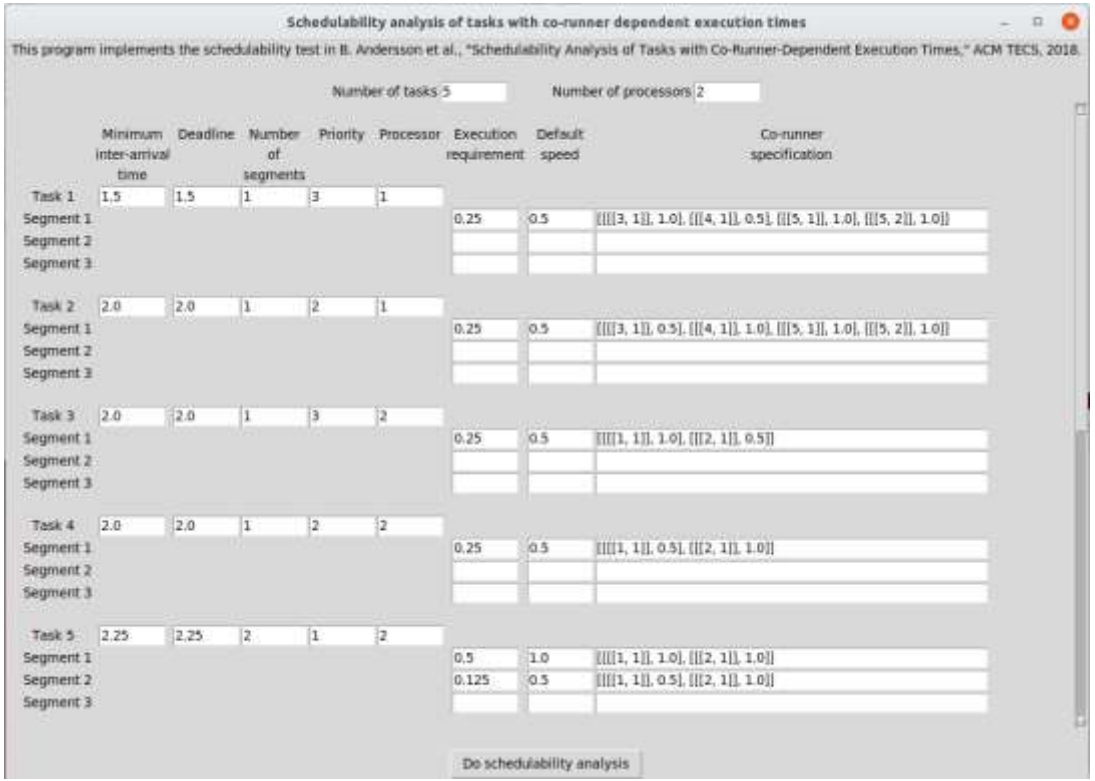
New verification procedure



Method to obtain abstractions

Configuration

# A Look at Our Analysis Tools - 1



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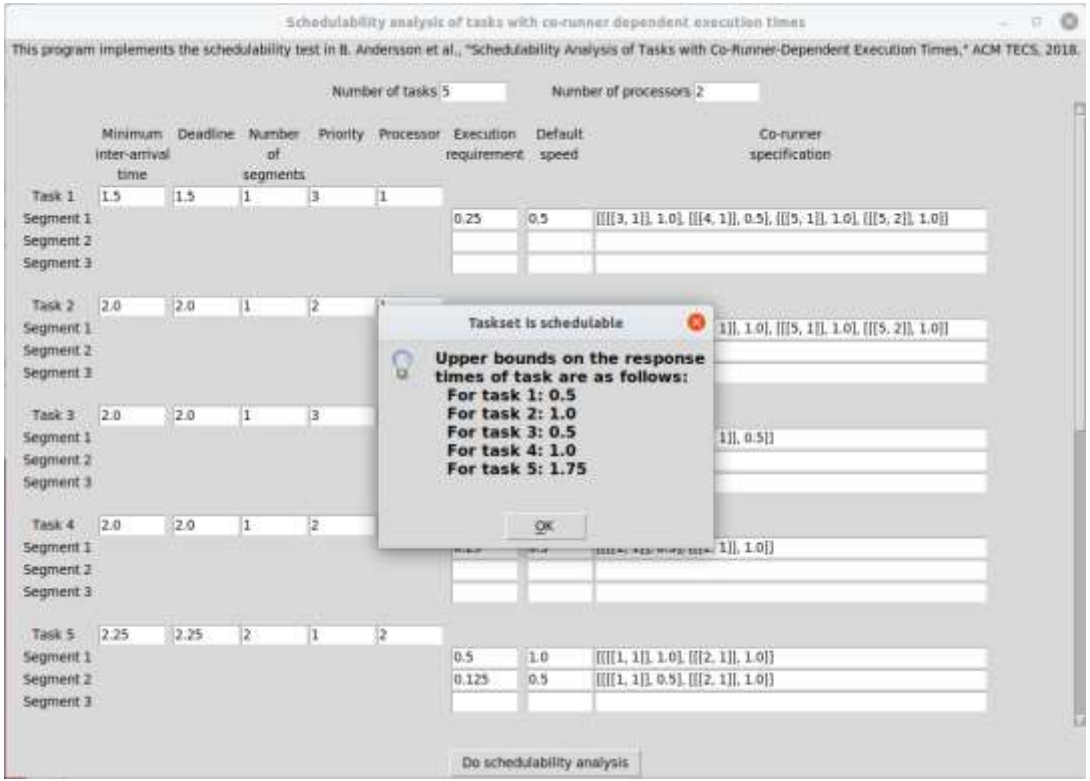

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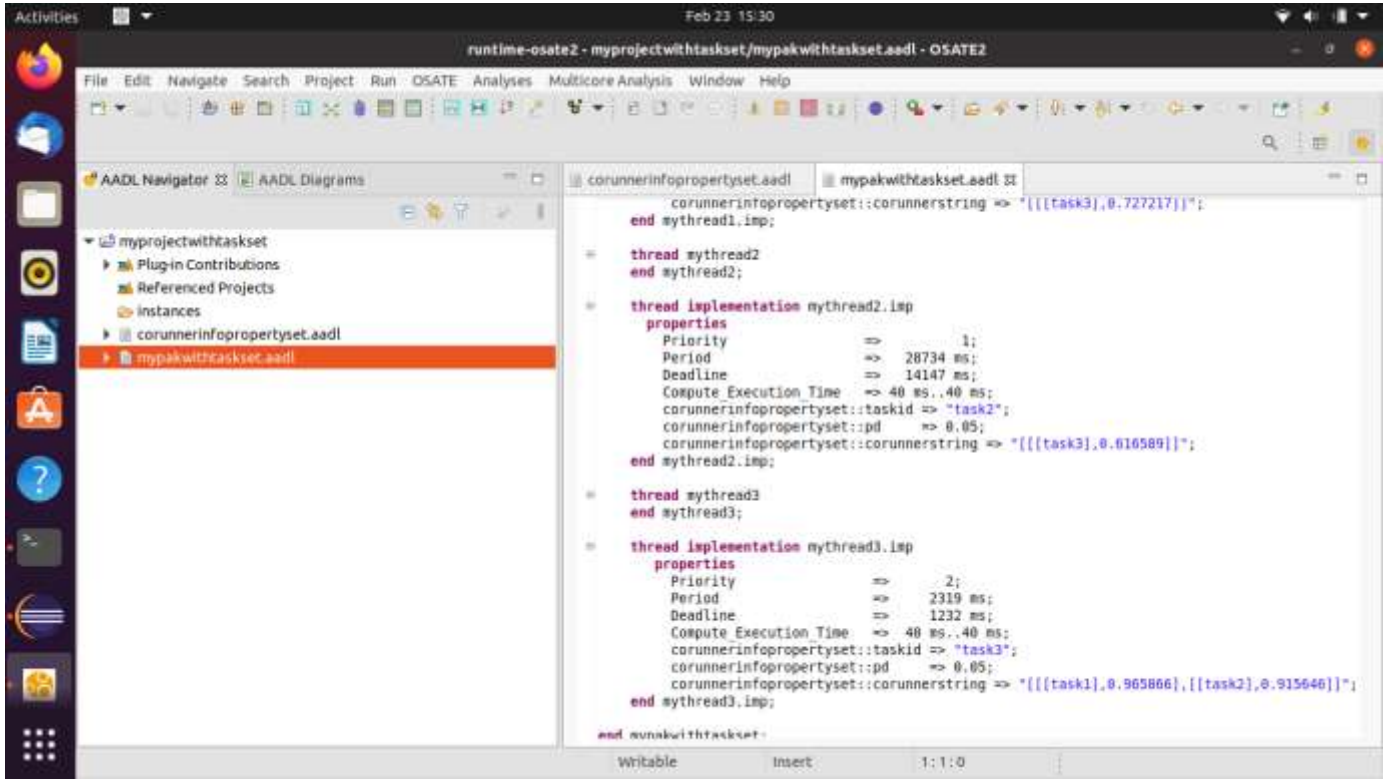

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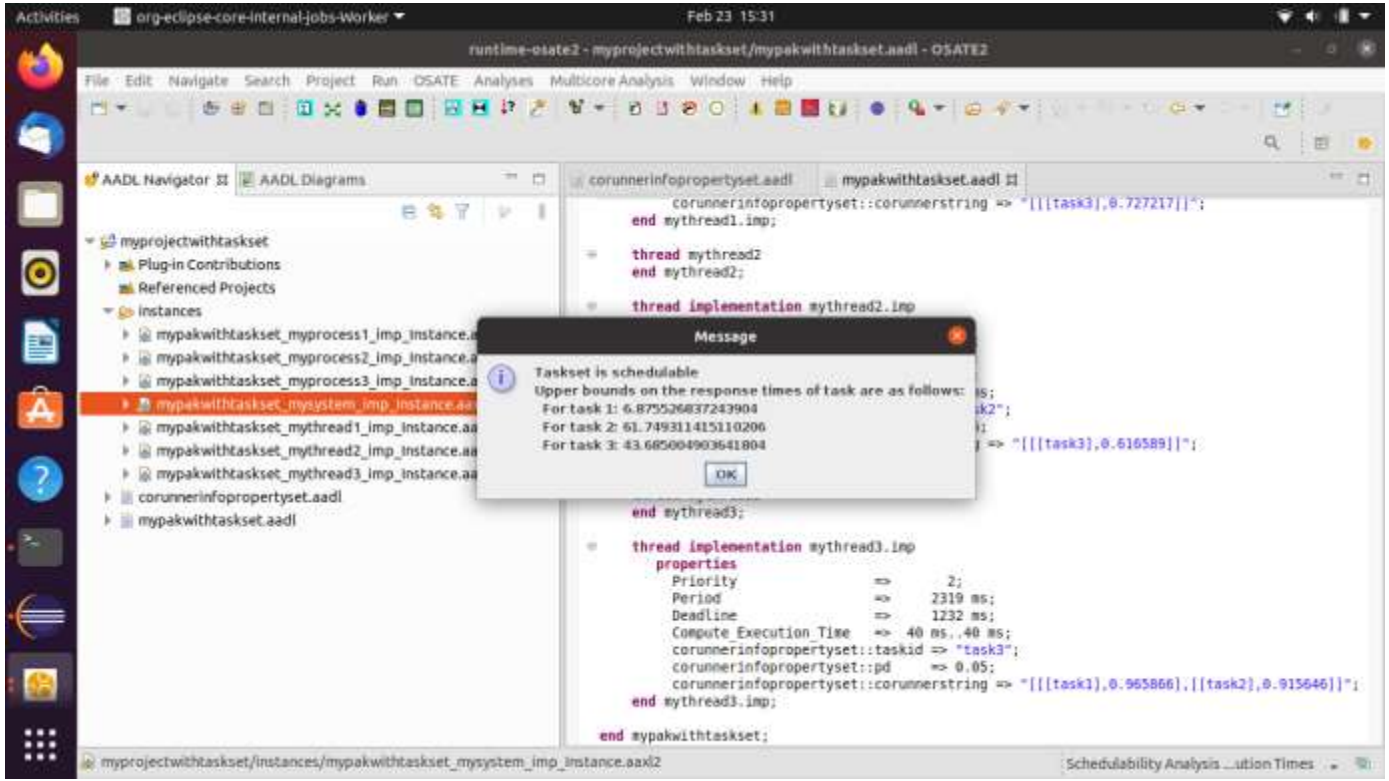
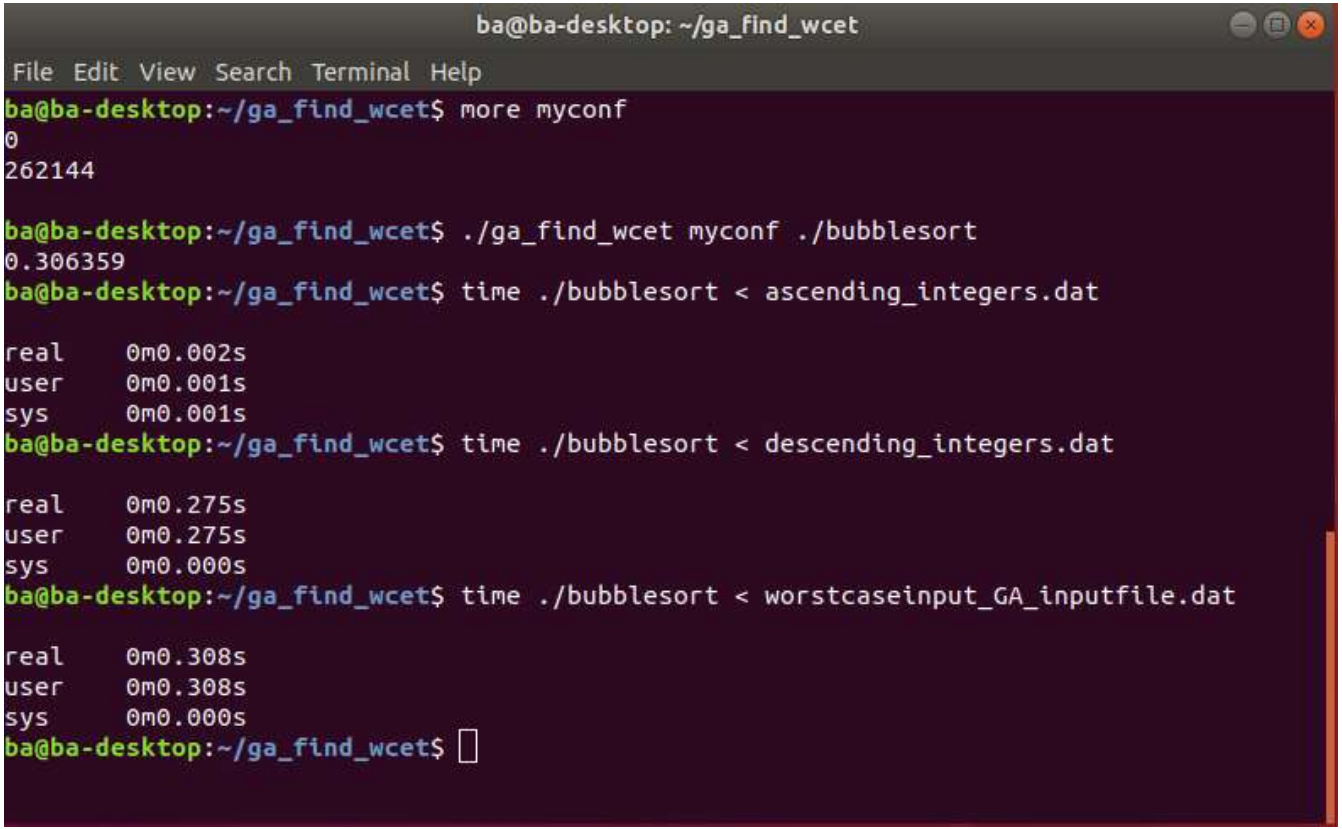


# A Look at Our Analysis Tools - 5



# Publications

B. Andersson, H. Kim, D. de Niz, M. Klein, R. (Raj) Rajkumar, and J. Lehoczky, "Schedulability Analysis of Tasks with Co-Runner-Dependent Execution Times, " ACM Transactions on Embedded Computing Systems, Vol. 17, No. 3, Article 71. May 2018.

B. Andersson, D. de Niz, and M. Klein, "The Multicore Challenge in Assured Autonomy," AUVSI Exponential 2021.

H. Kim, D. de Niz, B. Andersson, M. Klein and J. Lehoczky, "Addressing Multi-Core Timing Interference using Co-Runner Locking," IEEE Real-Time Systems Symposium, 2021.

V. Petrucci, B. Andersson, E. Massa, G. Lima, "Heterogeneous Quasi-Partitioned Scheduling," IEEE Real-Time Systems Symposium, 2021.

# Tools

http://www.andrew.cmu.edu/user/banderss/projects.html

# Team Photos

**Bjorn Andersson (SEI/CMU)**

**Dionisio de Niz (SEI/CMU)**

**Mark Klein (SEI/CMU)**

**John Lehoczky (CMU)**

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**Bill Anderson (SEI/CMU)**

**Anton Dimov Hristozov (SEI/CMU)**

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# Thanks!