40 Gb/s Autonomous Optical Packet Synchronizer

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Abstract: We demonstrate a 40Gb/s autonomous optical packet synchronizer with a resolution of 853ps and dynamic tuning range of 12.8ns. Layer-1 (BER) and Layer-2 (Packet Recovery) measurements are presented with > 15dB input power dynamic range.

OCIS Codes: (060.2330) Fiber optics communications, (060.4250) Networks

1. Introduction

All-optical packet switching provides a means of communications that has the potential to address issues in scaling to high-capacity electronic routers including footprint and power consumption [1]. In optical packet switches data is no longer processed at the bit-level but rather the packet level. The synchronizer presented in this paper is designed for optical switch architectures where the payload data is maintained in the optical domain while forwarding and routing information is extracted in the electronic domain. This is beneficial in the fact that although electronics are still used in the control plane, control signals at much lower frequency can be utilized which can reduce power consumption. In a real scalable packet network, packet switches must operate asynchronously [2]. Due to asynchronous operation and inter-node transmission length differences, packets arriving at a switch will be misaligned with the local clock and each other. It is thus advantageous to synchronize packets in time to the local clock for efficient switching and time management.

Previously, optical packet synchronizers have been proposed and demonstrated utilizing either wavelength conversion or semiconductor optical amplifier (SOA) based switches [3, 4]. While the former helps minimize the number of active components required the latter is more compact and amenable to integration. Integrated SOA based switches have been shown to operate at 40Gb/s with high extinction, low crosstalk, and fast switching times [5]. Also, synchronization using cascaded 1x2 integrated SOA switches with fiber delay lines has been demonstrated at a lower bit rate [6]. Further integration can be achieved through the use of low-loss silica delay lines or hybrid silicon technology which can reduce the footprint [7].

In this paper, we have successfully demonstrated dynamic synchronization of 40Gb/s packets by employing an optical packet synchronizer based on SOA switches, optical delay lines, and an asynchronous packet arrival time recovery circuit called a payload envelope detector (PED) [8]. Layer-1 (BER) measurements are presented with less than 0.5dB of power penalty and greater than 15dB of input power dynamic range. In order to test the dynamic capabilities of the synchronizer, a data stream of 40 byte packets at 40Gb/s is engineered to simulate asynchronous arrival and test all possible synchronizer states. Packets are aligned to the local clock within 853ps and are dynamically tuned over a range of 12.8ns. Layer-2 (packet recovery) results are presented for various input powers and dynamic error free performance is achieved for all states of the synchronizer.

2. Synchronizer Design

The synchronizer is based on a feed-forward design that utilizes SOAs and optical delay lines as depicted in Fig. 1. While the demonstrated synchronizer was constructed using discrete components, it is amenable to implementation using integrated waveguide delays. A combination of SOAs was used as the gates to select the packet delay and compensate for losses. In order to suppress accumulated amplified spontaneous emission (ASE), a band pass filter with a bandwidth of 2.4nm was placed at the output of the synchronizer. The attenuators were tuned so that the insertion losses for the various paths were as close as possible with the average and standard deviation equaling 3.43 and 0.22dB respectively. The tuning range was chosen to match the period of the local clock running at 78.125MHz equivalent to a period of 12.8ns. A four stage synchronizer design was used to provide a small enough resolution to compensate for the rise and fall times of the SOAs. Therefore, the relative delay through any configuration of the synchronizer can be given as $T(n) = n \times \Delta$ ($n = 0, 1, 2 \ldots 15$), where $\Delta = 853$ps and the tuning range is 12.8ns.

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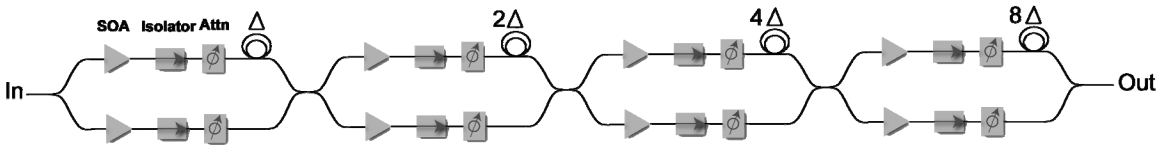


Fig. 1. Schematic of synchronizer

3. Experimental Implementation and Performance Measurements

Bit error rate measurements (BERs) were measured for a range of input powers into the synchronizer using PRBS 2^{31}-1 RZ data at 40Gb/s. Fig 2(a) shows BER plots at an input power of -7dBm into the synchronizer for n = 0, 5, 10 and 15. The power penalty is minimal and neither noise nor saturation is a major limitation for this set of operating conditions. Dynamic range measurements were taken by varying the input power into the synchronizer and the results are plotted in Fig. 2(b). Low input powers resulted in an increase in power penalty due to a degraded optical signal to noise ratio (OSNR). As the power is increased the power penalty reaches a minimum. For high input powers, saturation distorts the signal as well as decreases the gain of the SOAs which results in an increased power penalty. The offset in the dynamic range curves can be attributed to a misbalance of gain and loss for the various paths. Nonetheless, a dynamic range > 15dB was achieved for the different delays of the synchronizer.

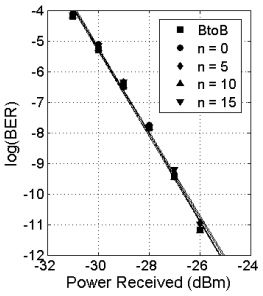
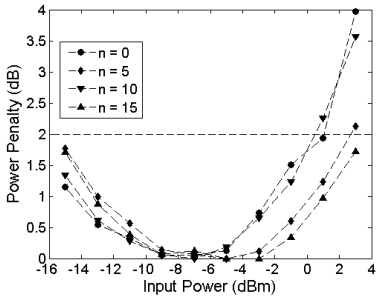
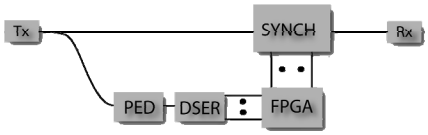


Fig. 2 (a) BER w/ Pin = -7 dBm



(b) Dynamic Range Measurement



(c) Experimental Setup

The experimental setup designed to test the dynamic tuning capabilities of the synchronizer is depicted in Fig. 2(c). In this experiment, 40 byte RZ packets at 40Gb/s are used as the data. The data stream is engineered to test all states of the synchronizer. The data stream consists of 16 packets where each packet is spaced by T (n) = 102.4ns + n x Δ (n = 0, 1, 2 … 15) and the total period equals 2.048μs. Packets with n = 0, 5, 10 and 15 and the 78.125MHz local clock are depicted in Fig. 3(a). Here the relative skew between the local clock and the transmitted packets can be clearly seen. The transmitted signal is tapped for electronic control processing. The payload envelope detector (PED) is used to detect incoming packets and generate packet envelopes. The PED consists of a 10GHz photo detector followed by a 2.5GHz limiting amplifier. The envelopes enter a 1:16 deserializer board operating at 10GHz which allows the rising edge of the packet to be sampled within 100ps. The deserialized envelope enters an FPGA based board where it is further deserialized from 16:128 channels so that it can be processed in parallel by the 78.125MHz local clock. In this experiment, the 10GHz and 78.125MHz clocks were derived from the transmitter to avoid the use of high speed clock recovery circuits which would be necessary if the control plane and transmitter were operated asynchronously. Here 16 channels of the deserialized data are used which correspond to the delays of the synchronizer. The deserialized data is compared to the rising edge of local clock to determine the delay needed to align the packet to the clock. The FPGA generates SOA control signals which correspond to the delay determined to synchronize the packet. If no envelope is detected then the FPGA sets the control signals corresponding to a delay of T (0). This default state is especially important when the rising edge of the envelope and clock overlap and the logic is in a state of hysteresis. The control signals are expanded to 38.4ns through SR latches in order to gate the packets. The signals are then latched through D flip flops in order to match the total delay of each stage of the synchronizer. The control signals are then fed into voltage to current converter boards which drive the SOAs. Thereby the packets are delayed accordingly and aligned to the local clock within 853ps as can be seen in Fig. 3(c).

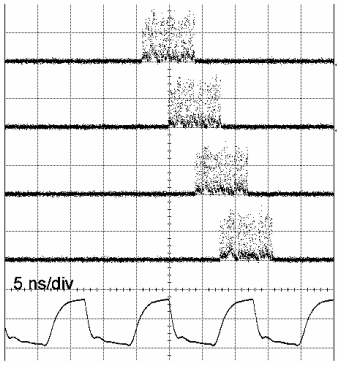
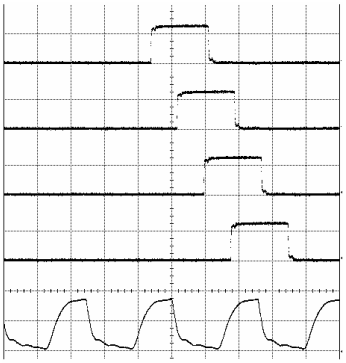
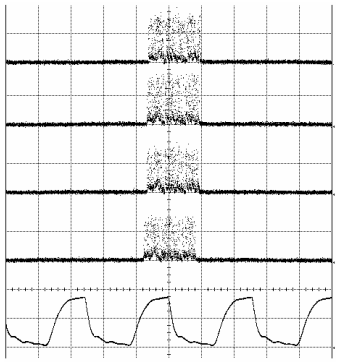


Fig. 3(a) Packets at synchronizer input



(b) Recovered payload envelopes



(c) Packets at synchronizer output

Layer-2 (packet recovery) measurements were conducted at various input powers for n = 0, 5, 10 and 15. Fig. 4(a) shows results at low input power (-24dBm). The signal is slightly degraded due to accumulated noise. Fig. 4(b) shows results at an optimal input power (-19dBm). The power penalty is less than 1dB at this input power because neither noise nor saturation is a significant problem. Fig. 4(c) shows results at high input power (-4dBm). Saturation causes the gain to decrease in the SOAs as well as distorts the signal which leads to low signal quality. Nonetheless, the synchronizer offers a large dynamic range, which makes it suitable for an optical packet switch.

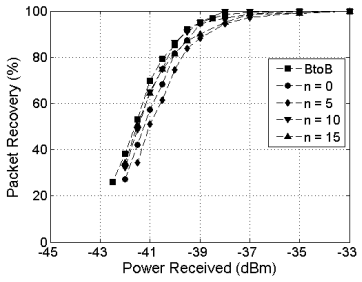
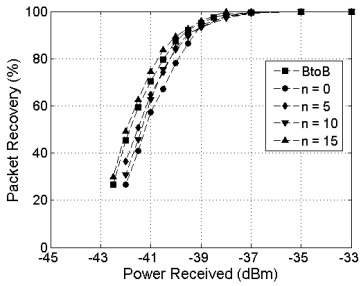
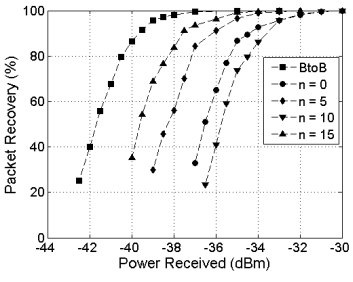


Fig. 4(a) Packet recovery at Pin= -24dBm



(b) Packet recovery at Pin= -19dBm



(c) Packet recovery at Pin= -4dBm

4. Summary

An optical packet synchronizer is demonstrated operating at 40Gb/s with less than 0.5dB of power penalty and greater than 15dB input power dynamic range. Dynamic synchronization of 16 packets within a data stream engineered to test all states of the synchronizer is achieved with a resolution of 853ps and dynamic tuning range of 12.8ns.

5. Acknowledgement

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6. References

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