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Thermal Mechanical Investigation of Ultra Wide Bandgap Materials and Devices

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14. ABSTRACT
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Project Overview

Research and development of ultra-wide bandgap (UWBG) semiconductor devices are underway to realize next-generation military power conversion and wireless communication systems. Devices based on β-phase gallium oxide (β-Ga_2O_3), aluminum gallium nitride ($Al_xGa_{1-x}N$, x is the Al composition), and diamond give promise to the development of power switching devices and radio frequency (RF) power amplifiers with higher performance and efficiency than today's commercial wide bandgap semiconductor devices based on gallium nitride (GaN) and silicon carbide (SiC). However, one of the most critical challenges for the successful deployment of UWBG device technologies is to overcome adverse thermal effects that impact the device performance and reliability. Overheating of UWBG devices originates from the targeted high power density operation and the poor intrinsic thermal properties of $Al_xGa_{1-x}N$ and β-Ga_2O_3. This report delineates the need and process for the electro-thermal co-design of UWBG electronic devices. Device electro-thermal modeling and thermal characterization techniques developed in this work are reviewed. In addition, early efforts on the design of device-level thermal management solutions are reported.

Summary of Research Findings

I. Introduction to the UWBG Semiconductors

Until the late 1980s, the mainstream semiconductor materials for power and radio frequency (RF) applications were Si, Ge, and conventional group III-V compound semiconductors such as GaAs and InP. Currently, wide bandgap (WBG) semiconductors GaN and SiC are used as the base material for advanced power and RF electronics[1–3]. As GaN and SiC technologies move closer to maturity, these devices are approaching the theoretical limit of the achievable performance, which is dictated by their fundamental material properties including the critical electric field. Accordingly, to meet the demanding requirements for higher power/frequency military applications, device engineers are pursuing the development of next-frontier devices based on ultra-wide bandgap (UWBG) semiconductors $Al_xGa_{1-x}N$, β-Ga_2O_3, and diamond.[4–6]

A number of figures of merit (FOMs) are often used to evaluate the relative merits of a particular semiconductor material for use in RF and power electronics. UWBG materials generally show an increased FOM over lower bandgap semiconductors. The Johnson figure of merit

(JFOM)[7] is often used to compare the potential of materials for building high-frequency transistors. The JFOM is defined as $JFOM = V_{BR}f_T$, where V_{BR} is the breakdown voltage and f_T is the unity gain cutoff frequency. The JFOM can also be expressed as $v_{sat}E_C$, where v_{sat} and E_C are the saturated carrier velocity and critical electric field, respectively. Table I shows that the JFOMs of $Al_xGa_{1-x}N$ and β-Ga_2O_3 surpass those for WBG materials, and diamond exhibits a JFOM comparable to GaN. Therefore, these UWBG materials offer the potential for the development of next-generation RF power amplifiers.

On the other hand, the lateral figure of merit (LFOM)[8] is a metric that compares the theoretically achievable switching performance of laterally-configured transistor devices. It is defined as $LFOM = V_{BR}^2/R_{ON,SP}$, where $R_{ON,SP}$ is the specific ON-resistance. Accounting for the lateral device geometry, the LFOM can also be expressed as $q\mu n_s E_C^2$, where q is the electron charge, μ is the channel mobility, and n_s is the sheet charge density. The LFOM is analogous to the conventional Baliga figure of merit (BFOM)[9,10] applicable to unipolar vertical power switches. The LFOMs in **Table I** for UWBG devices are calculated based on mobility values currently reported in literature for early-stage devices. Even in premature stages, UWBG devices have LFOMs approaching or greater than established GaN devices. The high LFOMs offered by the UWBG materials give promise to the development of lateral power switches with kV-range breakdown voltages and minimized device footprints.

Table I. *Material properties and figures of merit for conventional, WBG, and UWBG semiconductors. Data were adopted from references [6,11–18]. The LFOM calculation (normalized with respect to Si) assumes $n_s=10^{13}$ cm^{-2} and uses reported device channel mobilities. For diamond, the mobility and saturation velocity for holes are listed.*

Property	Conventional		WBG		UWBG		
	Si	GaAs	SiC	GaN	$Al_{0.85}Ga_{0.15}N$	β-Ga_2O_3	Diamond
Bandgap, E_G (eV)	1.12	1.43	3.26	3.42	5.61	4.8	5.47
Relative dielectric constant, ε	11.9	13.1	10.1	9.7	8.68	10	5.7
Breakdown field, E_C (MV/cm)	0.3	0.4	3	3.3	10.7	8	10
Carrier (channel) mobility μ (cm^2/Vs)	1400	8500	1020	1350(2000)	45(250)	200(180)	3800(69)
Carrier saturation velocity, v_{sat} (cm/s)	1×10^7	2×10^7	2×10^7	2.7×10^7	2.28×10^7	1.5×10^7	0.8×10^7
Thermal conductivity, k (W/mK)	150	46	490	130	8.5	11-27	2400
Normalized JFOM ($v_{sat}E_C$)	1	2.7	20	30	81	40	27
Normalized LFOM ($q\mu n_s E_C^2$)	1	11	73	170	230	100	55

The enhancement in the device-level performance according to the superior JFOM and LFOM translates into commensurate improvement in system-level size, weight, and power (SWaP) and efficiency. In particular, β-Ga_2O_3 offers the potential to address the cost performance trade-off for established WBG semiconductors by providing lower-cost melt-grown wafers and the higher performance suggested by the FOMs.[19] These advantages can be leveraged to improve power efficiency gains of military radar and satellite communication systems, and to build lighter and more efficient power conversion systems for electrified ground vehicles, aircrafts, and all-electric ships.

II. Representative UWBG Devices in Lateral Configurations

UWBG device technologies for laterally-configured devices are relatively more mature than vertical devices. For this reason, the electro-thermal co-design of laterally-configured UWBG devices was mainly investigated in this project. Nevertheless, it should be noted that active

research on the development of vertically oriented power transistors[20] and diodes[21–23] for applications that demand extreme voltage (>1 kV) and current levels (>100 A) are underway.

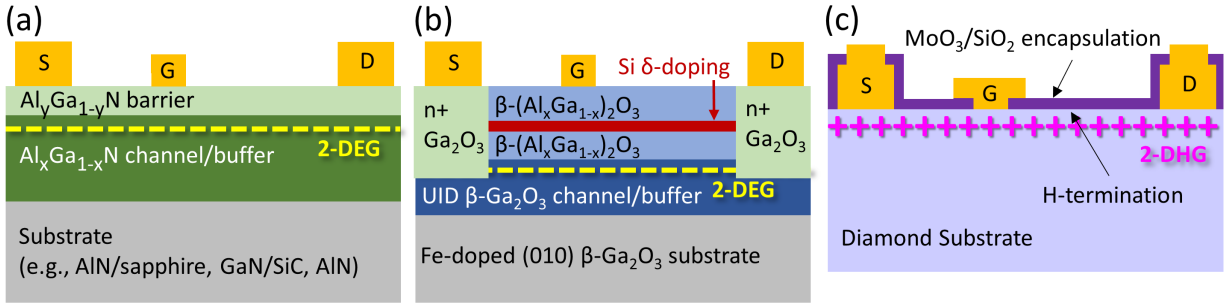

Figure 1. *Schematic epitaxial structures of (a) an $Al_xGa_{1-x}N$-channel HEMT, (b) a β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ MODFET, and (c) an H-terminated diamond FET.*

$Al_xGa_{1-x}N$: The bandgap energy, E_G, of $Al_xGa_{1-x}N$ peaks at 6.2 eV (x=1)[24], which results in the largest breakdown field (15.4 MV/cm)[10] among all the UWBG semiconductors listed in **Table I**. Moreover, the piezoelectric nature of the material allows for the fabrication of a high electron mobility transistor (HEMT) structure[25], which offers high electron sheet density (>10^{13} cm^{-2}) and mobility without impurity doping. A typical $Al_xGa_{1-x}N$-channel HEMT structure[26] is shown in **Figure 1 (a)**. Briefly, a 1-4 µm thick $Al_xGa_{1-x}N$ channel/buffer layer is heteroepitaxially grown on a non-native substrate such as AlN/sapphire[12,27,28] templates, GaN/SiC[29] templates, and AlN[30,31]. Subsequently, a thin (~20 nm) higher Al-content $Al_yGa_{1-y}N$ (y~x+0.15) barrier layer is grown over the $Al_xGa_{1-x}N$ channel. The $Al_yGa_{1-y}N/Al_xGa_{1-x}N$ heterointerface physically governs the device behavior through the formation of a polarization-doped two-dimensional electron gas (2DEG)[25]. It should be noted that the $Al_xGa_{1-x}N$ system can readily take advantage of the global manufacturing infrastructure associated with commercial InGaN LEDs, $Al_xGa_{1-x}N$-based ultra-violet LEDs[32], and GaN electronics.

β-Ga_2O_3: The primary advantage of β-Ga_2O_3 (E_G~4.8 eV)[16] over the other UWBG materials is that high crystalline quality substrates can be synthesized at low cost using melt growth techniques such as Czochralski and edge-defined film-fed growth, similar to the case of the melt-grown substrates that support ubiquitous Si devices.[33] While the intrinsic β-Ga_2O_3 material suffers from a relatively low bulk electron mobility[34,35], innovative device architectures such as the β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ modulation-doped field effect transistor (MODFET)[18,36,37] shown in **Figure 1 (b)** are being developed to overcome the room temperature mobility limitations arising from the strong Frölich interaction in β-Ga_2O_3.[38,39] A 2DEG channel is formed near the heterointerface via modulation doping, where electrons are transferred from a Si delta-doped region in the β-$(Al_xGa_{1-x})_2O_3$ barrier. Since the carriers are physically separated from the donor ions, scattering from the ionized impurities is greatly suppressed as well, enabling an overall higher electron mobility than earlier β-Ga_2O_3 lateral transistor structures (μ < 100 cm^2/Vs)[33].

Diamond: The favorable properties of diamond such as the large bandgap energy (E_G=5.47 eV), high critical electric field (8-10 MV/cm), high hole saturation velocity (0.8×10^7 cm/s), and the highest known thermal conductivity are listed in **Table I**.[6] The hydrogen (H)-terminated diamond field effect transistor (FET) achitecture[13] shown in **Figure 1 (c)**, along with the recent advances in diamond substrate synthesis by high-pressure-high-temperature (HPHT) and chemical vapor deposition (CVD) processes, gives promise to the establishment of diamond electronics

technologies. To circumvent difficulties in substitutional doping[6,40], the H-terminated diamond FET utilizes surface transfer doping[41]. Microwave hydrogen plasma treatment is used to achieve hydrogen termination of the diamond surface. The interaction between the H-terminated surface and adsorbed ions present in the atmosphere or an electron acceptor layer (e.g., MoO_3[42], V_2O_5[43]) results in energy band bending that creates a two-dimensional hole gas (2DHG) with a carrier density in excess of 10^{13} cm^{-2}. To improve the stability of the 2DHG channel, the device is passivated with a protective layer (e.g., hydrogen silsesquioxane (HSQ)[44], Al_2O_3[45], and SiO_2[46]).

III. Thermal Challenges

The high voltage/power operation and aggressive device scaling (i.e., reducing the device gate and channel lengths) enabled by the superior LFOMs of UWBG materials (**Table I**) will translate into extremely high-power densities within the active region (~1 MW/cm^2), which is even higher than that on the Sun's surface. However, the room temperature thermal conductivity of $Al_xGa_{1-x}N$ (<10 W/mK)[15] and β-Ga_2O_3 (anisotropic; 11-27 W/mK)[11] are the lowest among the technologically relevant semiconductor materials listed in **Table I**. The intended harsh operating conditions and poor thermal properties will result in excessive device self-heating unless proper thermal management solutions are implemented. Although the large bandgap energy may mitigate uncontrolled carrier conduction in the semiconductor caused by the increased thermal energy, the ohmic and gate contacts are not likely to withstand the extremely high channel temperatures.

Due to the excellent thermal conductivity of diamond, a misconception can arise that diamond electronics should be free of thermal issues. However, one of the largest challenges associated with H-terminated diamond FETs is the stability of the 2DHG channel at high temperatures or under harsh environmental conditions.[44,47] For instance, at temperatures beyond 200°C, the C-H bonds and/or the surface adsorbates were shown to be detrimentally impacted, resulting in an irreversible loss of the surface p-type conduction.[44]

Accordingly, device developers are recognizing that overheating is a major bottleneck to the success of the UWBG device technologies. In fact, no UWBG device reported to this day has achieved the performance expected by the superior JFOM/LFOM partly because a thermally limited technological plateau has been reached. It is necessary to engineer and reduce the junction-to-package thermal resistance of UWBG devices to a level comparable to or lower than today's WBG GaN and SiC counterparts to realize the targeted high power density operation.

IV. Electro-Thermal Co-Design

Traditionally, the design of power switching devices and RF power amplifiers has solely focused on maximizing the electrical performance by optimizing the epitaxial growth (e.g., AlGaN/GaN heterostructures) and improving device processing techniques (e.g., Ohmic contacts, field plate structures). Self-heating issues were indirectly recognized by the degradation of electrical performance[48] and their mitigation was considered to be an engineering problem that would result in de-rating of the device power output or improving the package-level design. However, as discussed above, UWBG devices are highly prone to overheating and thermal failure, with a minimal thermal margin to engineer. Current design practices, however, are often unable to accurately predict the thermal feedback caused by the power dissipation, leaving an incomplete model of the device performance and reliability. Such design practices may result in the development of less reliable components with degraded performance, both from an electrical and thermal/mechanical[49] standpoint. The need for electro-thermal co-design, which essentially means

thermal considerations are incorporated into the device design from the initial stage of the device development process, has already proven to be essential to exploit the full potential of GaN RF power amplifiers.[50]

The design of thermal management solutions for UWBG devices requires a physics-based model that accurately predicts the channel peak temperature rise under specified operating conditions. Creating such device thermal model requires the following electro-thermal co-design process. First, the physical properties that dictate the electronic and thermal transport within/across UWBG materials and interfaces must be accurately measured. Electrical characterization methods to determine electronic properties (e.g., carrier density, mobility, and saturation velocity) and device-specific electrical parameters (e.g., Ohmic contact resistance) are well established. However, thermal characterization methods suitable for measuring the thermo-physical properties of UWBG semiconductors are less accessible to device engineers and must be carefully chosen in real practices. Second, the device self-heating behavior in response to a specified voltage bias condition must be precisely estimated. This requires a 3D coupled electro-thermal modeling scheme that begins with solving for the charge transport and electrostatic potential within the semiconductor device. The Joule heat distribution derived from the electrical part of the coupled modeling scheme (2D simulation is sufficient for many devices)[51] is then imported into a 3D finite element thermal model that adopts the measured thermo-physical properties. The modeling output will be the device surface and internal temperature fields. Third, optical thermography techniques with sufficiently high spatial/temporal resolutions and measurement sensitivity are necessary to capture the physical processes associated with the unconventional characteristic length scales and operational environments (i.e., extreme heat flux, electric field, frequency) and to validate the multi-physics device model. Care must be exercised; respective techniques can easily have a factor of two disagreement in temperature rise where misinterpretation of the data may stem from the material selectivity and spatial resolution of each technique.[52–55] Finally, the validated device thermal model can be used for the design of device- and system-level passive and active thermal management solutions that locate the thermal heat sink as close as possible to the heat generation region (i.e., the device current channel). **Figure 2** illustrates the electro-thermal co-design process for UWBG semiconductor devices.

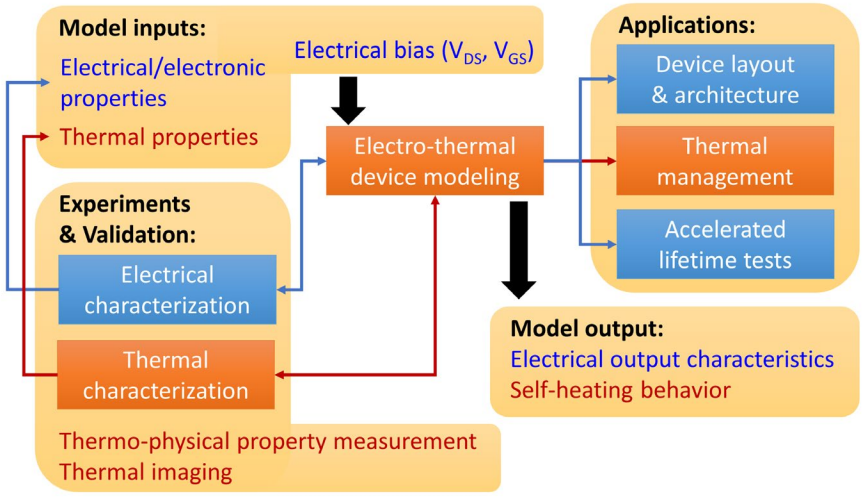

Figure 2. *Flow diagram of the device-level electro-thermal co-design process.*

1. Thermo-Physical Property Measurement

$Al_xGa_{1-x}N$: The $Al_xGa_{1-x}N$ structure can be viewed as a wurtzite phase GaN crystal with Al atoms randomly substituting the Ga cations within the group III cationic sub-lattice. Early reports[56–58] on the $Al_xGa_{1-x}N$ thermal conductivity show inconsistent results possibly due to the low quality of the tested materials and/or the low measurement sensitivity of the metrology techniques. Laser-based optical pump-probe techniques such as time-domain thermoreflectance (TDTR)[59] and frequency domain thermoreflectance (FDTR)[60] are ideal for the thermal conductivity measurement of $Al_xGa_{1-x}N$ and other UWBG thin films. TDTR and FDTR measurement results for ~1 μm thick metal organic chemical vapor deposition (MOCVD)-grown $Al_xGa_{1-x}N$ films are illustrated in **Figure 3 (a)**.[15] A remarkable reduction in the room temperature thermal conductivity with respect to the base GaN (x=0; the bulk value can reach beyond 200 W/mK[61–63]) and AlN (x=1; the bulk value can reach up to ~320 W/mK[64–66]) crystals is observed. The observed U-shaped trend is universal for ternary alloy semiconductors, which is a manifestation of phonon-alloy disorder scattering[67–69]. The low thermal conductivity of $Al_xGa_{1-x}N$ makes it challenging to dissipate the heat generated in the 2DEG region through the substrate (refer to the bottom-side cooling configuration shown in **Figure 8 (a)**). Therefore, top-side cooling methods are thought to be most suitable for the thermal management of $Al_xGa_{1-x}N$-channel HEMTs (to be discussed in **Figure 8 (b)**).[70] Above room temperature (or from ~100 K), the thermal conductivity of crystalline solids including GaN and AlN are well known to monotonically decrease with temperature.[62,64–66,71,72] However, data in **Figure 3 (b)** show the thermal conductivity of $Al_xGa_{1-x}N$ (x=0.3) remains relatively constant from 78 K up to 450 K, similar to the behavior of amorphous materials[69,73]. Data in **Figure 3 (a)** and **(b)** show that phonon-alloy disorder scattering dominates the thermal conductivity of the solid solution. The relatively constant thermal conductivity and electron mobility of $Al_xGa_{1-x}N$ at high temperatures suggest that $Al_xGa_{1-x}N$-channel HEMTs with a thermally-optimized design may be suitable for extreme-temperature applications[15,74–76].

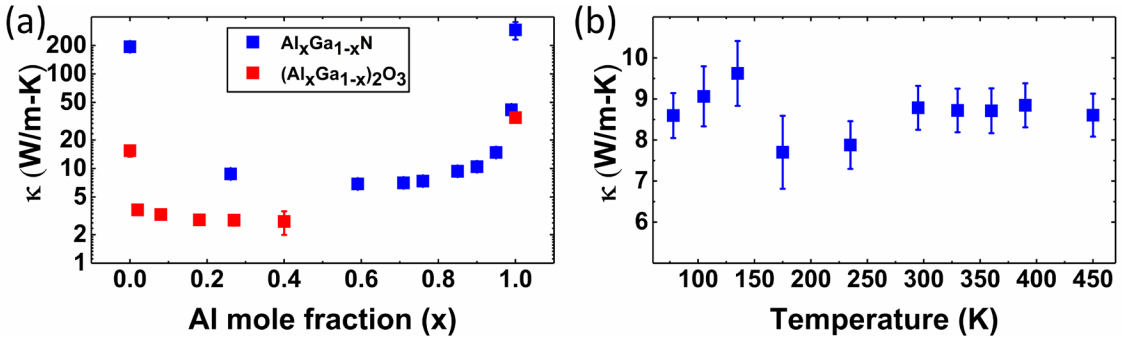

Figure 3. *(a) The cross-plane thermal conductivity of c-plane $Al_xGa_{1-x}N$ and ($\bar{2}01$)-oriented β-$(Al_xGa_{1-x})_2O_3$ obtained from TDTR and FDTR measurements.[15,77] (b) The temperature dependence of the thermal conductivity of an $Al_{0.3}Ga_{0.7}N$ thin film.*

β-Ga_2O_3: β-Ga_2O_3 exhibits a relatively low and anisotropic thermal conductivity.[11,78,79] The room temperature cross-plane thermal conductivity of (010), (001), ($\bar{2}01$), and (100)-oriented substrates were reported to be 27.0 W/mK, 14.7 W/mK, 13.3 W/mK, and 10.9 W/mK, respectively.[11] Therefore, device-level cooling methods such as substrate heterointegration (**Figure 8 (a)**) and flip-chip integration (**Figure 8 (b)**) will have to be used to prevent device overheating. For both thermal management techniques, the thermal energy generated in the device

channel will have to transport though either the β-Ga_2O_3 channel/buffer or the β-$(Al_xGa_{1-x})_2O_3$ barrier layer (**Figure 1 (b)**). Thin films often possess a lower thermal conductivity than the host bulk material due to phonon-boundary scattering effects. Therefore, the thermal conductivities of β-Ga_2O_3 and β-$(Al_xGa_{1-x})_2O_3$ heteroepitaxial thin films grown on c-plane and 6° offcut sapphire substrates were studied. In addition, interfacial thermal transport across the heterointerfaces was investigated.[77] It was previously reported in references [80,81] that β-Ga_2O_3 films grown on a 6° offcut sapphire substrate (**Figure 4 (c)**) by low pressure chemical vapor deposition (LPCVD) would possess a higher crystal quality than those grown on an on-axis c-plane sapphire substrate (**Figure 4 (b)**). **Figure 4 (a)** shows that the thermal conductivity of β-Ga_2O_3 thin films is a strong function of both film thickness and crystallinity due to phonon-boundary and phonon-defect scattering effects, respectively. β-Ga_2O_3 films on a 6° offcut sapphire substrate exhibit higher crystallinity and thermal conductivity than those for films grown on a c-plane sapphire substrate (**Figure 4 (a)-(c)**). However, the interface quality of a film on a 6° offcut sapphire substrate (**Figure 4 (f)**), which is represented by the interfacial thermal boundary conductance (TBC) (**Figure 4 (d)**), was inferior to that for β-Ga_2O_3 grown on a c-plane sapphire substrate (**Figure 4 (e)**). The thermal conductivity of β-$(Al_xGa_{1-x})_2O_3$ (which is necessary to create a MODFET structure in **Figure 1 (b)**) was measured for x=0.18 and was determined to be 3.6 W/mK in the [010] direction and 3.1 W/mK in the direction perpendicular to the $(\bar{2}01)$ plane.[82] **Figure 3 (a)** shows additional measurement results (using FDTR and TDTR) of the thermal conductivity of $(\bar{2}01)$-oriented β-$(Al_xGa_{1-x})_2O_3$ thin films grown via metalorganic vapor phase epitaxy (MOVPE)[83] on sapphire substrates.[77] Similar to the case of $Al_xGa_{1-x}N$, phonon-alloy disorder scattering dominates the thermal transport within β-$(Al_xGa_{1-x})_2O_3$. Both solid solutions possess a periodic lattice structure; however, the basis/lattice points lack compositional homogeneity due to the chemical disorder associated with the group-III cationic sublattice, occupied by Al and Ga atoms.[84] This disorder significantly limits the transport of heat carriers (i.e., phonons).

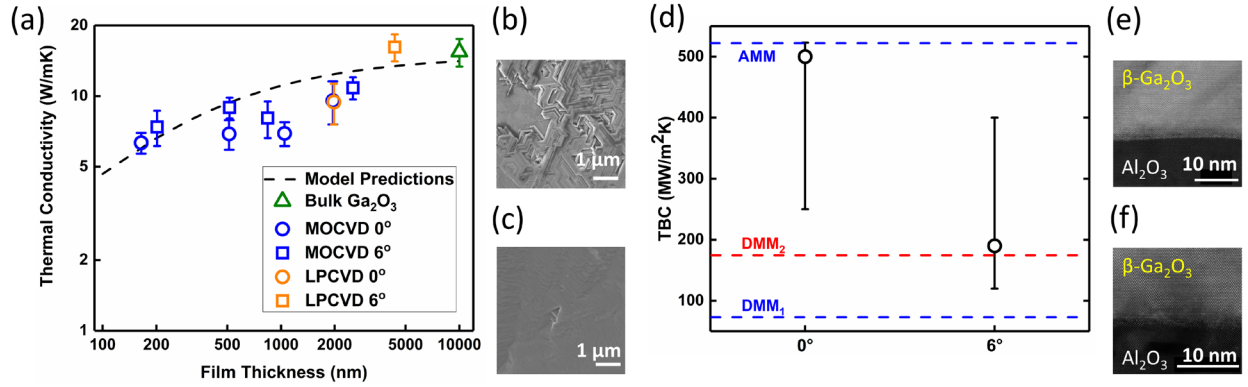

Figure 4. *(a) The measured cross-plane thermal conductivities of the β-Ga_2O_3 thin films and a bulk substrate. Top-view 50k× SEM images of LPCVD-grown films on (b) 0° and (c) 6°off-cut substrates. (d) The measured TBC of β-Ga_2O_3 grown on 0° and 6° off-axis c-plane sapphire substrates. Atomic scale STEM images representing β-Ga_2O_3 films grown on (e) 0° and (f) 6° off-axis c-plane sapphire substrates.*

Diamond: While diamond can be used as an active host material to construct UWBG semiconductor devices, it will also play a crucial role to mitigate overheating of $Al_xGa_{1-x}N$ and β-Ga_2O_3 electronics through integration efforts. The diamond integration approach has been proven to be effective in the development of GaN-on-diamond RF electronics.[50] We reported the first

study on the direct growth of polycrystalline diamond thin films on β-Ga_2O_3 (**Figure 5 (a)**).[85] The diamond thermal conductivity and effective diamond/β-Ga_2O_3 interfacial thermal boundary resistance (TBR) were measured to be ~110 W/mK and ~30.2 m^2K/GW (**Figure 5 (c)**). The thermal conductivity of bulk polycrystalline diamond films is generally isotropic and can be as high as 2200 W/mK, which is similar to that of bulk single crystal diamond.[86] However, the thermal conductivity within the first micron of synthesis (which is beyond the thickness of the films synthesized in our work) is much lower than the bulk value and is highly anisotropic due to phonon scattering with nucleation region defects and boundaries of the columnar grains (**Figure 5 (b)**).[87,88] Data in **Figure 5 (c)** suggest that the low thermal conductivity of the SiO_2 seeding layer dominates the effective TBR at the β-Ga_2O_3/diamond interface. While more data points are necessary to confirm this interim conclusion, this observation is similar to previous studies on diamond/GaN heterostructures using low thermal conductivity SiN_x seeding layers for the diamond film growth.[89,90]

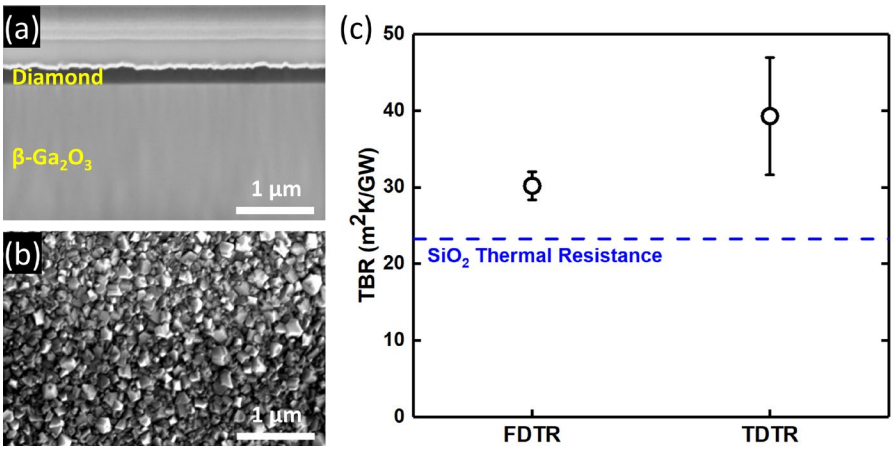

Figure 5. *(a) Cross-sectional scanning electron microscopy (SEM) image of the diamond/β-Ga_2O_3 structure. (b) A plan-view scanning electron microscopy (SEM) image of a 267 nm-thick polycrystalline diamond film grown on a ($\bar{2}$01) β-Ga_2O_3 substrate. (c) The effective diamond/β-Ga_2O_3 TBR measured by TDTR and FDTR methods.*

2. Electro-Thermal Modeling

A coupled 3D electro-thermal modeling scheme that calculates the Joule heat distribution and replicates phonon transport within/across the device epitaxial structure was developed and used to estimate the channel temperature rise of a β-Ga_2O_3 Schottky barrier diode (SBD)[91], metal-oxide-semiconductor field-effect transistor (MOSFET)[92,93], metal-semiconductor field-effect transistor (MESFET)[94], MODFET[82], vertical fin field-effect transistor (FinFET)[95], $Al_xGa_{1-x}N$-channel HEMT[15,70] and H-terminated diamond FET[96].

The 2D electrical portion of the electro-thermal model self-consistently solves, for each mesh point, the Poisson, current continuity, drift-diffusion (or electro-hydrodynamic), heat generation, and the heat diffusion equations to derive the electrostatic potential, electron concentration and their energy/temperature distributions, trap occupancy statistics, and electron/lattice temperature rise, as appropriate for the physics in the simulation. The resulting set of differential equations are then discretized, coupled, and solved. Finally, a solution is obtained by a nonlinear iteration method. By projecting the 2D Joule heat distribution (obtained from the electrical model) along the channel width, a 3D volumetric heat generation profile is obtained, which is imported into a 3D finite element thermal model. This 2D-3D coupling process is necessary to prevent over-

estimation of the channel temperature obtained from the 2D electrical model (due to the heat spreading ignored through the "absent" third dimension). Details of the electro-thermal modeling of UWBG devices can be found in references [82,97]. Exemplary steady-state simulation results for a β-Ga_2O_3 vertical fin field-effect transistor (FinFET)[98] are shown in **Figure 6**.

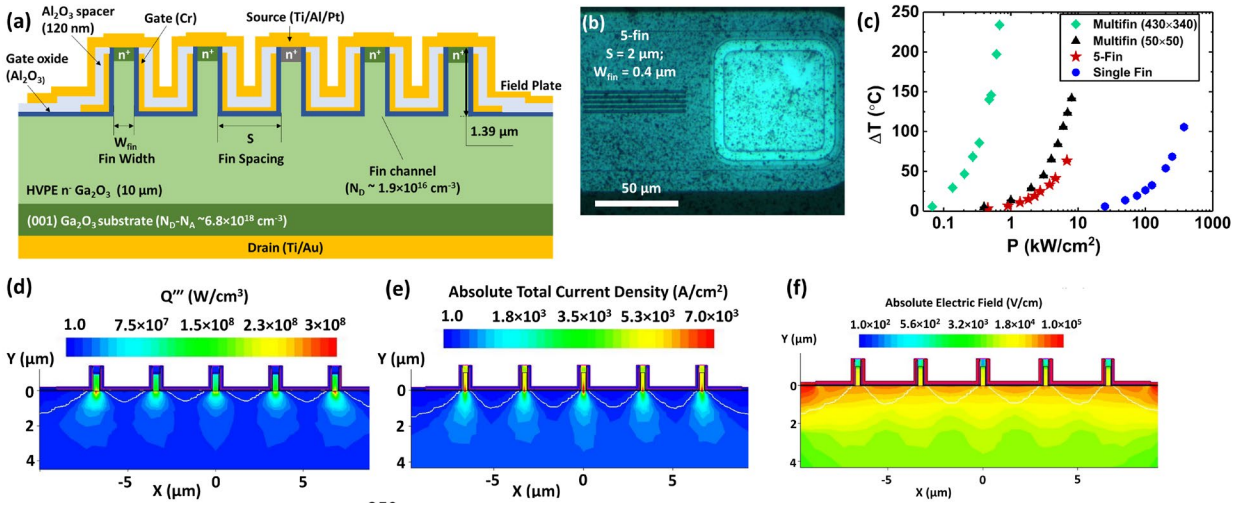

Figure 6. *(a) The epitaxial structure of a multi-fin β-Ga_2O_3 FinFET. (b) Optical image of a 5-fin FinFET. (c) The surface temperature rise of single-fin, 5-fin, and multi-fin devices with 50 μm×50 μm and 430 μm×342 μm active areas. (d) Joule heat distribution, (e) current density distribution, and (f) electric field distribution within a 5-fin FinFET.*

3. Device Thermography

Under high voltage and power operating conditions that lead to nonlinear heat generation within dimensionally scaled UWBG devices, sharp temperature gradients form across the channel region (especially for the low thermal conductivity $Al_xGa_{1-x}N$ and β-Ga_2O_3 systems). Electrical-temperature sensitive parameter (E-TSP) methods[99] are commonly used in industry to estimate the channel/junction temperature and thereby assess the device thermal resistance. However, electrical methods are limited to the measurement of the average temperature across the entire device channel, which results in a significant under estimation of the device peak temperature.[100] Therefore, to validate the electro-thermal device models to be used for the design of thermal management solutions, a high-resolution temperature mapping capability is necessary. Since the current channel for lateral UWBG devices are located several tens of nanometers below the device surface (**Figure 1**), *in situ* thermography techniques that can probe the surface temperature of the UWBG semiconductor are demanded.

At present, optical thermography techniques such as infrared thermal microscopy, thermoreflectance imaging, and micro-Raman thermometry are commonly used for the temperature mapping of WBG devices such as GaN HEMTs.[52,53] However, these techniques are incapable of probing the channel temperature of UWBG devices. Infrared thermography is incapable of probing the semiconductor channel due to its transparency to infrared thermal radiation.[54] It also lacks the spatial resolution (~3 μm)[101], which is necessary to probe the channel peak temperature. This technique has been adequately used to measure the temperature of rough metal electrodes (with relatively large area) of a β-Ga_2O_3 SBD[91] and MOSFET[92] as well as the fin channels of a β-Ga_2O_3 FinFET[95] at elevated base temperatures. Thermoreflectance thermal

imaging has been used to probe the metal electrode temperatures of β-Ga_2O_3 SBDs[91], MOSFET[92], MODFET[82], and $Al_xGa_{1-x}N$-channel HEMTs[15,52,70]. However, visible to near-ultraviolet wavelength illumination sources, commonly used for thermoreflectance imaging, cannot probe the channel region because UWBG semiconductors are transparent at these optical wavelength regimes.[55] Micro-Raman thermometry also lacks the sensitivity to measure the UWBG channel surface because optical probing is typically carried out by using a sub-bandgap laser excitation source (e.g., a 532 nm laser). Micro-Raman thermometry for GaN devices[102–104] (e.g., GaN HEMTs) also typically employs a sub-bandgap laser. In this case, the common practice of growing GaN on a dissimilar material (i.e., non-native substrate) gives Raman selectivity to the GaN thickness (commonly ~1 μm). For GaN HEMTs, this is arguably sufficient[105], but for UWBG devices, this will typically result in severe depth averaging and underestimation of the channel surface temperature. The standard Raman thermography technique has been adequately used to characterize the cross-sectional temperature field of a β-Ga_2O_3 SBD diced perpendicular to the ($\bar{2}$01) plane.[91] The optical transparency of the UWBG material and the confocality of the Raman microscope have been leveraged to characterize the temperature rise of the constituent layers (i.e., $Al_xGa_{1-x}N$, AlN, sapphire) of an as-grown $Al_xGa_{1-x}N$-channel HEMT.[70]

Raman thermography techniques that take advantage of low-dimensional materials as discrete (i.e., TiO_2 nanoparticles) or continuous (i.e., 2D layered materials) surface temperature transducers are most suitable for measuring the channel surface temperature of UWBG devices. Nanoparticle-assisted Raman thermometry was used to measure the steady-state temperature rise of discrete points on the channel of β-Ga_2O_3 MOSFETs[93], a MODFET[82], and $Al_xGa_{1-x}N$-channel HEMTs[15,70]. This method was also used to study the transient thermal dynamics of $Al_xGa_{1-x}N$-channel HEMTs.[52,70] This technique was also used to compare the thermal performance of an H-terminated diamond FET with those for devices based on GaN, β-Ga_2O_3, and $Al_xGa_{1-x}N$.[96] We developed a 2D material-assisted Raman thermography and characterized a β-Ga_2O_3 MODFET.[106] In **Figure 7**, surface temperature maps of a β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ transmission line measurement (TLM) device acquired by visible-wavelength thermoreflectance imaging and 2D material-assisted Raman thermography are shown. The TLM device was operating under a power dissipation level of 1 W/mm. For 2D material-assisted Raman thermography (**Figure 7 (c)**), CVD-grown monolayer MoS_2 was utilized as a surface temperature transducer. A distinctive feature of this technique is that a high resolution (~500 nm) full 2D temperature image can be acquired, regardless of the constituent materials of the device surface. In contrast, the temperature map acquired via visible-wavelength thermoreflectance imaging (**Figure 7 (b)**) demonstrates its limitation for being able to only probe the metal contacts.

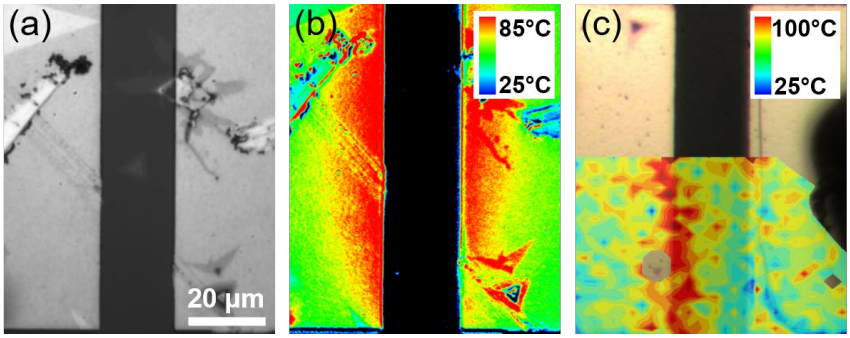

Figure 7. *(a) Optical image of a β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ TLM device. (b) A thermal image acquired via visible wavelength thermoreflectance imaging. (c) A continuous 2D surface temperature map generated by 2D material-assisted Raman thermography.*

When validating electro-thermal simulation results using local temperature values acquired from the aforementioned optical thermography techniques, it is important to create a temperature probe in the model with dimensions that correspond to the spatial resolution of the experimental method. This is because very large temperature gradients form in β-Ga_2O_3 and $Al_xGa_{1-x}N$ devices due to the low thermal conductivity of the base materials. Therefore, the simulated device peak temperatures are, in general, much higher than those probed by the optical methods with a spatial resolution on the order of 0.5 – 1 μm.

4. Device-Level Thermal Management

Both $Al_xGa_{1-x}N$ and β-Ga_2O_3 devices require device-level cooling solutions that locate the thermal heat sink in proximity to (ideally, <1 μm[50]) the heat source (i.e., the 2DEG channel). Here we discuss thermal management scenarios for a β-Ga_2O_3 lateral FET, where the aim is to extract heat from the bottom-side, top-side, or both sides of the device (i.e., double-sided cooling). Most conclusions derived from this discussion on a β-Ga_2O_3 lateral FET will equally apply to an $Al_xGa_{1-x}N$-channel HEMT.

Our study[92] on the device-level thermal management of a single-channel β-Ga_2O_3 MOSFET revealed that the channel temperature rise of a homoepitaxial device could exceed 1500 K under a targeted power dissipation level of 10 W/mm (3D electro-thermal simulation was performed in this work, where the device base temperature was kept at 25°C and the device surface was exposed to natural convection). This corresponds to a junction-to-package thermal resistance (R_{Th}) of 150 mm·K/W, which is unacceptably high. Results in this work highlight that a composite wafer, which consists of a thin β-Ga_2O_3 layer (<10 μm) integrated with a high thermal conductivity substrate (e.g., SiC, diamond), can mitigate device overheating. For the β-Ga_2O_3 materials system, a composite wafer formed via wafer bonding can serve as a platform for subsequent device fabrication that allow growth of homoepitaxial layers with the highest crystalline quality without threading dislocations. However, to maintain the structural integrity of the composite wafer without causing interface damage, low-temperature film deposition techniques such as low-temperature MOVPE[107] should be used to deposit the epitaxial layers. The fabrication of a β-Ga_2O_3/SiC composite substrate and subsequent homoepitaxial growth of a high-quality epitaxial layer via low-temperature MOVPE has been demonstrated.[108] For $Al_xGa_{1-x}N$-based lateral transistors, devices can be directly constructed on high-thermal conductivity single crystal AlN substrates instead of fabricating a composite substrate via wafer bonding.[30,31] Simulation results for bottom-side cooling of an $Al_xGa_{1-x}N$-channel HEMT can be found in reference [70]. To further reduce the R_{Th}, bottom-side cooling methods would need to be augmented by a high-thermal conductivity surface heat spreader (e.g., polycrystalline diamond [85]) combined with an active top-side heat extraction mechanism (e.g., air-jet impingement cooling[109]) to form a double-sided cooling platform[82].

Top-side cooling via flip-chip integration[110] is an alternative approach for the device-level thermal management. The key to accomplishing maximized top-side heat extraction using this configuration is to passivate the device surface with a high-thermal conductivity material (such as polycrystalline diamond[85]), locate large-area gold thermal bumps between the device metal electrodes and the carrier wafer, and use a high-thermal conductivity carrier wafer (e.g., SiC, diamond). While top-side heat extraction alone via flip-chip integration was shown to be sufficient to reduce the device thermal resistance to manageable levels,[70,82,92] one may flip-chip a device fabricated on a composite wafer to maximize the heat transfer performance (i.e., double-sided

cooling[82]).

The thermal management of multi-finger β-Ga_2O_3 and $Al_xGa_{1-x}N$ transistors will be much more challenging than the case of a single-channel device (at identical power density operation), as shown in reference [108]. This is due to the significantly increased device thermal resistance (3-4× higher R_{Th} for a 6-finger β-Ga_2O_3 device as compared to a single finger transistor)[108] caused by the thermal cross-talk[111,112] among individual current channels. For example, the aggravated self-heating of vertically-configured multi-fin β-Ga_2O_3 FinFETs as compared to single-fin β-Ga_2O_3 devices has been reported through experiments.[95]

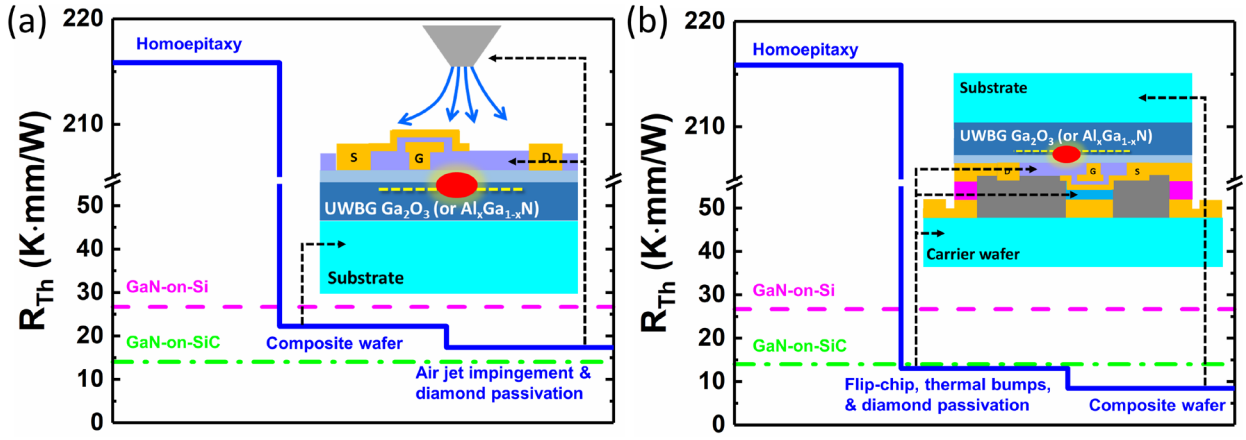

Figure 8. *Improvement of the β-Ga_2O_3 device thermal resistance by augmenting the device architecture with (a) bottom-side (substrate engineering) and (b) top-side (flip-chip integration) cooling solutions.*

Exemplary simulation results in **Figure 8 (a)** show that the thermal resistance of a six-finger β-Ga_2O_3 lateral FET with a source-connected field plate (the gate length, gate-to-source distance, gate-to-drain distance, and gate-to-gate pitch are 0.5 µm, 1.3 µm, 4.3 µm, and 45 µm, respectively) can be reduced to a level similar to today's commercial GaN HEMTs fabricated on Si and SiC[102,113] substrates by optimizing the electro-thermal device-design. In this simulation, the homoepitaxial device was augmented by replacing the native substrate with a polycrystalline diamond substrate[114] (the thicknesses of the substrate and the remaining β-Ga_2O_3 layer are 500 µm and 2 µm, respectively), incorporating a 2 µm thick polycrystalline diamond passivation layer[115–117], and integrating air-jet impingement cooling with a convective heat transfer coefficient of 17 kW/m^2K[109]. Further analysis of the modeling results (not shown) indicate that it is critical to minimize the thickness of the β-Ga_2O_3 layer of the composite substrate[92] and maximize the thermal conductance of the passivation layer by using a high-thermal conductivity material and/or growing it as thick as possible. Simulation results in **Figure 8 (b)** show the flip-chip integration approach[110] applied to the multi-finger β-Ga_2O_3 device fabricated on a (010)-oriented β-Ga_2O_3 substrate. This device is flip-chipped on a polycrystalline diamond carrier wafer while the device surface is passivated with polycrystalline diamond, and a 2 µm thick gold thermal bump[118–120] is inserted between the source-connected field plate and the polycrystalline diamond carrier wafer. The device architecture is further augmented by replacing the native substrate with synthetic polycrystalline diamond. The simulation results suggest that the flip-chip integration approach is indeed a viable solution to minimize the device junction-to-package thermal resistance, which can be even lower than that for today's GaN-on-Si power HEMTs and GaN-on-SiC RF power amplifiers. However, it should be noted that the interfacial thermal boundary resistances across various material

interfaces between the device surface and the carrier wafer are neglected in this simulation. Also, for this configuration, caution should be taken since any added capacitance may negatively impact the device high-frequency performance. For example, while the source-connected field plate is usually grounded for most RF power amplifiers, the drain electrode experiences a large RF voltage swing. For this reason, a thermal bump was only inserted between the carrier wafer and the source-connected field plate (but not the drain electrode) in the flip-chip configuration shown in **Figure 8 (b)**. For such cases, electrical simulation[121] should accompany the thermal design to estimate the effect of a thermal bump on the device switching performance. More details of this diamond-incorporated flip-chip integration scheme for UWBG lateral devices can be found in reference [122].

Thermal management of H-terminated diamond FETs should be approached from a different angle. As shown in our work on an H-terminated diamond FET,[123] diamond devices exhibit extraordinary thermal performance. Therefore, the need to enhance heat extraction from the device channel is minimal. However, one of the biggest challenges for H-terminated diamond FETs is to preserve the long-term environmental and thermal stability of the transfer-doped 2DHG channel.[44,47] For instance, the C-H bonds and/or the surface adsorbates of an air-exposed H-terminated diamond FET were shown to be detrimentally impacted beyond an ambient temperature of 200°C, resulting in an irreversible loss of the surface p-type conduction.[44] Recent reports in literature[124] show that high-temperature deposition of an Al_2O_3 protective layer renders a less susceptible H-termination. When capped with Al_2O_3, the diamond surface is protected from the atmosphere, in particular, from the hydroxide (OH^-) ions. Stable operation of an H-terminated diamond FET as well as a complementary FET up to 350°C was reported, enabled by an Al_2O_3-based dielectric technology.[124]

V. Conclusion

For legacy semiconductor materials, it was sufficient to consider the thermal aspects after the design and fabrication of an operational device. Doping profiles, channel geometry, and the layer stack were optimized electrically, and the thermal aspects were considered after these were finalized. For UWBG semiconductors, we see evidence that electro-thermal co-design techniques are essential even at this early stage to commercialize high-power, high-voltage, and fast-switching UWBG devices for next-generation military power electronics and wireless communication applications. The newly-developed modeling and characterization methods will become essential tools supporting near-future device reliability studies and temperature-accelerated direct current (DC) operational life tests[113,125,126]. UWBG device architectures must employ device-level thermal management solutions that minimize the device junction-to-package thermal resistance. The electro-thermal co-design process developed for UWBG devices in this AFOSR YIP project will eventually lead to the realization of higher device performance, prolonged component lifetime, and improved system-level size, weight, and power (SWaP) and efficiency.

References

[1] R.. Trew, G.L. Bilbro, W. Kuang, Y. Liu, and H. Yin, IEEE Microw. Mag. 56 (2005).

[2] I.C. Kizilyalli, Y.A. Xu, E. Carlson, J. Manser, and D.W. Cunningham, in *2017 IEEE 5th Work. Wide Bandgap Power Devices Appl.* (2017), p. 417.

[3] U. Mishra, S. Likun, and T. Kazior, Proc. IEEE **96**, 287 (2008).

[4] J.Y. Tsao, S. Chowdhury, M.A. Hollis, D. Jena, N.M. Johnson, K.A. Jones, R.J. Kaplar, S. Rajan, C.G. Van de Walle, E. Bellotti, C.L. Chua, R. Collazo, M.E. Coltrin, J.A. Cooper, K.R. Evans, S. Graham, T.A. Grotjohn, E.R. Heller, M. Higashiwaki, M.S. Islam, P.W. Juodawlkis, M.A. Khan, A.D. Koehler, J.H. Leach, U.K. Mishra, R.J.

Nemanich, R.C.N. Pilawa-Podgurski, J.B. Shealy, Z. Sitar, M.J. Tadjer, A.F. Witulski, M. Wraback, and J.A. Simmons, Adv. Electron. Mater. **4**, 1600501 (2017).
[5] S.J. Pearton, F. Ren, M. Tadjer, and J. Kim, J. Appl. Phys. **124**, 220901 (2018).
[6] C.J.H. Wort and R.S. Balmer, Mater. Today **11**, 22 (2008).
[7] E. Johnson, in *1958 IRE Int. Conv. Rec.* (1965), pp. 27–34.
[8] M.E. Coltrin, A.G. Baca, and R.J. Kaplar, ECS J. Solid State Sci. Technol. **6**, S3114 (2017).
[9] B.J. Baliga, J. Appl. Phys. **53**, 1759 (1982).
[10] Y. Zhang and J.S. Speck, Semicond. Sci. Technol. **35**, 125018 (2020).
[11] Z. Guo, A. Verma, X. Wu, F. Sun, A. Hickman, T. Masui, A. Kuramata, M. Higashiwaki, D. Jena, and T. Luo, Appl. Phys. Lett. **106**, 111909 (2015).
[12] A.G. Baca, A.M. Armstrong, A.A. Allerman, E.A. Douglas, C.A. Sanchez, M.P. King, M.E. Coltrin, T.R. Fortune, and R.J. Kaplar, Appl. Phys. Lett. **109**, 033509 (2016).
[13] S. Russell, S. Sharabi, A. Tallaire, and D.A.J. Moran, IEEE Trans. Electron Devices **62**, 751 (2015).
[14] A.F.M. Anwar, S. Shangli Wu, and R.T. Webster, IEEE Trans. Electron Devices **48**, 567 (2001).
[15] B. Chatterjee, J.S. Lundh, Y. Song, D. Shoemaker, A.G. Baca, R.J. Kaplar, T.E. Beechem, C. Saltonstall, A.A. Allerman, A.M. Armstrong, B.A. Klein, A. Bansal, H.R. Seyf, D. Talreja, A. Pogrebnyakov, E. Heller, V. Gopalan, A.S. Henry, J.M. Redwing, B. Foley, and S. Choi, IEEE Electron Device Lett. **43**, 461 (2020).
[16] S.J. Pearton, J. Yang, P.H. Cary, F. Ren, J. Kim, M.J. Tadjer, and M.A. Mastro, Appl. Phys. Rev. **5**, 11301 (2018).
[17] K. Ghosh and U. Singisetti, J. Appl. Phys. **124**, 85707 (2018).
[18] Y. Zhang, C. Joishi, Z. Xia, M. Brenner, S. Lodha, and S. Rajan, Appl. Phys. Lett. **112**, 233503 (2018).
[19] S.B. Reese, T. Remo, J. Green, and A. Zakutayev, Joule **3**, 903 (2019).
[20] M.H. Wong and M. Higashiwaki, IEEE Trans. Electron Devices **67**, 3925 (2020).
[21] W. Li, K. Nomoto, Z. Hu, D. Jena, and H.G. Xing, IEEE Trans. Electron Devices **67**, 3938 (2020).
[22] M. Dutta, F.A.M. Koeck, W. Li, R.J. Nemanich, and S. Chowdhury, IEEE Electron Device Lett. **38**, 600 (2017).
[23] M. Malakoutian, M. Benipal, F.A. Koeck, R.J. Nemanich, and S. Chowdhury, IEEE J. Electron Devices Soc. **8**, 614 (2020).
[24] R.R. Pelá, C. Caetano, M. Marques, L.G. Ferreira, J. Furthmüller, and L.K. Teles, Appl. Phys. Lett. **98**, 151907 (2011).
[25] O. Ambacher, J. Smart, J.R. Shealy, N.G. Weimann, K. Chu, M. Murphy, W.J. Schaff, L.F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, J. Appl. Phys. **85**, 3222 (1999).
[26] A.G. Baca, A.M. Armstrong, B.A. Klein, A.A. Allerman, E.A. Douglas, and R.J. Kaplar, J. Vac. Sci. Technol. A **38**, 20803 (2020).
[27] A.G. Baca, A.M. Armstrong, A.A. Allerman, B.A. Klein, E.A. Douglas, C.A. Sanchez, and T.R. Fortune, ECS J. Solid State Sci. Technol. **6**, S3010 (2017).
[28] A.G. Baca, B.A. Klein, A.A. Allerman, A.M. Armstrong, E.A. Douglas, C.A. Stephenson, T.R. Fortune, and R.J. Kaplar, ECS J. Solid State Sci. Technol. **6**, Q161 (2017).
[29] S.H. Sohel, A. Xie, E. Beam, H. Xue, T. Razzak, S. Bajaj, S. Campbell, D. White, K. Wills, Y. Cao, W. Lu, and S. Rajan, Appl. Phys. Express **13**, 36502 (2020).
[30] H. Tokuda, M. Hatano, N. Yafune, S. Hashimoto, K. Akita, Y. Yamamoto, and M. Kuzuhara, Appl. Phys. Express **3**, 121003 (2010).
[31] N. Yafune, K. Akita, S. Hashimoto, M. Kuzuhara, Y. Yamamoto, and H. Tokuda, Electron. Lett. **50**, 211 (2014).
[32] M. Shatalov, W. Sun, R. Jain, A. Lunev, X. Hu, A. Dobrinsky, Y. Bilenko, J. Yang, G.A. Garrett, L.E. Rodak, M. Wraback, M. Shur, and R. Gaska, Semicond. Sci. Technol. **29**, 84007 (2014).
[33] M. Higashiwaki and G.H. Jessen, Appl. Phys. Lett. **112**, 60401 (2018).
[34] M. Higashiwaki, K. Sasaki, H. Murakami, Y. Kumagai, A. Koukitu, A. Kuramata, T. Masui, and S. Yamakoshi, Semicond. Sci. Technol. **31**, 34001 (2016).
[35] G. Seryogin, F. Alema, N. Valente, H. Fu, E. Steinbrunner, A.T. Neal, S. Mou, A. Fine, and A. Osinsky, Appl. Phys. Lett. **117**, 262101 (2020).
[36] Y. Zhang, Z. Xia, J. Mcglone, W. Sun, C. Joishi, A.R. Arehart, S.A. Ringel, and S. Rajan, IEEE Trans. Electron Devices **66**, 1574 (2019).
[37] M.J. Tadjer, F. Alema, A. Osinsky, M.A. Mastro, N. Nepal, J.M. Woodward, R.L. Myers-Ward, E.R. Glaser, J.A. Freitas, A.G. Jacobs, J.C. Gallagher, A.L. Mock, D.J. Pennachio, J. Hajzus, M. Ebrish, T.J. Anderson, K.D. Hobart, J.K. Hite, and C.R. Eddy Jr., J. Phys. D. Appl. Phys. **54**, 34005 (2020).
[38] N. Ma, N. Tanen, A. Verma, Z. Guo, T. Luo, H. (Grace) Xing, and D. Jena, Appl. Phys. Lett. **109**, 212101 (2016).
[39] K. Ghosh and U. Singisetti, J. Mater. Res. **32**, 4142 (2017).
[40] R. Kalish, J. Phys. D. Appl. Phys. **40**, 6467 (2007).

[41] K. Hirama, H. Takayanagi, S. Yamauchi, Y. Jingu, H. Umezawa, and H. Kawarada, in *2007 IEEE Int. Electron Devices Meet.* (2007), pp. 873–876.
[42] S.A.O. Russell, L. Cao, D. Qi, A. Tallaire, K.G. Crawford, A.T.S. Wee, and D.A.J. Moran, Appl. Phys. Lett. **103**, 202112 (2013).
[43] K.G. Crawford, L. Cao, D. Qi, A. Tallaire, E. Limiti, C. Verona, A.T.S. Wee, and D.A.J. Moran, Appl. Phys. Lett. **108**, 42103 (2016).
[44] K.G. Crawford, D. Qi, J. McGlynn, T.G. Ivanov, P.B. Shah, J. Weil, A. Tallaire, A.Y. Ganin, and D.A.J. Moran, Sci. Rep. **8**, 3342 (2018).
[45] M. Kasu and T. Oishi, in *2016 IEEE Compd. Semicond. Integr. Circuit Symp.* (2016), pp. 1–4.
[46] T.G. Ivanov, J. Weil, P.B. Shah, A.G. Birdwell, K. Kingkeo, and E.A. Viveiros, in *2018 IEEE/MTT-S Int. Microw. Symp. - IMS* (2018), pp. 1461–1463.
[47] H. Kawarada, H. Tsuboi, T. Naruo, T. Yamada, D. Xu, A. Daicho, T. Saito, and A. Hiraiwa, Appl. Phys. Lett. **105**, 13510 (2014).
[48] R. Gaska, A. Osinsky, J.W. Yang, and M.S. Shur, IEEE Electron Device Lett. **19**, 89 (1998).
[49] S. Choi, E. Heller, D. Dorsey, R. Vetury, and S. Graham, J. Appl. Phys. **114**, 164501 (2013).
[50] A. Bar-Cohen, J.J. Maurer, and D.H. Altman, J. Electron. Packag. **141**, 040803 (2019).
[51] E.R. Heller and A. Crespo, Microelectron. Reliab. **48**, 45 (2008).
[52] J.S. Lundh, Y. Song, B. Chatterjee, A.G. Baca, R.J. Kaplar, A.M. Armstrong, A.A. Allerman, B.A. Klein, D. Kendig, H. Kim, and S. Choi, J. Electron. Packag. **142**, 031113 (2020).
[53] S.K. Oh, J.S. Lundh, S. Shervin, B. Chatterjee, D.K. Lee, S. Choi, J.S. Kwak, and J.-H. Ryou, J. Electron. Packag. **141**, 20801 (2019).
[54] A. Sarua, H. Hangfeng Ji, M. Kuball, M.J. Uren, T. Martin, K.P. Hilton, and R.S. Balmer, IEEE Trans. Electron Devices **53**, 2438 (2006).
[55] B. Chatterjee, C. Dundar, T.E. Beechem, E. Heller, D. Kendig, H. Kim, N. Donmezer, and S. Choi, J. Appl. Phys. **127**, 44502 (2020).
[56] W. Liu and A.A. Balandin, J. Appl. Phys. **97**, 073710 (2005).
[57] W. Liu and A.A. Balandin, Appl. Phys. Lett. **85**, 5230 (2004).
[58] B.C. Daly, H.J. Maris, W.K. Ford, G.A. Antonelli, L. Wong, and E. Andideh, J. Appl. Phys. **92**, 6005 (2002).
[59] D.G. Cahill, Rev. Sci. Instrum. **75**, 5119 (2004).
[60] A.J. Schmidt, R. Cheaito, and M. Chiesa, Rev. Sci. Instrum. **80**, 094901 (2009).
[61] T.E. Beechem, A.E. McDonald, E.J. Fuller, A.A. Talin, C.M. Rost, J.-P. Maria, J.T. Gaskins, P.E. Hopkins, and A.A. Allerman, J. Appl. Phys. **120**, 95104 (2016).
[62] Q. Zheng, C. Li, A. Rai, J.H. Leach, D.A. Broido, and D.G. Cahill, Phys. Rev. Mater. **3**, 14601 (2019).
[63] Y. Song, J. Lundh, W. Wang, J. Leach, D. Eichfeld, A. Krishnan, C. Perez, D. Ji, T. Borman, K. Ferri, J.-P. Maria, S. Chowdhury, J.-H. Ryou, B. Foley, and S. Choi, J. Electron. Packag. **142**, 041112 (2020).
[64] Y.R. Koh, Z. Cheng, A. Mamun, M.S. Bin Hoque, Z. Liu, T. Bai, K. Hussain, M.E. Liao, R. Li, J.T. Gaskins, A. Giri, J. Tomko, J.L. Braun, M. Gaevski, E. Lee, L. Yates, M.S. Goorsky, T. Luo, A. Khan, S. Graham, and P.E. Hopkins, ACS Appl. Mater. Interfaces **12**, 29443 (2020).
[65] G.A. Slack, R.A. Tanzilli, R.O. Pohl, and J.W. Vandersande, J. Phys. Chem. Solids **48**, 641 (1987).
[66] R.L. Xu, M. Munõz Rojo, S.M. Islam, A. Sood, B. Vareskic, A. Katre, N. Mingo, K.E. Goodson, H.G. Xing, D. Jena, and E. Pop, J. Appl. Phys. **126**, (2019).
[67] B. Abeles, Phys. Rev. **131**, 1906 (1963).
[68] S. Adachi, J. Appl. Phys. **102**, 63502 (2007).
[69] H.R. Seyf, L. Yates, T.L. Bougher, S. Graham, B.A. Cola, T. Detchprohm, M.-H. Ji, J. Kim, R. Dupuis, W. Lv, and A. Henry, Npj Comput. Mater. **3**, 49 (2017).
[70] J.S. Lundh, B. Chatterjee, Y. Song, A.G. Baca, R.J. Kaplar, T.E. Beechem, A.A. Allerman, A.M. Armstrong, B.A. Klein, A. Bansal, D. Talreja, A. Pogrebnyakov, E. Heller, V. Gopalan, J.M. Redwing, B.M. Foley, and S. Choi, Appl. Phys. Lett. **115**, 153503 (2019).
[71] E. Ziade, J. Yang, G. Brummer, D. Nothern, T. Moustakas, and A.J. Schmidt, Appl. Phys. Lett. **107**, 91605 (2015).
[72] E. Ziade, J. Yang, G. Brummer, D. Nothern, T. Moustakas, and A.J. Schmidt, Appl. Phys. Lett. **110**, 31903 (2017).
[73] D.Q. Tran, N. Blumenschein, A. Mock, P. Sukkaew, H. Zhang, J.F. Muth, T. Paskova, P.P. Paskov, and V. Darackchieva, Phys. B Condens. Matter 411810 (2019).
[74] A.G. Baca, A.M. Armstrong, A.A. Allerman, B.A. Klein, E.A. Douglas, C.A. Sanchez, and T.R. Fortune, ECS J. Solid State Sci. Technol. **6**, S3010 (2017).

[75] S. Mollah, K. Hussain, R. Floyd, A. Mamun, M. Gaevski, M.V.S. Chandrashekhar, I. Ahmad, G. Simin, V. Wheeler, C. Eddy, and A. Khan, Phys. Status Solidi **217**, 1900802 (2020).
[76] P.H. Carey, F. Ren, A.G. Baca, B.A. Klein, A.A. Allerman, A.M. Armstrong, E.A. Douglas, R.J. Kaplar, P.G. Kotula, and S.J. Pearton, IEEE J. Electron Devices Soc. **7**, 444 (2019).
[77] Y. Song, P. Ranga, Y. Zhang, Z. Feng, H.-L. Huang, M.D. Santia, S.C. Badescu, C.U. Gonzalez-Valle, C. Perez, K. Ferri, R.M. Lavelle, D.W. Snyder, B.A. Klein, J. Deitz, A.G. Baca, J.-P. Maria, B. Ramos-Alvarado, J. Hwang, H. Zhao, X. Wang, S. Krishnamoorthy, B.M. Foley, and S. Choi, ACS Appl. Mater. Interfaces **13**, 38477 (2021).
[78] M.D. Santia, N. Tandon, and J.D. Albrecht, Appl. Phys. Lett. **107**, 41907 (2015).
[79] P. Jiang, X. Qian, X. Li, and R. Yang, Appl. Phys. Lett. **113**, 232105 (2018).
[80] S. Rafique, L. Han, A.T. Neal, S. Mou, M.J. Tadjer, R.H. French, and H. Zhao, Appl. Phys. Lett. **109**, 132103 (2016).
[81] Z. Feng, M.R. Karim, and H. Zhao, APL Mater. **7**, 22514 (2018).
[82] B. Chatterjee, Y. Song, J.S. Lundh, Y. Zhang, Z. Xia, Z. Islam, J. Leach, C. McGray, P. Ranga, S. Krishnamoorthy, A. Haque, S. Rajan, and S. Choi, Appl. Phys. Lett. **117**, 153501 (2020).
[83] P. Ranga, A. Bhattacharyya, A. Chmielewski, S. Roy, R. Sun, M.A. Scarpulla, N. Alem, and S. Krishnamoorthy, Appl. Phys. Express **14**, 25501 (2021).
[84] H. Peelaers, J.B. Varley, J.S. Speck, and C.G. Van de Walle, Appl. Phys. Lett. **112**, 242101 (2018).
[85] M. Malakoutian, Y. Song, C. Yuan, C. Ren, J.S. Lundh, R.M. Lavelle, J.E. Brown, D.W. Snyder, S. Graham, S. Choi, and S. Chowdhury, Appl. Phys. Express **14**, 055502 (2021).
[86] T. Bai, Y. Wang, T.I. Feygelson, M.J. Tadjer, K.D. Hobart, N.J. Hines, L. Yates, S. Graham, J. Anaya, M. Kuball, and M.S. Goorsky, ECS J. Solid State Sci. Technol. **9**, 53002 (2020).
[87] A. Sood, R. Cheaito, T. Bai, H. Kwon, Y. Wang, C. Li, L. Yates, T. Bougher, S. Graham, M. Asheghi, M. Goorsky, and K.E. Goodson, Nano Lett. **18**, 3466 (2018).
[88] E. Bozorg-Grayeli, A. Sood, M. Asheghi, V. Gambin, R. Sandhu, T.I. Feygelson, B.B. Pate, K. Hobart, and K.E. Goodson, Appl. Phys. Lett. **102**, 111907 (2013).
[89] H. Sun, R.B. Simon, J.W. Pomeroy, D. Francis, F. Faili, D.J. Twitchen, and M. Kuball, Appl. Phys. Lett. **106**, 111906 (2015).
[90] J. Cho, D. Francis, D.H. Altman, M. Asheghi, and K.E. Goodson, J. Appl. Phys. **121**, 055105 (2017).
[91] B. Chatterjee, A. Jayawardena, E. Heller, D.W. Snyder, S. Dhar, and S. Choi, Rev. Sci. Instrum. **89**, 114903 (2018).
[92] B. Chatterjee, K. Zeng, C.D. Nordquist, U. Singisetti, and S. Choi, IEEE Trans. Components, Packag. Manuf. Technol. **9**, 2352 (2019).
[93] S.H. Kim, D. Shoemaker, B. Chatterjee, K.D. Chabak, A.J. Green, K.J. Liddy, G.H. Jessen, S. Graham, and S. Choi, in *2021 20th IEEE Intersoc. Conf. Therm. Thermomechanical Phenom. Electron. Syst.* (2021), pp. 324–327.
[94] A. Bhattacharyya, S. Roy, P. Ranga, D. Shoemaker, Y. Song, J.S. Lundh, S. Choi, and S. Krishnamoorthy, Appl. Phys. Express **14**, 76502 (2021).
[95] B. Chatterjee, W. Li, K. Nomoto, H.G. Xing, and S. Choi, Appl. Phys. Lett. **119**, 103502 (2021).
[96] J.S. Lundh, D. Shoemaker, A.G. Birdwell, J.D. Weil, L.M. De La Cruz, P.B. Shah, K.G. Crawford, T.G. Ivanov, H.Y. Wong, and S. Choi, Appl. Phys. Lett. **119**, 143502 (2021).
[97] B. Chatterjee, Electro-Thermal Investigation of Next Generation Wide Bandgap Electronics, The Pennsylvania State University, 2020.
[98] R.H. Montgomery, Y. Zhang, C. Yuan, S. Kim, J. Shi, T. Itoh, A. Mauze, S. Kumar, J. Speck, and S. Graham, J. Appl. Phys. **129**, 85301 (2021).
[99] N.A. Blumenschein, N.A. Moser, E.R. Heller, N.C. Miller, A.J. Green, A. Popp, A. Crespo, K. Leedy, M. Lindquist, T. Moule, S. Dalcanale, E. Mercado, M. Singh, J.W. Pomeroy, M. Kuball, G. Wagner, T. Paskova, J.F. Muth, K.D. Chabak, and G.H. Jessen, IEEE Trans. Electron Devices **67**, 204 (2020).
[100] N. Killat, M. Kuball, T.-M. Chou, U. Chowdhury, and J. Jimenez, in *2010 IEEE Int. Reliab. Phys. Symp.* (IEEE, 2010), pp. 528–531.
[101] J. Dallas, G. Pavlidis, B. Chatterjee, J.S. Lundh, M. Ji, J. Kim, T. Kao, T. Detchprohm, R.D. Dupuis, S. Shen, S. Graham, and S. Choi, Appl. Phys. Lett. **112**, 73503 (2018).
[102] S. Choi, E.R. Heller, D. Dorsey, R. Vetury, and S. Graham, IEEE Trans. Electron Devices **60**, 1898 (2013).
[103] T. Beechem, A. Christensen, S. Graham, and D. Green, J. Appl. Phys. **103**, 124501 (2008).
[104] M. Kuball and J.W. Pomeroy, IEEE Trans. Device Mater. Reliab. **16**, 667 (2016).
[105] R. Pearson, B. Chatterjee, S. Kim, S. Graham, A. Rattner, and S. Choi, J. Electron. Packag. **142**, 021012 (2020).
[106] J.S. Lundh, T. Zhang, Y. Zhang, Z. Xia, M. Wetherington, Y. Lei, E. Kahn, S. Rajan, M. Terrones, and S. Choi, ACS Appl. Electron. Mater. **2**, 2945 (2020).

[107] A. Bhattacharyya, P. Ranga, S. Roy, J. Ogle, L. Whittaker-Brooks, and S. Krishnamoorthy, Appl. Phys. Lett. **117**, 142102 (2020).
[108] Y. Song, D. Shoemaker, J.H. Leach, C. McGray, H.-L. Huang, A. Bhattacharyya, Y. Zhang, C.U. Gonzalez-Valle, T. Hess, S. Zhukovsky, K. Ferri, R.M. Lavelle, C. Perez, D.W. Snyder, J.-P. Maria, B. Ramos-Alvarado, X. Wang, S. Krishnamoorthy, J. Hwang, B.M. Foley, and S. Choi, ACS Appl. Mater. Interfaces (2021).
[109] B. Kwon, T. Foulkes, T. Yang, N. Miljkovic, and W.P. King, IEEE Trans. Components, Packag. Manuf. Technol. **10**, 220 (2020).
[110] S. Choi, G.M. Peake, G.A. Keeler, K.M. Geib, R.D. Briggs, T.E. Beechem, R.A. Shaffer, J. Clevenger, G.A. Patrizi, J.F. Klem, A. Tauke-Pedretti, and C.D. Nordquist, IEEE Trans. Components, Packag. Manuf. Technol. **6**, 740 (2016).
[111] A. Manoi, J.W. Pomeroy, R. Lossy, R. Pazirandeh, J. Würfl, M.J. Uren, T. Martin, and M. Kuball, Solid. State. Electron. **57**, 14 (2011).
[112] B. Chatterjee, D. Ji, A. Agarwal, S.H. Chan, S. Chowdhury, and S. Choi, IEEE Electron Device Lett. **42**, 723 (2021).
[113] S. Choi, E.R. Heller, D. Dorsey, R. Vetury, and S. Graham, IEEE Trans. Electron Devices **60**, 159 (2013).
[114] D. Altman, M. Tyhach, J. McClymonds, S. Kim, S. Graham, J. Cho, K. Goodson, D. Francis, F. Faili, F. Ejeckam, and S. Bernstein, Fourteenth Intersoc. Conf. Therm. Thermomechanical Phenom. Electron. Syst. 1199 (2014).
[115] Y. Zhou, R. Ramaneti, J. Anaya, S. Korneychuk, J. Derluyn, H. Sun, J. Pomeroy, J. Verbeeck, K. Haenen, and M. Kuball, Appl. Phys. Lett. **111**, 041901 (2017).
[116] J. Anaya, S. Rossi, M. Alomari, E. Kohn, L. Tóth, B. Pécz, K.D. Hobart, T.J. Anderson, T.I. Feygelson, B.B. Pate, and M. Kuball, Acta Mater. **103**, 141 (2016).
[117] E.O. Ziade, Thermal Transport in Thin Films and across Interfaces, Boston University, 2017.
[118] S. Jangam and S.S. Iyer, IEEE Trans. Components, Packag. Manuf. Technol. **10**, 1758 (2020).
[119] R. Mahajan, Z. Qian, R.S. Viswanath, S. Srinivasan, K. Aygün, W. Jen, S. Sharan, and A. Dhall, IEEE Trans. Components, Packag. Manuf. Technol. **9**, 1952 (2019).
[120] S.S. Iyer, S. Jangam, and B. Vaisband, IBM J. Res. Dev. **63**, 5:1 (2019).
[121] B.D. Tierney, S. Choi, S. DasGupta, J.R. Dickerson, S. Reza, R.J. Kaplar, A.G. Baca, and M.J. Marinella, IEEE Trans. Electron Devices **64**, 3740 (2017).
[122] D. Shoemaker, M. Malakoutian, B. Chatterjee, Y. Song, S. Kim, B.M. Foley, S. Graham, C.D. Nordquist, S. Chowdhury, and S. Choi, IEEE Trans. Components, Packag. Manuf. Technol. **11**, 1177 (2021).
[123] B. Chatterjee, Electro-Thermal Investigation of Next Generation Wide Bandgap Electronics, The Pennsylvania State University, 2020.
[124] C. Ren, M. Malakoutian, S. Li, and S. Chowdhury, in *2020 Device Res. Conf.* (2020), pp. 1–2.
[125] S. Lee, R. Vetury, J.D. Brown, S.R. Gibb, W.Z. Cai, J. Sun, D.S. Green, and J. Shealy, in *IEEE Int. Reliab. Phys. Symp. Proc.* (IEEE, 2008), pp. 446–449.
[126] A.R. Coutu, A.R. Lake, D.B. Christiansen, R.E. Heller, A.C. Bozada, S.B. Poling, D.G. Via, P.J. Theimer, E.S. Tetlak, R. Vetury, and B.J. Shealy, Electronics **5**, 32 (2016).

List of Peer-Reviewed Journal Articles Acknowledging the YIP Award

1. Samuel H. Kim, Daniel Shoemaker, Bikramjit Chatterjee, Andrew J. Green, Kelson D. Chabak, Eric R. Heller, Kyle J. Liddy, Gregg H. Jessen, Samuel Graham, and Sukwon Choi (2021), Thermally-aware Layout Design of β-Ga2O3 Lateral MOSFETs, IEEE Transactions on Electron Devices. *(Under review as of 10/17/2021)*
2. Sukwon Choi, Samuel Graham, Srabanti Chowdhury, Eric R. Heller, Marko J. Tadjer, Gilberto Moreno, Sreekant Narumanchi, A Perspective on the Electro-Thermal Co-Design of Ultra-Wide Bandgap Lateral Devices (2021), Applied Physics Letters *(In-press as of 10/17/2021)* **[Featured Article].**
3. Lundh, J. S. (Student Author - Graduate Student), Shoemaker, D. (Student Author - Graduate Student), Birdwell, A. G., Weil, J. D., De La Cruz, L. M., Shah, P. B., Crawford, K. G., Ivanov, T. G., Wong, H. Y., & Choi, S. (Author) (2021). Thermal performance of diamond

field-effect transistors. Applied Physics Letters 119(14), 143502. DOI: 10.1063/5.0061948 https://doi.org/10.1063/5.0061948
4. Chatterjee, B., Li, W., Nomoto, K., Xing, H. G., & Choi, S. (2021). Thermal design of multi-fin Ga2O3 vertical transistors. Applied Physics Letters 119(10), 103502. DOI: 10.1063/5.0056557 https://doi.org/10.1063/5.0056557
5. Song, Y., Shoemaker, D., Leach, J. H., McGray, C., Huang, H.-L., Bhattacharyya, A., Zhang, Y., Gonzalez-Valle, C. U., Hess, T., Zhukovsky, S., Ferri, K., Lavelle, R. M., Perez, C., Snyder, D. W., Maria, J.-P., Ramos-Alvarado, B., Wang, X., Krishnamoorthy, S., Hwang, J., Foley, B., & Choi, S. (2021). Ga2O3-on-SiC composite wafer for thermal management of ultrawide bandgap electronics. ACS Applied Materials & Interfaces 13(34), 40817–40829. DOI: 10.1021/acsami.1c09736, ISBN/ISSN: 1944-8244 https://doi.org/10.1021/acsami.1c09736
6. Song, Y., Ranga, P., Zhang, Y., Feng, Z., Huang, H.-L., Santia, M. D., Badescu, S. C., Gonzalez-Valle, C. U., Perez, C., Ferri, K., Lavelle, R. M., Snyder, D. W., Klein, B. A., Deitz, J., Baca, A. G., Maria, J.-P., Ramos-Alvarado, B., Hwang, J., Zhao, H., Wang, X., Krishnamoorthy, S., Foley, B., & Choi, S. (2021). Thermal conductivity of β-phase Ga2O3 and (AlxGa1–x)2O3 heteroepitaxial thin films. ACS Applied Materials & Interfaces 13(32), 38477–38490. DOI: 10.1021/acsami.1c08506, ISBN/ISSN: 1944-8244 https://doi.org/10.1021/acsami.1c08506
7. Shoemaker, D., Malakoutian, M., Chatterjee, B., Song, Y., Kim, S., Foley, B. M., Graham, S., Nordquist, C. D., Chowdhury, S., & Choi, S. (2021). Diamond-Incorporated Flip-Chip Integration for Thermal Management of GaN and Ultra-Wide Bandgap RF Power Amplifiers. IEEE Transactions on Components, Packaging and Manufacturing Technology, 1-1. DOI: 10.1109/TCPMT.2021.3091555
8. Lundh, J. S., Coleman, K., Song, Y., Griffin, B. A., Esteves, G., Douglas, E. A., Edstrand, A., Badescu, S. C. C., Moore, E. A., Leach, J. H., Moody, B., Trolier-McKinstry, S., & Choi, S. (2021). Residual stress analysis of aluminum nitride piezoelectric micromachined ultrasonic transducers using Raman spectroscopy. Journal of Applied Physics, 130(4), 044501. DOI: 10.1063/5.0056302. **[Editor's Pick]**.
9. Bhattacharyya, A., Roy, S., Ranga, P., Shoemaker, D., Song, Y., Lundh, J. S., Choi, S., & Krishnamoorthy, S. (2021). 130 mAmm-1 β-Ga2O3 metal semiconductor field effect transistor with low-temperature metalorganic vapor phase epitaxy-regrown ohmic contacts. Applied Physics Express, 14(7), 076502. DOI: 10.35848/1882-0786/ac07ef
10. Chatterjee, B., Ji, D., Agarwal, A., Chan, S. H., Chowdhury, S., & Choi, S. (2021). Electro-Thermal Investigation of GaN Vertical Trench MOSFETs. IEEE Electron Device Letters, 1-1. ISBN/ISSN #/Case #/DOI #: 1558-0563
11. Malakoutian, M., Song, Y., Yuan, C., Ren, C., Lundh, J. S., Lavelle, R. M., Brown, J. E., Snyder, D. W., Graham, S., Choi, S., & Chowdhury, S. (2021). Polycrystalline diamond growth on β-Ga2O3 for thermal management. Applied Physics Express. http://iopscience.iop.org/article/10.35848/1882-0786/abf4f1.
12. Kim, J., Lee, S., Song, Y., Choi, S., An, J., & Cho, J. (2021). Thermal conductivity of plasma-enhanced atomic layer deposited hafnium zirconium oxide dielectric thin films. Journal of the European Ceramic Society. ISBN/ISSN #/Case #/DOI #: 0955-2219 https://www.sciencedirect.com/science/article/pii/S0955221921000017.
13. Warzoha, R., Wilson, Adam/A, Donovan, B., Donmezer, N., Giri, A., Hopkins, P., Choi, S., Pahinkar, D., Shi, J., Graham, S., Tian, Z., & Ruppalt, L. (2020). Applications and Impacts

of Nanoscale Thermal Transport in Electronics Packaging. Journal of Electronic Packaging. ISBN/ISSN #/Case #/DOI #: 1043-7398 https://doi.org/10.1115/1.4049293.
14. Chatterjee, B., Song, Y., Lundh, J. S., Zhang, Y., Xia, Z., Islam, Z., Leach, J., McGray, C., Ranga, P., Krishnamoorthy, S., Haque, A., Rajan, S., & Choi, S. (2020). Electro-thermal co-design of β-(AlxGa1-x)2O3/Ga2O3 modulation doped field effect transistors. Applied Physics Letters, 117(15), 153501. https://aip.scitation.org/doi/abs/10.1063/5.0021275.
15. Chatterjee, B., Lundh, J. S., Song, Y., Shoemaker, D., Baca, A. G., Kaplar, R. J., Beechem, T. E., Saltonstall, C., Allerman, A. A., Armstrong, A. M., Klein, B. A., Bansal, A., Seyf, H. R., Talreja, D., Pogrebnyakov, A., Heller, E., Gopalan, V., Henry, A. S., Redwing, J. M., Foley, B., & Choi, S. (2020). Interdependence of Electronic and Thermal Transport in AlxGa1-xN Channel HEMTs. IEEE Electron Device Letters, , 41(3), 461-464. ISBN/ISSN #/Case #/DOI #: 1558-0563
16. Wang, W., Chen, J., Lundh, J. S., Shervin, S., Oh, S. K., Pouladi, S., Rao, Z., Kim, J. Y., Kwon, M.-K., Li, X., Choi, S., & Ryou, J.-H. (2020). Modulation of the two-dimensional electron gas channel in flexible AlGaN/GaN high-electron-mobility transistors by mechanical bending. Applied Physics Letters, 116(12), 123501. **[Editor's Pick]**.
17. Chatterjee, B., Dundar, C., Beechem, T. E., Heller, E., Kendig, D., Kim, H., Donmezer, N., & Choi, S. (2020). Nanoscale electro-thermal interactions in AlGaN/GaN high electron mobility transistors. Journal of Applied Physics, 127(4), 044502. **[Featured Article]**.
18. Lundh, J. S., Zhang, T., Zhang, Y., Xia, Z., Wetherington, M., Lei, Y., Kahn, E., Rajan, S., Terrones Maldonado, M., & Choi, S. (2020). 2D materials for universal thermal imaging of micro- and nanodevices: An application to gallium oxide electronics. American Chemical Society (ACS) Applied Electronic Materials, 2, 2945-2953. https://doi.org/10.1021/acsaelm.0c00574.
19. de Bock, P., Huitink, D., Shamberger, P. J., Lundh, J., Choi, S., Niedbalski, N., & Boteler, L. (2020). A System to Package Perspective On Transient Thermal Management of Electronics. Journal of Electronic Packaging. ISBN/ISSN #/Case #/DOI #: 1043-7398
20. Song, Y., Lundh, J., Wang, W., Leach, J., Eichfeld, D., Krishnan, A., Perez, C., Ji, D., Borman, T., Ferri, K., Maria, J.-P., Chowdhury, S., Ryou, J.-H., Foley, B., & Choi, S. (2020). The Doping Dependence of the Thermal Conductivity of Bulk Gallium Nitride Substrates. Journal of Electronic Packaging. 142(4): 041112. ISBN/ISSN #/Case #/DOI #: 1043-7398
21. Chatterjee, B., Lundh, J. S., Shoemaker, D., Kim, T. K., Kim, H., Giebnik, N. C., Kwak, J. S., Cho, J., & Choi, S. (2020). Characterization of the Interdependence Between the Light Output and Self-Heating of Gallium Nitride Light-Emitting Diodes. Journal of Electronic Packaging, 142(3). ISBN/ISSN #/Case #/DOI #: 1043-7398
22. Lundh, J. S., Song, Y., Chatterjee, B., Baca, A. G., Kaplar, R. J., Armstrong, A. M., Allerman, A. A., Klein, B. A., Kendig, D., Kim, H., & Choi, S. (2020). Device-Level Multidimensional Thermal Dynamics With Implications for Current and Future Wide Bandgap Electronics. Journal of Electronic Packaging, 142(3), 031113. ISBN/ISSN #/Case #/DOI #: 1043-7398
23. Pearson, R., Chatterjee, B., Kim, S., Graham, S., Rattner, A., & Choi, S. (2020). Guidelines for Reduced-Order Thermal Modeling of Multifinger GaN HEMTs. Journal of Electronic Packaging, 142(2). ISBN/ISSN #/Case #/DOI #: 1043-7398
24. Chatterjee, B., Shoemaker, D., Song, Y., Shi, T., Huang, H.-L., Keum, D., Krishnan, A., Foley, B., Hwang, J., Kim, H., & Choi, S. (2020). Cumulative Impacts of Proton Irradiation on the Self-Heating of AlGaN/GaN HEMTs. ACS Applied Electronic Materials.

25. Chatterjee, B., Zeng, K., Nordquist, C. D., Singisetti, U., & Choi, S. (2019). Device-level thermal management of gallium oxide field-effect transistors. IEEE Transactions on Components, Packaging and Manufacturing Technology, 9(12), 2352-2365. ISBN/ISSN #/Case #/DOI #: 2156-3985
26. Shrestha, R., Luan, Y., Shin, S., Zhang, T., Luo, X., Lundh, J. S., Gong, W., Bockstaller, M. R., Choi, S., Luo, T., Chen, R., Hippalgaonkar, K., & Shen, S. (2019). High-contrast and reversible polymer thermal regulator by structural phase transition. Science Advances, 5(12).
27. Lundh, J. S., Chatterjee, B., Song, Y., Baca, A. G., Kaplar, R. J., Beechem, T. E., Allerman, A. A., Armstrong, A. M., Klein, B. A., Bansal, A., Talreja, D., Pogrebnyakov, A., Heller, E., Gopalan, V., Redwing, J. M., Foley, B. M., & Choi, S. (2019). Multidimensional thermal analysis of an ultrawide bandgap AlGaN channel high electron mobility transistor. Applied Physics Letters, 115(15), 153503.
28. Wang, W., Lee, S. M., Pouladi, S., Chen, J., Shervin, S., Yoon, S., Yum, J. H., Larsen, E. S., Bielawski, C. W., Chatterjee, B., Choi, S., Oh, J., & Ryou, J.-H. (2019). Polarization modulation effect of BeO on AlGaN/GaN high-electron-mobility transistors. Applied Physics Letters, 115(10), 103502.
29. Bansal, A., Wang, K., Lundh, J. S., Choi, S., & Redwing, J. M. (2019). Effect of Ge doping on growth stress and conductivity in AlxGa1-xN. Applied Physics Letters, 114(14), 142101.
30. Oh, S. K., Lundh, J. S., Shervin, S., Chatterjee, B., Lee, D. K., Choi, S., Kwak, J. S., & Ryou, J.-H. (2019). Thermal management and characterization of high-power wide-bandgap semiconductor electronic and photonic devices in automotive applications. Journal of Electronic Packaging, 141(2), 20801--20817. ISBN/ISSN #/Case #/DOI #: 1043-7398
31. Chatterjee, B., Jayawardena, A., Heller, E., Snyder, D. W., Dhar, S., & Choi, S. (2018). Thermal characterization of gallium oxide Schottky barrier diodes. Review of Scientific Instruments, 89(11), 114903.
32. Shrestha, R., Li, P., Chatterjee, B., Zheng, T., Wu, X., Liu, Z., Luo, T., Choi, S., Hippalgaonkar, K., de Boer, M. P., & Shen, S. (2018). Crystalline polymer nanofibers with ultra-high strength and thermal conductivity. Nature communications, 9.
33. Dallas, J., Pavlidis, G., Chatterjee, B., Lundh, J. S., Ji, M., Kim, J., Kao, T.-H., Detchprohm, T., Dupuis, R. D., Shen, S., Graham, S., & Choi, S. (2018). Thermal characterization of gallium nitride p-i-n diodes. Applied Physics Letters, 112(7), 073503.
34. Kim, T. K., Cho, M. U., Lee, J. M., Cha, Y.-J., Oh, S. K., Chatterjee, B., Ryou, J.-H., Choi, S., & Kwak, J. S. (2018). Improved light output power of 16×16 pixelated micro-LEDs for headlights by enhancing the reflectivity and coverage of the p-electrode. Physica Status Solidi (a), 1700571--n/a. ISBN/ISSN #/Case #/DOI #: 1862-6319
35. Oh, S. K., Cho, M. U., Dallas, J., Jang, T., Lee, D. G., Pouladi, S., Chen, J., Wang, W., Shervin, S., Kim, H., Shin, S., Choi, S., Kwak, J. S., & Ryou, J.-H. (2017). High-power flexible AlGaN/GaN heterostructure field-effect transistors with suppression of negative differential conductance. Applied Physics Letters, 111(13), 133502.

List of Peer-Reviewed Conference Proceedings Acknowledging the YIP Award

1. Kim, S. H., Shoemaker, D., Chatterjee, B., Chabak, K. D., Green, A. J., Liddy, K. J., Jessen, G. H., Graham, S., & Choi, S. (2021). The effectiveness of heat extraction by the drain metal contact of β-Ga2O3 MOSFETs. 2021 20th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (iTherm). (pp. 324-327). DOI:

10.1109/ITherm51669.2021.9503276
2. Song, Y., Chatterjee, B., McGray, C., Zhukovsky, S., Leach, J. H., Hess, T., Foley, B., & Choi, S. (2020). Characterization of the thermal boundary resistance of a Ga2O3/4H-SiC composite wafer. 2020 19th Institute of Electrical and Electronics Engineers (IEEE) Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm). (pp. 154-157). ISBN/ISSN #/Case #/DOI #: 2577-0799
3. Chatterjee, B., Lundh, J. S., Shoemaker, D., Kim, T. K., Kwak, J. S., Cho, J., & Choi, S. (2019). Correlated Effects of Self-Heating, Light Output, and Efficiency of GaN Light-Emitting Diodes on Junction Temperature. ASME 2019 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems.
4. Lundh, J. S., Song, Y., Chatterjee, B., Baca, A. G., Kaplar, R. J., Armstrong, A. M., Allerman, A. A., Kim, H., & Choi, S. (2019). Integrated Optical Probing of the Thermal Dynamics of Wide Bandgap Power Electronics. ASME 2019 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems.
5. Chatterjee, B., Kim, T. K., Song, Y., Lundh, J. S., Han, S.-W., Shoemaker, D., Lee, J. M., Cho, M. U., Chu, R., Kwak, J. S., & Choi, S. (2019). Enhancement of the electrical and thermal performance of AlGaN/GaN HEMTs using a novel resistive field plate structure. 2019 18th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm). (pp. 362-369). ISBN/ISSN #/Case #/DOI #: 1087-9870
6. Chatterjee, B., Leach, J. H., Dhar, S., & Choi, S. (2018). Temperature and stress metrology of ultra-wide bandgap β-Ga2O3 thin films. 2018 17th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm). (pp. 202-207). ISBN/ISSN #/Case #/DOI #: 2577-0799