AFRL-AFOSR-UK-TR-2022-0001

Study of growth mechanism and planar defect formation in Beta-(AlxGa1-x)2O3/Ga2O3 heterostructures grown by MOVPE on differently oriented Beta-Ga2O3 substrates

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10/14/2021
Final Technical Report

Air Force Research Laboratory
Air Force Office of Scientific Research
European Office of Aerospace Research and Development
Unit 4515 Box 14, APO AE 09421

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*
14-10-2021

2. REPORT TYPE
Final

3. DATES COVERED *(From - To)*
15 Jul 2017 - 14 Jul 2021

4. TITLE AND SUBTITLE
Study of growth mechanism and planar defect formation in Beta-(AlxGa1-x)2O3/Ga2O3 heterostructures grown by MOVPE on differently oriented Beta-Ga2O3 substrates

5a. CONTRACT NUMBER

5b. GRANT NUMBER
FA9550-17-1-0279

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
Andreas Popp

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
FORSCHUNGSVERBUND BERLIN E.V.
RUDOWER CHAUSSEE 17
BERLIN, BERLIN 12489
DEU

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
EOARD
UNIT 4515
APO AE 09421-4515

10. SPONSOR/MONITOR'S ACRONYM(S)
AFRL/AFOSR IOE

11. SPONSOR/MONITOR'S REPORT NUMBER(S)
AFRL-AFOSR-UK-TR-2022-0001

12. DISTRIBUTION/AVAILABILITY STATEMENT
A Distribution Unlimited: PB Public Release

13. SUPPLEMENTARY NOTES

14. ABSTRACT

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15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			**17. LIMITATION OF ABSTRACT**	**18. NUMBER OF PAGES**	**19a. NAME OF RESPONSIBLE PERSON** JASON FOLEY
a. REPORT	**b. ABSTRACT**	**c. THIS PAGE**			**19b. TELEPHONE NUMBER** *(Include area code)* 555-555-5555
U	U	U	SAR	8	

Final Performance Report for EOARD Grant FA9550-17-1-0279

ß-Ga_2O_3 layers by MOVPE

September 30th 2021

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Period of Performance: 07/15/2017 – 07/14/2021

Abstract

β-Ga_2O_3 has a high potential to be used as material for high power switching devices. In this work the growth of homoepitaxial β-Ga_2O_3 layers by metal-organic vapor phase epitaxy (MOVPE) on (010) and (100) oriented substrates has been investigated. For device applications like MOSFETs, the interface properties between layers with different doping concentrations are crucial. Therefore, the deposition of modulation Si-doped layer structures, the investigation of interface properties and the study of the influence of substrate orientation are the main goals of this work. The substrate interface layer, as well as the interfaces between layers with different doping levels play an important role for the device performance. Si depth profiles measured by SIMS revealed a gradual junction between layers with different doping regimes for multilayers grown on (010) substrates, while multilayer grown on (100) 6° off oriented wafers show sharp interfaces. Using of (100) oriented substrates may reduce the leakage current and improve the device performance, pointing out at the same time a direction for device development.

Introduction

The oxide material system beta-gallium oxide (β-Ga_2O_3) is an emerging ultra-wide bandgap (4.8 eV) [1] semiconductor which is characterized by a theoretical breakdown field strength of about 8 MV/cm [2]. Due to these properties β-Ga_2O_3 has the potential to outperform SiC and GaN and to become the next generation of high-performance material for power electronic applications. Transistors based on β-Ga_2O_3 benefit from a low on-resistance at a given breakdown voltage, this leads to less power losses within a transistor switching operation [3]. The electrically active part of the device is thereby made up of a homoepitaxial thin layer. In this work we report about the homoepitaxial growth and characterization of (010) and (100) β-Ga_2O_3 layers by MOVPE.

Experiment and Results:

The layers were grown by using a vertical showerhead low-pressure MOVPE system (SMI Inc., USA). Triethylgallium (TEGa), O_2 gas and tetraethylorthosilicate (TEOS) were used as gallium, oxygen and Si sources, respectively. High-purity Ar worked as a carrier gas. For comparison (100) 6° off and (010) oriented ß-Ga_2O_3 substrates were used. The (100) oriented substrates were grown in house at IKZ by using the Czochralski method [4]. The wafering was performed by the CrysTec GmbH. The (010) oriented substrates were provided by Tamura and were grown by using edge defined film-fed-growth (EFG) technic. The (100) oriented substrates were pretreated consisting an etching step with phosphoric acid followed by an annealing step at 900°C under oxygen atmosphere to remove the damage layer due to polishing and to achieve an epi-ready surface. For the (010) substrate such a treatment is not necessary. However, both kinds of substrates where treated with a HF dilution for 5 min direct prior the growth procedure. The growth process was performed at 825° C and 5 mbar chamber pressure since these parameters were found to result in layers with best quality. To minimize in-plane inhomogeneity the susceptor was rotated at 500 rpm.

The morphology was analyzed by AFM (Bruker Dimension Icon) and the thickness of the layers was determined by spectroscopic ellipsometry (HORIBA Scientific UVISEL plus). The depth profile and the silicon concentration of the multilayer stack was measured by using secondary ion mass spectroscopy (SIMS) at RTG Mikroanalyse GmbH Berlin. The shape of the interfaces between the layers and the structural perfection were analyzed by SIMS and transmission electron microscopy (TEM), respectively.

Growth of delta-doped ß-Ga_2O_3 layers by MOVPE:

Our project partner the Air Force Research Laboratories (AFRL) fabricates MOSFET architectures on our ß-Ga_2O_3 layers. By using a delta doped multilayers structure an increase of the channel mobility is expected. Therefore, a multilayer structure of low and highly doped layers are necessary. Since 2017 a silicon doping range from $10^{17} – 10^{19}$ is achievable at IKZ [5]. As already well known the charge carrier mobility decreases with increasing charge carrier density. To combine both, a high doping concentration and a high mobility, the growth of delta-doped layers are necessary to form a potential well with the aim to provide electrons with a high mobility out of the highly doped layer into the low doped channel.

For this purpose stacking layer structures with the following shape were grown (see Fig. 1). On (010) oriented ß-Ga_2O_3 substrates 175 nm thick a low silicon doped (LD) layer was deposited followed by a very thin (few nm) highly silicon doped layer (HD). The structure was closed by another 20 nm LD layer.

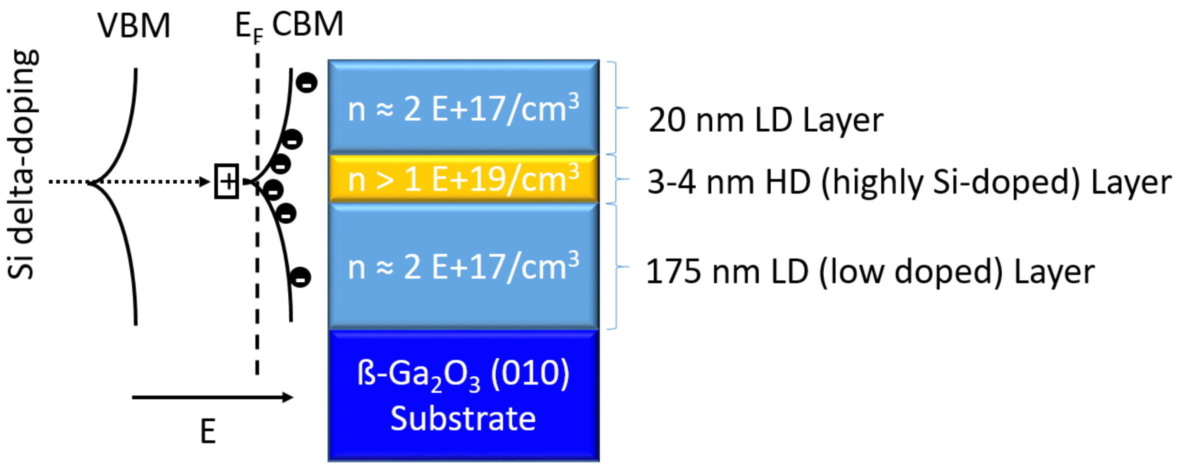

Figure 1 Scheme and structure of the desired delta doped layers.

Before the growth of the full stacking layer, several depositions run were performed to find the optimal growth conditions to grow good quality LD and HD layers. To check the electrical and morphological properties of the LD and HD layers two growth runs were performed separately.

1. Low doped: 175 nm with a desired n-type doping (Si) of $2{\cdot}10^{17}$cm^{-3}
2. High doped: 175 nm with a desired n-type doping (Si) of > $1{\cdot}10^{19}$cm^{-3} (to check the electrical properties this layer thickness was necessary)

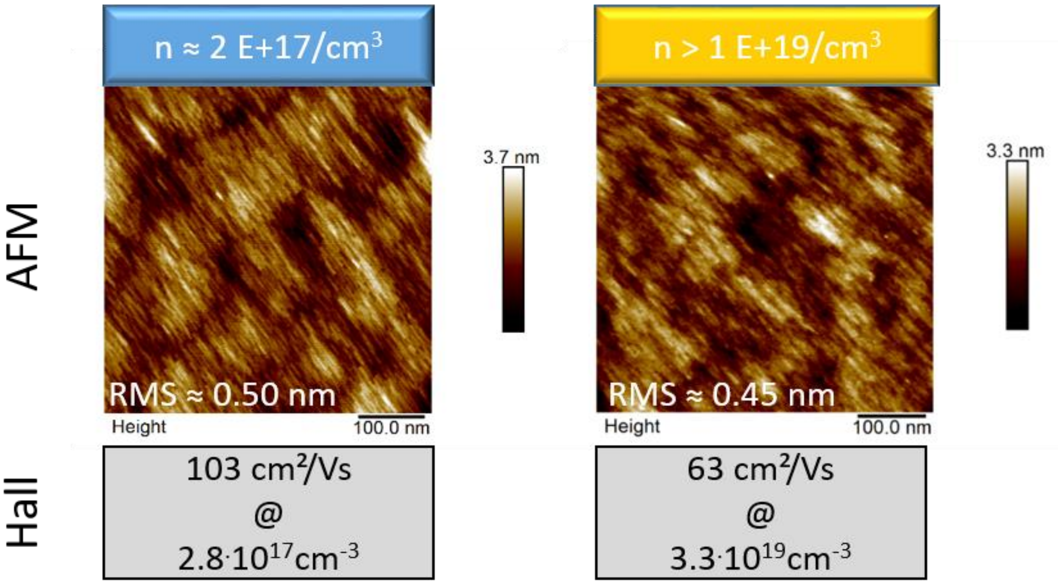

Figure 2 AFM and Hall results of the low doped and high doped 175 nm thick layers on (010) substrates.

Figure 2 shows the results for the separately grown low and high doped layers on (010) oriented ß-Ga$_2$O$_3$ substrates. Both showing smooth surfaces with typically faceted morphology with elongated features. The Hall measurements show that the desired doping concentration and mobility for both layers have been achieved.

These results allowed to go a step further to grow stacking layer. The critical points for delta doped layer are sharp interfaces between layers with different doping levels, since a blurred interface leads to a scattering of free charge carriers resulting in a decrease of the mobility. The idea is to provide electrons with a high mobility out of the HD layer into the LD layers to increase the channel mobility. To investigate the interface sharpness between the different layers test structures with thicker HD layer were grown (Fig. 3). These stacking layers with respect to the Si depth profile have been investigated by secondary ion mass spectroscopy. In addition, these test structures will also show if a Si memory effect is caused by the high doped layer and if a doping plateau is achievable.

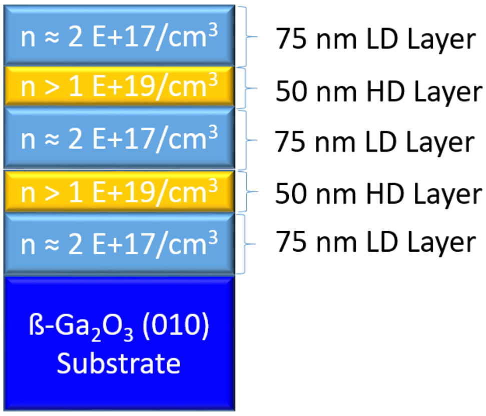

Figure 3 Scheme of the test structure.

Figure 4 (left) shows the morphology of the test stacking layer obtained by AFM. A flat and smooth surface is visible. The Si depth profile obtained by SIMS (Fig. 4 right) mainly contains three information:

1. A doping plateau has been achieved for both high doped layer.
2. The minimum doping level seems to increase with the layer thickness. This could be a hint for a memory effect.
3. A gradual junction from high doped to low doped layer is strongly visible.

A possible reason for this gradual junction could by the faceted surface of the (010) oriented layer. The actual growth in this case takes place on the facets which are oriented in the (110) direction [6,7]. This leads to a rougher surface compared to the (100) orientation with step flow. In contrast, the (100) orientation is a cleavage plane and has the lowest surface energy. These properties of the (100) orientation are good prerequisites for sharp interfaces between layers with different doping regimes.

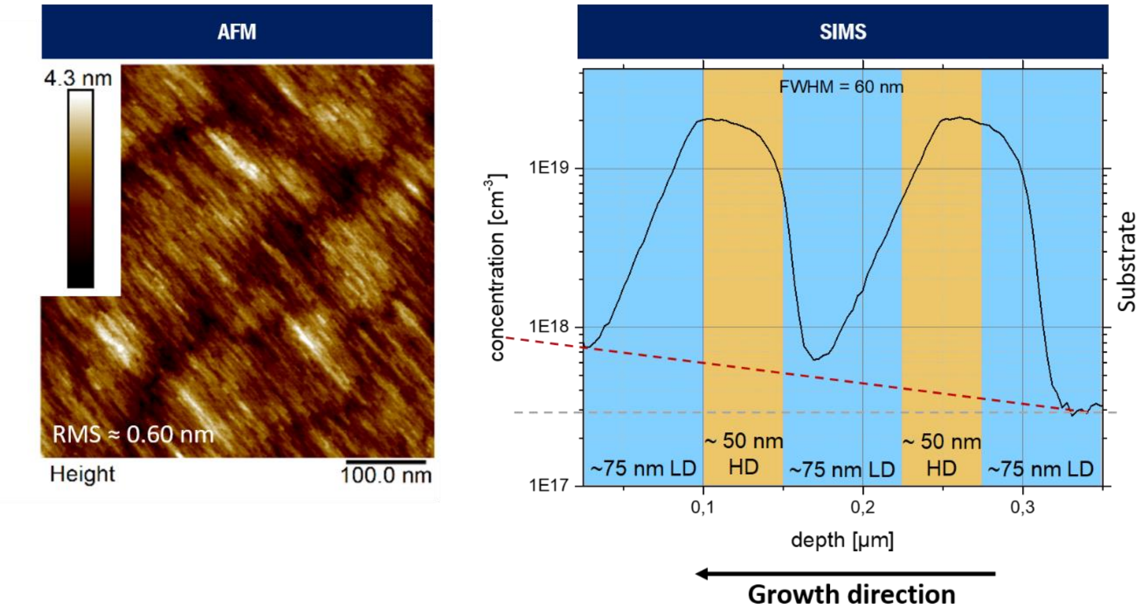

Figure 4 AFM image (left) and SIMS results (right) of the test stacking layer structure grown on a (010) oriented substrate.

Therefore, experiments were performed on substrates with two different orientations in the same growth run, (010) and (100)6° off to investigate the influence of the substrate orientation on the Si depth profile. The structure of the stacking layer was set to three low doped layers (75 nm thick for every layer) and in between two (15 nm thick layer) highly doped.

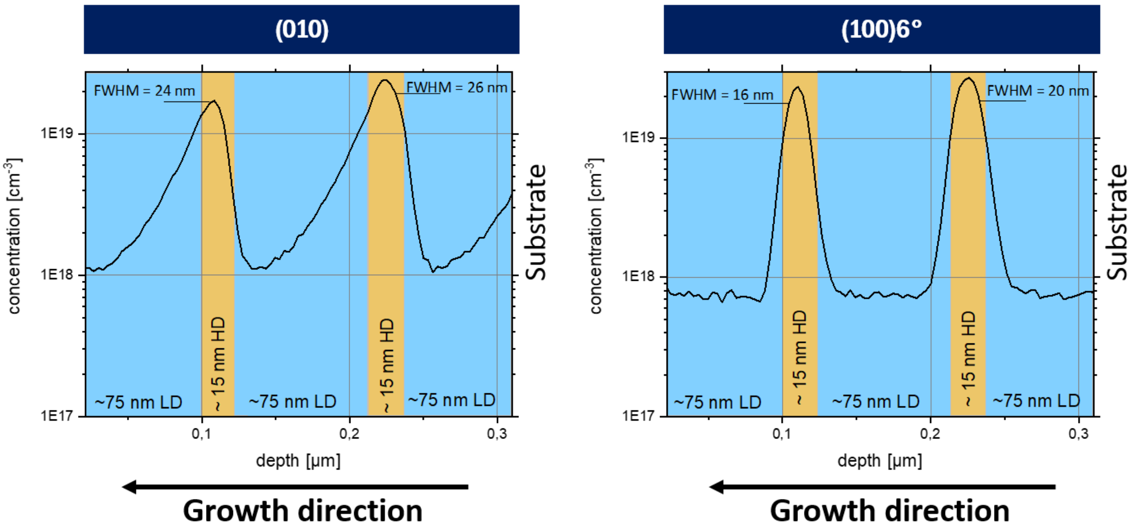

Figure 5 SIMS Si depth profiles of the test structures grown on a (010) and a (100)6°off oriented substrate.

The SIMS results depicted in Fig. 5 showing the Si depth profiles for the structures grown in the same run on (010) and (100)6° off oriented substrates. For both cases no Si memory effect is visible. But in case of (010) again a gradual junction from high to low doped regime has been found with a FWHM of around 25 nm. In contrast, the Si depth profile of the stacking layer grown on (100)6° off oriented substrate shows sharp interfaces between HD and LD layer leading to a smaller FWHM of 16 nm. This points out that the substrate orientation seems to have a big influence on the interface morphology which is the critical point for generating sharp interfaces.

Therefore, the growth of the desired stacking layer (see Fig. 1) was performed on a (010) and a (100)6° off substrate in parallel with the aim to compare the later device based on such structures at AFRL. In Fig. 6 the morphologies measured by AFM of these multilayers grown on (010) and (100)6° off oriented ß-Ga_2O_3 substrates are visible.

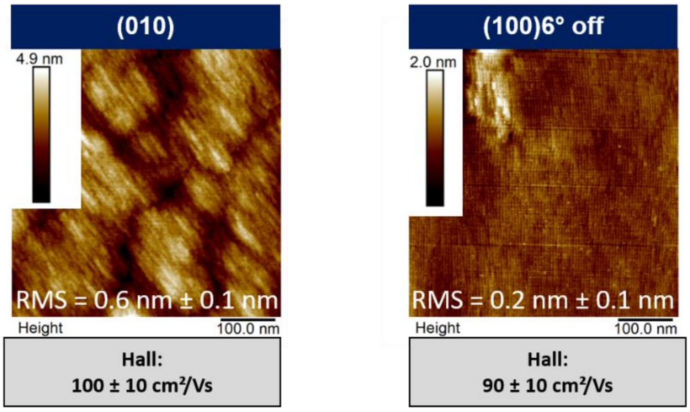

Figure 6 AFM and Hall results of the grown layer with desired structure on (010) and (100)6° off oriented substrates.

On the (010) the faceted growth leads to a surface roughness of ≈ 0.60 nm (RMS) while for the stacking layer grown on (100) 6° off step flow growth is visible resulting in a smooth surface with a RMS value of ≈ 0.20 nm, which is one third compared to the (010) case. The electrical properties measured by Hall show comparable high mobilities for both orientations, just slightly lower for the (100) case. The reason for that can be found by a structural investigation with TEM (see Fig. 7).

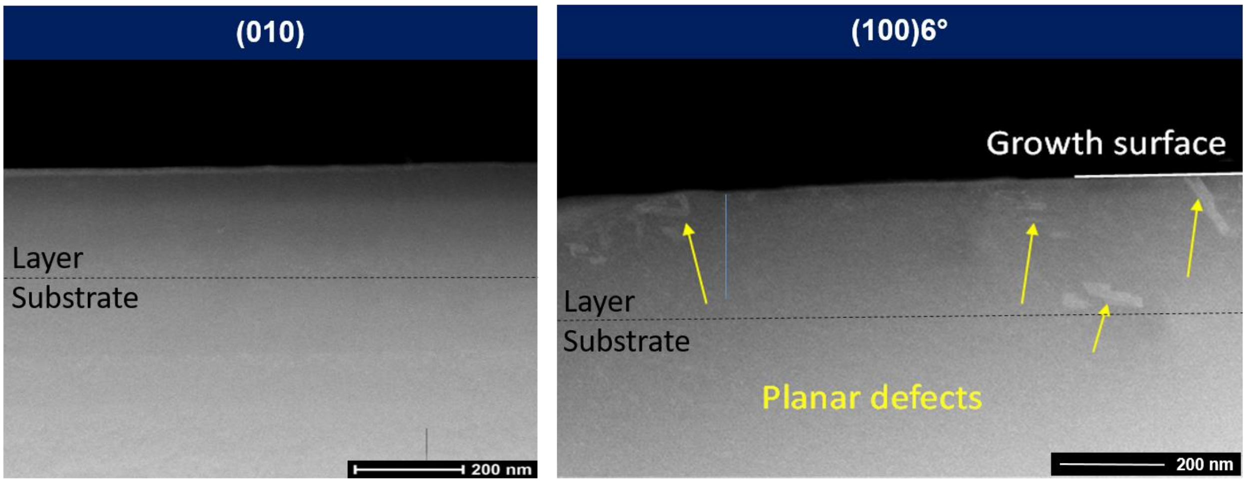

Figure 7 TEM results for the stacking layer grown on (010) and (100) 6° off oriented substrates.

The layer grown on (010) is characterized by an almost perfect structure with low defect density. The stacking layer on the (100)6° off substrate still shows some planar defects. This is in good agreement with the results from Hall. Since a defect means a compensation center, for the layer on (100) some free charge carriers has been trapped by defects which results in a lower mobility as shown in Fig. 6. These issue should be able to be bypassed by optimizing the provided offcut of the used substrate to adjust the diffusion length of the Ga adatoms to the terrace width of the surface steps [8].

Summery:

This work showed the influence of the substrate orientation on Si-depth profiles with respect to ß-Ga_2O_3 multilayer with different Si doping regimes. The SIMS Si-depth profiles for multilayer grown on (010) oriented substrate shows a gradual transition from high to low Si doping regions. The reason seems to be the surface morphology. For the faceted (010) layer surface the incorporation of Si seems to be inhomogeneous resulting in blurred interfaces. The Si-depth profiles of the multilayers grown on (100)6° off substrates instead show sharp interfaces between the high and low doping regions since the (100) orientation is a cleavage plane with the lowest surface energy. Therefore, the use of (100) oriented substrates may improve the device performance while the surface morphology seems to be the key point. The step flow growth on (100) off oriented substrates results in smooth layer surfaces with sharp interfaces, for layers grown on the (010) surface in turns it seems to be easier to achieve a lower defect density. Therefore, a combination of both advantages would be an interesting future direction. A certain off-cut also for the (010) orientation could suppress rotational domains to realize a step flow growth also on the (010) surface.

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Publications:

The performed work for the material development for lateral power devices made in this project was the base for three peer review publications by AFRL:

Title: “*Self-Heating Characterization of β-Ga2O3 Thin-Channel MOSFETs by Pulsed I-V and Raman Nanothermography*"

Authors: Nicholas A. Blumenschein, Neil A. Moser, Eric R. Heller, Nicholas C. Miller, Andrew J. Green, Andreas Popp, Antonio Crespo, Kevin Leedy, Miles Lindquist, Taylor Moule, Stefano Dalcanale, Elisha Mercado, Manikant Singh, James W. Pomeroy, Martin Kuball, Gunter Wagner, Tania Paskova, John F. Muth, Kelson D. Chabak ; Gregg H. Jessen

Citation: N. A. Blumenschein et al., *IEEE Transactions on Electron Devices*, vol. 67, no. 1, pp. 204-211, Jan. 2020,
doi: 10.1109/TED.2019.2951502

Title: “*Thin Channel β-Ga2O3 MOSFETs with Self-Aligned Refractory Metal Gates*"

Authors: Liddy, Kyle; Green, Andrew; Hendricks, Nolan; Heller, Eric; Moser, Neil;Leedy, Kevin; Popp, Andreas; Lindquist, Miles; Tetlak, Stephen; Wagner, Guenter; Chabak, Kelson; JESSEN, Gregg

Citation: Liddy et al., 2019 *Appl. Phys. Express*
doi: 10.7567/1882-0786/ab4d1c

Title: *“Lateral β-Ga2O3 field effect transistors”*

Authors: Kelson D. Chabak, Kevin D. Leedy, Andrew J. Green, Shin Mou, Adam T. Neal, Thaddeus Asel, Eric R. Heller, Nolan S. Hendricks, Miles T. Lindquist, Antonio Crespo, Nicholas C. Miller, Kyle Liddy, Neil A. Moser, Robert C. Fitch Jr. , Dennis E. Walker Jr. , Donald L. Dorsey, Gregg H. Jessen

Citation: Kelson D Chabak *et al* 2020 *Semicond. Sci. Technol.* **35** 013002
doi: 10.1109/LED.2017.2694805