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Developing Computational Algorithms to Predict the Quality of High Voltage GaN Diodes Using Data Science and Machine Learning- FY21 Naval Innovative Science and Engineering (NISE) Final Report

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14. ABSTRACT

A major roadblock in developing GaN power electronic devices is the reliable manufacturing of substrates and epitaxial layers, thus there is a need to develop quick, non-destructive techniques for predicting the quality of devices fabricated on wafers. This research project focused on collecting large data sets on vertical PiN diodes to developed computational algorithms for doing this. Specifically, Raman spectroscopy was used to detect high crystal stress points associated with higher leakage currents, and machine learning was applied to optical profilometry images to predict the quality of vertical PiN diodes. It was found that high crystal stress points detected by Raman doubled that chance of a high leakage failure, and machine learning was 91% effective at predicting the forward bias conductions using optical profilometry. This results from the research will help future GaN projects screen wafers and epi, saving the costly fabrication process of devices.

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CONTENTS

1. INTRODUCTION 2
2. COLLECTING OPTICAL DATA FOR INPUT PARAMETERS 2
3. DEVICE FABRICATION 3
4. COLLECTING ELECTRICAL DATA FOR OUTPUT PARAMETERS 4
5. CONCLUSIONS 7

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DEVELOPING COMPUTATIONAL ALGORITHMS TO PREDICT THE QUALITY OF HIGH VOLTAGE GAN DIODES USING DATA SCIENCE AND MACHINE LEARNING - FY21 NAVAL INNOIVATIVE SCIENCE AND ENGINEERING (NISE) FINAL REPORT

1. INTRODUCTION

A major goal of the Naval Power and Energy Systems Technology Development Roadmap is to develop wide bandgap semiconductor power switching technology capable of handling loads over 15 kV DC. However, with current SiC technology created payloads about 15 kV is infeasible. Vertical diodes and Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) based on GaN can theoretically achieve 20 kV DC loads. Unfortunately, GaN wafer technology is immature and produces inconsistent results, thus a need to develop quick, non-destructive techniques for predicting the quality of the wafers is essential. Multiple techniques have been proposed to fulfil this role from previous NRL projects [1], [2].

In a previous NRL Karles Fellowship project [3], it was determined that points of high crystal stress can be detected using Raman spectroscopy and increase the leakage currents of MESA isolated diodes by several order of magnitude. Additionally, optical profilometry was determined to be able to accurately estimate the yield of wafers. The objective of this NISE project was to improve the accuracy of these methods and develop higher quality diodes for efficient fabrication of wafers with particular focus on using data science and machine learning techniques.

In order to develop algorithms for accurately predict the quality of the diodes, a set of input and output data must be acquired. For this project the input data consisted of Raman spectroscopy and Optical profilometry data and the output consisting of IV curves taken after vertical PiN diodes were fabricated on the sample.

2. COLLECTING OPTICAL DATA FOR INPUT PARAMETERS

The input data for developing a mathematical algorithm or training a machine learning model included Raman spectroscopy and optical profilometry are useful for detecting the uniformity of the wafers and epitaxial layers. In particular, Raman spectroscopy can be used to detect variations in crystal stress and electron carrier concentration; while optical profilometry can be used to detect abnormal surface features, which likely resulted from defects in the substrates or epitaxial layers. This section discusses these techniques in detail and how data was collected for research.

Raman spectra were excited using a 532 nm laser, and was taken over larger sample areas. The samples were type IIa- having a regular pattern of crystal defects as defined in a previous project. Two peaks in the spectra were used to identify regions of defect. First, the E_2 peak was used to determine changes in crystal stress. These stress points typically indicate a higher concentration of defects. The defects often results in increased electron carrier concentrations detected by shifts in the A_1 (LO) peak [3]. Detailed descriptions of these peaks and methods for calculating carrier concentration can be found in Kuball's work [4].

To fabricate diodes with a variety of conditions, the Raman spectra was used to align diodes to the regular pattern of crystal stress points. **Figure 1a** shows the A_1 (LO) peak revealing the sample has regular patterns of circular areas with higher carrier concentration. **Figure 2b** shows the E_2 peak in a similar region. There are small red regions representing a small change in crystal stress roughly at the center of the circular areas in **Figure 1a**, suggesting that the changes in crystal stress cause the increased carrier

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concentration. Note that the E_2 peak shift is very small (~0.1 cm^{-1}) thus it is difficult to detect. Using the center of the A_1 (LO) features is much easier to detect thus more reliable.

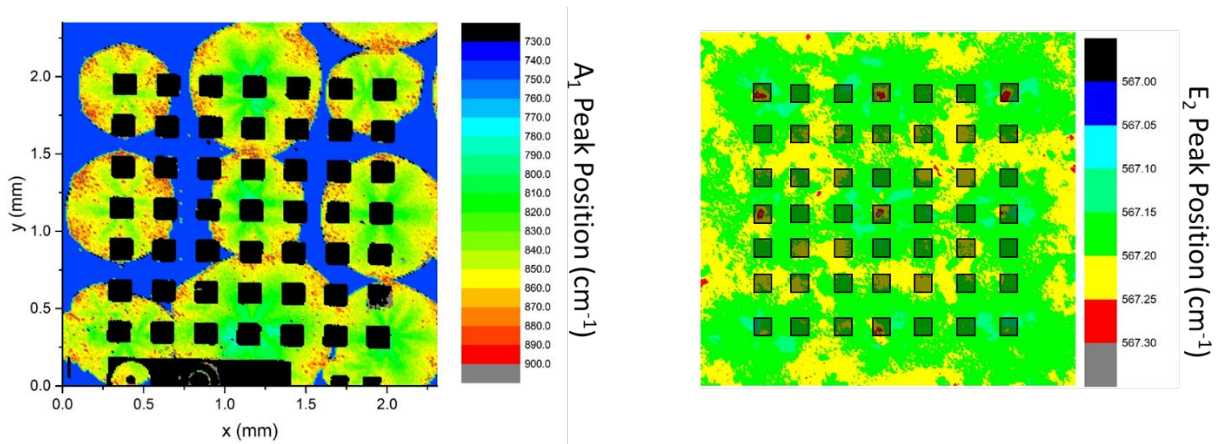

Fig 1. Raman spectra of the A_1 (LO) peak (left) and E_2 peak (right) in a similar region. The black boxes represent areas the anode metal of vertical devices covered.

Optical profilometry can be taken using the Zygo™ Optical profilometer in the Nanoscience Institute and is used to detect abnormal spots on the surface of the wafers. These abnormalities can be caused by defects below the surface of the wafer, which can cause catastrophic failure; however, many of the surface defects produced are benign, thus it will take a more complex algorithm to determine the effect these have on device performance. From this method, however, regions of high probability of catastrophic failure can be detected by finding large bumps or pits on the wafer. An example optical profilometry image is shown in **Figure 2**. From this figure several bumps and pits are observed, including at the regions of high crystal stress detected by Raman spectroscopy.

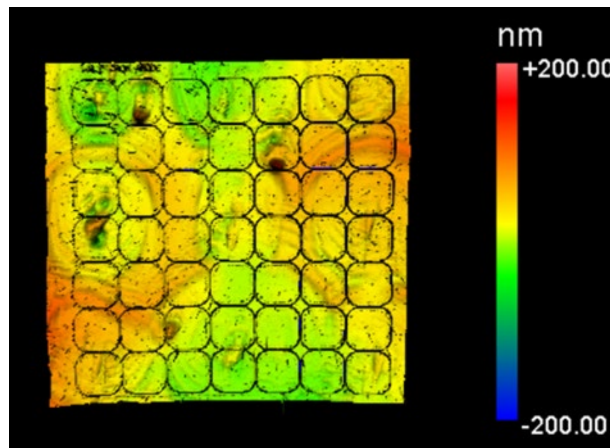

Fig 2. Optical profilometry map of the diodes before device fabrication of the same region as **Figure 1a**. The positions of the devices are separated by a trench etched using a Cl_2 plasma.

3. DEVICE FABRICATION

Generating the output data to In previous research the diodes were fabricated with a MESA isolation created by a Cl_2 etch [3]; however, for this project the trench isolation was combined with an implant isolation and Junction Termination Extension layers created using a N_2 implant. A diagram of the diodes

is shown in **Figure 3.** These diodes were fabricated in grid 7x7 devices long as displayed in **figures 1 and 2.** This fabrication pattern meant that 9 of the 49 diodes were on the high crystal stress points.

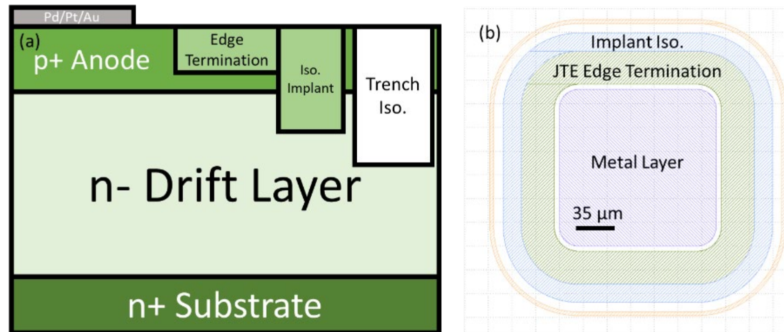

Fig 3. A side view (a) and a top view (b) diagram of the sample design.

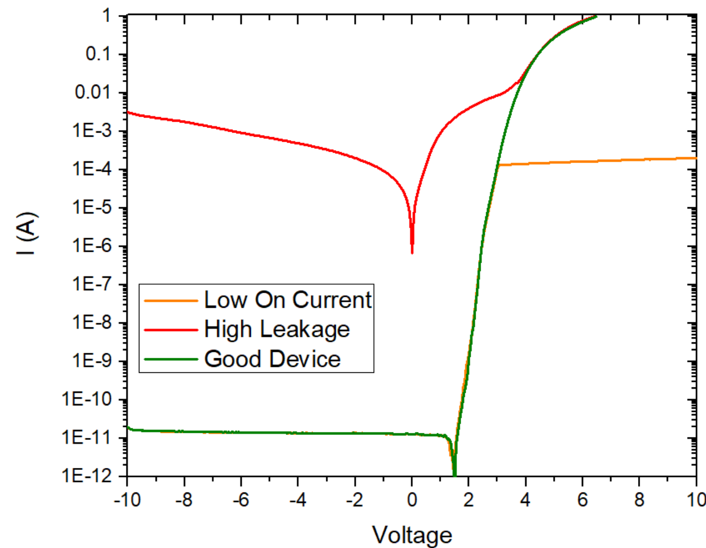

Fig. 4. Three example curves of typical vertical diodes are shown. A good devices (green), a device with high leakage (red), and a device with a low on state current (orange) are included.

4. COLLECTING ELECTRICAL DATA FOR OUTPUT PARAMETERS

Current-voltage (IV) curves were taken using a Keithley 4200A-SCS Parameter Analyzer with a pre amplifier. The first set of curves taken were from -10 V (reverse bias) to +10 V (forward bias). **Figure 4** shows example curves of this type of measurement on similar diodes. The ideal diodes will have a low leakage current at negative voltages, and a high, on-state current at forward bias voltages. Additional curves were taken to -200 V reverse bias to test the leakage and the robustness of the devices at higher voltages.

The first outcome of this research project was using traditional (non-machine learning) programming algorithms to detect the probability of the device failure. First step was correlating the Raman spectroscopy data to the diodes quality. The high crystal stress points have a major impact on the reverse

leakage current. **Figure 5a** shows the distribution of reverse leakage currents on all devices taken. From this we can surmise that >90% of all device have leakage currents below $2{\cdot}10^{-7}$ A/cm^2. By separating the samples by distance from stress points (**Figure 5b**) it can be seen that the diodes on the stress point are much more likely to have higher leakage current. **Table I** shows the leakage current at 3 different distances from the crystal stress. The percentage of devices with high leakage > $2{\cdot}10^{-7}$ A/cm^2 drops from 20% to 5% by avoiding the stress points. Additionally, avoiding the stress points cuts the probability of the device failing by half. This indicates that using Raman to look for defects is effective and will be used in future projects.

Figure 5. Raman maps of type I (uniform), type II-a (patterned), and type II-b (irregular) wafers [1].

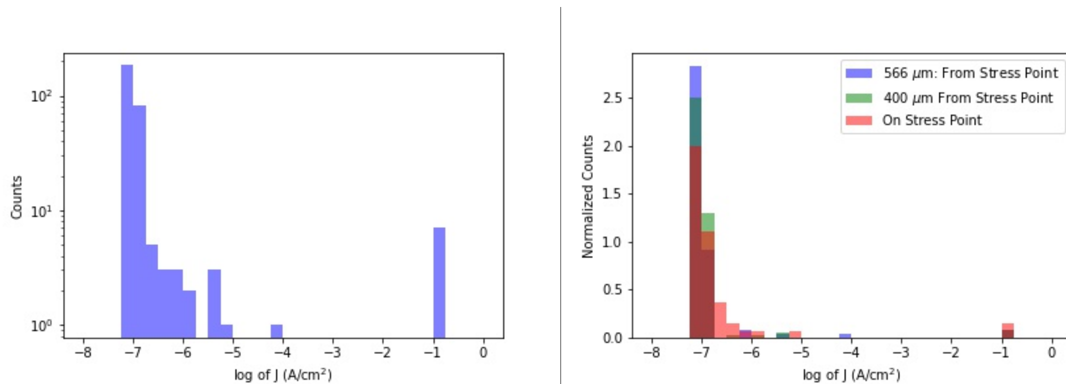

Fig. 5. (Left) Histogram Distribution of leakage current data at -200 V reverse bias. (Right) The same plot except divided into three regions based on the distance from the crystal stress points detected in Raman.

Distance From Stress Point	Number of Devices	High Leakage Fail ($>2{\cdot}10^{-7}$ A/cm^2)	Median J (A/cm^2) at -200 V
0	54	20%	1.01E-7
400 µm	144	5%	9.1E-8
566 µm	96	6%	9.2E-8
All Samples	296	9%	9.2E-8

Table I. Data showing the distribution of leakage current at -200 V reverse bias at different distance from the crystal stress points detected using Raman spectroscopy (see **Figure 1**)

The non-machine learning programming algorithms for optical profilometry mapping technique involves measuring a full 2-inch wafer then dividing the data into grids to estimate the device sizes. As described in previous research [5], [6], the long range optical techniques can be used to estimate the yield using a generalized ESD test to detect outliers combined with a measurement of the surface RMS. This method is accurate enough for wafer screening; however, it has yet to be demonstrated whether specific types of surface features can be used to predict device failure. In this project, higher resolution optical profilometry images were taken and are shown in **Figures 6a-b** with corresponding -200 V reverse leakage currents shown in **Figures 6c-d**. The three devices circles are the ones which catastrophically failed at 200 V. These devices had either a bump in the edge termination region of the devices, or a pit > 1.5 µm deep. However, several benign surface abnormalities are present as well as regions with poor device performance yet smooth optical profilometry images.

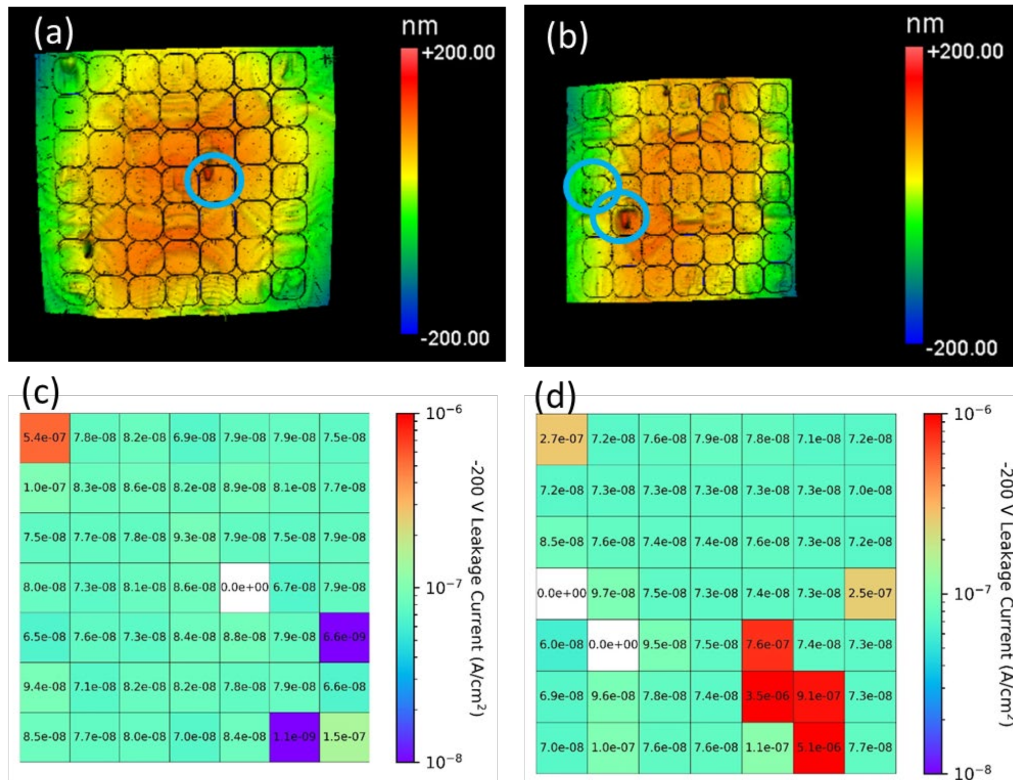

Fig. 6. (a-b) Optical profilometry images with corresponding -200 V reverse leakage currents (c-d). The circled devices catastrophically fail and are labeled as white in the leakage current maps.

5. MACHINE LEARNING ALGORITHM

Using the optical profilometry as the input data and the diodes IV curves as the output data, a machine learning algorithm was trained. On each device, the optical profilometry data was pipelined through a series of filters (see **Figure 7**) to create a large array of input variable to train the model. The model predicts the shape of the IV curve.

To test the accuracy of the prediction, the model was trained on 80% of the devices and tested on the other 20%. The table in **Figure 8** shows the an example of a prediction of the ideality factor, max forward current, 200 V reverse leakage current, on-resistance, and turn on voltage. The test predicted all these properties within 5% of the experimental result. The accuracy of all max forward current and on-resistance tested points can be found in the graphs in **Figure 8**. From there, it is found that 91% of the points tested are within 5% of the predicted values, suggesting the algorithm is effective at predicting forward bias conditions. This is expected since high surface roughness, dust particles, and carbon hillocks would likely increase the contact resistance or epitaxial layer resistivity, which can clearly be detected with this technique [2]. For reverse bias conditions, the results are inconclusive since very few devices exhibited high leakage current, thus there was not enough data to effectively train the model. It will likely require tens of thousands of diodes to do so. However, since clear defects are observed in the optical profilometry where the devices failed, it is possible that a well-trained model could detect these. However, several devices have no defect present and high leakage current (the red devices in **Figure 6d**) showing it is possible that defects invisible to optical profilometry have high leakage; however, these results could be a result of imperfect device processing, which would not be detectable by machine learning unless data was taken at each processing step.

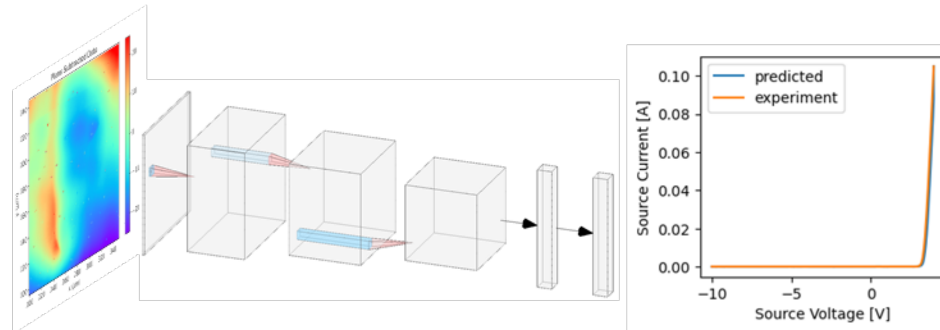

Fig. 7. Prediction pipeline in which an optical image of GaN surface input is fed to a convolutional neural network to predict vertical pin diode current-voltage response

Outputs	Data	Predicted	Error %
ideality_factor	2.0	2.1	-1.7
Max I_{fwd} (A/cm^2)	31.0	29.8	4.1
200 V I_{rev} (A/cm^2),	-8.3	-7.9	5.4
R_{on} (Ω-cm^2)	6.2	6.5	-5.2
V_{on}	3.1	3.3	-5.2

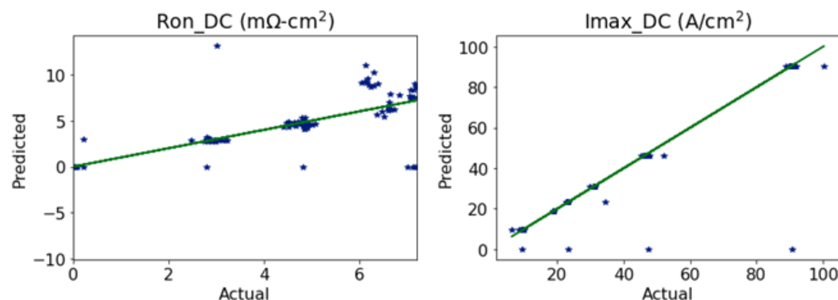

Fig. 8. The results of testing the machine learning model on devices not included in the training for the on-resistance (left) and the maximum forward current (right) are shown. Point closer to the line represent the predicted value and actual values matching. Additionally, this model was employed for pass/fail yield prediction with 91% accuracy on test (i.e., not training) data

6. CONCLUSIONS

This project demonstrated that Raman spectroscopy can be used to detect high crystal stress points, which strongly correlates with an increase leakage current. Optical profilometry images can be used to detect defects that cause catastrophic failures; however, the presence of benign defects makes it difficult to use for a simple quick detection method without an advanced algorithm. Thus, a machine learning algorithm was developed to study the effects of optical profilometry on device performance. The results showed that this algorithm was 91% accurate at predicting the forward bias behavior of devices, and it is possible that the devices it could accurately predict were failures due to device processing errors.

The main purpose of this NISE program was to develop techniques to help screen substrates and improve the yield of devices manufacturing in future GaN 6.2 programs including FY 22 programs “High-Voltage Planar Low Damage GaN Power Switch” and “20 kV Gallium Nitride Electromagnetic Pulse Arrestor for

Grid Reliability." The computational techniques from this project will be used in these programs and future programs.

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