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POWER GAN SCHOTTKY DIODES UNDER CURRENT DENSITY STRESSING

by

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13. ABSTRACT (maximum 200 words)

Silicon is commonly used in modern electronics; however, the technical specs are being maxed. Wide bandgap semiconductors such as gallium nitride (GaN) are being explored to further the development of better power electronics. This thesis continues testing conducted by Naval Postgraduate School student Burnell Clemmer, who designed a testing box capable of stressing wide bandgap semiconductors and found that they were failing quickly under stress.

The objective of this thesis was to identify the range of operation for GaN Schottky diodes and their failure mechanisms under high current density stressing to allow for better designs for high voltage power diodes. In order to accomplish this, we conducted a series of high temperature operating life stress experiments by running an electrical current through representative bulk GaN power diodes for extended periods of time. We then documented their degradation by taking current-voltage-temperature characteristic plots throughout the test. The results generally showed that both time and current density increased the rate of degradation of the devices, but concrete conclusions could not be drawn due to limited amount of data and inconsistencies.

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POWER GAN SCHOTTKY DIODES UNDER CURRENT DENSITY STRESSING

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ABSTRACT

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LIST OF ACRONYMS AND ABBREVIATIONS

BH	barrier height
C-V	capacitance-voltage
DC	direct current
DD	double diode
DUT	device under test
EECP	Equilibrium of Electrochemical Potential
FL	Fermi level
GaN	gallium-nitride
GPIB	Generic Purpose Interface Bus
HTOL	high-temperature operating life
IPES	Integrated Power and Energy System
I-V	current-voltage
I-V-T	current-voltage-temperature
MIDN	midshipmen
MIGS	Metal Induced Gap States
MS	metal-semiconductor
NAVSEA	Naval Sea Systems Command
PC	personal computer
Pd	palladium
NPS	Naval Postgraduate School
PN	p-type/n-type
R-G	recombination-generation
SBH	Schottky barrier height
SD	single diode
Si	silicon
SiC	silicon-carbide
UPS	Uninterruptible Power Supply
USN	United States Navy
USNA	United States Naval Academy
WBG	wide bandgap

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When I set out to take on this research, I had very little knowledge of semiconductor physics. So first and foremost, I'd like to thank my advisor, Professor Weatherford, and his research associate, Matt Porter, for their patience with me as I struggled and worked my way through all the issues I came across. I need to thank Professor Weatherford's new research associate, John Vitalich, for his constant encouragement and wise words, "Just get it done." I'd also like to thank MIDN Pass-Robles from USNA for helping me with getting the data plotted. I may never have finished without your help.

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I. INTRODUCTION

A. MOTIVATION

The first bipolar transistor was invented in 1947 [1]. Since then, there have been numerous advances in the semiconductor field, but only recently have scientists taken a serious look at using new materials other than silicon, selenium, and germanium for semiconductor devices. With the blossoming of power electronics in all areas of industry, better electronic devices are required to meet the ever-increasing demands. All throughout the world, high-powered electric machinery is becoming more prevalent; however, current semiconductors are struggling to keep up with growing voltage and power requirements. To push technology further, it has become more important than ever to pursue different avenues of semiconductor research.

Improved high-power electronics are critical for novel industries such as electric cars and the modernization of power grids throughout the world. With more reliable and efficient semiconductor devices, maximum range and time to fully charge batteries could be drastically improved, making electric cars more practical as an alternative to current combustion engines. Modernizing power grids also relies heavily on the use of power electronics. As power companies look to use microgrids and power storage to meet needs of modern power consumptions, again, they will, too, rely on power electronics.

The U.S. Navy (USN) is interested in the frontier of power electronics. With the development of the DDG-1000 power system, USN has shown its commitment to shifting from legacy power systems to new high-power hybrid electric multi-mission power systems. With the advent of the 1 kVDC Integrated-Fight-Through-Power system, currently in use onboard DDG-1000, the Navy has put forth more emphasis on working with industry and academia to develop more capable shipboard power distribution systems as laid out in [2]. Naval Sea Systems Command (NAVSEA) is continuing to develop improved power systems in the form of Integrated Power and Energy System (IPES) which, “utilizes integrated energy storage and power along with advanced controls to

provide a distribution bus suitable for servicing highly dynamic mission loads and propulsion demands" [2].

The USN requires advanced power systems to meet the demands of fledgling new weapon systems. In [2], USN lists directed energy weapons, radiated energy systems, and kinetic energy weapons as some of the new technologies for which current power systems are insufficient. As the power demands of the Navy and the world continue to grow, the need for improved semiconductors will continue to grow with it.

B. RELATED WORK

In 2016, an NPS thesis student studied the reliability and degradation of vertical gallium-nitride (GaN) Schottky diodes on various metallization types and process cleans [3]. Gardner [3] documented the barrier height, Richardson's constant, series resistance, leakage current, and ideality factor of these various devices and attempted to prove the existence of Schottky's interface inhomogeneities. Ultimately, he was able to categorize the reliability of the various devices; however, he stated that the non-ideal fabrication methods and experimental testing issues limit the conclusively of his study. He also noted that more data points were required to find the mean-time-to-failure of the devices.

In 2019, another NPS student designed, built, and tested a standalone High Temperature Operating Life (HTOL) system that could be used for long-term stress testing of devices in a controlled environment while taking measurement data throughout [4]. Clemmer [4] then used said system to conduct current stress testing of commercial GaN Schottky devices and documented results. He found evidence of inhomogeneity at the Schottky interface, and his results matched the models proposed by Tung in [5]. However, quick degradation of devices under high current stress limited the scope of the results.

C. OBJECTIVE

This research will take over from [4], focusing on slowing down the degradation process of the devices by lowering stress current and increasing the time length of stressing. The aim is to get a better picture of the processes that cause degradation of the devices and better document the reliability of commercial GaN vertical Schottky diodes. To do this, the

same system as Clemmer [4] was used as well as the same devices. With Current-Voltage-Temperature (I-V-T) measurements, this study calculated the leakage current, barrier height, and Richardson's constant of the devices over the stressing period.

D. ORGANIZATION

This report provides background on the theory, followed by the results and conclusions. Chapter II goes into the background of Schottky diodes, their characteristics, interface models, and the theory on interface inhomogeneity. Chapter III contains a brief overview of the HTOL system designed by [4] and the experimental methodology used in this experiment. Chapter IV contains the results of the experiment and the data collected. Chapter V contains the conclusions and future work proposed after the findings.

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II. BACKGROUND

This chapter reviews the difference in types of semiconductors, the theory behind Schottky diodes, electrostatics of Schottky diodes, current-voltage characteristics, and non-ideal models.

A. CHARACTERISTICS OF WIDE BANDGAP SEMICONDUCTORS

For decades, silicon (Si) has been the main type of material used in semiconductor electronics because it is easy to work with and its properties are well known. However, new materials are being investigated now due to the material limitations of Si. Silicon carbide (SiC) and gallium nitride (GaN) are wide bandgap (WBG) materials that show promise for power electronics [6]. A WBG material is defined as a material with a bandgap of 2.2 eV or higher [7]. This WBG means lower carrier concentrations in the depletion region, which results in lower leakage currents during reverse bias of devices. This makes WBG devices and ideal candidate for power devices where leakage current would lead to higher power consumption [6].

There are several other characteristics of power devices that are relevant to look at in addition to bandgap (E_g). [6] lists the following:

- Critical field strength (E_c) affects the on-state resistance of the drift region. When the critical field strength is higher, the region is smaller resulting in a lower resistance.
- Carrier mobility (μ) is how easily carriers, either electrons or holes, can move through the material.
- Thermal conductivity is how easily the material conducts heat, which is important for preventing overheating in devices.

Table 1 shows the characteristics of Si, SiC, and GaN.

Table 1. Material Properties of Semiconductors. Adapted from [6].

Property	Si	SiC	GaN
Bandgap (eV)	1.12	3.26	3.4
Critical field (10^6 V/cm)	.3	3.5	3.3
Carrier mobility (cm^2/V x sec)	1500	650	990
Thermal conductivity (W/cm^2 x K)	1.5	5	1.3

From Table 1, GaN has a critical field strength eleven times greater than that of Si, but the thermal conductivity of it is slightly lower resulting in a greater chance of overheating.

B. SCHOTTKY DIODES

A metal-semiconductor (MS) contact can be either symmetrical or asymmetrical. In the asymmetrical case, there is a larger barrier to charge carrier transport in one direction, which causes an asymmetrical non-linear current versus voltage (I-V) curve [8]. This takes place when an n-type semiconductor, which has an excess number of electrons, is used and is known as a Schottky diode. In the symmetric case, there is not a barrier to charge carrier transport in either direction, which results in a symmetric linear I-V curve. [8] This uses a p-type semiconductor, which has an excess of holes, and is known as an ohmic contact. The barrier refers to the potential difference between the metal and the semiconductor, which restricts the carrier flow between the two.

The Schottky-Mott rule focuses on only the electrostatics of the diode and assumes an ideal interface between the metal and semiconductor [5]. An ideal MS contact assumes three properties. These are listed by Pierret in [9]:

1. The metal and semiconductor are assumed to be in intimate contact on the atomic scale, with no layers of any type (such as an oxide between the components.
2. There is no interdiffusion or intermixing of the metal and semiconductor.
3. There are no adsorbed impurities or surface charges at the MS contacts. [9]

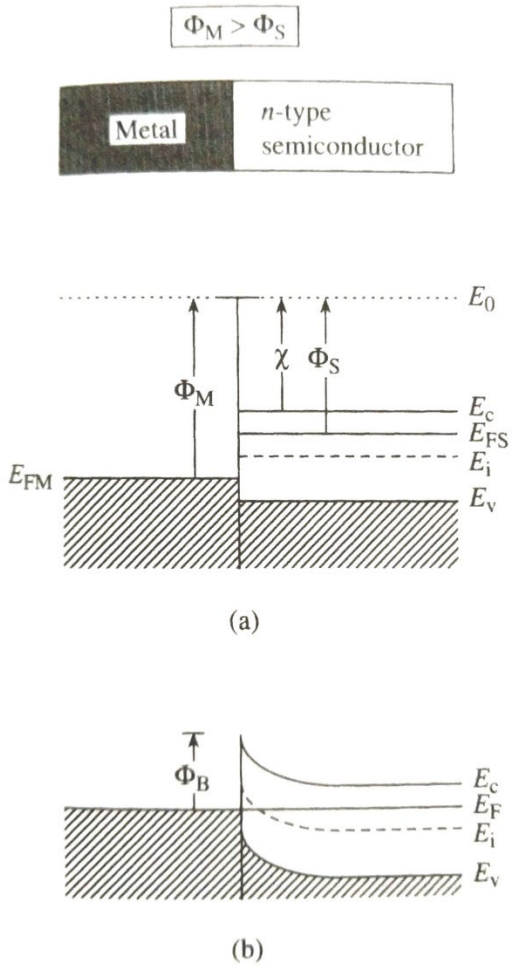
Pierret [9] explains that the energy band diagram for Schottky diodes relies on the energy difference between the vacuum energy level (E_0) and Fermi level (FL) energy (E_F),

known as the work function. He defines work function for the metal (Φ_M) as a defined material characteristic and the work function for a semiconductor (Φ_S) is based on the electron affinity (χ), $\chi = (E_0 - E_C)$, which is a defined material characteristic of the semiconductor and the energy difference between the conduction band (E_C) and the E_F. This difference is defined by the doping of the semiconductor [9]. Φ_S is defined by Equation 1.

$$\Phi_S = \chi + (E_C - E_F). \quad (1)$$

In the case where $\Phi_M > \Phi_S$, the result is a Schottky contact. When the two materials meet, the Fermi level (FL) must be equalized. This will result in electron transfer from the semiconductor to the metal and a depletion region will form in the semiconductor [9]. Figure 1 shows this process. Part a is before material contact is made and it is visible that $\Phi_M > \Phi_S$. Part b shows after contact is made. The FL has been leveled across the contact resulting in the depletion region and barrier near where the semiconductor makes contact. The barrier height is defined in Equation 2:

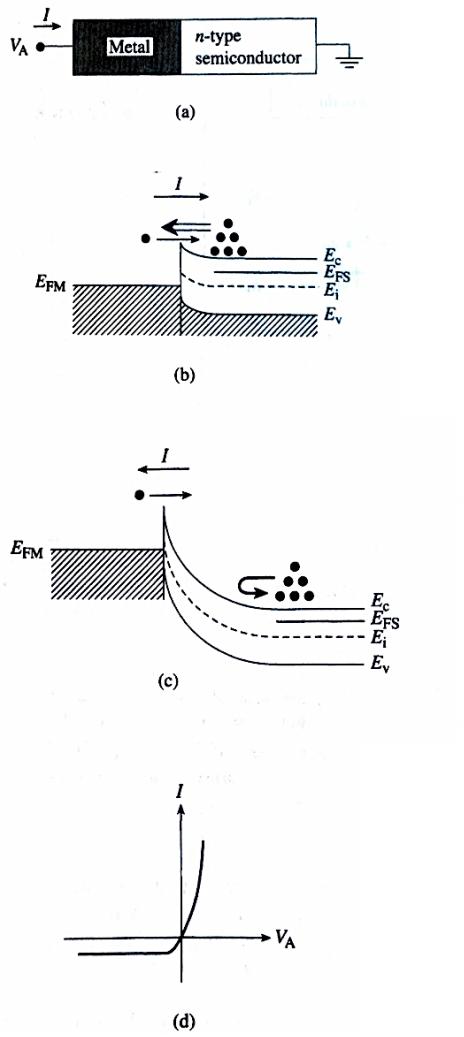
$$\Phi_B = \Phi_M - \chi. \quad (2)$$



(a) Immediately before materials make contact. (b) After materials make contact and equilibrium is achieved.

Figure 1. Energy Band Diagram for $\Phi_M > \Phi_S$. Source: [9].

When applying a voltage bias (V_A) to the diode, it is possible to increase or reduce the barrier height of the contact. For the example shown in Figure 2, a voltage is applied to the metal and the semiconductor is grounded, shown in part a. When V_A is positive, the metal fermi level (E_{FM}) is lowered below that of the semiconductor fermi level (E_{FS}). As is shown in part b, this reduces the barrier height and allows electrons to flow across the contact. When V_A is negative, E_{FS} is further lowered below E_{FM}, which increases the barrier height. This prevents electrons from traveling from the semiconductor to the metal. Some electrons are able to flow from the metal to the semiconductor causing a small reverse bias current [9].



(a) Defining the voltage bias. (b) Forward bias. (c) Reverse bias. (d) I-V characteristics

Figure 2. Effect of Voltage Bias on a MS Contact Where $\Phi_M > \Phi_S$. Source: [9].

1. Electrostatics

Schottky diodes have voltage drop across them similar to p-type/n-type (PN) junctions. This voltage, known as the built-in voltage, is defined by [9] in Equation 3:

$$V_{bi} = \frac{1}{q}[\Phi_B - (E_C - E_F)]. \tag{3}$$

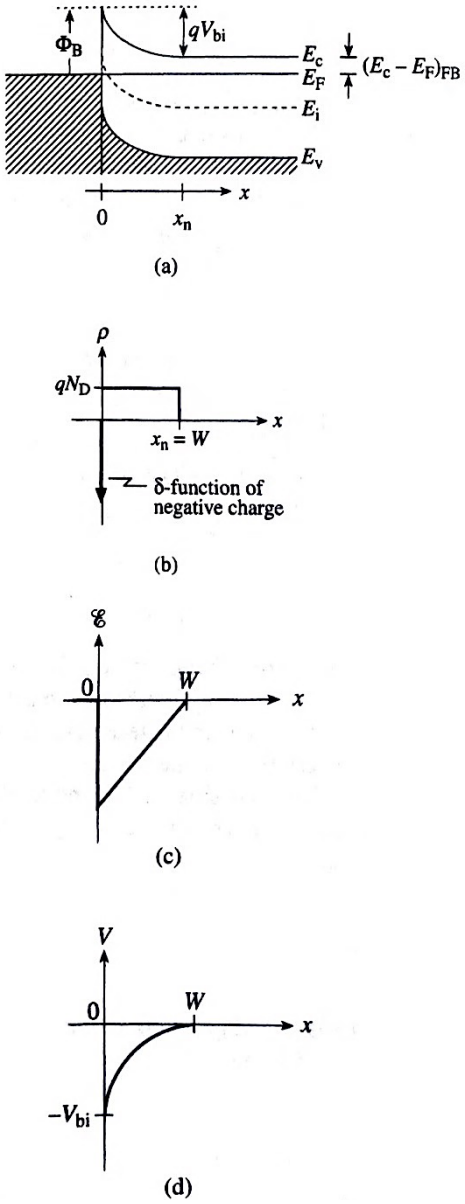
This voltage is graphed in Figure 2, part a.

As mentioned previously, the MS contact creates a depletion region in the semiconductor. This region is positively charged due to the n-type doping in the semiconductor. But since there is no p-type semiconductor to balance out the charge, electrons accumulate on the edge of the metal [9]. The charge density(ρ) in the depletion region, shown in Figure 2b, can be described by Equation 4 [9], where x_n is the width of the depletion region:

$$\rho = \begin{cases} qN_D & \dots \quad 0 \le x_n \le W \\ 0 & \dots \quad x_n > W \end{cases} . \tag{4}$$

Since the excess charge is only at the contact in the metal, it follows that in the metal, $\mathcal{E} = 0$ and V is constant. The semiconductor electric field can be found using Poisson's Equation [9], Equation 5:

$$\frac{d\xi}{dx} = \frac{\rho}{K_S \varepsilon_0} \cong \frac{qN_D}{K_S \varepsilon_0} \quad \dots \quad 0 \le x_n \le W . \tag{5}$$



(a) Built-in voltage. (b) Charge density (c) Electric field (d) Electrostatic potential

Figure 3. Defining Electrostatics of Schottky Diodes. Source: [9].

Integrating Equation 5 results in the Equation 6 [9]:

$$\xi(x) = -\frac{qN_D}{K_S \varepsilon_0}(W - x) \ldots \qquad 0 \le x \le W\,, \tag{6}$$

which is plotted in Figure 3c.

For finding the voltage potential equation, [9] points out that dV/dx = - $\mathcal{E}$. Solving this for V results in Equation 7:

$$V(x) = -\frac{qN_D}{2K_S\varepsilon_0}(W-x)^2 \qquad \ldots \qquad 0 \le x \le W\,, \tag{7}$$

which is graphed in Figure 3 d.

Finally, evaluating Equation 7 when x = 0, results in V(0) = - ($V_{bi} - V_A$) where V_A is the voltage bias applied to the metal shown in Figure 2. Solving the V(0) for the depletion width results in Equation 8 [4]:

$$W = \left[\frac{2K_S\varepsilon_0}{qN_D}(V_{bi}-V_A)\right]^{1/2} \tag{8}$$

2. I-V Characteristics

When explaining the current flow in a diode, [9] contrasts the MS diode with a PN, stating that in a PN diode, the dominant current usually arises from recombination and generation (R-G) in the depletion region. Pierret goes on to say, though R-G does occur in the MS diode, due to the low barrier height at the metal seen by electrons, electron injection dominates current flow. This is referred to as thermionic emission. According to thermionic emission, electrons in the depletion region will pass over the barrier if their velocity in the direction of the interface results in a kinetic energy greater than the energy of the barrier minus the forward bias voltage [9]. From this statement, Pierret [9] derives the current equation, shown in Equation 9 and 10, which is nearly identical to the PN diode equation:

$$I = I_S(e^{qV_A/kT} - 1)\,, \tag{9}$$

where the saturation current (I_S):

$$I_S = AA^*T^2e^{-\Phi_B/kT}\,. \tag{10}$$

In Pierret's [9] saturation current equation, Equation 10, A is the area of the diode and A* is the effective Richardson's constant. An ideality factor, η, is often inserted into Equation 9 to correct for the non-ideal nature of the Schottky contact [10].

The other current transport processes pointed out by [10] are electron tunneling through the barrier, recombination in the depletion region, electron diffusion in the depletion region, and holes injected by the metal into the semiconductor.

In Gardner's thesis [3], he observed different current processes for the on-state of the diode. Figure 4 shows a typical I-V relationship for GaN Schottky diode that he created. Gardner identifies three regions: Region I where, due to combination of tunneling and recombination, higher than expected current occurs caused by imperfection in the Schottky contact. Region II, he explains, is dominated by thermionic emission, and in region III, due to series resistances, current begins to drop lower than expected.

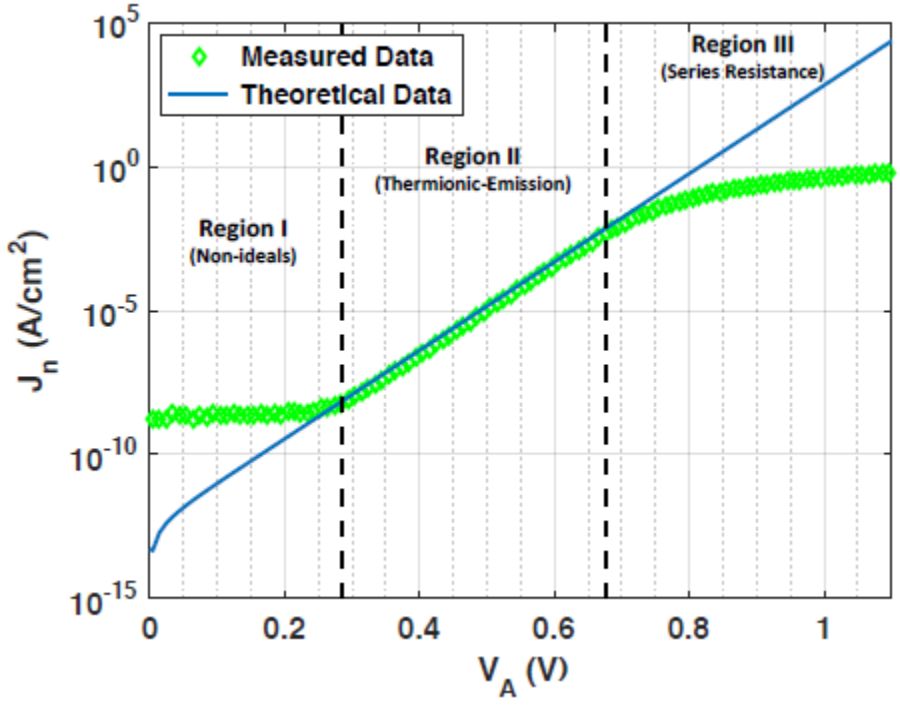


Figure 4. Theoretical and Experimental Semi-Logarithmic I-V Plot for an n-type GaN Schottky Diode. Source: [3].

Applying Equation 9 to the semilogarithmic plot in region II, Gardner created a linear fit for the thermionic emission current in that region, shown in Equation 11

$$\ln(I) = \ln(I_S) + \frac{q}{\eta kT} V_A, \tag{11}$$

where $\ln(I_S)$ is the y-intercept of the fit and η can be found from the slope. From there, [1] demonstrates that, using Equation 10, Φ_B can be solved by Equation 12:

$$\Phi_B = \frac{kT}{q} \ln\left(\frac{A^* T^2}{I_S}\right). \tag{12}$$

a. Barrier Height from I-V-T

Solving in the above method assumes the value of A^*. [1] then goes into another way of solving for barrier height while also solving the effective Richardson's constant, by leveraging the temperature dependance of Equations 9 and 10. By taking the I-V characteristics of a device at various temperatures and solving for the saturation current at each temperature, what is known as a Richardson plot can be produced, which shows the natural logarithm of the saturation current over the temperature squared (I_S/T^2) vs q/kT. Using the line of fit from Equation 13, the variables can be solved.

$$\ln\left(\frac{I_S}{T^2}\right) = \ln\left(A^*\right) - \frac{q\Phi_B}{kT}. \tag{13}$$

A^* is found from the y intercept of the line of fit and Φ_B is solved from the slope. Figure 5 shows an example of a Richardson's plot using 5 initial current measurements for a device taken at 5 temperatures.

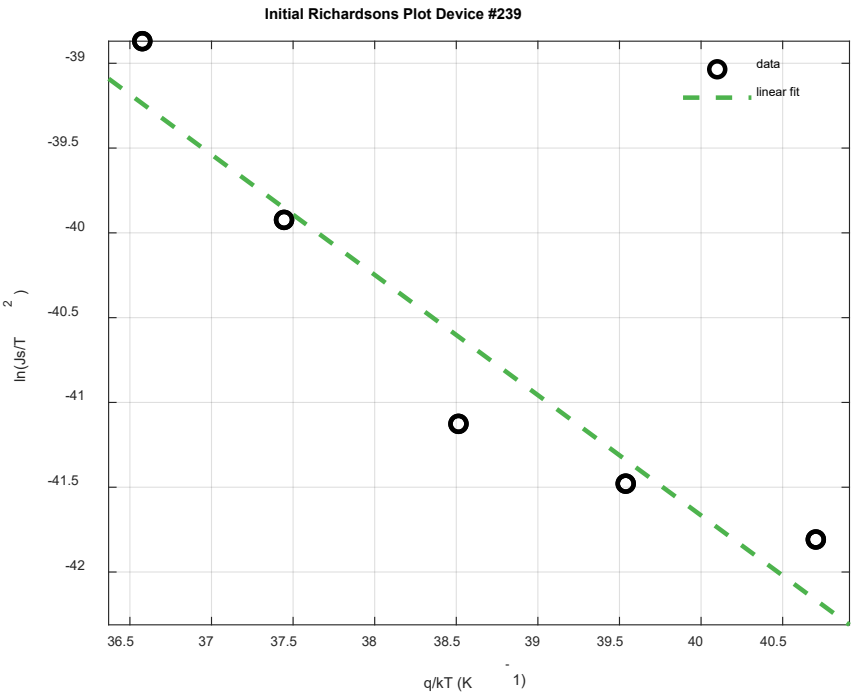


Figure 5. Initial Richardson's Plot for Device 239.

b. Barrier Height from C-V

Barrier height can also be calculated using capacitance-voltage (C-V) measurements. [1] demonstrates that when $1/C^2$ is plotted versus applied voltage, the barrier height can be calculated using equation 14:

$$\Phi_B = V_i + V_n + \frac{kT}{q} - \Delta\Phi, \tag{14}$$

where V_i is the x-intercept on the graph and V_n is the depth of the Fermi level below the conduction band. Figure 6 shows an example C-V plot that could be used to calculate barrier height.

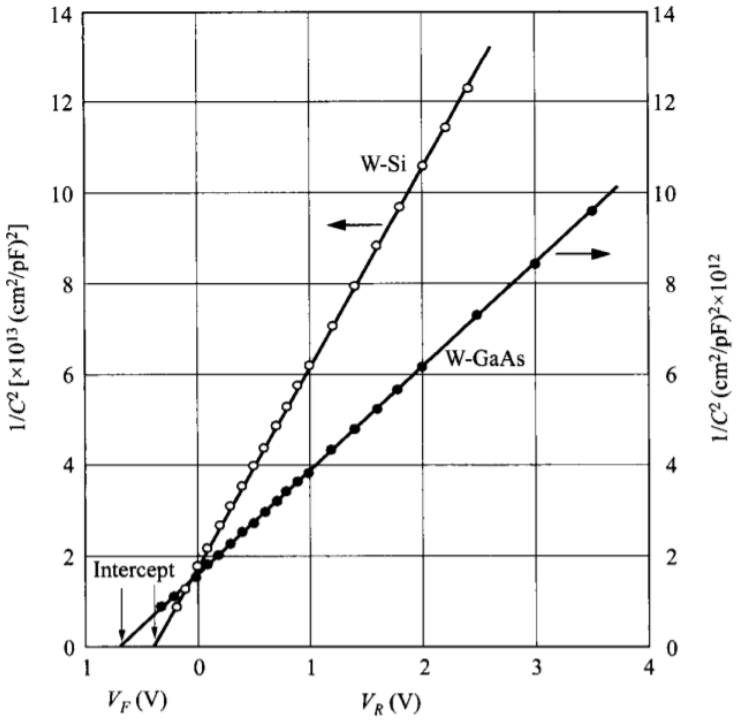


Figure 6. $1/C^2$ versus V for Two Diodes. Source: [1].

C. NON-IDEAL SCHOTTKY THEORY

The Schottky-Mott model previously discussed assume an ideal MS interface and only looks at the electrostatics. The model fails because the actual charge distribution is different from the linear superposition that is used due to the close interface of the two materials creating chemical bonds between them [5].

1. Early Models

Early simple models focused on an idea called "Fermi level pinning," where the FL was said to be pinned to a certain energy level based on Φ_M and the Schottky barrier height (SBH) [5]. Tung [5] explains that this was found by applying a linear fit to a graph of SBH versus Φ_M of MS interfaces with varying metals. The Bardeen model used a small dielectric layer between the metal and semiconductor to eliminate the MS surface states, but Tung points out that there would still be surface states between the metal and dielectric and the dielectric and semiconductor. Another model, assumed the formation of metal-

induced gap states (MIGS) inside the bandgap of the semiconductor, allowing electrons to flow from the metal to the semiconductor, known as the MIGS model [5]. Tung identifies that the issue with this model is that electron transfer occurs at all energy levels of the metal and semiconductor, not just inside the bandgap, and that this model has taken on the issues of the previous model by substituting surface states for MIGS.

2. Inhomogeneous Interface

The Equilibrium of Electrochemical Potential (EECP) model is a more modern model that proposes SBH is dependent on the chemical bonds between the metal and semiconductor [5]. In this model, Tung states that Fermi level pinning is based on polarized chemical bonds at the interface, vice surface states or MIGS. This theory also explains variations in SBH due to inhomogeneity in chemical bonds at the MS interface. Using this model, Tung [5] calculates SBH using Equation 15 and 16:

$$\Phi_B = \gamma_B(I_S - \Phi_M) + (1-\gamma_B)\frac{E_g}{2}, \tag{15}$$

where

$$\gamma_B = 1 - \frac{e^2 N_B d_{MS}}{\varepsilon_{it}(E_g/2+\kappa)} \tag{16}$$

In Equation 15, d_{MS} is the bond length at the MS interface, N_B is the density of bonds at the interface, ε_{it} is the effective dielectric constant at the MS interface, E_g is the bandgap energy, and κ is the sum of all hoping interactions [5] [3].

SBH inhomogeneity results in regions small areas of low SBH compared to the rest of the interface [11]. For analysis, Tung assumes these areas to be small circles and narrow semi-infinite strips, whose geometries are shown in Figure 7. He provides Equation 17 for the voltage potential for a small low SBH circle where V_{bb} is the band bending for a MS interface with homogenous SBH, z is the position in the direction perpendicular to the interface, W is the depletion width, V_n is the difference between the FL and the conduction-

band minimum, V_a is the applied voltage, Δ is the change in SBH, and R_0 is the radius of the circular region:

$$V(0,z) = V_{bb}\left(1-\frac{z}{W}\right)^2 + V_n + V_a - \Delta\left(1-\frac{z}{(z^2+R_0^2)^{1/2}}\right). \quad (17)$$

He [11] provides Equation 18 for the voltage potential of a strip where L_0 is the width:

$$V(x,y,z) = V_{bb}\left(1-\frac{z}{W}\right)^2 + V_n + V_a - \frac{\Delta}{\pi}\tan^{-1}\left(\frac{|x|+L_0/2}{z}\right) + \frac{\Delta}{\pi}\tan^{-1}\left(\frac{|x|-L_0/2}{z}\right). \quad (18)$$

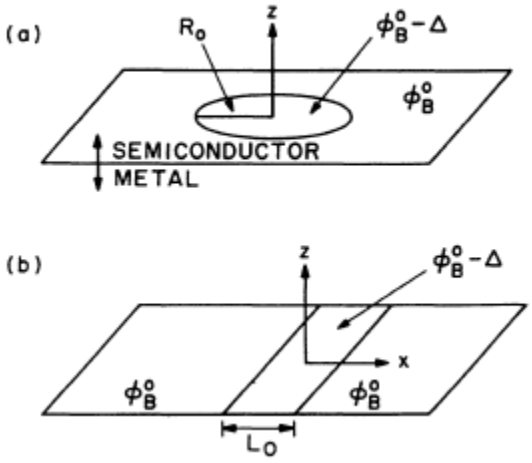


Figure 7. Geometries of Low SBH Area (a) Circular (b) Strip. Source: [11].

In these regions, the carrier transport across them is not constrained by the interface SBH as it would for a homogenous MS interfaces, but is instead the transport carriers across the low SBH area [5]. Tung states that "saddle point" potential is most responsible for controlling carrier transport in the regions. Figure 8 illustrates the voltage potential difference at a low SBH area with low and high doping. As can be seen, with lower doping, the SBH is more uniform and thus results in a smaller saddle potential.

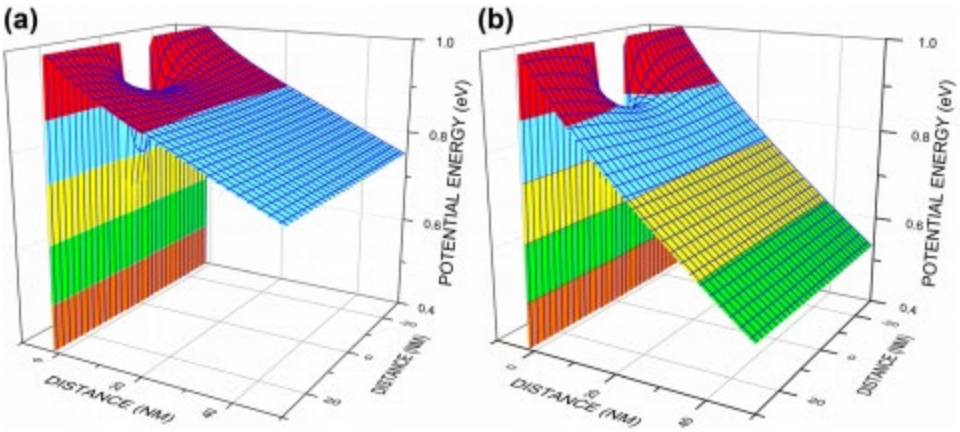


Figure 8. Saddle Point Potential for (a) Low Doped Semiconductor (b) High Doped Semiconductor. Source: [5].

Figure 9 shows the potential well for a narrow strip of low SBH, showing that this differential voltage potential exists deep into the depletion region and is not just a surface phenomenon.

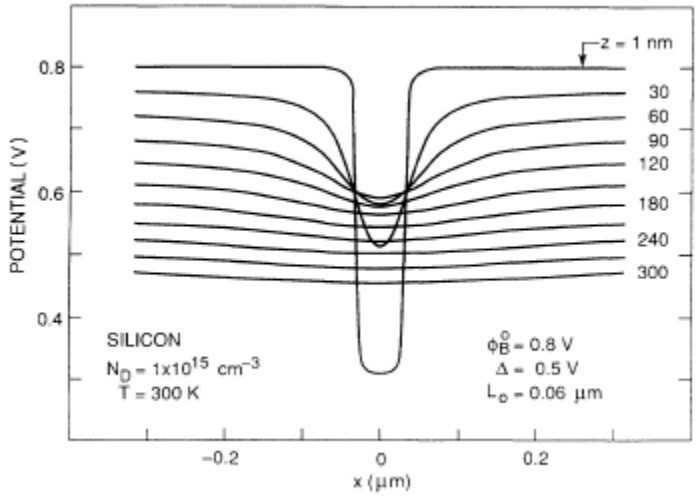


Figure 9. Voltage Potential for Narrow Strip of Low SBH. Source: [11].

Another interesting aspect of these low SBH regions is a voltage bias changes the so does the saddle point potential. Equations 17 and 18 show this by incorporating voltage

bias. Applying a forward bias to the interface increases the saddle point potential, while reverse bias reduces it [5]. This characteristic is illustrated in Figure 10.

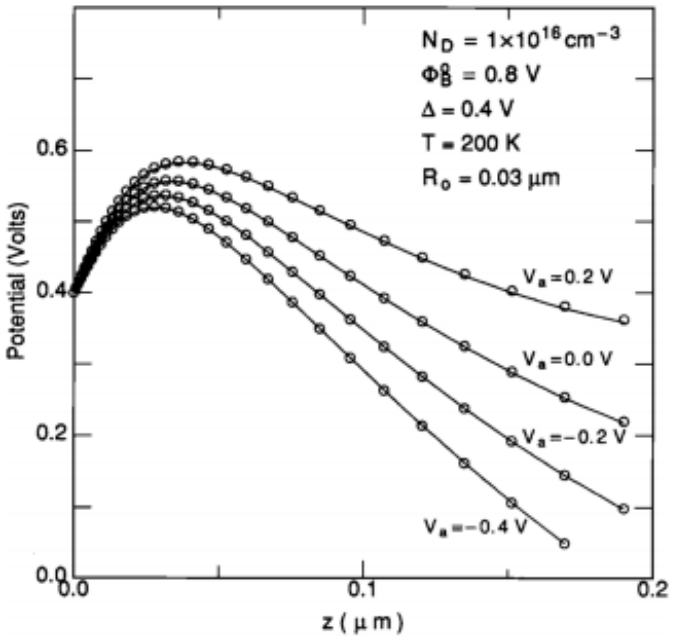


Figure 10. Saddle Potential for a Low SBH Circular Region at Different Voltage Biases. Source: [5].

3. Current Calculations for Inhomogeneous Interface

When calculating current for a diode with inhomogeneous SBH, the current at zones of low barrier height must be incorporated into the equation. Tung [11] derives the current equation into two parts: one which is the current across the diode with uniform SBH and the other, the current flowing through the regions of low barrier height. He also states that small regions of higher SBH are likely present; however, they can be ignored in this analysis because little current will flow through and will have little impact on overall electron movement. In a sharp distribution of low SBH patches, Tung's total current equation is shown in equation 19, where $\beta = 1/k*T$, c1 is the concentration of the patches, and γ_0 is a region-specific parameter defined in Table 2.

$$I_{tot} = AA^*T^2 e^{-\beta\Phi_B^0}\left[e^{\beta V_A} - 1\right]\times\left[1 + \frac{4c_1\pi\eta^{2/3}\gamma_0}{9\beta V_{bb}^{2/3}} e^{\frac{\beta\gamma_0 V_{bb}^{1/3}}{\eta^{1/3}}}\right]. \quad (19)$$

For broad distribution of low SBH patches, the regions vary in both shape and density. Tung uses statistical distribution of patches and strips to calculate current for this case, which is more likely for nonideal MS interface [11]. Equation 20 shows the total current for a broad distribution of SBH variation where ξ, κ, and f(β,V_{bb}) are defined in Table 2.

$$I_{tot} = A^* AT^2 e^{-\beta\Phi_B^0}\left(e^{\beta V_A} - 1\right)\times\left[1 + f(V_{bb})e^{\beta^2\kappa V_{bb}^{\xi}}\right]. \quad (20)$$

In Table 2, σ is the standard deviation of the patch density. Tung assumes the standard deviation to have one-half of a gaussian distribution [11]. He also assumes that the patches are well separated and therefore do not have interactions with one another.

The current through the low SBH regions is calculated as it were one large patch with lower barrier height [11]. Tung states that the effective SBH for this region can be calculated using Equation 21,

$$\Phi_{eff} = \Phi_B^0 - \beta\kappa V_{bb}^{\xi}. \quad (21)$$

Equation 20 shows that SBH in this region is temperature dependent and therefore, the current coming from this region is also temperature dependent [11]. Tung also states that the ideality factors of the currents must also be temperature dependent, resulting in Equation 22,

$$\eta_{tot} \approx 1 + \xi\beta\kappa V_{bb}^{\xi-1}. \quad (22)$$

Tung [11] states that experimentally, I-V curves often exhibit current composed of 2 or more components. He goes on that at low biases, the forward current is determined by leakage current and then as bias increases, the I-V relationship become semilogarithmic as thermionic emission takes over. Tung further states that experimental data also suggests that the leakage current is caused to do to interface inhomogeneity vice surface states where

current flows through low SBH regions. This leakage current is limited to low biases due high series resistance in the regions due to the small area that current must flow through.

Table 2. Parameters for Electron Transport. Adapted from [11].

Parameter	Patch	Strip
γ_0	$3\left(\frac{\Delta R_0^2}{4}\right)^{1/3}$	$2\left(\frac{\sqrt{2}L_0\Delta}{\pi}\right)^{1/2}$
ξ	2/3	1/2
κ	$\frac{\sigma_1^2}{2\eta^{2/3}}$	$\frac{\sigma_2^2}{2\eta^{1/2}}$
$f(\beta,V_{bb})$	$\frac{8c_1\sigma_1\pi\eta^{1/3}}{9V_{bb}^{1/3}}$	$\frac{c_2\pi\sigma_2^{3/2}\sqrt{\beta}\eta^{1/8}L_{strip}}{1.46V_{bb}^{1/8}}$

III. DIODE STRESS TEST SYSTEM DESIGN AND METHODOLOGY

This chapter will explain the High Temperature Operating Life (HTOL) system that was used to test the devices.

A. HTOL SYSTEM OVERVIEW

The system was built and designed by Clemmer [4], a thesis student who began the stress testing research of the palladium (Pd) GaN continued in this thesis. His system, based on commercial HTOL systems, aims to allow for current stressing multiple devices, for multiple days, while controlling temperature and humidity in the Devices Under Test (DUT) chamber. In addition, the system allows for I-V measurements to be taken periodically throughout the testing at various temperatures. To do this, he integrated a control computer, a testing module, power supplies, and Source/Monitor.

The equipment used in the system are a "personal computer (PC), Netgear 24-port gigabit switch, HP4142B direct current (DC) Source/Monitor, Siglent programmable DC power supplies, and back-uninterruptable power supply (back-UPS)" [4]. The computer control operation of the devices and communicates to them through the switch using ethernet, except for the Source/Monitor, which had to be connected General Purpose Interface Bus (GPIB) due to not having an ethernet port. Power supplies maintained the stress current by varying voltage during testing, and the HP4142B took I-V measurement. Back-UPS were used to ensure that the system never lost power and testing was not interrupted. Figure 11 shows the overview of the testing setup.

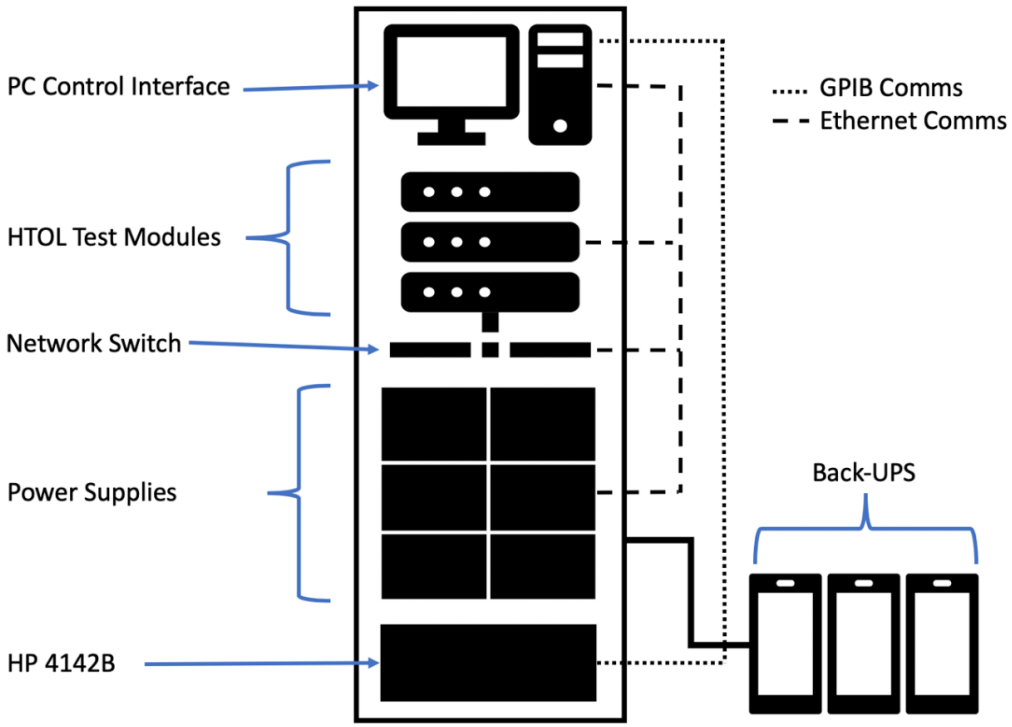


Figure 11. HTOL System Overview. Source: [4].

The testing module was designed to control the environment that for the DUT and connect them to power source for stressing and the Source/Monitor for testing. The DUT can handle testing of 4 devices at once and is atmospherically sealed to control the environment. Temperature is maintained using thermoelectric coolers that can control temperature from 10 - 60°C and temperature reading are recorded throughout testing. The chamber also monitors humidity and can purge the environment with nitrogen if humidity gets too high. This is important when conducting tests on unpackaged devices.

The testing module also contains a switching matrix that sequentially disconnects each device from the power sources and connects it to the Source/Monitor at specified intervals during the stressing to take the I-V measurements. This allows measurements and stress to occur autonomously and eliminates the potential for human error in the measurements.

The temperature and humidity as well as the switching is controlled by two microcontrollers in the testing module. In addition, they are responsible for passing all of temperature and humidity data, as well as the current state of the system to the control computer so that it can be logged and the computer can correctly control the power supplies and Source/Monitor.

The overall system is controlled by the personal computer using a LabVIEW program. The temperature and humidity, device measurements, and system status are displayed on the computer monitor via LabVIEW. LabVIEW also contains a GUI that guides the user through system and test setup. In the test setup, the user can choose stress current, stress temperature, and specific temperatures that the measurements are taken at, as well as the voltage range and number of points taken in the I-V curves. The I-V curves that are collect are exported to excel files that are labeled with the time that the reading was taken, the temperature it was taken at, and the device that the curve corresponds to.

B. METHODOLOGY

The goal of the testing is to document the degradation of the devices over days of stress testing. Initially, the first tests were simply to get the HTOL system back in working order and familiarization of the equipment. No more than two devices were tested simultaneously due to finding that the system struggled to maintain temperature when more devices were tested at once.

Next, preliminary tests were run on devices for 72 hours from currents 1 - 2A. I-V-T measurements were taken every 2 hours at 5 temperatures between 10 and 50°C. The system had difficulty running continuously for 72 hours straight due to connectivity issues between the control computer and the computer and test modules. A workaround was devised where the system was restarted each day and time would be added from the previous days to the time counter. This allowed for longer testing.

Once the system was able to test for longer periods, two-week tests were conducted on 6 devices at currents 1.5A, 1.75A, and 2A. I-V-T measurements were taken every 3 hours at 5 temperatures between 10 and 50°C.

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IV. STRESS TESTING RESULTS

A. INITIAL TESTING FOR APPROXIMATELY 72 HOURS

Initial testing was completed for 8 devices at 1A, 1.4A, 1.6A and 1.8A. Leakage current was measured at -50V at 20°C. Barrier height was calculated using Richardson's plots by leveraging the temperature dependance of the saturation current. The saturation current was taken from the point on the I-V curve, when plotted on a semilogarithmic plot, where the curve was linear. This area is shown in the I-V curve for device 27 in Figure 12. Data for all devices tested in initial testing is displayed at the end of this section in Table 3. Inhomogeneity spread was calculated using Python scripts written by Research Assistant Matthew Porter, using Tung's current equation, shown in Equation 20. For some of the devices, the Python scripts would not accept the data for plotting inhomogeneity spread, so for those devices the spread is unknown.

1. Initial Testing 1A

The I-V curve for device 27, shown in Figure 12, shows the diode has a linear relationship initially. This characteristic is masked as voltage increased due to increasing forward series resistance. Diodes with this characteristic were classified as single diode (SD).

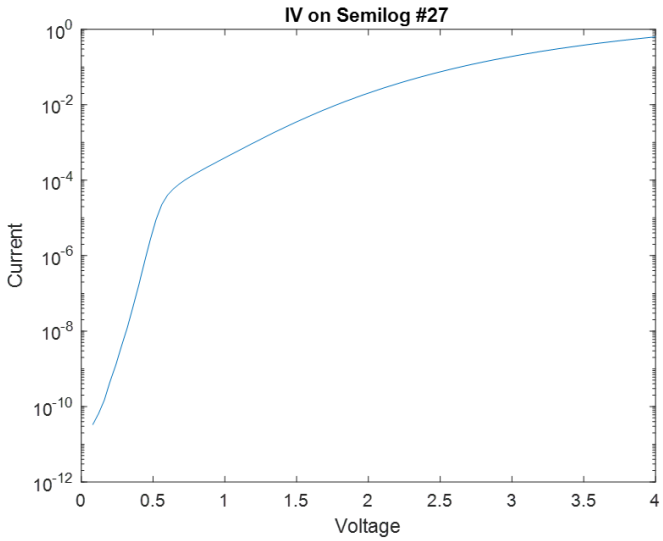

Figure 12. Semilogarithmic I-V Curve Device 27

The leakage current, shown in Figure 13, for device 27 showed little change over the stressing period. The average leakage current for the device was -0.0242 μA.

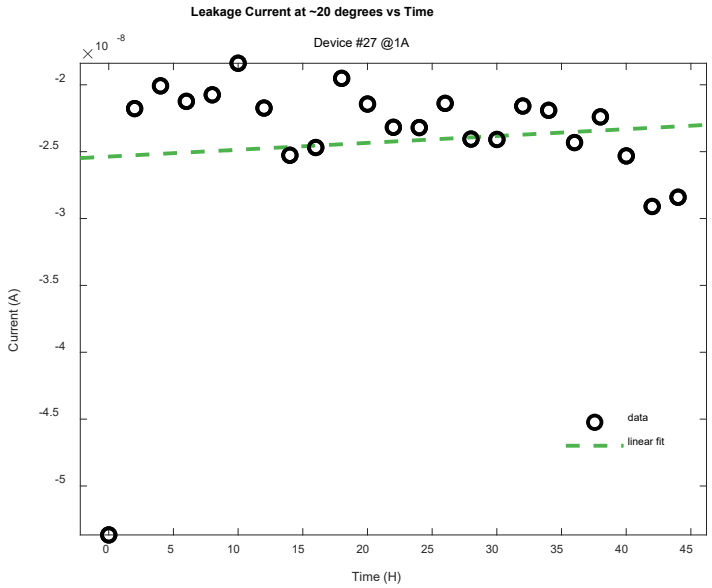

Figure 13. Leakage Current versus Time Device 27 Stressed at 1A.

Barrier height for device 27, shown in Figure 14, also showed little change over the stressing period. Average barrier height was measured at 1.117 V. The inhomogeneity spread for Device 27 showed little change over time, displayed in Figure 15.

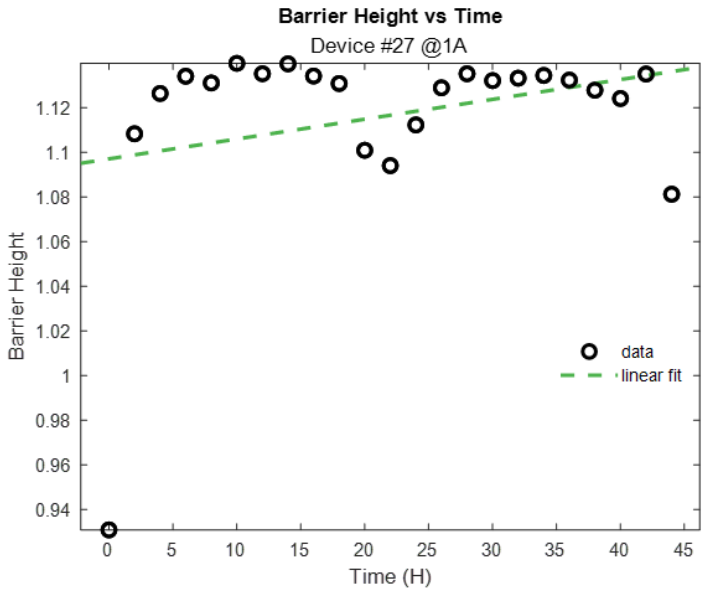

Figure 14. Barrier Height versus Time Device 27 Stressed at 1A

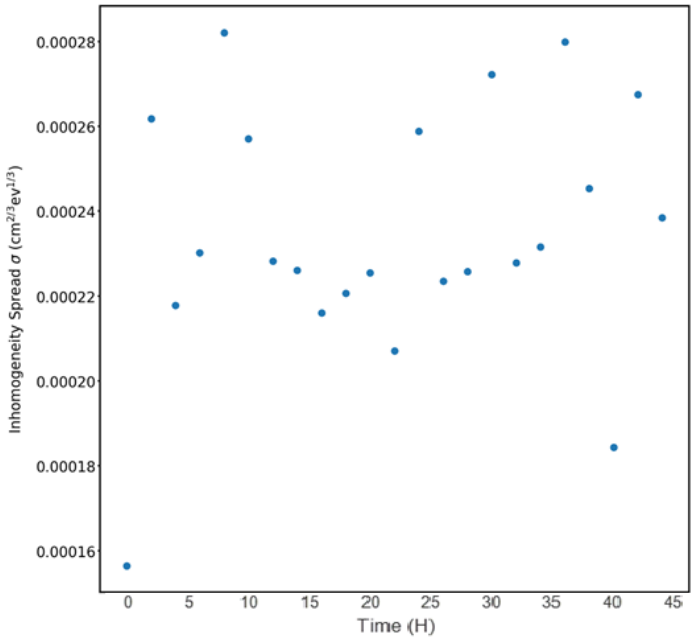

Figure 15. Inhomogeneity Spread versus Time Device 27 Stressed at 1A

The I-V curve for device 42, shown in Figure 16, does not show the initial linear characteristic that was displayed by device 27 in Figure 12. The device appears to show

two diode characteristics as seen by the two bends in the early part of the curve shown in Figure 15. Devices with this nonlinear characteristic were described as double diode (DD).

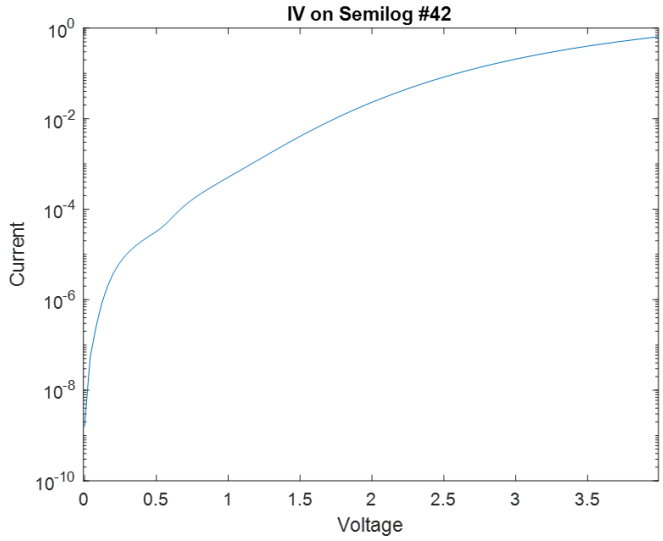

Figure 16. Semilogarithmic I-V Curve Device 42

Leakage current for device 42, plotted in Figure 17, showed a 26% decrease in leakage current stressing time. The average leakage current for the device was -9.963 µA.

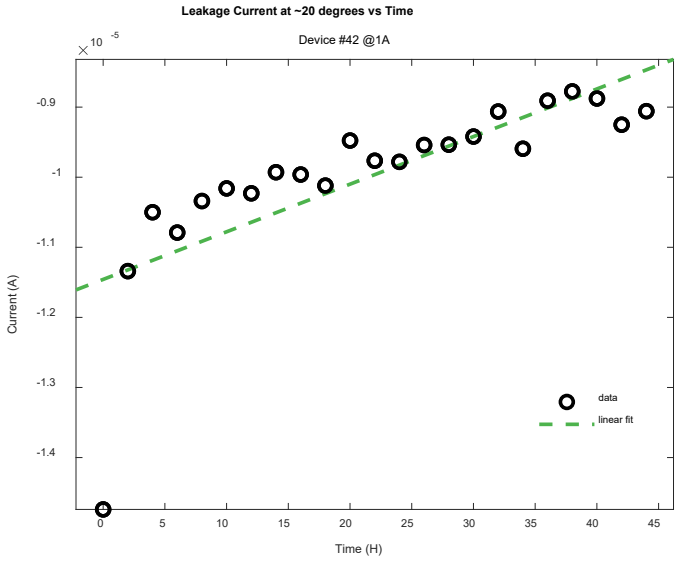

Figure 17. Leakage Current versus Time Device 42 Stressed at 1A.

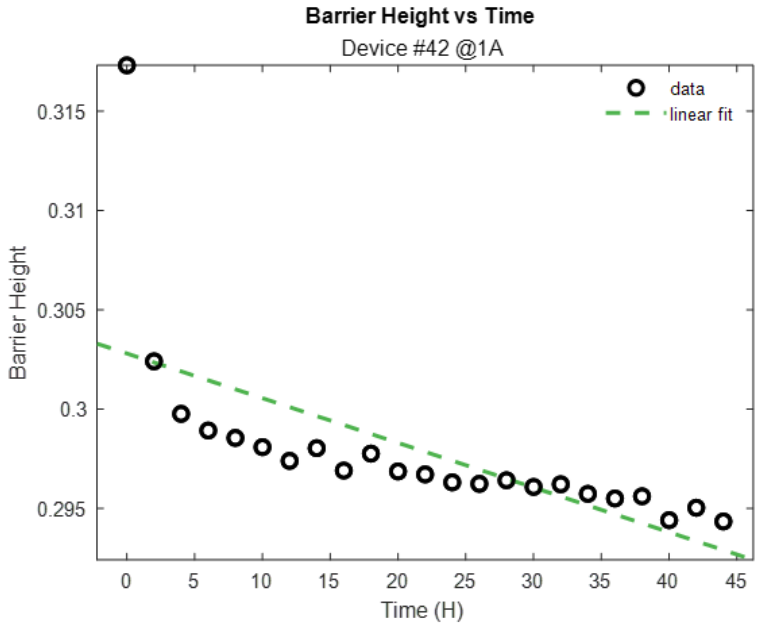

Figure 18. Barrier Height versus Time Device 42 Stressed at 1A.

Barrier height (BH) for device 42, displayed in Figure 18, did not change substantially over stressing period. Average barrier height was measured at 0.298V for device 42 which is much lower than the previous device. This uncharacteristically low barrier height could explain the high leakage current seen by the device. Unfortunately, the Python scripts used to plot inhomogeneity spread would not accept the data for device 42.

For stressing at 1A, both devices did not show significate changes in BH, likely due to low stressing current. Device 42 showed a significant decrease in leakage current during the stressing but also had an unusually low BH. The decrease in leakage current could be related to this defective BH. Device 27 did not show a large change in inhomogeneity spread, which is consistent with the low stress current.

2. Initial Testing 1.4A

Device 119 shows a small DD characteristic in Figure 19. Leakage current, displayed in Figure 20, over stressing period showed very little change over time with and average leakage current of -5.987 μA. BH, plotted in Figure 21, also showed little change over the stressing period, with average BH 0.841V. BH did show significant drops at

approximately 24-hour intervals. Inhomogeneity spread over the interval appears to not show much of a trend, shown in Figure 22.

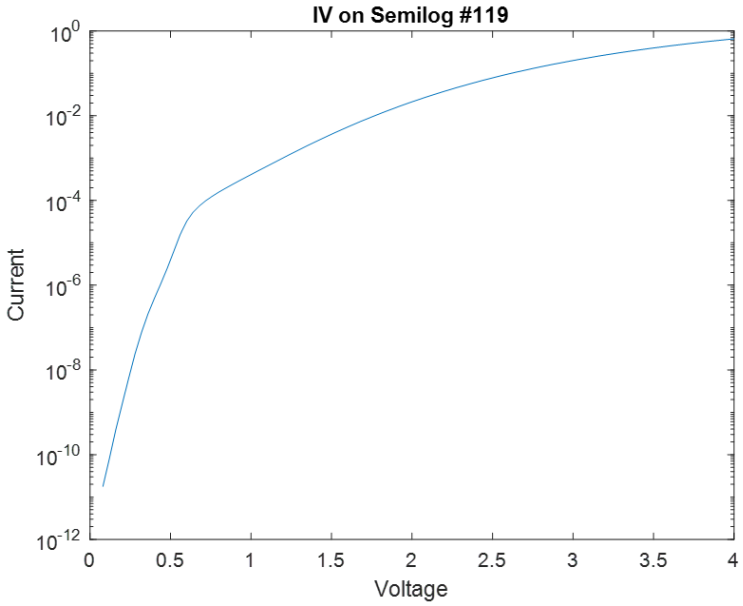

Figure 19. Semilogarithmic I-V Curve Device 119

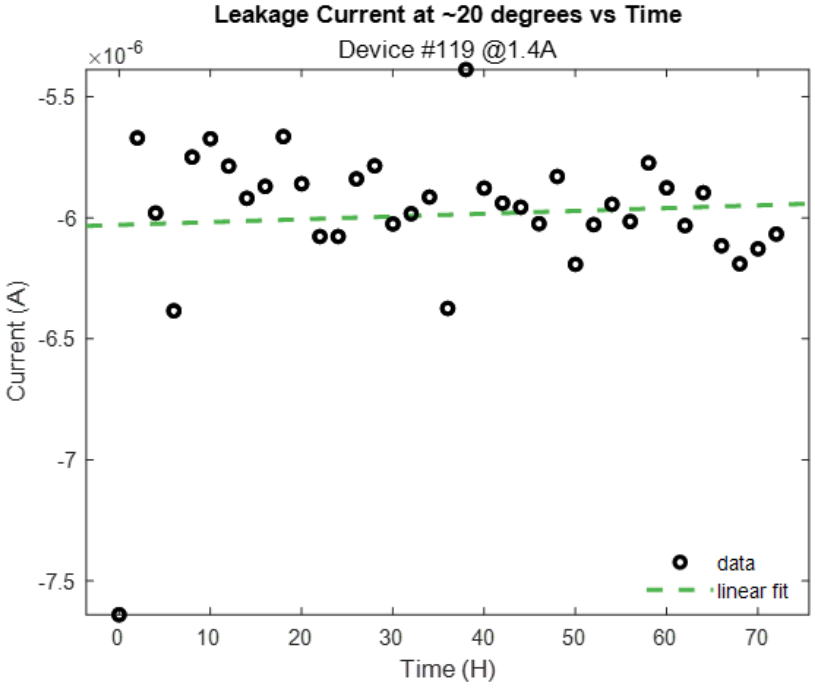

Figure 20. Leakage Current versus Time Device 119 Stressed at 1.4A

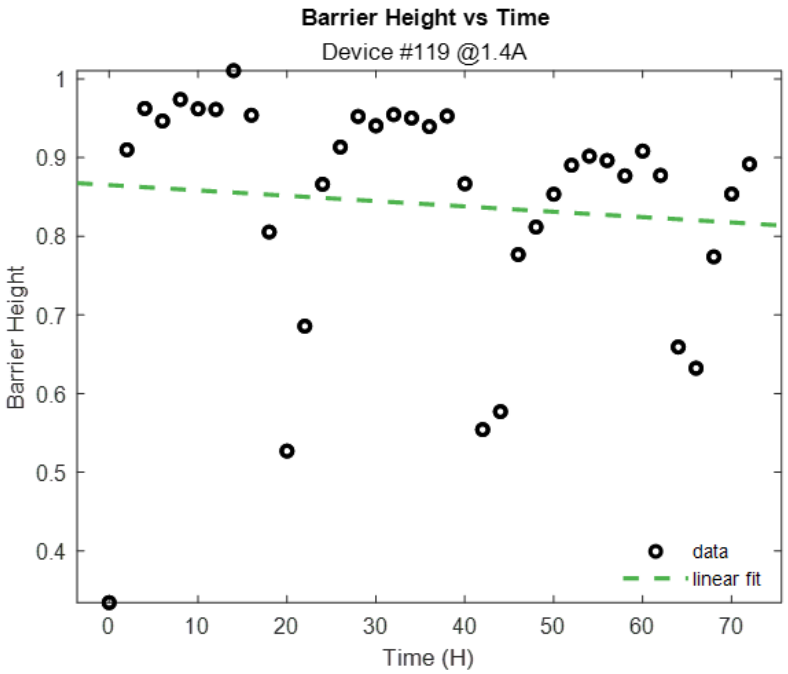

Figure 21. Barrier Height versus Time Device 119 Stressed at 1.4A

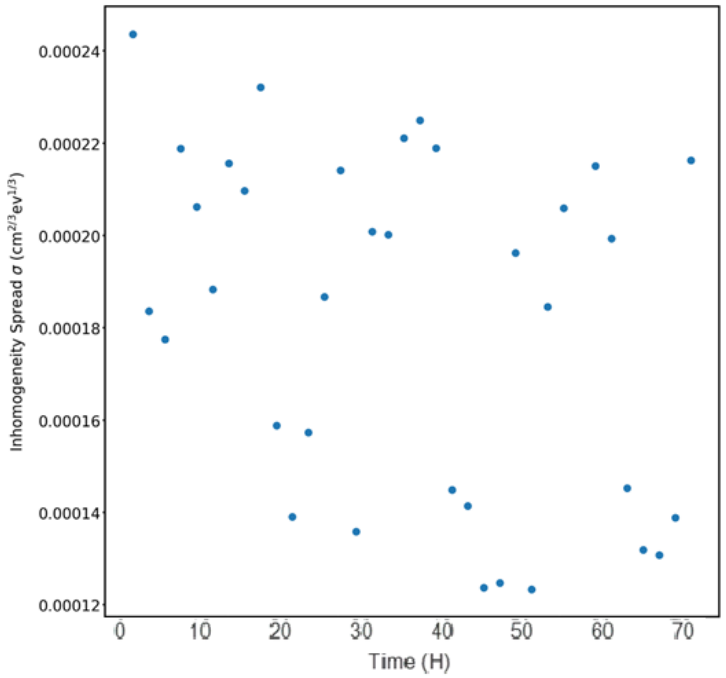

Figure 22. Inhomogeneity Spread versus Time Device 119 Stressed at 1.4A

Device 215 showed SD characteristics in the I-V plot in Figure 23. The leakage current plot in Figure 24 shows a 20% increase in leakage current over time with an average leakage current of -0.0883 μA. Barrier height for device 215, shown in Figure 25, exhibits an 8% decrease in BH over stressing period with an average BH of 0.968 V. The increase in leakage current could be explained by the decrease in BH. Again, inhomogeneity spread shows little change in Figure 26 likely due to low stress current.

Both devices stressed during this period showed small decreases in BH with device 215 having the greater decrease along with an increase in leakage current. The BH plots in Figures 21 and 25 both displayed significant drops in BH at 24-hour intervals during testing and then returned to the average BH in between the drops. This indicates some issue during testing at night, possibly the system struggling to maintain an even temperature. Inhomogeneity spread remained relatively constant during this testing.

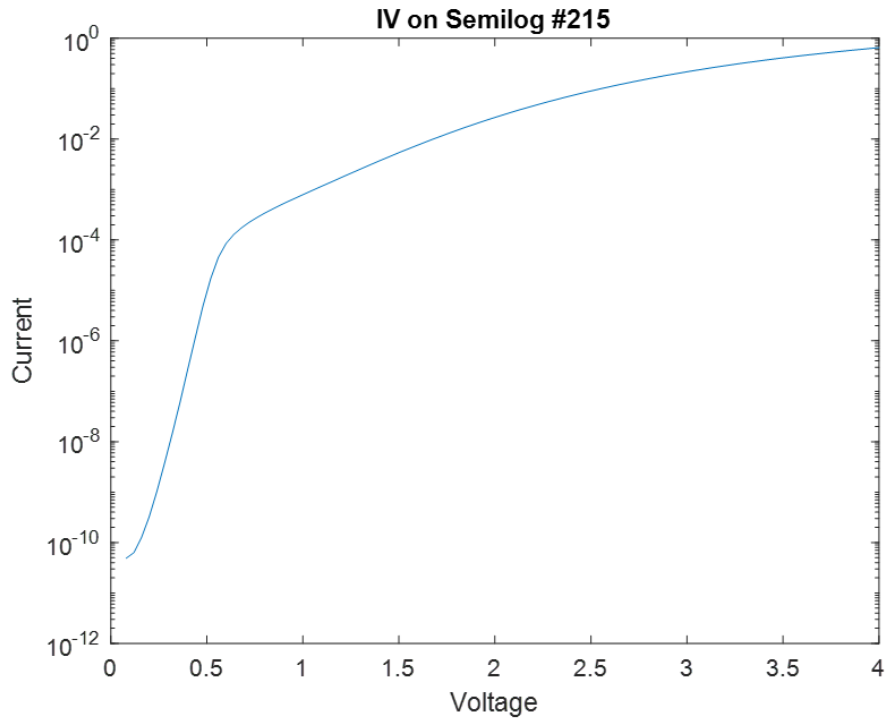

Figure 23. Semilogarithmic I-V Curve Device 215.

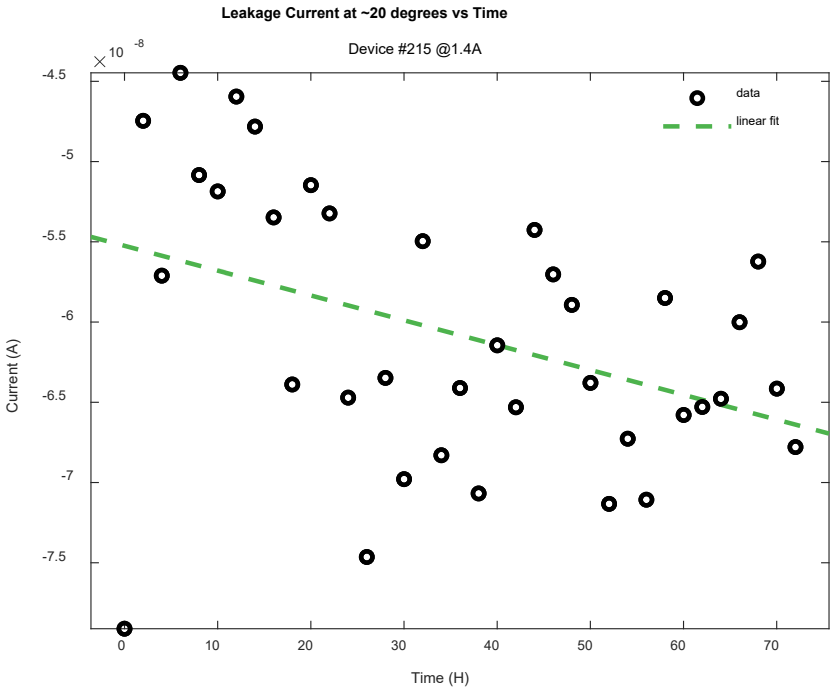

Figure 24. Leakage Current versus Time Device 215 Stressed at 1.4A.

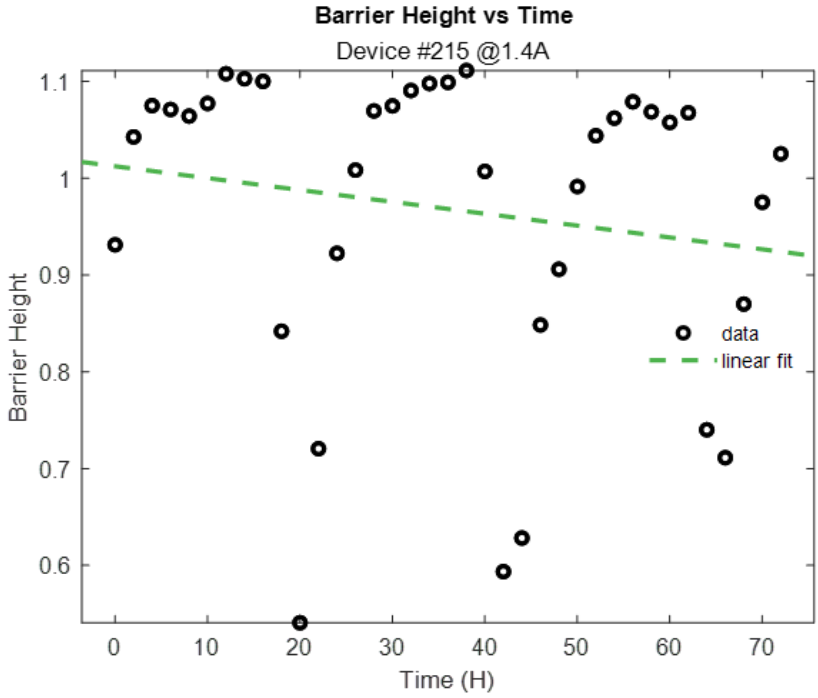

Figure 25. Barrier Height versus Time Device 215 Stressed at 1.4A

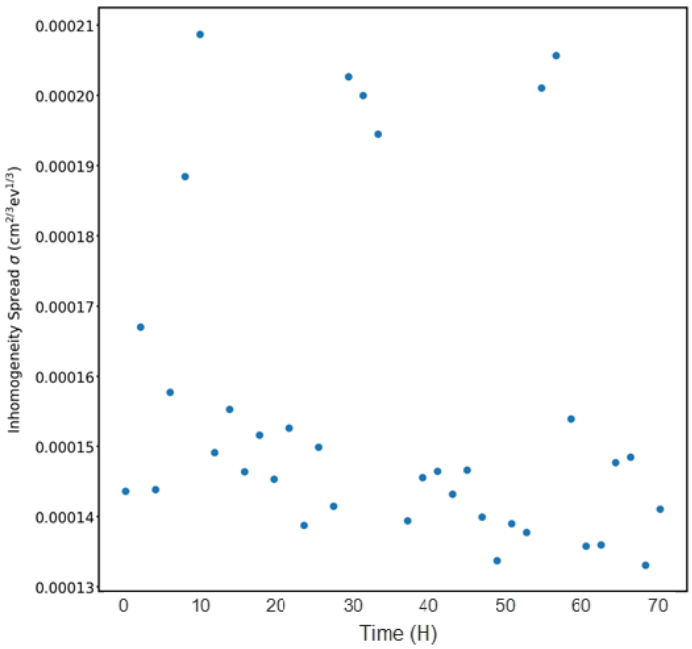

Figure 26. Inhomogeneity Spread versus Time Device 215 Stressed at 1.4A

3. Initial Testing 1.6A

Device 152 showed SD characteristics in Figure 27. Leakage current increased over time by 26% with an average leakage current of -0.841 μA, shown in Figure 28. BH, shown in Figure 29, decreased overtime by 10% with an average BH of .862 V which would account for the increase leakage current. Inhomogeneity spread for this device, shown in Figure 30, again remained relatively constant despite a few outliers, likely due to noise in the system.

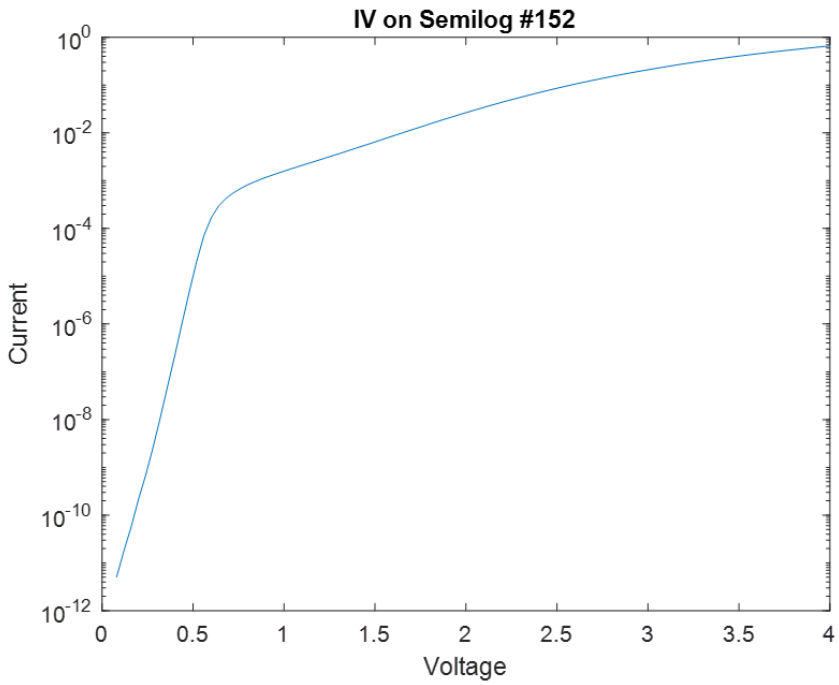

Figure 27. Semilogarithmic I-V Curve Device 152

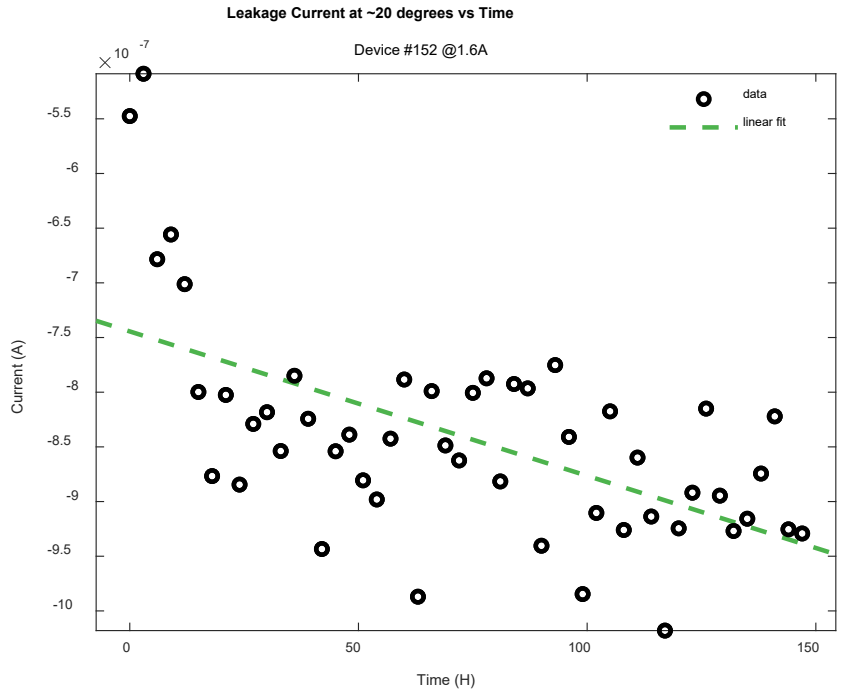

Figure 28. Leakage Current versus Time Device 152 Stressed at 1.6A.

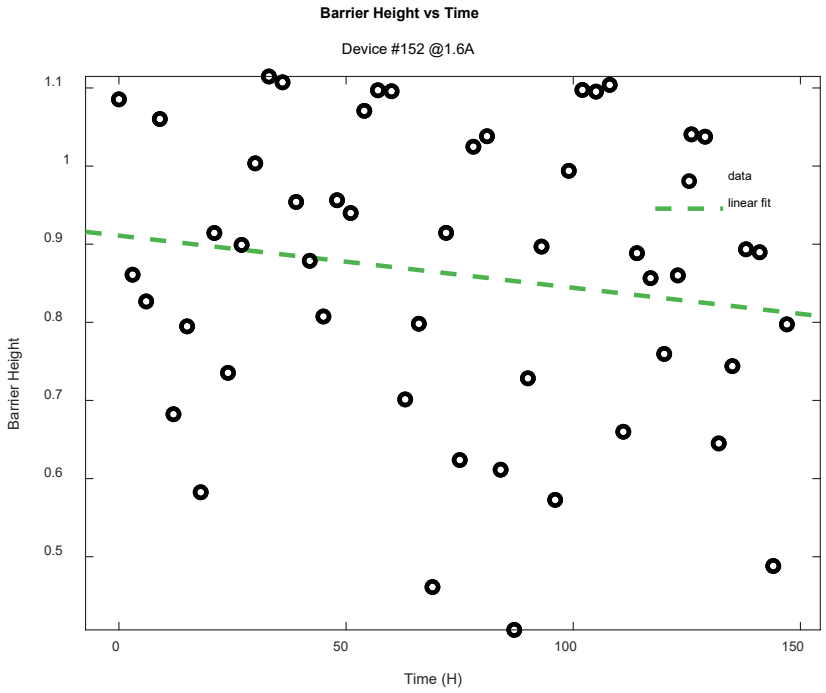

Figure 29. Barrier Height versus Time Device 152 Stressed at 1.6A.

Device 238 exhibited SD characteristics shown in Figure 31. Leakage Current for the device, shown in Figure 32, increased by 77% over the stressing period with an average leakage current of -0.0161 μA. The BH for device 238, shown in Figure 33, remained the same with an average of .772 V. The average leakage current was the lowest of all devices tested, which could account for the large percent increase as the device was stressed. Even with the increase in leakage current, the device did not reach the level of leakage current of the other devices. So, despite the large percentage change, the actual leakage current of the device did not increase very much. Inhomogeneity spread, shown in Figure 34, appeared to jump between two values, possibly indicating a degradation of the device over stressing period.

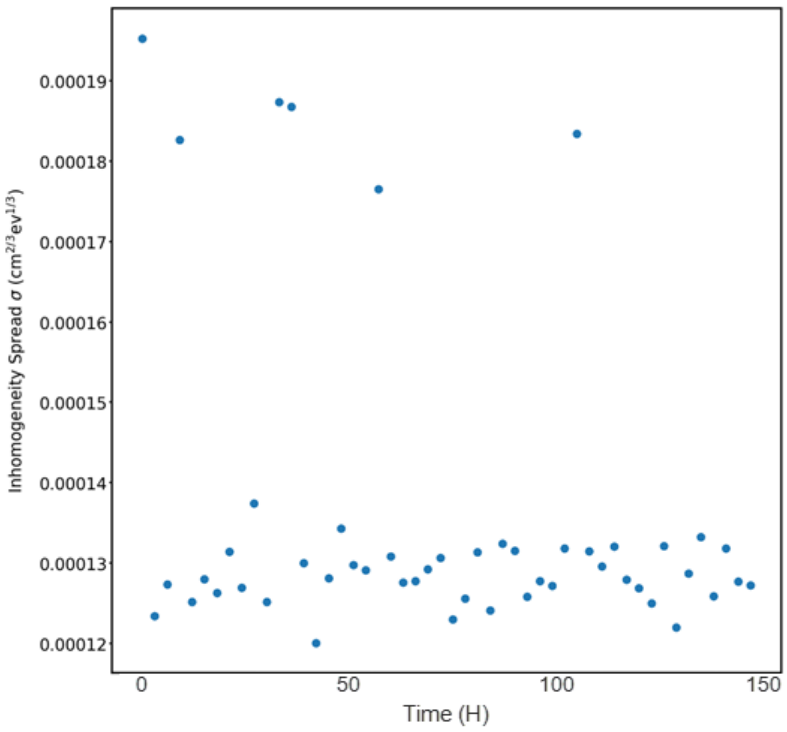

Figure 30. Inhomogeneity Spread versus Time Device 152 Stressed at 1.6A

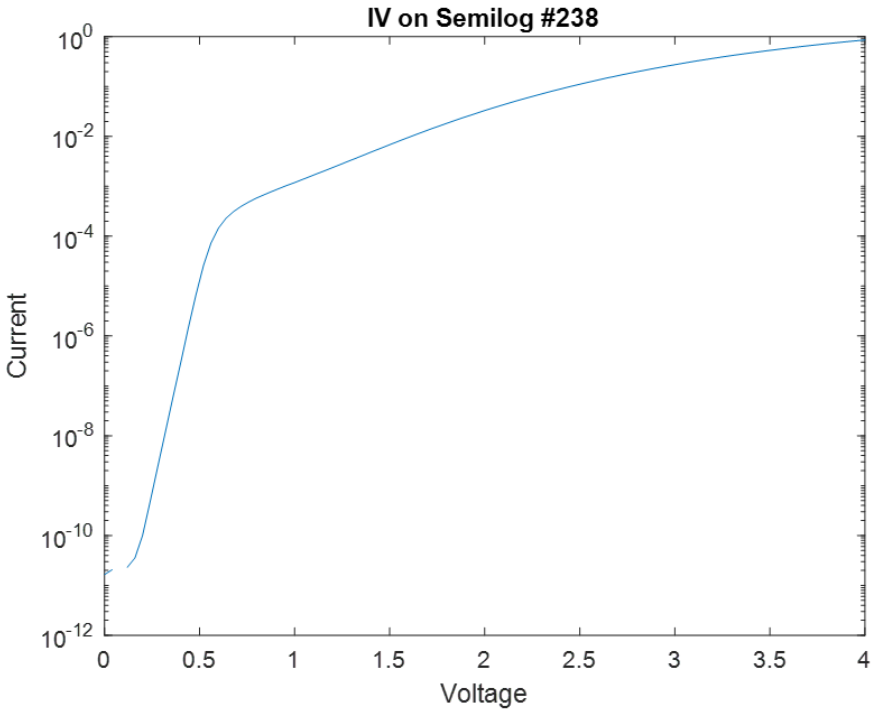

Figure 31. Semilogarithmic I-V Curve Device 238

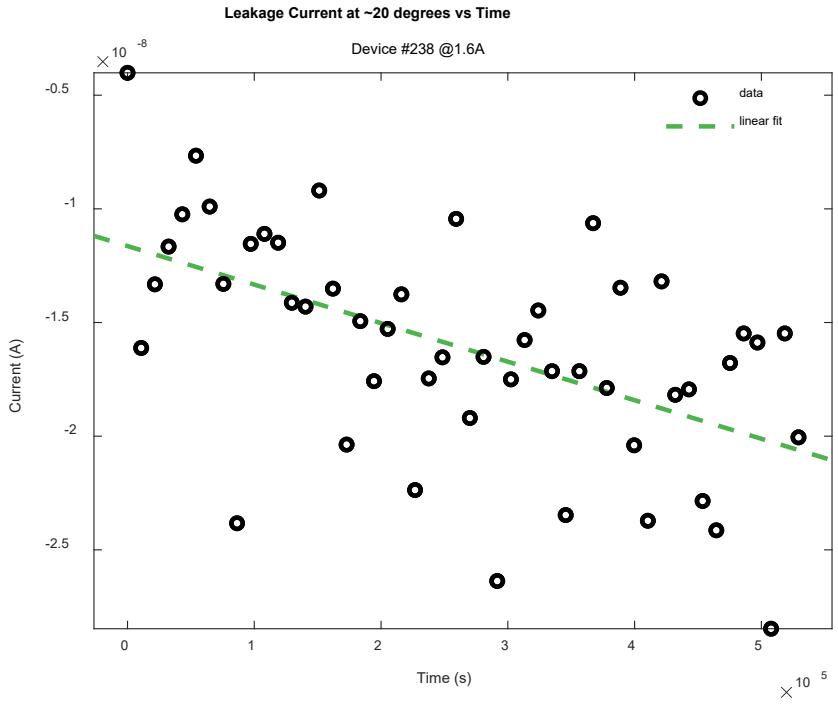

Figure 32. Leakage Current versus Time Device 238 Stressed at 1.6A

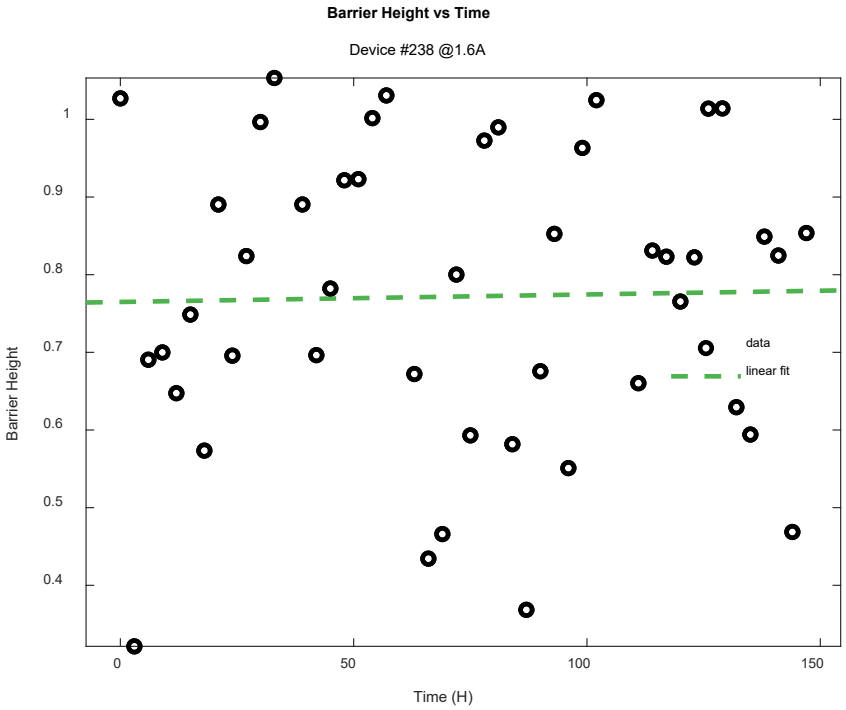

Figure 33. Barrier Height versus Time Device 238 Stressed at 1.6A

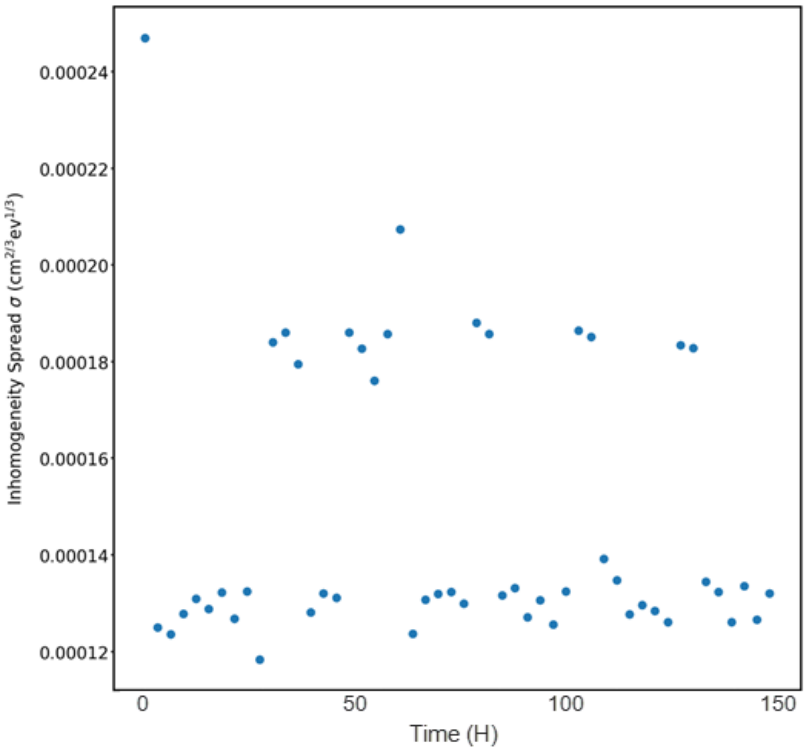

Figure 34. Inhomogeneity Spread versus Time Device 238 Stressed at 1.6A

At 1.6A of stress testing, device 152 showed a significant decrease in BH while device 238 was unchanged. Both devices exhibited increases in leakage current, but due to the low average leakage current, device 238 actual increase in leakage current was small compared to Device 152 which can be explained by the little change in BH. The BH plots shown in Figures 29 and 26 also displayed significant variance at this level of stress. Inhomogeneity spread for both devices seemed to jump between two values after a short period of stressing. This could possibly indicate a degradation in the interface of the devices.

4. Initial Testing 1.8A

Device 176 showed DD characteristics in Figure 35. The leakage current for this device, shown in Figure 36, decreased by 15% over the stressing period with an average of -0.438 μA. The BH, shown in Figure 37, also decreased over the period by 40% with an average of .307V. With the BH so low, like device 42, it is apparent that this diode was not

performing correctly and is likely why both BH and leakage current decreased. Inhomogeneity spread could also not be plotted for the devices stressed at 1.8A due to the Python scripts not accepting the data.

Device 216 displayed SD characteristics shown in Figure 38. Figure 39 displays the leakage current which increased by 39% over the stressing period, with an average of -0.0816 μA. The BH for the device, shown in Figure 40 decreased by 81% over the stressing period, indicating that the device was highly degraded by the stressing. It also accounts for the large increase in leakage current.

At 1.8A of stress current, both devices showed large degradation of BH, but since device 176 began the testing with a very low barrier height, it indicates the device was already degraded at the beginning of testing, which may account for the odd decrease in leakage current. Device 216 showed a large decrease in BH and large increase in leakage current which is expected.

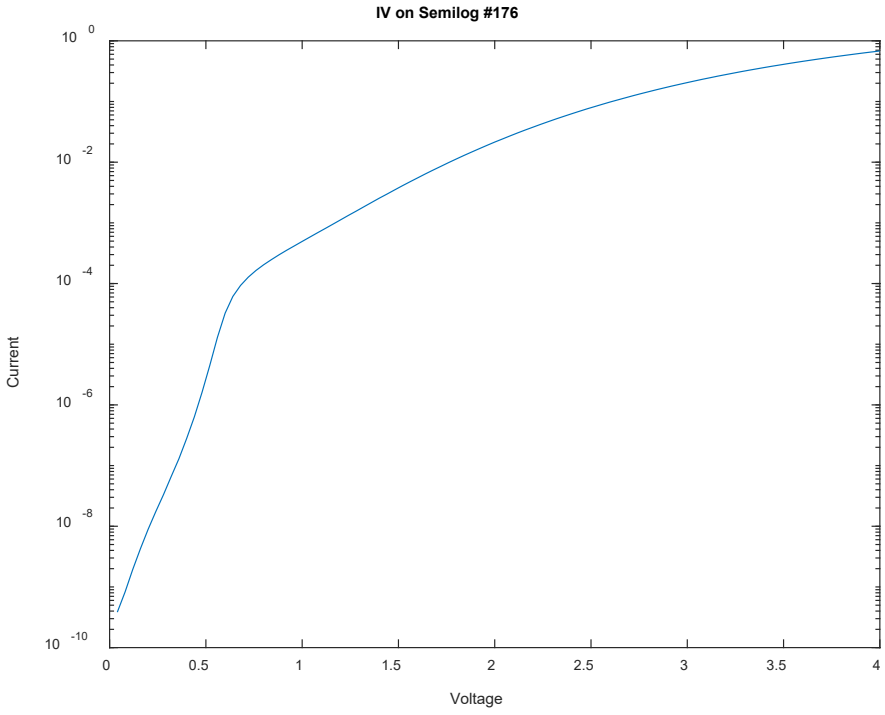

Figure 35. Semilogarithmic I-V Curve Device 176.

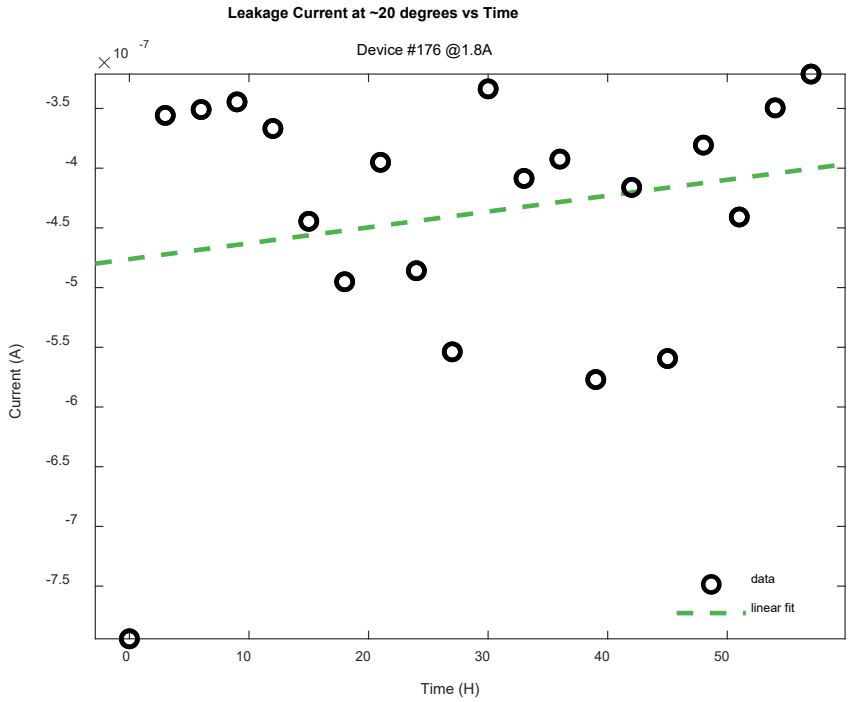

Figure 36. Leakage Current versus Time Device 176 Stressed at 1.8A

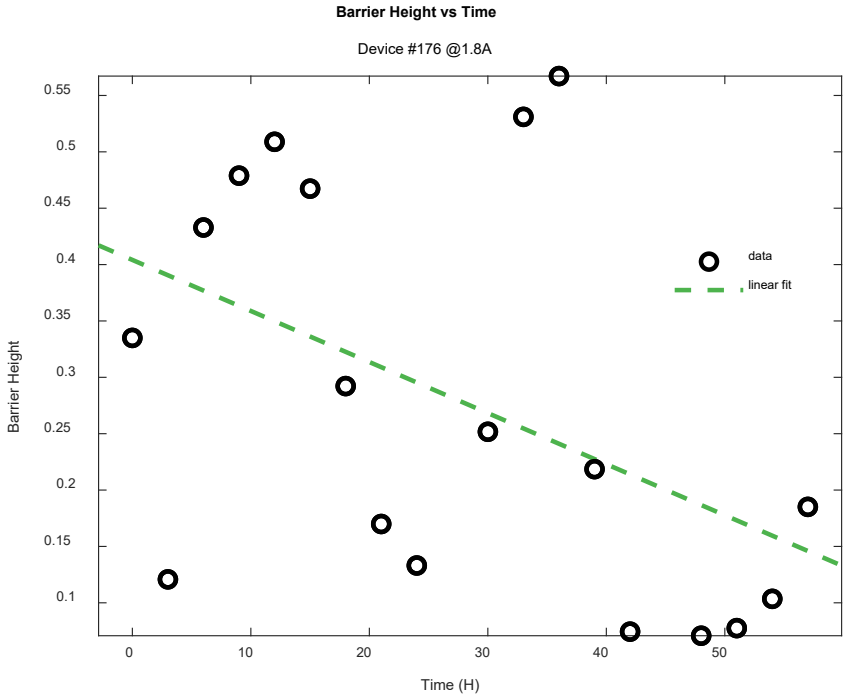

Figure 37. Barrier Height versus Time Device 176 Stressed at 1.8A

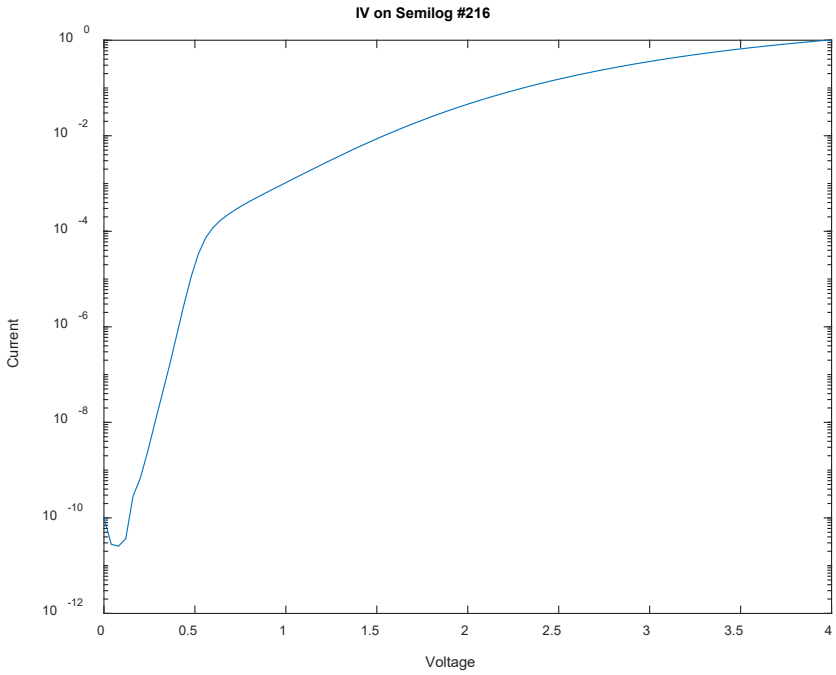

Figure 38. Semilogarithmic I-V Curve Device 216

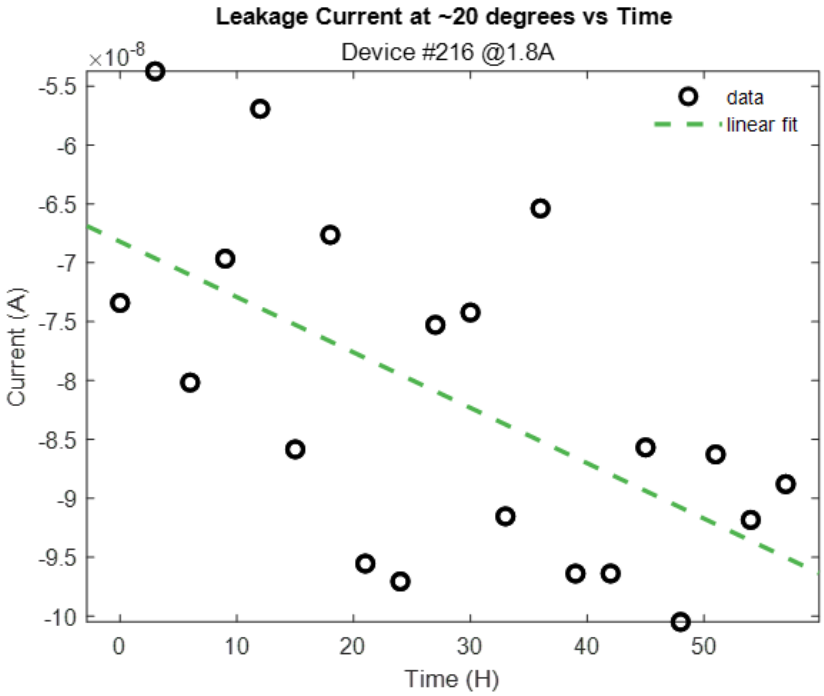

Figure 39. Leakage Current versus Time Device 216 Stressed at 1.8A

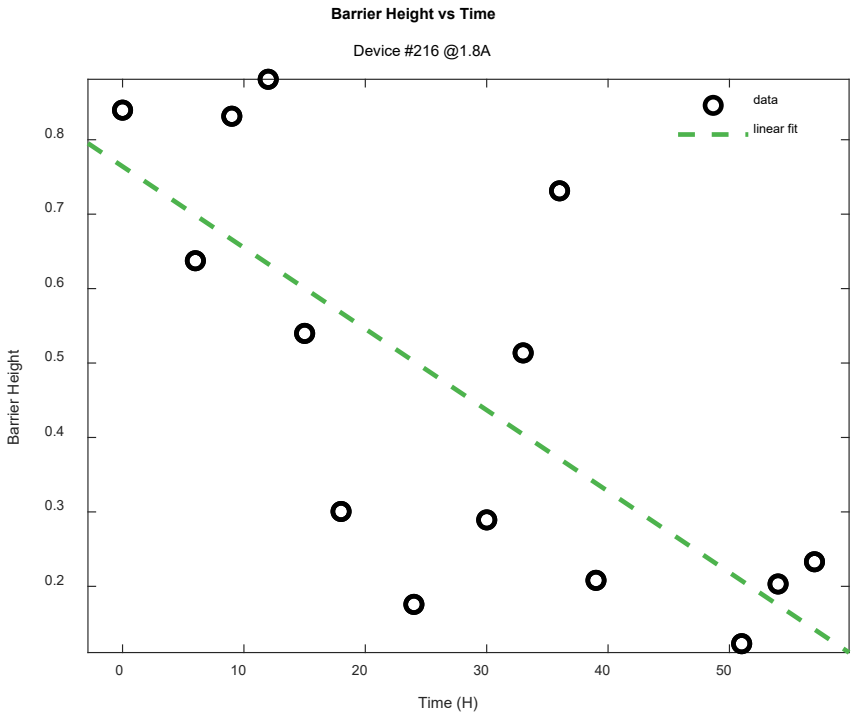

Figure 40. Barrier Height versus Time Device 216 Stressed at 1.8A

5. Results Initial Testing

Table 3 shows the results of all the devices tested during initial (short term) testing. Of the 8 devices tested, all showed either little change in BH or a decrease over the stressing period. Devices showed stronger degradation of BH as stress current was increased except for in the case of device 238, stressed at 1.6A, which showed no change in BH and seemed to show little degradation. 5 of the 8 devices showed increase leakage current over the testing period, with current generally increasing more rapidly at higher stress currents. The leakage current for device 27 decreased by 9% but was stressed at a low current and showed little degradation in BH. Devices 42 and 172 showed large decreases in leakage current but both devices had unusually low BH to begin with indicating that both devices were degraded at the beginning of testing. Overall, the initial testing showed stressing both decreased BH and increased leakage current over the period with degradation increasing with stressing current. At low stressing, devices showed little change in inhomogeneity

spread. The devices stressed at 1.6A seemed to begin to show degradation, but unfortunately, the inhomogeneity could not be capture for the devices at 1.8A.

Table 3. Results of Initial Testing

Device #	Strs Cur (A)	Diode	BH Avg (V)	BH Chng (V)	BH Chng %	LC Avg (µA)	LC Chng (µA)	LC Chng %
27	1	SD	1.117	0.0391	3.6	-0.0242	0.00226	-8.9
42	1	DD	0.298	-0.0099	-1	-9.963	2.99	-26.1
119	1.4	DD	0.841	-0.0489	-5.7	-5.987	0.0832	-1.4
215	1.4	SD	0.968	-0.0883	-8.7	-0.0608	-0.0111	20.2
152	1.6	SD	0.862	-0.0981	-10.8	-0.841	-0.194	26.1
238	1.6	SD	0.772	0.0142	1.9	-0.0161	-0.00897	77.1
176	1.8	DD	0.307	-0.153	-39.9	-0.438	0.0757	-15.9
216	1.8	SD	0.453	-0.622	-81.4	-0.0816	-0.0268	39.3

Strs Cur: Stress Current, Avg: Average Value Over Testing, Chng: Change in value Over Testing, Chng %: Percentage Change of Value over Testing

B. LONG-TERM TESTING FOR APPROXIMATELY 336 HOURS

Long-term testing was completed on 6 devices at 1.5A, 1.75A, and 2A. Due to issues with running the equipment for that long of a period, the system was restarted each day to prevent connectivity time out. The data from each day was then combined by adding time from the previous days testing. Measurements were taken every 3 hours at the same temperatures as with the initial testing and calculations were completed in the same manner as well. At the end of this section, Table 4 shows the overall results of the long-term testing.

1. Long-Term Testing 1.5A

Device 239 showed SD characteristics during stressing in Figure 41. The leakage current, plotted in Figure 42, decreased by 19% over the stressing period with an average current of -2.362 µA. The BH, displayed in Figure 43, for the diode increased 3% during the stressing with an average of 0.701 V. This small increase in BH may have been caused by annealing of the diode and could explain the decrease in leakage current. Inhomogeneity spread, displayed in Figure 44, began inconsistently, but settled out after some initial stressing.

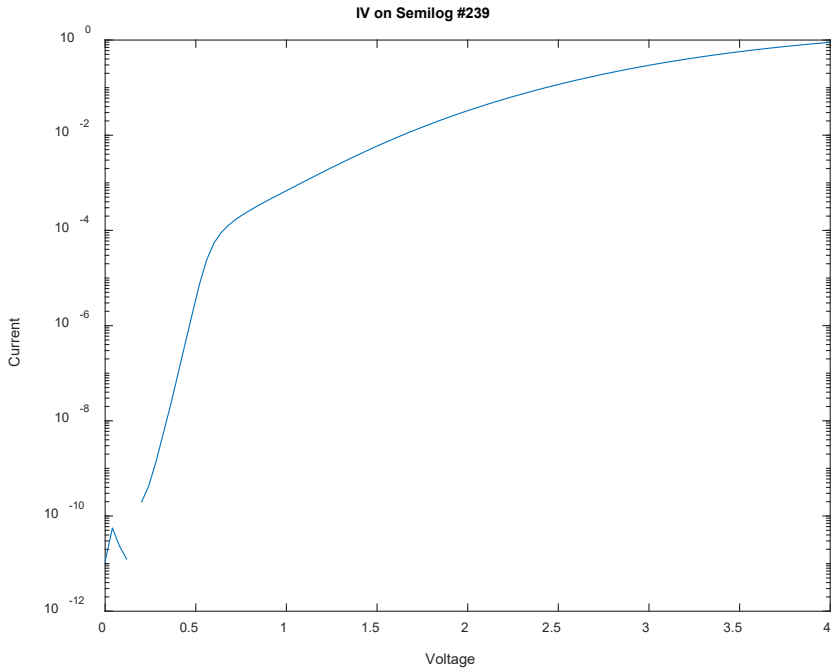

Figure 41. Semilogarithmic I-V Curve Device 239

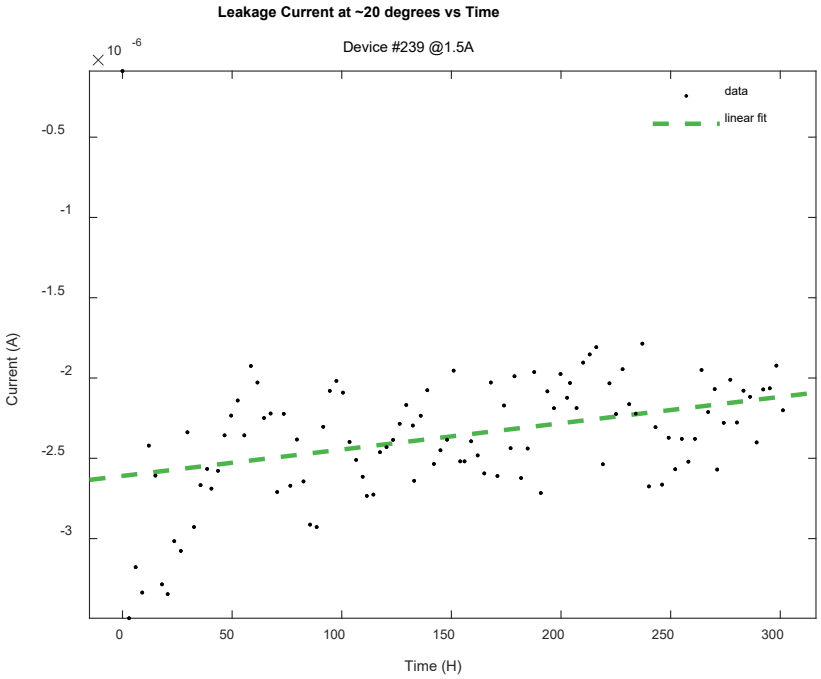

Figure 42. Leakage Current versus Time Device 239 Stressed at 1.5A

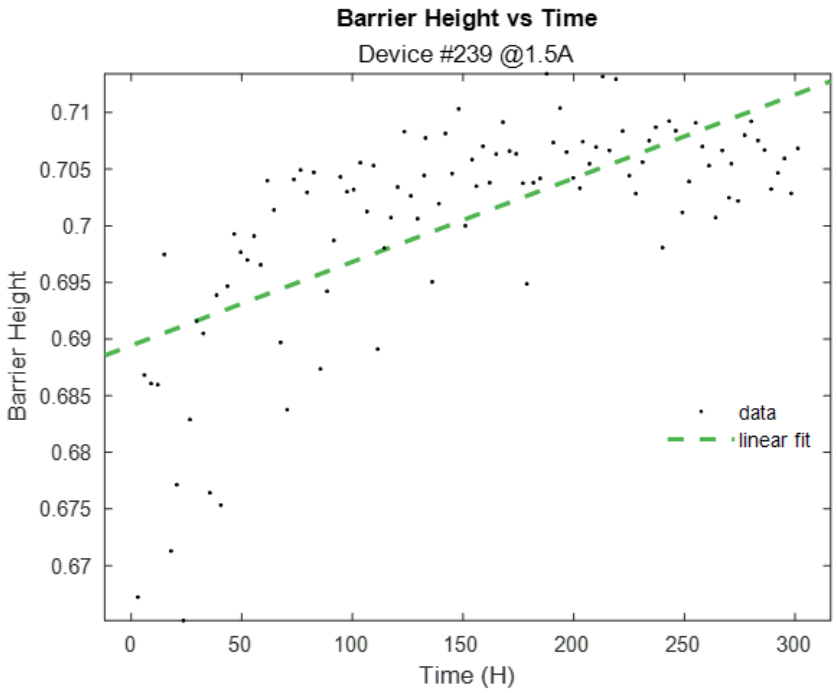

Figure 43. Barrier Height versus Time Device 239 Stressed at 1.5A

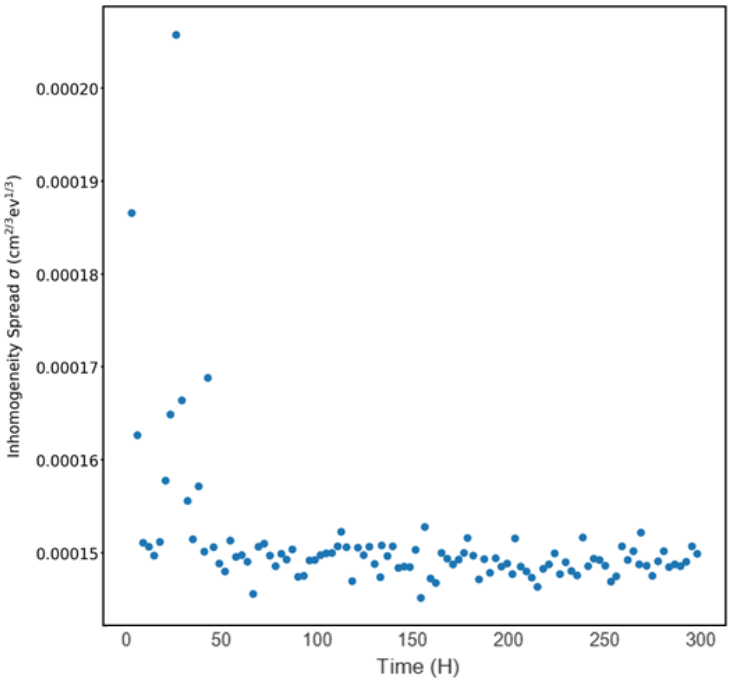

Figure 44. Inhomogeneity Spread versus Time Device 239 Stressed at 1.5A

Device 314 showed SD characteristics shown in Figure 45. The leakage current, plotted in Figure 46, shows that the leakage current increased by 20% during testing with an average of -0.089 μA. The BH, plotted in Figure 47, increased by 18% over the testing with an average of .999 V. Inhomogeneity spread was very inconsistent in this stressing period, shown in Figure 48.

At 1.5A of stress current, both diodes BH increased during the stressing period. However, only Device 239 showed the decrease in leakage current that was expected with this. This odd behavior by device 314, showing increase in BH and leakage current, does not fit the predictions of the diodes. This odd behavior could account for the differences in the inhomogeneity spread of the two diodes.

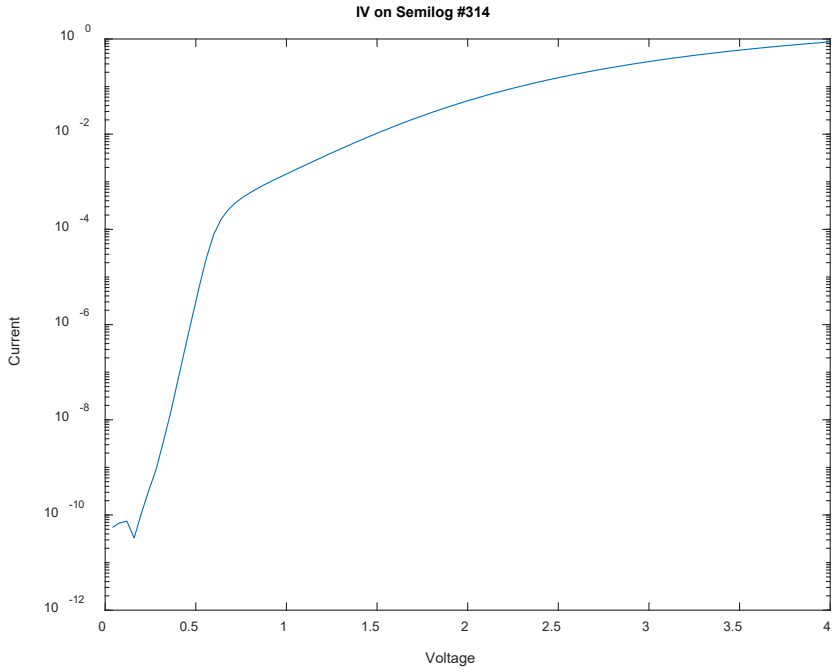

Figure 45. Semilogarithmic I-V Curve Device 314

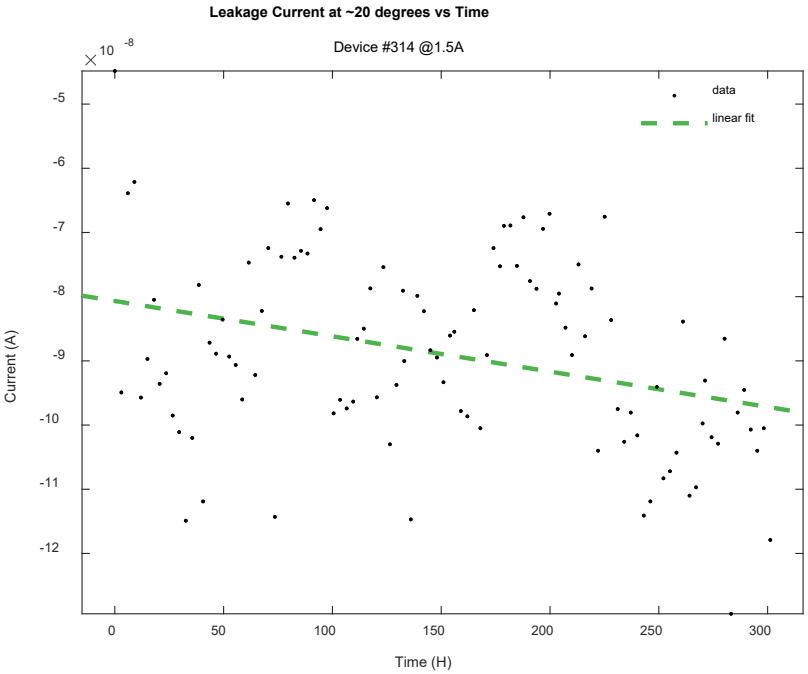

Figure 46. Leakage Current versus Time Device 314 Stressed at 1.5A

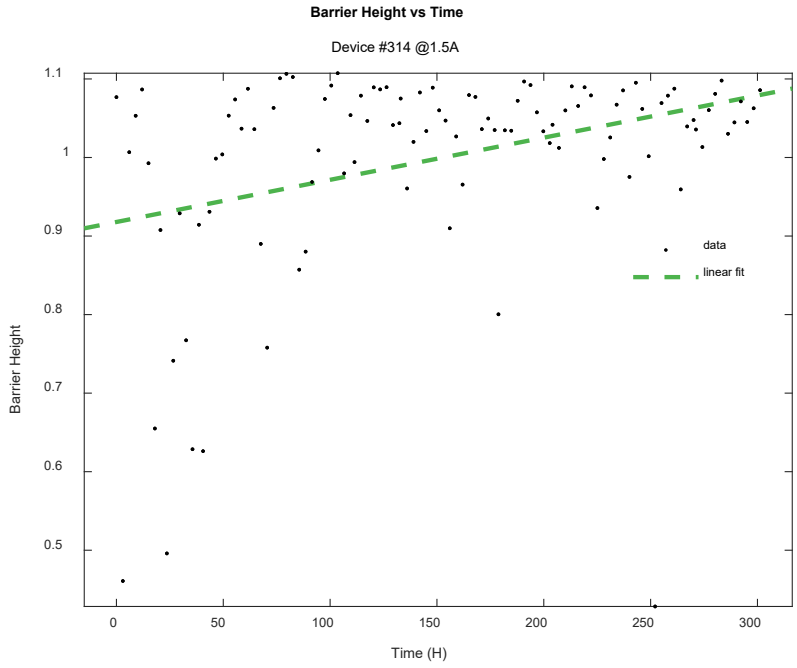

Figure 47. Barrier Height versus Time Device 314 Stressed at 1.5A

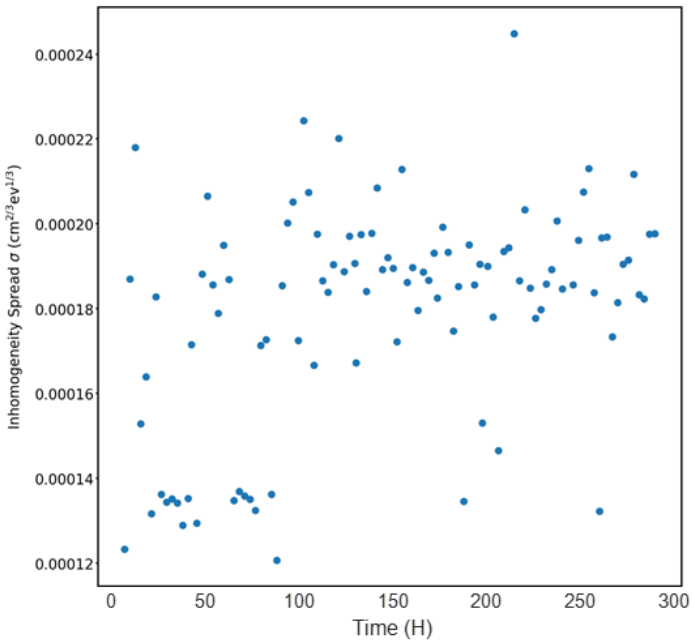

Figure 48. Inhomogeneity Spread versus Time Device 314 Stressed at 1.5A

2. Long-Term Testing 1.75A

Device 115 shows DD characteristics in Figure 49. The leakage current, shown in Figure 50, decreased 17% over time with an average current of -0.222 μA. BH, displayed in Figure 51, increased 5% overtime with an average BH of .913 V. Unfortunately, the Python scripts would not accept the data for the diodes tested at this stressing current.

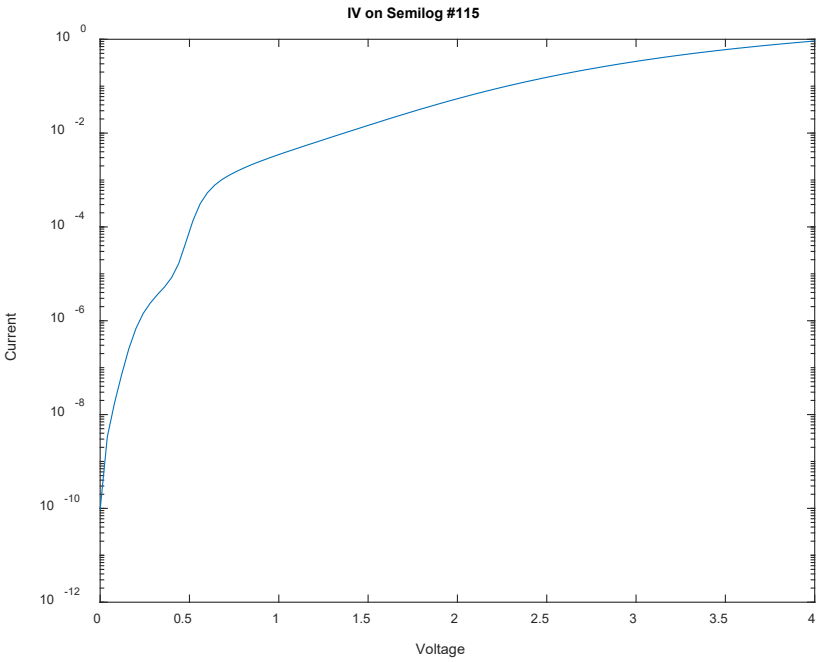

Figure 49. Semilogarithmic I-V Curve Device 115

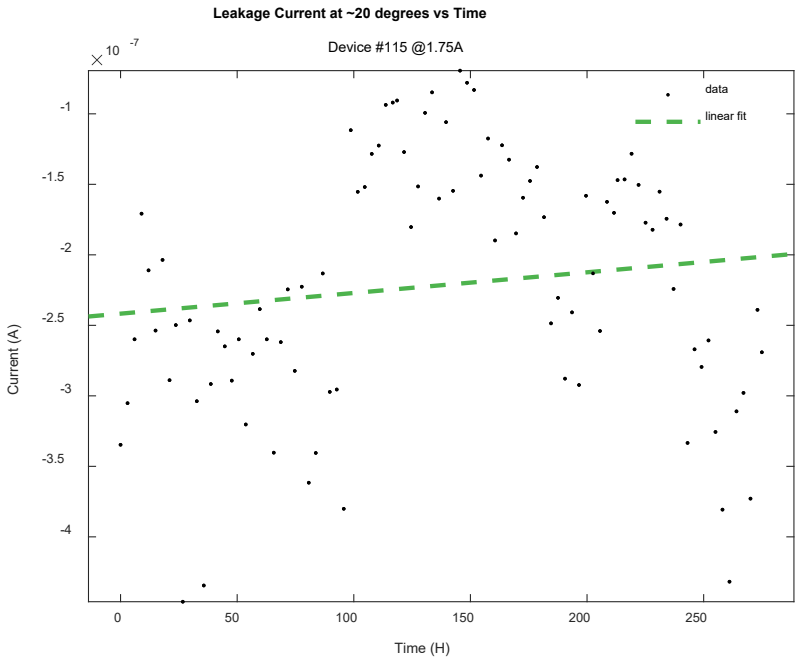

Figure 50. Leakage Current versus Time Device 115 Stressed at 1.75A

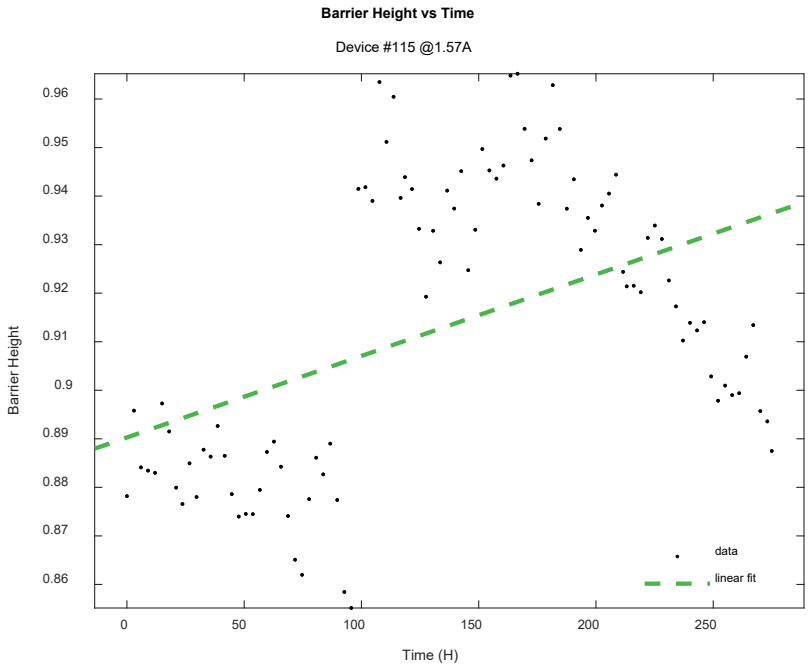

Figure 51. Barrier Height versus Time Device 115 Stressed at 1.75A

Device 206 showed SD characteristic in Figure 52. Figure 53 shows the leakage current for the device increased by 12% over the stressing period with an average leakage current of -0.427 μA. The BH, shown in Figure 54, increased by 4% over the stressing period with an average BH of .779 V.

Again, at this testing sequence, both diodes showed increases in BH over the stressing period. Also, as with the previous long term test at 1.5A, one of the diodes, device 115, showed decrease in leakage current, while the other, device 206, had its leakage current increase. With increase in BH, one would expect the leakage current to decrease but again, one of the devices defies that logic. During this testing, both devices leakage current, shown in Figure 50 and 53, there was a large decrease in leakage current halfway through the stressing that then began to increase. This anomaly likely because of an extended off period where the system stopped testing prematurely and had to be restarted. This may explain for the contradictory nature of this stress testing.

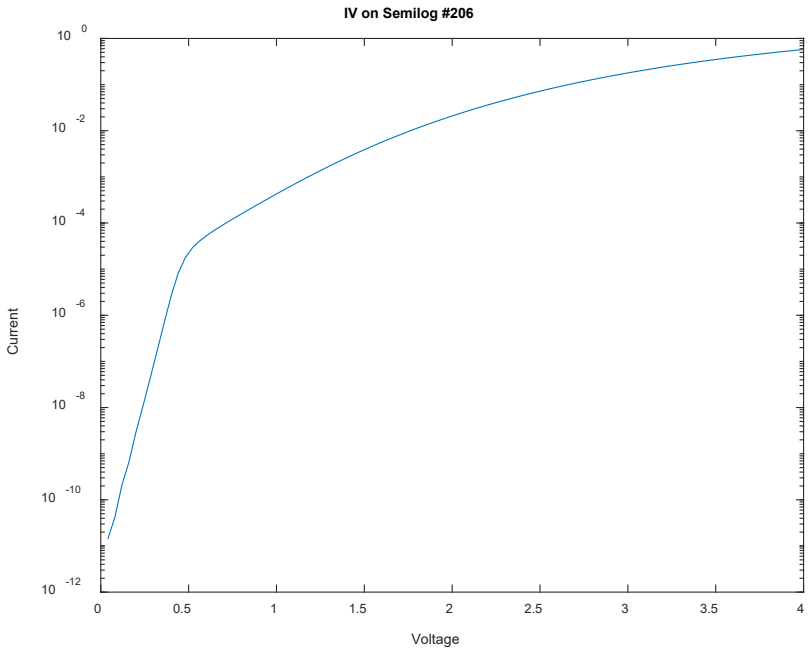

Figure 52. Semilogarithmic I-V Curve Device 206

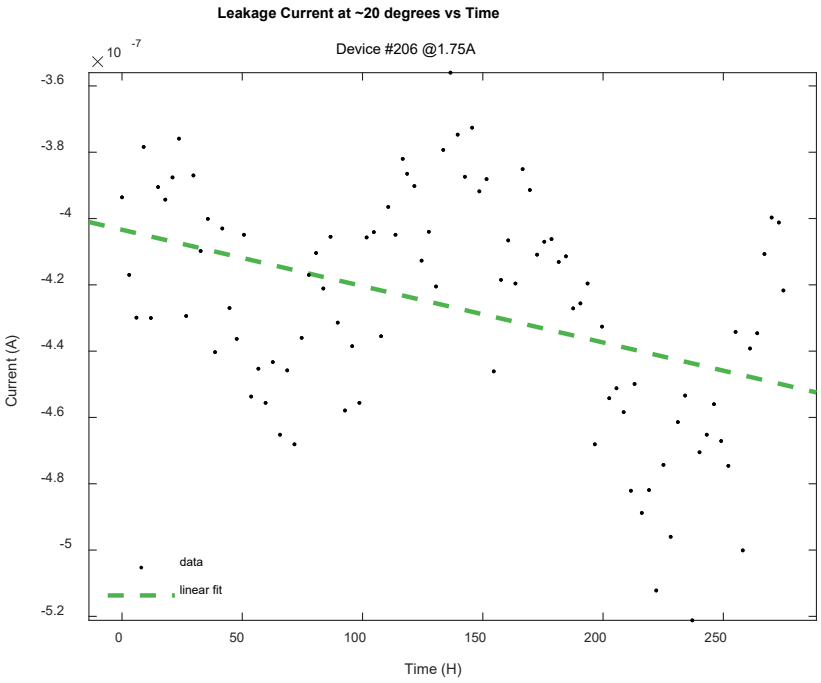

Figure 53. Leakage Current versus Time Device 206 Stressed at 1.75A

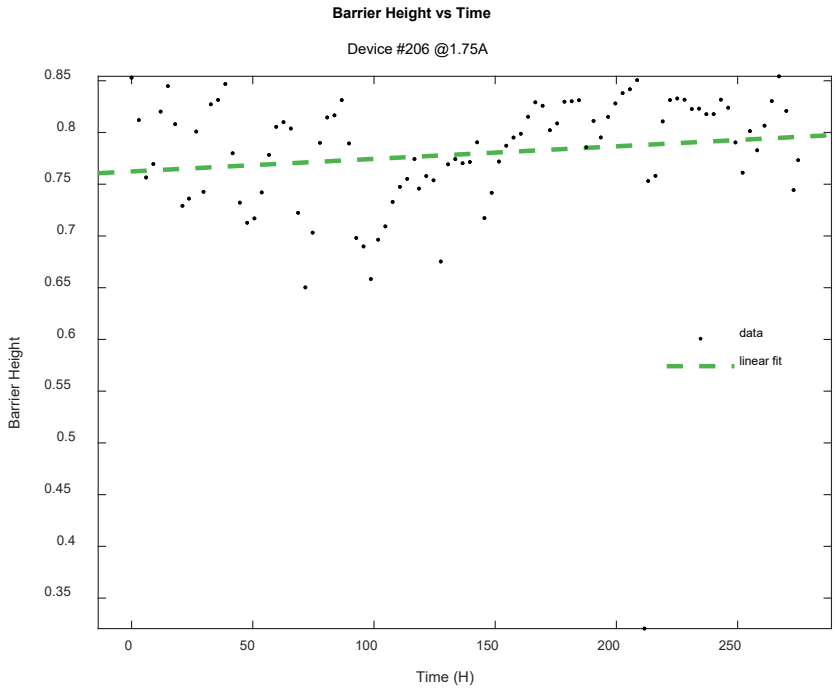

Figure 54. Barrier Height versus Time Device 206 Stressed at 1.75A

3. Long-Term Testing at 2A

Device 207 showed SD characteristics in Figure 55. The leakage current, plotted in Figure 56, showed decreasing current over the stressing period by 32% with an average current of -1.021 μA. The BH, plotted in Figure 57, increased by 3% over the stressing period with an average of .585V. The device shows the expected characteristic of decreasing leakage current with increasing BH. Figure 58 shows an apparent decrease in inhomogeneity spread over the testing period. At this stress current, the device appears to be degrading.

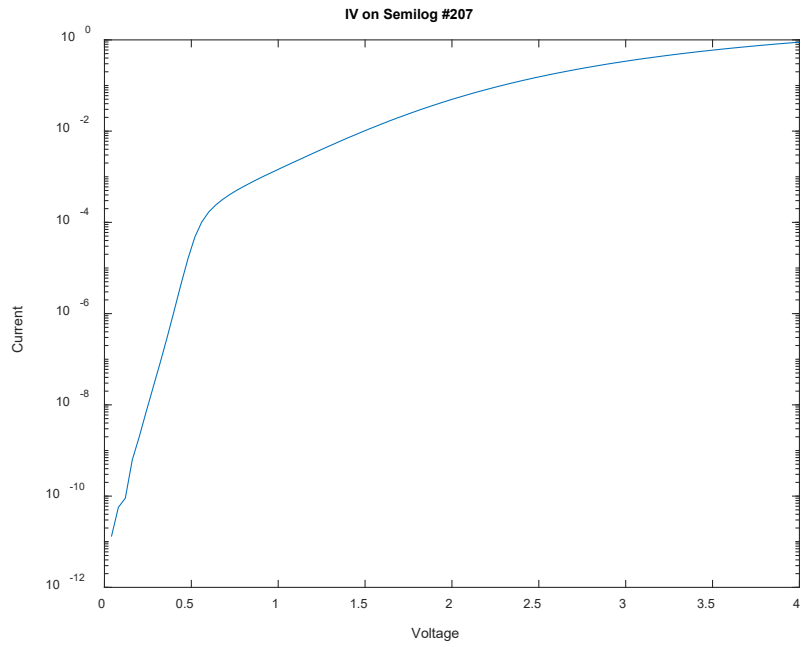

Figure 55. Semilogarithmic I-V Curve Device 207

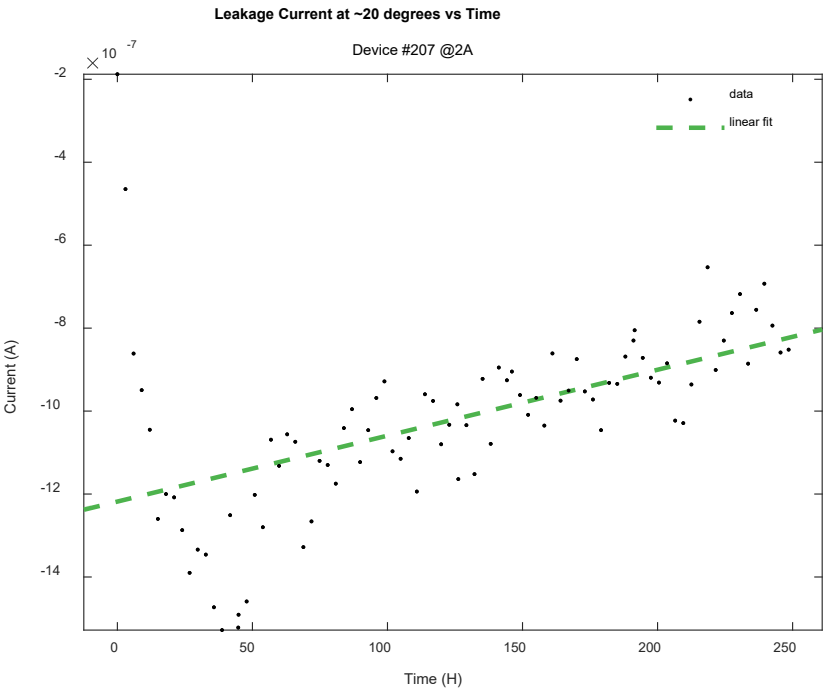

Figure 56. Leakage Current versus Time Device 207 Stressed at 2A

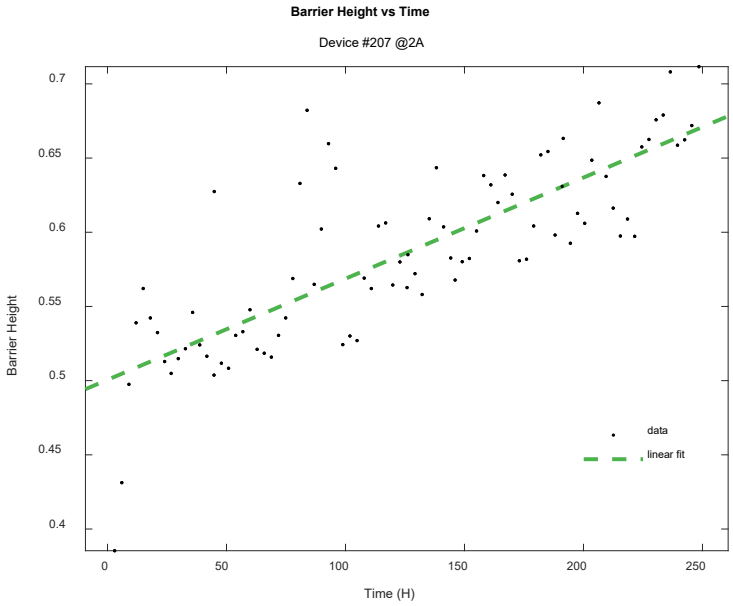

Figure 57. Barrier Height versus Time Device 207 Stressed at 2A

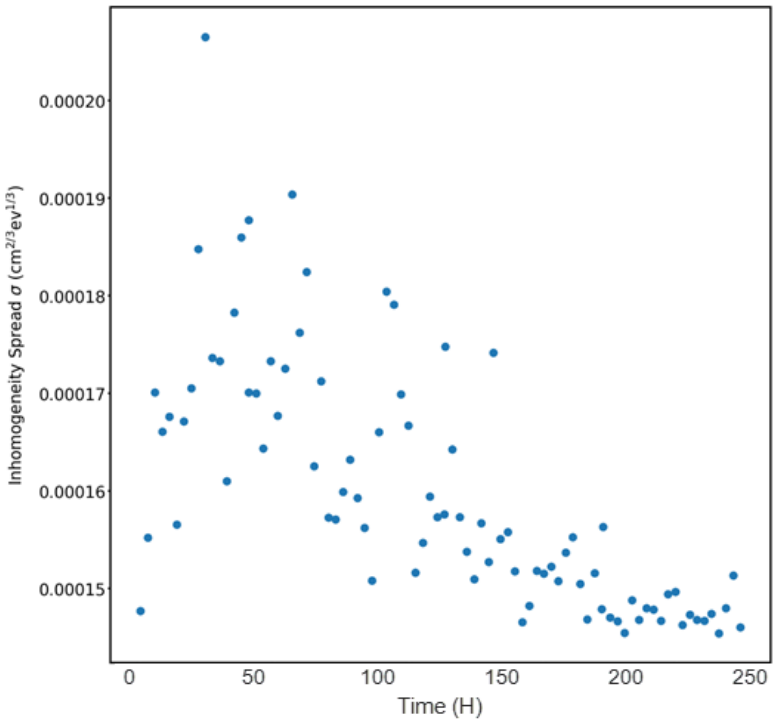

Figure 58. Inhomogeneity Spread versus Time Device 207 Stressed at 2A

Device 313 showed SD characteristics, plotted in Figure 59. The plot of the leakage current of the device in Figure 60 shows that leakage current decreased by 7% over the stressing period with an average current of -1.17 μA. The BH of the device, shown in Figure 61, shows that the BH for the device increased by 6% over the stressing period with an average of .576 V. Figure 62 again shows the inhomogeneity spread decreasing over the stressing period.

During this sequence of stressing, both devices displayed decreasing leakage current and increasing BH. The devices also had the lowest average BH of any of the devices tested during long term testing. The devices also had decreasing inhomogeneity spread over the stressing period. This is the first time that a strong trend was observed.

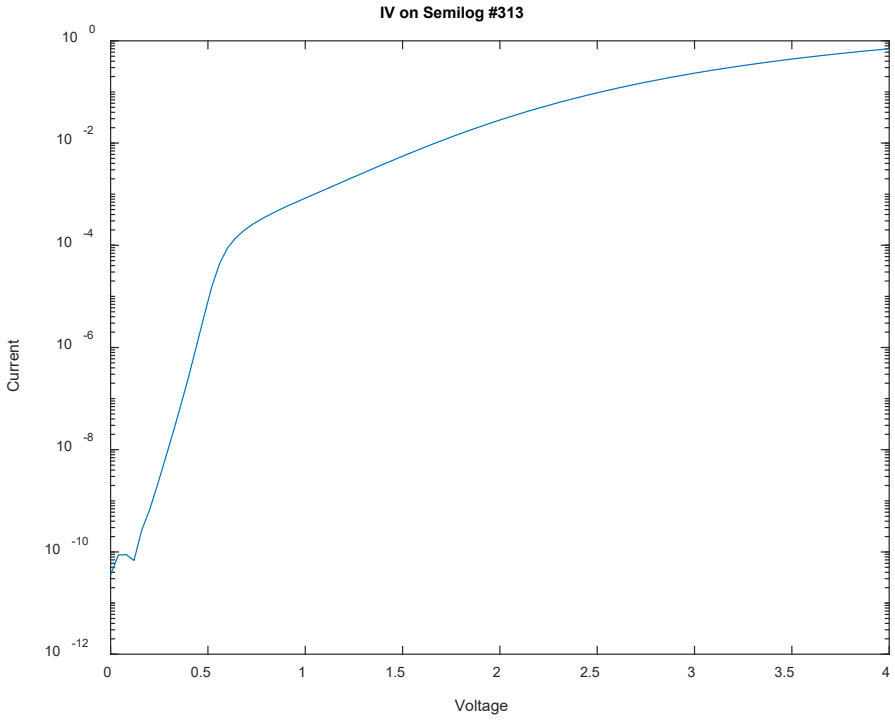

Figure 59. Semilogarithmic I-V Curve Device 313

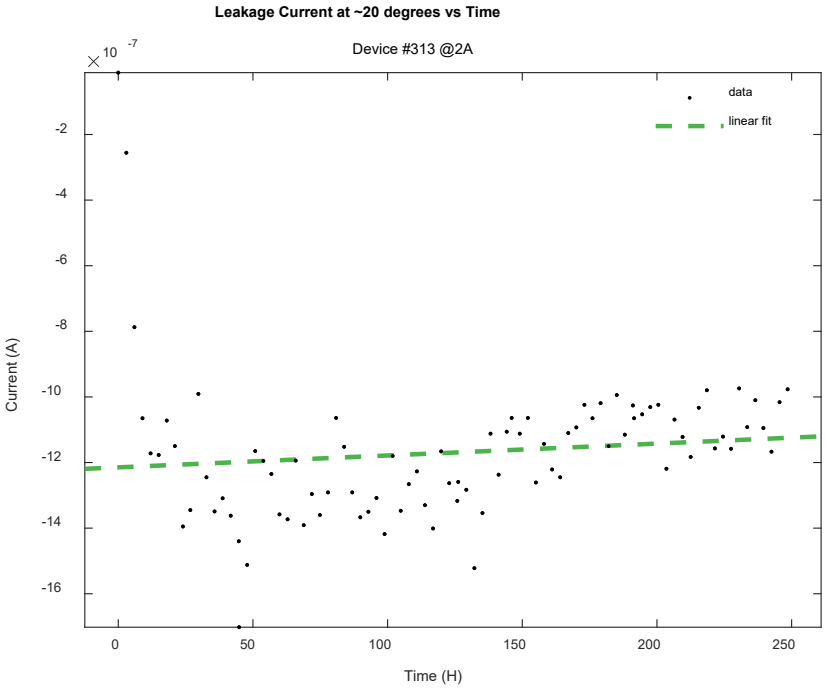

Figure 60. Leakage Current versus Time Device 313 Stressed at 2A

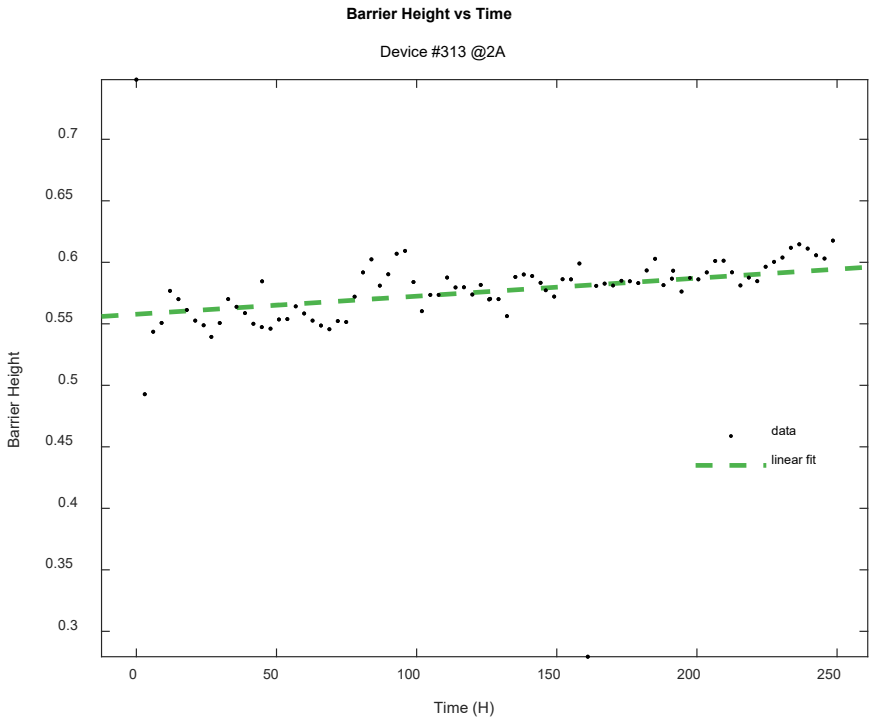

Figure 61. Barrier Height versus Time Device 313 Stressed at 2A

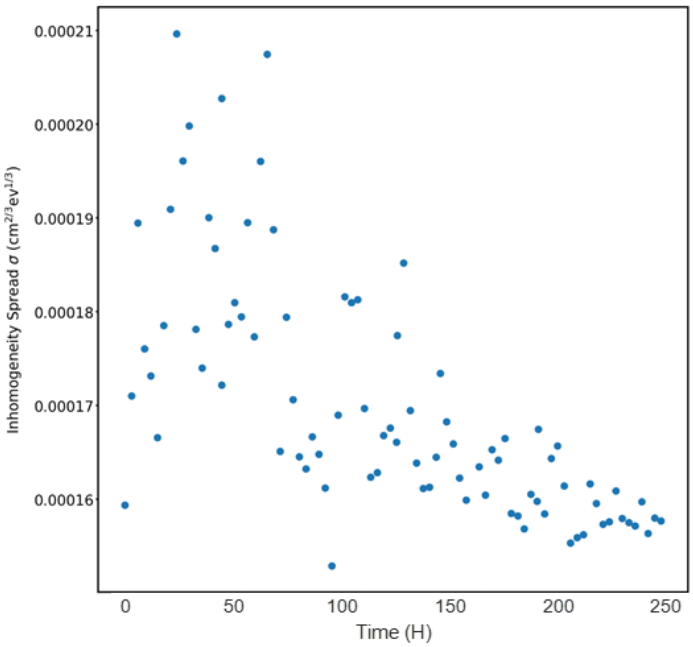

Figure 62. Inhomogeneity Spread versus Time Device 313 Stressed at 2A

4. Results of Long-Term Testing

After the long-term stress testing, all devices showed increases in BH over the stressing period which contradicts what occurred during the initial testing, where in most devices, the BH decreased. Also, of the 6 devices tested, only the two devices stressed at 2A did the leakage current decrease in the way that would be expected with an increased BH for both devices. At 1.5 A and 1.75 A, one of the devices showed an increase in BH. At 2A stress current, the average BH was unusually low when compared to the other devices which was the only indication of increasing degradation as stress current increased. BH change over all stress currents was relatively similar. Only at 2A of stress current did we see strong trends with the inhomogeneity spread, with both diodes showing decreasing spread over time.

Table 4. Results of Long-Term Testing

Device #	Strs Cur (A)	Diode	BH Avg (V)	BH Chng (V)	BH Chng %	LC Avg (µA)	LC Chng (µA)	LC Chng %
239	1.5	SD	0.701	0.022	3.2	-2.362	0.494	-18.9
314	1.5	SD	0.999	0.162	17.6	-0.089	-0.0166	20.5
115	1.75	DD	0.913	0.046	5.2	-0.222	0.0403	-16.7
206	1.75	SD	0.779	0.0334	4.4	-0.427	-0.0467	11.6
207	2	SD	0.585	0.169	3.4	-1.021	0.395	-32.4
313	2	SD	0.576	0.0364	6.5	-1.17	0.09	-7.4

Strs Cur: Stress Current, Avg: Average Value Over Testing, Chng: Change in value Over Testing, Chng %: Percentage Change of Value over Testing

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V. CONCLUSION

This section will draw conclusions from the research collected and make recommendations for future work of the HTOL system and Schottky diode testing at NPS.

A. CONCLUSIONS

The short-term stressing of devices showed strong evidence that extend high currents on the devices both reduced barrier height and increased leakage current as the devices degraded. Although the data on leakage current plots and BH plots behaved rather erratically, the trends showed that as stress time increased, the devices continued to degrade. The data from the short-term testing also indicated that as stress current increased, so did the level of degradation of the devices.

However, the long-term testing results did not match the conclusions that were drawn from the short-term testing. In all cases of long-term testing, the devices showed increased BH. The leakage current trends during long term testing were also inconclusive. Only at 2A stressing current did the change in leakage current match, where both devices showed decrease in leakage current, which is what would be expected with an increase in BH. In the other stressing conditions, specifically 1.5 A and 1.75 A of stress current, the devices contradicted each other with one device decreasing leakage current and the other device increasing leakage current. Due to this, no concrete conclusions can be drawn from the long-term testing.

The cause of this erratic behavior during long term testing may be due to the requirement to restart the system each day in order to get the system to run for the extended amount of time. During the short-term testing, the system ran autonomously from start to finish. In cases where the system timed out due to connectivity, that data was thrown out and the test was restarted with new devices. With the current system, there was no way to get a complete two-week stress period, so stressing periods were conducted daily and the data was combined at the end. This is likely the cause of the disagreement from the short term to the long term.

Unfortunately, because inhomogeneity spread could not be plotted for all the tests run, it is difficult to draw conclusions from it. Of all the tests that plots were able to be gathered from, the only ones that showed any sort of trend were the ones that took place at 2A, the highest stress current used. From this, it seems that past this stress current, further degradation would be seen.

B. FUTURE WORK

The most immediate future work for this research would be to correct the connectivity issue that the system is experiencing, so that long term tests can be conducted autonomously. A lot of time was wasted in the beginning of this research restarting 72-hour tests that had failed in the middle of stressing. It is also believed that this would improve the level of data that was collected for longer test periods, such as the two-week stressing periods attempted in this research.

The next step would be to improve and build more HTOL modules for the system. The current system is built to test four devices at a time, but due to the system struggling to maintain proper temperature, only two devices were stressed at a time. With better temperature control in the testing chamber, an increased number of devices could be stressed at once. On that same idea, with more HTOL modules built, the number of devices that can be tested at once increased drastically. Lots of data from devices will be the key to drawing conclusions on the failure mechanisms of these specific devices.

Finally, as mentioned above, much more data is required to truly understand the degradation process of these devices. Unpackaging of the devices pre and post stressing would further provide indicators of what is going on inside the devices. Stressing many more devices at varying lengths of time and stress currents will continue to fill out the picture of what is causing them to degrade. More study needs to be done on Tung's current equations. There were tests that demonstrated changes in inhomogeneity, but without further testing, no conclusions could be made.

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