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Development of an RF-Link for Secondary-Side Control of Power Conversion Systems

by C Wesley Tipton IV and Donald H Porschet

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DEVCOM Army Research Laboratory

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14. ABSTRACT
In this note, we describe the development of an RF-based data link used to transfer power regulation information in a wireless power transfer system. This approach has been taken to reduce the weight of the secondary-side converter. A 434 MHz, frequency-shift keying transceiver is employed to relay control feedback information at a rate of 31.25 kbps.

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power conversion, secondary-side control, wireless power transfer, data link, battery charging

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1. Introduction

Power conversion systems are usually tightly coupled in that current and/or voltage feedback signals are connected directly to the control electronics. In applications requiring galvanic isolation, direct connection is not allowed and there is an option of having primary-side control (PSC) or secondary-side control (SSC).[1] When using PSC, the value of the converter's output is inferred from the value of a primary-side parameter. Of course, the relationship between the output value and parameter value must be known and fixed. In SSC, the output value is measured on the secondary side and that value is transmitted to the controller. Inductive, capacitive, and/or optical devices are often placed in the feedback path to achieve isolation. In applications where there are physical barriers, such as implantable medical devices, it is possible to use same path of electro-magnetic energy transfer to power and provide feedback to regulate that power.[2]

In this note, we describe the design and implementation of an RF-based data link used to transfer control information in an SSC system with the goal of reducing the mass of the secondary-side power conversion system. We will not present the operational theory or performance of the link in this note.

2. System Description

Consider the wireless power transfer system of Fig. 1 where there exists a fixed charging station and a mobile, perhaps autonomous, vehicle. Furthermore, because of operational requirements, these systems may be loosely coupled both physically and electrically during charging. It is desired to charge the battery source of the mobile platform using power transmitted by the fixed platform. Electrical power is to be transferred through an air-core transformer whereas control feedback information is transferred through an independent RF data link. Minimizing the weight of the mobile system is of prime importance. In this, like other battery-charging applications, we require two feedback variables: battery voltage and charging current. Given that 8-bit resolution is sufficient, and assuming additional bits for start, stop, and error-checking information, we can estimate a message length of 24 bits. Because the load changes relatively slowly, we expect that a control loop update rate of 1 kHz is adequate and, therefore, a data rate of at least 24 kbps is needed. This rate may be surpassed by all modern communications equipment and protocols; however, few (if any) of these have the low latency required by real-time control applications.

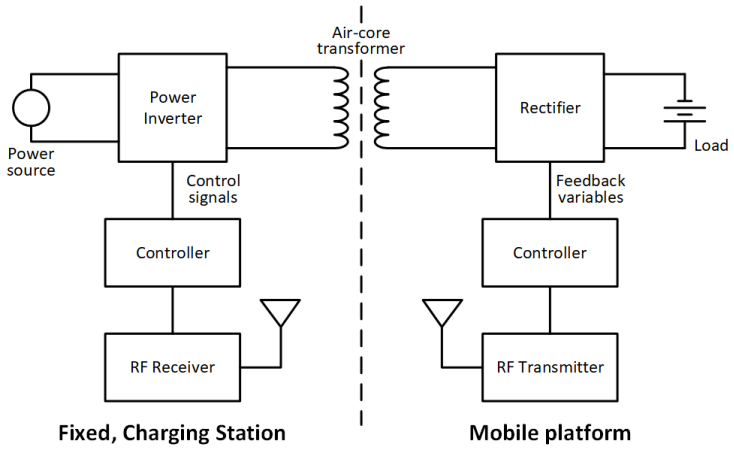

Fig. 1 Isolated, wireless power transfer system

2.1 RF-Link Transmitter

A simplified block diagram of the RF-link transmitter is shown in Fig. 2 and its electrical schematic is given in Appendix A. There are two analog (0 to 3 V) channels and two digital channels. The analog channels provide voltage and current feedback information whereas the digital signals may be used to convey status or other command information.

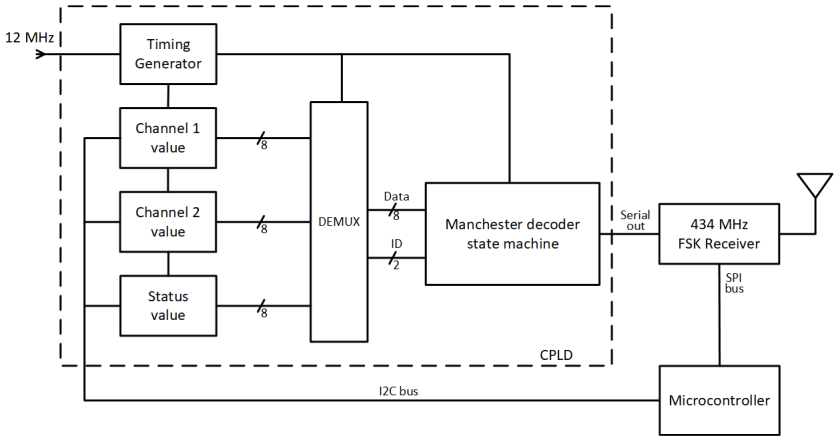

Fig. 2 Simplified diagram of RF-link transmitter

The analog signals are fed to a pair of AD7741, voltage-to-frequency converters by Analog Devices. The AD7741 is clocked at 6 MHz ($f_{v\text{-}f}$) and its output contains a fixed-width pulse at a frequency modulated by the analog input. At the full-scale input voltage, the output frequency is $0.45f_{v\text{-}f}$ and at zero-scale, the output frequency is $0.05f_{v\text{-}f}$. The waveform frequency is converted to its binary representation by a gated counter. Given that an 8-bit value is desired, the maximum

count ($count_{max}$) of 255 can be achieved at the highest frequency by applying a gate with duration of

$$t_{gate} = \frac{0.45 f_{v-f}}{count_{max}}. \quad (1)$$

At the selected gating time of 92 μs, the full-scale count will be 248 and the corresponding zero-scale count will be 28.

The two analog counter values and the two digital inputs (now expanded to an 8-bit status byte) are fed to a multiplexer, which scans these three input values and outputs one of them, with a corresponding 2-bit identifier, to the encoder. The Channel 1 and Channel 2 count values are alternatingly sent to the encoder to maximize the update rate of these feedback variables. Being of lower priority, the status byte is only sent if the status value has changed since the last byte sequence or after every eighth byte of analog count.

The encoder uses the data byte and byte identifier to form the data frame to be transmitted. In this design, the Manchester encoding scheme is used. As shown in Fig. 3, the encoded signal is simply the exclusive-OR of the data value and the 31.25 kHz, bit transmission clock. This method, therefore, encodes the binary value of logic 1 as a falling-edge and logic 0 as a rising-edge and allows for asynchronous transmission at a fixed data rate. All of the digital encoding logic is implemented through the very high-speed integrated circuit (VHSIC) hardware description language (VHDL) and implemented in an Intel, EPM570-series complex programmable-logic device (CPLD) using Intel's Quartus Prime development software.

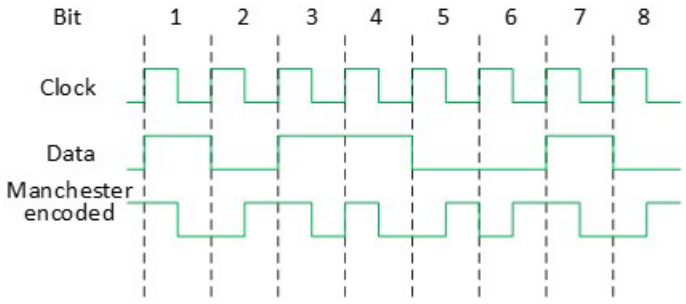

Fig. 3 Manchester encoding waveforms

The data frame format for the link is shown in Fig. 4. Each frame consists of 1 start bit, 2 identifier bits, 8 data bits (and up to 2 stuffing bits), 1 parity bit, and 4 stop bits. Stuffing bits are needed to prevent data bits from being interpreted as stop bits by the receiver. In our transmission scheme, 4 stop bits are used. Therefore, no more than 3 consecutive 1's are allowed in the data frame. The encoder tracks the

data stream and inserts (or stuffs) a "0" after the occurrence of 3 consecutive 1's. Even parity is calculated by performing an exclusive-OR over the identifier and data bits. Once the frame is formed, it is converted into a serial stream and fed to the RF transmitter.

Fig. 4 Manchester encoded data frame

The frequency-shift keying (FSK) transmitter is based on the MAX7060, 280 MHz to 450 MHz programmable transmitter by Maxim-Analog Devices.

The component values selected for the MAX7060 were based on FSK operation at carrier frequency of 433.9 MHz, shift frequencies of ±50 kHz, and data transmission rate of 31.25 kbps. Both the MAX7060 data sheet[3] and related application note[4] provide useful information on component selection. The carrier frequency of 433.9 MHz was chosen to lie within the European industrial, scientific, and medical band. This frequency is also within the U.S. 70-cm amateur radio band and, at transmission powers less than 1 W, is available for radio control applications. The MAX7060 has a maximum power rating of 25 mW.

The power amplifier (PA) output impedance matching and filter networks were designed based on the discussions presented in the application note and using online design tools. A simulation model of these circuits is shown in Fig. 5. The 3rd-order, Chebyshev low-pass filter (C22, C23 and L2 in Appendix A) was designed for a corner frequency of approximately 480 MHz and component values were estimated using the online LC Filter Tool.[5]

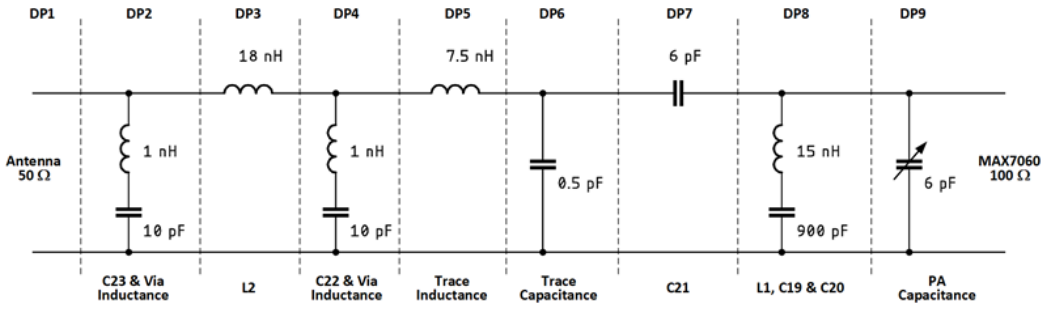

Fig. 5 Circuit model of the power amplifier filter and matching circuits

Where significant, printed circuit board (PCB) trace and via inductance/capacitance were included in the circuit model. Trace inductance was calculated using an online

calculator[6] and trace capacitance was estimated using a published[7] value of 1 pf/in. The value of via inductance associated with capacitors C22 and C23 was estimated using

$$L_{via} \approx 5.08h\left(\ln\left(\frac{2h}{r}\right)+1\right), \tag{2}$$

where L_{via} is via inductance (nH), h is height of the via (in), and r is the radius of the via (in).

The impedance matching network (L1 and C21) and the PA's tunable output capacitance are used to match the 50-Ω antenna to the 100-Ω PA output. Fig. 6 shows the constant-resistance/reactance Smith chart for the circuit of Fig. 5. The points on the chart labeled DB1, DB2, and so on, correspond to the circuit components. Using a Smith chart design tool[8] and starting at the antenna (DB1), the unknown component values are varied so that the end-point (DB9) resides on the 100-Ω constant-resistance circle (100 + i0 Ω). The output capacitance of the PA may be varied, through firmware, from 4.5 pF to 12.25 pF in 0.25 pF steps. To begin the graphical design process, the PA output capacitance was set to approximately mid-range (8 pF). Then, the value of C21 was iterated until the path between DP7 and DP8 intersected the point 100 + i0 Ω. Finally, a minimal, standard-value inductor was chosen for L1 such that the tuning of point DB9 was possible. With the values shown, the PA's load impedance is 101 – i0.8 Ω.

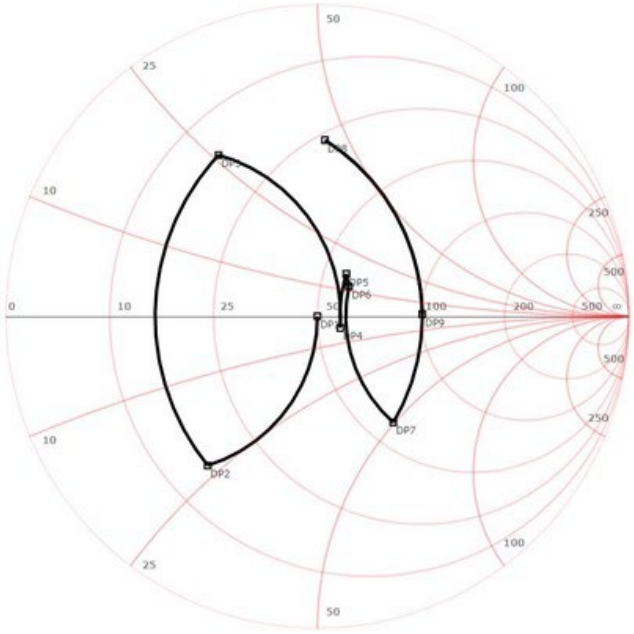

Fig. 6 Constant-resistance/reactance Smith chart of the filter and matching circuits

An uSP410, 433 MHz, surface-mounted, monopole antenna from Linx Technologies is used in both transmitter and receiver subsystems. Microstrip transmission line design was performed using an online calculator[9] to ensure a PA-to-antenna trace impedance of 50-Ω was maintained. A relative dielectric constant value of 4.0 for the PCB dielectric (FR4) and a trace height above ground plane of 0.015 inch were used to determine the desired trace width. The overall dimensions of the antenna ground plane are 1.5 inches by 3.3 inches, which was defined by the uSP410 data sheet[10] as an optimal size. The four-layer PCB design includes a solid ground plane covering the entirety of layer 2 (where layer 1 is the top layer) and power planes are provided on layers 3 and 4 to the greatest extent possible.

As previously mentioned, the operation of the MAX7060 is defined by external biasing components as well as programming internal registers through the SPI bus interface. Table 1 lists the register values used in this application.

Table 1 MAX7060 firmware configuration values

Register	Value	Register	Value
0x0	0x01	0x8	0x13
0x1	0x1F	0x9	0xB1
0x2	0x6A	0xA	0xF3
0x3	0xF8	0xB	0xB1
0x4	0x00	0xC	0xE6
0x5	0x02	0xD	0xB1
0x6	0x00	0xE	0xDA
0x7	0x00	0xF	0xFF

Note: Table values are hexadecimal.

The prototype transmitter is shown in Fig. 7. The right half of the circuit board contains the monopole antenna and required ground plane.

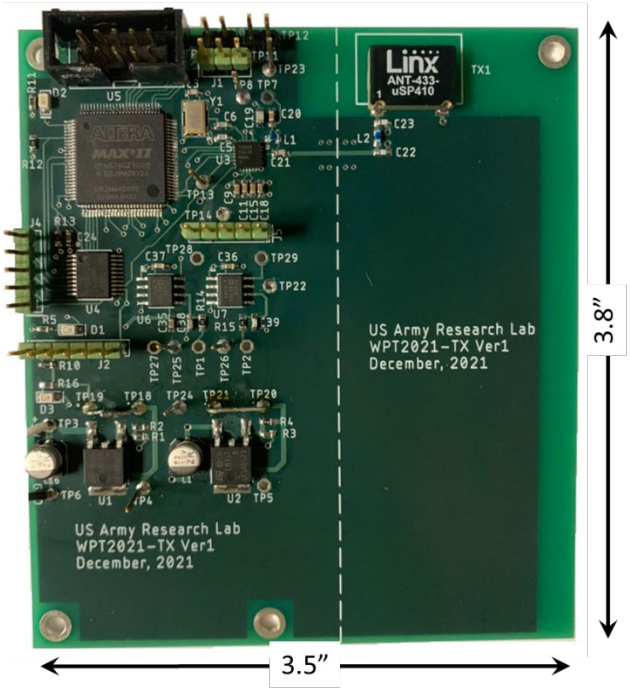

Fig. 7 RF-link transmitter assembly

2.2 RF-Link Receiver

A functional diagram of the receiver is given in Fig. 8 and its schematic is shown in Appendix B. The digital data stream from the FSK receiver is fed to the Manchester decoder, which is implemented as a state machine within the CPLD. The state machine includes logic to synchronize the receiver; detect and extract the identifier, data, and parity bits; and perform parity checking. A more detailed description of the state machine is given in Appendix C. Validated data bytes are stored in registers that may be read by the microcontroller through the Inter-Integrated Circuit (I2C) bus. In this case, the microcontroller also executes the power inverter’s control algorithm and would, therefore, have direct access to the feedback values.

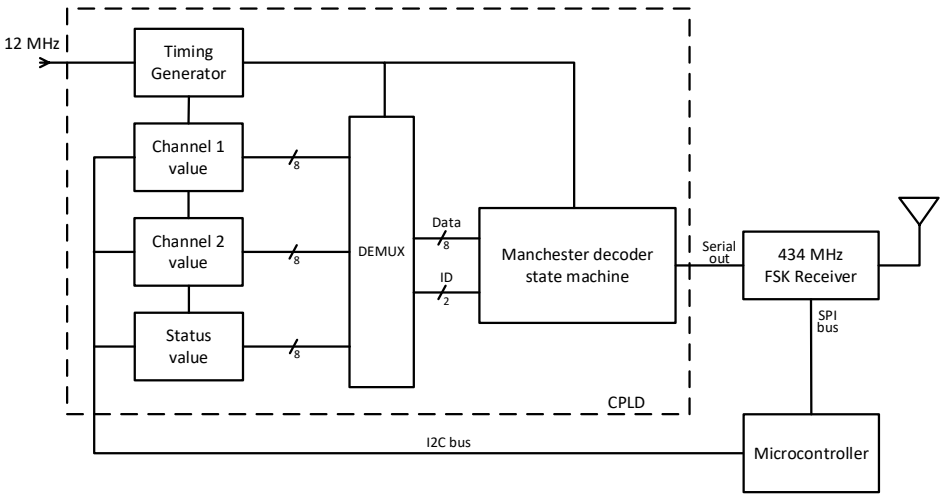

Fig. 8 Simplified block diagram of RF-link receiver

The FSK receiver is based on the Maxim Integrated MAX1471 super-heterodyne receiver integrated circuit. The MAX1471 theory of operation is given in its data sheet[11] and its configuration is straightforward. In this application, a 45-kHz corner frequency was used (1.5× bit rate) to design the low-pass Bessel data filter. And the data-slicer threshold was generated by the peak-detector circuits. Similar to the FSK transmitter, the MAX1471 is configured for operation by programming its internal registers and these register values are given in Table 2.

Table 2 MAX1471 firmware configuration values

Register	Value	Register	Value
0x0	0xB8	0x2	0x40
0x1	0x68	0x3	0x85

Notes: Registers not listed use default values. Table values are hexadecimal.

The most difficult aspect of the decoding process is data frame synchronization. Here, the position of the sampling point, within the bit window, must be established and the start bit must be detected. Figure 9 shows a typical data frame and an expanded view (bit window) of the first bit. A clock frequency of 16 times the bit rate of 31.25 kHz is used to sample the data stream. Due to the nature of the encoding scheme (Fig. 8), we expect that logic values should be stable at points one-quarter and three-quarters into the bit window. To detect the start bit, the received data stream is sampled every 2 μs until a logic transition is detected. At this point, the sampling circuit waits 4 clock cycles (8 μs or one-quarter of the bit window) before sampling the stream and saving the result in a 10-bit shift register. After this, the stream is sampled and saved every 16 μs and the contents of the shift register are compared to the binary value “1010101001,” which would be present

after 4 stop bits and 1 start bit. If this value is not detected within 32 clock pulses, the detection algorithm is restarted. Once the value is detected, the receiver has been synchronized and the remaining bits within the frame are extracted by sampling every 16 μs and assessing edge transitions. The decoder is re-synchronized at the beginning of every data frame.

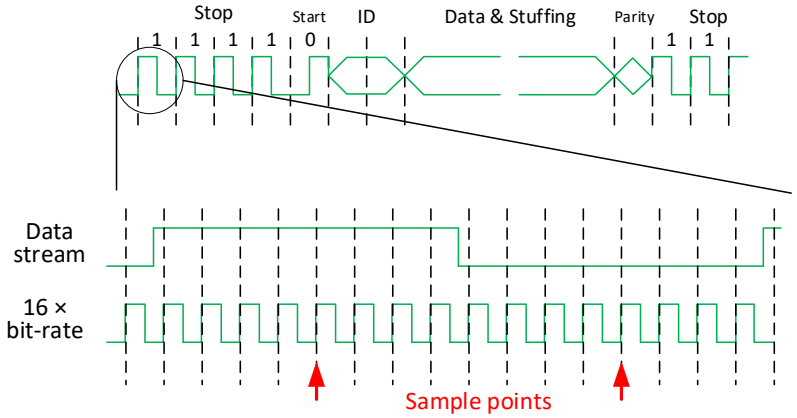

Fig. 9 Data frame synchronization and sampling

The prototype receiver is shown in Fig. 10. Again, the right half of the circuit board contains the monopole antenna and required ground plane.

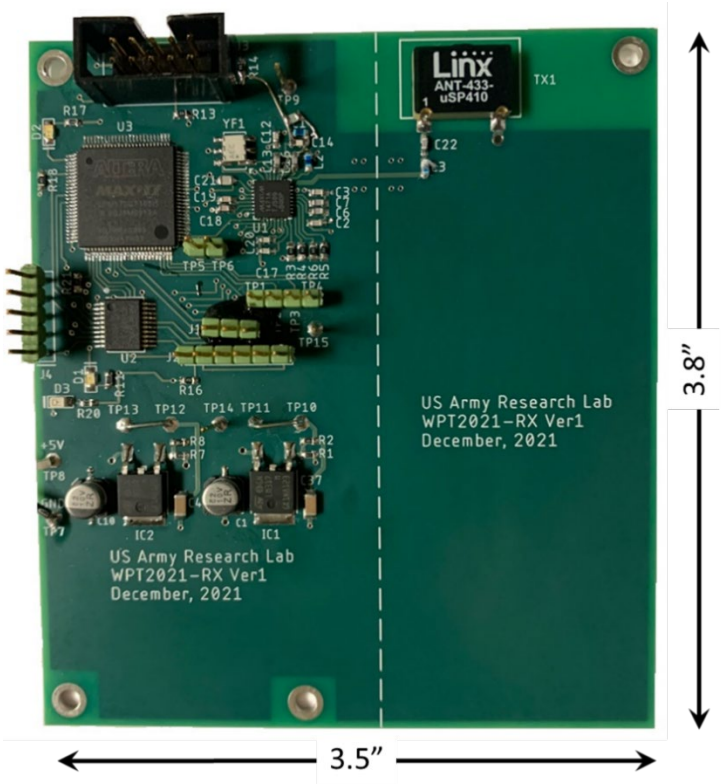

Fig. 10 RF-link receiver assembly

3. Summary

This note presents the development highlights of an RF data link for real-time control of a wireless battery charging system. Integrated, transmitter, and receiver circuits greatly simplified the design and the use of a variety of computer-aided analysis tools shortened the design cycle.

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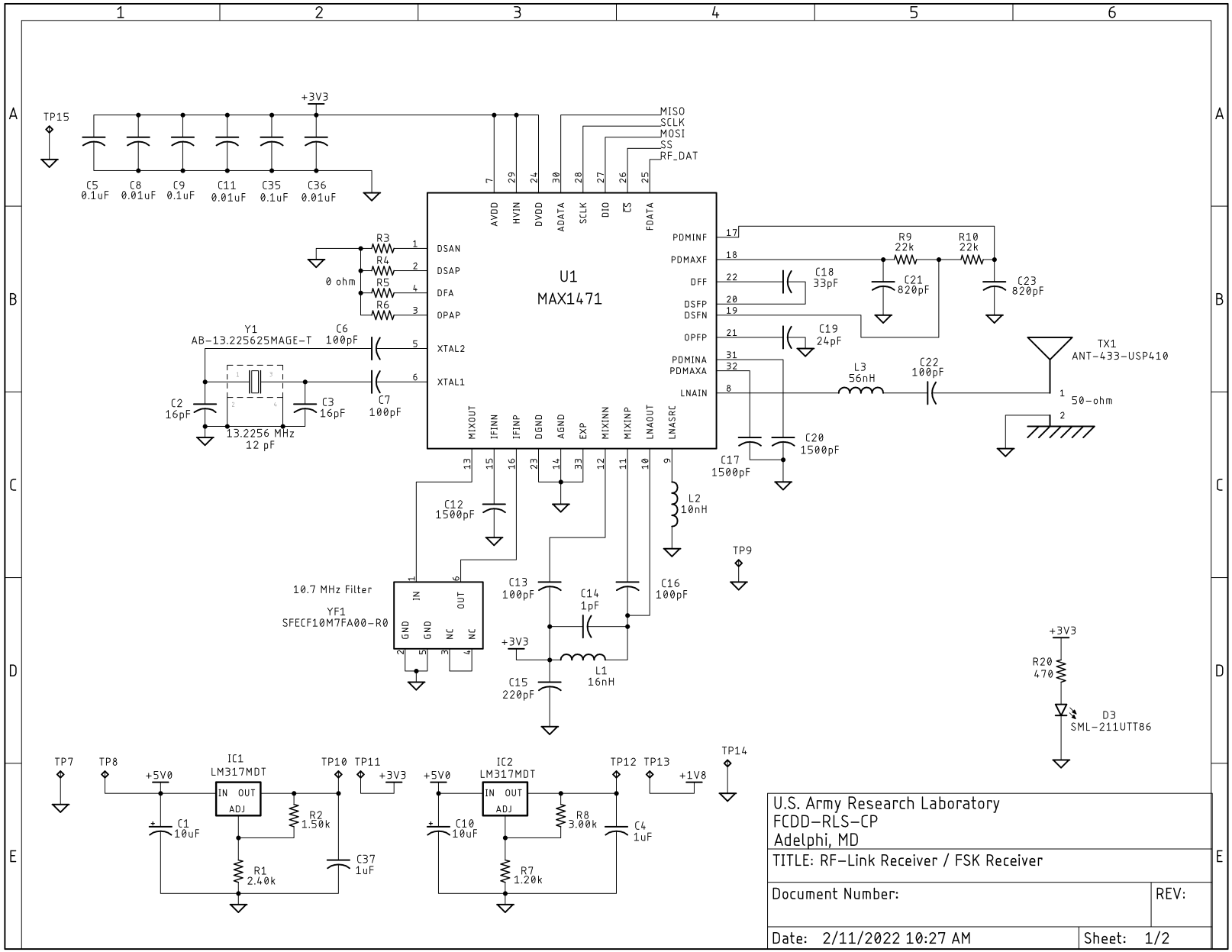
Appendix A. RF-Link Transmitter Schematic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3
4
5
6
A
B
C
D
E
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C7 100pF
C2 16pF
C3 16pF
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12 pF
PDMINF
PDMAXF
DFF
DSFP
DSFN
OPFP
PDMINA
PDMAXA
LNAIN
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R10 22k
C18 33pF
C21 820pF
C23 820pF
C19 24pF
C20 1500pF
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L2 10nH
TP9
10.7 MHz Filter
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C16 100pF
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TP11
+3V3
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R1 2.40k
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R7 1.20k
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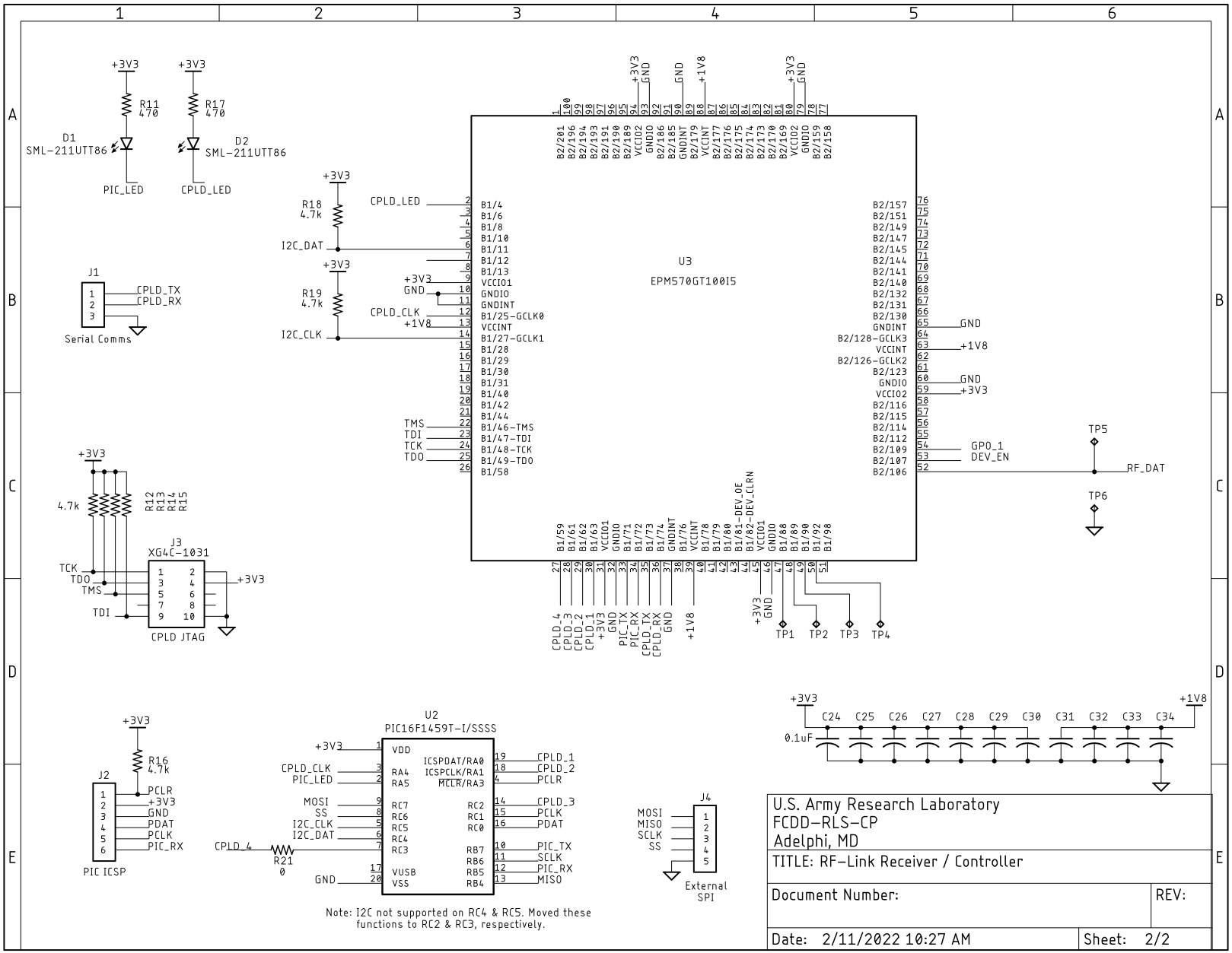
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J4
External SPI
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SML-211UTT86
D2
SML-211UTT86
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R17 470
R18 4.7k
R19 4.7k
R12 R13 R14 R15 4.7k
R16 4.7k
R21 0
TP1
TP2
TP3
TP4
TP5
TP6
RF_DAT
GPO_1
DEV_EN
C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34
0.1uF
Note: I2C not supported on RC4 & RC5. Moved these functions to RC2 & RC3, respectively.
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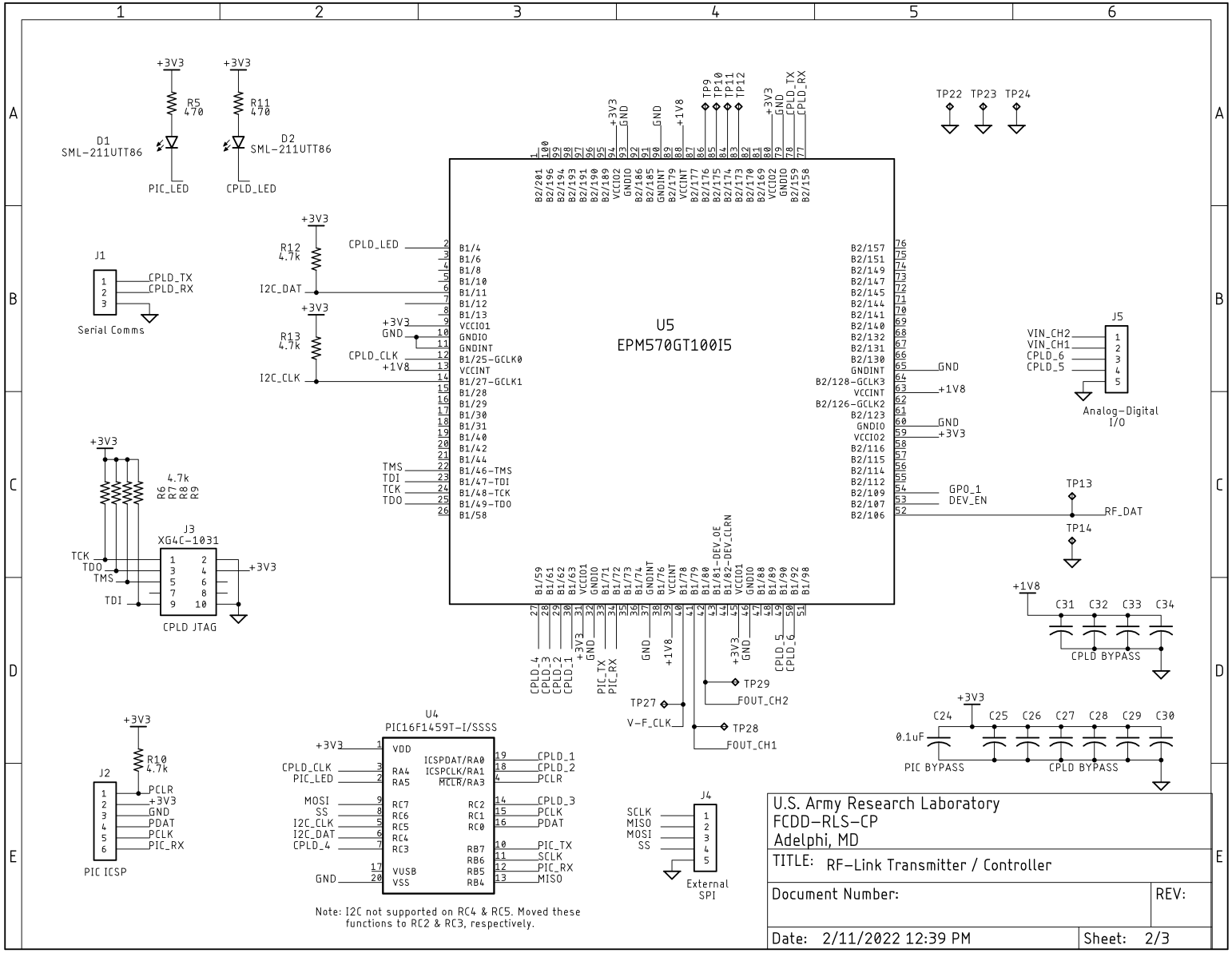
Appendix B. RF-Link Receiver Schematic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U5
EPM570GT100I5
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Note: I2C not supported on RC4 & RC5. Moved these functions to RC2 & RC3, respectively.
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CPLD JTAG
PIC ICSP
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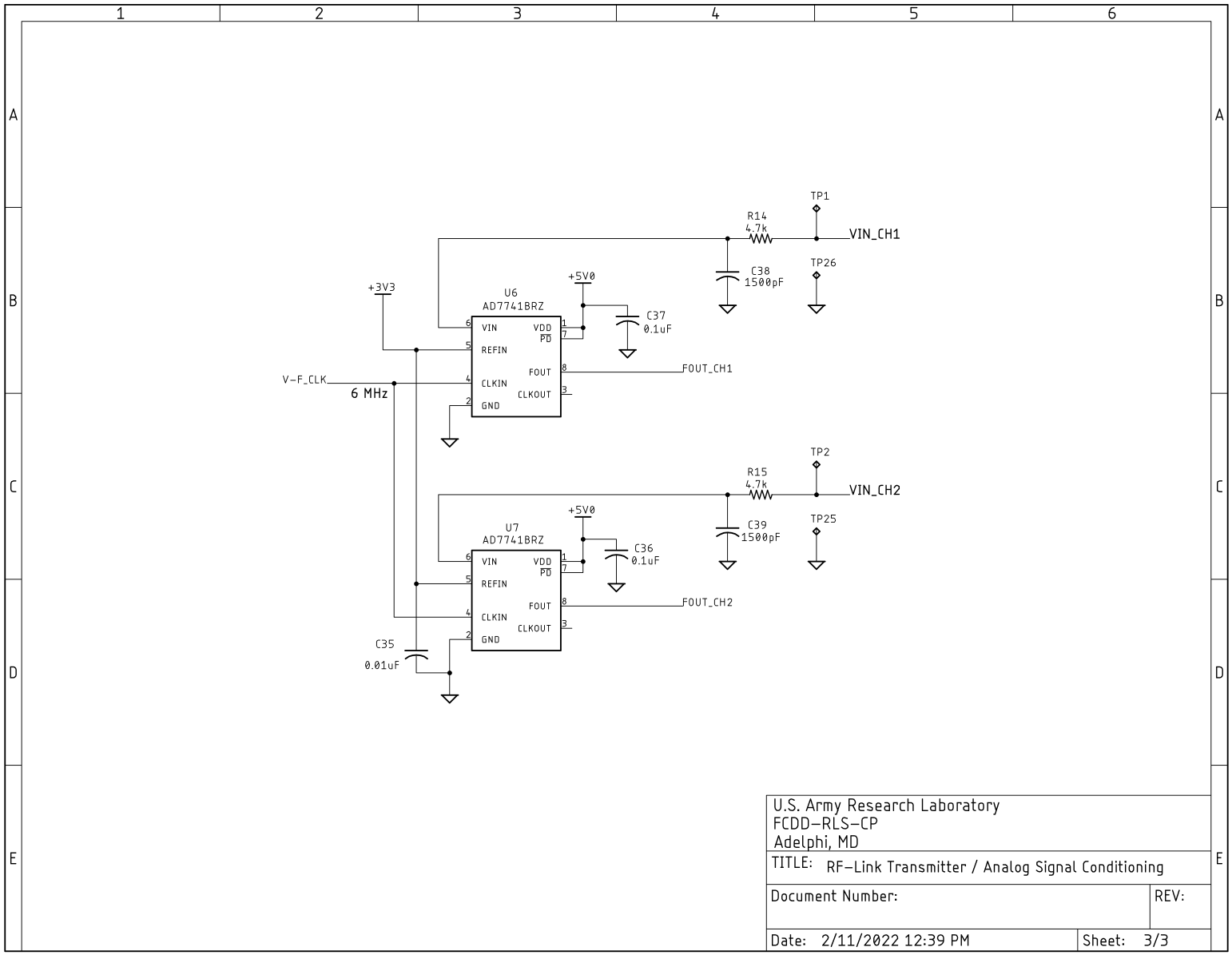
CPLD BYPASS
PIC BYPASS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TITLE: RF-Link Transmitter / Analog Signal Conditioning
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Appendix C. Manchester Decoder State Machine Description

Table C-1 Manchester decoder state machine description

State 0	• Initialize counters and values • After edge detected, goto State 1
State 1	• Sample data stream 8 μs after edge • Save this sample in the matching shift register • Goto State 2
State 2	• Sample and save data in matching register every 16 μs • If match to "1010101001" occurs, goto State 3 • If no match after 16 bits, goto State 0
State 3	• Sample and save data in matching register every 16 μs • Evaluate data edges to extract *identifier* bits • Begin parity calculation and bit-stuffing count • If edge is not detected within bit window, fault. Goto State 0 • Else, after identifier is extracted, goto State 4
State 4	• Sample and save data in matching register every 16 μs • Evaluate data edges to extract *data* bits • Continue parity calculation and bit-stuffing count • If three consecutive "1's" are extracted, skip the next bit as a "0" stuffing bit. • If edge is not detected within bit window, fault. Goto State 0 • Else, after data is extracted, goto State 5
State 5	• Sample and save data in matching register every 16 μs • Evaluate data edges to extract *parity* bit • Continue bit-stuffing count • If three consecutive "1's" extracted, skip the next bit as a "0" stuffing bit. • If edge is not detected within bit window, fault. Goto State 0 • Else, after parity is extracted, goto State 6
State 6	• Sample and save data in matching register every 16 μs • Compare the calculated and received parity values • If parity values agree, then store the data value into the register indicated by identifier bits • Goto State 0

List of Symbols, Abbreviations, and Acronyms

ARL	Army Research Laboratory
CPLD	complex programmable-logic device
DEVCOM	US Army Combat Capabilities Development Command
FSK	frequency-shift keying
I2C	inter-integrated circuit
PA	power amplifier
PCB	printed circuit board
PSC	primary-side control
RF	radio frequency
SPI	serial peripheral interface
SSC	secondary-side control
VHDL	VHSIC hardware description language
VHSIC	very high-speed integrated circuit

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