

CHAPTER 12. UNDERSTANDING INTERFACES FOR HOMOEPITAXIAL GAN GROWTH

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The recent availability of commercial bulk GaN substrates enables vertical GaN devices to become a reality through homoepitaxial growth. However, additional materials challenges need to be understood and surmounted to fully develop the technology. The first step to this is forming an understanding of the influences of the interface on growth and device performance. This chapter will examine the effects of surface preparation and initiation on growth morphology, impurity incorporation, interface composition, as well as how these issues affect device performance.

Keywords: GaN, homoepitaxy, epitaxy, interface, vertical, surface preparation, roughness, diodes

12.1. INTRODUCTION

GaN-based devices have become ubiquitous in daily life with the commercialization and widespread adoption of light emitting diodes (LEDs) [1,2,3]. In addition, they have been highly useful as electrical devices in rf and microwave applications in the form of high electron mobility transistors (HEMTs) [4,5]. As such, one may ask why research still continues in this successful material. The answer is that, though successful, the electrical devices are still not meeting the theoretical limits of the material. The best GaN-based HEMT device technology is still only attaining around a third of the theoretical estimated breakdown field ($> 3 \text{ MV/cm}$) [6].

The main culprits are two-fold: heteroepitaxial growth and lateral device geometry. Current commercial devices are grown on non-native substrates, mainly Si, SiC, and sapphire. None of these are lattice-matched or thermally matched with GaN, and require varying degrees of buffer layers and engineered strain in order to produce epitaxial layers. Si substrates have the additional issue of diffusion of Ga into the substrate without appropriate buffer layers, while sapphire substrates are highly insulating restricting their use to only lateral conducting devices. The two most direct consequences of the lattice and thermal mismatch are defectivity in the material, mainly in the form of dislocations, and major limitations on the thickness of the GaN layers. The critical thickness for cracking of a GaN film is generally around $5 \mu\text{m}$, but varies a bit with substrate material and buffer layers [7]. It generally trends lower ($\sim 2 \mu\text{m}$) when grown on Si substrates, even with multiple strain engineered buffer layers [8]. Dislocations are scattering sites in lateral devices for both electrons and phonons, which reduces mobility and decreases thermal conductivity [9-11]. A schematic of the most common lateral device, the high electron mobility transistor (HEMT) is shown in Figure 12.1a. In this geometry, the conduction path of lateral devices is very close to the surface, allowing surface states to impair the operation of the substrate. Additionally, extremely high fields are formed at the gate edge, requiring extensive thermal engineering efforts, which have been the subject of multiple large programs over the past decade [12,13].

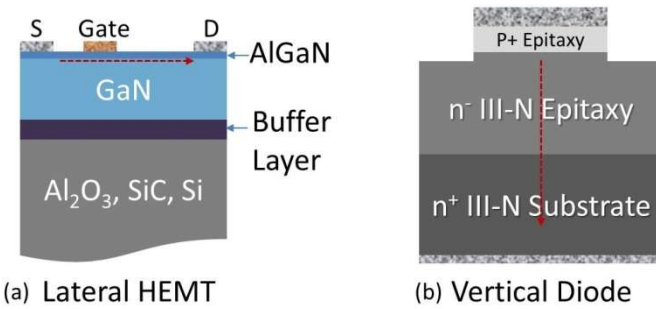


Figure 12.1. (a) Basic schematic for a GaN-based lateral HEMT for comparison with (b) a vertical p-n diode. The red dotted line denotes the electron conduction path through the device.

To alleviate this, and allow devices to reach the full potential of the material, a vertical device geometry grown on a thermally and lattice matched substrate with low dislocations is needed. Figure 12.1b shows a very simple schematic for a vertical diode. The advantage to this geometry is that conduction path flows vertically through both epi and substrate, meaning the characteristics are determined by the intrinsic bulk properties of the nitrides. Additionally, this geometry allows for a distributed field, meaning less thermal management and, with the use of native, lattice matched substrates, the ability to grow thick epitaxial layers. This is important, as thick layers with low impurity concentration are required to reach high breakdown fields, as shown in the plot of avalanche and punch-through breakdown of GaN Schottky diodes in Figure 12.2 [14]. Unlike SiC, Si, GaAs and other semiconductor workhorses, a native bulk substrate for GaN has been historically unavailable. Breakthroughs in hydride vapor phase epitaxy and ammonothermal growth techniques have enabled the recent development and commercialization of bulk GaN substrates [15-19]. However, the availability of native substrates does not automatically enable high quality homoepitaxial layers. Taking heteroepitaxial growth recipes and directly applying them to native substrates without forming an understanding of the GaN substrate interface surface and characteristics of the initial stages of growth does not necessarily lead to successful growth. The effects of the structural and chemical characteristics of the substrate/epitaxial interface on growth and device performance will be covered herein for GaN oriented in the +c (0001) direction by metal organic chemical vapor deposition (MOCVD).

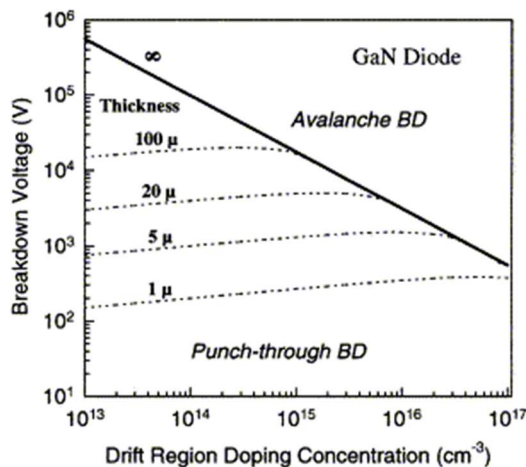


Figure 12.2. Calculated breakdown voltage as a function of doping concentration and thickness of the drift region in GaN n-n+ diodes. Reprinted from [14], Copyright (2000), with permission from Elsevier.

12.2. SURFACE INTERFACE STRUCTURE

In epitaxial growth, the structure of the starting substrate surface is extremely important. Although the surface can be changed slightly during the ramp to growth temperature and during initiation of the growth, many of the initial surface features are set by the substrate manufacturer's product specifications. These characteristics include wafer offcut, bow, and surface roughness. In addition to these standard specifications, there are additional challenges in uniformity of impurities with in the substrates that are starting be noticed [20]. The technology to produce bulk GaN substrates is not fully mature, and control over these characteristics is developing at the same time the manufacturers are scaling their technology to larger substrate diameters.

12.2.1. OFFCUT

The basic mechanism of single-crystal growth stems from atoms orderly attaching onto the crystal surface at an edge [21,22]. For epitaxial growth, a regular surface of steps is the preferred surface to start this. In heteroepitaxial growth, these steps are seeded by the spiral growth around dislocations (Figure 12.3a). For growth on a native substrate, where the starting substrate is crystalline and lattice matched, an alternative method to provide a stepped surface is possible. A periodic stepped surface can be produced by cutting and polishing the original crystal substrate at an angle to the basal plane (Figure 12.3b). Such substrates are referred to as offcut or mis-cut. The benefit is that by using a stepped surface, the growth conditions can be chosen such that the growth of the steps outpaces the growth at dislocations, producing a smooth film with each atomic layer forming as a 2D sheet, where the terrace width is determined by the offcut angle.

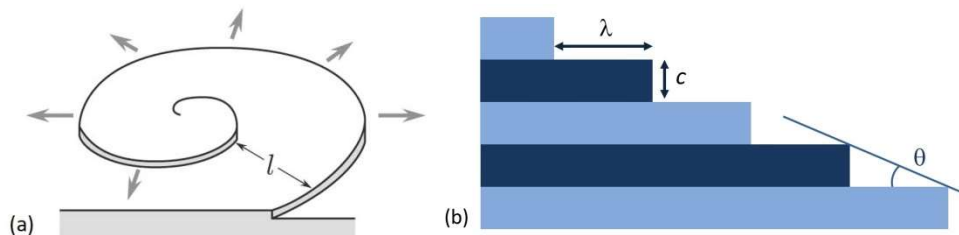


Figure 12.3. (a) Schematic of steps originating spirally from a dislocation, which is the source of growth steps in heteroepitaxy. Reprinted from [23], Copyright (2016), with permission from Elsevier. (b) Illustration of an offcut crystal, where the step width, λ , is set by the geometric relationship between step height, c (lattice constant), and offcut angle, θ .

The offcut angle has a direct impact on the morphology of epitaxial films. On vicinal substrates (0 degree offcut), screw dislocations will still dominate as step producers, resulting in a rough surface decorated by hillocks [24]. With HVPE GaN substrates containing $\sim 10^6$ dislocations/cm², this results in a very rough morphology. With increasing offcut (toward m), the growth morphology smooths, resulting in regularly stepped surfaces at 0.5-1 degree offcut angles [25-27]. At offcuts larger than 1 degree, although the epitaxial layers appear macroscopically smooth by optical microscopy, more detailed characterization show that the surfaces are stepped, but the steps are bunched [25,28]. This

step-bunching means that the regular bi-layer stacking of the surface is interrupted, with varying step heights. However, at these smaller offcut angles, step meandering is sometimes observed in the epitaxial films. In homoepitaxial GaN growth by HVPE, Fujikura and Konno showed that step meandering at offcuts under a degree could be reduced at low V/III ratios or high growth temperatures (Figure 12.4) [29].

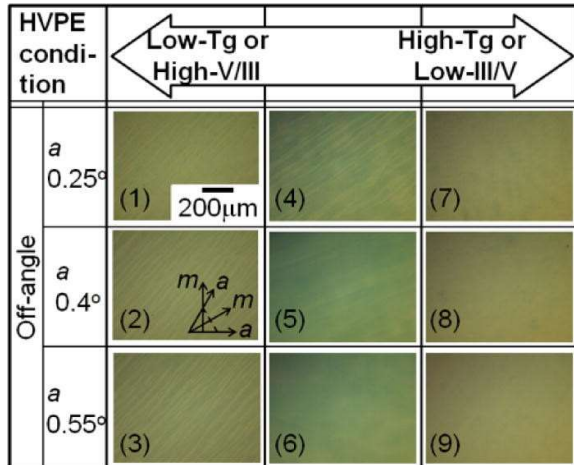


Figure 12.4. Growth parameter dependence of step meandering in HVPE homoepitaxial growth of 20-30 μm on substrates with different offcuts. Reprinted from [29], with the permission of AIP Publishing.

The offcut not only affects homoepitaxy morphology, but it can also influence incorporation rates of different species in the films. The most straight-forward effect is on InGaN composition. Increasing the offcut reduces the incorporation of indium into the films [25,30]. The effect on AlGaIn composition seems negligible [31,32], however it has been reported that increasing the offcut decreases crack generation in AlGaIn films on GaN [25]. Additionally, screw dislocation density in the AlGaIn films is independent of offcut, but edge dislocation density decreases at offcuts greater than 1.4 degrees [31]. As far as n-type dopants, no real change is seen in silicon or oxygen incorporation with changing offcut [33,34]. However, magnesium (Mg) incorporation has a few conflicting reports. Several reports show no increase in Mg concentration in the films which changing offcut, however, at the same time, they show an increase in hole concentration and reduced resistivity with increased offcut angle [35,33]. Suski et al. report this increase in p-type carrier concentration to be due to decreasing compensating donors in the films [33], while Jiang et al. attributes it to higher carbon incorporation in the p-GaN, observed in SIMS. Grenko et al. report an opposite effect on Mg incorporation, showing a reduction in Mg concentration with increasing offcut, using PL, CL, and SIMS to study their films. However, the samples also had an undoped GaN layer grown on top of the p-GaN layers, and SIMS showed Mg migrated to the p-GaN/undoped GaN interface. This effect was more pronounced with increased offcut angles [31]. Revisiting the effect of offcut on carbon incorporation, although Jiang et al. saw a significant effect of offcut on carbon concentration in p-GaN layers, the effect on n-GaN layers was much smaller, reducing from 7×10^{16} to $5 \times 10^{16} \text{ cm}^{-3}$ when decreasing the offcut by 0.4 degrees [35]. The C suppression with increased offcut was attributed to reduced step motion velocity. This may mean that the C incorporation is highly dependent on growth parameters, as another report finds the opposite relationship on unintentionally doped films, namely an increase in C with

increasing offcut. In this case, the increased carbon is attributed to an increasing number of steps, and a lower energy barrier for C to incorporate at steps than elsewhere on the surface [34].

12.2.2 WAFER BOW

Offcut is not the only consideration for surface preparation, especially for bulk GaN substrates grown by HVPE. A majority of the commercially available GaN substrates use this method to grow thick layers on non-native substrates, sometimes patterned, use dislocation gettering techniques to reduce the defects, then separate the GaN layers from the non-native seed. Since growing on a non-native substrate, some lattice or thermal mismatch exists, and when growing thick layers (>400 μm), lead the wafers to bow [36,37]. In order to produce flat substrates, these layers must be polished. However, with the original bow, this can result in variations in step density across the wafer surface, all of which is illustrated in Figure 12.5. This, in turn, affects the uniformity of the homoepitaxy grown on such surfaces in roughness and, potentially, impurity incorporation.

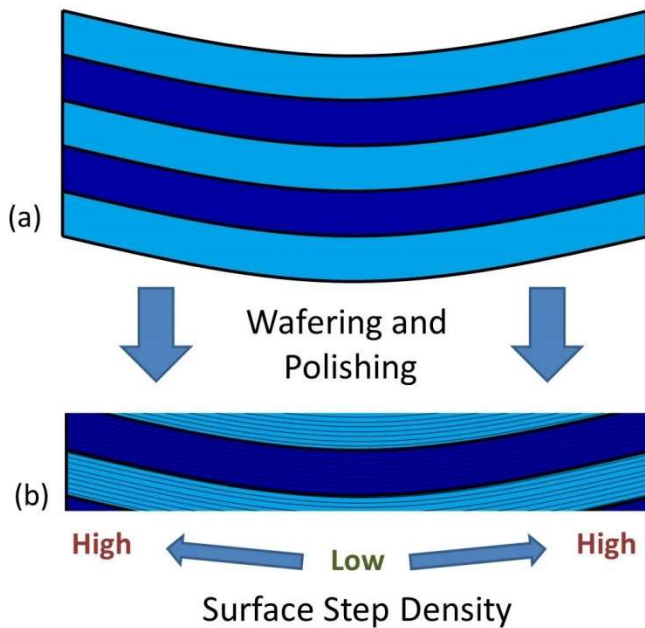


Figure 12.5. Schematic illustrating the effect of wafering and polishing a bowed wafer on step density. The bowed wafer (a) shows curvature over the entire lattice in the case of compressive stress at the wafer surface. A view of it after wafering and polishing is shown in (b), with additional lattice lines drawn to make the change in step density more apparent. This case results in many more steps on the wafer edge than in the center.

12.2.3 SURFACE POLISH AND MORPHOLOGY

Most commercial substrates come with root mean square (RMS) roughness specifications that are on the Angstrom scale. AFM scans of these substrates generally show regular, stepped surfaces, as required for step-flow growth. However, each manufacturer uses a different, normally proprietary, recipe, and the results are not always equivalent. On a small scale ($10 \times 10 \mu\text{m}^2$), the surface appears smooth and regularly stepped, as required by the specifications. An example of this is shown in Figure 12.6. However, the macro-scale roughness also needs to be taken into consideration, especially for

large devices. At scan lengths of hundreds of microns, these surface differences between wafers and vendors is quite dramatic, examples of which are shown in Figure 12.7 [20]. The best way to characterize the incoming GaN substrates is not just on a small, micro-scale, but also using large scale, rapid techniques like optical profilometry, Raman mapping, and PL mapping in order to see these differences, as well as some startling impurity uniformity issues within the wafers [20]. The reason the macro scale is also important, is that the epitaxy conforms to the surface, and increasingly magnifies these features with increasing thickness [34]. For vertical devices, where the homoepitaxial layers will need to be 100 μm thick, this will result in very rough surfaces.

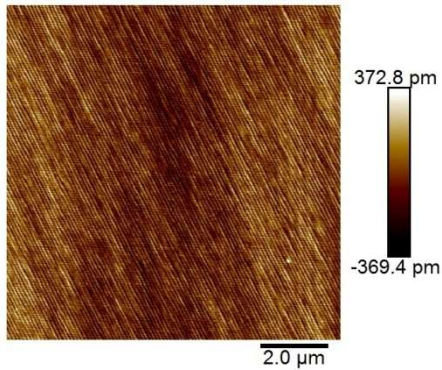


Figure 12.6. A representative example of a small-scale AFM scan ($10 \times 10 \mu\text{m}^2$) of an incoming substrate.

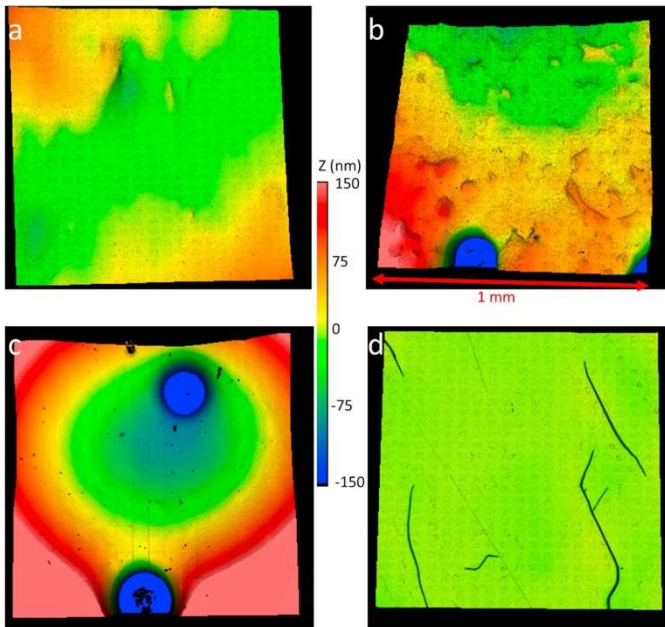


Figure 12.7. Examples of larger scale optical profilometry scans ($1 \times 1 \text{mm}^2$) of several substrates, using the same height scale. The difference in roughness is considerable on these scales, with large features present in (b), but a relatively smooth surface on (a). The substrate in (c) shows large wafer bow, and (d) is perfectly flat, despite cracking that occurred during dicing. Reprinted from [20], Copyright (2018), with permission from Elsevier.

12.3 CHEMICAL INTERFACES

Homoepitaxial growth by MOCVD has several advantages over molecular beam epitaxy: higher growth rate, reasonable vacuum levels, and large-scale commercialization. For cleaning the interface, it is especially advantageous, as ramping the substrates to temperature is done under an ammonia atmosphere with some hydrogen and/or nitrogen as the carrier gases. Not only does this keep the GaN substrates from decomposing, but it also serves to remove C and O from those surfaces without additional ex situ steps. Until recently, most MOCVD growers believed that was the end of the story: the MOCVD homoepitaxial interface is generally clean of C and O, as seen in the bottom two plots of Figure 12.8. However, with homoepitaxial growth and regrowth of p-n junctions, a small snag has come to the attention of the community. This is in the form of a spike of Si at the growth (or regrowth) interface, and is illustrated in Figure 12.8 [31,34,38,39]. This ubiquitous spike reaches very high levels on growth on bulk substrates, but is also seen on GaN templates on sapphire. The source of the Si is still under consideration. Several sources have been debated, including impurities left behind from the polishing process, coatings on the wafer carrier, Si from inside the reactor, excess Si left during decomposition of the substrate during ramping conditions, and something mysterious coming from the atmosphere. Experiments from Hite et al. and Pickrell et al. suggest that it is an atmospheric effect [38,39]. These have shown the only time a major spike is observed is when the interface is exposed to atmosphere – not during ramp, not during growth interrupts held at high temperature, and not when kept under vacuum. This is shown in Figure 12.9 [38]. The Si spike observed in samples that are exposed to atmosphere do also have dependence on the Si concentration in the original substrate. Figure 12.10 shows this, where GaN templates grown on sapphire with higher levels of n-type doping do have a larger spike at the interface than the unintentionally doped films when exposed to atmosphere prior to regrowth. However, the largest change in Si incorporation is for the unintentionally doped sample.

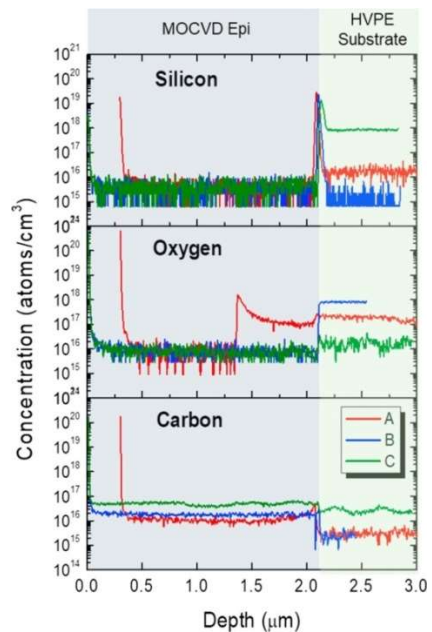


Figure 12.8. SIMS data showing MOCVD regrowth on three different bulk GaN HVPE substrates in a single run. Although the interface between the substrate and MOCVD homoepitaxy is rather clean, a spike in Si at that interface reaches levels of 10^{19} atoms/cm³ before falling back down to unintentionally doped levels. Reprinted from [34], Copyright (2018), with permission from Elsevier.

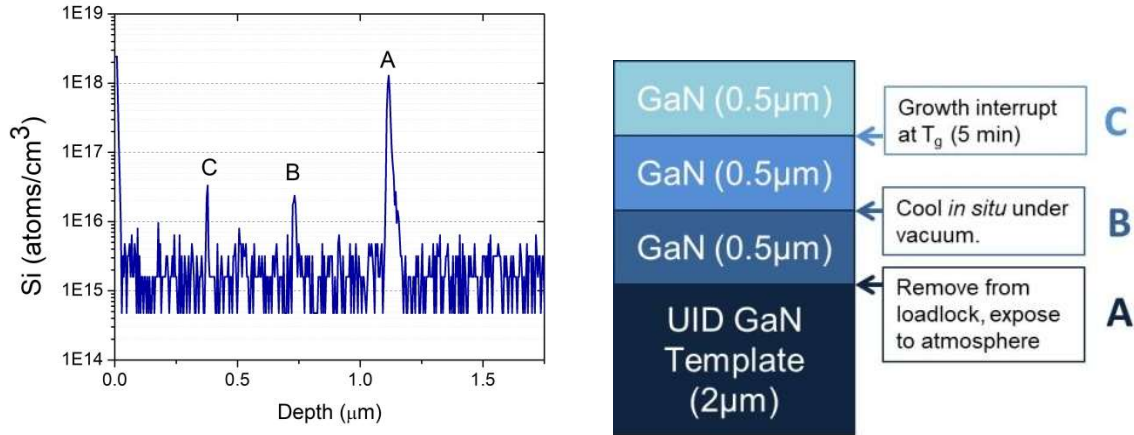


Figure 12.9. (a) SIMS data and (b) structure schematic illustrating Si incorporation at the regrowth interface of a GaN surface (A) exposed to atmosphere, (B) cooled and regrown under vacuum, and (C) 5 minute growth interrupt held at growth temperature. © IOP Publishing. Reproduced with permission [38]. All rights reserved.

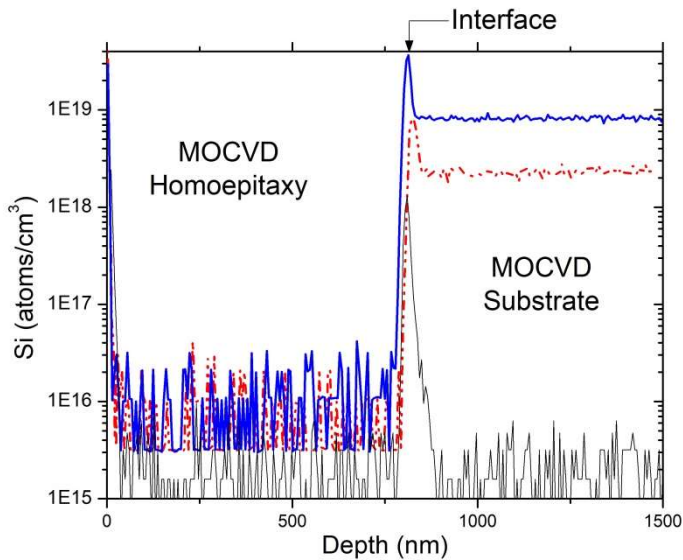


Figure 12.10. SIMS data showing the homoepitaxial growth interface on three substrates with different doping levels: undoped (gray), 2×10^{18} cm⁻³ (dotted red), and 8×10^{18} cm⁻³ (thick blue). The largest spike, in relation to the levels in the substrate, is found in the undoped sample.

12.4. EFFECTS ON DEVICE PERFORMANCE

In the previous sections the effects of the surface and interface were discussed in regards to growth morphology, species incorporation, and interfacial layers. All of these have effects on the performance of devices fabricated from such homoepitaxial films.

12.4.1. SURFACE MORPHOLOGY EFFECTS

The impact of surface morphology is a first order issue. Immediately, it can be observed that changes in offcut and step density from wafer bow and polish cause uniformity issues across wafer surfaces. The electrical effect, as observed in Schottky diodes, is found in areas of large-scale roughness at the wafer surface. For devices fabricated in regions where the RMS roughness over a 200 x 200 um is over 50 nm, an increased leakage current and decreased breakdown field is observed [40]. Smoother regions of the same wafer showed higher breakdown fields, with simple structures lacking field management reaching critical breakdown fields of 1.4 MV/cm. In p-n diodes on homoepitaxial growth, a non-optimal offcut produces rough surfaces, which also show high leakage and fail high-temperature reverse-bias (HTRB) reliability stress tests [41]. This direct impact of roughness on reverse leakage current is plotted in Figure 12.11. This report predicted an even more stringent cut-off for surface roughness, 25 nm, measured on long length scales. As such, the results indicate that surface roughness can be employed as a metric to screen epitaxial layers, where substantial variation on offcut angle across the substrate acts as a potential limitation to epitaxial layer uniformity and repeatability.

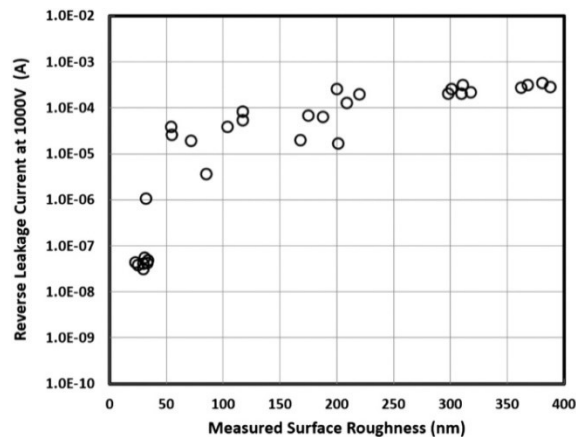


Figure 12.11. Plot of leakage current vs. surface roughness. Reprinted from [41], Copyright (2015), with permission from Elsevier.

12.4.2. CHEMICAL INTERFACE EFFECTS

For vertical devices, an n+ substrate is normally required; therefore the conduction caused by a Si spike at the initial growth of a drift layer on the bulk substrate is not an important issue. However, this is an issue for lateral devices on semi-insulating bulk substrates as well as any p-type regrowth required in more advanced vertical devices. It has been shown that a lateral HEMT on a regrown buffer has increased off-state leakage due to the presence of Si at the interface when compared to a non-regrown structure [38]. In regrown p-GaN layers forming a p-i-n diode, the Si interfacial layer

causes the device to act like a Zener tunnel diode, with temperature independent leakage current [39].

12.5. CONCLUSION

Understanding the growth surface preparation and interface is extremely important in developing homoepitaxial growth of GaN for vertical devices where thick films, regrowth, and high purity layers are required. Preparing the surface morphology is the first step. For smooth growth, regular steps, controlled across the surface, are provided by a slight offcut of the native substrate crystal. If the offcut is too low, hillocks form. If it is too high, step bunching can occur. For GaN, optimal offcuts have been reported between 0.5 to 1 degree, but this can vary with growth conditions. Rough morphology can occur due to variations in offcut due to substrate bow and defects in wafer polishing. This roughness has a direct impact on vertical diodes, reducing the breakdown voltage and increasing leakage current. Additionally, surface cleaning and growth initiation must be taken into consideration, especially on for regrowth on low-doped layers, as a Si interfacial layer appears at all regrowth interfaces after exposure to atmosphere. This still needs to be understood and solved. This layer can also cause increased leakage current in p-n diodes. However, even with these considerations, high voltage vertical devices are already being demonstrated, which are coming closer to the theoretical breakdown field of GaN than lateral devices.

Acknowledgements

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