Performance Report

Title of Proposal: Condition-Based Maintenance Algorithms for Power Converters using Wide-bandgap Devices

Period of Performance: October 1st, 2018 — May 15th, 2021

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1 Program Objective

The objective of this project is to predict failures and remaining useful life in power electronic building blocks (PEBBs) comprising Silicon Carbide (SiC) devices. The condition-based maintenance algorithms will be demonstrated on a DC/DC High Frequency Transformer made using 1.7 kV SiC devices. The project will be in collaboration with Dr. John S. Donnal, who has pioneered non-intrusive load monitoring technology, from the United States Naval Academy (USNA). The effort will involve four major components:

(A) Design of a dc/dc high frequency transformer made using 1.7 kV SiC devices.

(B) Power monitoring, signature recognition, and advanced sensing.

(C) Control architecture and power cycling of the modular PEBBs.

(D) Development and demonstration of condition-based maintenance algorithms on the proposed dc/dc high frequency transformer.

2 Progress Summary

This report summarizes our progress on line item A, B, and C. Our progress so far at a high-level are as follows: items a - f were covered in the first report in 2018; items g - k were done in year 2019; items l - r were achieved in year 2020 and items s - x were performed in 2021:

(a) Performed literature review to understand the landscape and different approaches, the research community has investigated for monitoring the health of SiC devices.

(b) Developed plan to identify an approach through which we can create thermal stress on the SiC-based converter.

(c) Down-selected the SiC MOSFET that we will be using to create the LLC-resonant dc-dc converter.

(d) Designed the converter using the SiC MOSFET by calculating different component values required to achieve the operation at rated load.

(e) Performed preliminary simulation using LT-Spice to validate operations in open-loop at the corner points i.e. high power and low power.

(f) We are having monthly meeting with Dr. John Donnal of USNA and he is working on the sensing circuit. Once we have a complete design of the converter we will layout the PCB that will include our power converter design and Dr. Donnal's sensing circuit.

(g) Designed and fabricated a PCB prototype of the proposed PEBB (H-bridge), with a rating of at least 1 kV DC-link voltage and maximum load current of 30 A (RMS).

(h) Tested the fabricated PEBB with a L-R load for verification up to 1 kW of output power at 200 V DC-link voltage (20% of rated DC voltage) and 5 A of output RMS current (16% of rated load current).

(i) Designed, fabricated and verified the capacitor bank of the LLC resonant converter.

(j) Designed inductor and ordered the Litz wire (Lead time: 1 month) that will be used to make the inductor of the resonant tank.

(k) Designed the transformer of the LLC resonant converter.

(l) Constructed the resonant inductor and transformer for the resonant tank.

(m) Performed initial open-loop control on the resonant converter.

(n) With the assistance from the USNA team, a prototype PCB to sense degradation is built and then tested on the PEBB.

(o) Published a paper in Applied Power Electronics Conference (APEC) 2020, entitled "Condition Monitoring of SiC MOSFET utilizing gate leakage current."

(p) Designed and fabricated a new PCB of the PEBB integrated with the sensing circuit to demonstrate feasibility of the overall system.

(q) Performed literature review to examine various methods to analyze and/or control a resonant converter.

(r) Performed state-plane analysis of the resonant converter operations modes and used simulation to verify the correct state trajectory.

(s) Analyzed the dependency of switching frequency on the current leakage estimation for condition monitoring. Data after proper calibration from the results now show independence of duty ratio, switching frequency, dc-link voltage, and drain (load) current.

(t) Used the new PEBB with integrated sensing circuit to test the condition monitoring technique at 1 kV dc-link voltage and 25 A of peak drain current.

(u) Manuscript entitled "Condition Monitoring of SiC MOSFET utilizing gate leakage current." is submitted and under review by the IEEE Transactions on Power Electronics (TPEL).

(v) Methods to establish communication between the micro-controller and PC at high voltage environments were investigated.

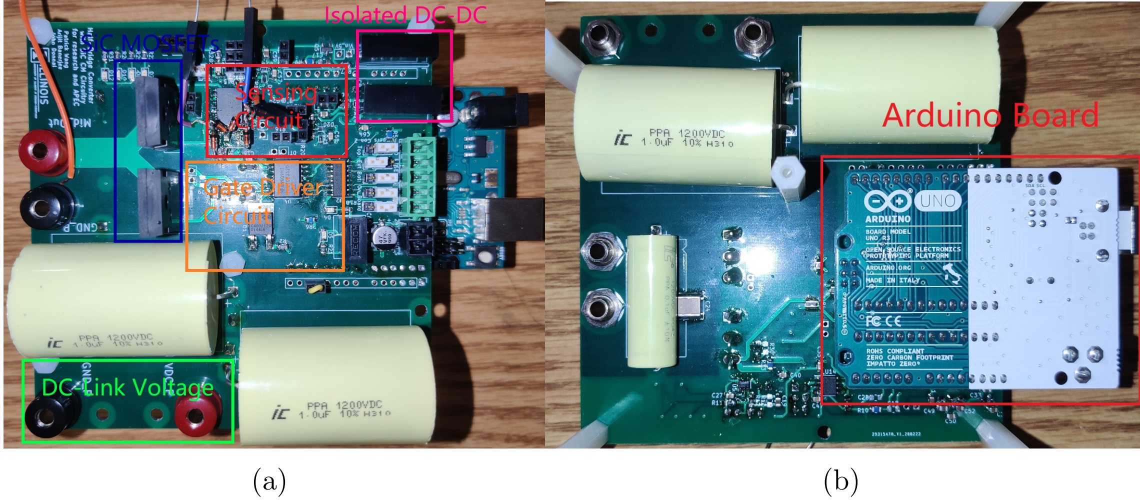
(w) Serial communication interface such as JTAG and UART signals are stepped up to higher voltages and converted to USB signals away from the power converter.

(x) Developed a modular, full-bridge PEBB with flexible setup of uni-directional or bi-directional power transfer, passive or active rectification, controlled by a C2000 32-bit MCU from TI with condition monitoring.

Condition monitoring has been achieved for a resonant converter operating at various converter operating conditions. Going forward, the next step is to build and test the modular PEBB, program the MCU to achieve power cycling as proposed, and record data of the gate leakage current of aging devices with the proposed sensing circuit.

3 SiC MOSFET Condition Monitoring

Following the work presented in the last report, one of the main objective is to test the condition monitoring technique near rated conditions, especially at a higher dc-link voltages and drain current of the device under test. This is achievable using the new half-bridge PEBB presented in the previous report, shown in Fig. 1.



(a) (b)

Figure 1: Annotated (a) top view of the half-bridge PEBB with integrated sensing circuit (b) bottom view of the circuit.

This prototype is designed for a dc-link voltage up to 1.2 kV and integrates the condition monitoring circuit to be part of the gate driver circuit. The Arduino provides the switching signals as well as automated data recording for the estimated leakage current using the available ADCs. With a LLC resonant tank as the load, the drain current of the MOSFET could be pushed much higher without significant output load, due to the magnetizing current in the transformer. The circuit configuration for the test setup is shown in Fig. 2.

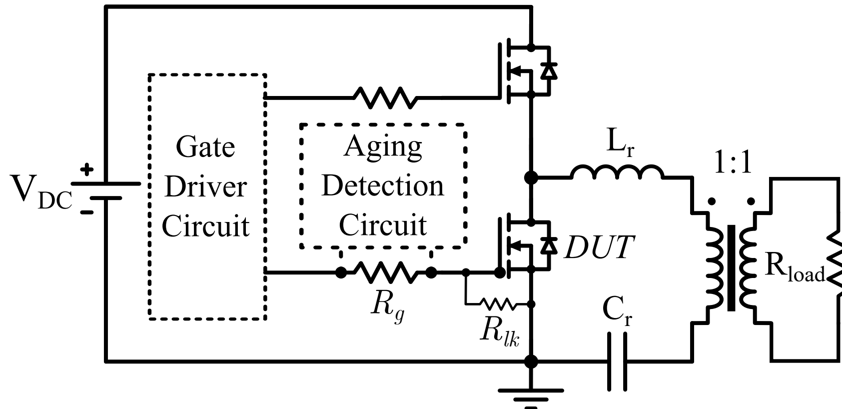


Figure 2: Circuit diagram of the experimental setup to obtain data and validate the proposed method. The aging detection circuit is attached across the external gate resistor of the low-side SiC MOSFET. An additional resistor R_{lk} is placed across gate-to-source to mimic gate leakage current.

3.1 Functionality at Higher Ratings

To test the robustness of the proposed condition monitoring circuit, we attempted to operate the converter near the rated conditions of the SiC MOSFETs. In Fig. 3, the converter is operating with 1 kV dc-link voltage, 24 A peak drain current duty ratio of 0.5 at 100 kHz switching frequency. Under this condition, data were captured for various predetermined gate leakage current of 0 mA (healthy device), 5 mA, 9 mA, and 19 mA, shown in Fig. 4. These leakage current were produced by placing a leakage resistance R_{lk} across the gate and the source of the MOSFET. This was shown in the literature to be an accurate replication of an aged MOSFET device. With a known gate leakage current, we can directly compare the estimated gate leakage current to the actual gate leakage current as shown in Fig. 4.

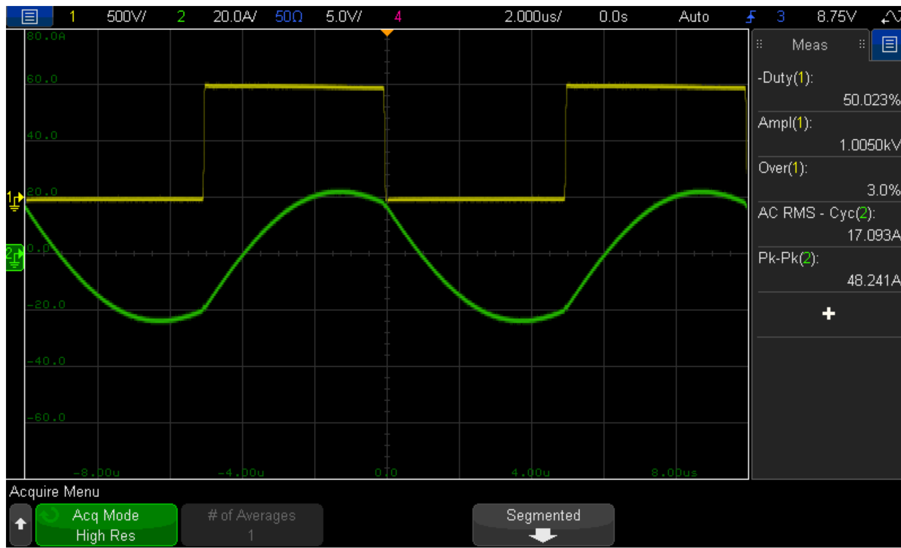


Figure 3: Oscilloscope capture of voltage waveform V_{ds} (yellow) across the DUT and the switching output current I_{out} (green).

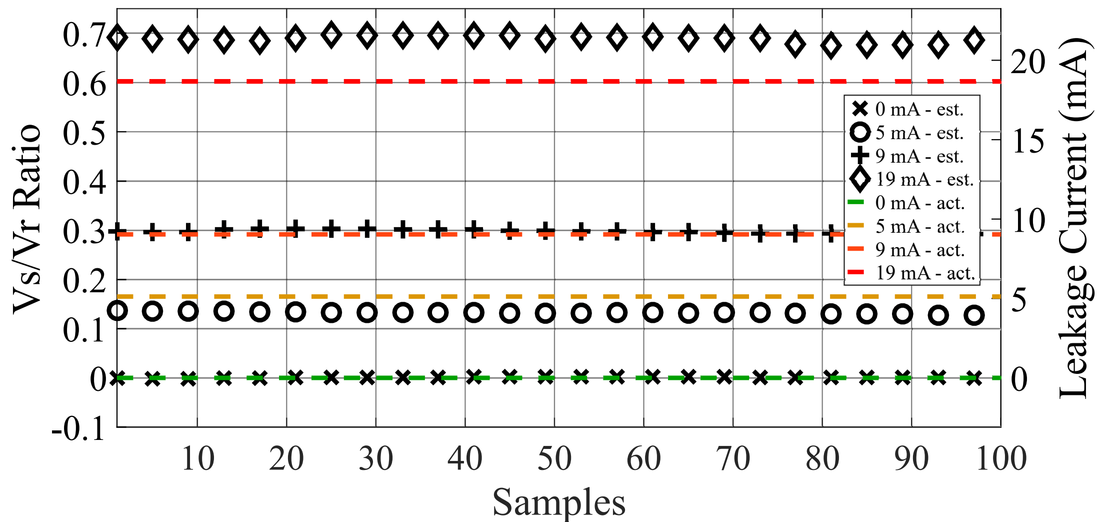


Figure 4: 100 calibrated samples recorded over a period of 10 seconds compared to actual gate leakage current for cases of 0 mA, 5 mA, 9 mA, and 19 mA. Data is averaged and truncated for clarity.

3.2 Frequency Dependency and Calibration

As explained in the previous report, as well as in our published work [?], the ratio of the integrator output v_s and v_r allows us to estimate the on-state gate leakage current. v_s tracks the total positive charge which has entered the gate, while v_r tracks the total on-time. v_s, can be mathematically represented as

$$v_s(T_s) = \frac{T_s R_g G_s}{T R_o C_o}[\int_0^{t_1} \widehat{i}_t(t)dt + \int_0^{DT} i_{g,lk\text{-}on}(t)dt] \quad (1)$$

which can be observed to have two components. The first term consists of a current pulse $\widehat{i}_t(t)$ which lasts for a short period of time t_1 during the transient turn-on event. This current is likely truncated since the intermediate op-amp will be saturated, hence we cannot claim it is the actual gate charge q_g (i.e. from the datasheets) instead we will use $\widehat{q}_t$, as shown in Eq. (2).

$$v_s(T_s) = \frac{T_s R_g G_s}{R_o C_o}[\widehat{q}_t f_{sw} + D I_{g,lk\text{-}on}] + C_2 \quad (2)$$

The second term is the charge during the on-state due to gate leakage. In a healthy device, we would expect the second term to be zero, hence only the first term remains. The value of v_s, due to the first term, would be proportional to the switching frequency. Since the more number of times we switch, the more times the gate would be charged.

It was therefore possible to quantify $\widehat{q}_t$ by varying the switching frequency on a healthy device, as shown in Fig. 5. The equation shown can be used to calibrate v_s to achieve more accurate estimation at various switching frequencies shown in the next section.

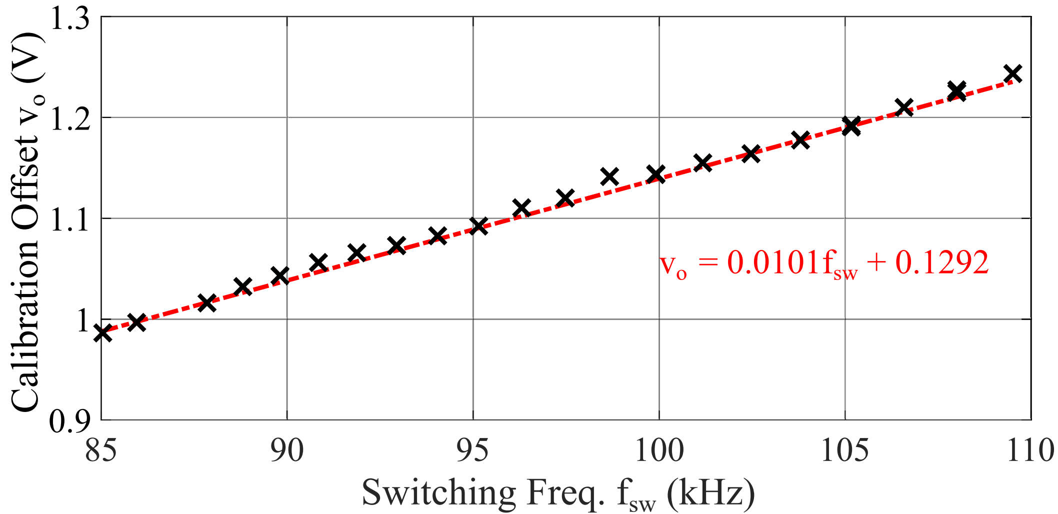
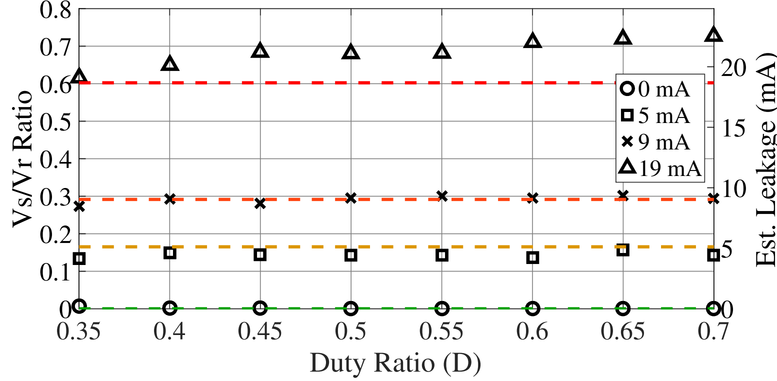


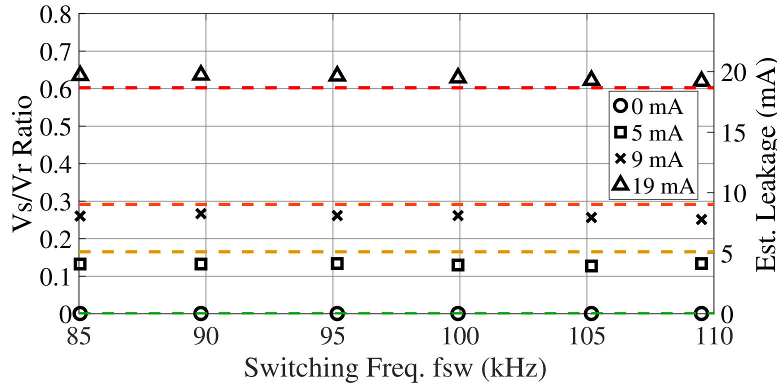
Figure 5: Readings of output v_s of a healthy MOSFET device vs. switching frequency. Since no leakage current exists, the output is a result of transient charges $\widehat{q}_t$ and the integrator incrementing due to non-ideal op-amp characteristics. Equation shown in the figure can be used as the calibration equation for all conditions.

3.3 Experimental Results

This section shows the robustness and consistency of the sensing circuit regardless of the power converter operations. The calibrated v_s/v_r ratio should remain constant for a given leakage current regardless of duty ratio, dc-link voltage, output load, and switching frequency of the converter.



(a)



(b)

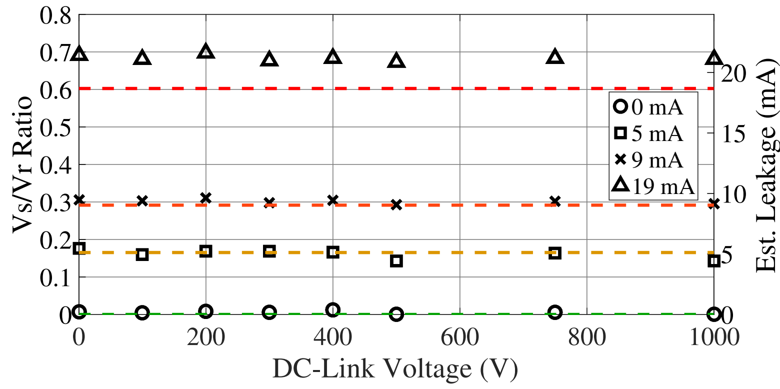
Figure 6: Captured data of calibrated v_s/v_r ratio and the equivalent leakage current versus (a) duty ratio D and (b) switching frequency f_{sw} for various known leakage currents. Unless stated otherwise, converter operates at a duty ratio of 0.5, dc-link voltage of 1 kV, output power of 3 kW and switching frequency of 100 kHz. With proper calibration, v_s/v_r ratio and the equivalent leakage current show consistency across various duty ratio and switching frequency. For (b), DC-link voltage is set at 300 V and output power of 1 kW.

The calibrated v_s/v_r ratio versus duty ratio D plot is shown in Fig. 6 (a). Four data sets are plotted for the cases with 0 mA, 5 mA, 9 mA and 19 mA of gate leakage current. The ratio remains constant as long as duty ratio is above 0.35; the values drop as duty ratio becomes smaller. The reason behind this phenomena is because during the transient turn-on event t_1, the op-amp is designed to be saturated. Any additional gate charge due to gate leakage current will not be integrated. The gate leakage current information during t_1 is essentially lost. To solve this problem, one could redesign the gain such that the op-amp does not saturate during transient switching. This however, will have a big impact on the resolution and accuracy of the measurement, as the first

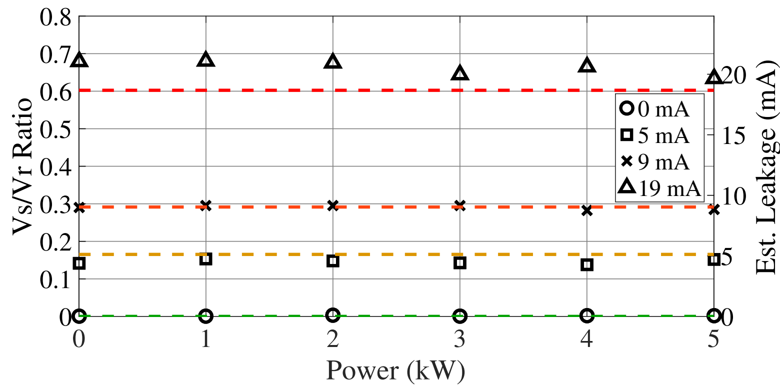
term in Eq. (1) will now dominate the second term. After calibration, we would barely detect anything due to leakage. With the current setup, while the estimation of leakage current changes at lower duty ratio, the diagnostic ability of the circuit is still functional. We can still clearly distinguish and aged device from a healthy device.

Figure 6 (b), show that while the original v_s value is switching frequency dependent, with proper calibration the calibrated v_s/v_r ratio becomes constant for varying switching frequencies. Switching frequency is swept near the resonant frequency of 100 kHz. The dc-link voltage and output power for this test is kept at 300 V and 1 kW respectively, since switching loss become significant at lower frequencies.

Additional converter operating conditions such as variations in dc-link voltage and load show the independence and consistency of the current estimation with the calibrated v_s/v_r ratio, as presented in Fig. 7 (a) and (b), respectively. In both scenarios, there is a clear distinction between each data sets of different leakage and the measurements match the actual value. These experimental data validate the diagnostic functionality of the method, which remains unaffected by the changes in converter operating conditions.



(a)



(b)

Figure 7: Captured data of calibrated v_s/v_r ratio and the equivalent leakage current versus (a) dc-link voltage and (b) output power (load) for various known leakage currents. Unless stated otherwise, converter operates at a duty ratio of 0.5, dc-link voltage of 1 kV, output power of 3 kW and switching frequency of 100 kHz. With proper calibration, v_s/v_r ratio and the equivalent leakage current show consistency across various dc-link voltage and load condition.

4 Peripheral Communication Setup

While running experiments and obtaining data using the ATMega328P, an issue occurred which the serial connection between the PC and the MCU was interrupted. This phenomenon occurs whenever the dc-link voltage of the converter went above 600 V. While the exact reason is still unknown, the current hypothesis is that the USB cable from the PC to the Arduino board is picking up too much noise due to the switching of the converter. This would eventually cause the PC to break the connection to the MCU, and it would be unable to reconnect until the MCU has been rebooted. The peripheral interface between the MCU and the FTDI (USB-to-UART converter) is unlikely to be the cause of this issue as it had short traces on the same circuit board.

To resolve the issue during data collection, the v_s and v_r values (data) were stored on the 1K-byte EEPROM on-chip memory of the MCU and then retrieved after each testing condition. This however, is not a long term solution once we attempt to collect data as we perform power cycling to actively age the SiC devices.

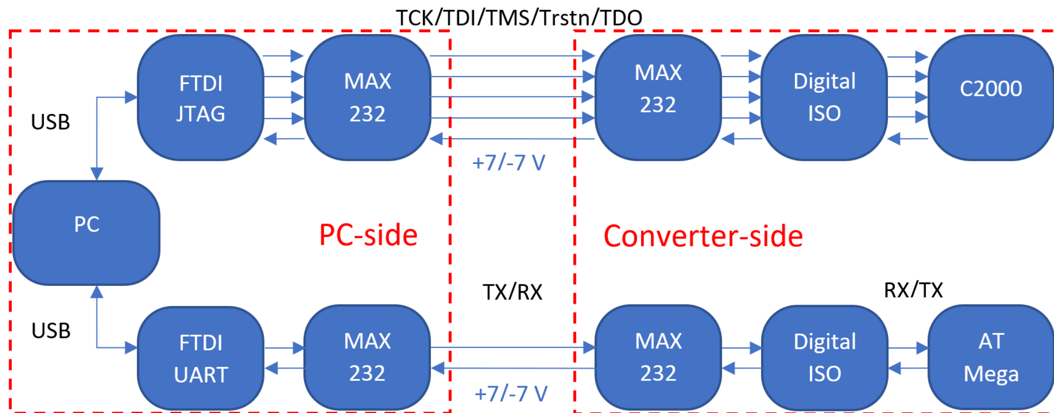


Figure 8: Block diagram of proposed method to overcome communication loss over noisy environment.

The proposed solution to this problem is having the FTDI chip located far away from the noisy environment, as shown in Fig. 8. The USB cable will connect the PC to the FTDI chips across a short distance, while the peripheral communication lines such as (TX/RX for UART) or (TCK/TDI/TMS/Trstn/TDO for JTAG) will be connected to the MCU via a longer, D-sub cable. To ensure that the peripheral signals are not interfered, MAX232 driver/receiver will be used to drive a high and low signal of +7/-7 V, respectively. This ensures that signal transferred from the MCU to the FTDI will not be distorted due to noise.

4.1 Prototype Circuit

Prototype circuits, as shown in Fig. 9 have been built and tested under non-noisy environment so far. The MAX232 limits the maximum bit-rate and therefore the JTAG clock frequency TCK is limited to 100 kHz for reliable communication. (The clock frequency can be changed in the 'Target Connection Setup' in Code Composer Studio for C2000 MCUs from TI). Using this method, the C2000 MCU can still be programmed via the Code Composer Studio, and serial communication between the PC and MCU functions.

For the ATMega328P, the UART TX/RX is only capable of receiving data from the MCU. The converter-side circuit will be a plug-in in future PEBBs. Further tests still need to be performed under noisy environments.

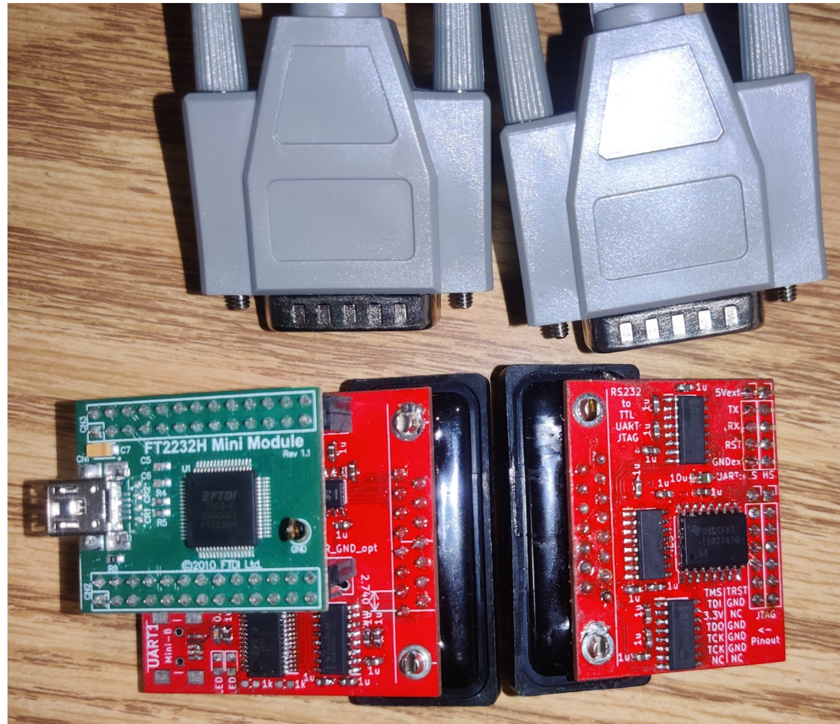


Figure 9: Prototype circuit of the peripheral communication line between the PC and the MCUs. On the left is the PC-side, and on the right is the converter-side of the circuit shown in Fig. 8.

4.2 FTDI Programming

The FTDI chips need to be flashed and programmed accordingly for their purposes in order to communicate with the MCU. For instance, the FT2232H used to establish JTAG with the C2000 MCU requires the XDS100 debug program to be burned in to the memory to establish connection with the MCU via the Code Composer Studio. This can be achieved using the FT_PROG available from the FTDI utilities homepage. The user interface of the software is shown in Fig. 10. Once a device has been recognized, a template (available on TI if attempting to connect to C2000) should be chosen and then programmed onto the device.

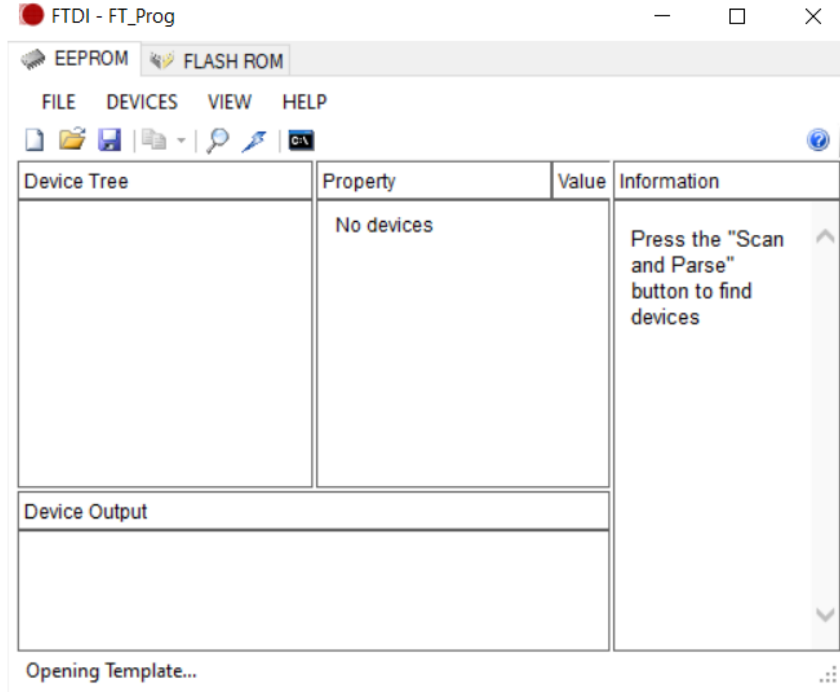


Figure 10: The FTDI programmer used to erase and write the memory of FTDI chips in order to establish communication with the MCUs.

5 Modular PEBB

The design of a modular PEBB would allow us to replace and modify the circuit is more appropriate if we attempt to power cycle and purposely degrade the devices. In one incident, when the devices failed while delivering 6 kW of output power, the accident caused by the failure damaged the circuit board, rendering the rest of the circuit useless. Our attempt is to create a modular PEBB, as shown in Fig. 11, such that all logic signals remain on the 'main board', while power components such as the SiC MOSFETs and diodes that would require replacement, are connected to the 'main board' via standoffs and pogo pins. This way, they could be easily replaced without assembling an entire circuit in case of a sudden failure. A prototype circuit has been partially built and tested, shown in Fig. 12, which sits on top of the heat sink which all devices share.

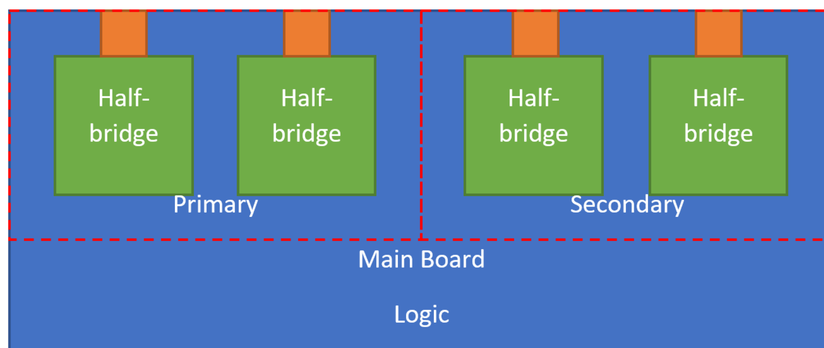
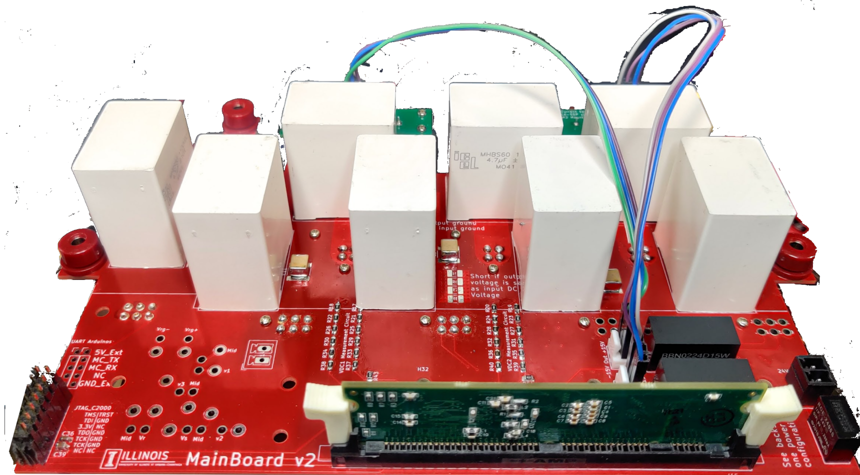
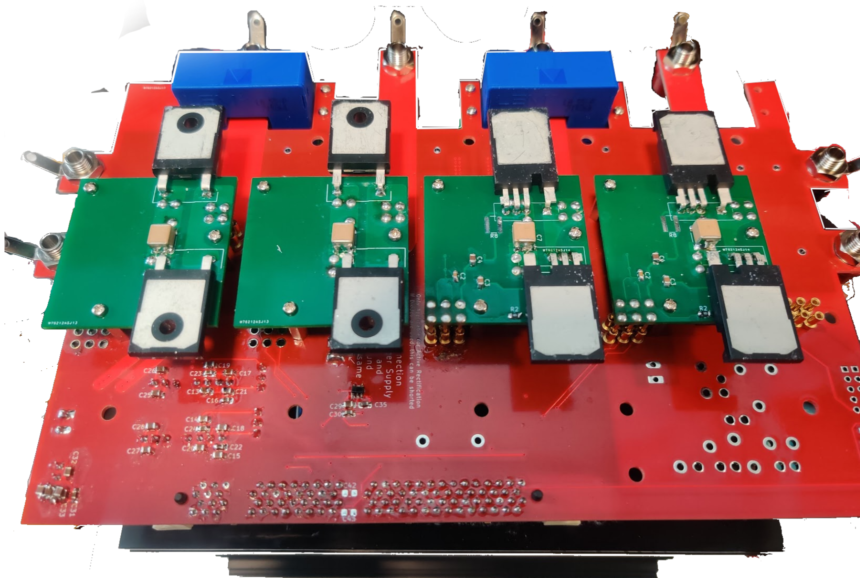


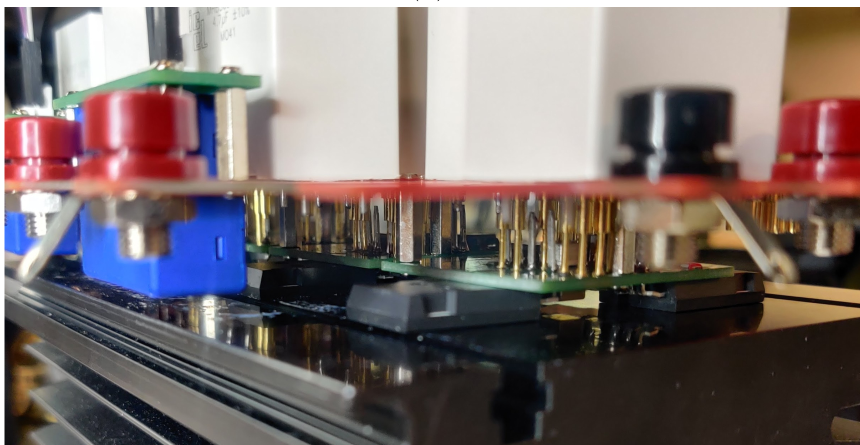
Figure 11: Proposed modular PEBB with a total of 4 adjustable half-bridges (green). The primary H-bridge has a different dc-link and ground than the secondary H-bridge; they can be adjusted to be the same.



(a)



(b)



(c)

Figure 12: (a) Top view, (b) bottom view and (c) side view of the assembled modular PEBB.

The half-bridges, either a pair of active SiC MOSFETs or passive diodes are shown in Fig. 13. They can be reconfigured interchangeably based on the converter design.

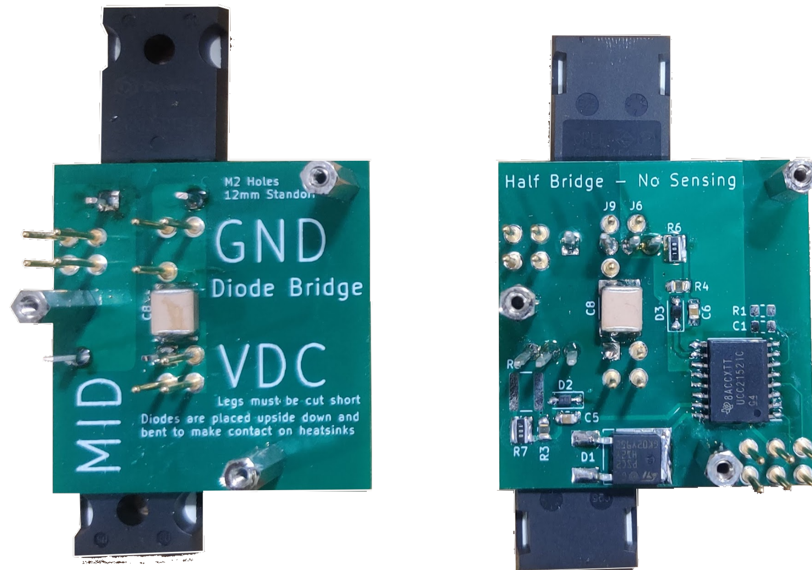


Figure 13: Diode-bridge on the left, half-bridge with SiC MOSFETs on the right.

5.1 Experimental Results

The PEBB was tested with an active H-Bridge at the primary and a full-bridge rectifier at the secondary of the transformer up to 500 V dc-link voltage. At 500 V, connection between the C2000 MCU and PC was undisturbed, and the PC could still maintain and receive serial data from the ATMega328P to retrieve current leakage information. The test setup is shown in Fig. 14.

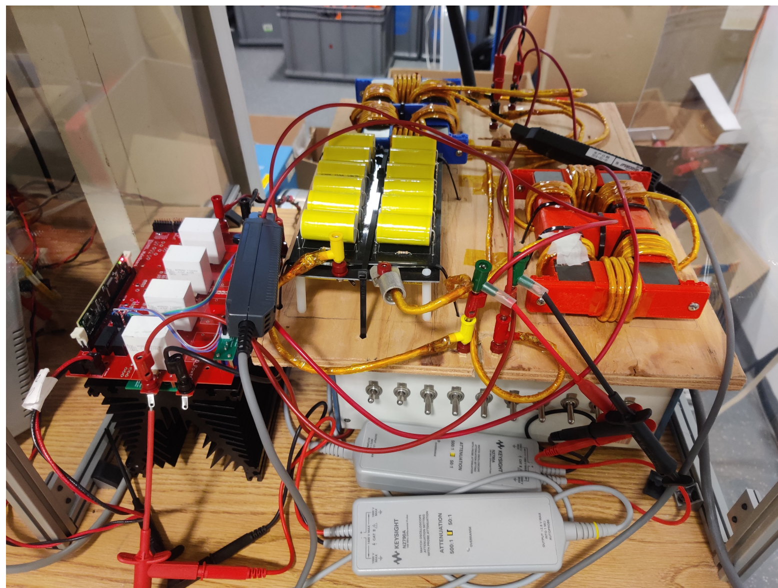


Figure 14: Test setup of running PEBB as a full-bridge resonant converter with 500 V of DC-link voltage.

Oscilloscope capture of the input voltage to the resonant tank, resonant inductor current, magnetizing inductor current, transformer secondary output current and DC output voltage is shown in Fig. 15.

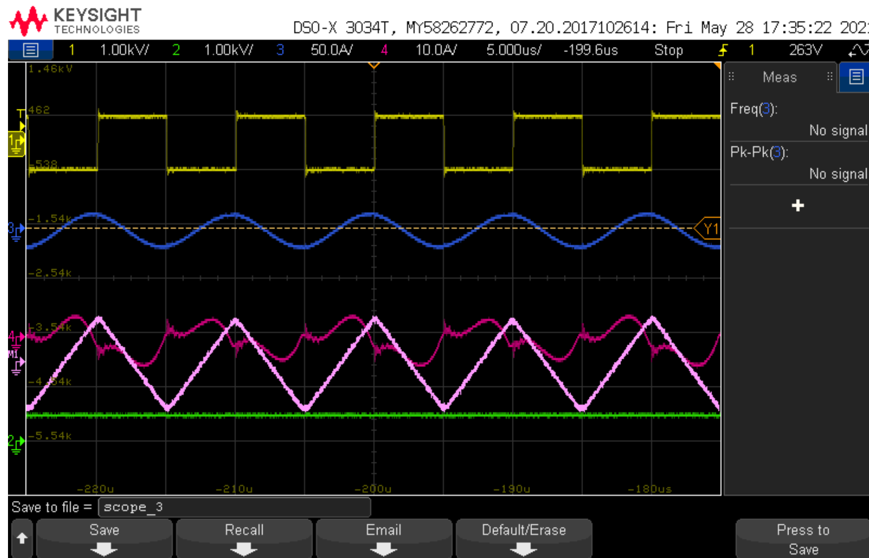
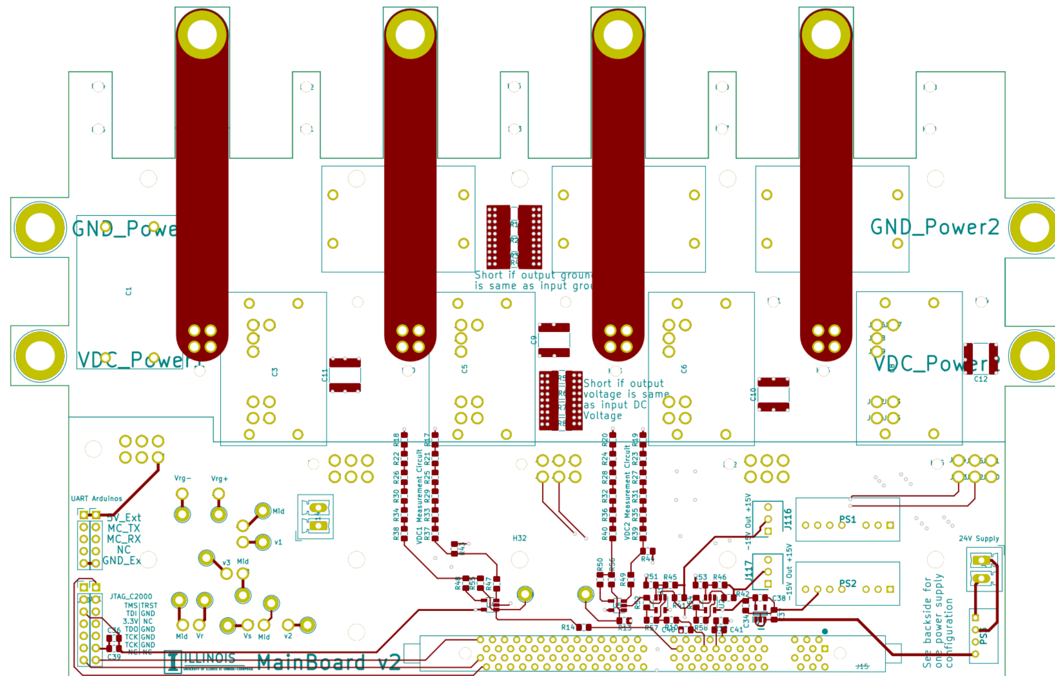


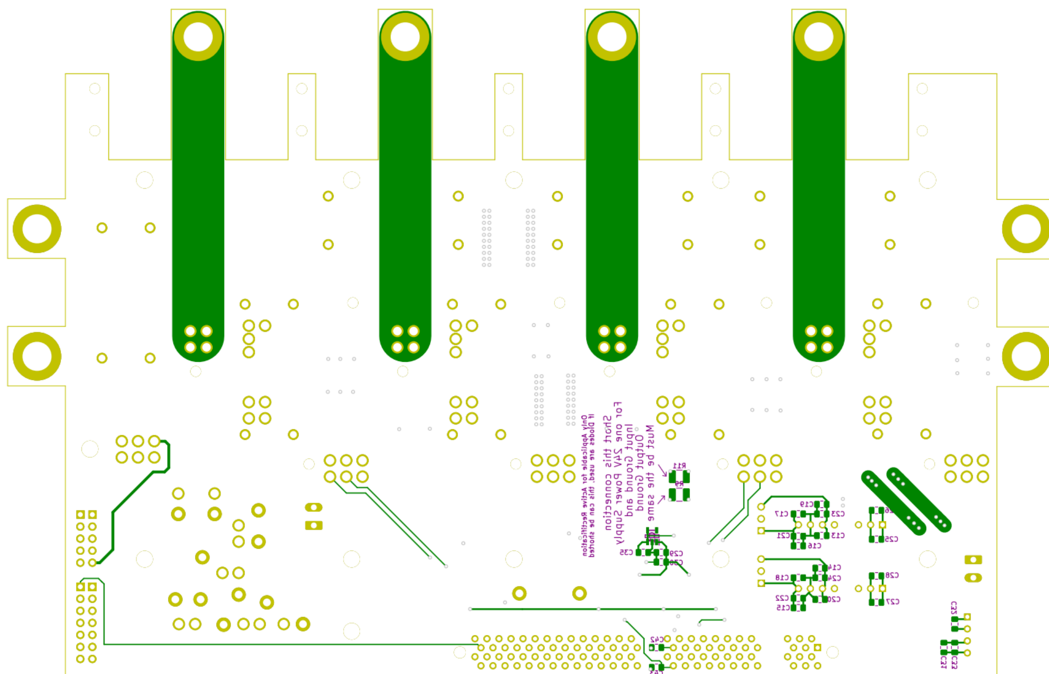
Figure 15: Oscilloscope capture of input voltage of resonant tank (yellow), resonant inductor current (blue), magnetizing inductor current (pink), transformer secondary output current (magenta/CH4), and DC output voltage (green) at 500 V DC-link voltage and 1.5 kW output power.

5.2 Main board Layout

The main board consists of four layers, as shown in Fig. 16 and 17. The main board contains isolated power supplies which provide power for the measurement circuits, microcontrollers and gate driver circuits. Current measurement and voltage measurement circuits measure the both primary and secondary side, which is sufficient for closed-loop control in the future. DC-link capacitors are placed at the power-side of the main board.

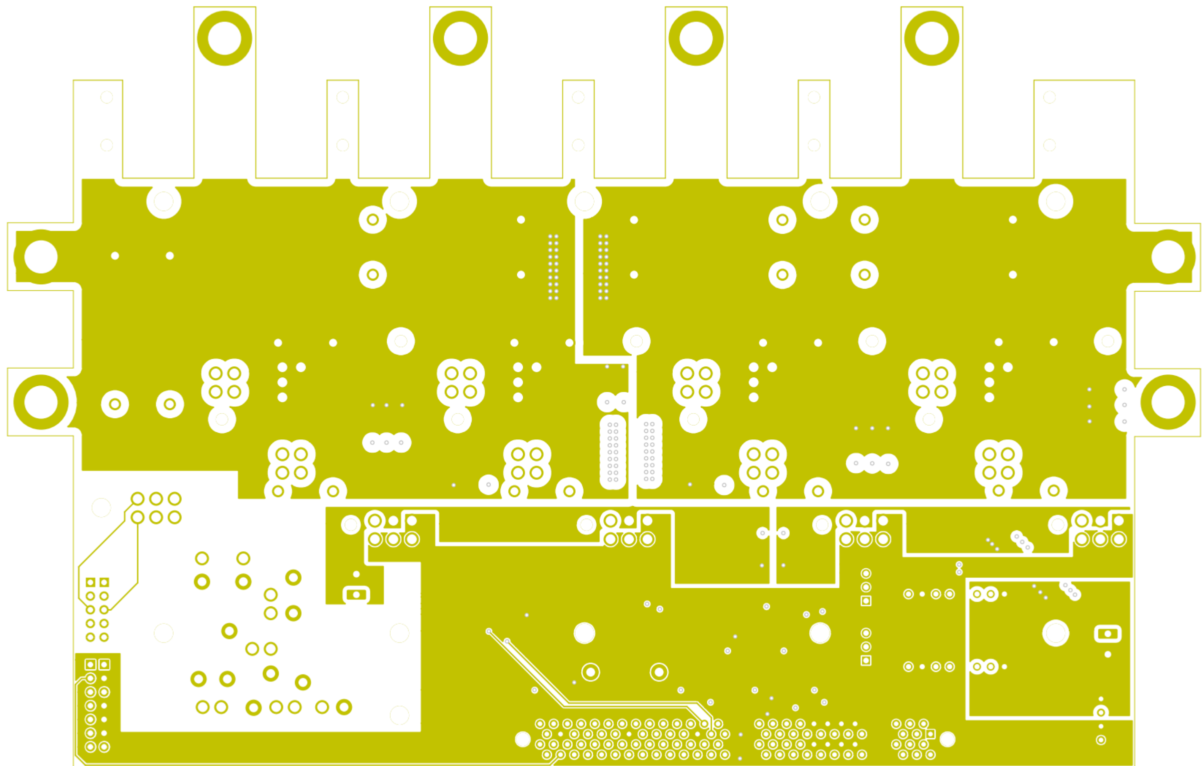


(a)

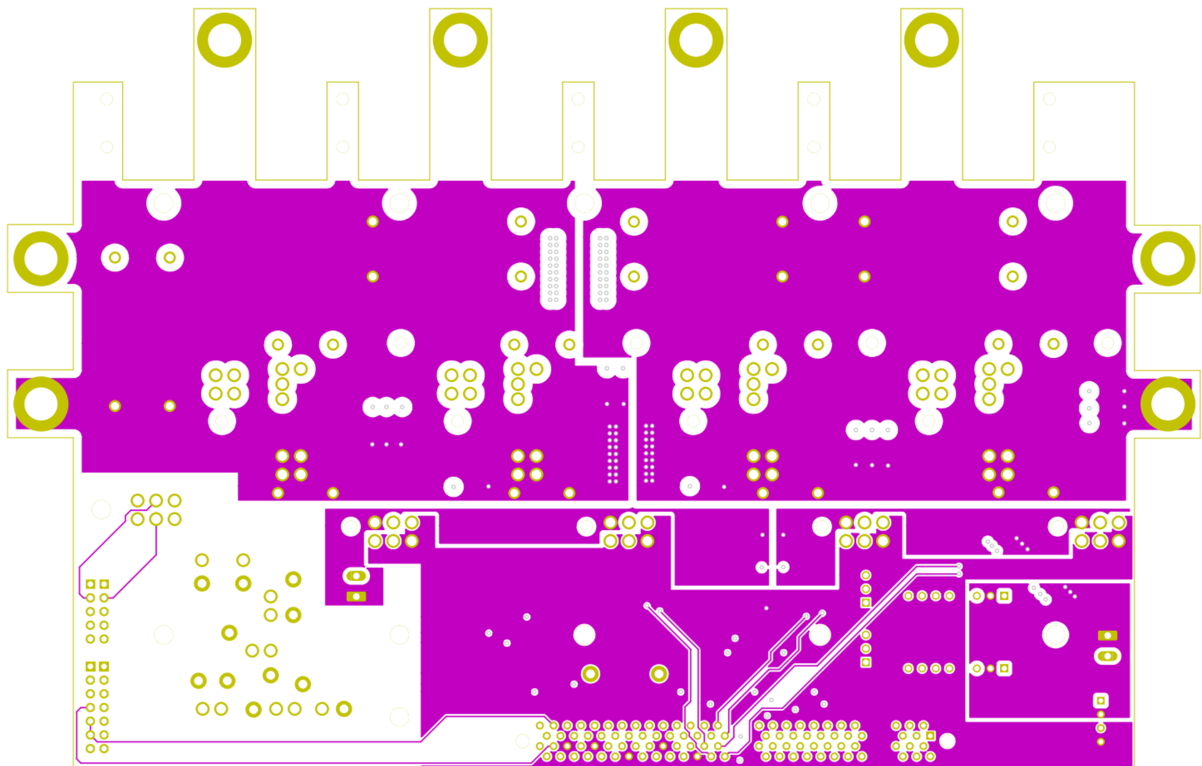


(b)

Figure 16: (a) Top view and (b) bottom view of the main board PCB.



(a)



(b)

Figure 17: (a) Inner layer 1 and (b) inner layer 2 of the main board PCB.

5.3 Modules Layout

The diode-bridge modules and SiC MOSFETs half-bridge and are shown in Fig. 13. The layout of those are straight forward shown in Fig. 18 and 19.

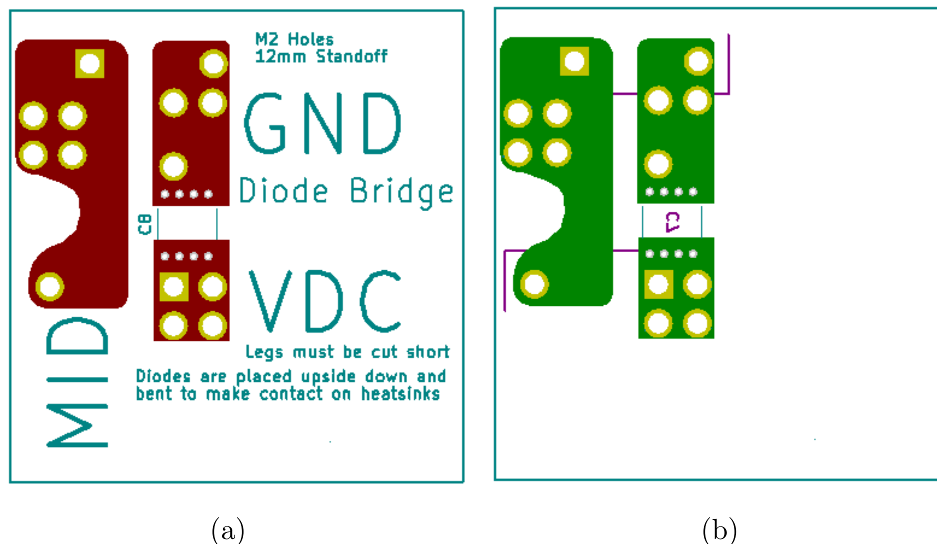


Figure 18: (a) Top view and (b) bottom view of the diode-bridge module PCB.

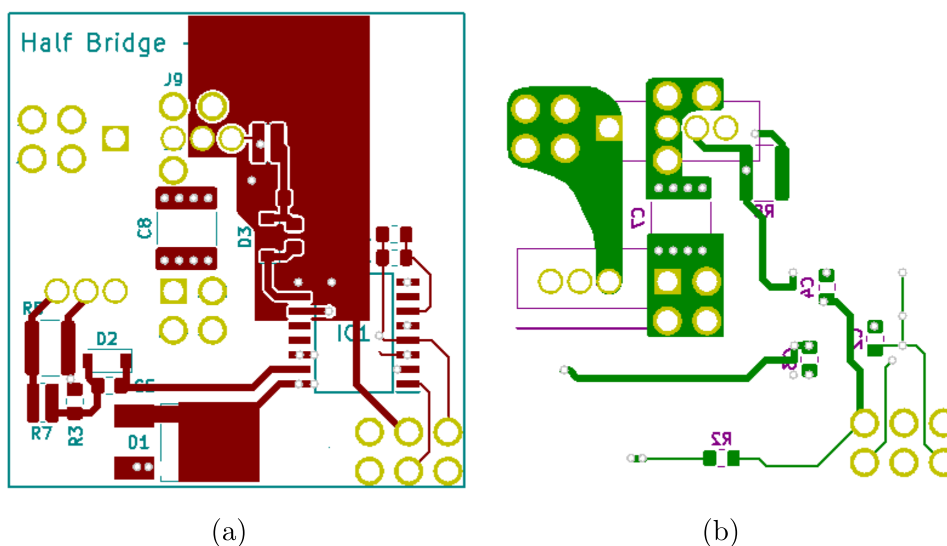


Figure 19: (a) Top view and (b) bottom view of the half-bridge module PCB.

The current sensors are modules designed to be mounted at the edge of the PCB such that the PCB trace from the main board enters between the sensor.

A SiC MOSFET half-bridge with condition monitoring technique for both low-side and high-side is shown in Fig. 20.

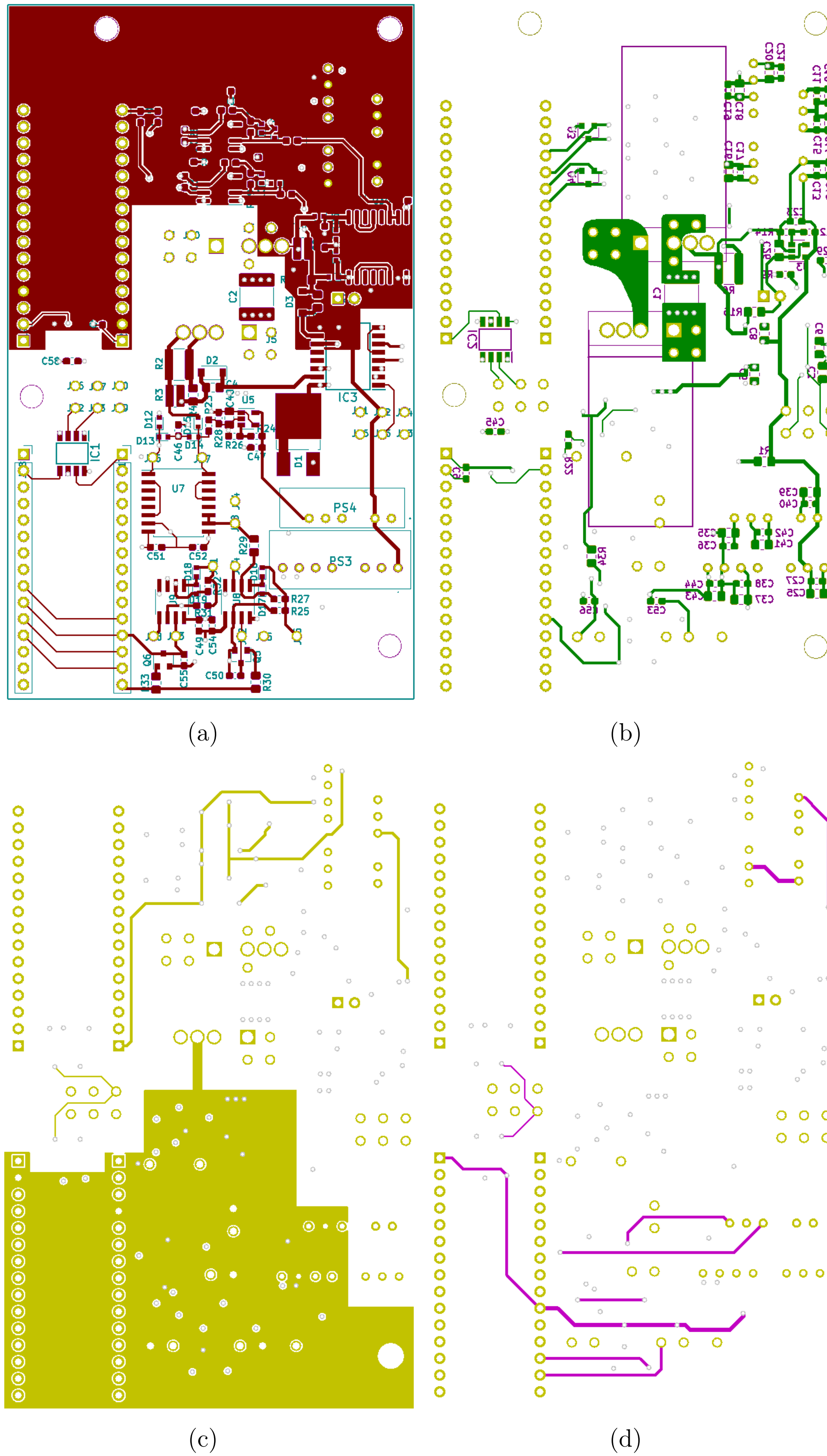


Figure 20: (a) Top view, (b) bottom view, (c) inner layer 1 and (d) inner layer 2 of the half-bridge module PCB with condition monitoring.

6 Going Forward

Going forward, the next step is to finish building and testing the modular PEBB. The C2000 MCU must be programmed to achieve power cycling as proposed, and data of the gate leakage current for aging devices will be collected via the proposed condition monitoring technique.

7 Acknowledgment

The team deeply acknowledges all the help and support that Dr. John Donnal from USNA provided. We are continuing having regular bi-weekly discussions with Dr. Donnal. Also, the team is grateful to the Office of Naval Research and Mr. Lynn Petersen for the generous support of this research.

REPORT DOCUMENTATION PAGE

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED	
		START DATE	END DATE
23 December 2021	Final	20210401	20211223

4. TITLE AND SUBTITLE

Condition Monitoring of SiC MOSFETs Based on Gate-Leakage Current Estimation

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Silicon carbide (SiC) MOSFETs have a lower loss, faster switching, and better thermal conductivity compared to silicon MOSFETs; however, their reliability remains a major concern hindering their widespread adoption. In situ, low-cost condition monitoring of the devices within the power converter can alleviate this concern. Gate-leakage current has been shown to be one of the most consistent failure precursors of degraded SiC MOSFETs. This article presents an approach to monitor the condition of SiC MOSFETs by an in situ estimation of the gate-leakage current using an add-on circuit. A prototype converter along with the extended monitoring circuit is used to experimentally validate the proposed approach. The proposed strategy ensures that the gate-leakage current estimation approach is solely dependent on the gate-oxide degradation and has a minimum dependence on the converter's operating conditions, including duty ratio, dc-link voltage, switching frequency, and output power, opening opportunity to device-level prognostics using sophisticated algorithms.

15. SUBJECT TERMS

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