Project Report
TIP-174

Vertical CMOS Logic: FY21 Advanced Devices Technical Investment Program

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14 April 2022

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ABSTRACT

Pushing data-intensive applications such as artificial intelligence and machine learning to edge nodes requires increasing performance and reducing power of digital CMOS logic as well as increasing the number of available arithmetic logic units and cache memory capacity. To realize such improvements, the vision of the vertical CMOS logic concept is to turn the entire CMOS transistor logic layer on its side to build vertical logical gates composed of six or more vertically oriented transistors monolithically fabricated from a single silicon nanowire. Akin to skyscrapers in a densely populated city, the vertical logic scheme will enable an enormous increase in computational resources while at the same time improving circuit-level performance and power.

FY21 was the first year of an anticipated three-year effort. The scope of the effort for FY21 was adjusted from the original proposal to reflect the awarded funding. This report describes progress on the three revised tasks. Section 1 provides an introduction to the technology concept. Section 2 covers logic set functionality and calculations of energy efficiency. Section 3 explores potential fabrication process flows. Section 4 describes progress toward selective epitaxial nanowire growth. Section 5 is a brief summary and outlook toward FY22.

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1. INTRODUCTION TO VERTICAL LOGIC

CMOS circuits are characterized using metrics of power, performance, and area (PPA). All three components of PPA are improved by shrinking the transistor size, which results in reduced logic cell resistance and capacitance and increased number of resources. This geometrical scaling has been successful for decades, and has been enhanced by a progression from planar transistors to FinFETs and nanowires (Figure 1) which increase device density per unit area. However, geometrical scaling is approaching irreducible limits based on the fundamental physics of charge distribution and the size of the electron wavefunction. Further dimensional scaling beyond these limits will not be possible using conventional transistors and materials. With scaling in lateral dimensions reaching a roadblock, a possible path forward is to use vertical scaling. By vertically stacking transistors, we can continue increasing the number of transistors per unit area (and per unit cost) as described by Moore's law (Figure 1).

One layer of vertically integrated logic will reduce area by as much as 4x. In addition, because the cells terminate vertically, they can be stacked on top of one another leading to almost limitless vertical scaling of transistor density. This may seem unrealistic, but one can look to Samsung's production 136-layer NAND flash as an example of extreme vertical scaling. Performance and power—often reported as the quotient of the two (i.e., GOPS/W)—is expected to increase by 6x. This is equivalent to approximately four nodes of traditional scaling (which will not be possible, in any case).

The microelectronics industry is exploring several approaches to transistor stacking, include complementary FETs (CFETs), end-of-line wafer bonding, middle-of-line wafer bonding, and laser recrystallization of polysilicon. The vertical CMOS logic described in this work is a more radical approach, as all of the other devices are still horizontal transistors, subject to the same scaling limits described above. Vertical logic would break through these dimensional constraints by rotating the transistor current flow out of the plane of the wafer, allowing for a more compact device and lower parasitic capacitance. We believe vertical logic is preferred to more exotic information processing devices proposed in the academic literature, such as spintronics or optical computing, because it builds upon the existing base of silicon process technology and does not invoke early-stage material concepts or unproven computing schemes. Instead, the underlying device physics of vertical logic is well understood, but the process integration is extremely challenging.

Risk-reducing the concept in this Line program will hopefully allow for development of an externally sponsored project to demonstrate the PPA benefits in silicon. Such an extreme advance in PPA would provide a tactical advantage to U.S. government computing systems, particularly those at edge nodes that are power-constrained. It would also provide a strategic national economic advantage by enabling U.S. chip manufacturers to leapfrog foreign competition and regain dominance as the supplier of leading edge microelectronics. For these reasons, we expect technology transition to occur through the OSD MINSEC program, the CHIPS for America Act, or the anticipated National Semiconductor Technology Center.

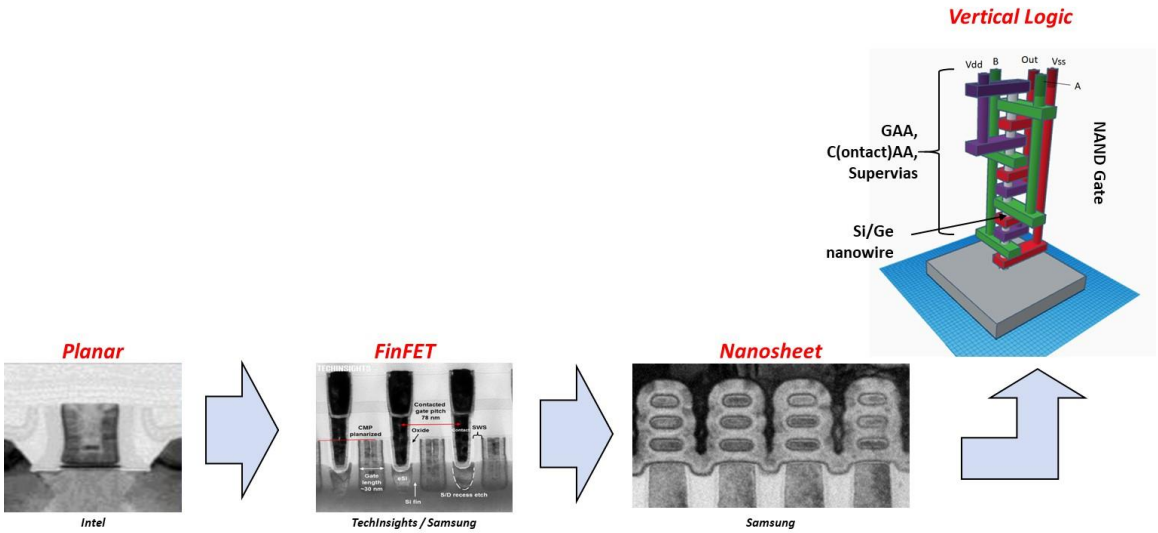

Figure 1. Progression of MOSFET technology.

2. LOGIC SET CONSTRUCTION AND PERFORMANCE ESTIMATES

For the vertical logic concept to serve as a practical successor to horizontal CMOS, one must be able to instantiate the same canonical logic gates. Figure 2 shows the vertical logic implementation of the six basic cells. The complete set requires a minimum of six transistors and six wiring tracks if no higher-level wiring is used in the cell. Importantly, all six cells can be implemented with three NMOS transistors at the bottom of the nanowire and three PMOS transistors at the top of the nanowire. This reduces the difficulty of nanowire growth, as will be shown in a subsequent section.

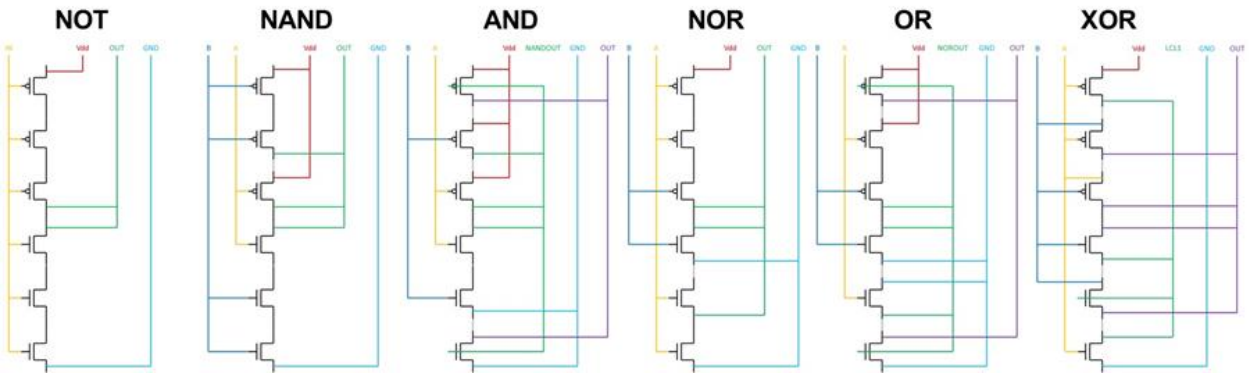

Figure 2. Basic standard cells instantiated in vertical logic.

The energy efficiency of vertical logic comes from the reduction in wirelength—and concomitant reduction in parasitic capacitance—of these cells compared to a traditional planar layout. Increasing the density of the circuit also brings the interconnect wiring closer together, however, which increases capacitance. So the capacitance of various layouts should be evaluated with supervia pitch, supervia diameter, and pin placement as variables. Constraining the problem is area; we want to maintain as small a footprint as possible for the device.

A COMSOL model of a two-input NAND cell is illustrated in Figure 3. The mutual capacitance matrix of each input and output, known as "pin capacitance" was calculated for multiple geometries. One set of results is shown in Figure 4 for conditions that result in a low capacitance while still decreasing area by more than 6x over a commercial foundry layout. The capacitance is reduced by a factor of 4 to 7 depending on exactly which commercial technology is used for comparison. As the switching energy of the cell is given by CV^2, this result validates that, if successful fabricated, the vertical logic structure will significantly improve computational energy efficiency.

We note that computational performance (speed) is just as critical a metric as energy efficiency (see Section 5).

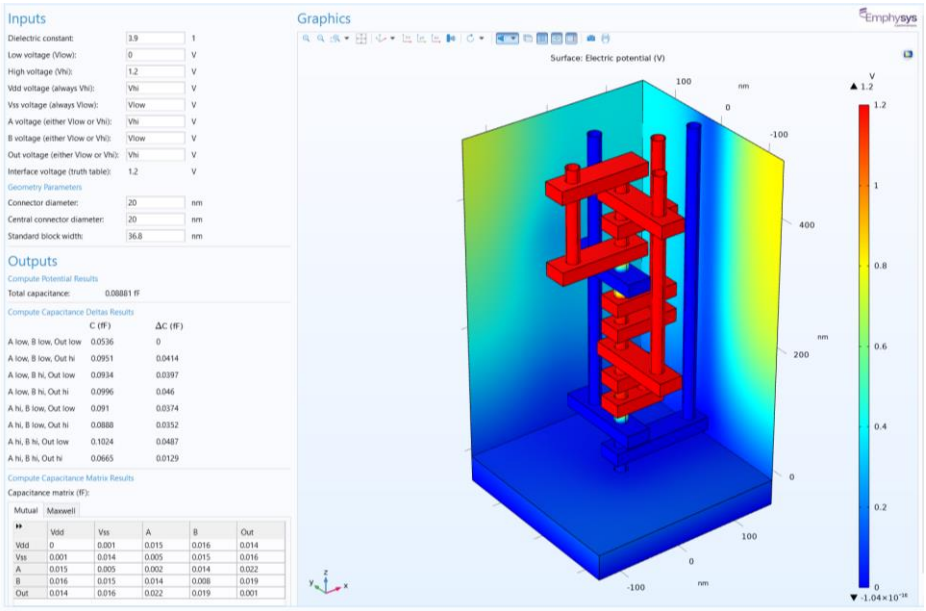

Figure 3. COMSOL capacitance model.

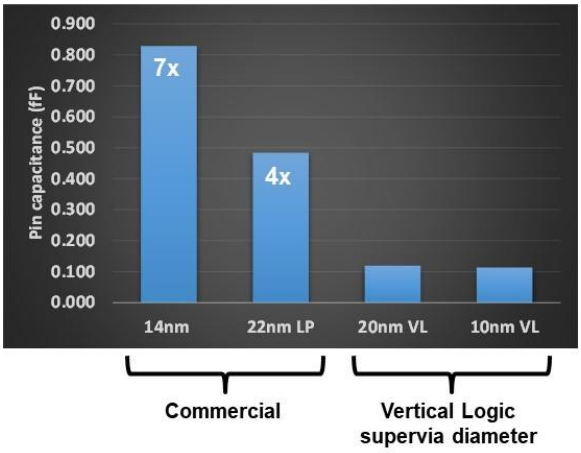

Figure 4. Capacitance of vertical logic NAND cell compared to commercially available technology.

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3. VERTICAL LOGIC FABRICATION FLOW

Vertical logic processing requires growth of vertical nanowires of Si and/or Ge, which will be sub-sectioned into six or more vertical-channel transistors through replacement gate and damascene supervia processing. An integration scheme that consist of over 400 individual processing steps was developed. Being comparable to the fabrication effort of leading edge production facilities, the scheme is not practical to complete fully in the current effort. Rather, the proposed work is to mitigate risks, develop new key modules, and demonstrate prototype structures. This is not a show-stopper for commercial fabrication but it is not practical to attempt the under the current effort. The major process steps are listed in Figure 5.

To risk-reduce the fabrication, we intend to perform three activities: develop a silicide bonding process, develop the critical silicon epitaxy module, and develop process simulations of the full flow. The silicide bonding process is described below, the silicon epitaxy in Section 4, and the process simulations in Section 5.

Figure 5. Reduced vertical logic process flow.

The nanowire bonding process essentially breaks up the full vertical logic flow into sequential fabrication of six individual transistors. This incurs penalties in area, power, and performance but is still superior to a planar layout. This approach may in the end be a compromise that is more practical for commercial fabrication, or could be thought of as a stepping stone toward monolithic vertical logic. The flow is shown in Figure 6. A short nanowire is fabricated from a pre-deposited silicon epi stack into a single vertical transistor including the source, drain, and gate contacts. Nickel is used as the contact metal, or at

least at the top of the contacts where they will electrically connect to the next transistor. A nickel-coated silicon-on-insulator (SOI) wafer with the proper epitaxially grown silicon stack is electrically connected to the contacts on the previous transistor through a thermally-driven nickel silicide reaction. The backside handle silicon and oxide layer are removed, leaving an electrically connected epi stack. This epi stack is fabricated into a second transistor, followed by nickel silicide bonding to a third wafer, etc.

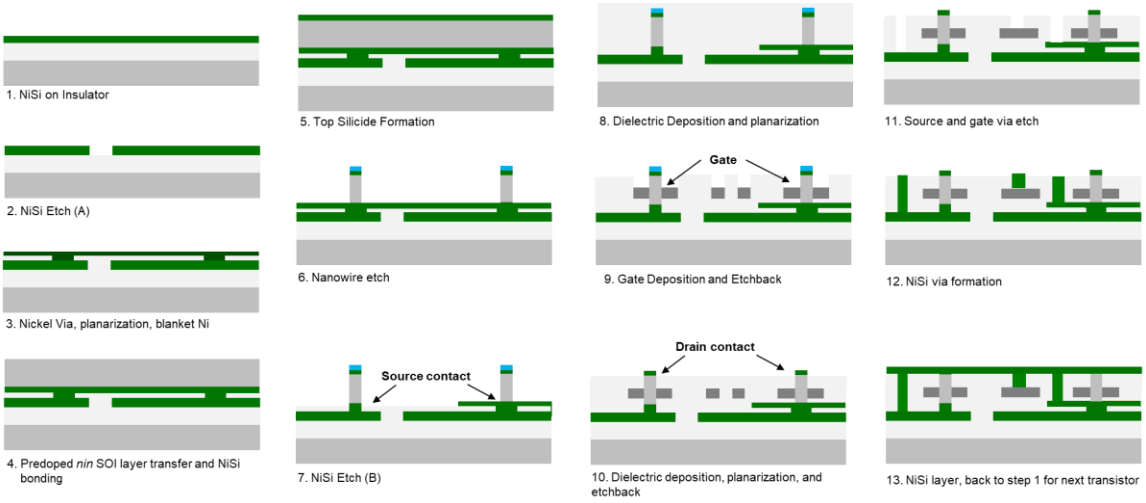

Figure 6. Nickel silicide bonding flow.

The critical nickel silicide bonding step is currently being developed in the Microelectronics Laboratory but electrical results are not yet available.

4. SILICON EPITAXY DEVELOPMENT

One fundamental challenge to vertical transistors is the formation of the abrupt junctions required in deeply scaled devices. Because the transistor is now vertical, ion implantation can no longer easily be used to dope the source, drain, extension, and channel regions. Instead, the dopants (typically boron and phosphorous) should be incorporated during growth of the constituent epitaxial layers. There are four aspects to this that result in process tradeoffs. First, high doping levels are required to reduce source/drain resistance. Second, complete—or nearly complete—dopant activation is required (interstitial dopants are electrically inactive). Third, the epitaxial silicon must be of very high quality with low defect density to ensure high mobility. Fourth, to support short gate lengths, on the order of 10 nm, the transition from highly doped to undoped silicon must be very abrupt, on the order of 1 decade of dopant concentration per 2 nm distance.

There are several processing trade-offs to consider during development of the epitaxial layers. For instance, increasing the growth temperature increases dopant activation and decreases defect density, which improves critical device parameters such as $R_{external}$ and channel mobility. But, high growth temperature accelerates dopant diffusion, which degrades control of the source/drain junction to the channel and increases parasitic capacitance. Developing a silicon epitaxy process that can address this conflict while still meeting the required device metrics has been a significant part of the effort this first year.

Development is being performed on the ASM Germanium Epitaxy tool that was installed in the Microelectronics Laboratory to support Ge detectors for integrated photonics. A silicon precursor (dichlorosilane) was installed and experiments performed to demonstrate *undoped* single crystal silicon growth first. This was successfully achieved (Figure 7). Undoped SiGe will be used as a sacrificial layer to isolate the six vertical transistors in the nanowire stack, and growth of $Si_{0.8}Ge_{0.2}$ was also successfully demonstrated (Figure 8).

Figure 7. ASM Epsilon epitaxy equipment and TEM of single crystal silicon film grown in the ML.

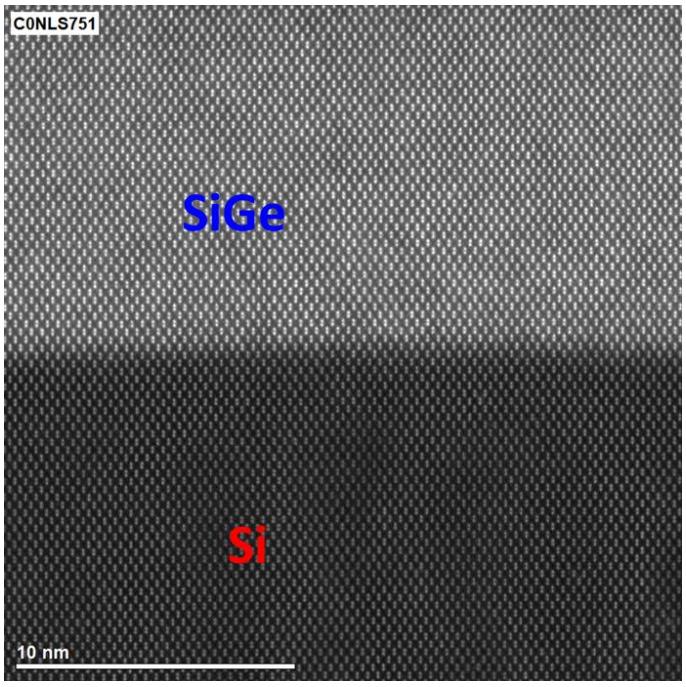

Figure 8. STEM-HAADF of SiGe epitaxial growth on silicon.

Demonstration of intrinsic epitaxial layers was followed by in-situ doping experiments, for boron (p-type) and phosphorous (n-type) dopants. Figure 9 shows an early attempt to grow a multilayer stack of these materials as would be required in the vertical logic implementation. The layers of the doped silicon "sandwich" are clearly visible in the TEM. Although visually appealing, the contrast between layers is indicative of relatively high defect density owing to the higher-than-necessary dopant concentrations in the Si:B layers at the substrate interface. The SIMS profile quantifies the dopant concentration (the electrically active dopant concentration may be less). Phosphorous doping is on the low end of the desired $1x10^{20}$ cm^{-3} to $5x10^{20}$ cm^{-3} range. The boron concentration is above this range. There is significant phosphorous diffusion into the intrinsic silicon region, though the boron stack appears less. This result is counterintuitive as boron is known to high higher diffusivity than phosphorous, and because the boron-doped stack is grown first, it experiences higher thermal budget. This suggests that the phosphorous contamination in the intrinsic region is due to external factors, most likely residual phosphorous on the walls of the deposition chamber that incorporates into film during intrinsic silicon growth. Improved layer separation by chamber cleans/purges was necessary.

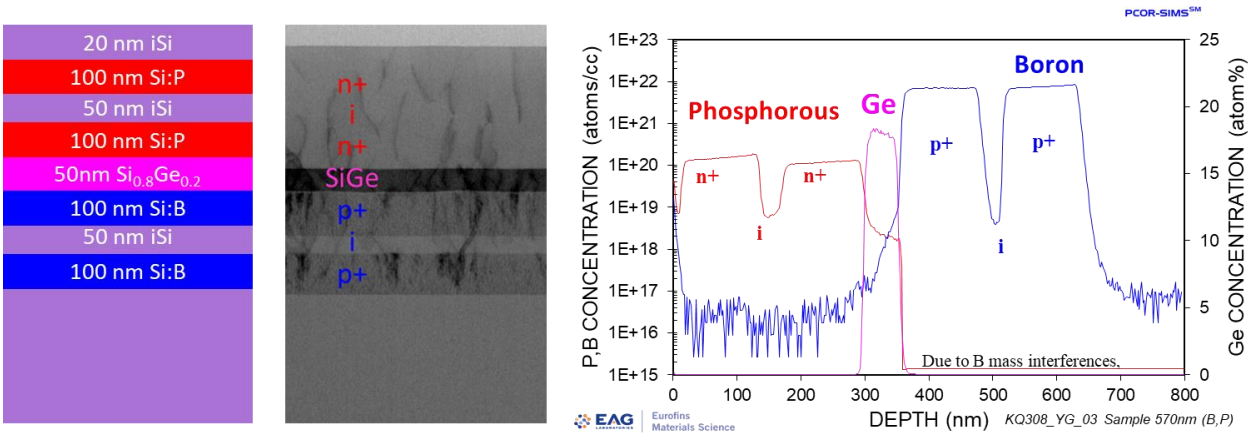

Figure 9. Initial doped silicon stack: schematic, STEM-BF, SIMS profile.

After further process optimization including protocols to reduce phosphorous contamination, the latest results given in Figure 10 were realized. The TEM images show less contrast between layers suggesting reduced defectivity. The phosphorous concentration has increased and the boron concentration has decreased as desired (though further reduction is planned). There is less phosphorous contamination in the instrinsic silicon layer as well. Though more work needs to be done to meet the device requirements (Section 5), these results are very promising.

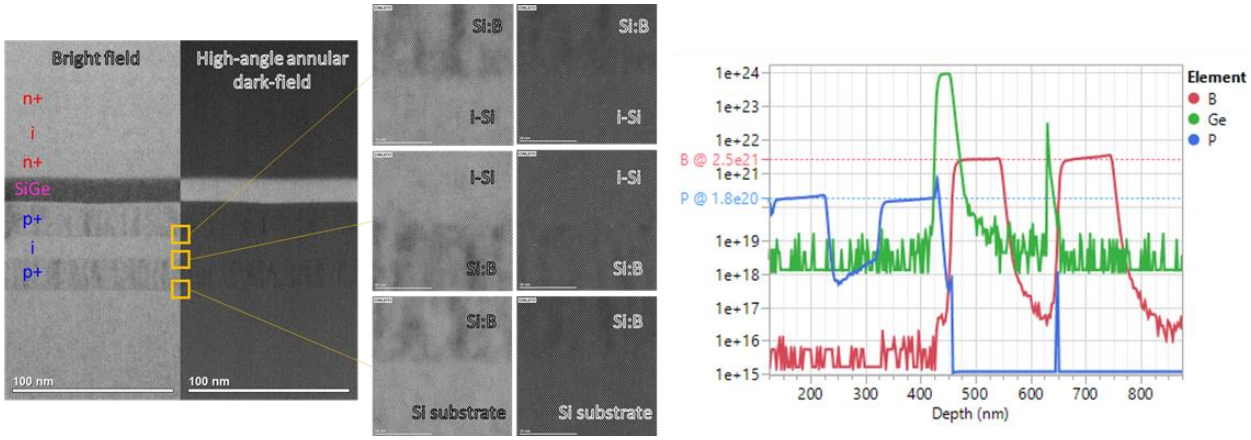

Figure 10. Improved doped silicon growth: STEM-BF, STEM-HAADF, SIMS profile.

5. SUMMARY AND OUTLOOK

Progress toward vertical logic devices has been made in several areas including cell design, capacitance modeling, candidate process flows, nickel silicide wafer bonding, and silicon nanowire growth. Two patent disclosures (Section 6) have been submitted related to the technology. At this time no serious and unanticipated technical challenges have been uncovered. But there is still a long road to complete vertical logic cell demonstration. In FY22, we are hopeful that we can develop process models to conduct virtual process experiments on a complete vertical logic device. We are also planning to develop full Design-Technology Co-Optimization (DTCO) models to estimate the performance of the logic cells leading to a reliable GOPS/W metric. Lincoln Laboratory does not have sophisticated process or DTCO modeling capability in-house so we are currently in discussions with outside vendors to develop the models. We anticipate electrical testing of nickel silicide test structures in FY22. Optimization of the silicon epitaxial process will continue, including novel approaches to reduce dopant diffusion such as exploring new silicon precursor gases. Single p/i/p and n/i/n vertical transistor fabrication is planned to begin risk reduction of gate and contact technology.

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6. PATENT DISCLOSURES

1. Steven Vitale, Jakub Kedzierski, “Vertical CMOS Logic” M.I.T. Case No. 23266L
2. Jakub Kedzierski, Steven Vitale, “Sequential Vertical Transistor Technology” M.I.T. Case No. 23264L

Note that both of these disclosures are “on hold” at the MIT TLO pending demonstration that the technology has been reduced to practice.

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13. ABSTRACT

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