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THESIS

MODELING AND CONTROL OF A MODULAR MULTILEVEL RECTIFIER

by

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March 2022

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MODELING AND CONTROL OF A MODULAR MULTILEVEL RECTIFIER

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requirements for the degree of

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ABSTRACT

Medium-voltage direct current (MVDC) systems will be the backbone of power systems in the future naval fleet due to its numerous benefits compared with the existing medium-voltage alternating current (MVAC) systems. The rectifier is a key component in an MVDC system that converts the AC electrical power from ship generators to DC power for further transmission and distribution. The power density, efficiency, and power quality of the rectifier are critical to successfully implement an MVDC system. The goal of this thesis is to further improve the benefits of a new rectifier topology, the modular multilevel rectifier (MMR), by designing and implementing control system improvements.

Using a real-time simulator, the MMR control system improvements were tested by simulating a system comprised of an MMR converting power from a 6.6 kV AC generator to a stable 12 kV DC bus. The various control improvements were tested against benchmark simulation results. This study shows that the control system improvements enhance the MMR power quality and reduce the number of required components making the MMR an ideal choice for naval MVDC systems.

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LIST OF ACRONYMS AND ABBREVIATIONS

AC	alternating current
GUI	graphic user interface
IGBT	insulated gate bipolar transistor
MMC	modular multilevel converter
MMR	modular multilevel rectifier
MVAC	medium-voltage alternating current
MVDC	medium-voltage direct current
PF	power factor
PI	proportional-integrational
PWM	pulse width modulation
Q	reactive power
qd0	quadrature-direct-zero reference frame
SM	submodule

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I. INTRODUCTION

U.S. naval vessel technology and future warship platforms aim to have greater capabilities, efficiencies, power density, and modularity than what exists in the U.S. fleet today [1]. The method of electrical power distribution used on future ships for use by various combat systems and electric propulsion will be a major decision that could limit or enhance future platform performance. Doerry's study [2] finds that medium-voltage alternating current (MVAC) power distribution systems currently used on U.S. naval vessels will not be able to effectively handle these future electrical power requirements. Therefore, a medium-voltage direct current (MVDC) distribution system will become the standard means of electrical distribution aboard naval vessels due to its increased efficiency and power density.

Traditionally, the U.S. Navy has used gas- or steam-powered turbines to drive an electric generator to produce alternating current (AC) power. Separately, similar turbines also provide the mechanical power for vessel propulsion. To implement a MVDC distribution system, the AC power produced from a generator must be converted from AC to DC, or rectified. Traditional power converters capable of the estimated power needs of a warship have serious drawbacks for shipboard use. A rectifier that is lighter, smaller, and modular will provide the most benefit to a warship. A new rectifier topology, the modular multilevel rectifier (MMR), has shown promise as the best option for shipboard use from research conducted in [3] and [4] due to its efficiency, power quality, and power density. The MMR is a derived rectifier topology from the well-studied modular multilevel converter (MMC). This study specifically examines and improves the MMR control system and verifies the operation through real-time simulations, proving that the MMR is the best candidate for a MVDC rectifier onboard future naval vessels.

A. SIGNIFICANCE OF RESEARCH

The MMR researched in this study would provide an efficient, space-saving method for rectifying the AC power from a ship generator into DC for use on an MVDC system. An MVDC distribution system offers substantial benefits to a naval vessel, and the MMR

is the key component to its performance. Doerry's research [5] shows that an MVDC distribution system offers greater efficiency, improved power density with space and weight savings, greater flexibility for planning and operation, and ease of electric propulsion integration.

An MVDC distribution system decouples the generators from a common bus frequency [5]. The MMR does not require a specific AC frequency for operation which allows the electrical generators to operate at their most efficient speed. These generators can also be designed differently. Smaller but faster rotating generators capable of similar power production can save space and weight onboard. Doerry [5] describes how multiple generators can even operate at different speeds from each other to maximize efficiency for their respective loads. The lack of a common bus frequency also reduces the ship acoustic signature, critical for naval vessels [2].

An MVDC system is simpler to operate because it only requires voltages to be matched to parallel sources [5]. This is much easier than an MVAC system that requires voltage, frequency, and phase to match. Additionally, Doerry's study [2] point out that an MVDC system has no reactive power component, meaning cabling can be made smaller for equivalent powers. The same study explains how an MVDC systems can also utilize common, solid-state transformers for changing voltage levels for specific equipment. MVDC distribution by itself offers efficiency and space savings, offering greater flexibility of ship design and payload options.

MVDC distribution allows electric propulsion to be more easily implemented on a naval vessel. Electric propulsion consists of an AC electric motor and a motor drive. The motor drive inverts DC power to AC power for use by the electric motor [6]. The motor drive can be connected through the MVDC distribution system, or to an MMR directly. Electric motors offer space, weight, and cost savings for the vessel [7]. Electric motors can be directly coupled to the propeller. Therefore, no bulky sets of reduction gears are needed which saves significant space and weight, improves propulsion system reliability, and allows the overall ship layout to be optimized because it is no longer necessary to place equipment along a shaft line. This allows for unconventional ship layouts that permit placement of motors and propellers at different angles, locations other than the stern, and

even the use of rotatable pods [7]. Separation of generators and electric motors is also possible and makes survivability of shipboard systems more likely with dispersed equipment.

Electric motors also offer incredible efficiency benefits for a naval vessel. U.S. Navy ships operate at a wide range of speeds. Traditional gas or steam turbines are most efficient only within a small window of their operating envelope. By contrast, electric motors can operate at around 95% efficiency over almost the entire band of their rated power [8]. This is very useful for warships which often patrol at slow speeds but require the ability to transit at maximum power from time to time. A similar benefit is the ability of electric motors to make large amounts of torque at low speeds. Traditional mechanical propulsion setups do not offer the near instant torque of an electric motor.

Without the need for propulsion turbines, the electrical load used for the electric motors is placed on the electrical turbines. There are multiple benefits that stem from this decoupling [9]. First, the overall number of prime movers is reduced. This allows a fewer number of overall turbines, all connected to an electrical generator, to be loaded closer to their rated values for extended periods of time. This allows the electric turbines to operate efficiently, which is when they are heavily loaded [10]. Second, fewer prime movers take up less physical space within the ship. Ships can be designed smaller with equivalent capabilities, or the layout altered for greater mission-oriented payload. Finally, the increased efficiency afforded by electric propulsion can provide greater vessel range compared to an equivalently powered system or allow ships to be designed smaller but with the same capabilities as current warships.

The MMR will be directly responsible for powering the MVDC distribution system. The MMR would allow full use of MVDC benefits, including electric propulsion, by future naval vessels.

B. RESEARCH METHOD

The control system of the MMR is critical for achieving its full potential operation and subsequent benefits. Currently, MMR control strategies have not been fully explored in previous studies conducted in [3] and [4]. This study aims to provide an improved control

system for the MMR with the main objective to achieve unity power factor (PF). As discussed in Chapter II, this enables the full space and weight savings of the MMR to be achieved by reducing the number of components compared to an MMC.

The system implemented in this research consists of a turbine driven, three-phase AC generator coupled to a stable DC bus by an MMR. A motor drive unit for the electric propulsion then inverts the DC to AC for use by an electric motor. Other shipboard systems are powered directly from the MVDC bus.

The MMR control system was improved by implementing idealized current commands from derived equations, reactive power (Q) feedback controls, and common mode voltage control. These control system changes were simulated using a real-time simulator. The control system proposed in this thesis improves the operation of the MMR, making this topology a better choice than an MMC for shipboard power rectification.

C. CHAPTER OVERVIEW

Chapter II discusses the topology and operating principles of the MMC. The MMR derived topology and operation are described in detail. Chapter III discusses the base control system used for the MMR. The specific improvements researched in this paper will be derived and discussed in detail. Chapter IV presents the chosen real-time simulator and associated software and hardware. Its benefits and basic operation will be examined. Additionally, the real-time simulator will be verified by testing an MMC model to ensure an MMR can be accurately modeled with the simulator. Chapter V presents the MMR model used for simulation in the real-time simulator. The results of the improved MMR control system will be presented. Finally, Chapter VI summarizes the simulation results and present ideas for future MMR research.

II. TOPOLOGY AND OPERATING PRINCIPLES

In this chapter, the basic topology and operation of the MMC is reviewed. A detailed description of the topology and operation of the MMR is then discussed. Understanding the MMC is vital to understanding the derived MMR topology and its operation. The key benefits of the MMR will be identified.

A. MODULAR MULTILEVEL CONVERTER REVIEW

The MMC is a mature voltage converter topology for high-voltage DC or MVDC applications. It offers modularity, scalability, low harmonics, high efficiency, and high reliability [11]. Additionally, MMCs are versatile, capable of conversions from AC-DC, DC-AC and AC-AC. The benefits of the MMC make it an ideal choice for the future of power conversion in many commercial and military applications [12]. The downside of the MMC is the increased energy storage requirement. When compared to a traditional multilevel converter, the MMC requires approximately three times the energy storage [4]. This leads to a lower power density, which is a negative attribute for naval vessel applications.

1. Topology

For a three-phase system, the MMC consists of three phase legs [13]. Each phase is split at a midpoint into two arms, an upper and lower arm, which connects one AC terminal to the DC terminal. Each arm contains multiple submodules (SM) and an inductor connected in series to help limit the current flow between phases. The SMs act as independently controllable voltage sources. Figure 1 shows the basic topology for a three-phase MMC in a configuration to rectify AC to DC.

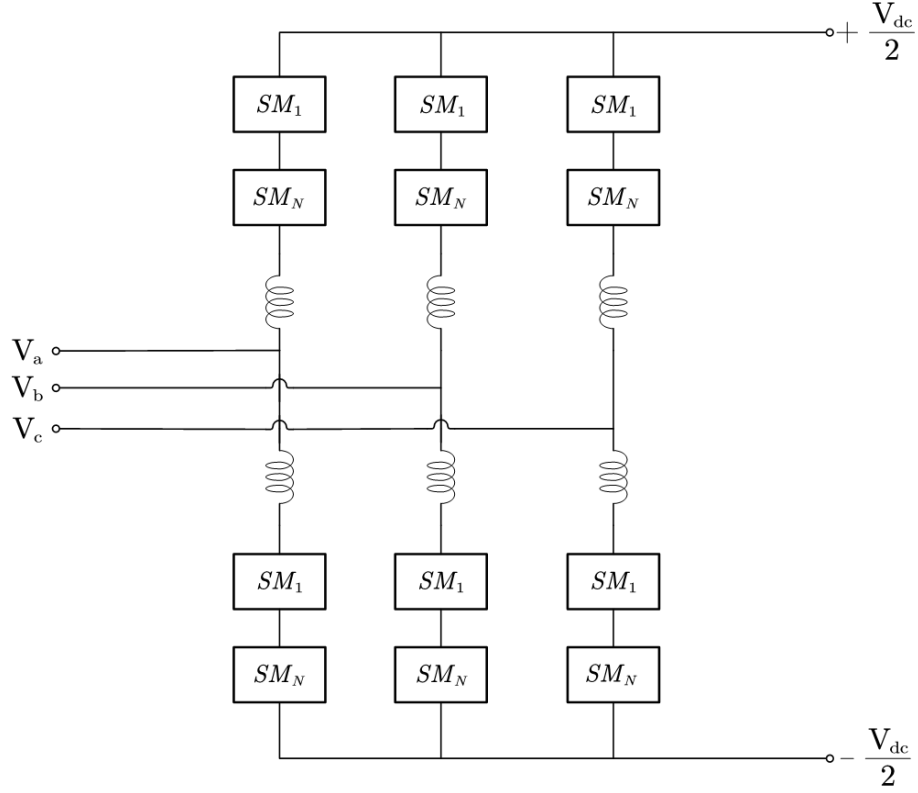


Figure 1. Three-phase MMC topology

2. Operation

The SMs are the heart of the MMC operation and are independently regulated by the MMC controller. The SMs can be a few different variations of topologies. The most popular is a half-bridge SM, shown in Figure 2, which consists of two semiconductor devices, such as insulated gate bipolar transistors (IGBT), connected in series [14]. The capacitor connected across the two IGBTs for energy storage allows the SMs to act as a voltage source, but it also contributes to increasing the volume and weight of the converter. The SM connection terminals are to the midpoint between the two IGBTs and the lower IGBT terminal. For this study, the upper IGBT is referred to as “S1” and the lower IGBT is referred to as “S2.”

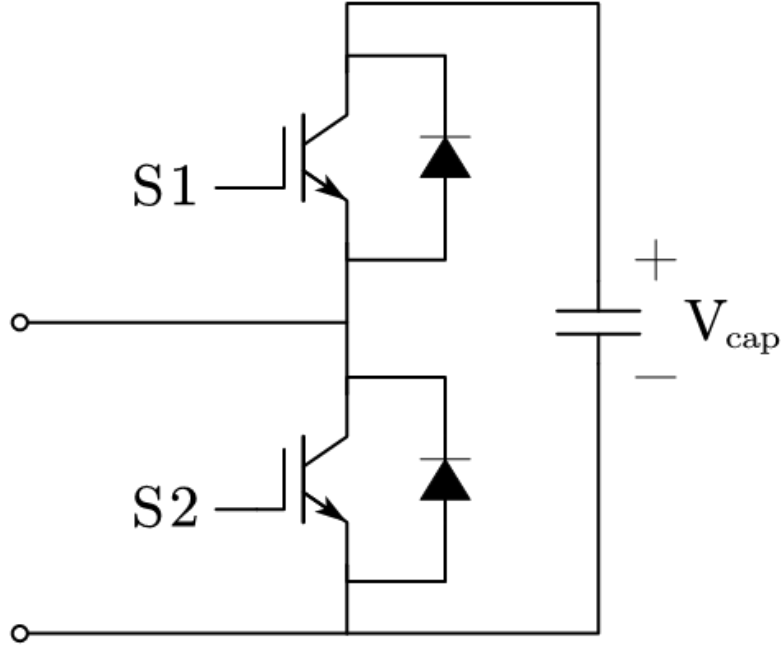


Figure 2. Half-bridge SM

Each SM produces two discrete voltages across its terminals which make each SM a controllable voltage source [15]. The half-bridge SM is controlled as a unipolar device so if S1 is on, then S2 must be off and if S1 is off, then S2 must be on. When S1 is on, regardless of the current direction, the voltage across the SM terminals will be equal to the voltage across the SM capacitor, V_{cap} . When S1 is off, regardless of current direction, the voltage across the SM terminals will be equal to 0 V [14]. Therefore, for N number of SMs connected in series per arm, the total arm voltage output can be in the range of 0 V to NV_{cap} . Figure 3 shows the state of an SM producing either 0 V or V_{cap} .

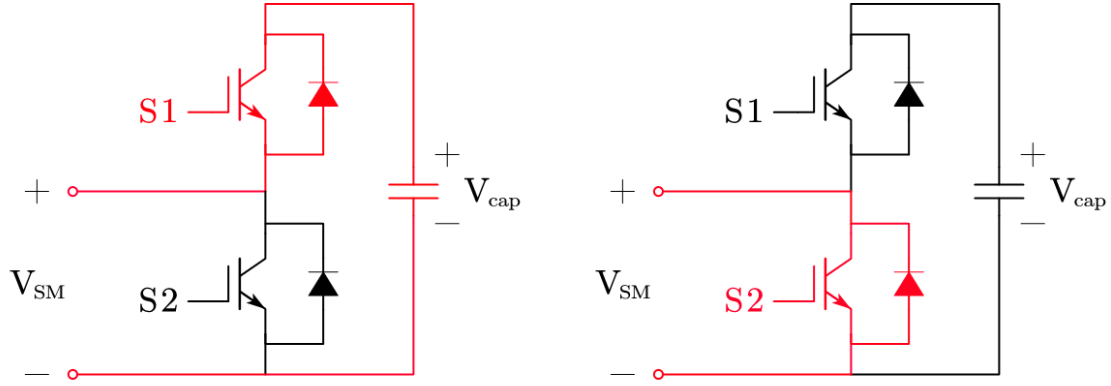


Figure 3. Half-bridge with S1 on (L), Half-bridge SM with S2 on (R)

The topology of the MMC can be simplified for modeling purposes by combining the series connected SMs of each arm into a single controllable voltage source. These single voltage sources are referred to with an “n” or “p” designator. For example, for a-phase, the upper arm voltage source is V_{pa} . The lower arm voltage source becomes V_{na} . This simplified model and nomenclature used throughout this study is shown in Figure 4.

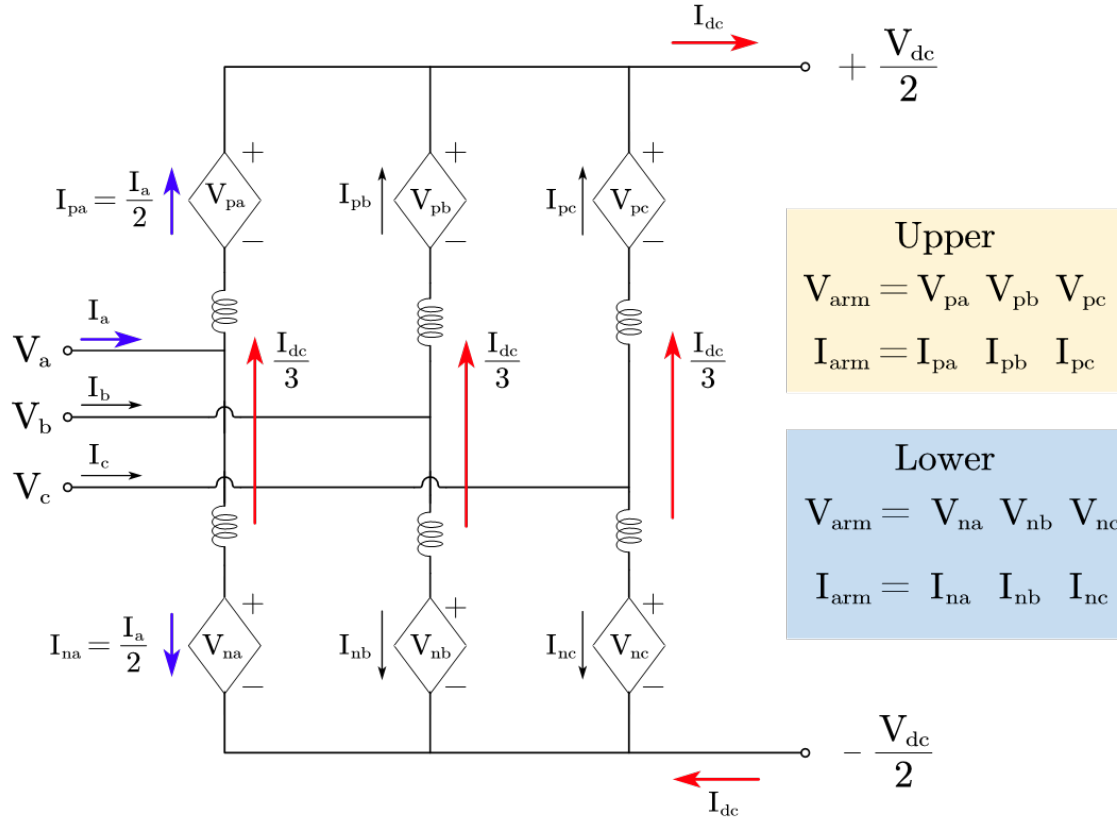


Figure 4. Simplified MMC model, nomenclature, and current flow

By using Kirchhoff's Voltage Law and assuming the voltage drop across the arm inductors is negligible, a set of equations relating the voltages of an MMC can be derived. The following equations are shown for the a-phase, but are similarly applied to all three phases.

$$V_{na} = \frac{V_{dc}}{2} + V_a \quad (1)$$

$$V_{pa} = \frac{V_{dc}}{2} - V_a \quad (2)$$

$$V_{na} + V_{pa} = V_{dc} \quad (3)$$

The current distribution of an MMC must be understood as well. Assuming ideal conditions, the AC phase currents $I_{a,b,c}$ are divided equally between the upper and lower arm of each phase. Additionally, the DC current I_{dc} is divided equally into thirds across the three phase legs. Therefore, using Kirchhoff's Current Law, the following equations are derived for the a-phase but can be applied to all three phases.

$$I_{pa} = \frac{I_{dc}}{3} + \frac{I_a}{2} \quad (4)$$

$$I_{na} = \frac{I_{dc}}{3} - \frac{I_a}{2} \quad (5)$$

Equations (4) and (5) are shown visually in Figure 4. The voltage and current equation derived above are necessary for implementing a control system for the MMC and are similar to those used in the design and implementation of the MMR control system examined in this thesis.

Although the MMC is capable of providing multiple different power conversions, this study only focuses on rectifying AC-DC. To rectify AC-DC, each of the six arms must provide voltage in a particular magnitude and time as to maintain a stable DC voltage. Figure 5 shows how the upper and lower arm voltage of one phase work together to produce constant DC voltage.

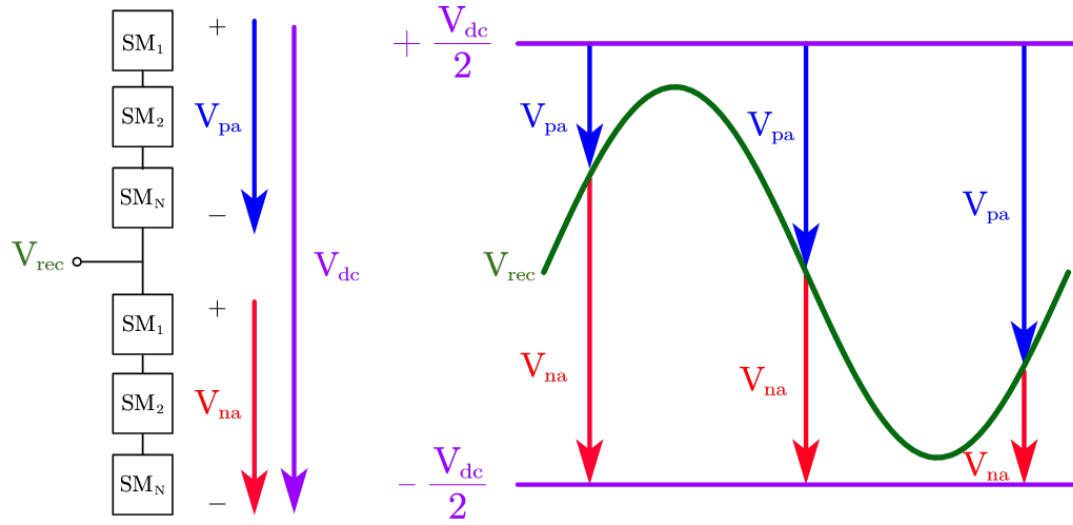


Figure 5. MMC voltage relationships and general operation

When compared to other voltage converters, the MMC is unique in that there are circulating currents within the phases of the converter, as shown in Figure 6. These circulating currents must be limited by the controller. Unbalanced current flow leads to an uneven amount of charging and discharging of the SM capacitors. This leads to challenges concerning device ratings, V_{cap} ripple, and efficiency of the converter.

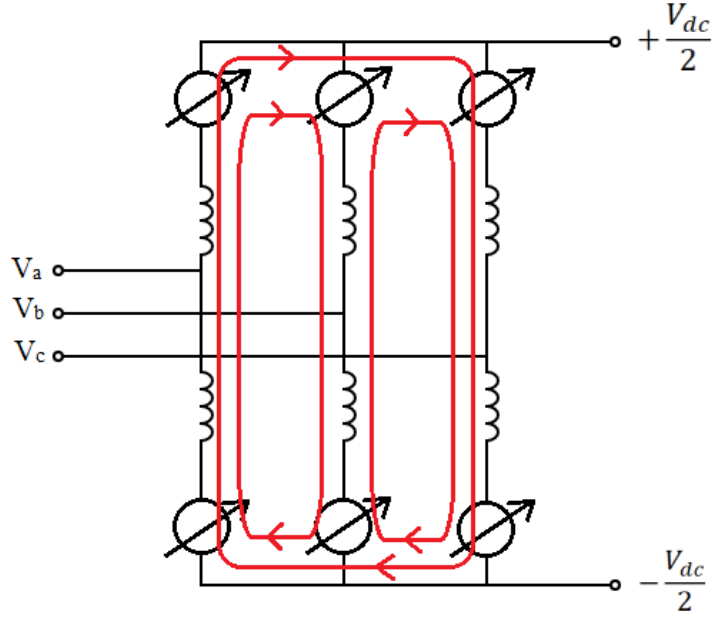


Figure 6. MMC circulating currents

To prevent degraded MMC performance, the SM capacitor voltages must be balanced. This topic has been researched extensively and is not the focus of this paper. The most simple technique of capacitor voltage balancing, known as “sorting” was used in this research and will be briefly discussed [16], [17]. The goal of sorting is to arrange each SM of each arm in either ascending or descending order based on the arm current polarity. Sorting does not dictate how many SMs are “on” or “off.” It only determines which SMs are on or off based on the required amount from the pulse width modulation (PWM) output. For reference, Table 1 provides a summary of how an SM responds based on the current polarity and its state.

Table 1. SM states. Source: [18]

S1	S2	V_{SM}	I_{SM}	SM state	Capacitor
ON	OFF	V_{cap}	> 0	ON	Charging
ON	OFF	V_{cap}	< 0	ON	Discharging
OFF	ON	0	> 0	OFF	Unchanged
OFF	ON	0	< 0	OFF	Unchanged

The sorting algorithm is simple however its downside is the increase in switching losses due to the frequent switching of the SMs as their sorted order changes in time. To reduce switching losses, the sorting algorithm can be executed every few switching cycles. This technique was used in both the MMC and MMR simulations presented in this thesis.

B. MODULAR MULTILEVEL RECTIFIER OVERVIEW

The MMR topology is derived from the MMC with the addition of a set of four diodes added to each phase leg [4]. The major benefits of the MMC are retained with the MMR, which is modularity, scalability, efficiency, reliability, and excellent harmonic performance. This study will show that the MMR offers exceptional power quality for AC-DC rectification while reducing the number of SMs by up to half.

1. Topology

Like the MMC, the MMR contains three phase legs that connect each AC terminal to the DC terminal through an upper and lower arm. Each arm consists of an inductor and multiple half bridge Si IGBT SMs connected in series. The major feature of the MMR topology are the diode stacks. Each phase receives one diode stack, made of 4 diodes, for a total of 12 diodes for a three-phase system [4]. As seen in Figure 7, the upper arm of each phase connects to the cathode and anode of two diodes and the lower arm of each phase also connects to the anode and cathode of two other diodes. All four of these diodes are connected in series with a midpoint connection between each phases 2nd and 3rd diode. D₁ and D₄ connect the DC bus to the phase arms. For this study, the diode stack is comprised of silicon (Si) diodes.

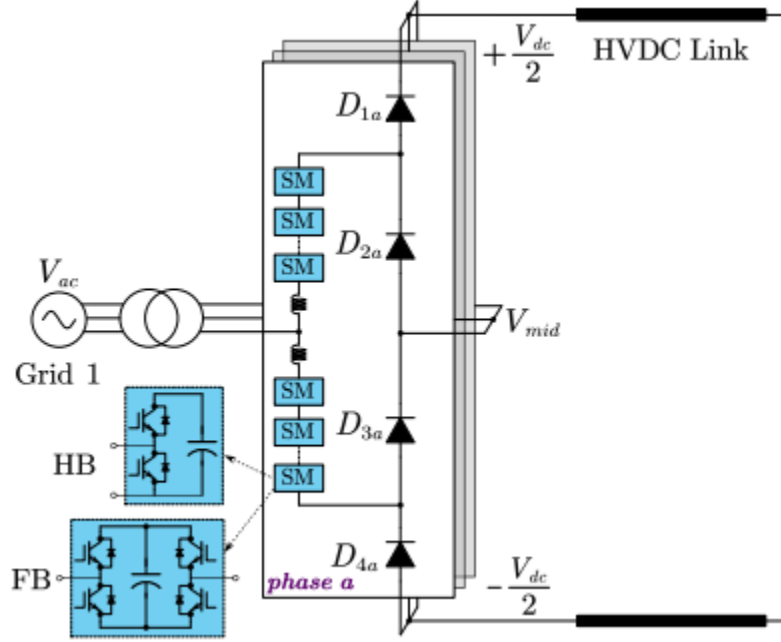


Figure 7. MMR topology. Source: [4].

2. Operation

The MMR operation cannot be treated like the MMC, although there are similarities. The state of the diodes within each diode stack is determined only by the polarity of the current [4]. The state of the MMR itself is what determines which diodes in the diode stack will be conducting or not. Therefore, each phase of the MMR has three distinct modes of operation, shown in Figure 8. Each phase of the MMR can either be in a positive “P,” negative “N,” or zero “Z” state [4]. Thus, for a three-phase system, there are 12 possible states for the MMR.

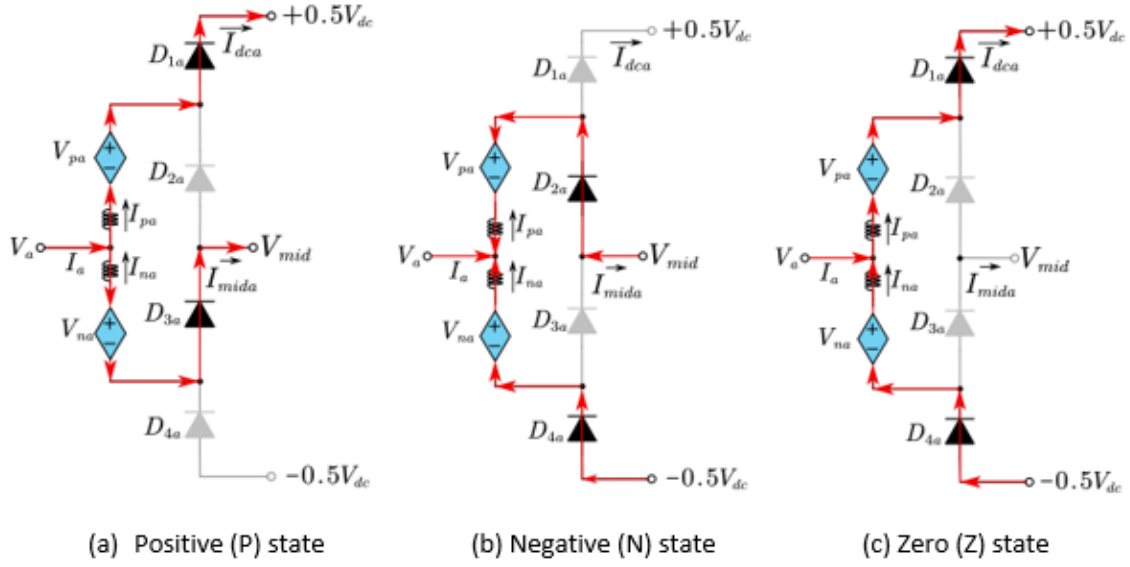


Figure 8. MMR phase states. Source: [4].

As seen in Figure 8, the P state is obtained when both the AC voltage and AC current are positive. D_1 and D_3 are conducting and the phase is connected to the midpoint. The N state is obtained when both the AC voltage and AC current are negative. D_2 and D_4 are conducting and again the phase is connected to the midpoint. The Z state is defined for when the polarity of the AC voltage or AC current is not well determined, such as crossing zero. In the Z state, diodes D_1 and D_4 are conducting and the phase is not connected through the midpoint.

Much like the MMC, a base set of equations relating the MMR voltages can be derived using Kirchhoff's Voltage Law. However, each phase has a separate set of unique equations depending on which state, P, N, or Z, it is in. The nomenclature for the single modeled controllable voltage source of each phase, comprised of the series connected SMs of an arm, are the same as shown in Figure 4. The midpoint connection voltage of the diode stacks V_{mid} is depicted in Figures 7 and 8. Each of the following equations is applicable to all three phases.

For P state:

$$V_{na} = V_a - V_{mid} \quad (6)$$

$$V_{pa} = \frac{V_{dc}}{2} - V_a \quad (7)$$

For N state:

$$V_{na} = \frac{V_{dc}}{2} + V_a \quad (8)$$

$$V_{pa} = V_{mid} - V_a \quad (9)$$

For Z state:

$$V_{na} = \frac{V_{dc}}{2} + V_a \quad (10)$$

$$V_{pa} = \frac{V_{dc}}{2} - V_a \quad (11)$$

The different states of each phase introduce a complexity that an MMC-based controller cannot handle. As a visual aid for the added complexity, as well as an overview of how the phase states interact, Figure 9 shows the MMR states over a full line cycle.

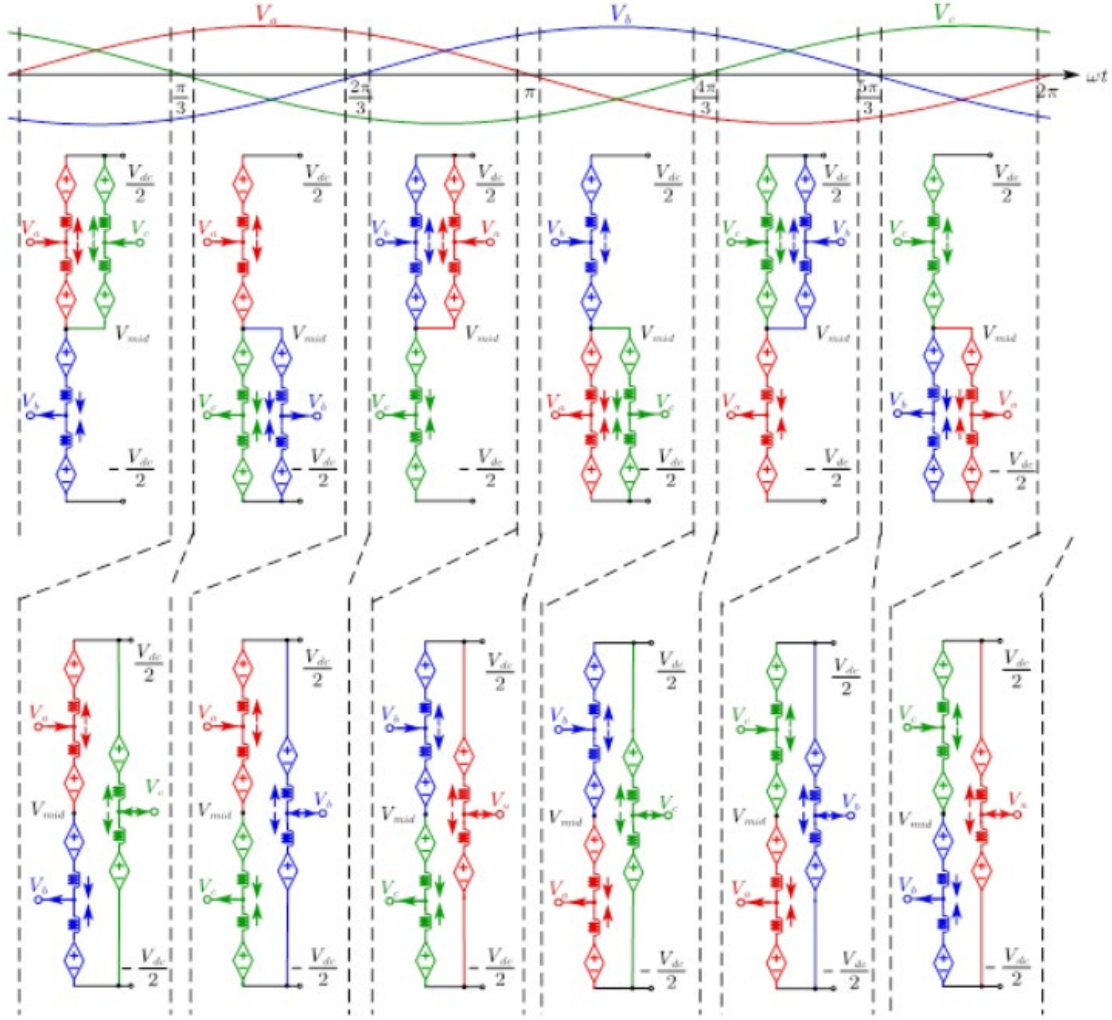


Figure 9. Three-phase MMR phase states over one line cycle. Source: [4].

While Figure 9 presents a control problem, it also illustrates the main benefit the diode stacks provide for the MMR. The midpoint across the diode stacks allows the phases to interact. For an MMC, each phase is only connected in parallel across the DC bus. The DC bus voltage must be blocked by only the two arms of each phase. But, for an MMR, the phase arms can become connected in series across phases through the midpoint. Therefore, at any time there are two phases connected in series. In other terms, the DC bus voltage is blocked by up to four arms. This feature is what allows the MMR to operate with half of the SMs as an MMC for an identically rated system.

The MMR benefit of 50% SMs, as compared to an MMC, is fully realized when the MMR operates at unity PF. Examining a single phase in the Z state provides further insight why unity PF for an MMR is important. For example, if the MMR is operating at a lagging PF, then the AC phase current I_a will lag AC phase voltage V_a . In this case, when V_a crosses the zero line and become positive, I_a will still be negative. As shown previously, the state of the MMR is determined only by current polarity because the diode stacks cannot be actively controlled. For this example, equation (10) is now:

$$V_{na} = \frac{V_{dc}}{2} + (V_a > 0) \quad (12)$$

The upper arm in the a-phase must now block more than half of the DC bus voltage. This would require more SMs or SMs with higher voltage ratings. For the same situation, at unity PF, V_a will equal zero when I_a equals zero. Therefore, the upper arm in the a-phase is only responsible for blocking half of the DC bus voltage.

The MMR studied in [3] and [4] shows promise as a future choice for shipboard rectification in an MVDC distribution system. The complex nature of the topology calls for a robust control system that has not yet been studied. Therefore, this thesis aims to improve the MMR controller by specifically designing and implementing PF controls so the MMR can operate at unity PF over a variety of operating conditions as well as provide controls to mitigate adverse effects when unity PF is not perfectly achieved.

III. MMR CONTROLLER IMPROVEMENTS

This chapter presents the improvements to the MMR control system originally implemented in [3] by Kinney. First, an overview of Kinney's control system will be presented. The specific improvements to the control system will then be derived and examined in detail. The improvements discussed in this chapter aim to maximize the MMR benefits presented in Chapter II. The controller improvements are designed to operate the MMR at unity PF to reduce the arm voltage stress to half of the DC bus voltage allowing the number of SMs to be reduced by half compared to an MMC.

A. MMR CONTROLLER REVIEW

The objective of this thesis is to improve the base MMR controller implemented in [3] and shown in Figure 10.

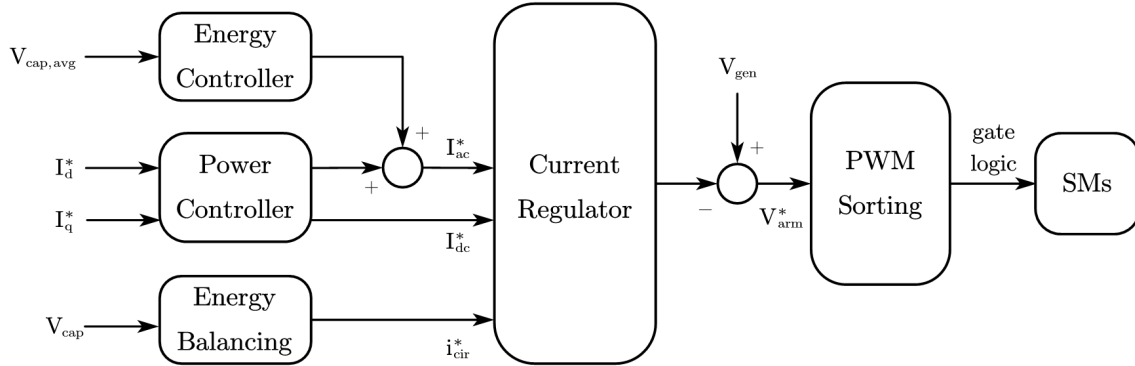


Figure 10. Base MMR control system

The MMR controller shown in Figure 10 includes feed forward controls, DC current I_{dc} controls, and I_{arm} controls. The AC current is controlled by proportional-integral (PI) controllers in the quadrature-direct-zero ($q d 0$) synchronous reference frame and then converted back to the abc frame. I_{dc} controls and I_{arm} controls provide additional input to the final voltage command. The final voltage command is fed into low level controls where pulse width modulation (PWM) is used to enable the switching of each individual SM in each arm. The controller in [3] was successful at balancing phase circulating currents,

managing the phase states, and providing I_{dc} to the DC bus, however it did control PF, limiting the MMR potential performance and benefits by not actively reducing the V_{arm} .

B. UNITY PF CONTROLS

The MMR control system improvements designed for this study are threefold. First, the feed forward portion was idealized by using equations to calculate the current commands instead of using a set value. Second, Q feedback controls were created to drive the MMR Q to zero. Finally, a common mode voltage control was inserted to improve the MMR performance when the PF is not perfectly at unity, such as transients or dynamic conditions. These three separate portions were added to the base MMR controller presented in [3] and shown in Figure 10.

The controller was modeled in Simulink for use in the real-time simulator, which is discussed in Chapter IV. Both Simulink blocks and C code were used to carry out all functions of the controller. The Simulink blocks were used because they are convenient for design and troubleshooting. The C code was used for phase state specific controls because the controller must respond differently in each phase as previously discussed in Chapter II.

The general system used in design is illustrated in Figure 11. It consists of a three-phase AC generator, the MMR, and a stable DC bus. Resistors and inductors are added in series in each phase to model the non-ideal generator.

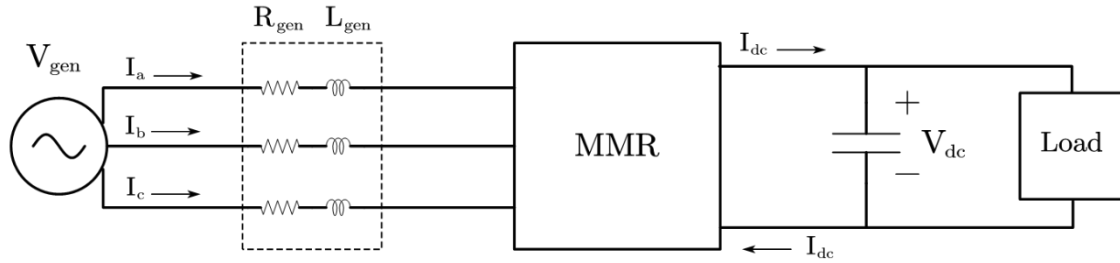


Figure 11. MMR system circuit diagram

1. Feed-Forward Control Based on Model Parameters

In [3], basic feed forward was used to convert a current command to a voltage command. This thesis sought to improve the open loop portion by idealizing the current commands by using basic assumptions about the system and known system relationships. Most of the control system is implemented in the $qd0$ reference frame, which rotates with the AC voltage and AC current waveforms. This allows the waveforms to be stationary and can then be represented as DC signals in the synchronous reference frame which simplifies the control system calculations by removing the frequency component.

The first assumption used to derive the ideal current commands is that the three-phase generator AC voltage V_{gen} is known. Additionally, the generator is operating at unity PF where the phase angle θ is equal to zero degrees. Finally, the power required by the DC bus loading P is known. With these assumptions, the idealized current commands can be derived. In the $qd0$ reference frame, the current commands are i_q^* and i_d^* .

In the phasor domain, assumptions one and two provide the generator voltage. It is equal to $V_{gen}\angle 0^\circ$. To convert $V_{gen}\angle 0^\circ$ into the $qd0$ domain, the following equations are required.

$$V_{d,gen} = |V_{gen}| \sin \theta \quad (13)$$

$$V_{q,gen} = |V_{gen}| \cos \theta \quad (14)$$

Evaluating Equations (13) and (14) respectively yields:

$$|V_{gen}| \sin 0 = V_{d,gen} = 0 \quad (15)$$

$$|V_{q,gen}| \cos 0 = V_{q,gen} = V_{gen} \quad (16)$$

The generator voltage is now equal to zero in the d-axis and V_{gen} in the q-axis. Next, the power equation was used to relate P and the currents i_d and i_q . The power equation in the $qd0$ reference frame is:

$$P = \frac{3}{2}(V_d I_d + V_q I_q) \quad (17)$$

After substituting, we are left with:

$$P = \frac{3}{2}(V_{gen} I_q) \quad (18)$$

For usage in the MMR control system, equation (18) is rearranged. P becomes the input power command P^* and the output is i_q^* as shown in equation (19).

$$I_q^* = \frac{2P^*}{3V_{gen}} \quad (19)$$

The controller is now able to convert a single P^* and output the ideal i_q^* as shown in Figure 12. The ideal i_d^* is still unknown.

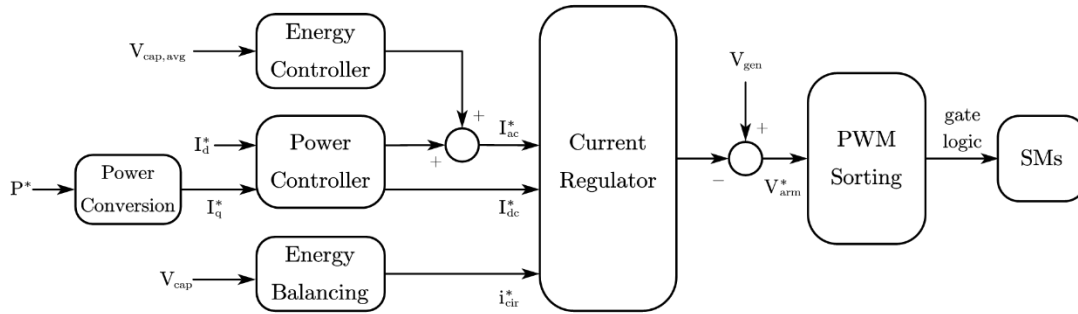


Figure 12. MMR control system with active power command

Kinney used a constant value of zero for the i_d^* in his research. This was improved upon in this thesis by analyzing the portion of the simplified system of Figure 11 between the generator and the MMR SMs as shown in Figure 13.

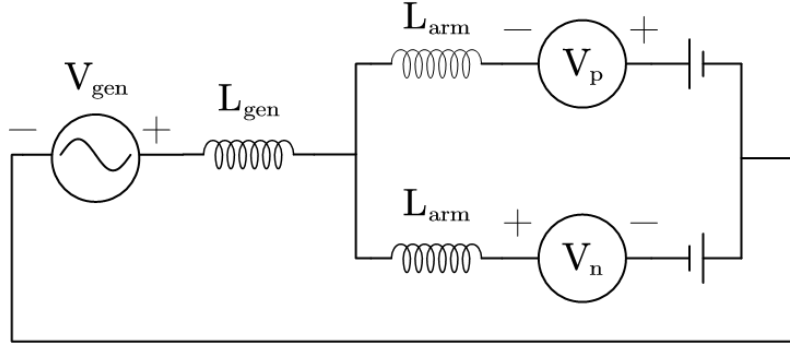


Figure 13. MMR single-phase representation

Figure 13 displays the generator voltage V_{gen} , the MMR upper and lower arm voltages represented as a controllable source, V_p and V_n , the generator inductance L_{gen} and the MMR arm inductance L_{arm} . Figure 13 was used to calculate an equivalent system reactance X between the generator and the MMR SMs. Combining the inductances and applying the electrical frequency f_{gen} the estimated system reactance was calculated as follows:

$$X = (L_{gen} + \frac{L_{arm}}{2})2\pi f_{gen} \quad (20)$$

By combining the inductances, Figure 13 was further simplified into a single-phase representation of the modeled system between the generator and the MMR. V_p and V_n combine to form V_{rec} . This representation is shown in Figure 14 and was used to calculate the ideal i_d^* .

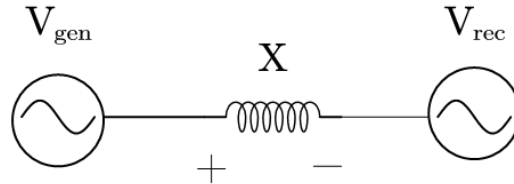


Figure 14. MMR simplified single-phase representation

The ideal i_d^* was computed by simultaneously solving a set of three equations. The set of equations was generated by first conducting a voltage analysis of the system in Figure 14. In the phasor domain, V_{rec} can be solved for as follows:

$$V_{rec} = V_{gen} - jXI \quad (21)$$

Equation (21) was transferred into the $qd0$ reference frame using the following transformation [19]:

$$\begin{bmatrix} f_q \\ f_d \\ f_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos \theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin \theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \quad (22)$$

Resulting in:

$$V_{d,rec} = V_{d,gen} - XI_d \quad (23)$$

$$V_{q,rec} = V_{q,gen} + XI_q \quad (24)$$

Equations (23) and (24) are the first two equations out of the set of three. The last equation in the set is derived from equations (23) and (24) by assuming that voltage and current are in phase which results in:

$$\frac{V_{q,rec}}{V_{d,rec}} = \frac{I_q}{I_d} \quad (25)$$

Therefore, recalling that $V_{d,gen}$ is zero, i_q is the i_q^* , and solving equations (23), (24), and (25) simultaneously for i_d^* yields:

$$\frac{-XI_q^*}{V_{q,gen} + XI_d^*} = \frac{I_d^*}{I_q^*} \quad (26)$$

Further simplification leads to:

$$-XI_q^{*2} = V_{q,gen}I_d^* + XI_d^{*2} \quad (27)$$

Applying the quadratic formula to solve for i_d^* yields the following:

$$I_d^* = \frac{-V_{q,gen} \pm \sqrt{V_{q,gen}^2 - 4XI_q^{*2}}}{2X} \quad (28)$$

The only possible solution for equation (28) is the addition result from the quadratic formula.

Now, from a single power command, the ideal i_d^* and i_q^* are calculated and fed into the rest of the controller from [3]. The improved ideal feed forward current commands portion of the MMR control system is shown in Figure 15.

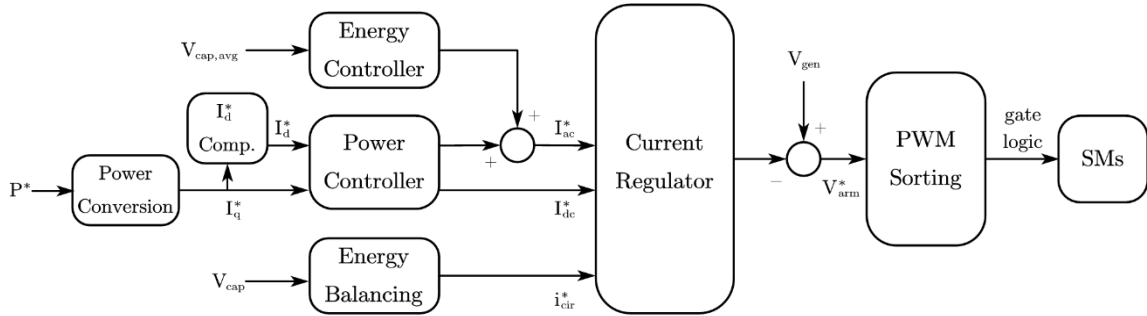


Figure 15. MMR controller with ideal feed forward controls

The current commands should be able to operate the MMR closer to unity PF than just a constant i_d^* . However, because the commands are made with multiple assumptions, further controls are required. Therefore, Q feedback controls were derived and implemented. The relative phase angle between the MMR AC voltage and AC current can be obtained in degrees by monitoring system signals. However, this tactic would be slow because of the trigonometric functions. Additionally, trigonometric functions may insert unwanted singularities from sign convention or operating near 0 or 90 degrees. Instead, an

approach to use Q was developed. Q represents the reactive power of a system. If the MMR Q is zero, then the MMR apparent power and real power will be equal. This is the same as saying the MMR is at unity PF. In the $qd0$ reference frame, Q is calculated by:

$$Q = \frac{3}{2}(I_d V_q - I_q V_d) \quad (29)$$

The PF controls were implemented by first calculating the system Q . The voltage commands V_d^* and V_q^* , as well as the current feedback $i_{d,fb}$ and $i_{q,fb}$, were used to calculate the system Q . This value was then referenced to zero and sent to an integrator. The decision to use current feedback was to provide real system data to obtain a faster response from the controller. Figure 16 shows the Q feedback controller integrated into the MMR controller along with the previously discussed ideal feed forward controls

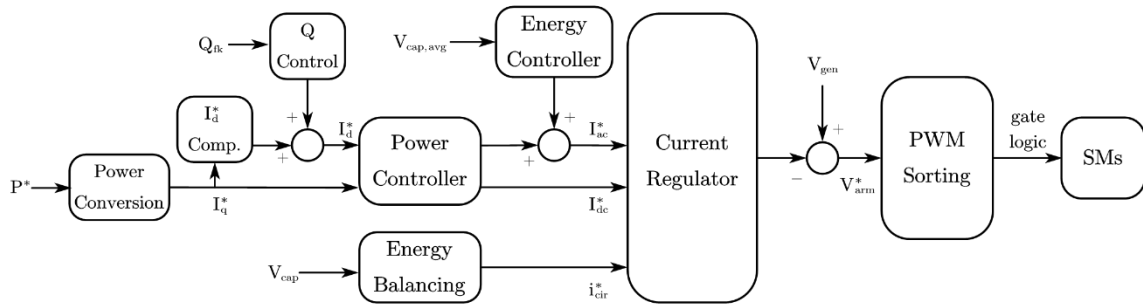


Figure 16. MMR controller with Q feedback and ideal feed forward controls

The output of the Q feedback controller was added into the output of the i_d^* signal discussed earlier in this section. The Q feedback controller output is added to the i_d^* signal so it can adjust the ideal command for the MMR real operating condition and account for any imperfections in the assumptions made while deriving the current commands.

2. Common Mode Voltage Control

Common mode voltage control was introduced in this new MMR controller as a means to improve the MMR performance specifically when it is not operating at unity PF. During transients or any period of time when the PF controls of Chapter III.A have not

adjusted the PF to unity, the common mode voltage controls will provide temporary assistance to improve the MMR performance.

The purpose of the common mode voltage control is to provide temporary assistance by holding the AC voltage of one phase at zero when there is a mismatch between the MMR AC voltage and AC current polarity. For example, if the MMR is operating at a lagging PF, then current will cross zero after voltage. In this case, the voltage will be a different polarity than the current and will resist the flow of current until current also crosses zero. This will lead to current distortion and poor performance. By holding the AC voltage at zero until the AC current also crosses zero, there will be no opposing stress placed on the current which will help limit any adverse effects when the MMR is not at unity PF.

The common mode voltage control was implemented within the C code portion of the controller because these controls are only necessary when a phase is in the Z state. Access to specific states is conducted within the C code. Additionally, the common mode voltage control is equated in the abc reference frame. The control works by first identifying when any phase is in the Z state. When a phase is in the Z state, a common mode voltage, V_{cm} , is calculated as follows:

$$V_{cm} = -V_{cmd} \quad (30)$$

V_{cmd} is the voltage command that is output from PI controllers referenced in Chapter III.A. The V_{cm} is then added to V_{cmd} as follows:

$$V_{out} = V_{cmd} + V_{cm} \quad (31)$$

V_{out} is now a new, temporary voltage command that will be equal to zero. Once the associated phase AC current and AC voltage are the same polarity, the common mode voltage controls are no longer active.

For any time where a phase is not in the Z state, V_{cm} is equal to zero. Additionally, because the studied MMR is for a three-phase system, V_{cm} is applied to all phases equally. The final result is that the voltage command of the affected phase is held at zero until

current also passes zero. The voltage command then returns to its unmodified value for that time. This prevents any distortion or unwanted forces on the MMR phase currents. A flowchart of the common mode voltage controller is shown in Figure 17 and an example of how the common mode voltage control changes the commanded voltage is shown in Figure 18.

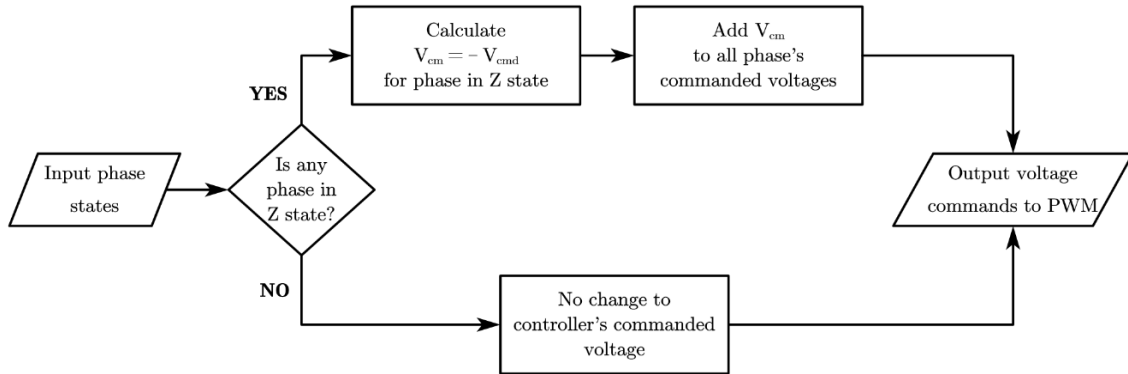


Figure 17. Common mode voltage control flowchart

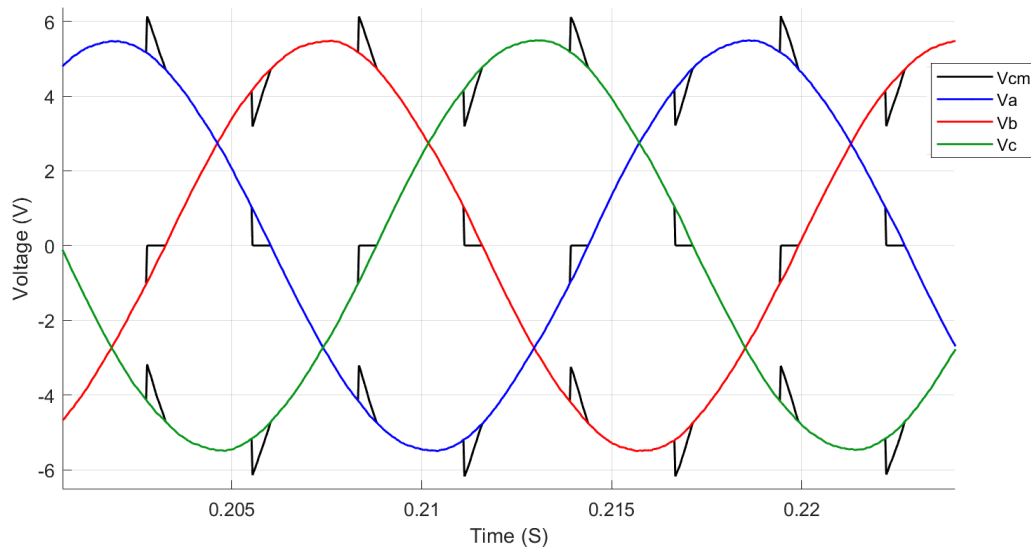


Figure 18. Common mode voltage control example

The common mode voltage control example in Figure 18 represents a three-phase AC system where the AC current is leading the AC voltage. Looking at the upper and lower

peaks of a single phase, it is shown how the V_{cm} controls for the other two phases are also applied. However, when the other two phases are in the Z state, the AC current and AC voltage will always be the same polarity because it is a balanced three-phase system.

In summary, the control system improvements to the MMR presented in this paper are the ideal feed forward i_d^* and i_q^* , the Q feedback controls, and the common mode voltage controls. The ideal current commands and Q controls are designed to operate the MMR at unity PF while the common mode voltage control is designed to reduce negative effects when the MMR is not at unity PF for any reason. The final improved MMR control system is shown in Figure 19.

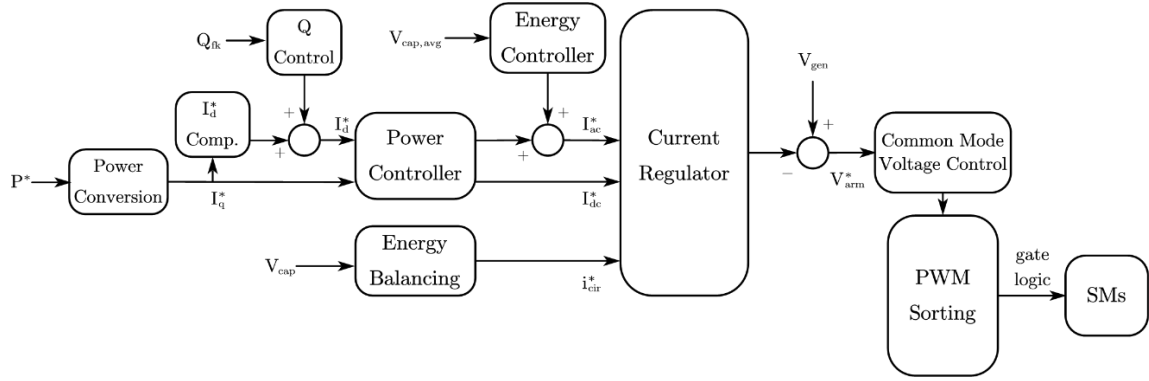


Figure 19. Final improved MMR controller

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IV. REAL-TIME SIMULATOR

This chapter presents the real-time simulator software and associated hardware from OPAL-RT. The benefits of real-time simulation, model requirements, and hardware specifications will be presented. Finally, the real-time simulator will be used to simulate an MMC converting AC to DC.

A. OPAL-RT RT LAB

Real-time simulation is a modeling practice that aims to have the simulation time be equal to real world time. For this thesis, OPAL-RT RT Lab software was used in conjunction with the OPAL-RT OP5707XG hardware. To progress the future work and study of the MMR and understand the MMR real-time performance, the OPAL-RT RT Lab software was chosen to model the MMR. Real-time simulation has three main benefits for this research and future research of the MMR. First, complex models, such as an MMR, can be simulated much faster boosting the efficiency of testing. Second, the RT Lab software is easily scalable. For example, adding more SMs in an MMR model is easy to do and does not slow down simulation speed. Finally, the real-time simulator provides the groundwork for future research by providing capabilities to conduct hardware in the loop simulations using the OP5707XG I/O ports.

RT Lab uses Simulink models as the input to the software. Specific model and simulation setting are required. The following subsections provide details on how models must be changed and what simulation settings must be used. These details also provide an understanding of how the real-time simulator works.

1. Subsystems

RT lab interacts with Simulink models for real-time simulation but requires specific modifications before use. RT Lab needs all portions of a model be placed within a subsystem. The topmost layer of the Simulink model must consist of only the subsystems discussed in this paragraph. The subsystems are specific and require distinct nomenclature. The main purpose of the subsystems is to separate the model between computational and

graphic user interface (GUI) nodes [20]. They also assign the computational nodes to different CPU cores on the OPAL5707XG. Any portion of a model that needs to be seen or interacted with by the user must be put into a single GUI subsystem. Any portion of the model that is computational in nature must be placed in a computation subsystem. The GUI subsystem must be named in the following format: “SC_anyName.” Computational subsystems must be named in the following format: “SM_anyName” or “SS_anyName.” There must be at least one SM subsystem per model. Any additional computational subsystems must be of a SS designation. Allowable subsystem configurations are shown in Figure 20.

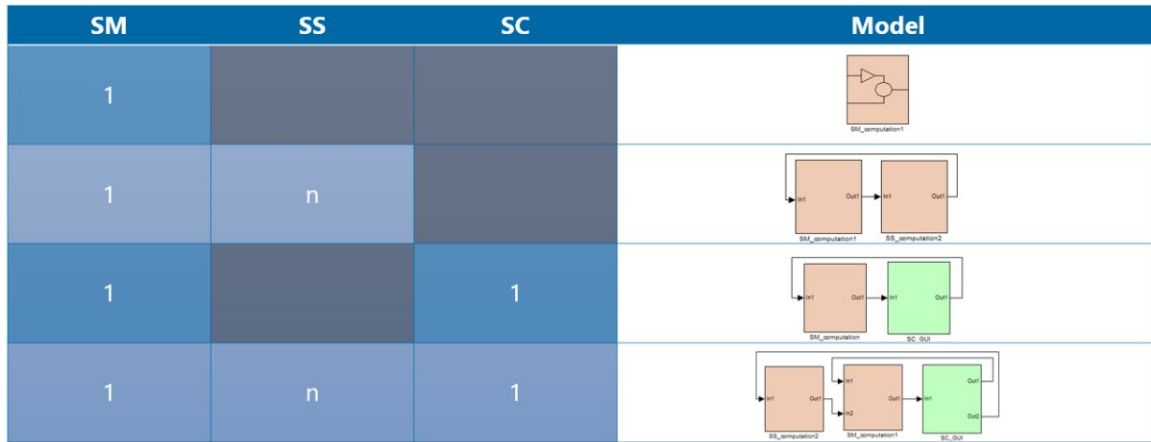


Figure 20. Allowable RT Lab subsystem configurations. Source: [20].

The subsystem designations tell the RT Lab software how to distribute the model between the host computer and the OP5707XG during simulation. The GUI subsystem is run and displayed from the host computer. The other computational subsystems are run from the OPAL hardware CPU cores. This allows for optimal performance and enables the real-time capabilities. The SC and SS subsystems are further optimized because each is run on a separate core on the OPAL 5707XG.

The top layer of an MMC model, simulated for software and hardware verification later in this chapter, is shown in Figure 21. Only one SM subsystem was used because the RT Lab license held only allows for one core in the OP5707XG to be active. Other

subsystems may be used within the SC, SS and SM subsystems and have the same functionality as a normal Simulink model subsystem.

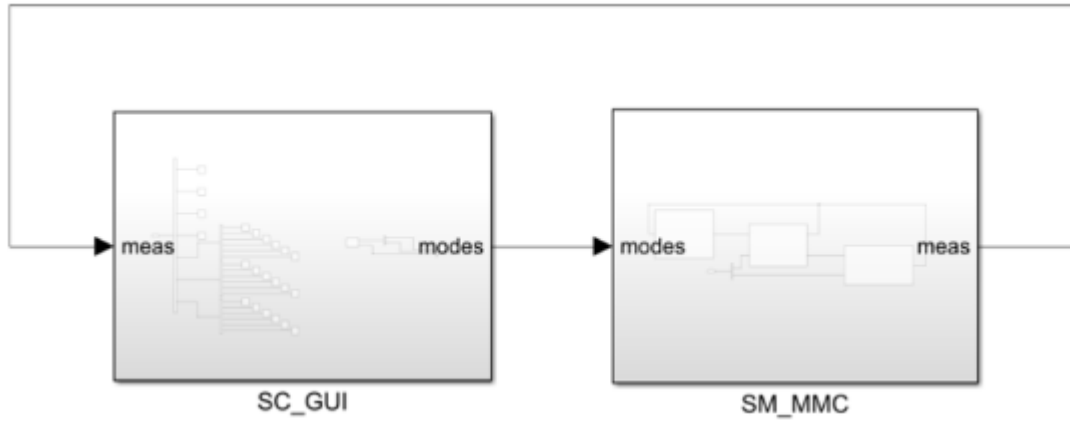


Figure 21. MMC verification model topmost layer

2. OpComm Blocks

The second modification for a standard Simulink model to be used in RT Lab is the addition of “OpComm” blocks. OpComm blocks must be added between the “inport” block and any other blocks of each computational or GUI subsystem. OpComm blocks coordinate the real-time and non-real-time data between the subsystems [20]. The OpComm block must be placed into the model after the subsystem is created and named in order for the block to properly link and coordinate the data. An example is shown in Figure 22.

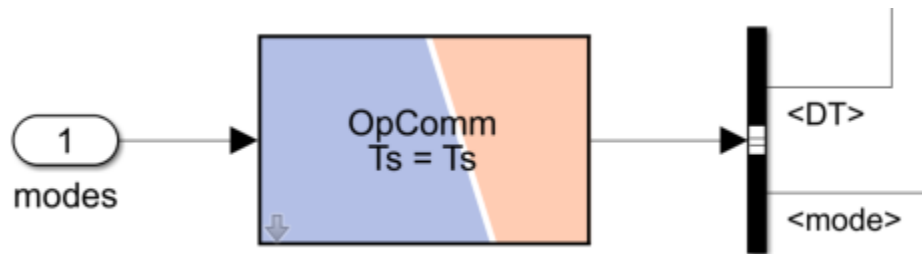


Figure 22. RT Lab OpComm block

The OpComm block is only capable of receiving one type of signal, synchronous or asynchronous [20]. Synchronous signals are what RT Lab designates for real-time computations and they are generated from within SM or SS subsystems. Asynchronous signals are not used for real-time data and are generated within SC subsystems. Therefore, if a subsystem receives data from both an SC and SS subsystem, two OpComm blocks must be used, one for each data type [20]. An example of subsystem and OpComm block placement is provided in Figure 23.

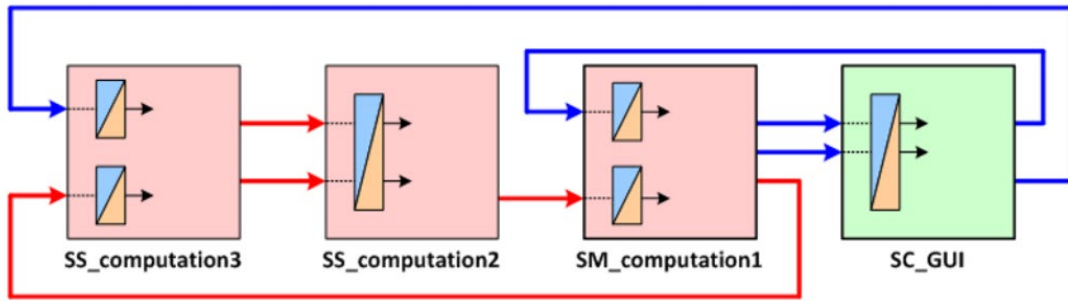


Figure 23. Subsystem and OpComm block placement example. Source: [20].

3. Data Acquisition

In a normal Simulink model, the user can send data directly to the Matlab workspace using a “ToWorkspace” block. In RT Lab, the computations of the model are run on the OP5707XG and the signals sent back to the host computer are asynchronous, or not real-time. There also may be instances, depending on the model complexity and number of signals, where the bandwidth between the host and the OP5707XG cannot handle the amount of data the GUI subsystem needs. For this reason, obtaining required data from the SC subsystem from a ToWorkspace block is not allowed. A specific RT Lab “OpWriteFile” block must be used instead [20]. The OpWriteFile block creates a .mat or .csv file that can then be loaded into the Matlab workspace for further processing. The OpWriteFile block records the desired signal directly from the OP5707XG cores and onto its hard drive, which ensures no data is lost even if the host computer is not able to see signals in real-time. The size of the data acquisition must be set by the user depending on

the number of signals, sampling rate, and length of data required. An OpWriteFile block is shown in Figure 24.

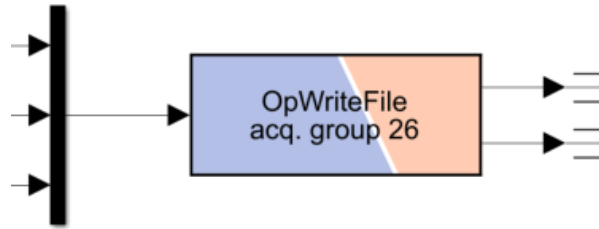


Figure 24. OpWriteFile block

4. Simulation Parameters

The simulation parameters applied to a model can change its real-time simulation performance drastically. For sample time, RT Lab requires the use of a fixed step size [20]. Real-time simulations cannot be performed if the software does not know the step size of the next sample, as in a variable step time case. Choosing a step size that is too short will prevent the OP5707XG CPUs from completing all required computations before the next sample is required. This is referred to as an “overrun” and is depicted visually in Figure 25.

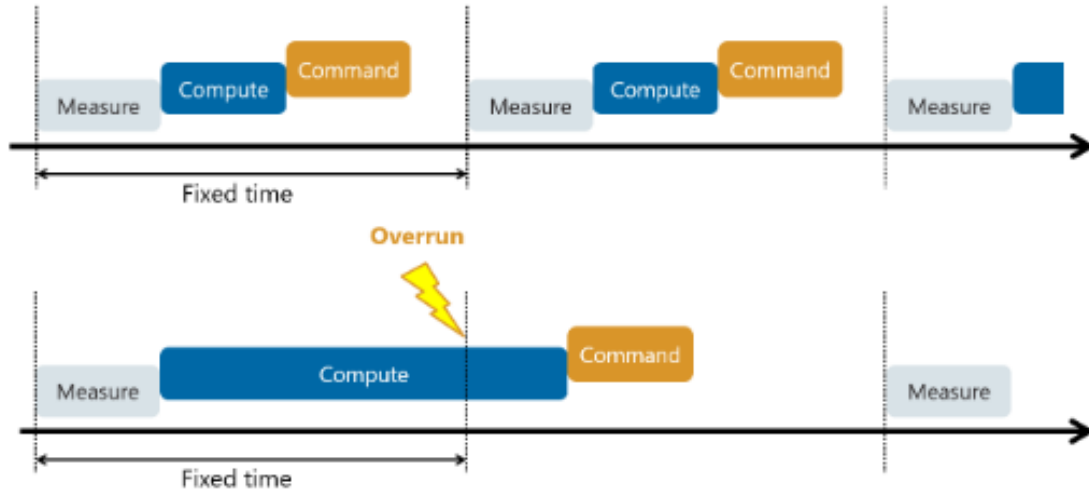


Figure 25. Overrun visualization. Source: [20].

A step size that is too long may allow system responses to be missed while waiting for the next sample, leading to less accurate simulation results. Therefore, the smallest allowable sample time that does not cause overruns to occur is ideal for accurate real-time simulation.

5. OP5707XG Hardware

The hardware used in conjunction with RT Lab is the OPAL-RT OP5707XG. The OP5707XG is a standalone computer that connects to the PC of the user via an ethernet cable. Essentially, it is a separate computer with between four to 16 CPU cores, depending on purchase options, and a VIRTEX-7 FPGA with support of up to 128 analog or 256 digital I/O ports for hardware-in-the-loop simulation [21]. The SM subsystems are simulated on the OP5707XG cores. For this research, only one CPU core is licensed, therefore only one computational subsystem is supported. A functional diagram of the OP5707XG is shown in Figure 26.

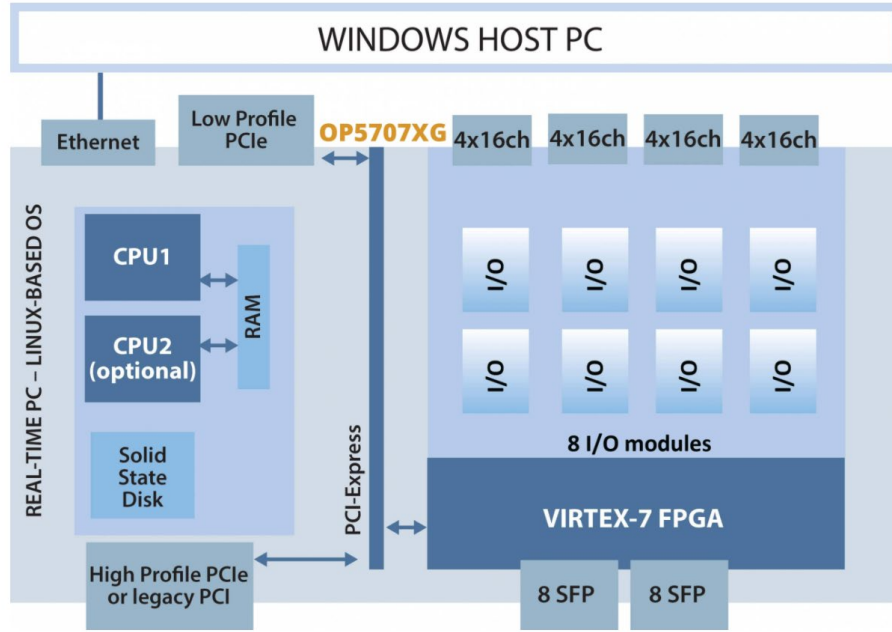


Figure 26. OP5707XG architecture. Source: [20].

6. ARTEMiS Software Plug-in

ARTEMiS, or Advanced Real-Time ElectroMechanical Simulator, is an additional software plug-in from OPAL-RT that contains a special block library for advanced modeling within RT Lab [22]. ARTEMiS implements a solver, referred to as state-space nodal, which is specifically designed to “combine the accuracy potential of state-space methods with the ability of the nodal approach to handle circuits with large numbers of switches” [22]. For this research, the ARTEMiS plug-in provides an essential block library that allows for the modeling of the series connected SMs of each arm in an accurate and user-friendly manner. The blocks were created and intended for use with MMC models, however their operation in the MMR model is still valid because only the only changes from an MMC to an MMR are the diode stacks and the control system. The SMs are identical.

a. MMC 1P Cell

The MMC 1P Cell is a single block that allows a user to implement up to 50 SMs in series [22]. The block allows the user to adjust essential parameters for the SM such as

initial V_{cap} , switch resistance, number of SMs, and the SM type. An example of the MMC 1P Cell used in the MMC verification model is shown below in Figure 27. The inputs “Group: 1” and “Group: 2” control the “S1” and “S2” IGBTs discussed in Chapter II. For the half-bridge SMs used in this research, these inputs are vectors of ones and zeros where the vector length is equal to the number of SMs per cell. The “para” input provides data to the SMs from the MMC CPU block which is discussed in the next subsection. The input “G5” is unused for half-bridge SMs and consists of a vector of zeros of length twenty-five as a placeholder. The output “ V_{cap} ” provides capacitor voltage for each individual SM. The output “iv” provides the current and voltage across all SMs which is equivalent to V_{arm} and I_{arm} . The “center” and “common” terminals are the upper and lower arm connections, respectively.

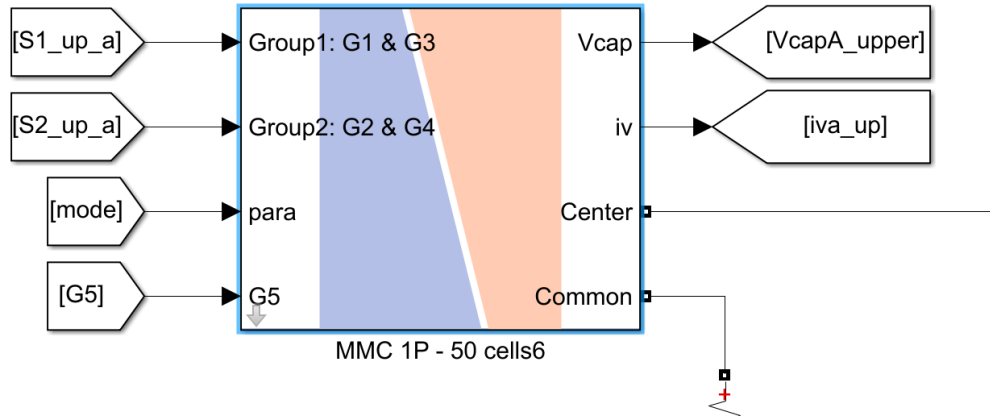


Figure 27. MMC 1P Cell block

b. MMC Parameters Block

The MMC Parameters block accepts user input for various MMC parameters and distributes those values to the MMC 1P Cells [22]. Relevant values used in this study are the SM capacitor capacitance, shunt resistance, and IGBT deadtime. The block allows other parameters to be set for advanced modeling such as fault introduction and ARTEMiS specific PWM techniques. The MMC parameters block is shown in Figure 28.

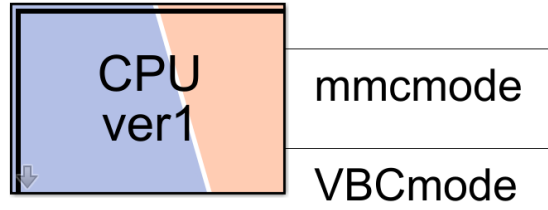


Figure 28. MMC parameters block

B. REAL-TIME SIMULATOR VERIFICATION

To verify the operation and accuracy of the software and hardware, the real-time simulator was tested by simulating an MMC. An MMC was chosen because it is the parent topology of the MMR and well-studied. If the SMs in the MMC can be properly modeled in the real-time simulator, then they will be modeled correctly in the MMR because they are the same. This section presents the MMC model system parameters, the model, and a brief overview of the results to verify the real-time simulator performance.

1. System Parameters

The system parameters for this verification simulation were chosen to represent a practical shipboard MVDC electrical distribution system powered from turbine-driven AC generators. For comparison purposes, the values of key parameters follow those in [3] and are shown in Table 2.

Table 2. MMC system and model parameters

Parameter	Value	Parameter	Value
Power rating	35 MVA	V_{cap}	1 kV
AC voltage	6.6 kV	Number SMs/arm	12
DC voltage	12 kV	SM capacitance	40 mF
AC frequency	60 Hz	Switching frequency	5 kHz
L_{gen}	1 mH	Sample time	25 μ s

The MMC will be controlled as a rectifier and convert three-phase AC to DC. The DC bus is modeled with a DC voltage source for stability.

2. Model

The topmost layer of the MMC was previously displayed in Figure 21. The MMC GUI subsystem is shown in Figure 29. This is where the user can view vital parameters of the MMC, such as various system voltages and currents, through the numerous viewing scopes. The MMC parameters block is also present and provides user defined parameters to the computational subsystem.

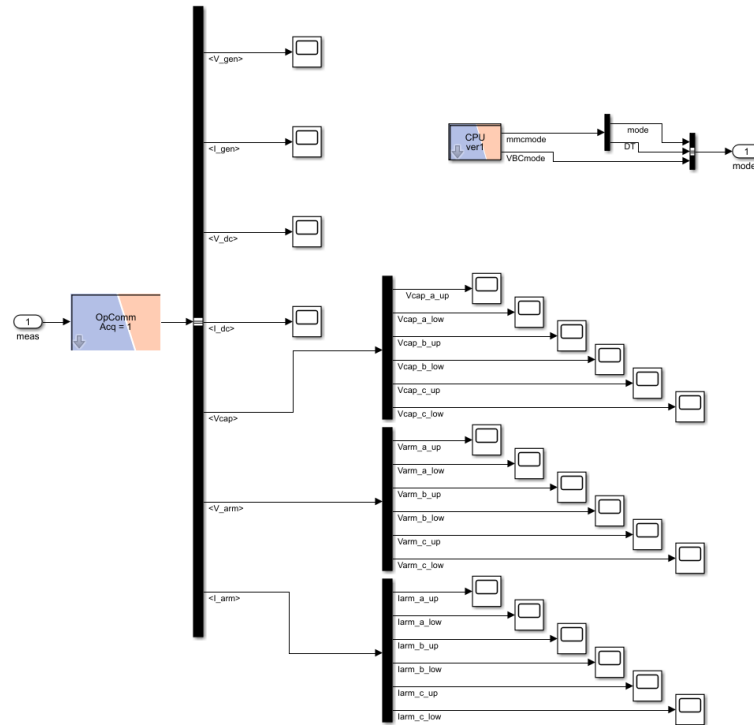


Figure 29. MMC GUI subsystem

The computational subsystem is separated into three non-RT LAB specific subsystems. The actual MMC circuitry subsystem is shown in Figure 30. This subsystem contains the MMC 1P Cells discussed earlier and the topology of the MMC discussed in Chapter II is represented by this subsystem.

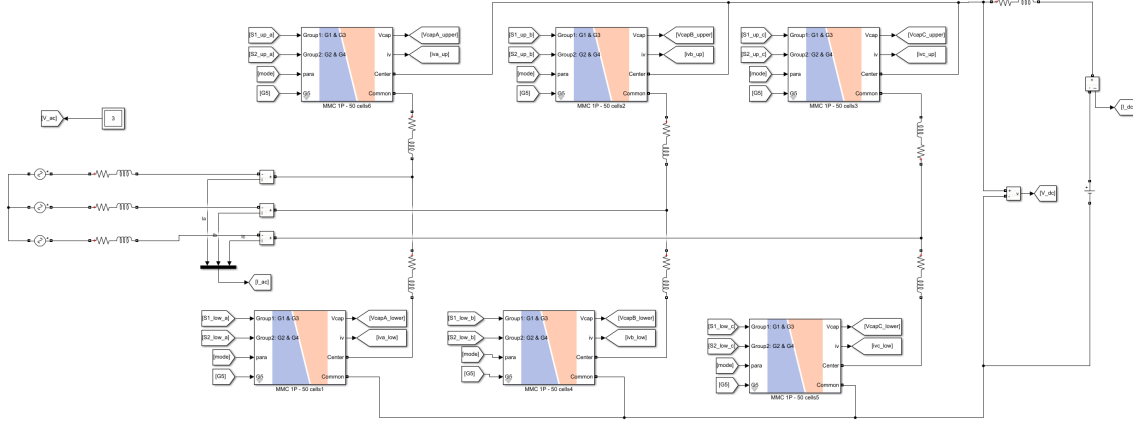


Figure 30. MMC circuit subsystem

The controller subsystem is shown in Figure 31. This subsystem contains non-ideal open loop controls, I_{dc} controls, and arm current balancing controls. This control system was used by Kinney in [3].

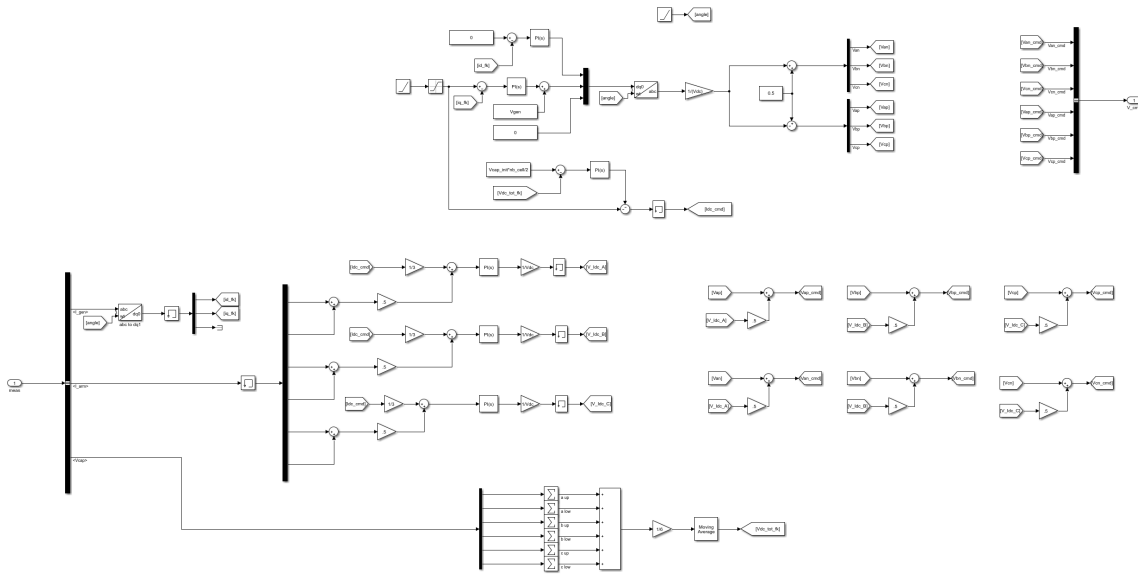


Figure 31. MMC control system subsystem

The remaining subsystem within the computation subsystem is where the PWM and SM capacitor voltage balancing is carried out. This subsystem is displayed in Figure 32.

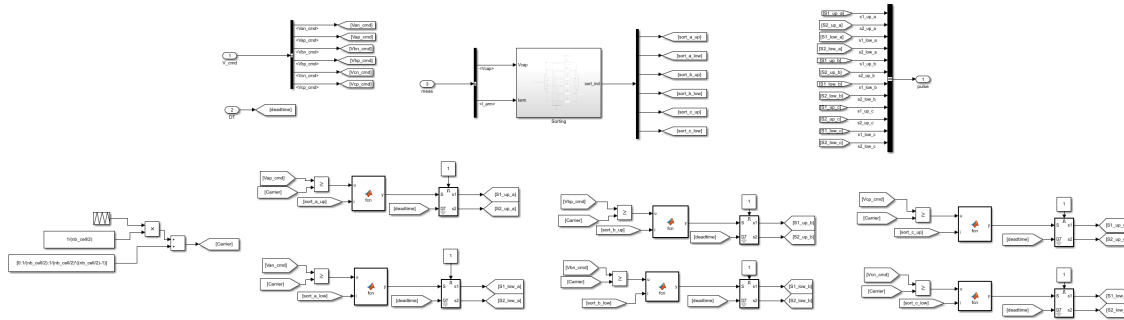


Figure 32. MMC PWM and SM capacitor voltage balancing subsystem

3. Results

The following section discusses the results of simulating a basic three-phase MMC as a rectifier in the real-time simulator. The reason for this simulation was to verify the operation of the real-time simulator and ensure the modeling techniques used for the MMR create accurate results.

The three-phase generator currents drawn by the MMC are shown in Figure 33. The MMC causes no visible distortion to the generator current. This is due to the high number of voltage levels per arm and well-balanced capacitor voltages.

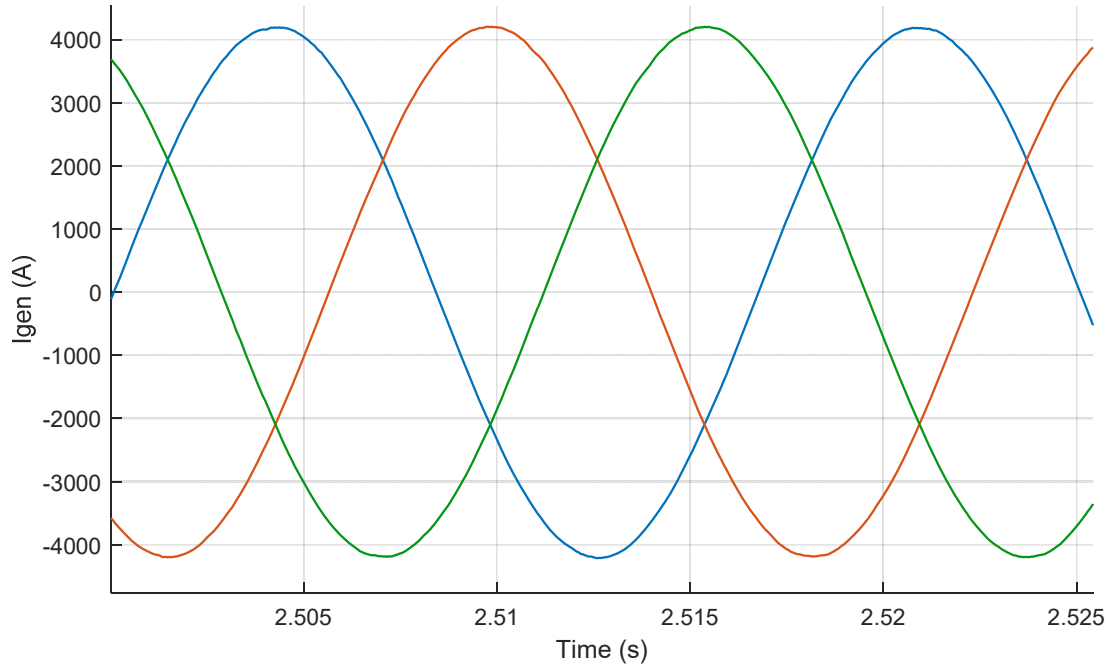


Figure 33. MMC three-phase AC generator current waveform

The MMC a-phase upper V_{arm} is plotted in Figure 34. The 12 distinct voltage levels are clearly depicted. The relative sloping of the different levels also indicates the state the capacitors are in, either charging or discharging. Figure 34 shows that each MMC arm is blocking the full DC bus voltage. The a-phase upper I_{arm} is shown in Figure 35. The I_{arm} waveform is sinusoidal-like in shape but is also not centered about the zero crossing. Per the established positive current direction, the overly negative current flow shown in Figure 35 represents the current flow out of the “top” of the arm and into the DC bus which is expected for the modeled rectifier operation. These results are consistent with experimental data from [23] and [24].

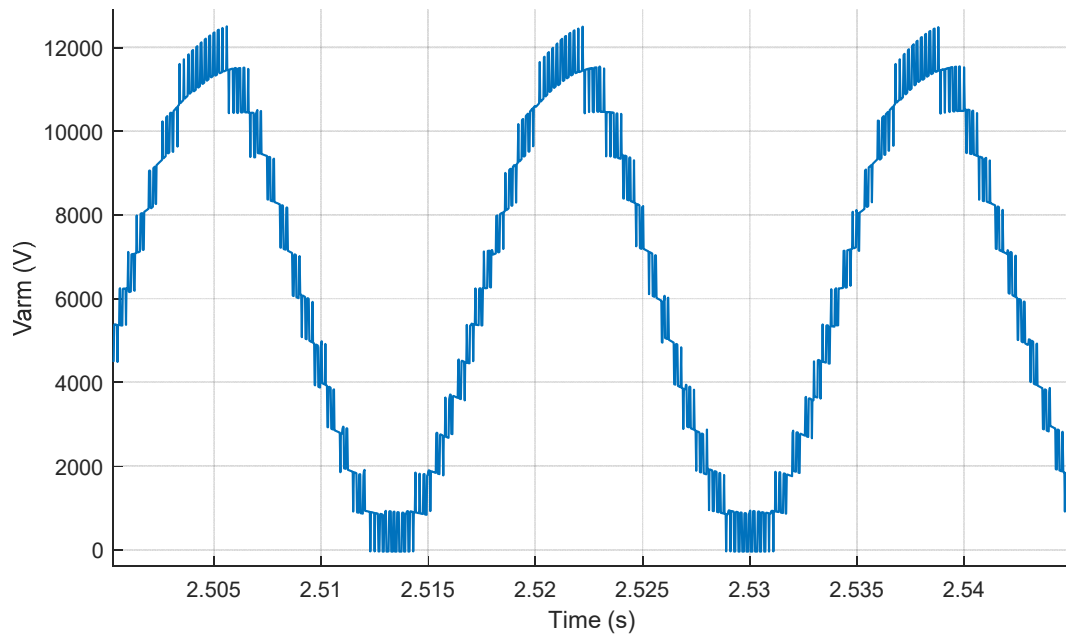


Figure 34. MMC a-phase upper arm voltage

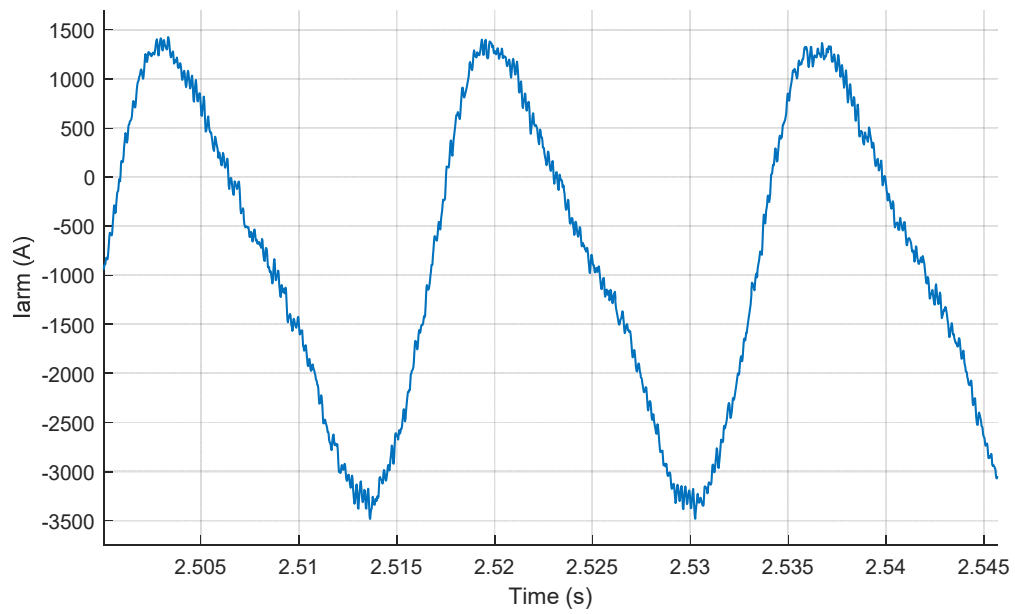


Figure 35. MMC a-phase upper arm current

The real-time simulator was able to model the individual SMs accurately as the results were comparable to experimental results obtained in [23] and [24]. With a switching frequency of 5 kHz and sample time of 25 μ s, the real-time simulator obtained 8 samples per fundamental switching cycle. The a-phase upper arm capacitor voltages are plotted in Figure 36. The summed capacitor voltages for each arm are plotted in Figure 37. The sorting algorithm was able to maintain the capacitor voltages balanced.

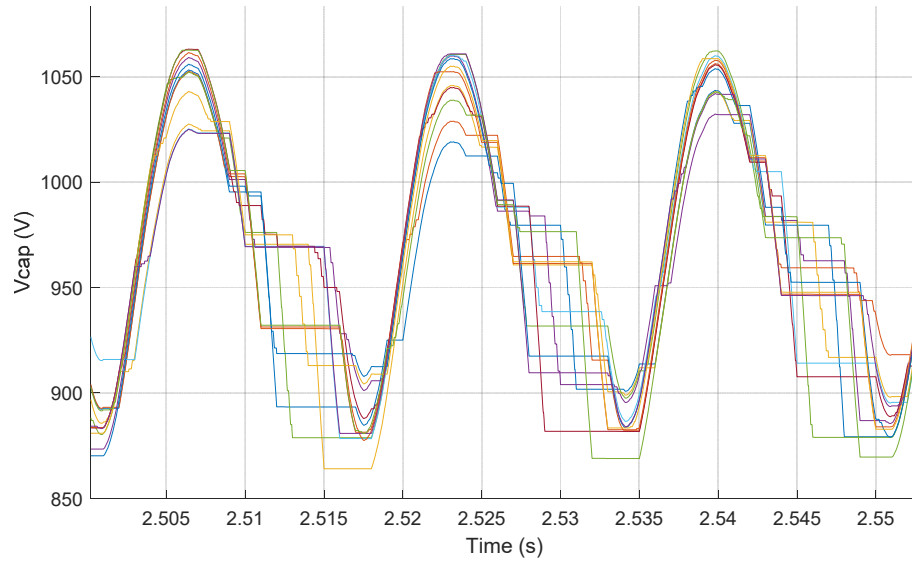


Figure 36. MMC a-phase upper arm individual capacitor voltages

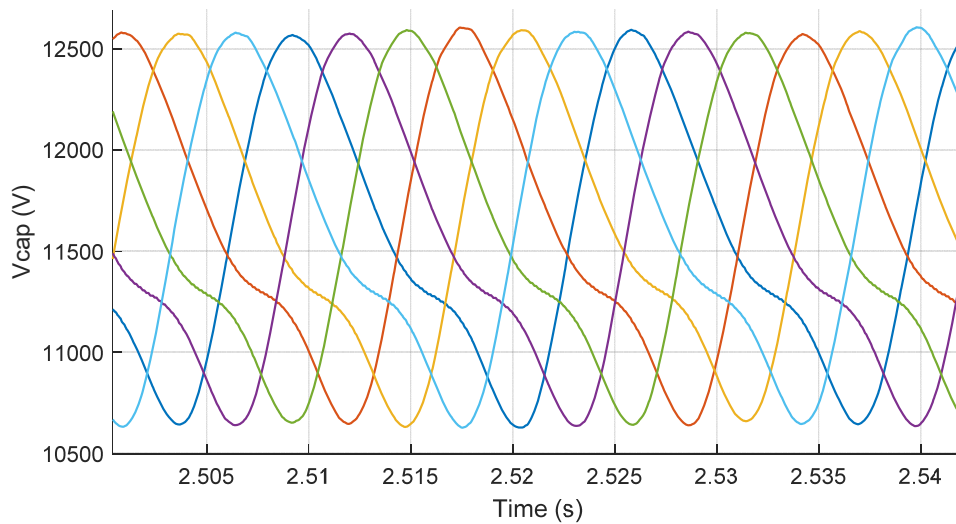


Figure 37. MMC summed arm capacitor voltages

The real-time simulator was able to run the MMC model and accurately record data with no data loss. The real-time simulator, with a sample time of 25 μ s, provided enough samples for accurate modeling of the SMs while simulating fast enough to match real world time. In comparison, the same simulation ran in Simulink required about 35 real world seconds for every simulation second. This simulation verified the ability of the real-time simulator to accurately model the MMR in real-time.

V. SIMULATION RESULTS AND ANALYSIS

This chapter presents the results of running an MMR model in the real-time simulator. The chapter begins by presenting the MMR model and the system parameters. Then, the results of the real-time simulations are presented. Results will start with the baseline MMR controller used in [3]. Next, the results of the model with the ideal feed forward and Q feedback control will be presented. The impact of the common mode voltage control will then be discussed.

A. MODEL AND SYSTEM PARAMETERS

The MMR system parameters were identical to those of the MMC verification in Chapter IV. A summary of the parameters is shown in Table 3. The only difference in the system is the number of SMs per arm was reduced by half to 6 SMs because the MMR only requires 50% of the SMs compared to an MMC and is the main benefit of the MMR.

Table 3. MMR simulation and model parameters

Parameter	Value	Parameter	Value
Power rating	35 MVA	V_{cap}	1 kV
AC voltage	6.6 kV	Number SMs/arm	6
DC voltage	12 kV	SM capacitance	40 mF
AC frequency	60 Hz	Switching frequency	5 kHz
L_{gen}	1 mH	L_{arm}	100 μH

The model consists of a three-phase AC generator linked to a stable DC bus by an MMR. The stable DC bus is modeled by using an ideal DC voltage source. To demonstrate the MMR PF over a variety of operating conditions, the reference active power P^* was ramped from 16 MW to 34 MW over 2.2 seconds. This provides better insight to the ability of the modified control system to regulate the PF over a wide range of power in dynamic and steady state conditions.

The simulation was run at a sampling frequency of 40 kHz, or 25 μs per sample. This value was chosen to be as small as possible without causing overruns during the real-

time simulation. This sampling rate ensured accurate modeling of the SMs by providing 8 samples for each fundamental switching cycle. Per Chapter IV, the MMR Simulink model consists of a SC and an SM subsystem. The SM subsystem contains three non-RT Lab specific subsystems for the control system, the PWM and sorting algorithm, and the MMR circuitry. The topmost layer of the MMR model is shown in Figure 38 and Figure 39 displays the MMR GUI subsystem.

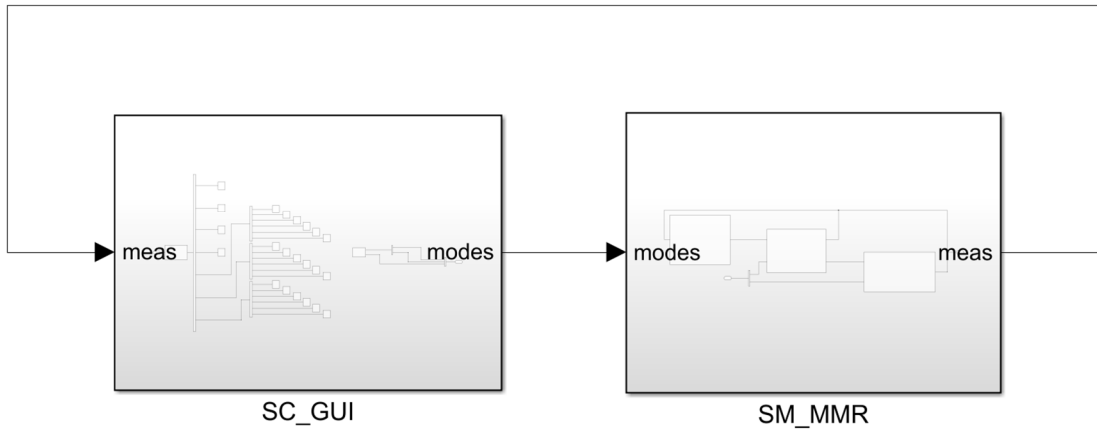


Figure 38. MMR Simulink model top layer

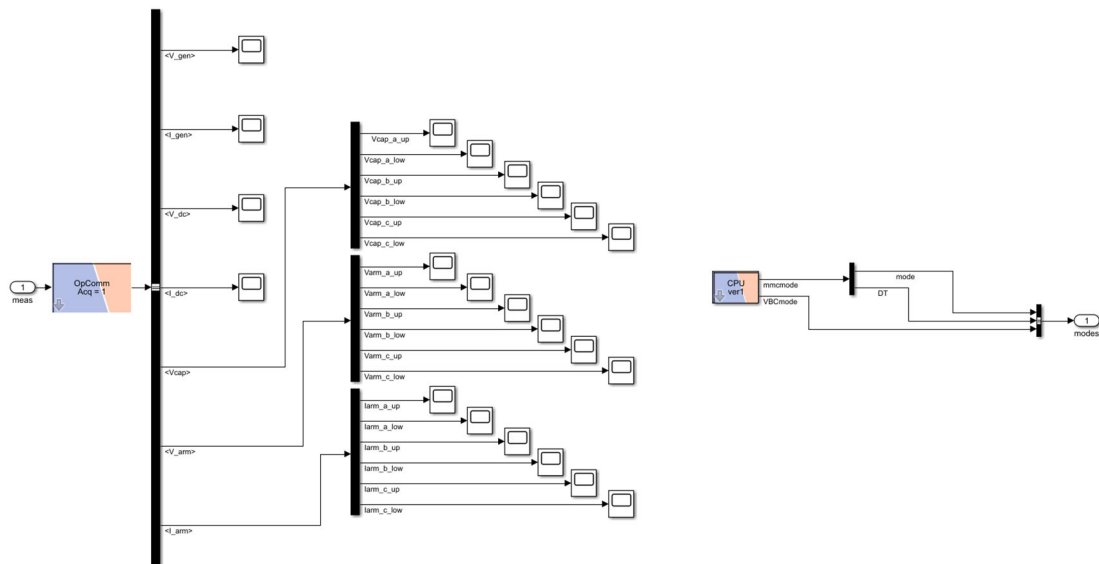


Figure 39. MMR Simulink model GUI subsystem

The portion of the model that represents the MMR topology discussed in Chapter II is shown in Figure 40. The circuitry is nearly identical to the MMC model with the exception of the three diode stacks consisting of four diodes each. The midpoint connecting the center of each phase diode stack can be seen.

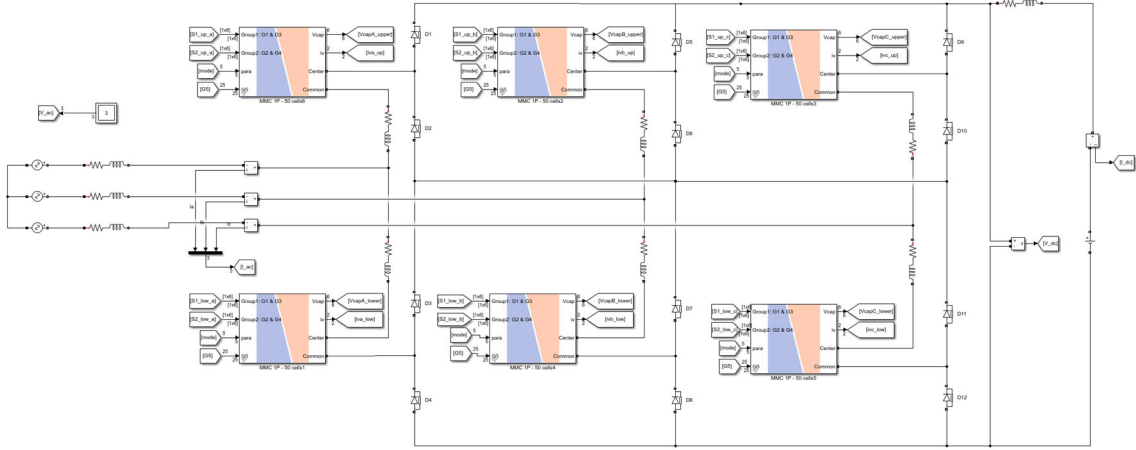


Figure 40. MMR model topology subsystem

The model control system is configured per Figure 19. The outputs of the control system are 6 voltage commands, one for each arm. These voltage commands are sent to the PWM and sorting subsystem which is identical to Figure 32. Finally, after sorting the switching logic is sent to each of the MMC 1P Cell blocks to control each SM state.

B. BASE MMR CONTROLLER RESULTS

To fully understand how the improved control system researched in this study helps, a baseline must first be set. For this simulation, the ideal i_d^* equation was removed and i_d^* was set to a constant zero. Also, the Q feedback control gain was set to zero, removing any effects it has on the system. The common mode voltage was set to a constant zero. This controller is now identical to that used in the topology comparison in [3]. The three-phase AC current drawn by the MMR is shown in Figure 41.

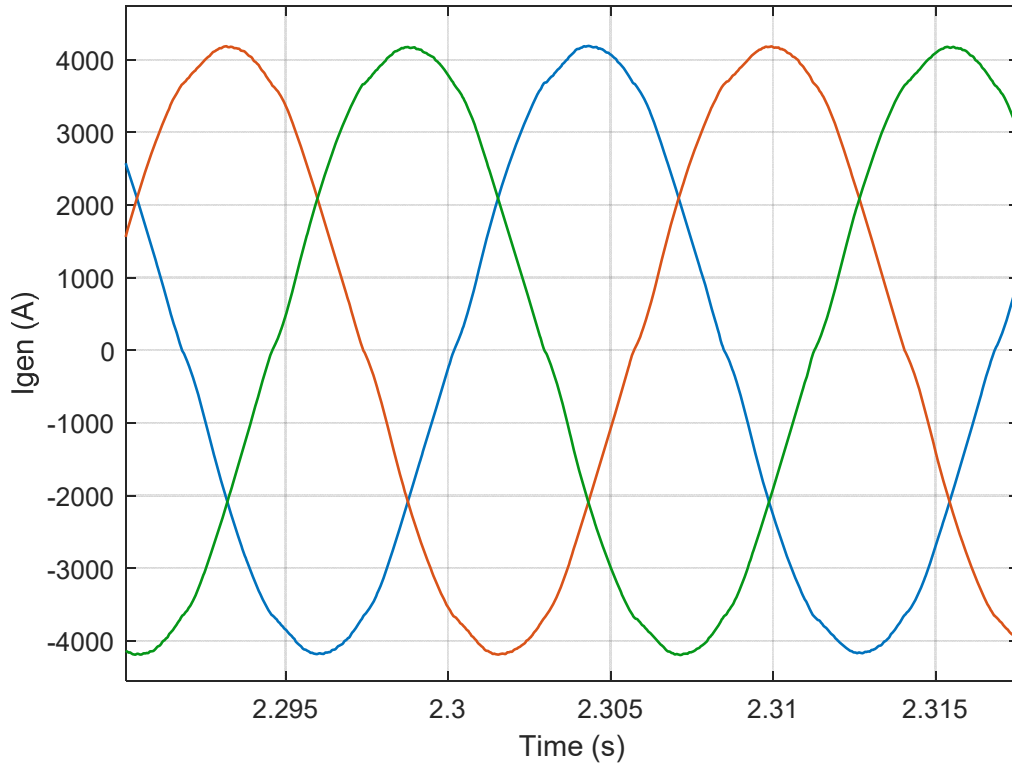


Figure 41. MMR base controller three-phase AC generator current waveform

Figure 41 shows visible current distortion at the upper and lower peaks, as well as the zero crossing for all three phases. The a-phase upper V_{arm} is shown in Figure 42. The peak value obtained is roughly half of the arm voltage achieved by the MMC. The peak value of V_{arm} was 6.453 kV. This is the benefit of the MMR as compared to an MMC. Also, the general waveform of the arm voltage is no longer sinusoidal. The implementation of the diode stacks causes a transition point between states where the sinusoid gets “sliced” in half, creating a unique waveform.

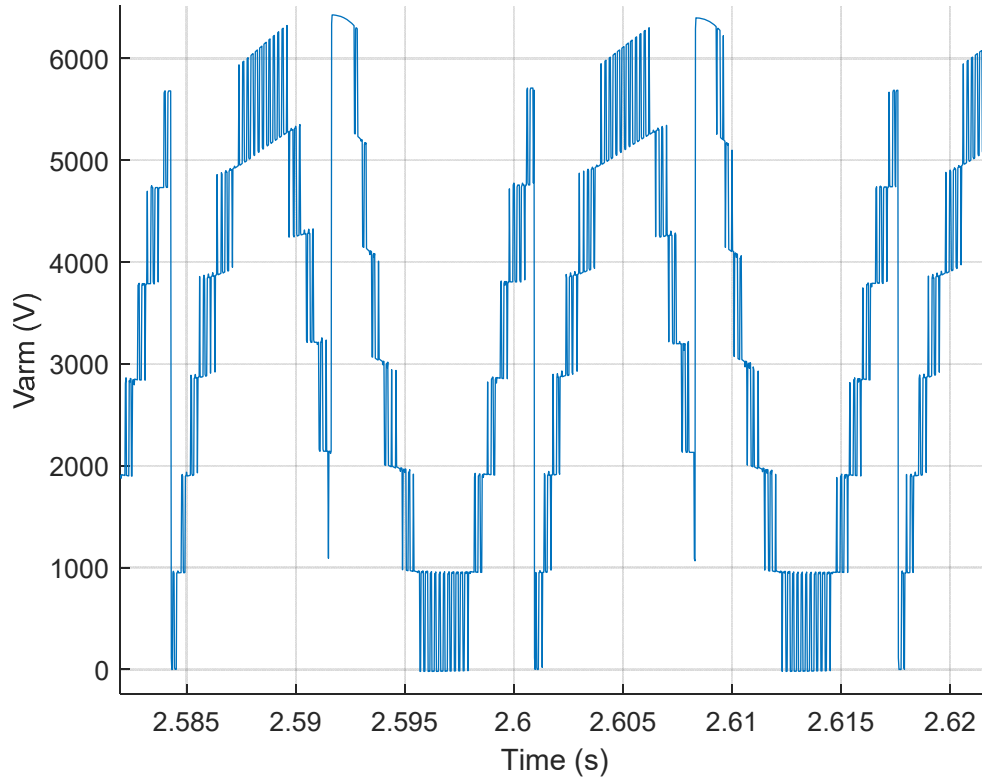


Figure 42. MMR base controller a-phase upper arm voltage

The a-phase upper I_{arm} is plotted in Figure 43. The impact of the diode stacks is clearly seen when the current changes polarity. Flat spots at the zero crossing represent a disruption in current flow. Like the MMC, the I_{arm} waveform is sinusoidal-like in shape. There is a greater portion that is negative, which corresponds to current flowing out of the top of the SMs and into the DC bus.

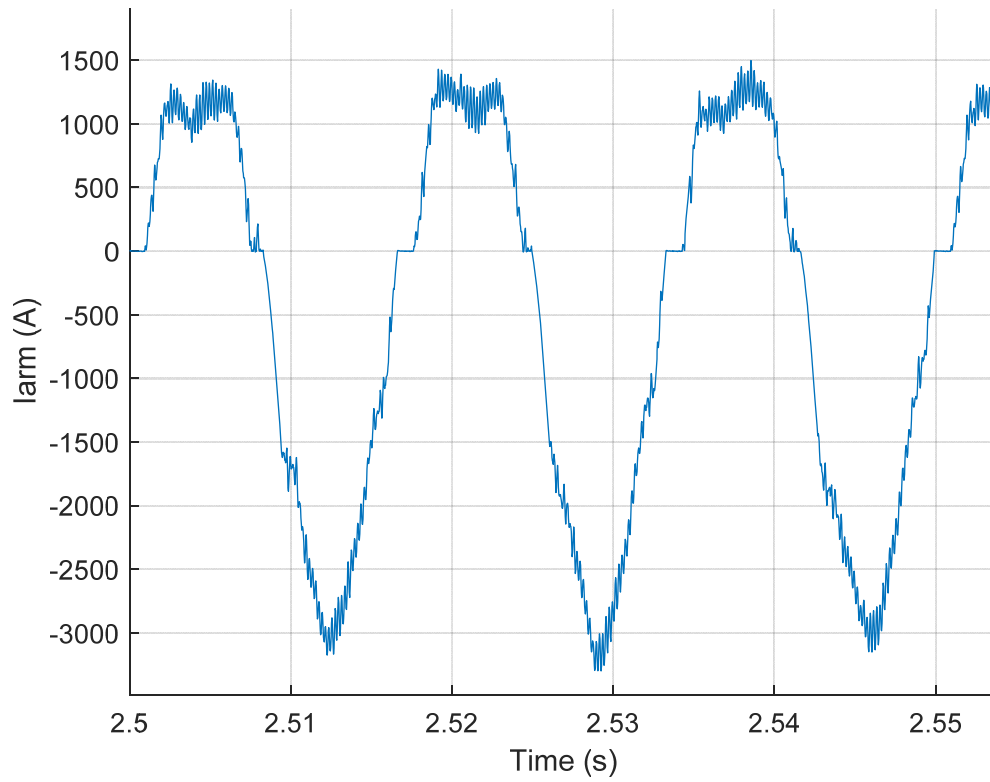


Figure 43. MMR base controller a-phase upper arm current

Figure 44 shows both individual capacitor voltage for a single arm and summed capacitor voltages for each arm. The waveforms are similar to those of an MMC. Though not vital for this study, Figure 44 ensures that the model is operating correctly and the capacitor voltages are maintaining balance throughout the simulation.

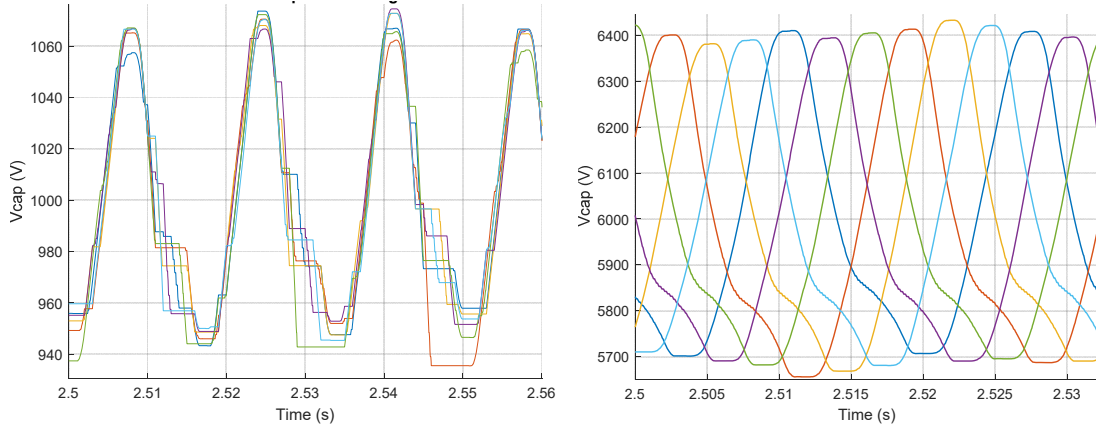


Figure 44. MMR base controller arm capacitor voltages (L) and summed arm capacitor voltages (R)

Finally, an examination into the relative phase angle, θ , between the MMR AC current and AC voltage, which represents the MMR PF, will be the key in identifying the added benefits of the new MMR control system researched in this study. Figure 45 shows the MMR AC current and AC voltage θ for the first 5 seconds of the simulation. The angle begins 8 degrees out of phase and finally steadies out at 18 degrees out of phase. The first 2.2 seconds show the dynamic portion of the simulation in which P^* is linearly ramped. Figure 45 shows that without control, the MMR PF is roughly linear with the MMR power. At steady state, the MMR PF remains constant.

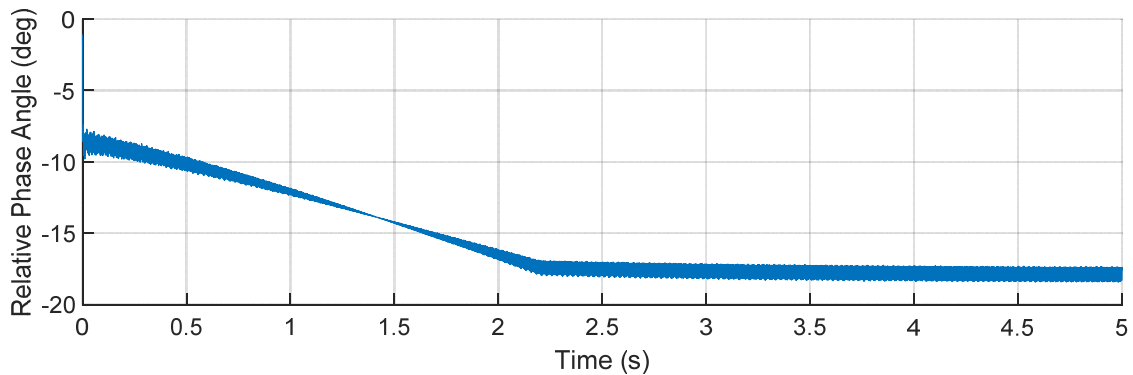


Figure 45. MMR base model dynamic and steady state voltage and current relative phase angle

Figure 45 shows that the MMR, without any specific PF controls, does not naturally operate at unity PF. For further visualization, Figure 46 shows the a-phase AC current and AC voltage overlaid. The leading current represents a capacitive load as seen by the generator. The magnitude to which they are out of phase is apparent, as well as the level of waveform distortion caused by the non-unity PF. When the current crosses zero, the waveform bends towards the polarity of the voltage due to the opposite stress imposed by the out of phase voltage. The same effect distorts the waveform when the other two phases also cross zero because it is a balanced three-phase system.

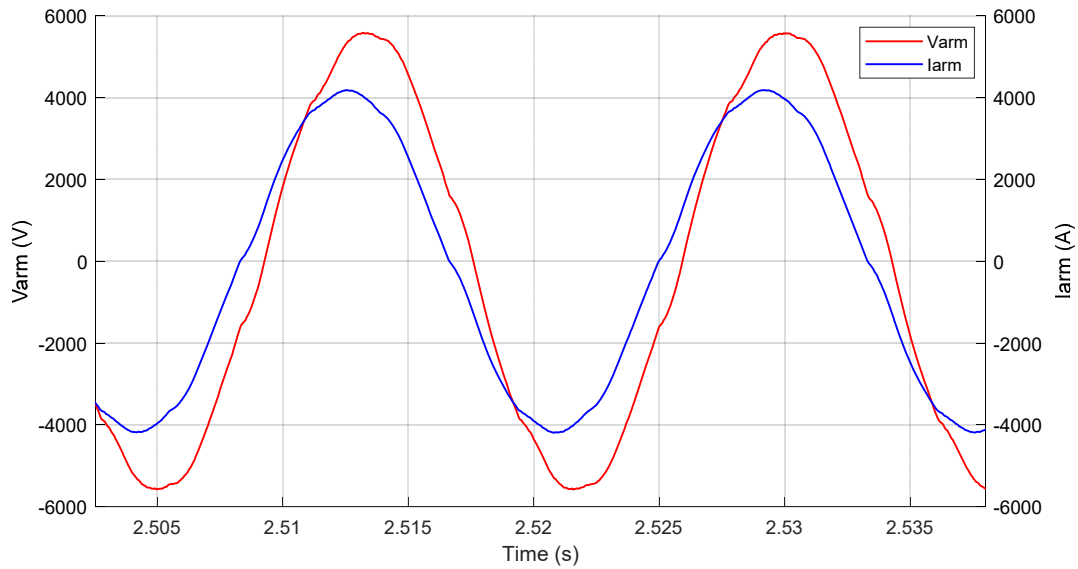


Figure 46. MMR base controller a-phase voltage and current

These results show that the MMR with the control system in [3] is capable of rectifying AC to DC while cutting the arm voltage in half as compared to an MMC. This is the main benefit of the MMR. However, these results also show that without being monitored and controlled, the MMR PF will depart from unity. This causes current distortion, and draws more current than if operated at unity PF.

C. IMPROVED MMR CONTROLLER RESULTS

This section contains the results when the ideal i_d^* feed forward, Q feedback, and common mode voltage controls were implemented together. No system or model parameters were changed from the base controller results. The three-phase AC generator current drawn by the MMR in this simulation is shown in Figure 47.

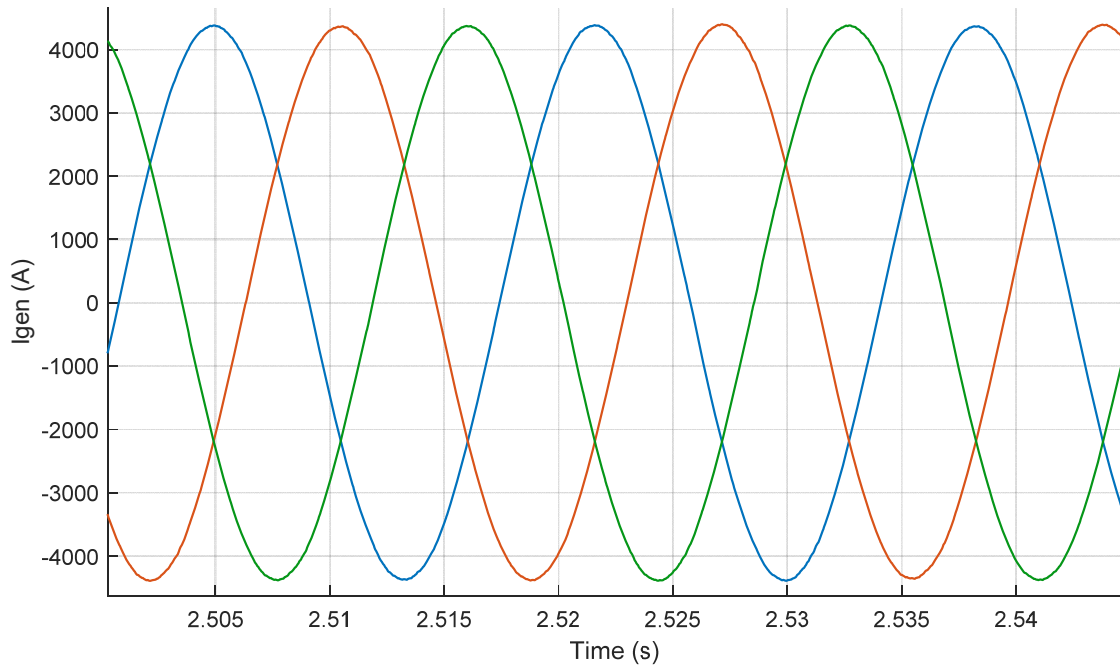


Figure 47. MMR improved controls three-phase AC generator current waveform

The improved MMR control system greatly enhanced the quality of the AC current waveform. There is no visible distortion. The a-phase upper arm V_{arm} is plotted in Figure 48.

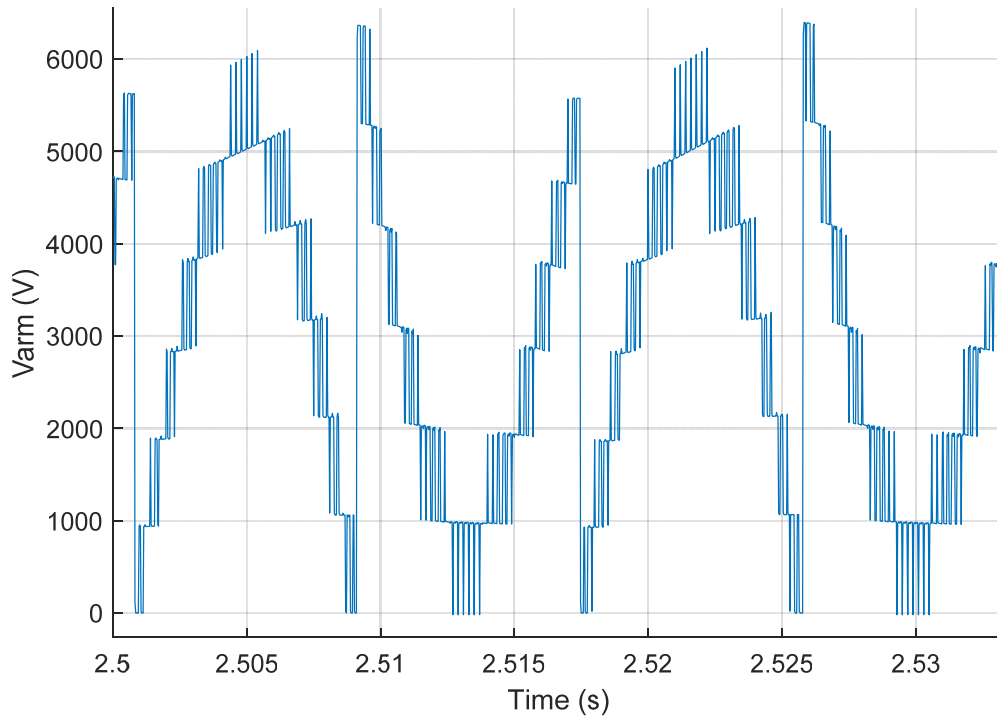


Figure 48. MMR improved controls a-phase upper arm voltage

The results show that the overall shape of the waveform did not change. However, the maximum arm voltage recorded was 6.083 kV. This is a reduction of 370 V across the MMR arm when compared to the baseline results. This reduction in maximum arm voltage reduces the stress across each of the SMs. The a-phase upper I_{arm} is shown in Figure 49. The flat portions from the baseline I_{arm} are no longer seen. Current flow is smoother as it changes polarity, however there are some spikes at the zero crossing.

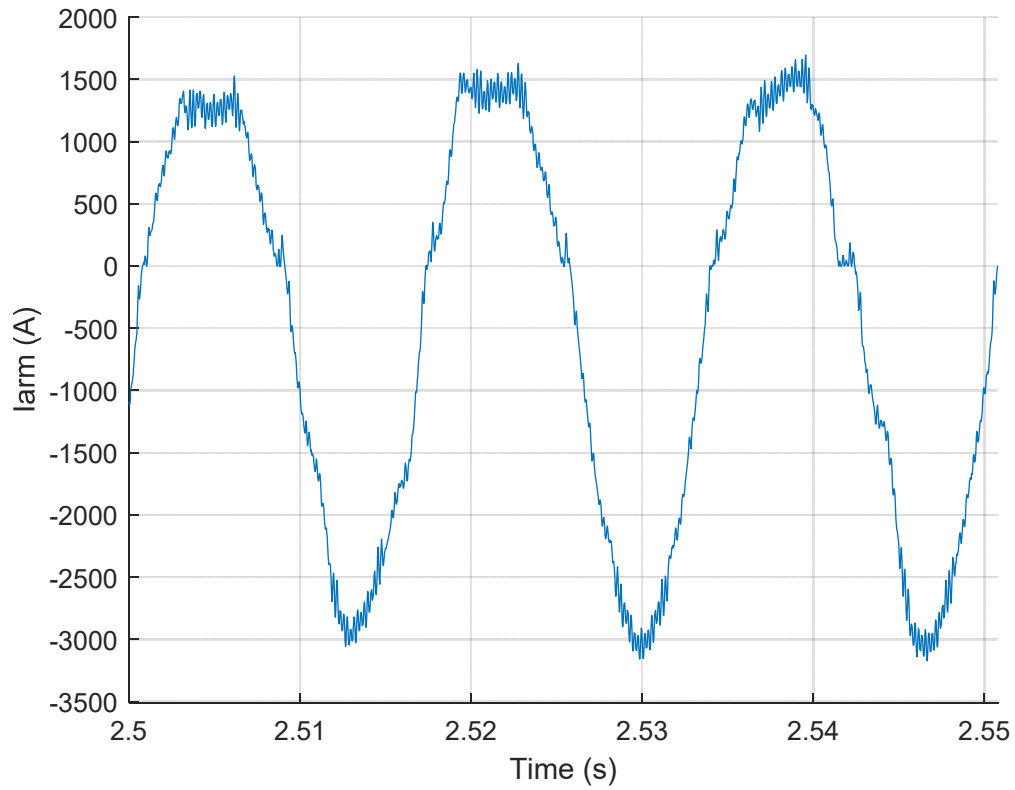


Figure 49. MMR improved controls a-phase upper arm current

The results of the relative phase angle θ between the MMR AC voltage and AC current is plotted in Figure 50. The results clearly show that the controls derived in this research force the MMR to operate at unity PF. The transition at 2.2 seconds from ramped to steady P^* also shows the relative speed the controls have. The controls maintain the PF at unity.

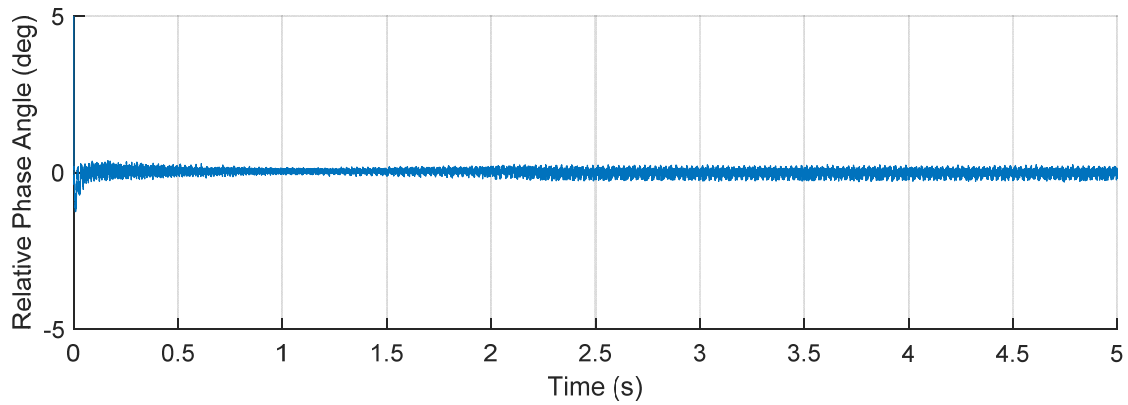


Figure 50. MMR improved controls dynamic and steady state AC voltage and AC current relative phase angle

A further visual into how well the three new controls work together is shown in Figure 51. Figure 51 plots the MMR a-phase AC voltage, AC current, and common mode voltage output. The PF was commanded to unity fast enough that at the first zero crossing almost no input from the common mode voltage controls was needed. By the second zero crossing, the MMR was operating at unity PF and the common mode voltage controls were not needed by the system.

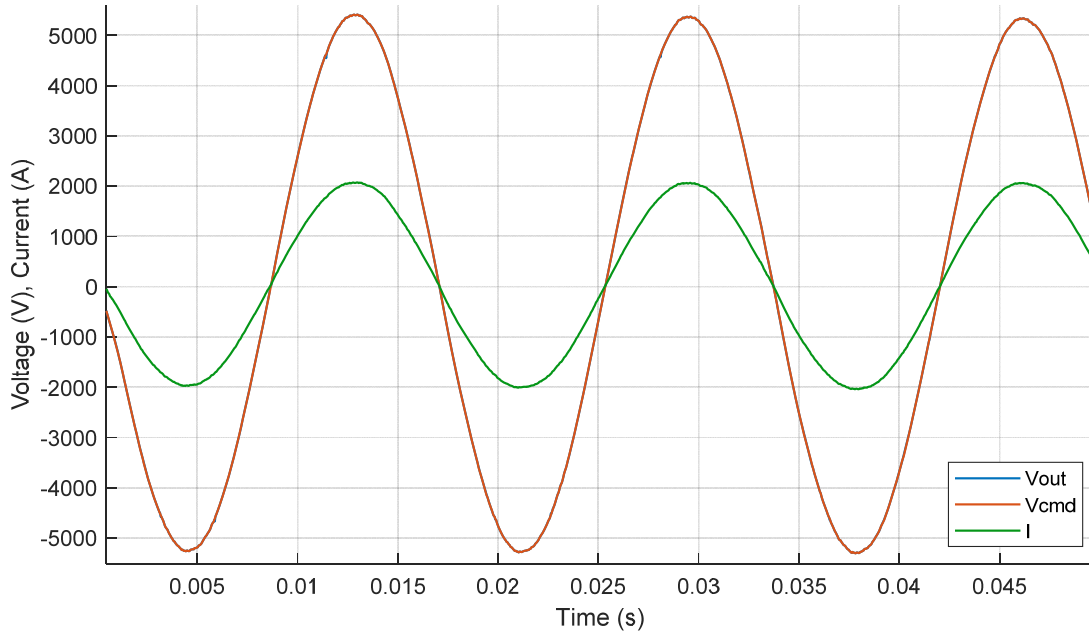


Figure 51. MMR improved controls AC voltage, AC current, common mode voltage overlay

The MMR simulation results with the improved feed forward, Q feedback, and common mode voltage controls was highly effective. The improved feed forward and Q feedback controls successfully operated the MMR at unity PF over a wide range of its power rating. Additionally, the arm voltage stress was reduced, amplifying the benefits of the MMR by allowing half the SMs compared to an MMC for an equivalent system. The feed forward and feedback controls implemented worked well enough that the common mode voltage control did not have provide noticeable benefits. Therefore, the following section provides a detailed analysis specifically for the performance of the common mode voltage control.

D. COMMON MODE VOLTAGE RESULTS

The simulation results of section C showed that the feedforward and feedback controls developed in this thesis were effective at maintaining the MMR at unity PF. Thus, the full benefits of the common mode voltage controls were not fully examined. A separate set of simulations were conducted to better explore scenarios in which the common mode

voltage controls could add greater benefit to the MMR. For these simulations, all simulation and model parameters were the same as presented in Table 3 unless otherwise stated.

For the first common mode voltage control test, a simulation was run with the baseline controller from section B. The only difference is the common mode voltage control was inserted into the control system. Recall from section B that with no control system improvements, the MMR operated with a θ of 18 degrees at steady state. This simulation tests the common mode voltage controls in an extreme condition. Figure 52 plots θ from this simulation against the result from no common mode voltage control.

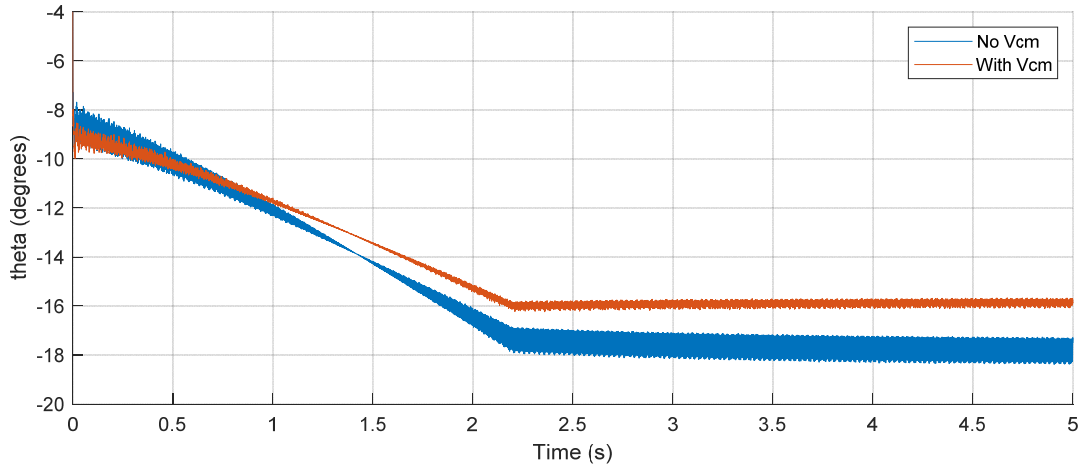


Figure 52. MMR baseline controls with common mode voltage control

Although the common mode voltage controls will not drive θ to zero, the controls were effective at reducing θ by 2 degrees at steady state. Additionally, the band of θ was much narrower with the common mode voltage controls which allows for more predictive operation of the MMR. The real goal of the common mode voltage controls is to prevent current distortion at the zero crossing. To evaluate this parameter, Figure 53 shows the original controller a-phase voltage command V_{cmd} , AC current I , and common mode voltage control final voltage command V_{out} .

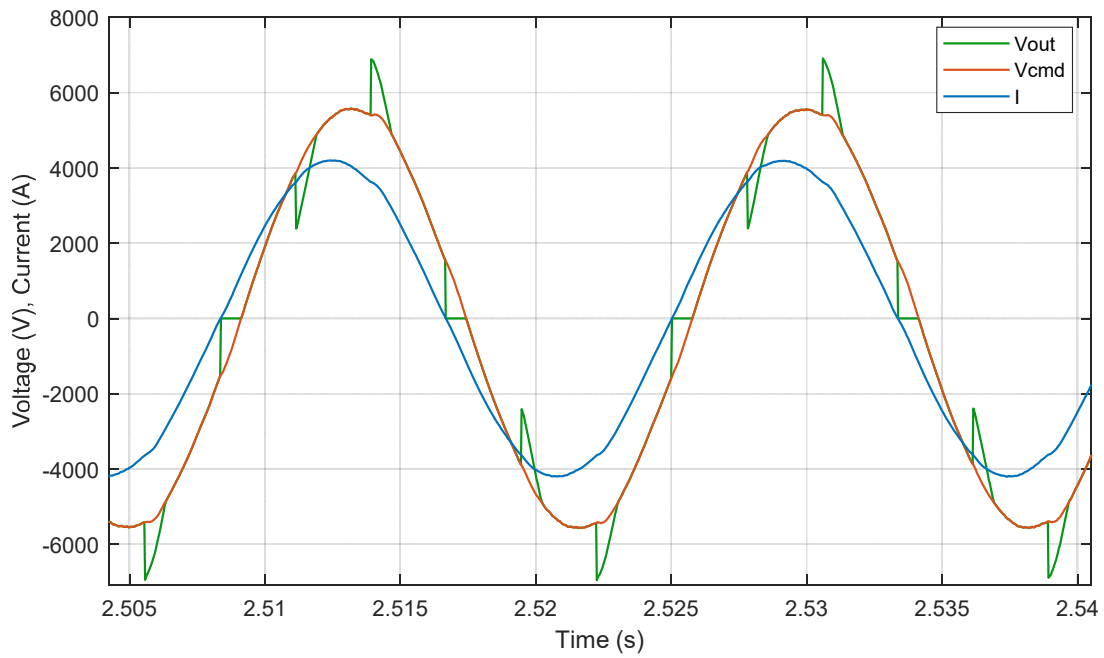


Figure 53. MMR baseline controls a-phase AC voltage, AC current, common mode voltage overlay

The current in Figure 53 shows substantially less distortion as it changes polarity as compared to the results without common mode voltage control, shown in Figure 46. Waveform distortions are still present around the peaks of the current waveform, however. Figures 54 and 55 plot the a-phase generator current drawn by the MMR for the baseline results and the baseline controller with common mode voltage control at the zero crossing and upper peak, respectively. The zero crossing and peaks are magnified for detail.

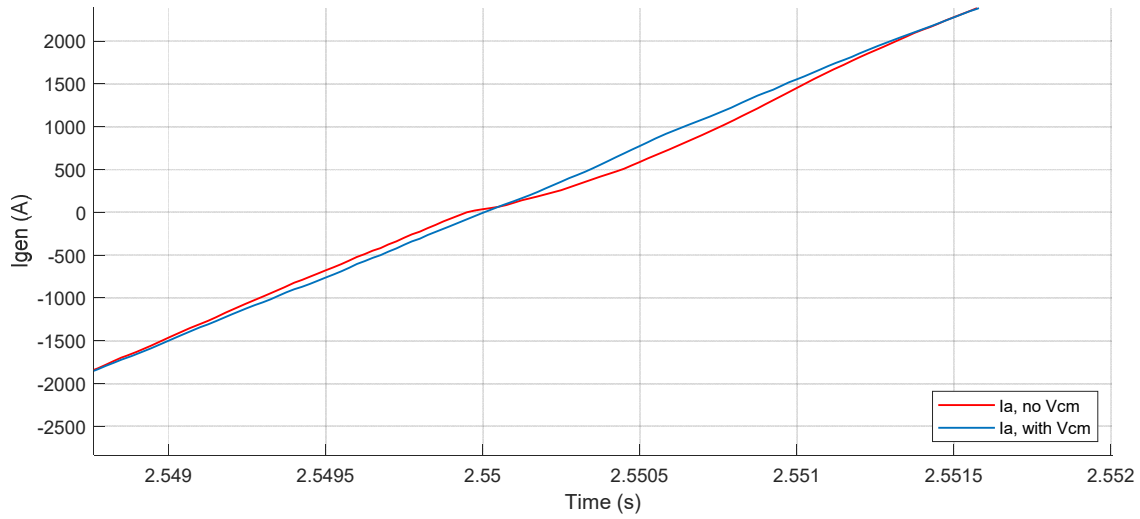


Figure 54. MMR baseline controls, a-phase AC generator current zero crossing with common mode voltage control

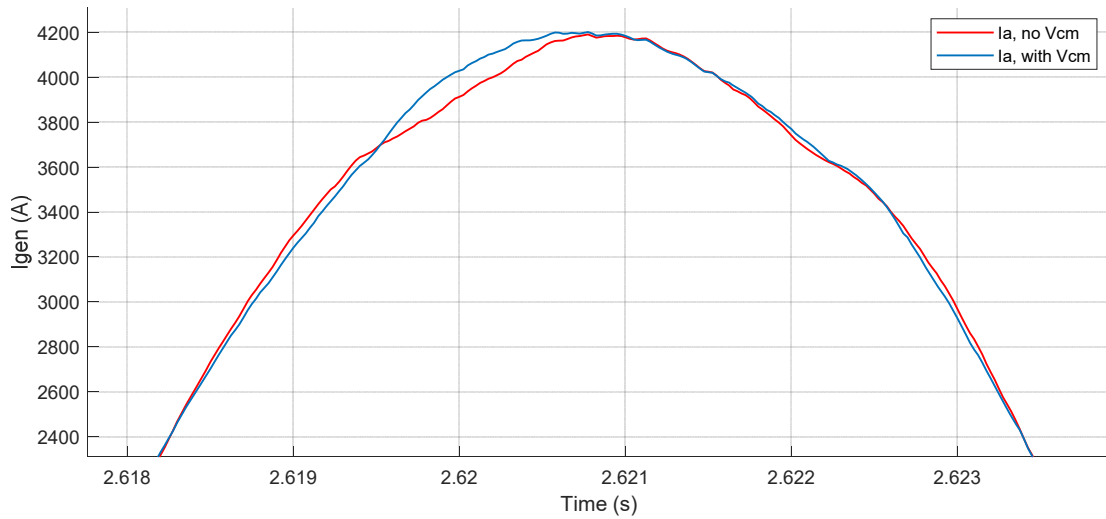


Figure 55. MMR baseline controls, a-phase AC generator current upper peak with common mode voltage control

Figures 54 and 55 demonstrate how the common mode voltage control mostly eliminated the current distortion at the zero crossing. The controls were also effective at minimizing the first distortion the current waveform experiences at the peak. The common mode voltage controls were not able to help the second peak distortion as the waveform

returned towards zero. Additionally, the common mode voltage controls were beneficial in lowering the V_{arm} of each phase. Figure 56 plots a-phase upper V_{arm} . The maximum voltage was 6.085 kV. This is only 2 V higher than the model with all controller improvements of section C and 368 V less than the baseline results of section B.

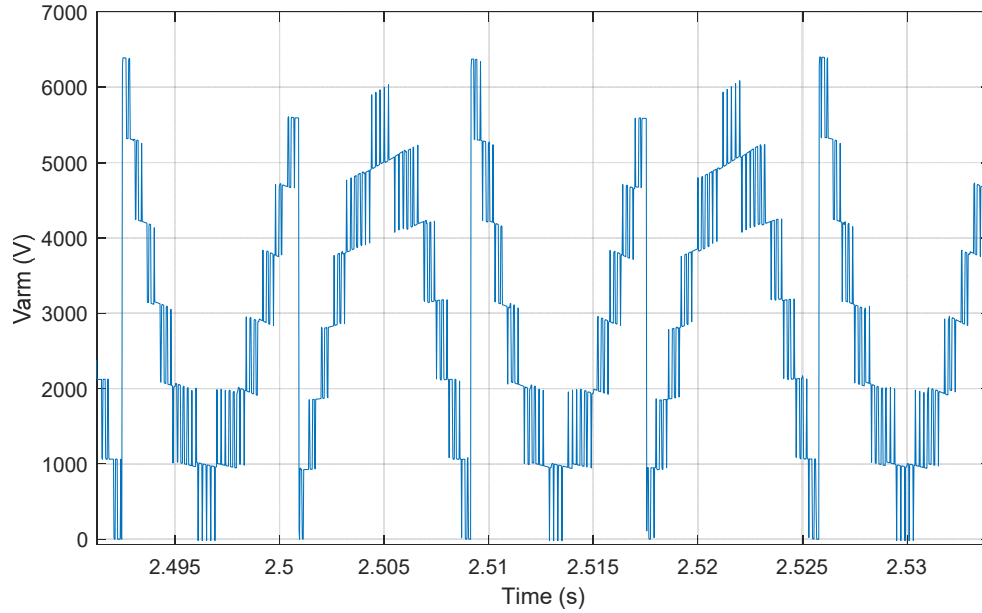


Figure 56. MMR baseline controls with common mode voltage control a-phase upper arm voltage

Overall, for the extreme case of the baseline control system, the common mode voltage controls proved to be effective at eliminating portions of the AC current distortion, mildly improving PF, and reducing arm voltage stress.

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VI. CONCLUSIONS AND FUTURE WORK

This chapter summarizes the real-time simulation results of an MMR with the control system improvements presented in this thesis. Future research ideas for the relatively new MMR topology will be discussed.

A. CONCLUSIONS

The research conducted in this thesis successfully examined, derived, and implemented a novel control system for the MMR. The controls were specifically designed to operate the MMR at unity PF in order to fully realize the maximum benefits of the MMR. At unity PF, the MMR can operate with half of the SMs and an equal SM capacitance compared to an MMC for an equivalent system. The main points observed during this research are presented in the following sections.

1. MMR PF Controls

The ideal feed forward and Q feedback controls designed and simulated in this thesis proved to be highly effective at keeping the MMR AC voltage and AC frequency in phase. Thus, the maximum voltage each arm had to block was reduced by 370 V, or about 6% of the theoretical $V_{dc}/2$ value as compared to the baseline controller. This is critical for the MMR to operate with 50% of the SMs, reducing size, weight, and cost. Without these controls, as proven by the baseline simulation results, the MMR will deviate from unity PF which would draw greater generator current, require additional or higher rated SMs, and have reduced power quality.

2. Common Mode Voltage Controls

The common mode voltage control by itself also proved effective at reducing the voltage each arm had to block. With only the common mode voltage controls, the maximum arm voltage was reduced by 368 V compared to the baseline controller. The common mode voltage control was not able to correct the MMR PF but it was successful at improving the AC current distortion at the zero crossing and when the waveform approached a peak as seen in Figures 54 and 55.

3. Benefits of Real-Time Simulation

The OPAL-RT real-time simulator was able to model the MMR in real-time without data loss while maintaining a high enough sampling rate to obtain eight samples per switching cycle. The real-time simulator benefited this research by reducing the time to run simulations of the MMR by about 30 times compared to the equivalent Simulink model. This allowed for a much higher volume of testing and research to improve the MMR control system. The real-time simulator will benefit future work by providing means to easily scale the model with additional SMs and provide an easy-to-use interface for hardware-in-the-loop simulations.

B. FUTURE WORK IDEAS

The MMR control system can be improved further by applying more advanced sorting algorithms, different PWM schemes, and streamlining the overall number of operations to reduce the computation time of the controller. These factors can improve the MMR efficiency and help transition this research into a hardware prototype. Currently, the MMR has only been researched through theory and computer simulations. One area to study is the addition of hardware into the model, which can be done with the OPAL-RT real-time simulator. Additionally, research into building a physical MMR can be conducted to gain a better understanding of the size, weight, and cost savings the MMR offers over an MMC. Finally, research into the electromagnetic interference of the MMR would be beneficial for building a physical MMR for experimental testing.

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