FUNDAMENTAL AND APPLIED WIDE BANDGAP SEMICONDUCTOR DEVICE MODELING FOR NEXT GENERATION NAVAL APPLICATIONS

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1. Introduction

This final report provides a synopsis of the progress made by Dr. Raghav Khanna's research team at The University of Toledo (UT) during the entire performance period of the grant indicated on the title page. Several projects were undertaken during the performance period, each of which will be elucidated in greater detail in subsequent sections of this report. These projects are:

Modeling and Characterization of High-Frequency Dispersion Effects in Wide Bandgap Semiconductors

Wide bandgap semiconductor power conversion circuits benefit from high switching frequencies, which enable the use of smaller filtering components leading to higher power density. However, the extended spectral content resulting from fast switching wide bandgap semiconductor power conversion circuits is encroaching on frequencies previously only observed in the RF community [1]. This new paradigm in dynamic behavior of power conversion has led to unforeseen challenges both in modeling and characterizing the performance of wide bandgap semiconductors. As an example, the work conducted on this grant has demonstrated that the parasitic per terminal junction capacitances of the semiconductor as well as the stray inductance of the circuit board can vary with frequency. That is, as the spectral content within the power conversion circuit changes, so does the value of the parasitic capacitances and inductances. This phenomenon, known as frequency-dispersion, can lead to significant challenges in modeling and predicting the performance of future fast-switching devices.

The work conducted under this grant presents new empirically corroborated modeling techniques to effectively deal with this challenge. A SPICE model of a 1.2 kV SiC MOSFET is developed and its static characteristics are empirically validated. Frequency-dependent models for the parasitic capacitances of the SiC MOSFET are also developed in SPICE. The simulation also contains frequency-dependent models for the stray inductances of the package of the device, as well as that of the entire circuit board. Empirical transient switching data is obtained from the SiC device, and is fed into the simulation to "train" the model to account for frequency-dispersion. Once trained, the model can predict the frequency-dispersive behavior of the SiC devices under various testing conditions, including changes in voltage, current, and frequency. As the frequency content in future power conversion circuits containing wide bandgap semiconductors will continue to increase, the framework presented in this work can be used to predict the performance of forthcoming GaN and SiC devices, as well as other promising fast-switching ultra-wide bandgap materials.

Effect of Substrate Materials on Circuit Performance of Current and Future GaN Devices

Semiconductor devices based on GaN are playing a critical role in the low and high voltage power electronics arena. Low voltage GaN devices can be manufactured in economically viable fashion using lateral HEMT technologies. Higher voltage (> 1 kV) devices will require vertical architectures in order for GaN to achieve its performance limits, which are theoretically superior to SiC [2], [3], [4]. A significant challenge in fabricating vertical GaN devices is the ability to find low-cost compatible and reliable substrates. Modeling and simulation efforts can be undertaken to determine how substrates can impact the performance of current and future GaN devices. As the physics of lateral GaN HEMT technology are well-established, modeling the effect that various substrate materials have on the performance of these devices can be used as a precursor to understand how different substrates can impact the behavior of future vertical GaN devices. The work conducted on this grant endeavors to develop a framework which allows better understanding of how various substrate materials can affect the performance of GaN devices. A finite element model of a fabricated 600 V GaN HEMT is developed using technology-computer aided design (TCAD). After empirically validating the static characteristics of the device, the substrate material is then altered, from Si to Sapphire, and also to GaN. The resulting effect on the capacitance of the device is then assessed. As the capacitance of the device determines its switching characteristics, this work is essential to understanding how various substrate materials can impact the performance of future high voltage GaN devices.

Although the work performed in this investigation utilizes a lateral GaN HEMT as the device under test, the methodologies undertaken, and moreover the framework can be applied to future high voltage vertical GaN devices, currently under consideration. Such investigations of high voltage vertical GaN devices are the scope of PI Khanna's current ONR grant (2021 – 2024), which is outside the scope of this report.

Reliability of Current and Future GaN Devices

Lifetime and reliability testing of current and next generation GaN devices is critical to understanding performance degradation, and for designing future robust semiconductors [5]. The reliability work conducted under this grant investigated degradation mechanisms of lateral GaN HEMTs in various application and testing circuits. Although the work focused on lateral GaN technology, the methods utilized can be readily adapted to vertical GaN architectures. In this way, the nuances between design criteria for low voltage GaN (lateral structures) and high voltage GaN (vertical structures) can be better understood. Design modifications can then be proposed to achieve robust performance across the entire spectrum of low and high power GaN devices.

In one study of this project, five distinct GaN-based boost converters were tested concurrently. All five converters had identical operating parameters and features. The only difference was the maximum gate-driving voltage utilized for each of the five GaN devices. The maximum driving voltage for each respective converter was 5.0 V, 5.2 V, 5.4 V, 5.6 V, and 6.0 V respectively. It is known that higher driving voltages will improve both switching and conduction behavior of the device. However, the insulative gate material used in GaN HEMTs is known to be sensitive to high potentials, allowing for a trade-study to find the optimal driving voltage. The analysis of this boost converter experiment yielded new understandings of failure mechanisms in GaN HEMTs which are also described in this report. For the first time, correlation and causation are observed between overshoot voltage on the gate-terminal, as well as injected gate current. A direct connection between overshoot, gate-current and the converter's efficiency is also established in the investigation.

Conventional step-stress studies are also pursued. In this test, the drain and source terminals are shorted to ground, thereby eliminating the possibility of current-collapse-related device degradation. A physical understanding for all the observed phenomena is provided in this report.

Integration of TCAD w/ Circuit Simulation for Rapid Optimization of Wide Bandgap Semiconductors

The power electronics modeling and simulation community continuously grapples with the challenge of balancing the trade-off between a simulation's fidelity and convergence time [6]. In some cases, a simulation will converge extremely rapidly, at the expense of precision and accuracy. In other cases, a simulation will provide very accurate results, but will take too long to converge. This issue is further exacerbated by the need to conduct circuit-level simulations of physics-based models as well as behavioral models. Physics-based models contain several semiconductor device parameters, which have real and physical meanings. Behavioral models contain simplified mathematical parameters, which do not have a physical basis. Both models can produce accurate results, however, the physics-based model will take considerably longer to simulate than the behavioral model. On the other hand, the physics-based model allows for simulated circuit-level phenomena to be correlated directly to real physical parameters. That is, a meaningful sensitivity analysis can be undertaken with physics-based models, which allows one to understand how various parameters influence the circuit-level behavior of the device. Such an advantage is not offered by faster behavioral models since their parameters do not contain physical meaning.

The work conducted under this grant for this project seeks to develop an integrated framework for device physics models and behavioral circuit simulation models. Device physics models are developed in TCAD, and behavioral characteristics are exported into circuit simulation. An objective is defined for the circuit-level model, such as a targeted efficiency, or operating temperature. If the objective is not met, a parallel optimization loop interacts with the device physics simulation to determine the parameter values necessary

for the objective to be met. This framework will allow for rapid prototyping of semiconductor devices which are optimized for the application in which they are implemented. The established framework developed under this grant was used to set the stage for PI Khanna's current grant (2021 – 2024) which allows for fabrication of high voltage vertical GaN diodes, optimized for their application. The vertical GaN diodes, currently under consideration are outside the scope of this report. The framework developed is within the scope of this report and is elucidated further in the following section.

2. Technical Results

The results obtained from the four projects above are provided in this section as follows.

2.1. Modeling and Characterization of High-Frequency Dispersion Effects in Wide Bandgap Semiconductors

Fig. 1 provides an overview of the framework that was developed to model frequency-dispersion in wide bandgap semiconductors. The framework works as follows. Initially a static semiconductor device model is developed using an integrated MATLAB-SPICE scheme. The well-known Level 3 SPICE MOSFET model is chosen as the core model, although any stable model can be utilized. Empirical static characteristics such as current-voltage (IV) measurements are fed into the framework. The parameters within the Level 3 MOSFET are varied in a manner to compute the difference, or "cost" between the simulated static characteristics and the empirical static characteristics. An optimization algorithm is used to minimize this cost so that there is essentially no observable difference between the simulated and measured data. This results in the IV characteristics seen in Fig. 2, for the 1.2 kV SiC MOSFET under consideration.

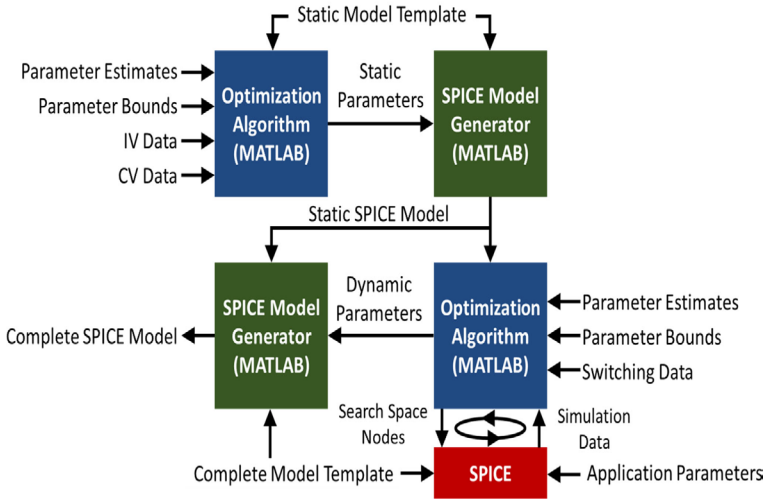


Figure 1. System architecture for modeling frequency dispersion in wide bandgap semiconductors.

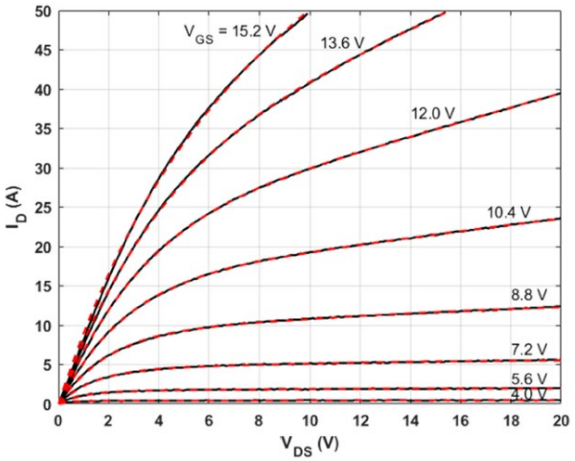


Figure 2. Experimental and simulated forward conduction behavior for 1.2 kV SiC MOSFET.

As seen in Fig. 1, the modeling framework captures the empirical data extremely well, with good fits in both the linear and saturation regions of operation. It is also worth noting that the gradual transition between the two regions of operation, which is a unique feature of SiC MOSFETs, is also accurately modeled. The CV characteristics of the device were also modeled. Once the static model is set using the "Spice Model Generator" seen in the framework architecture shown in Fig. 1, a dynamic device model is the developed in SPICE. Empirical switching data from a converter or double pulse test (DPT) is fed into the simulation. A cost is determined between the empirical transient switching data and the simulated behavior using the same optimization algorithm previously described. The per-terminal junction capacitances of the device model and the parasitic stray inductances o the simulations are varied so that the cost is minimized. This results in the simulated and empirical turn-off data seen in Fig. 3.

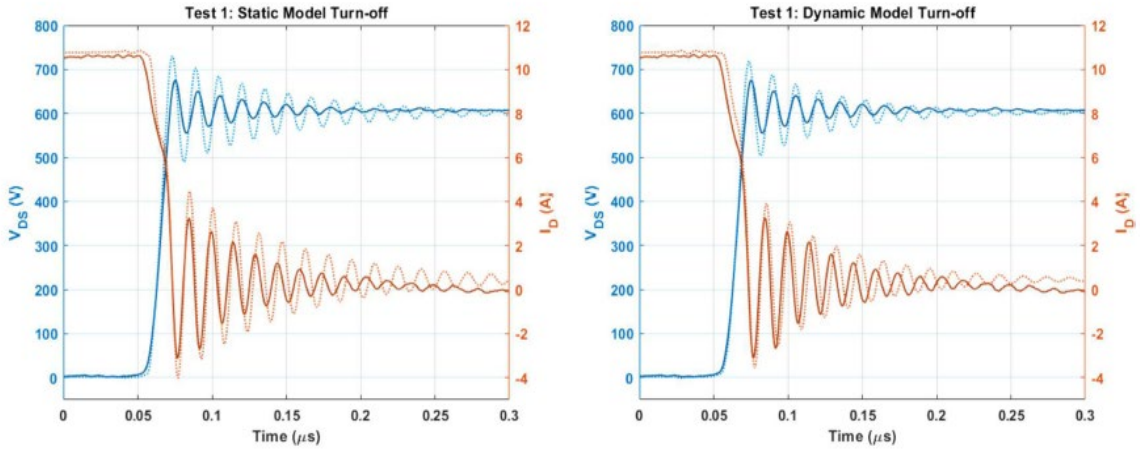


Figure 3. Empirical and simulated switching data for (a) static model turn-off and (b). dynamic model turn-off.

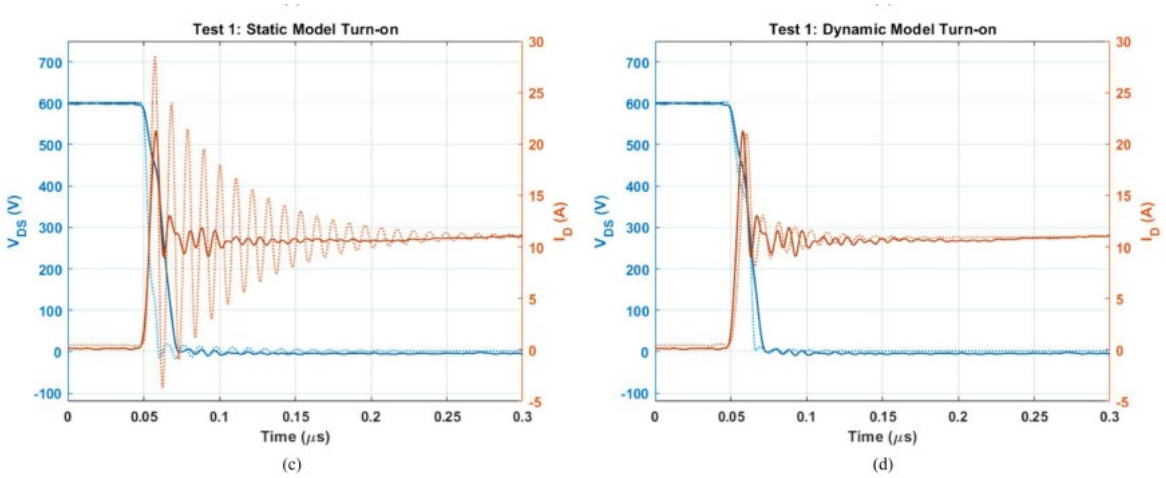


Figure 4. Empirical and simulated switching data for (a) static model turn-off and (b) dynamic model turn-off.

Fig. 3(a) shows the model performance when there is no dynamic tuning. That is the capacitances and inductances are not varied, and only the static model is used to predict device performance. Fig. 3(b) shows the results obtained when there is both static and dynamic tuning. That is, the results in Fig. 3(b) are provided by a model that allows the capacitances and inductances to vary. Comparison of the waveforms seen in Fig. 3 clearly demonstrate that the dynamic model is superior in predicting the turn-off behavior of the SiC MOSFET. A similar comparison is provided in Fig. 4 for turn-on behavior, where again the dynamic model provides better prediction capability than the static model.

A final step to validating the framework is to test its functionality in a different operating point with the dynamic tuning loop removed. That is, the trained model that was used to yield the results given in Figs. 3 and 4 must then be implemented in an "orthogonal" operating condition to assess its predictive capability. The data in Figs. 3 and 4 is taken at a nominal operating condition of 600 V and 11 A. The orthogonal operating condition is 600 V and 22 A. Comparison between simulated and measured turn-off and turn-on behaviors, in the orthogonal operating condition are provided in Figs. 5 and 6 respectively.

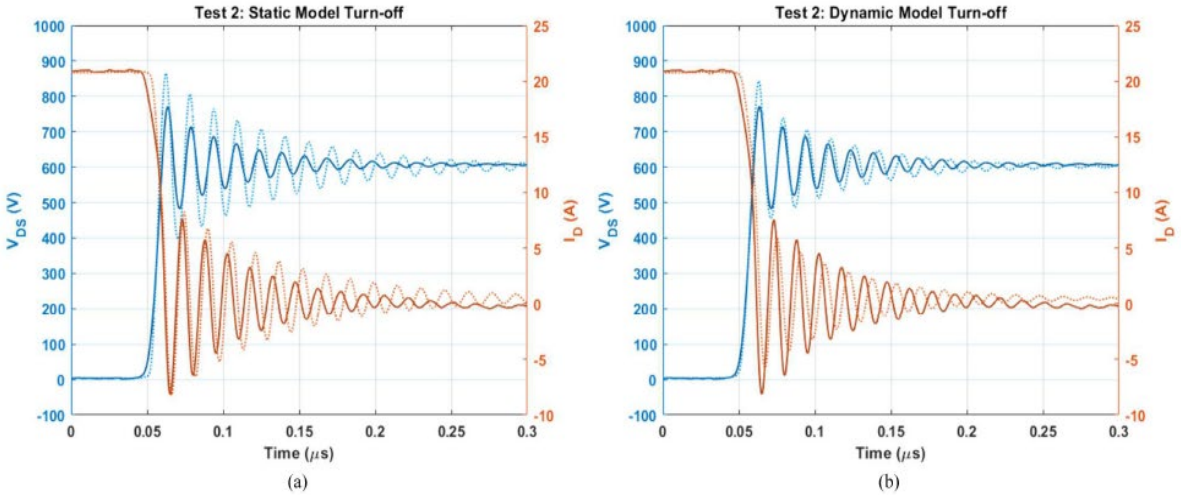


Figure 5. Orthogonal dataset. Empirical and simulated switching data for (a) static model turn-off and (b). dynamic model turn-off.

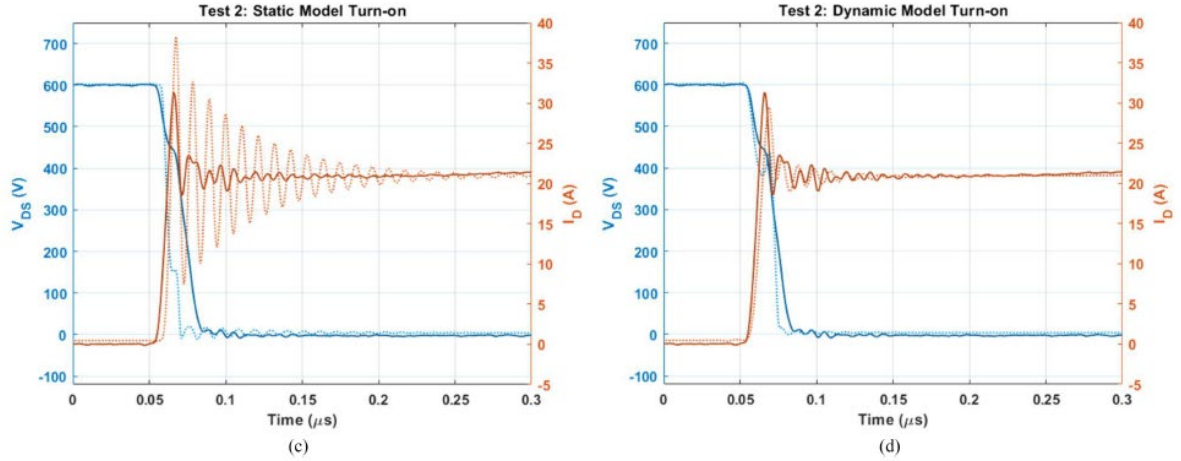


Figure 6. Orthogonal dataset. Empirical and simulated switching data for (a) static model turn-off and (b) dynamic model turn-off.

As can be seen in Figs. 5 and 6, the dynamic model is better than the static model at predicting the behavior of the SiC MOSFET in the orthogonal operating condition. This proves that the capacitances and inductances of the circuit are indeed varying with the spectral content contained in the circuit, and provisions to account for this behavior must be included in next generation modeling infrastructures of wide and ultra-wide bandgap semiconductors. PI Khanna and his team published this work in [7] for SiC, and then extended this modeling framework to commercially available GaN HEMTs, as reported in [8].

2.2. Effect of Substrate Materials on Circuit Performance of Current and Future GaN Devices

The device modeled in this work is a GaN/AlGaN HEMT structure grown on a Si substrate produced by HRL Laboratories, LLC. A two-dimensional cross section of the device is shown in Fig. 7. At zero bias, strain between the GaN channel layer and the thin AlGaN layer produces a piezoelectric charge at the interface that will result in the formation of a two-dimensional electron gas. The simulated structure consists of over 100,000 meshed elements.

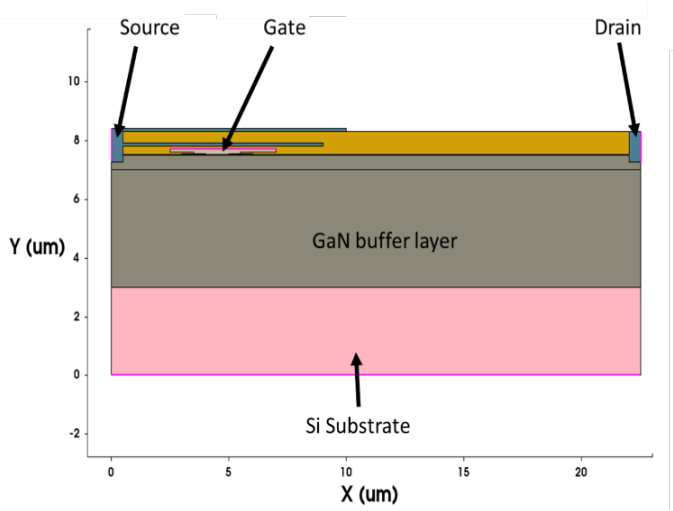


Figure 7. Cross section of modal recessed gate GaN FET.

A validated TCAD model requires accurately capturing the forward and transfer current-voltage characteristics of the device. This is accomplished with proper consideration of the charge carrier concentration in the two-dimensional electron gas formed at the AlGaN/GaN interface. The piezoelectric coefficients for the device are set using values previously reported in the literature. The piezoelectric charge is compensated by donor traps at the SiN/AlGaN interface. For modeling transfer characteristics, the threshold voltage is captured by use of fixed acceptor charges under the gate of the device. To obtain accurate forward curves, the on-resistance of the device, R_{ON}, is adjusted based on mobility degradation due to scattering of the acceptor charges under the gate. Radiative and Shockley-Reed-Hall recombination was

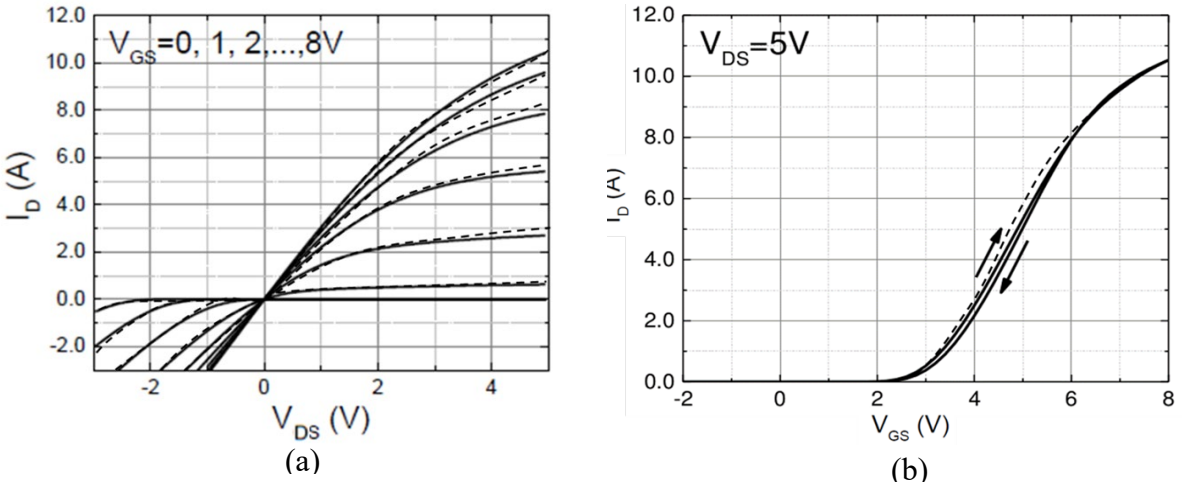


Figure 8. Current-voltage characteristics. Empirical lines are solid and modeled lines are dotted. (a) Forward curves. (b) Transfer curves.

taken into consideration due to the high currents in the device. These considerations lead to the modeled and measured forward and transfer curves obtained in Fig. 8.

To adequately model the capacitance-voltage characteristics of the GaN HEMT, the device's geometry was taken into consideration. Imaging from a tunnelling electron microscope allowed for refinement of the field-plate dimensions. These dimensions have direct influence on the capacitance-voltage characteristics of the device. Electric field modulation is known to have significant effect on the capacitance-voltage characteristics of a device, which thus required accurate modeling of the silicon nitride (SiN) layer that was used for field passivation. This leads to the comparison of modeled and measured capacitance-voltage characteristics seen in Fig. 9.

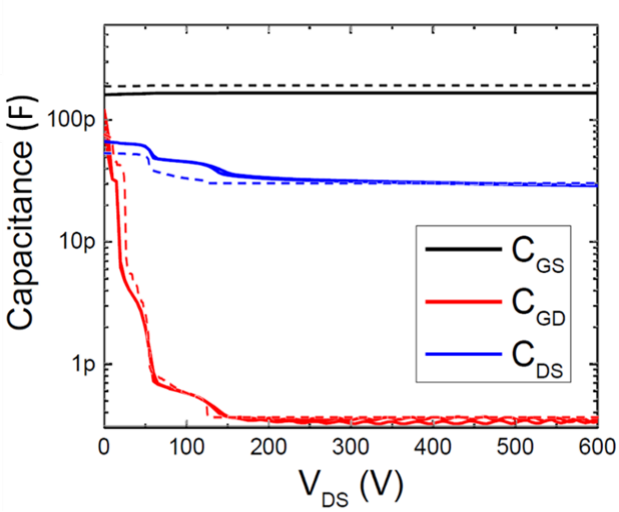


Figure 9. Capacitance-voltage curves. Solid lines are measured, and dotted lines are modeled.

With the model fully validated in terms of its static-operating characteristics, the objective of the work was to assess how different substrate materials would impact the capacitance-voltage characteristics of the device. This understanding would also reveal how different substrate materials would impact the switching performance of the device. In addition to the Si substrate used for the nominal device, two alternative substrates were also considered. Sapphire was one of the alternatives and GaN was the other. The advantages and disadvantages of the three substrate materials (including the nominal Si) are determined by their cost, as well as their lattice mismatch with the conductive AlGaN/GaN channel. In terms of cost, the Si substrate material would be the least expensive, followed by Sapphire, and then finally GaN. However, in terms of lattice matching, the native GaN substrate would intuitively be the favored substrate choice, followed by Sapphire, and then Si. The impacts that these different substrate materials have on the drain-source (C_{DS}) and gate-drain (C_{GD}) capacitance of the HEMT was then characterized. As the gate-source capacitance has relatively little dependence on the drain-source voltage (as seen in Fig. 9), this capacitance was left out of the analysis.

Fig. 10 depicts the effect of the three substrate materials on the two junction capacitances of interest. Fig. 10(a) shows the effect on C_{DS} while Fig. 10(b) provides the effect on C_{GD}. As can be seen in Fig. 10, the lowest observed C_{DS} and C_{GD} are obtained when the GaN substrate is utilized. Intermediate values for these capacitances result when the Sapphire substrate is used. Finally, the highest observed capacitances are yielded by use of the Si substrate. With these measured capacitances, corresponding switching characteristics are provided in Fig. 11, which depicts transient voltage and current waveforms in both turn-on and turn-off conditions. Fig. 11(a) shows three different simulated turn-on behaviors for the GaN HEMT

when each of the three substrate materials are used. Fig. 11(b) depicts the same for turn-off behavior. As can be seen in Fig. 11, the GaN substrate yields the fastest switching transitions in terms of both voltage and current, for turn-on and turn-off characteristics. It is instructive to note, however, that the difference in switching performance resulting from the Sapphire substrate and the GaN substrate may not be worth the extra cost of the GaN substrate. A more comprehensive cost-performance analysis could reveal that the Sapphire substrate would be the most optimal choice.

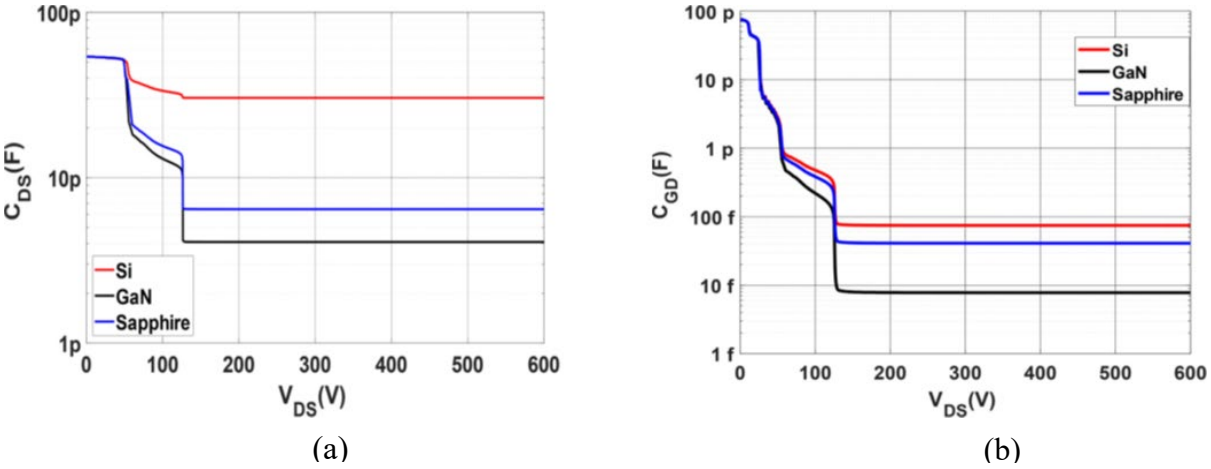


Figure 10. Capacitance-voltage characteristics of GaN HEMT for three substrates. Empirical lines are solid and modeled lines are dotted. (a) C_{DS}. (b) C_{GD}.

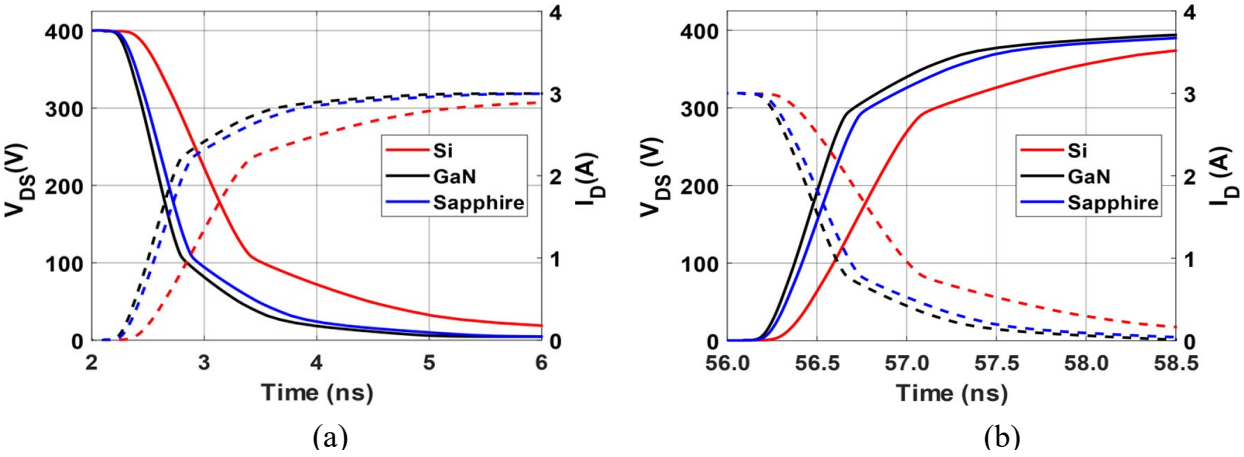


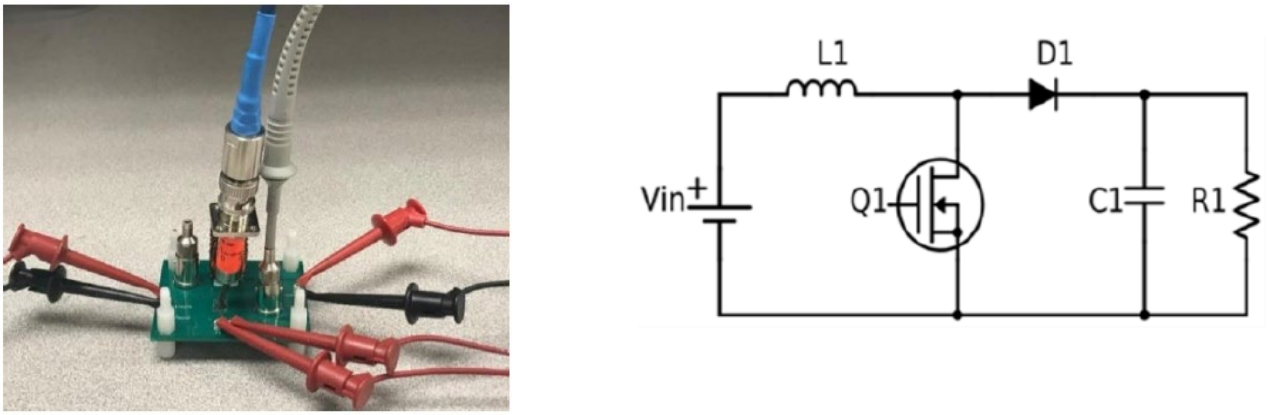
Figure 11. Switching characteristics of GaN HEMT for three substrates. Solid lines are voltage and dotted lines are current. (a) Turn-on behavior. (b) Turn-off behavior.

PI Khanna and his team published the development of the model first in [9], and then extended the utility of the model to assess the effect of substrate choice on the device's transient performance, which was subsequently reported in [10].

2.3. Reliability of Current and Future GaN Devices

Five empirical GaN-based boost converters were developed for the reliability assessment. Fig. 12 shows the empirical setup as well as the converter topology. The parameters and design of each converter were identical except for the gate-driving voltage. The first converter had a gate-driving voltage of 5.0 V; the second had a gate-driving voltage of 5.2 V, and the third a gate-driving voltage 5.4 V. The fourth and fifth

converter had gate-driving voltages of 5.6 and 6.0 V respectively. A step-frequency stress analysis was performed to analyze the device's failure mechanisms at different forward biased gate voltages. The critical degradation point of the devices was closely monitored in terms of converter efficiency, gate current, and gate voltage overshoot. In this experiment, the frequency was varied from 100 kHz to 1.5 MHz in increments of 100 kHz every three minutes at a given steady-state gate-driving voltage.



(a) (b)

Figure 12. Prototype Boost converter for reliability test. (a) Empirical test-board. (b) Converter topology.

The step-frequency stress analysis allowed for several significant observations. While operating at the recommended gate-voltage, the converter remained consistent in performance, and no unexpected significant drops in efficiency were recorded. However, when the steady-state driving-voltage was increased to 5.8 V or higher, a significant drop in efficiency was recorded after some time. The drop in efficiency occurred concurrently with an increase in gate current. The efficiency changes versus frequency and its comparison with gate current and gate voltage overshoot can be seen in Figs. 13 and 14 for two devices – Part Q and Part T.

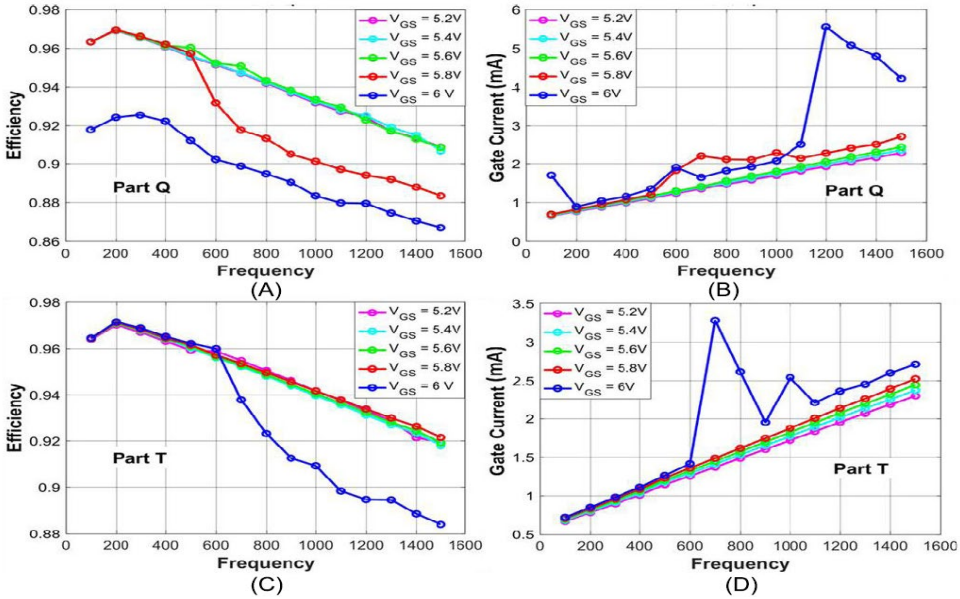


Figure 13. (a) and (c) Efficiency vs frequency for Part Q and Part T. (b) and (d) Gate current vs frequency for Part Q and Part T.

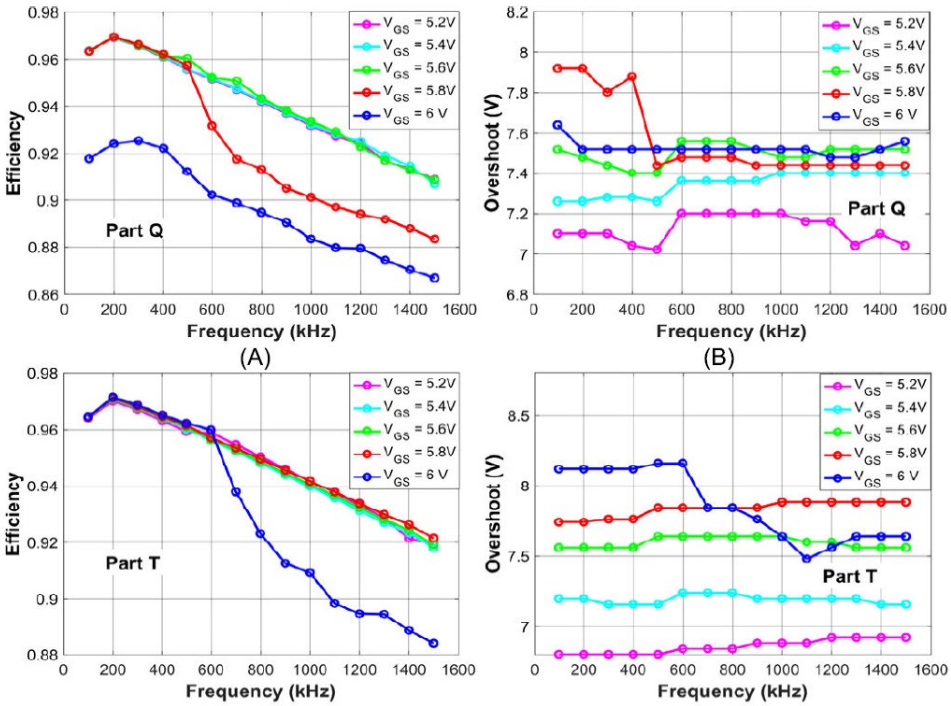


Figure 14. (a) and (c) Efficiency vs frequency for Part Q and Part T. (b) and (d) Gate voltage overshoot vs frequency for Part Q and Part T.

Part Q and Part T were tested in the boost converter from 100 kHZ to 1.5 MHz with 100 kHz increment as shown in Figs. 13 and 14. After the entire spectrum of frequencies was swept, the gate-driving voltage was incremented by 0.2 V and the frequency sweep was repeated. This processed repeated from 5.2 V to 6.0 V of gate-driving voltage. At each gate-driving voltage and frequency pair, the efficiency of the converter, gate current, and gate voltage overshoot was recorded. As shown in Fig. 13(a) for Part Q at a gate-driving voltage of 5.8 V and frequency of 500 kHz, the performance of the converter declines due to degradation of the device. It was observed that the overall efficiency of the devices decreases as frequency increases, with a maximum recorded efficiency of 97% around 200 kHz when operating a driving voltage of 5.2 V, 5.4 V, 5.6 V, and 5.8 V. For the first three gate-driving voltages, the overall efficiencies decrease by approximately 0.5% per 100 kHz with the lowest efficiency of 91% recorded at 1.5 MHz. However, for a gate-driving voltage of 5.8 V, a sharp drop in efficiency was observed was observed from 96% at 500 kHz to 93% at 600 kHz. This drop in efficiency corresponds to the instant when the gate current increases, as observed in Fig. 13(b). Similarly, in Fig 13(c) and Fig 13(d), a drop in efficiency, and corresponding gate current increase are observed for Part T at 6 V. These observations were noted for numerous devices with degradation consistently occurring between 5.8 V and 6.0 V, at frequencies between 400 and 600 kHz. Corresponding declines in overshoot are also noted at these instances of interest.

To further support the results observed in Figs. 13 and 14, another stress experiment was conducted. In this experiment, Part U was held at a constant gate-driving voltage of 5.6 V for periods of 60 minutes or greater. The efficiency of the converter, gate-source voltage overshoot, and gate-current were all monitored and measured. Three trials of this test were conducted on Part U, at a gate-driving voltage of 5.6 V for 60 minutes. In all cases, the same Part U was utilized. For purposes of naming convention, the first trial with Part U was termed Part U1, and the second trial termed Part U2 etc. In the first three trials with a constant-gate driving voltage of 5.6 V, the efficiency of the converter, gate-voltage overshoot, and gate current all remained at nominal levels. However, in the fourth trial, termed Part U4, the gate-voltage was increased to 5.8 V. As previously observed in Figs. 13 and 14, this is the gate-driving voltage where degradation occurs. These observations are further validated as seen in the data shown in Fig. 15. Shown in Fig. 15(a) is a time-

dependent comparison of efficiency and overshoot for Part U3 and Part U4. Fig. 15(b) provides a comparison of efficiency and gate-current for Part U3 and Part U4. As seen in Fig. 15(a) and Fig. 15(b), Part U3 does not degrade and maintains adequate performance throughout the 60 minute test at a steady-state driving voltage of 5.6 V. However, for Part U4, indications of degradation are observed after five minutes of continuous operation at steady-state driving gate-driving voltage of 5.8 V. This is evident by the drop in efficiency, reduction in gate-voltage overshoot, and fluctuation in gate-current for Part U4.

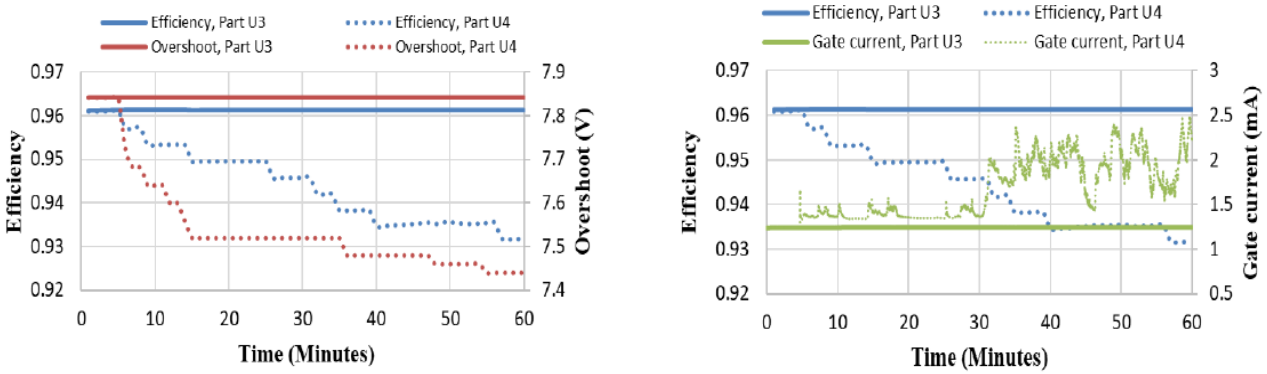


Figure 15. Efficiency, overshoot, and gate-current vs time for Parts U3 and U4. (a) Efficiency and overshoot vs time. (b) Efficiency and gate-current vs time.

To describe these effects, the band structures and current mechanisms of the devices under test can be examined for the possible tunneling and trap effects observed in Figs. 13, 14, and 15. The main current mechanisms for this device are: thermionic emission of electrons and associated diffusion, thermionic field emission and its associated diffusion. It is possible that significant diffusion current may replace some or all of the indicated thermionic current. Fig. 16 then identifies the main theorized trapping effects at play in this device. These are namely trap-assisted tunneling through shallow interface traps, and Shockley-Reed-Hall recombination through shallow and deep traps. These highly non-linear effects can then be used to account for the non-ideal behavior observed in Figs. 13, 14, and 15. PI Khanna and his team published these results and theories in [11].

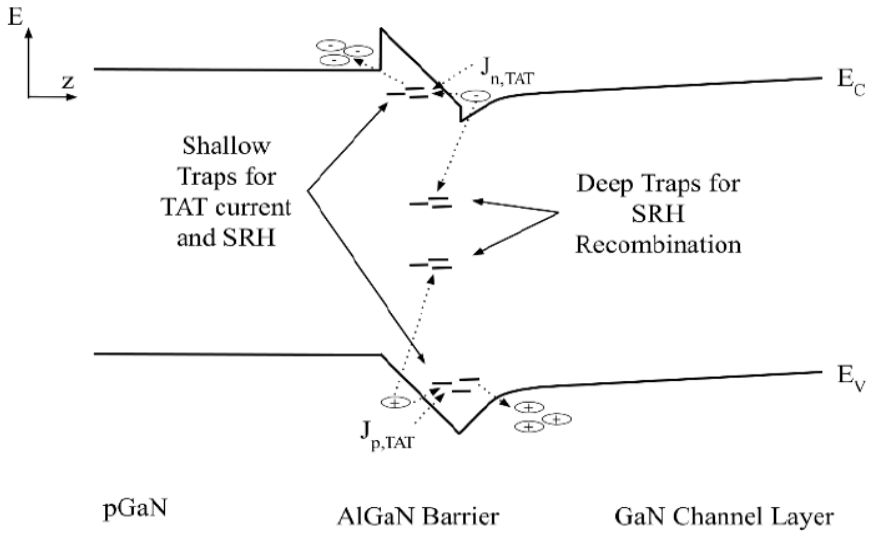


Figure 15. Efficiency, overshoot, and gate-current vs time for Parts U3 and U4. (a) Efficiency and overshoot vs time. (b) Efficiency and gate-current vs time.

2.4. Integration of TCAD w/ Circuit Simulation for Rapid Optimization of Wide Bandgap Semiconductors

Fig. 16 shows the proposed framework for integrating device physics models into circuit simulation, while running a parallel optimization algorithm so that targeted application metrics can be met. As seen in Fig. 16, an integration scheme is used to link TCAD physics platforms to circuit simulation. In the circuit simulation, the device is implemented in any power electronic application, such as an electric navy ship, renewable energy installation, etc. A targeted application metric is chosen to be met, such as efficiency, operating temperature, power density, etc. If the application metric is not met, an optimization algorithm calculates the difference between the simulated metric and the targeted goal, and then modifies the device physics parameters accordingly so that the metric can be met on the next iteration. This process is completed in a streamlined fashion in order to rapidly prototype semiconductors that are optimized for their intended application goal.

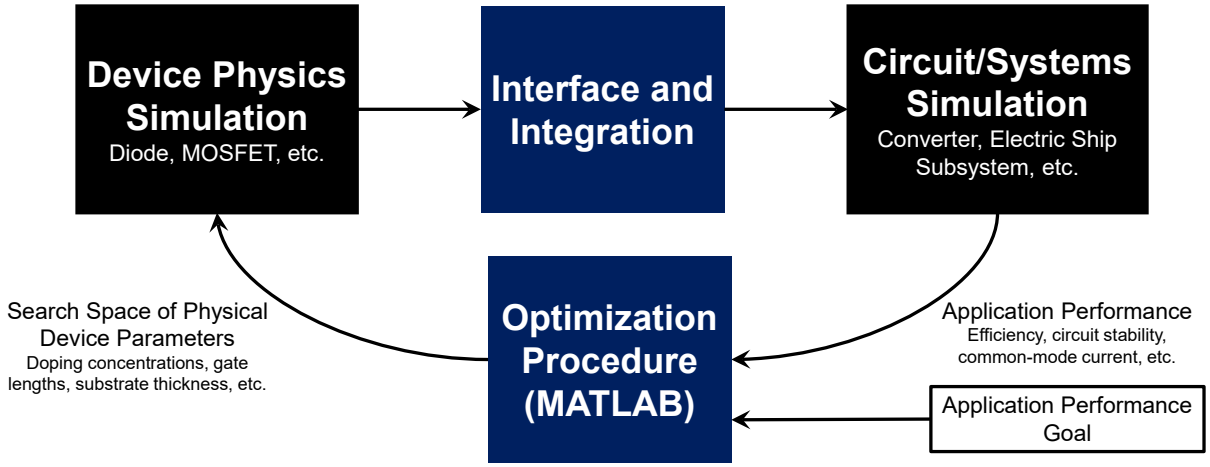


Figure 16. Proposed modeling infrastructure. Optimization of device model parameters to ensure fill performance entitlement for WBGs devices.

A theoretical pGaN-gated 200 V HEMT device was designed in TCAD, seen in Fig. 17. This HEMT jas a similar structure to devices made by *Efficient Power Conversion Corporation*. The device in Fig. 17 was optimized according to two device-physics parameters, the AlGaN doping concentration, and the gate-drain length. These parameters have competing influence on switching and conduction loss for a semiconductor device. That is, as one parameter increases in value, the switching loss becomes less while the conduction loss goes up. The opposite is true for the other parameter, leading to a classic optimization problem. Such problems are well known in the semiconductor industry, however have never been solved with real-time optimization, as proposed here. Initial best guesses for these two parameters are used to minimize the energy losses in a Boost Converter. Three initial guesses for these two parameters lead to three different sets of IV and CV characteristics. Each set of curves is then exported from TCAD and used to set three simulation models of the device in the MATLAB-SaberRD Interface seen in Fig. 16. Each device is then implemented in a Boost converter to minimize total losses due to the semiconductor.

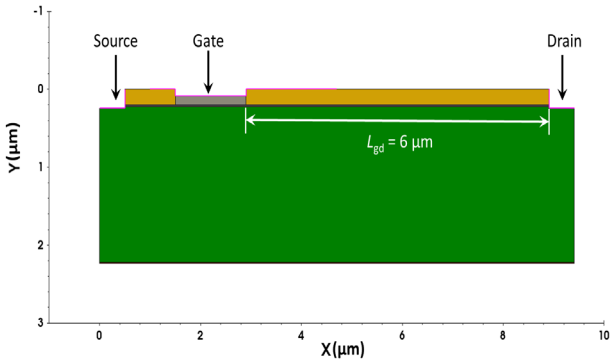


Figure 17. Theoretical pGaN gate device designed in TCAD.

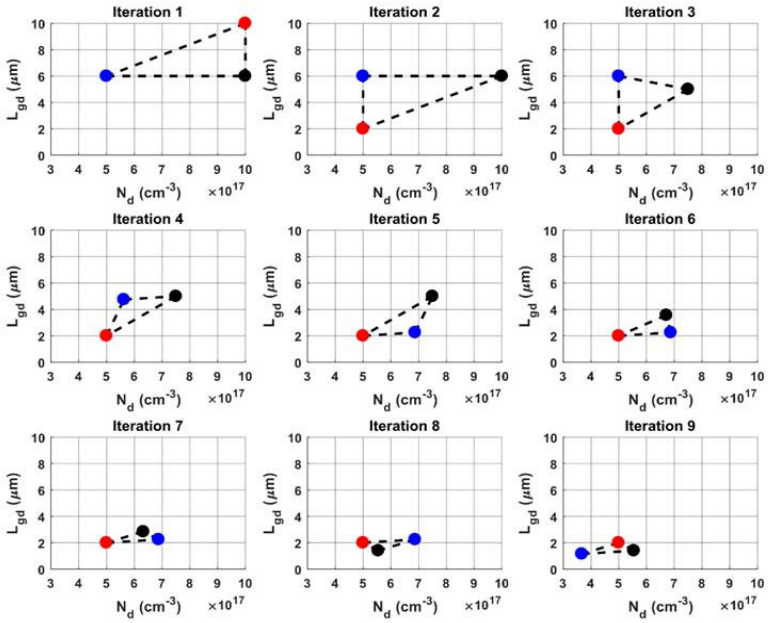


Figure 18. Simplex pairs of L_{GD} and N_d at each iteration for Boost converter case study

Each simplex point was then implemented in the downhill simplex [12]. Fig. 18 shows how each simplex pair of the two device parameters is *reflected, expanded, contracted, and shrunk*, over several iterations in order to design and optimize a device that minimizes energy loss. Fig. 19 illustrates the calculated energy loss after each iteration for the corresponding three simplex points. As seen in both Figs. 18 and 19, the procedure iterates nine times before an optimal design is found. The optimal design results from Simplex Point 3, with final values of 3.7673 x 10^{17} cm^{-3} for N_d and 1.156 µm for L_{GD}. As seen in Fig. 19, these design parameters result in a calculated energy loss of 51.8 mJ. Thus, the proposed optimization procedure theoretically leads to an approximate 40% reduction in energy loss due to the switching transistor. Fig. 20 illustrates the final optimized device.

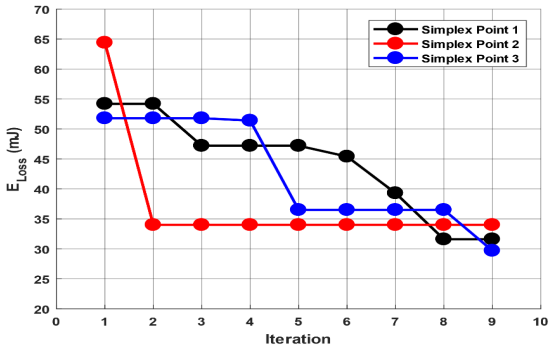


Figure 19. Calculated E_{loss} for each simplex point over nine iterations. Colors correspond with those seen in Fig. 18 for each simplex point.

Though promising, the results would be more compelling with experimental corroboration. Using data provided to the PI by Naval Research Lab, the modeling and optimization process described above will be empirically validated for vertical GaN diodes. The procedure will be applied to both a reliability thrust as well as the high voltage proof of concept thrust. Furthermore, particular emphasis will be placed on reliability parameters, such as substrate doping, electron mobility, carrier lifetime and others. These are the

parameters that exhibit degradation over time, and lead to failure in various applications. This process will also be extended to circuit simulation in order to calculate absolute maximum parasitic inductance values, which also cause circuit level failures of wide bandgap semiconductors.

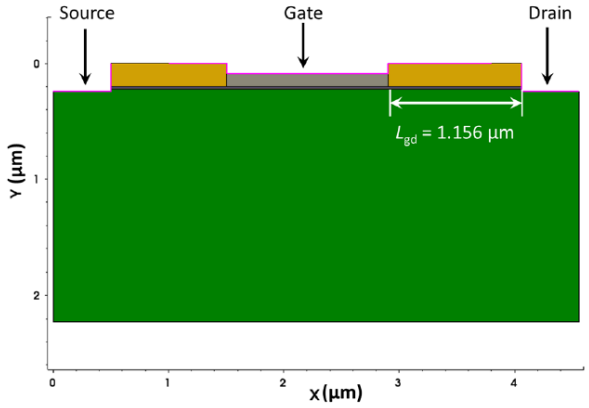


Figure 20. Best pGaN-gated FET for minimizing loss after nine iterations. Design has 3.7673 x 10^{17} cm^{-3} for N_d and 1.156 µm for L_{GD}.

PI Khanna and his team reported on this methodology in [13], and more recently, under a new ONR grant, have extended the framework to vertical GaN diodes *with* empirical corroboration, as reported in [14] and [15]. References [14] and [15] have been developed under a new ONR grant, and are outside the scope of the herein presented report.

3. Publications Resulting from Research Grant

- M. R. Hontz, R. Chu, and **R. Khanna**, "Effect of substrate choice on transient performance of lateral GaN FETs," in *IEEE Journal of the Electron Devices Society*, vol. 8, no. 1, pp. 331-335, December 2020. DOI: 10.1109/JEDS.2020.2981607

- A. J. Sellers, M. R. Hontz, **R. Khanna**, A. N. Lemmon, B. T. Deboi, and A. Shahabi, "An automated model tuning procedure for optimizing prediction of dispersive behavior in wide bandgap semiconductor FETs," in *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 12252-12263, November 2020. DOI: 10.1109/TPEL.2020.2986928

- R. L. Kini, S. Dhakal, S. Mahmud, A. J. Sellers, M. R. Hontz, C. Tine, and **R. Khanna**, "An investigation of frequency dependent reliability and failure mechanism of pGaN gated GaN HEMTs," in *IEEE* Access, vol. 8, pp. 137312 – 137321, August 2020. DOI: 10.1109/ACCESS.2020.3011453

- J. P. Kozak, A. Barchowsky, M. R. Hontz, N. Koganti, W. E. Stanchina, G. F. Reed, Z-H. Mao, and **R. Khanna**, "An analytical model for predicting turn-on overshoot in normally-off GaN HEMTs," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 99-110, March 2020. DOI: 10.1109/JESTPE.2019.2947152

- W. Collings, T. Nelson, A. J. Sellers, **R. Khanna**, A. Courtay, S. Jimenez, and A. N. Lemmon, "Optimization algorithms for dynamic tuning of wide bandgap semiconductor device models," in the *2021 IEEE Applied Power Electronics Conference*, Phoenix, AZ, USA, pp. 2427-2433, June 2021. DOI: 10.1109/APEC42165.2021.9487029

- M. R. Hontz, W. Collings, A. Courtay and **R. Khanna**, "An optimization framework for GaN power device design and applications," in the *2019 IEEE Workshop on Wide Bandgap Power Devices and Applications*, Raleigh, NC, USA, pp. 302-309, October 2019. DOI: 10.1109/WiPDA46397.2019.8998872

- C. New, A. N. Lemmon, B. T. Deboi, M. R. Hontz, A. J. Sellers, and **R. Khanna,** "Comparison of methods for switching loss estimation in WBG systems," in the *2019 IEEE Electric Ship Technology Symposium*, Washington D.C., USA, pp. 569-576, August 2019. DOI: 10.1109/ESTS.2019.8847837

4. Future Work

The work conducted on this grant lays the foundation for simulation and fabrication of future high voltage vertical GaN devices. Currently, PI Khanna and his team are working with personnel from the Naval Research Lab to design high voltage vertical GaN diodes, in a project entitled **PROMPT: P**rocedure for **R**apid **O**ptimization and **M**odeling of **P**ower **T**echnologies. This project is aimed toward *understanding the fundamental modeling techniques necessary to allow WBGs to achieve their full performance entitlement in terms of voltage handling capability and reliability*. To empirically validate the proposed modeling framework, the PI will be provided data from NRL as mentioned in the attached support letter. The framework will consist of two thrusts, one meant for manufacturability and **reliability**, and the other for proof of concept. A high-level description of both thrusts is illustrated in Fig. 21. The manufacturability thrust will include modeling and design, in increments, of 1.2 kV, 3.3 kV, and 6.5 kV vertical GaN diodes that are fabricated using homoepitaxial growth. This thrust will focus on reliability of the GaN diodes, with a particular emphasis on substrates. The proof of concept thrust will include modeling and design, in increments, of 5 kV, 10 kV, and 20 kV vertical GaN diodes which are fabricated with thick epitaxy and low doping. For both thrusts, several different devices of varying sizes and ratings will be modeled. From the various trends and patterns observed in device behavior, scaling rules will then be developed to predict the performance of future higher voltage GaN devices that are currently not available. The research focused objectives of this proposal are described in technical detail next, followed by a discussion on considerations for validation. Preliminary results on developing the first iteration of the GaN diodes, and methods for developing scaling rules are also discussed. **The proposed framework is extensible to promising technologies of the future such as Ga_2O_3 or diamond.**

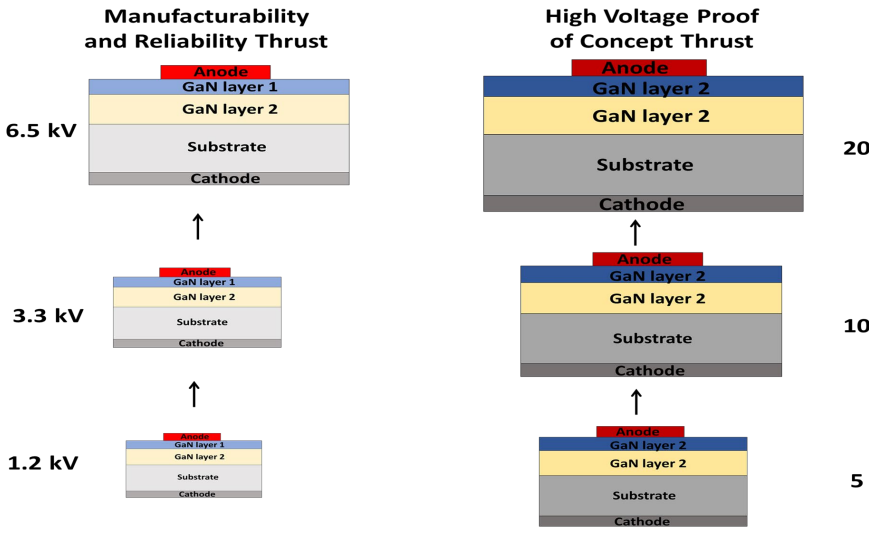


Figure 21. Two high voltage vertical GaN diode thrusts.

5. Personnel

Graduate Students

- Dr. Michael Hontz: PhD student; August 2015 – May 2019: Dr. Hontz's PhD studies were funded in part due to this grant. He completed his PhD in May of 2019 and is currently employed at the Naval Surface Warfare Center in Philadelphia, PA.

- Dr. Andrew Sellers: PhD student; August 2016 – May 2020: Dr. Seller's PhD studies were funded in part due to this grant. He completed his PhD in May of 2020 and is currently employed at Typhoon-HIL in Boston, MA.

- Mr. William Collings: PhD student; August 2020 – Present time: Mr. Collings' PhD studies were funded in part by this grant. He conducted an internship at the Naval Research Lab during Summer 2021. He is currently conducting a summer-internship at Typhoon HIL, Boston, MA.

- Mr. Tolen Nelson: PhD student; August 2020 – Present time: Mr. Nelson's PhD studies were funded in part by this grant.

Principle Investigator

- Dr. Raghav Khanna: Associate Professor, EECS Department University of Toledo. Dr. Khanna conducted and supervised the research activities for this grant.

6. Acknowledgement

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