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A SOFTWARE/HARDWARE (SW/HW) SENSORY-RICH MONITORING SYSTEM FOR SYSTEM-ON-CHIP (SoC) DESIGNS

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Brown University

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14. ABSTRACT

The project developed an integrated SW/HW monitoring system for System-on-a-Chip (SOC). The effort has three elements. One, hardware sensors to measure spatial and temporal features such as temperatures, voltages, and process variability. Two, a software processing layer to provide a sensory-rich environment to process, extrapolate, and fuse the measurements of the sensors. Three, conducted comprehensive post-silicon characterization and calibration techniques to characterize and minimize the errors in the sensors.

15. SUBJECT TERMS

System-on-a-Chip integrated monitors, on-chip temperature, voltage, and process variability sensors, sensor fusion, chip characterization, chip calibration

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1 SUMMARY

The *overarching goal* of the project is to develop an integrated SW/HW monitoring system for system-on-a-chip (SoC) designs that includes (1) hardware sensors to measure spatial and temporal features such as temperatures, voltages and process variability; (2) a software processing layer to provide a sensory-rich environment to process, extrapolate and fuse the measurements of the sensors; and (3) conduct comprehensive post-silicon characterization and calibration techniques to characterize and minimize the errors in the sensors.

In this project we designed and taped-out two chips successfully:

1. **AMS-based sensors chip**. In our first design, we designed and released AMS sensors for temperature, voltage and timing. We designed in TSMC 180 and GF14, and we taped-out using TSMC 180nm.
2. **All Digital sensors + MCU chip.** In our second design, we designed all digital sensors for temperature, voltage and timing together with a Microcontroller (MCU) unit for signal processors. We performed all simulations for GF14 and tape-out for TSMC 65nm.

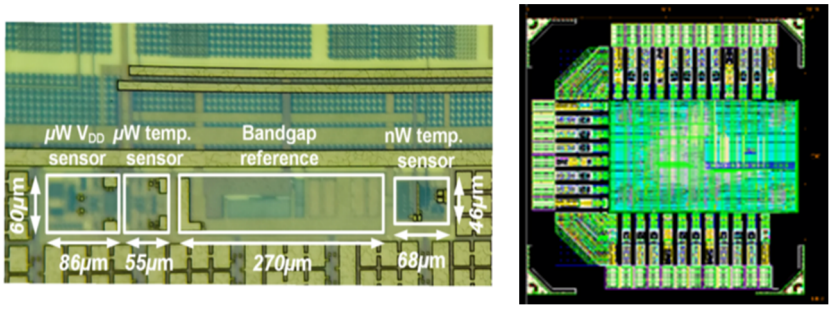


Figure 1: Digital Sensors and MCU Chip

2. Detailed Description of Technical Achievements

A. AMS-based sensor chip

Design, simulation and layout of the bandgap reference current source

Our first design point is a bandgap reference current source that gives stable output despite temperature and voltage variations. The design of the circuit is given below.

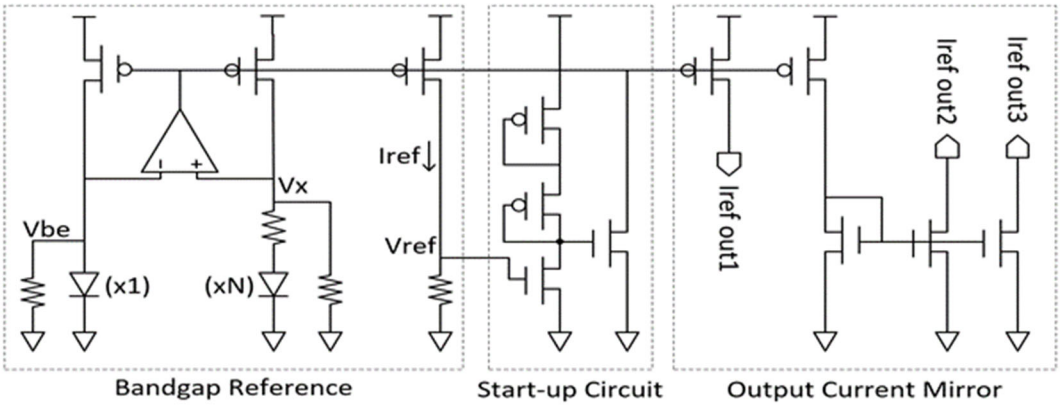


Figure 2: Bandgap Reference Current Source Circuit Implementation

The forward voltage drop of a diode *Vf1* is complementary to the absolute temperature (CTAT), due to the strong temperature dependence of the saturation current Is:

$Vf1 = kT/q*ln(I/Is)$

Biased with the same current and with an area ratio of *N,* the voltage difference between two diodes *(Vf1-Vf2)* is proportional to the absolute temperature (PTAT):

$Vf1-Vf2 = kT/ q*ln(N)$

With identical PMOS transistors, we can balance the CTAT and PTAT coefficients to make the current I_{REF} insensitive to temperature and supply voltage, by choosing the proper values of *R2* and *R3*:

$I_{REF}= Vf1/R2 + (Vf1-Vf2)/R3$

After layout, the area of the proposed bandgap current source is 70 um x 280 um and the current consumption is 6uA.

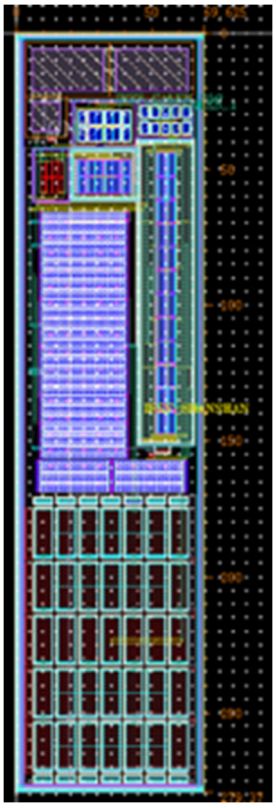


Figure 3: Bandgap Reference Current Source Chip Design

Design, simulation and layout of temperature AMS sensor

Using the bandgap reference current source, we then designed the temperature sensor. The schematic is given in the following figure.

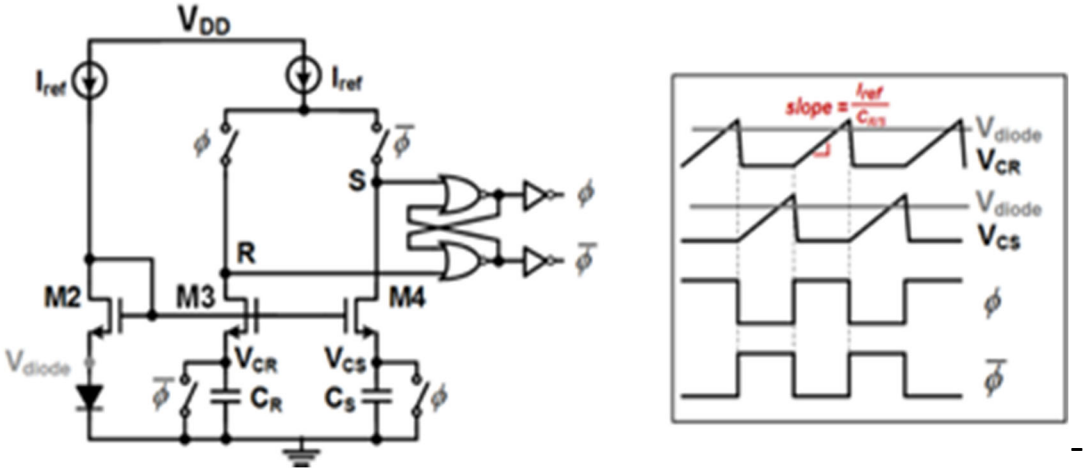


Figure 4: Temperature Sensor Circuit Implementation and Waveforms

In the temperature sensor, one branch of IREF flows through the diode to generate a CTAT voltage V_{diode} equal to $kT/q*ln(I_{REF}/I_S)$, which is CTAT. Meanwhile a second matched current

charges the capacitor $C_R(C_S)$ with a ramp slope of $I_{REF}/C_{R(S)}$. *M2* and *M3 (M4)* act as a common-gate amplifier, to compare V_{diode} with the voltage on the capacitor V_{CR} (V_{CS}). Once the ramp voltage V_{CR} (V_{CS}) exceeds V_{diode}, M3 or M4 triggers the SR latch and toggles its outputs. The oscillation period is:

$$T = 2*V_{diode}*C_{R(S)} / I_{REF}$$

Since I_{REF} is voltage- and temperature-independent, the period T is complementary to the absolute temperature (CTAT), following V_{diode}. We then translated this design into SPICE simulations and simulated the period of the output signal as a function of the operating temperature and the process corner. The plot below summarizes the results. The period of oscillation decreases linearly as a function of the temperature, over the practical expected range of -20 C to +120 C. The outputs also show that different corners lead to different linear trends. Thus, it will likely be necessary to calibrate each chip at one or more known temperatures.

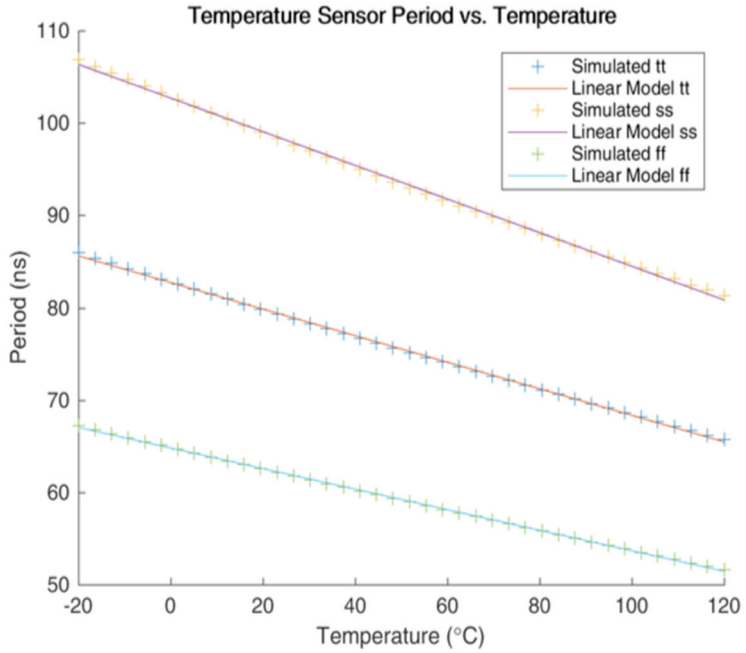


Figure 5: Temperature Sensor Period versus Temperature

Using Cadence Virtuoso, we also created a layout of our temperature sensor to assess the total area. The layout is given in the next figure. Our layout gives an area of 70 um x 60 um, and post-layout simulations yield a current consumption of 8 uA.

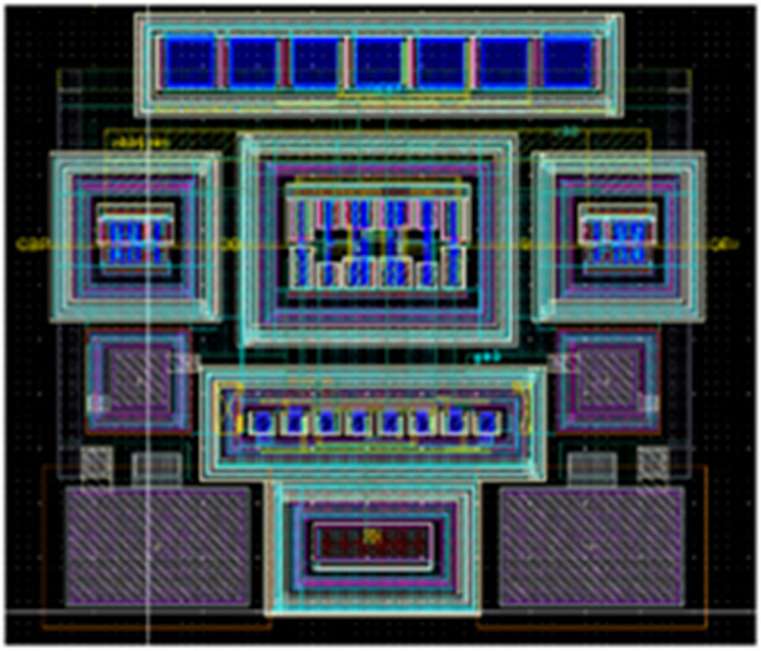


Figure 6: Temperature Sensor Chip Design

Design, simulation and layout of AMS voltage sensor

The design of the voltage sensor is given below. In the supply voltage V_{DD} sensor, we put five diode-connected PMOS transistors in series between V_{DD} and ground, to form a voltage divider. Thus the source voltage of M2 is $2/5*V_{DD}$. Similar to the temperature sensor, the period of this oscillator can be expressed as:

$T = 2*2/5*V_{DD}*C_{R(S)}/I_{REF}$,

which is proportional to the supply voltage

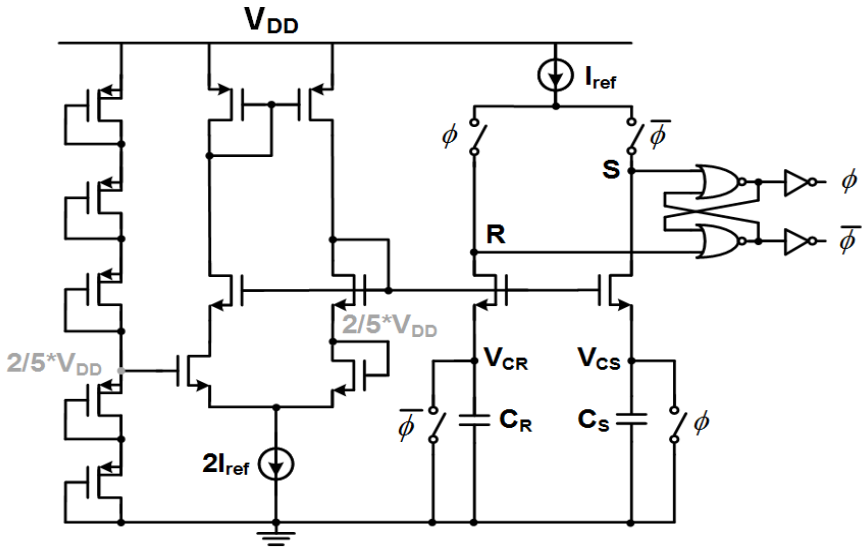


Figure 7: Voltage Sensor Circuit Implementation

We then translated this design into SPICE simulations and simulated the circuit as a function of the voltage (VDD) and the process corner. The plot above summarizes the results. The period of oscillation increases linearly as a function of the operating voltage, over the expected range of operation from 1.5 V to 2.0 V for 180 nm technology. The output also shows that different corners lead to different linear trends. Once again, this may require at least one point of calibration during manufacturing.

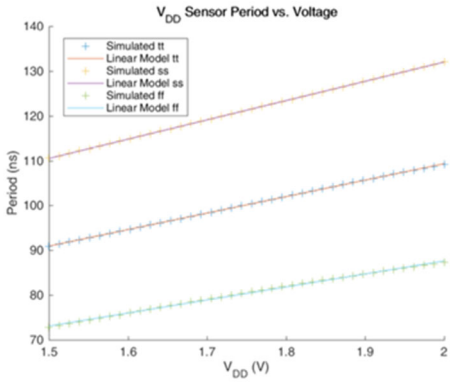


Figure 8: Voltage Sensor Period versus Voltage

Using Cadence Virtuoso, we also created a layout of our voltage sensor. The layout is given in the next figure. Post-layout, the voltage sensor has an area of 70 um x 100 um and current consumption of 9.75 uA.

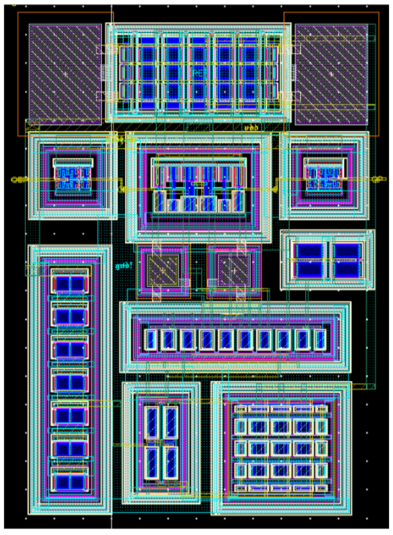


Figure 9: Voltage Sensor Layout

<u>Design, simulation and layout for Timing (P) critical path monitoring (CPM) circuit</u>

We devised a flexible and area-efficient critical path monitor (CPM) with a wide dynamic range. The CPM is a collection of NAND4 and NOR4 gates that are connected together in a programmable way to mimic a critical path. The user can program the wiring between the NAND/NOR gates to control the timing of the CPM monitor to mimic their actual critical path. In TSMC 180nm the shortest delay path is 762.8 ps, while the longest delay is 1.504 ns.

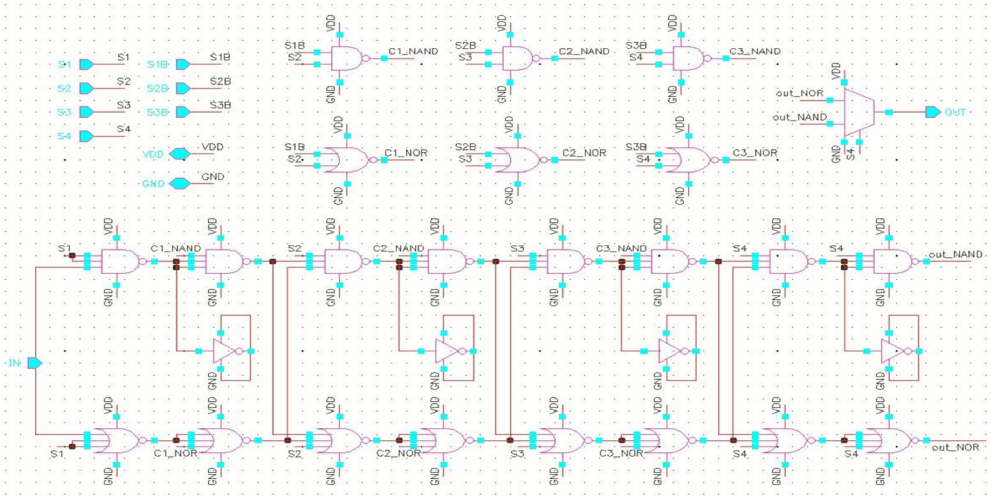
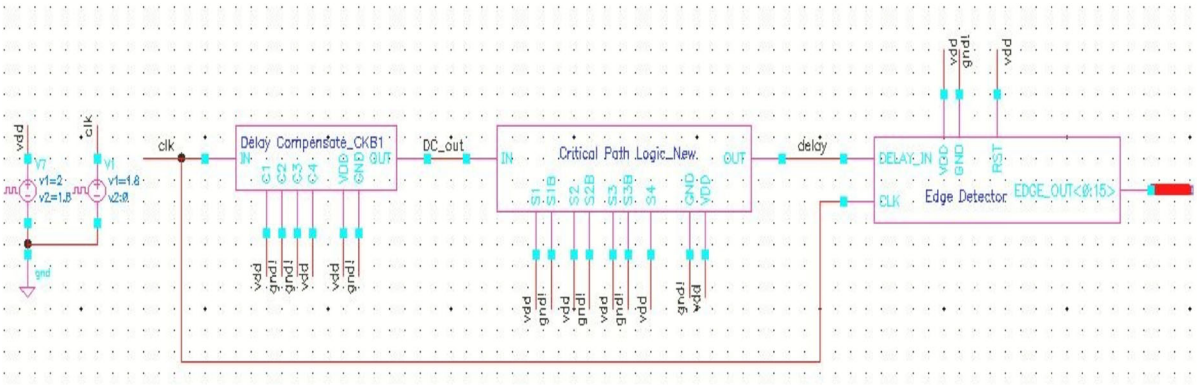


Figure 10: Timing Critical Path Monitoring Circuit Implementation

We created a testbench for our CPM monitor. It includes a programmable critical path and an edge detector that translates the delay from the CPM into a digital value. The next two schematics include the testbench and results from our simulation showing correct operation.



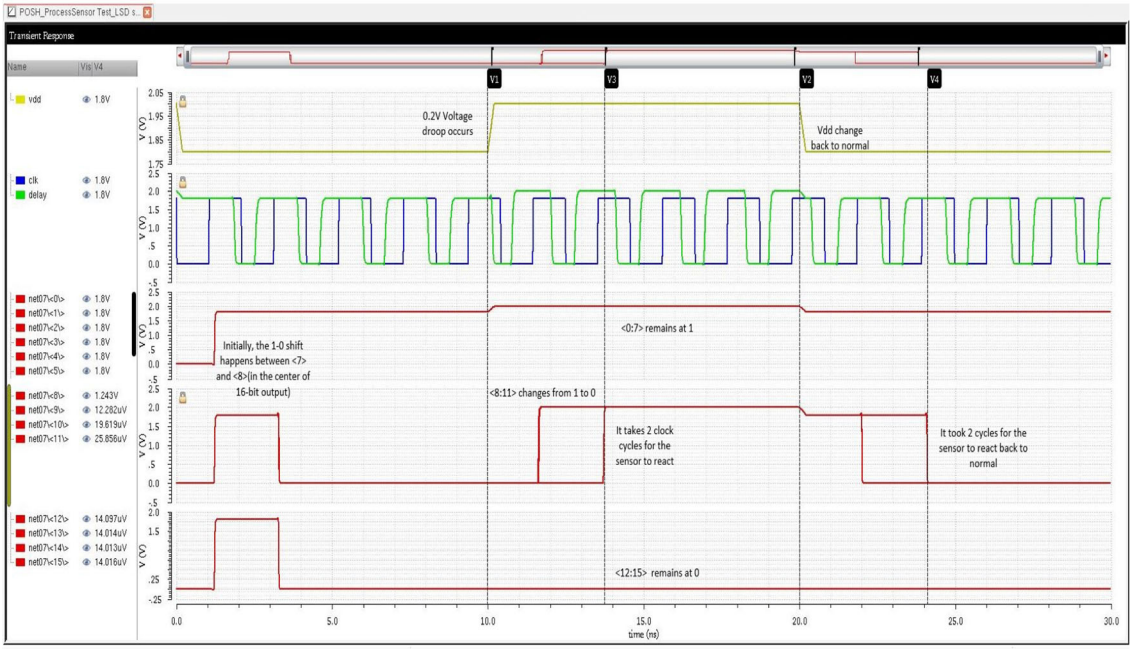


Figure 11: Testbench with Simulation

We have also implemented the layout in TSMC 180nm. The circuit has a competitive area of 130 um x 30 um. The circuit is 100% composed of standard logic cells, and its area and energy will improve in more modern technology nodes.

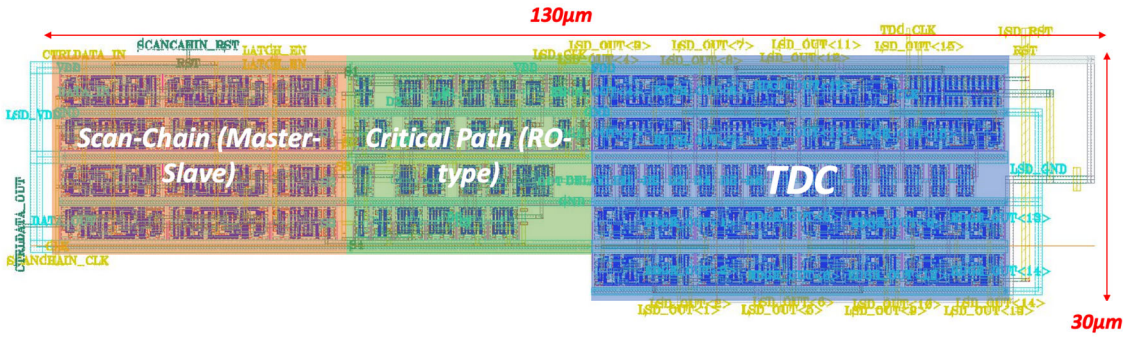


Figure 12: TSMC 180nm Layout

Tape-out and Test Measurements

We taped out a chip in TSMC 180 nm which included the T and V sensors that we designed, implemented and simulated in the first quarter. In preparation for post-silicon characterization, we designed and fabricated the following printed circuit board.

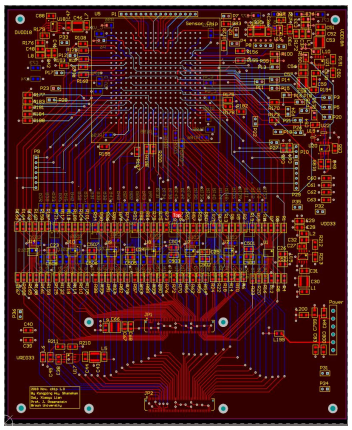


Figure 13: Printed Circuit Board Layout

The test chip was wirebonded in a ceramic pin grid array. A die photograph is shown below. It is annotated with outlines of the uW VDD sensor, the uW temperature sensor, the bandgap reference, and the integrated nW hybrid voltage+temperature sensor.

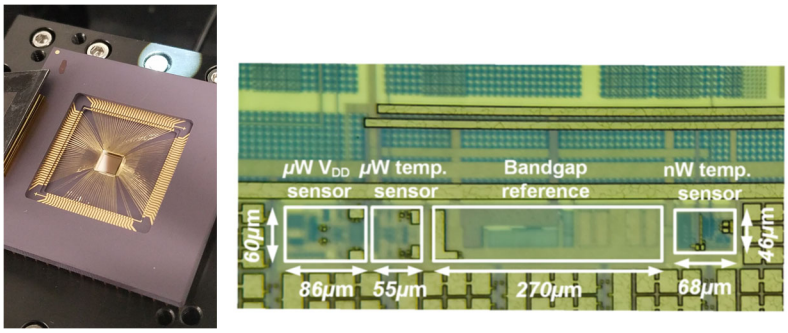


Figure 14: Packaged Test Chip with Sensors Enlarged

The components were soldered to the PCB, including a test socket for characterizing multiple chips.

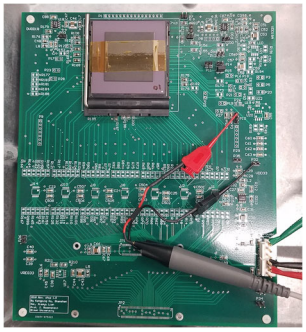


Figure 15: Final Test Board

We then conducted post-silicon characterization for the thermal sensor. Below we show the period of the sensor output vs the temperature, measured using a climate control chamber. We also plot the nonlinearity error (i.e., difference between actual set temperature and sensor

reported temperature) versus actual temperature. Overall, the temperature sensor is working as designed.

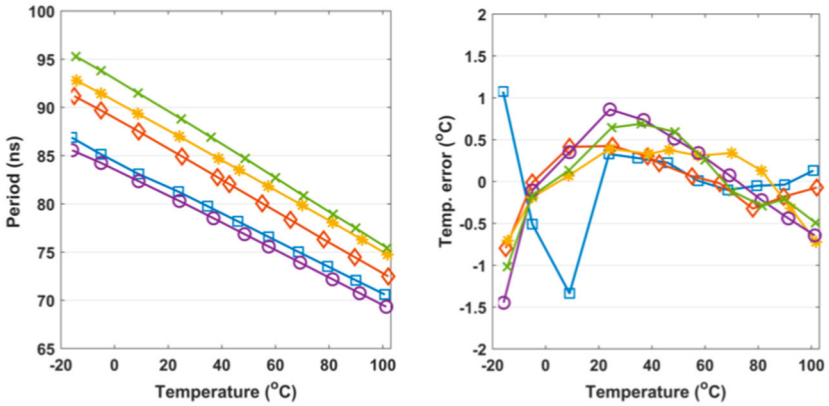


Figure 16: Measured Thermal Sensor Output and Nonlinearity Error

We then conducted post-silicon characterization for the voltage sensor. Below we show the period of the sensor output as the supply voltage was varied. We also plot the nonlinearity error (i.e., difference between actual set voltage and sensor reported voltage) versus actual voltage. The supply voltage sensor is working as designed.

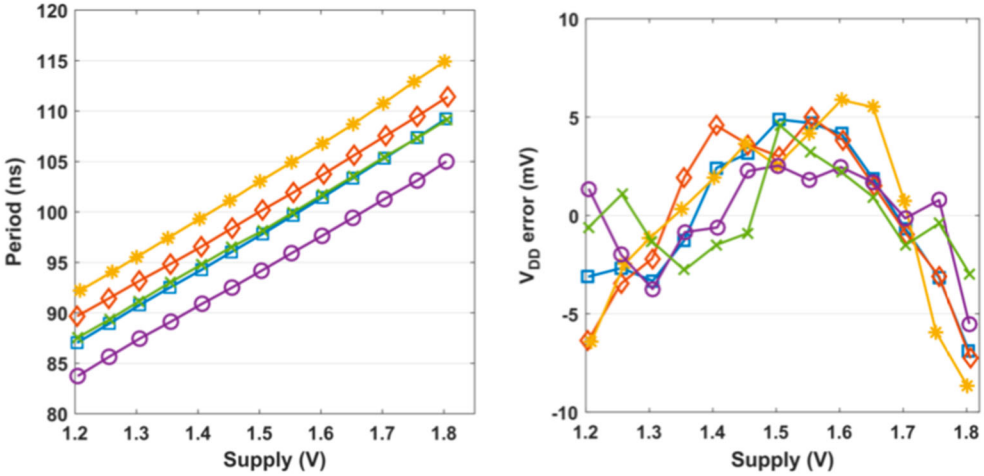


Figure 17: Measured Voltage Sensor Output and Nonlinearity Error

The figure below shows a plot that compares our thermal sensors' performance against other published temperature sensors in the literature. The circuits achieve excellent figures of merit, while significantly improving both area and power.

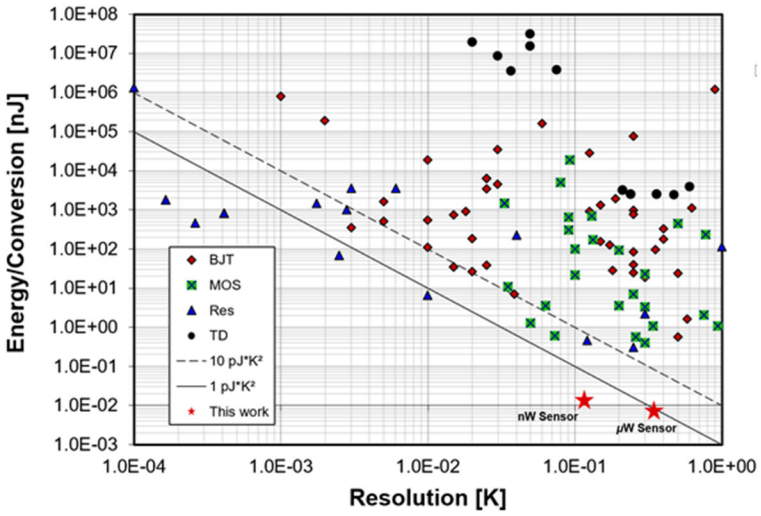


Figure 18: Comparison of Temperature Sensor Results to Published Data

B. All digital sensor chip

All digital thermal and voltage sensors

Our AMS porting to GF12 shows non-ideal scaling for our analog component. GF12 is mostly optimized for digital designs. Thus, we designed an all-digital V & T sensors that we simulated in GF14 and TSMC 180 nm, and we taped-out in GF14. The main idea is that digital delays are sensitive to P & V & T. Instead of calibrating some parameters out, we can infer T&V measurements from critical path data.

In this case we use our CPM timing sensors (given below) to measure the delay of the critical path replica, and use the results to infer temperature and voltage.

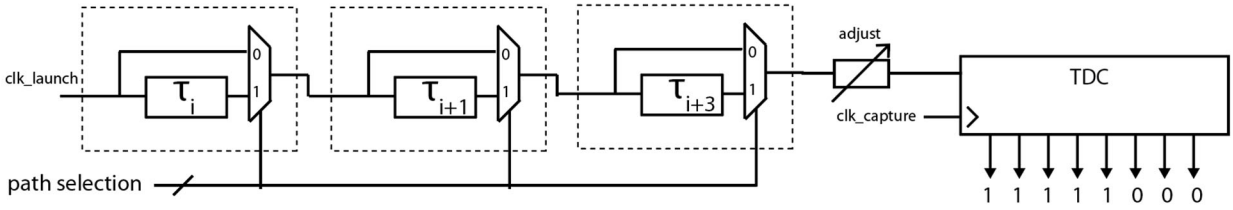


Figure 19: Timing Sensor Implementation

The main challenge here is that the CPM has weak sensitivity to temperature, thus we cannot achieve good resolution (<1C) with one CPM. Thus, we used multiple CPM sensors so that we can have several delay measurements that are functions of P, V, and T with enough independence. For instance, the figure below shows an inverter delay as a function of temperature for multiple inverter types in the standard cell library for GF12. The plot shows that if we deploy enough diversity in the building blocks (e.g., inverters) of our CPM design, we can improve the sensitivity of the CPM monitor to temperature variations.

Using the delay-temperature characterization results, we devised a multivariate regression using delays from 4 inverter types to infer temperature. The figure below gives the error between the estimated temperature vs the actual temperature for our model. The results show that a quadratic regression model can have an error of about 0.44 C.

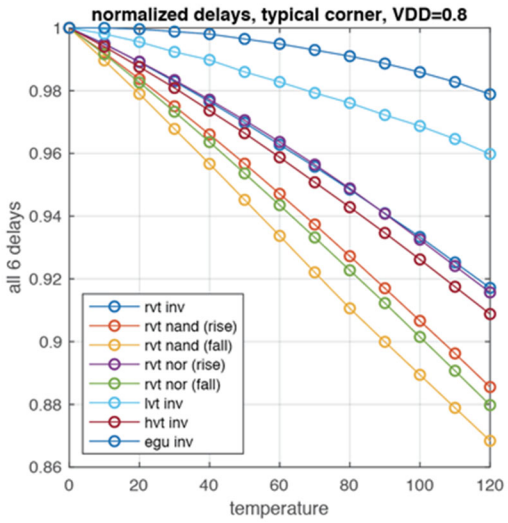


Figure 20: Error between the Estimated Temperature versus the Actual Temperature

Thus, we developed an all new digital design for T and V sensors. A sensor tile includes 9 different types of ring oscillators: slvt, lvt, rvt, NAND4 and inverters, and extended gate devices with different vt (eg, egu, egv). The tile also includes a coarse-fine readout structure, which is a 16-bit counter and fine readout with : 48-bit TDC. We can use correlations between several devices to implement a form of high-order temperature compensation while estimating Vdd, or vice versa. For example, the next figure shows actual iso-delay characteristics for different ring oscillators (ROs) inside the tile. Note that using a single RO is not sufficient as there are many (V, T) pairs that yield the same delay. However, by including a diversity of ROs designed with different devices, we can identify the operating (T, V), which is the intersection point of the iso-delay characteristics With this approach V & T can be treated independently, and we can use multivariate regression to train models which simultaneously estimate V & T. We can either fit a linear regression or a constrained nonlinear function. Below illustrates one example with a system of equations $T = 1 + \sum(\alpha_1\tau + \alpha_2 \log\tau)$, and $V = 1 + \sum(\beta_1\tau + \beta_2 \log\tau)$ which can be trained to find α and β which minimize mean-squared error. For example, the next plot shows the training error and testing error using our simulation data. The results show that we can estimate the temperature within 0.2 C and the voltage within 400 mV.

ASIC flow for uController

To process the data from the sensors, we included a RISCV microcontroller.

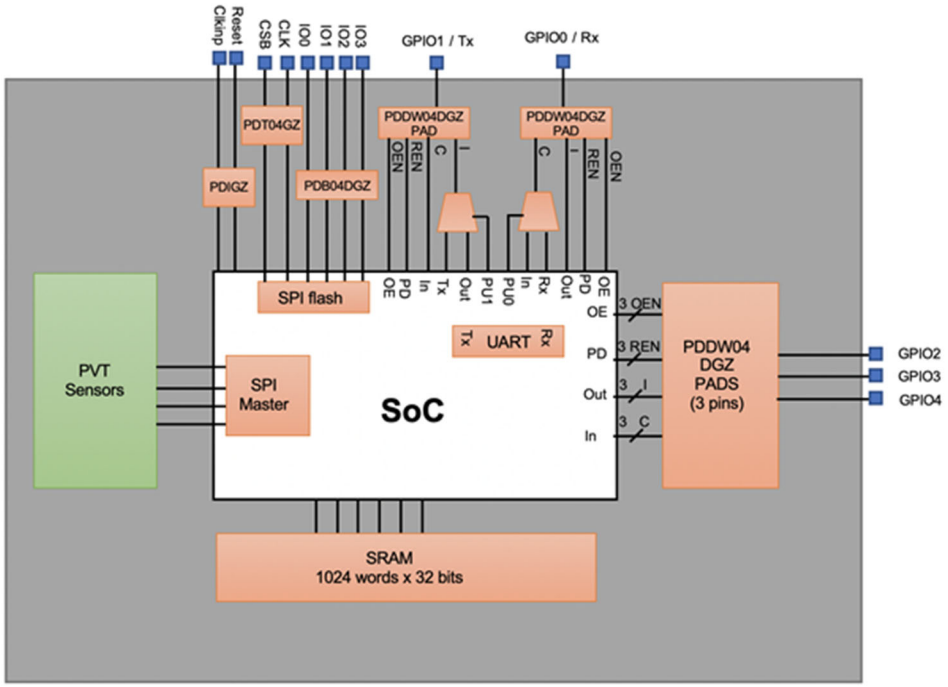


Figure 21: ASIC Flow

The RTL of the final design includes:

- Integration of the SPI master to interface with the sensors
- Integration of the SPI memory controller (SPI flash) to interface with the flash memory
- Integration of the GPIO peripherals
- Integration of the I/O pads
- Design of the shared GPIO/UART pins

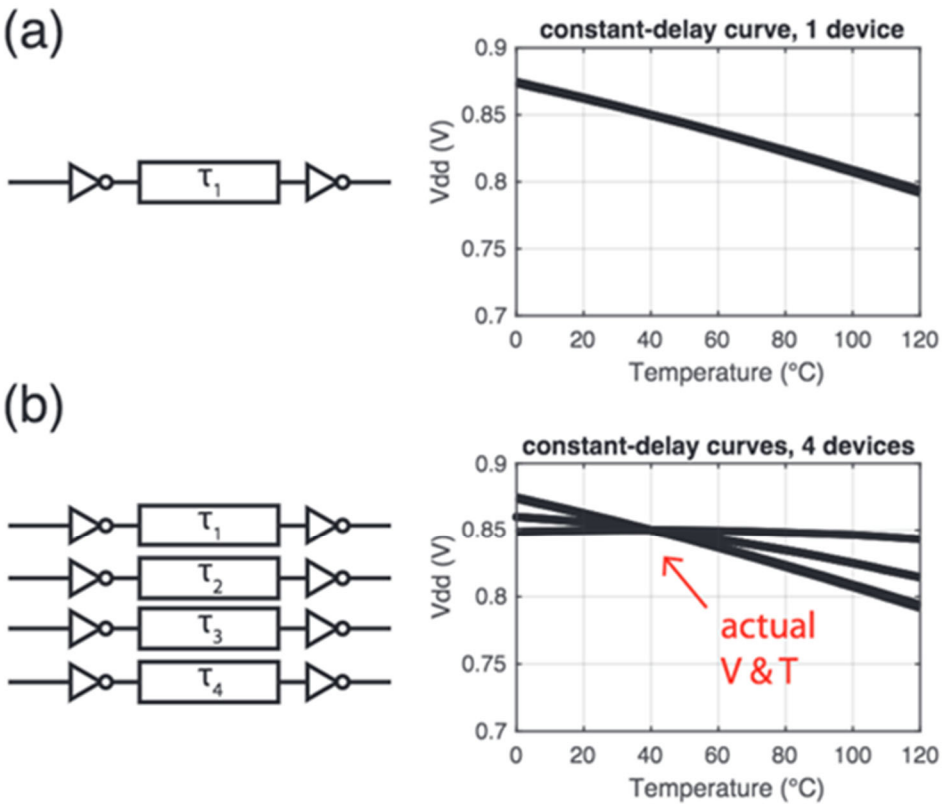


Figure 22: Delay Curves for One Device and Four Devices

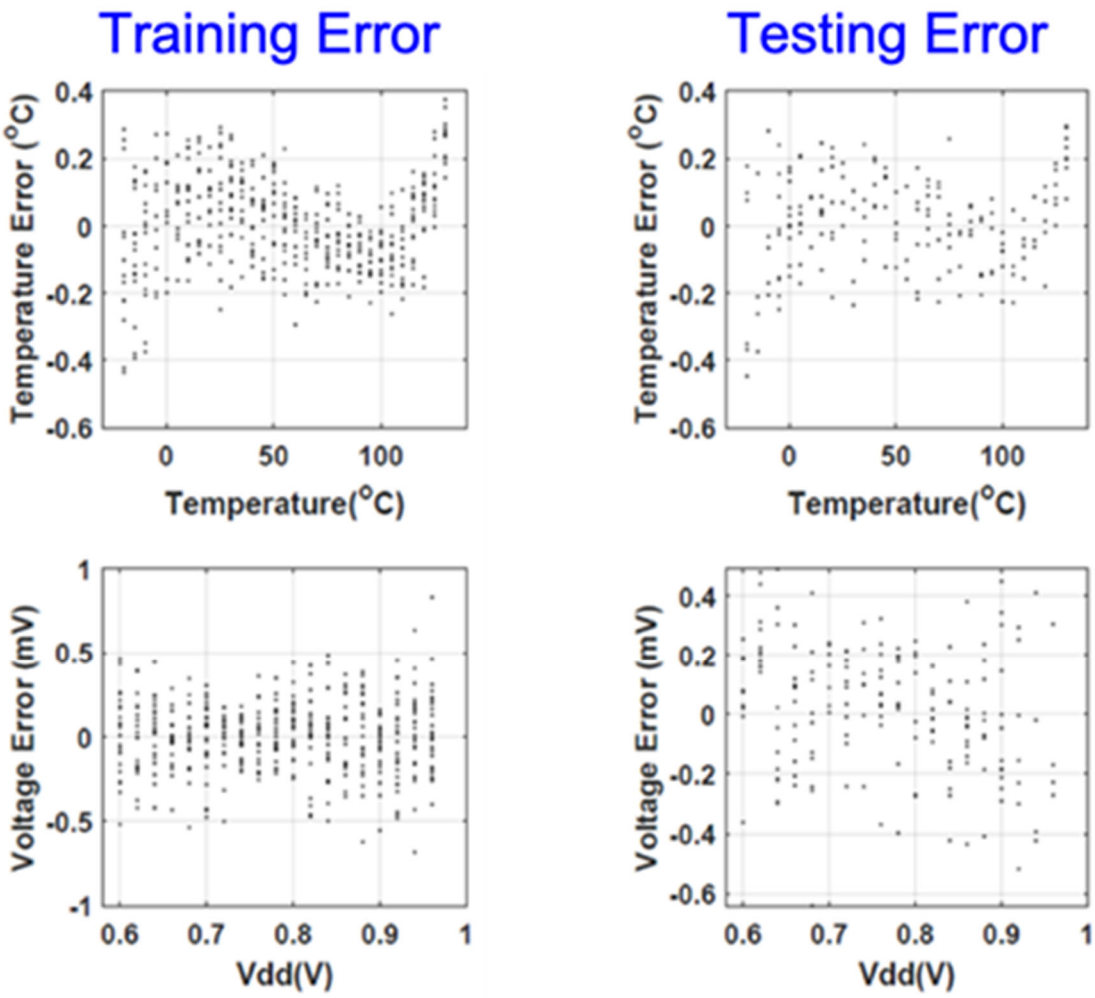
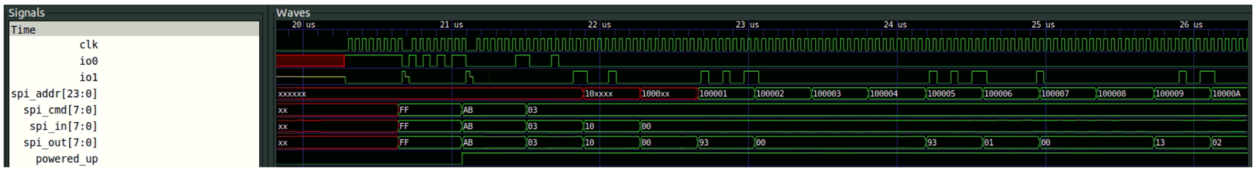


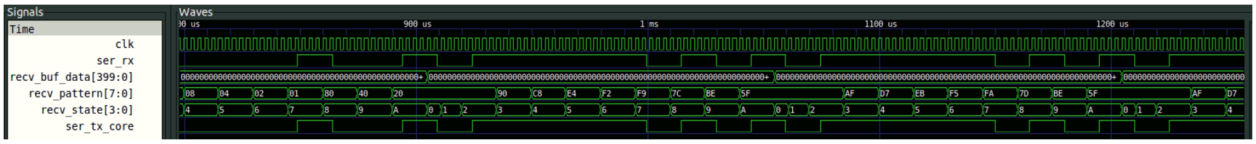
Figure 23: Temperature and Voltage Sensor Training Error and Testing Error

- **Pre-synthesis simulation**

SPI flash memory interface:



UART interface :



GPIO interface :

SPI Master + PVT Sensors :

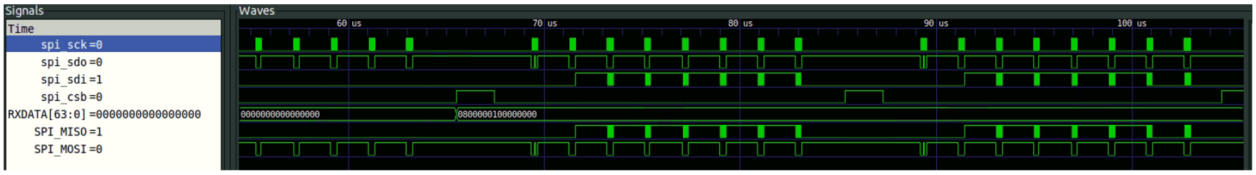


Figure 24: Timing Simulations

- **Post-synthesis simulation of the uController:**

After synthesizing the uController with all the previously mentioned peripherals we performed a post-synthesis simulation by connecting the uController to a verilog model that mimics a flash memory:

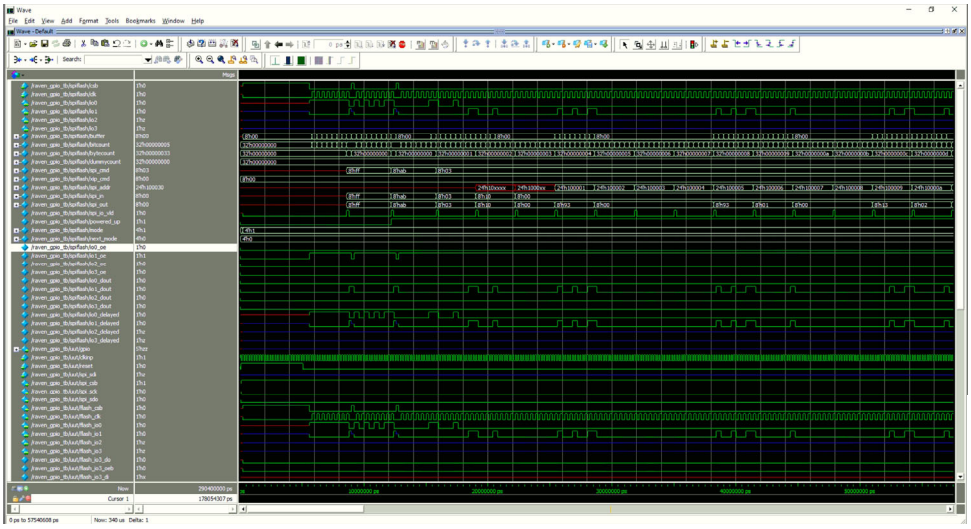


Figure 25: Post-Synthesis Simulation

- **SPI slave connection and communication multiplexing:**

There, in total, four PVT sensors in each corner of the chip. All sensors are daisy-chained to each other as one complete SPI slave. To make sure the PVT sensor can work independently without the microcontroller, multiplexing logic is added to the SPI connection. The diagram is attached below. When reset is low, the SPI connection will be initialized to use the pad by default.

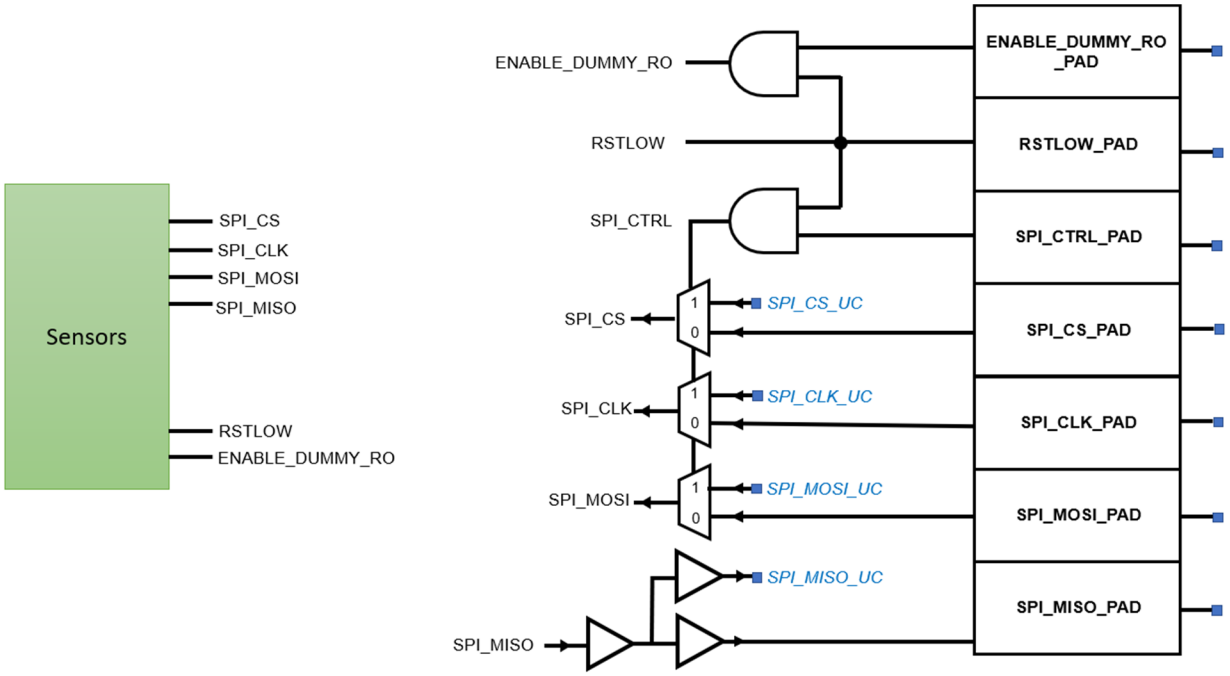


Figure 26: Schematic of SPI and Communication Multiplexing

The post-PNR simulation result is attached below. As shown in the screenshot the sensor passed the verification overall.

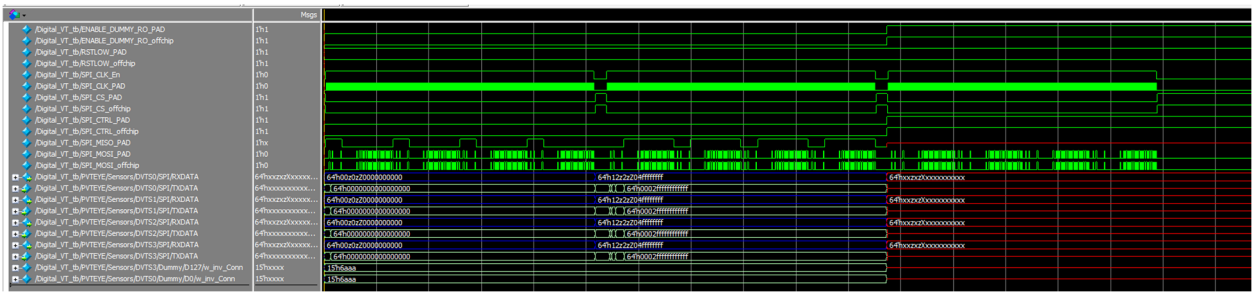


Figure 27: Post-PNR Simulation

Digital flow & Chip Tape-out:

The design of this chip was implemented through the ASIC flow with industry tools. The synthesis was done with Synopsys Design Compiler and Cadence Gunes. The Place-and-Routing was done by Cadence Innovus. Dummy fill and seal ring were added using Calibre. The final layout of the chip is DRC violation free. Screenshots of our floorplan and full-chip are attached below. We put a hard fence for every ring-oscillators to make sure they are placed in a small and packed region to minimize the phase noise caused by wire load.

The dimension of the chip is 1mm x 1mm. The core area is 665um x 390um. Totally 32 GPIOs are included, with 20 signal pads and 12 power pads. The chip is expected to be wire-bonded.

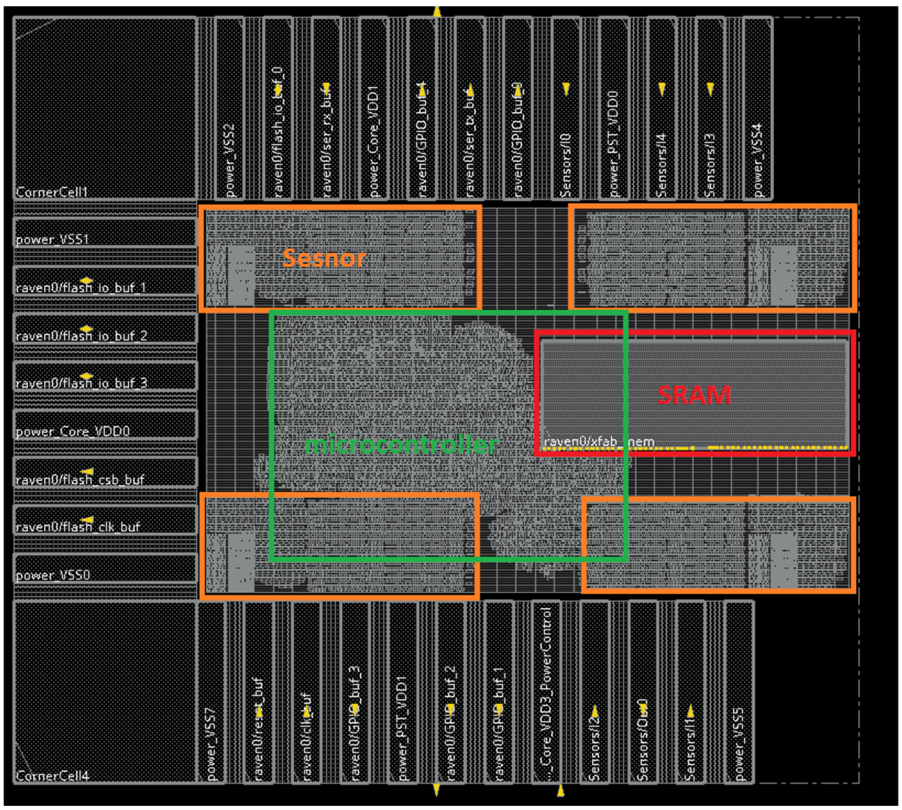


Figure 28: Chip Floor Plan

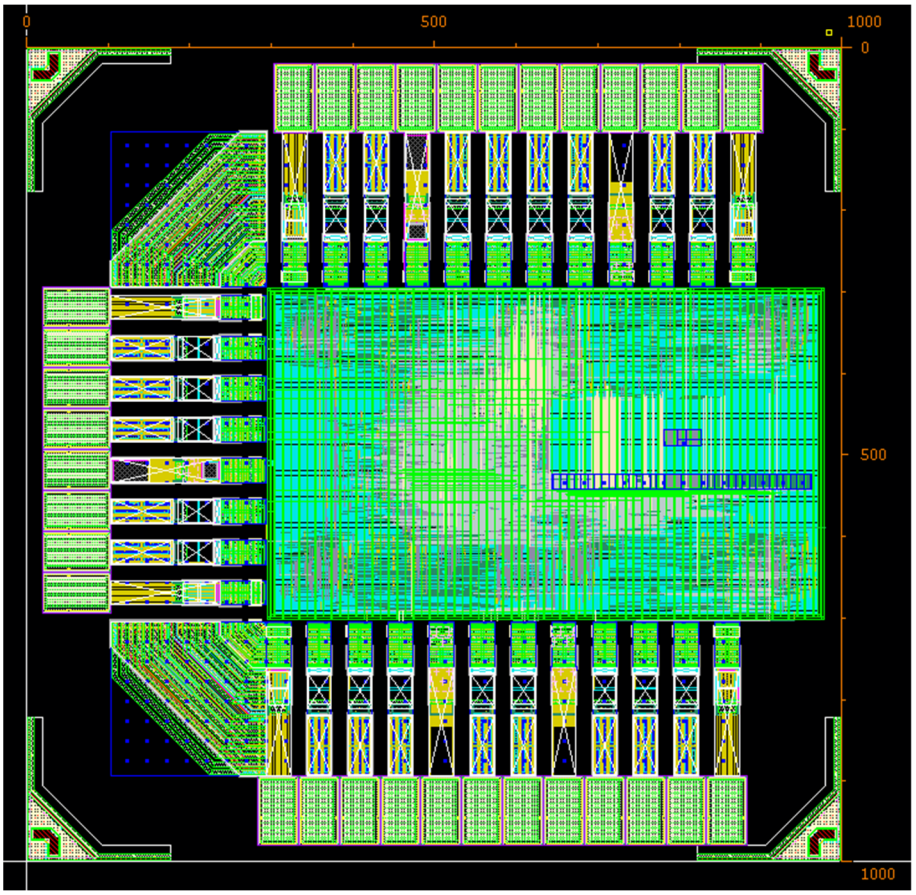


Figure 29: Full Chip Layout

2 RESOURCE/STAFFING/CONTRACTING STATUS

- Sherief Reda (PI)
- Jacob Rosenstein (co-PI)
- Sofiane Chetoui (PhD student)
- Xiaoyu (Steven) Lian (PhD student)

3 PAPERS

- S. Dai, C. Tulloss, X. Lian, K. Hu, J. Rosenstein and S. Reda, *Temperature and Supply Voltage Monitoring with Current-mode Relaxation Oscillators*, in IEEE VLSI-Soc 2020.
- X. Lian, S. Reda and J. Rosenstein, Simultaneous Estimation of Temperature and Voltage from Digital Delay Diversity, *IEEE VLSI-SoC 2020.*
- S. Chetoui and S. Reda, Coordinated Self-tuning Thermal Management Controller for Mobile Devices, accepted in IEEE Design & Test 2020.

LIST OF SYMBOLS, ABBREVIATIONS, AND ACRONYMS

ACRONYM	DESCRIPTION
AFRL	Air Force Research Lab
AMS	Analog Mixed Signal
ASIC	Application Specific Integrated Circuit
CPM	Critical Path Monitor
CTAT	Complementary to the Absolute Temperature
DARPA	Defense Advanced Research Projects Agency
DRC	Design Rule Check
GPIO	General Purpose Input/Ouput
HW	Hardware
I/O	Input/Output
IREF	Reference Current
MCU	Microcontroller
PCB	Printed Circuit Board
PMOS	P-channel Metal Oxide Semiconductor
PNR	Place and Route
PTAT	Proportional to the Absolute Temperature
RISCV	Open Standard Instruction Set Architecture
ROs	Oscillators
RTL	Register-Transfer Level
SoC	System-on-a-Chip
SPI	Serial Peripheral Interface
SW	Software
TDC	Time-to-Digital Converter
TSMC	Taiwan Semiconductor Manufacturing Company
U.S.	United States
UART	Universal Asynchronous Receiver-Transmitter
VDD	Voltage Drain Drain