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Design of a Battery-Powered Gate Driver for Medium-Voltage Silicon Carbide Switch Modules in Pulsed Applications

by Damian Urciuoli and Miguel Hinojosa

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14. ABSTRACT

A compact battery-powered gate driver was designed to enable a wide range of switching modes for a series-connected, medium-voltage, silicon carbide metal–oxide–semiconductor field-effect transistor or insulated-gate bipolar transistor in pulsed applications. The gate driver's battery power source eliminates the need to isolate power from a supply referenced to a fixed potential. To prolong the gate driver's shelf life, the circuit is designed to be disabled in a low-power state by default. The gate driver is designed to have a relatively thin profile to provide voltage standoff between neighboring series-connected switches. Features include a wide range of configurable gate currents, an asymmetric turn-on/turn-off gate-resistance network, voltage clamps for gate protection, and a Miller clamp to reduce transient-induced gate-voltage excursion while in the off state.

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Energy Sciences, battery-powered gate driver, medium voltage, high voltage, silicon carbide

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1. Introduction

Silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs), insulated-gate bipolar transistors (IGBTs), and diodes with blocking voltages in excess of 10 kV have been fabricated and demonstrated.[1–6] Several challenges are presented when implementing and operating switch configurations with series-connected devices having blocking voltages greater than 10 kV. One such challenge is designing a versatile gate driver to control switches at the second-and-higher levels of series-connected configurations including multilevel configurations in pulsed applications. Generally, variants of one of three different gate-driver architectures are used to provide biasing of the gate of an upper-level MOSFET or IGBT in switch-mode applications. These architectures may be referred to as charge pump, pulse transformer isolated, and isolated DC-DC converter. Each architecture has advantages and drawbacks.

Charge-pump gate drivers, also referred to as boot-strap gate drivers, are commonly used in applications with bus voltages up to several hundreds of volts. An advantage of this type of gate driver is that it does not require an isolated DC-DC converter. However, it requires a charge-pump diode having a blocking voltage exceeding the bus voltage of the application and only supports limited switching conditions and switch configurations. Pulse-transformer-isolated gate drivers can be used to galvanically isolate the driving signal and power source from an upper-level switch. This type of gate driver also does not require an isolated DC-DC converter. However, it requires a pulse transformer with an isolation-voltage rating exceeding the bus voltage of the application.

The requirement to reset the flux in the pulse-transformer core, and limitations imposed by parasitic leakage inductance and inter-winding (input to output) capacitance, can preclude the use of pulse-transformer-isolated gate drivers in many applications. Gate drivers using an isolated DC-DC converter to bias the gate of an upper-level switch require the DC-DC converter to have an isolation-voltage rating exceeding the bus voltage of the application. However, because the applied bias of the gate driver is independent of the internal coupling and switching cycle of the isolated converter and independent of the switching cycle(s) of the medium-voltage switch configuration, the gate driver can support a wide range of duty cycles and switching frequencies. Additionally, the isolated converter may easily be configured to provide two output voltages with a common reference to be used for positive and negative gate biases to significantly improve immunity to switching-induced gate transients.

A battery-powered gate driver was designed to enable a wide range of switching modes for a network of two or more series-connected medium-voltage SiC MOSFETs or IGBTs in pulsed applications. A rechargeable battery was selected for the gate-driver power source because the application only requires the switch network to operate for intermittent and short time intervals. The battery allows the gate driver to be referenced to the potential of the source or emitter of its respective switch in the series-connected switch network, thereby eliminating the need for voltage isolation while coupling to a power source referenced to a fixed potential. To provide sufficient standoff to prevent voltage breakdown between gate drivers connected to neighboring series-connected switches, the gate driver was designed to use a pouch battery and have a relatively thin profile to be oriented in a plane perpendicular to the plane of a switch module. Apart from the added requirement to monitor and/or manage the battery state of charge, the gate driver was designed to provide the aforementioned operational benefits of a gate driver with an isolated DC power source.

2. Circuit Design

The gate-driver circuit schematic is shown in Appendix A. Some resistor values are listed as "TBD" (to be determined) on the schematic and will be determined based on individual SiC switch parameters and during empirical evaluations of the gate-driver circuit. A single-cell, rechargeable, lithium-polymer battery (S1) with a nominal voltage of 3.7 V and a capacity of 400 mAh was selected to power the gate driver. The pouch cell is 4.9 cm long, 2.3 cm wide, and 0.4 cm thick and has a mass of 9.5 g. The 400-mAh capacity is sufficient to operate the gate driver intermittently at output power levels in the range of 1 to 2 W. The gate-driver circuit is designed to have a fixed connection to the battery to allow the unit to be encapsulated with dielectric material to prevent voltage breakdown through the gate driver in medium- and high-voltage systems. To prolong the shelf life of the battery-powered unit, the gate-driver circuit was designed to be disabled in a low-power state by default. In the disabled state, the battery is electrically disconnected from the majority of the gate-driver circuit by a p-channel MOSFET (M1). An ultra-low-power LED (D8) remains connected to the battery through a current-limiting resistor (R7) to provide a visual indication (through an insulated window in the dielectric encapsulation) of battery voltage about a predetermined threshold. The gate driver is enabled by providing a continuous optical signal to a phototransistor (Q1), which turns on the MOSFET (M1) connecting the battery to the rest of the gate-driver circuit. To facilitate enabling multiple gate drivers in a system, an optical transmitter (D3) is provided on the gate driver to repeat the enable signal as an output. This allows multiple gate drivers to be enabled in a chain from a system controller's single optical signal. Additionally, the enable-signal output of the last gate driver in a chain may be returned to a system controller to verify the enable state of all gate drivers in the chain. The signal for gate control is input to the gate driver through a separate optical receiver (U3).

The positive and negative gate-bias-supply voltages of the driver are designed to be provided by non-isolated DC-DC converters powered by the 3.7-V battery. Gate-to-source/emitter biases of 20 and –5 V were selected for the on- and off-state biases of the SiC switch, respectively. The DC-DC converters were designed using discrete components with switch-mode power-supply-controller integrated circuits (ICs) to allow design flexibility and a relatively thin profile. The –5-V supply is designed with a MAX774 (U2) buck-boost converter control IC, an SSM3J334R p-channel MOSFET (M3), a PMEG4010ETR Schottky diode (D2), and a 22-µH ASPI-6045S-220M-T inductor (L2). The 20-V supply is designed with a MAX1771 boost converter control IC (U1), an SI2318A n-channel MOSFET (M2), a PMEG4010ETR Schottky diode (D1), and a 47-µH CLF10060NIT-470M inductor (L1). Both converters share over 40 µF (C1-5, C12) of total input capacitance. The output capacitances of the buck-boost and boost converters are 80 µF (C14-19, C22-23) and 40 µF (C8-11), respectively. Input and output ripple voltages of both converters will be evaluated, and capacitances will be increased if needed.

The gate driver is designed with optional features to protect the SiC switch and improve its operation. A product line of driver ICs having 9-A (IXDI609YI), 14-A (IXDI614YI), and 30-A (IXDI630YI) current ratings was selected. Each driver is offered in a TO-263-5 package with the same pin assignments, allowing the design to accommodate the driver best suited to the SiC switch and application. The output of the driver IC is inverted with respect to its input logic. This function was selected to cancel out the logic inversion produced by the open-collector output of the HFBR-2524Z optical receiver (U3). A series-connected diode (D4) and resistor (R11) can be connected in parallel with the gate resistor (R10) at the output of the driver to provide a reduced gate resistance during switch turn-off transitions. To protect the gate of the SiC switch, the output of the driver can be clamped to the 20- and –5-V bias-supply rails by Schottky diodes D5 and D6, respectively. This approach was used instead of conventional gate-to-source/emitter bidirectional Zener-diode clamping to more effectively reduce gate-to-source/emitter voltage excursions above 20 V and below –5 V.[7] The D5 and D6 diodes also allow clamped energy to be distributed back to the bias-supply rails of the gate driver instead of being dissipated by Zener diodes. Finally, to reduce gate-voltage bounce commonly observed during turn on of the opposite (upper or lower) switch in a half-bridge switch configuration, a Miller clamp was included in the gate-driver design.[7,8] The drain of an SI2318A n-channel MOSFET (M4) is connected to the gate-driver output to provide a low-impedance path to the –5-V bias supply during the off state of the SiC switch. To allow MOSFET M4 to turn on after the SiC switch turns off, and to turn off before the SiC switch turns on, a UCC27517 auxiliary gate driver IC (U5) and an asymmetric gate-resistance network (R12, R13, D7) is provided. The asymmetric gate-resistance network of M4 allows the auxiliary gate driver (U5) to operate from the same input signal provided to the gate-driver IC (U4) for the SiC switch.

3. Circuit Layout

A printed circuit board (PCB) layout for the gate driver was designed. The design consists of two layers of 1-oz/ft^2 (35-µm-thick) copper with overall PCB dimensions of 7.4 cm (2.9 inches) by 3.0 cm (1.2 inches). The top and bottom copper layers of the gate-driver layout are shown in Appendix B. The image of the bottom copper layer is mirrored about a vertical axis for alignment with the top-layer image. To limit the overall thickness of the gate driver to 1.7 cm, most of the circuit components are placed on the top layer, allowing the battery to lay flat on and connect to the bottom layer. A large copper plane on the bottom layer serves as the PCB ground plane, which corresponds to the return node labeled "RTN" in the schematic. The optical input and output devices are placed on the top layer along the short side (right side of image) of the PCB to reduce the space occupied by fiber-optic lines during operation. The midsection of the top layer is occupied by DC-DC-converter components and associated input and output capacitors. The left side of the top layer is populated with the gate-driver and gate-protection components. A 3-pin through-hole footprint (J1) is used to accommodate a modified SubMiniature version A (SMA) coaxial connector to connect to the gate and source or emitter of the SiC switch.

4. Conclusion

The design of a battery-powered gate driver for a medium-voltage SiC MOSFET or IGBT switch in a series-connected switch network for pulsed applications was presented. A battery was selected for the gate-driver's power source to provide operation during intermittent and short time intervals. Using a battery allows the gate-driver's supply to be referenced to the potential of the source or emitter of its respective switch without the need to isolate power from a supply referenced to a fixed potential. To prolong the gate-driver's shelf life, the circuit is designed to be disabled in a low-power state by default. The gate-driver design is 1.7 cm thick and can be mounted perpendicular to a switch module to increase voltage standoff between neighboring series-connected switches. The gate driver has a wide range of configurable gate currents and is designed with an optional asymmetric turn-on/turn-off gate-resistance network, optional voltage clamps for gate protection, and an optional Miller clamp to reduce transient-induced gate-voltage excursion while in the off state. The gate driver will be fabricated, and undefined passive-component values will be determined based on circuit evaluation and SiC switch parameters.

5. References

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Appendix A. Electrical Schematics of the Battery-Powered Gate-Driver Design

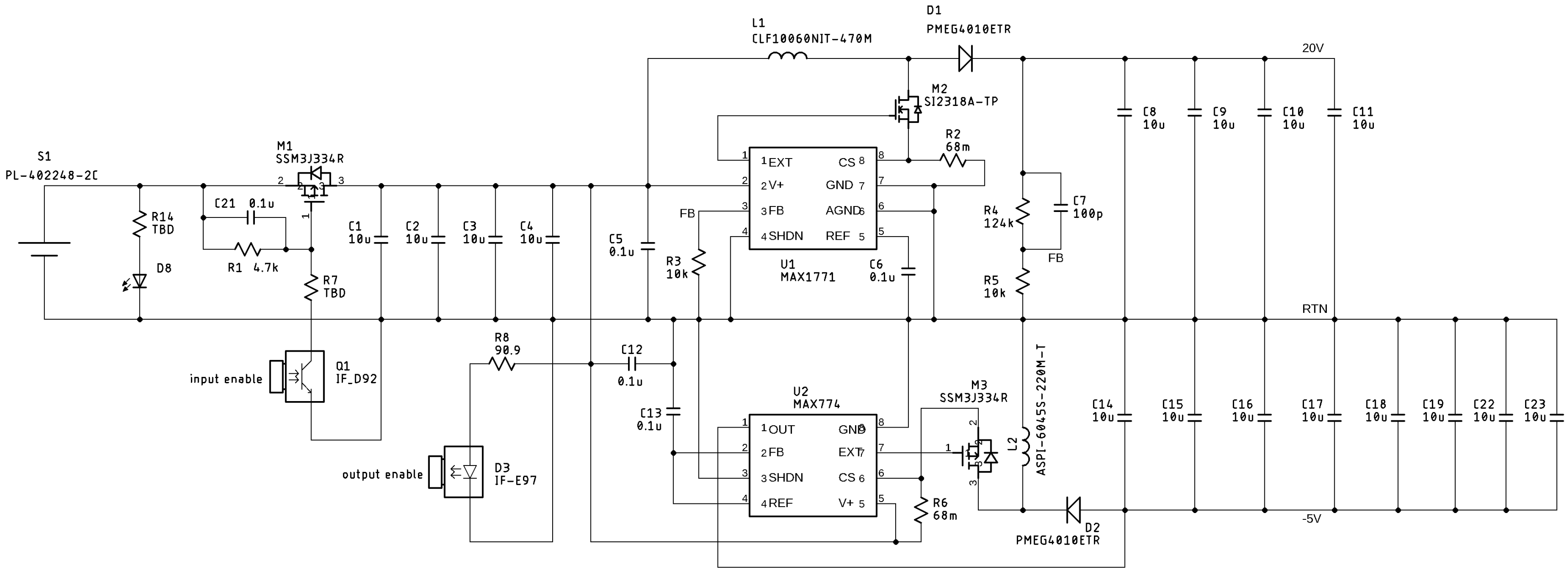

Fig. A-1 Battery-powered gate-driver design schematics, part 1

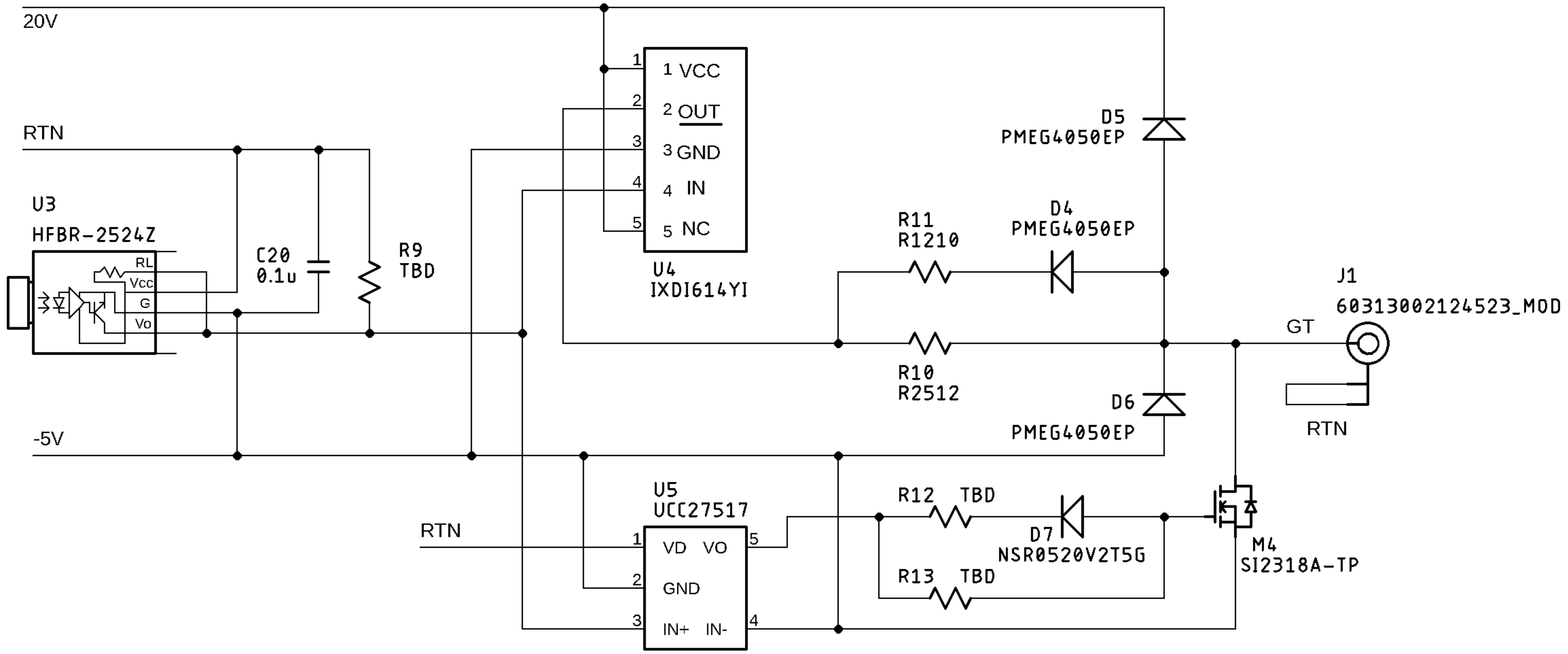

Fig. A-2 Battery-powered gate-driver design schematics, part 2

Appendix B. Printed Circuit Board Layout of the Battery-Powered Gate-Driver Design

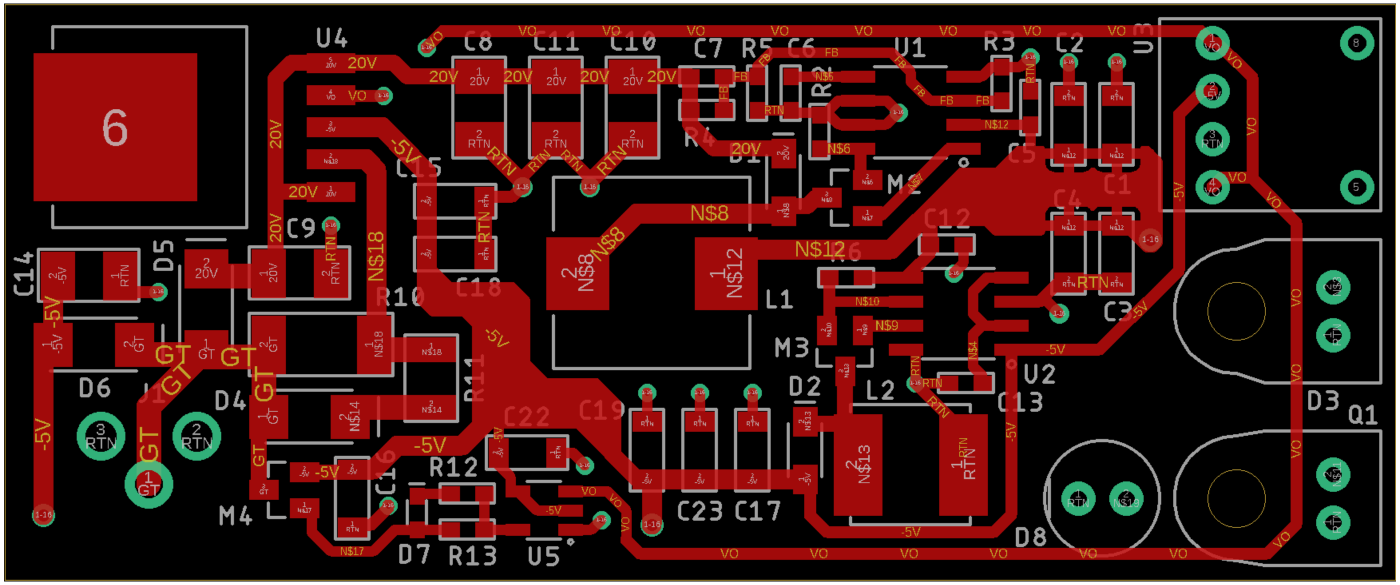

Fig. B-1 Top copper and silkscreen printed circuit board (PCB) layers of the battery-powered gate-driver design (scale: 2.5:1)

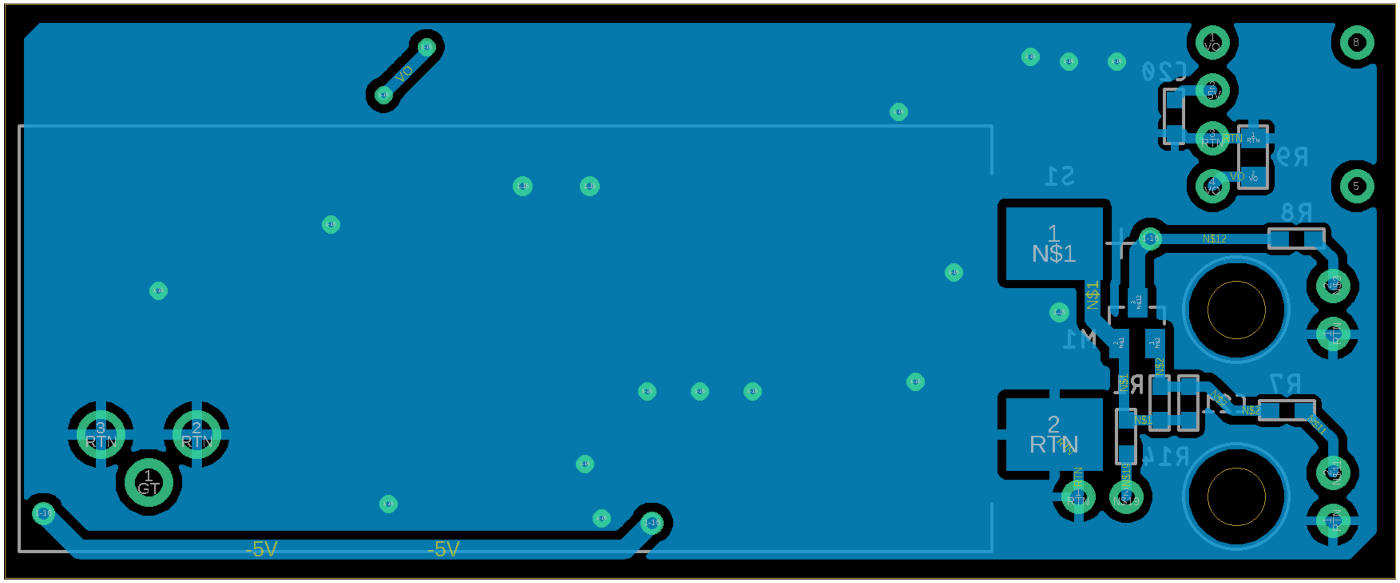

Fig. B-2 Bottom copper and silkscreen PCB layers of the battery-powered gate-driver design (scale: 2.5:1)

List of Symbols, Abbreviations, and Acronyms

ARL	Army Research Laboratory
DC	direct current
DEVCOM	US Army Combat Capabilities Development Command
IC	integrated circuit
IGBT	insulated-gate bipolar transistor
LED	light-emitting diode
MOSFET	metal–oxide–semiconductor field-effect transistor
PCB	printed circuit board
RTN	return
SiC	silicon carbide
SMA	SubMiniature version A
TBD	to be determined

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