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NEGATIVE CAPACITANCE ENABLED SCALING TO ACHIEVE 1 THz CUT-OFF FREQUENCY TRANSISTORS ON A CMOS PLATFORM

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Final Report

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14. ABSTRACT
Investigate the use of very completely new physical concept, namely utilizing negative capacitance in a ferroelectric oxide to boost Cox by using the ferroelectric oxide as a gate insulator in advanced transistors. This necessitated not only obtaining the desired physical effect but also material discovery and optimization to integrate with Si transistors.

15. SUBJECT TERMS
Negative Capacitance, effective oxide thickness (EOT), HZO Tri-gate FET, SOI transistor

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Table of Contents

Section **Page**

List of Figures ii
1 EXECUTIVE SUMMARY 1
2 TECHNICAL DETAILS 4
3 LIST OF PUBLICATIONS: 12
LIST OF ABBREVIATIONS, ACRONYMS, AND SYMBOLS 13

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List of Figures

Figure **Page**

Figure E1: Left Panel Measured Inversion Capacitance Commercially Available, Advanced Si Transistors, Right Panel Injection Velocity Showing NCFETs can Retain the Velocity Despite Enhanced Capacitance, Therefore Leading to Larger Current and Higher Frequency Operation Compared to most Advanced Si Transistors 2
Figure E2: Left Panel: TCAD Simulations Showing Scaling Roadmap for Different EOTs Including the EOT Demonstrated in the Program and Right Panel: TCAD Simulations Showing Program Goals as a Function of Lg as Enabled by Negative Capacitance from Left Panel........... 2
Figure 1: Energy Landscape Flattening 5
Figure 2: In-plane Synchrotron Grazing-incidence Diffraction (IP-GID) of a Bare 2 nm HfO_2-ZrO_2HfO_2 tri-layer Indexed to the Tetragonal P42/nmc and Orthorhombic $Pca2_1$ Phases (a) (left) and (Right) zoom-in of the Spectrum about the Orthorhombic $(111)_o$ and Tetragonal $(101)_t$ Reflections, Confirming the Co-existing Structural Polymorphs in the 2 nm film. (b) Two-dimensional Reciprocal Space Map of the Bare 2 nm HfO_2ZrO_2-HfO_2 trilayer, indexed by Integrating the Diffraction Spectrum. The lack of fully Polycrystalline Rings Illustrates that the 2 nm HfO_2-ZrO_2-HfO_2 trilayer is highly-oriented, consistent with TEM Imaging. (c) Synchrotron Spectroscopy (XAS) of the bare 2 nm HfO_2-ZrO_2-HfO_2 Trilayer at the (left) Hf M_3- and (center) Zr $L_{3,2}$-edges: (right) the Presence of Linear Dichroism (orbital polarization) provides Further Evidence of Symmetry-breaking in these Oriented Thin Films. (d)Second Harmonic Generation (SHG) Mapped Across the Bare 2 nm HfO_2-ZrO_2-HfO_2 trilayer; the presence of SHG intensity Confirms Broken Inversion Symmetry in these Ultrathin Ferroic Films 6
Figure 3: MIM C-V Hysteresis Loops for a Mixed FE-AFE HfO_2-ZrO_2 Multilayer Demonstrating Higher Capacitance Compared Against its AFE (ZrO_2) and FE (Zr:HfO_2) Counterparts of the Same Thickness (a), (b) Inverse Capacitance Versus Thickness of the MIM HfO_2-ZrO_2 Multilayers up to 5 Superlattice Repeats (10 nm), with an Extracted Permittivity of 52 , Extremely Large for HfO_2-based Oxides. (c) MIM *C-V* Hysteresis Loops for HfO_2-ZrO_2 Multilayers of the Same Periodicity Demonstrating an Evolution from Mixed-ferroic to FE-like Hysteresis upon cooling slightly below room Temperature. The proximity to the Temperature Dependent Phase Transition suggests the HfO_2-ZrO_2 Heterostructures Lies Near its Maximum Electric Susceptibility Position, Ideal for Negative Capacitance Stabilization. (d) MOS Accumulation *C-V* of HfO_2ZrO_2-HfO_2 Trilayer Compared to AFE ZrO_2, FE Zr:HfO_2, and DE HfO_2*,* all of the Same Thickness (2 nm), Indicating Mixed-ferroic Behavior is Optimal for Enhancing Capacitance Rather than Purely FE or AFE behavior. (e) Accumulation *C-V* of the HfO_2-ZrO_2-HfO_2 Trilayer Compared to Bilayer and solid Solutions Films of the Same Thickness (ALD cycles) and Composition (Hf:Zr cycles).Inset: Schematic of Multilayer versus solid Solution. (f) Accumulation *C-V* Curves for a 2 nm HfO_2-ZrO_2-HfO_2 Trilayer Grown on sub-nm SiO_2 fit to Effective Oxide thickness (EOT) Simulations. Inset: Gate Leakage of the Same Heterostructure Stack 7

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Figure **Page**

Figure 4: Wide field-of-view cross-Sectional TEM images of the HfO_2-ZrO_2 Multilayer Structure and its Corresponding Intensity Line Scan(a), (bottom right) Averaged Across the Entire Field-of-view (FoV) of the Top Cross-sectional Image (~ 150 nm. A physical SiO_2 Thickness of 8.6 Å is Extracted from Analysis of the Averaged Intensity Line Scan of the wide FoV TEM. (b) Electrically Obtained *Q-V* Relation from Dielectric HfO_2 and Al_2O_3 Thickness Series of SiO_2 + Si Charge Layer, fit to an 8.0 Å EOT Simulation 8
Figure 5: Measured Output Characteristics of the Lg=90 nm Transistors (a) and (b) Measured Transconductance 9
Figure 6: Small-Signal Equivalent Circuit Model (a), (b) Measured and Modeled S-Parameters (50MHz-10GHz) and (c) extracted Extrinsic and Intrinsic Model Parameters using S-parameter Fitting 10
Figure 7: Measured and Simulated Y-parameters show that the Improvement in Cgg and gm is Preserved in GHz Frequency Range (a), (b) VS Model Captures Charge Density Dependence of νinj. (c) High Charge Density for same VGS in HZO gives rise to 5% Higher νinj at VGS = 1.6, causing Additional Boost in gm... 10
Figure 8: 14% f_T Improvement in HZO FET Due to Higher gm and Increased Internal and External Capacitance Ratio in HZO FET (a), (b) Delay-time Analysis Shows that τ_{ext} has the Higher Impact on the Boost in f_T 11

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1 Executive Summary

Problem Statement and Approach: When one looks at the transit time of electrons through a short channel Si transistor it is found that below a channel length of 16 nm, the cut-off frequency should reach 1 THz. However, in practice, the cut-off frequency in Si transistors of similar gate length is found to be roughly half of that (~500 GHz). This discrepancy can be easily understood by recognizing the fact that the parasitic capacitance in very short channel transistors is roughly similar to the device capacitance itself:

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{ox} + C_{par}} = \frac{1}{2\pi}\frac{v}{L}\cdot\frac{1}{1 + C_{par}/C_{ox}}$$

Therefore, although counter-intuitive from a conventional point of view, one way to substantially improve the cut-off frequency of an advanced Si transistor will be to substantially increase Cox. However, increasing Cox faces fundamental challenges:

i. There is no known high-K oxide other than HfO_2 that is process compatible with Si and can satisfy the device reliability requirements

ii. Reducing interfacial SiO_2 comes with substantial reduction in mobility which then reduces the effective velocity leading to a zero-sum impact on f_T.

In this context we proposed a very completely new physical concept, namely utilizing negative capacitance in a ferroelectric oxide to boost C_{ox} by using the ferroelectric oxide as a gate insulator in advanced transistors. This necessitated not only obtaining the desired physical effect but also material discovery and optimization to integrate with Si transistors.

Main Achievements:

Fig. E1 summarizes our main accomplishments. As it can be seen from the left panel, we discovered and integrated a gate stack that led to the promised capacitance boost, essentially achieving substantially larger capacitance than most advanced, commercially available transistors. Importantly, as the right panel shows, transistor data showed that down to Lg=20 nm, the velocity of electrons did not get affected, indicating that the capacitance boost did not lead to any adverse effect on transport. These results present a breakthrough in electronic devices, enabling a capability that did not exist before.

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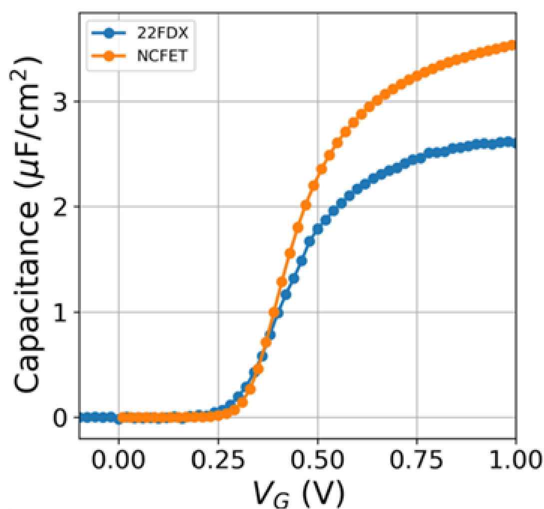


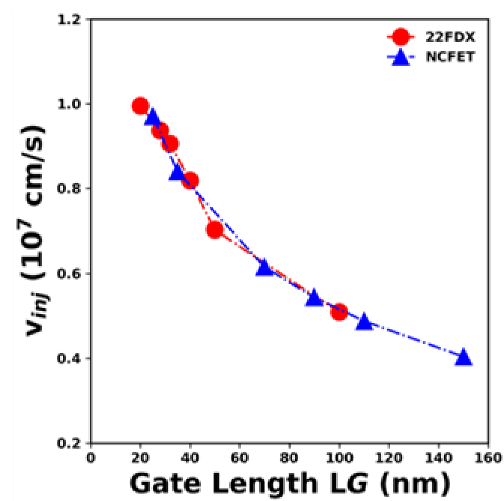
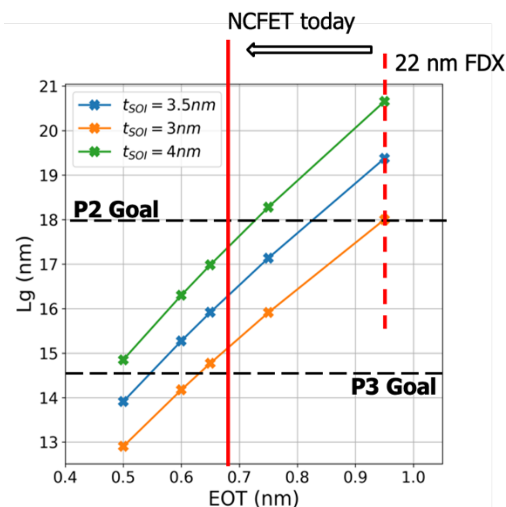


Figure E1: Left Panel Measured Inversion Capacitance Commercially Available, Advanced Si Transistors, Right Panel Injection Velocity Showing NCFETs can Retain the Velocity Despite Enhanced Capacitance, Therefore Leading to Larger Current and Higher Frequency Operation Compared to most Advanced Si Transistors



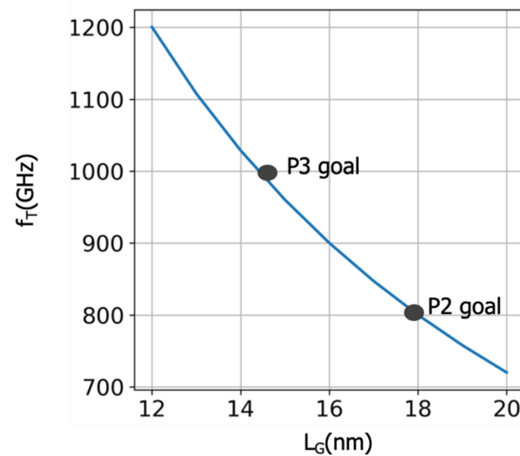


Figure E2: Left Panel: TCAD Simulations Showing Scaling Roadmap for Different EOTs Including the EOT Demonstrated in the Program and Right Panel: TCAD Simulations Showing Program Goals as a Function of Lg as Enabled by Negative Capacitance from Left Panel

Experimentally calibrated TCAD results showed that the capacitance boost will allow *planar transistors to scale to Lg~12-15 nm* which is sufficient to exceed the phase 3 goal of the program (see Fig. E2). We note that, the enabling of planar transistors to scale is crucial – conventionally below Lg=20 nm, FINFET technology has been used whose 3D geometry introduces substantial parasitic capacitance, making them inappropriate for ultra-high frequency operation.

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Conclusions: Unfortunately, the epi-reactor needed to fabricate source/drain for very short channel transistors broke down during COVID-19, which when much of this program was ongoing. Due to the lock-down and then supply chain issues, the tool could not be fixed and our short channel transistors had substantial $R_{S/D}$ which over-shadowed the high frequency performance of the devices at the phase 1 review. It was judged that we should not be allowed to go to the Phase 2.

Nonetheless, we achieved all the main scientific breakthroughs that we set out for. A number of 'first-in-the-field' results were published as a result of this program in both materials and devices (see the publication list at the end of this report). What remains is the fabrication of short channel transistors – there are no real barriers there. As we are coming out of COVID related complications, our toolset is operational again and we expect to soon see data from short channel transistors with good $R_{S/D}$. We remain committed to the overall goal of taking Si transistors beyond f_T~800 GHz and convinced that with the breakthrough we achieved with Negative Capacitance gate stacks, this goal will be achieved in near future.

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2 Technical Details

Recent results of negative capacitance (NC) in Ferroelectric materials [1-10] and negative capacitance field effect transistors (NCFET) have established that the NC effect [44,76,77] can provide a charge boost and an improved short channel effect. This provides a completely new avenue to improve the transistor performance in the ultra-scaled regime. In addition, the integration of the ferroelectric material necessary to obtain these benefits into Foundry process has already been demonstrated [44]. As a result, NCFET transistors shows significant potential to push the cut-off frequency of CMOS compatible Si transistors to new limits. In addition, NC enables novel pathways to control the properties of the ferroelectric material, which is also applicable to non-volatile memory devices. As a part of this program, we are synthesizing and optimizing ferroelectric materials with atomic control to enable devices, both logic and RF transistors and memory with unprecedented performance.

We note here that NC effect comes through the optimization and adoption of a new gate stack and as a result, it is a complimentary technology and its effect will be additive to any other performance booster approach that is being explored for conventional transistors such as ways to increase channel mobility, methods to reduce parasitic capacitance, techniques to improve series resistance and others. We will use the planar, FDSOI technology as our device platform as this platform has shown better behavior than bulk counterparts under radiation.

Technical Details:

RF transistors:

In advanced silicon transistors, the gate oxide is a series combination of an 8-8.5 Å interfacial SiO_2, formed with a self-limiting process, and a ~ 2 nm high-κ dielectric HfO_2 layer. A high capacitance of the gate oxide is desirable to suppress short channel effects. The capacitance is conventionally represented by effective oxide thickness (EOT), $EOT = t_{SiO2} + t_{HK}/(\varepsilon_{HK}/\varepsilon_{SiO2})$, where lower EOT represents higher capacitance. Therefore, the EOT minimum value is limited by the interfacial SiO_2 thickness. Indeed, even integrating HfO_2 as the high-κ layer, the EOT is typically ~9 Å. To go below this value, the semiconductor industry has implemented sophisticated scavenging techniques to reduce the SiO_2 thickness after the full gate stack is formed, which scales the EOT, but also results in undesirable leakage and mobility degradation.

To overcome the deleterious effects of scavenging when scaling EOT, we developed an ultrathin HfO_2-ZrO_2 superlattice gate stack that exploits mixed ferroelectric-antiferroelectric (FEAFE) order (Fig. 1a,b). Our films demonstrate mixed ferroic order down to 2 nm thickness -- the same thickness of high-κ oxide used in advanced transistors. Moreover, when integrated with silicon, it shows an overall EOT of <6.5 Å even though both transmission electron microscopy (TEM) and electrical characterization reveal 8.0-8.5 Å interfacial SiO_2 thickness, as is typically expected. The EOT shows a clear dependence on the specific sequence and layering, underlying atomic-level control of the gate oxide behavior. No scavenging of the interfacial SiO_2 results in substantially lower leakage current for the same EOT compared to benchmarks established by major semiconductor industries. In addition, no mobility degradation is observed as EOT is scaled with these HfO_2-ZrO_2 ferroic gate stacks. Furthermore, large ON current (1 mA/μm) obtained in L_g = 90 nm transistors indicate that there is no adverse effect on the carrier velocity.

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Therefore, ultrathin HfO_2-ZrO_2 multilayers exploiting ferroic order provide a new pathway toward energyefficient gate stacks for advanced transistors.

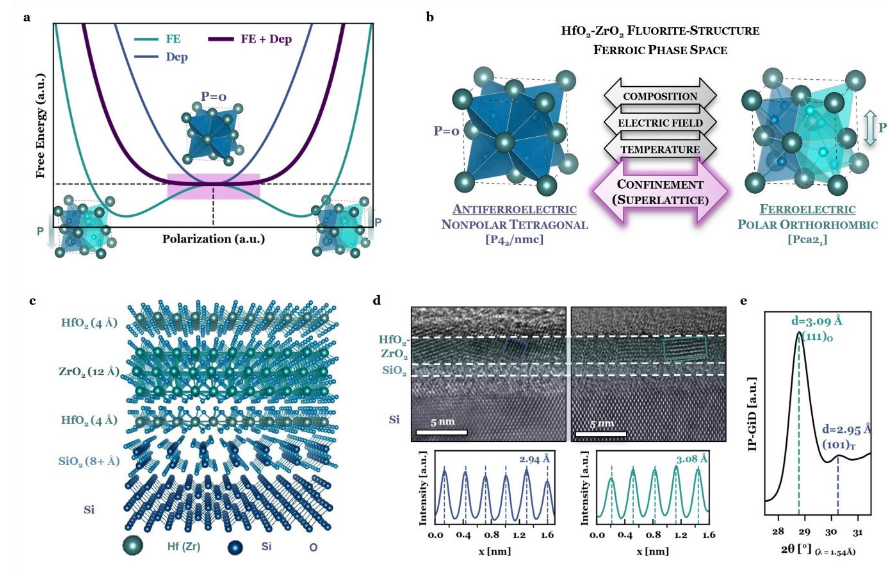

Figure 1: Energy Landscape Flattening

A ferroelectric (FE) double-well shaped energy landscape is flattened by the depolarization field energies (Dep) present in a laterally arranged polar-nonpolar (e.g. orthorhombic ferroelectric - tetragonal antiferroelectric) thin film system. The flattening of the energy landscape increases the permittivity of the overall system, as susceptibility is proportional to the inverse curvature of the landscape; such flattening is analogous to negative capacitance stabilization. (b) Engineering ferroic phase competition in the HfO_2-ZrO_2 fluorite-structure system. Beyond the conventionally-studied tuning parameters -- composition, electric field, temperature-- here we introduce dimensional confinement via superlattice layering to tailor ferroic phase competition at the atomic-scale. (c) Schematic of the HfO_2-ZrO_2 fluorite-structure multilayer on Si. (d) HR-TEM image of the atomic-scale HfO_2-ZrO_2 -HfO_2 trilayer (top) and extracted *d*-lattice spacings (bottom) corresponding to the fluoritestructure AFE tetragonal ($P4_2$/nmc, red) and FE orthorhombic ($Pca2_1$, blue) phases, respectively. Synchrotron IP-GiD demonstrating the presence of both the AFE *T*-phase $(101)_t$ and FE *O*-phase $(111)_o$ reflections whose *d*-lattice spacings are consistent with those extracted from TEM.

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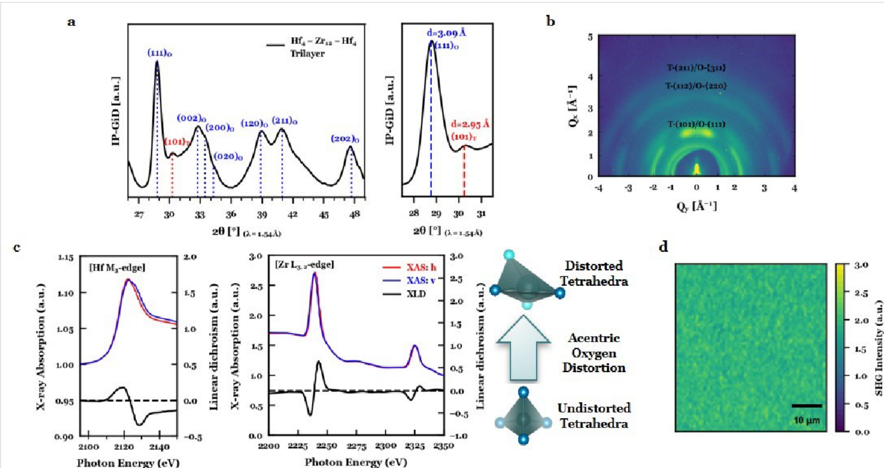

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Thin films of HfO_2-ZrO_2 were grown using ALD in which the nanolaminate periodicity is dictated by the sequence of Hf:Zr (4:12) ALD cycles before the Hf-Zr superstructure is repeated various times (Figure 1c). The underlying mixed ferroic order in these HfO_2-ZrO_2 heterostructures is established by high-resolution transmission electron microscopy (TEM) (Fig. 1d) and in-plane grazing incidence diffraction (Fig. 1e, Fig. 2a,b). Both techniques indicate the presence of the tetragonal ($P4_2/nmc$, T-) and orthorhombic ($Pca2_1$, O-) phases, which correspond to antiferroelectric and ferroelectric order in fluorite-structure films, respectively. Furthermore, local TEM imaging indicates the ferroelectric (orthorhombic) and antiferroelectric (tetragonal) phases are laterally intertwined (Fig. 1d). Synchrotron X-ray spectroscopy and optical spectroscopy further confirm the presence of inversion symmetry breaking in the 2 nm HfO_2-ZrO_2-HfO_2 heterostructure (Fig. 2c,d). The laterally-intertwined nonpolar-polar phases present in the ultrathin HfO_2-ZrO_2-HfO_2 heterostructure are conducive to flattening the ferroelectric energy landscape through depolarization fields (Fig. 1a). We also note that flattening of the energy landscape via depolarization fields is the same underlying principle of the negative capacitance effect, in which depolarization fields essentially stabilize the ferroelectric locally at a higher energy state compared to the ground state of an isolated, homogeneous ferroelectric.

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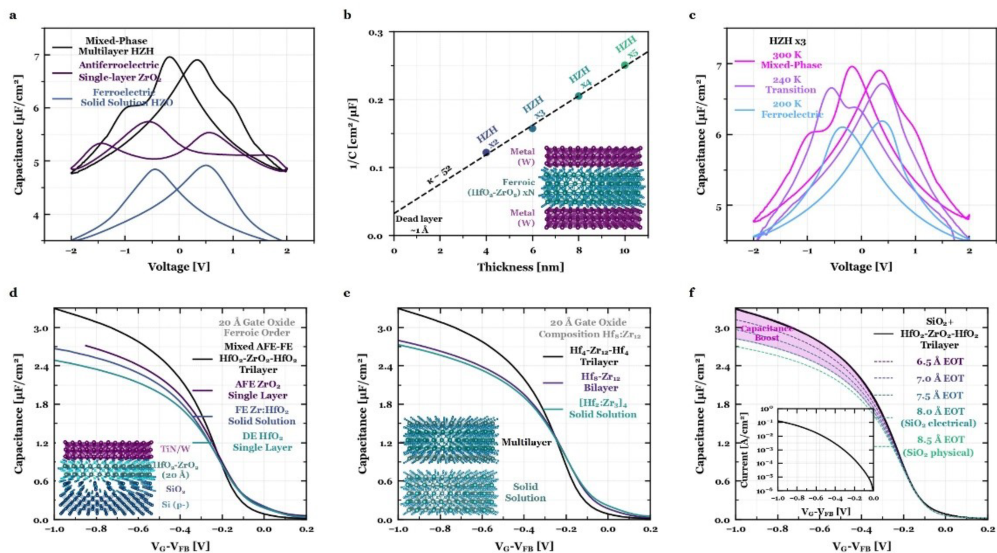

Figure 3: MIM C-V Hysteresis Loops for a Mixed FE-AFE HfO_2-ZrO_2 Multilayer Demonstrating Higher Capacitance Compared Against its AFE (ZrO_2) and FE (Zr:HfO_2) Counterparts of the Same Thickness (a), (b) Inverse Capacitance Versus Thickness of the MIM HfO_2-ZrO_2 Multilayers up to 5 Superlattice Repeats (10 nm), with an Extracted Permittivity of 52 , Extremely Large for HfO_2-based Oxides. (c) MIM *C-V* Hysteresis Loops for HfO_2-ZrO_2 Multilayers of the Same Periodicity Demonstrating an Evolution from Mixed-ferroic to FE-like Hysteresis upon cooling slightly below room Temperature. The proximity to the Temperature Dependent Phase Transition suggests the HfO_2-ZrO_2 Heterostructures Lies Near its Maximum Electric Susceptibility Position, Ideal for Negative Capacitance Stabilization. (d) MOS Accumulation *C-V* of HfO_2ZrO_2-HfO_2 Trilayer Compared to AFE ZrO_2, FE Zr:HfO_2, and DE HfO_2, all of the Same Thickness (2 nm), Indicating Mixed-ferroic Behavior is Optimal for Enhancing Capacitance Rather than Purely FE or AFE behavior. (e) Accumulation *C-V* of the HfO_2-ZrO_2-HfO_2 Trilayer Compared to Bilayer and solid Solutions Films of the Same Thickness (ALD cycles) and Composition (Hf:Zr cycles).Inset: Schematic of Multilayer versus solid Solution. (f) Accumulation *C-V* Curves for a 2 nm HfO_2-ZrO_2-HfO_2 Trilayer Grown on sub-nm SiO_2 fit to Effective Oxide thickness (EOT) Simulations. Inset: Gate Leakage of the Same Heterostructure Stack

The 2 nm trilayer on top of SiO_2 demonstrates lower EOT than the thickness of SiO_2 interlayer alone, carefully extracted via physical (8.5 Å) and electrical (8.0 Å) methodologies, providing evidence of capacitance enhancement. Overall, our optimized gate stacks show **record low EOT and record high capacitance** for an unscavanged stack.

To confirm the higher susceptibility in the mixed AFE-FE system directly, we performed capacitance-voltage (*C-V*) hysteresis loops in metal-insulator-metal (MIM) capacitor structures on thicker films with the same superlattice periodicity (Fig. 3a). Besides features indicative of mixed FE-AFE order, the total capacitance for the superlattice is larger than both conventional AFE ZrO_2 and FE Zr:HfO_2 of the same thickness (Fig. 3a), demonstrating enhanced susceptibility. To quantify the permittivity, capacitance measurements were performed across the superlattice thickness series. These measurements yield an extracted permittivity of ~ 52 (Fig.

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3b), which is larger than both FE orthorhombic Zr:HfO_2 and AFE tetragonal ZrO_2 values. Furthermore, low temperature *C-V* measurements for thicker HfO_2-ZrO_2 multilayers, where enhanced FE phase stabilization is expected, demonstrate an evolution from mixed-ferroic to FE-like hysteresis upon cooling slightly below room temperature (~240 K, Fig. 2c), consistent with temperature-dependent X-ray spectroscopy indicating transition from mixed tetragonal-orthorhombic phase to predominately orthorhombic structure at similar temperatures.

Next, the superlattices were grown on SiO_2-buffered Si substrates in metal-oxide semiconductor (MOS) capacitor structures. A 20-cycle thick multilayer was grown with ALD following the same stacking as before i.e. Hf:Zr:Hf 4:12:4. Accumulation *C-V* curves of the superlattice stack results in significantly larger capacitance in comparison to other conventional stacks -- DE HfO_2, AFE ZrO_2, FE Zr:HfO_2 -- of the same 20 Å thickness (Fig. 3d). Furthermore, the Hf:Zr:Hf 4:12:4 trilayer demonstrates enhanced capacitance compared to a bilayer (Hf:Zr 8:12) and solid solution (Hf:Zr $[2:3]_4$) of the same thickness and Hf:Zr composition (Fig. 3e). The overall energy landscape flattening, and corresponding increase in capacitance, is determined by the stacking of the atomic-scale HfO_2-ZrO_2 layers, rather than composition, as solid solution of the composition does not provide the same high capacitance (Fig. 3e). Furthermore, compared to HfO_2-ZrO_2 solid solutions across a range of Zr-rich compositions, the HfO_2-ZrO_2-HfO_2 multilayer demonstrates larger capacitance. This indicates the enhanced capacitance in HfO_2-ZrO_2-HfO_2 films is not simply driven by doping, but can instead be tuned by the configuration of the multilayer structure.

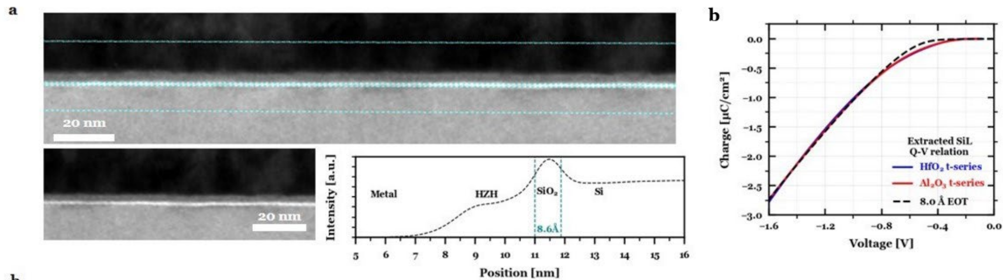

Figure 4: Wide field-of-view cross-Sectional TEM images of the HfO_2-ZrO_2 Multilayer Structure and its Corresponding Intensity Line Scan(a), (bottom right) Averaged Across the Entire Field-of-view (FoV) of the Top Cross-sectional Image (~ 150 nm. A physical SiO_2 Thickness of 8.6 Å is Extracted from Analysis of the Averaged Intensity Line Scan of the wide FoV TEM. (b) Electrically Obtained *Q-V* Relation from Dielectric HfO_2 and Al_2O_3 Thickness Series of SiO_2 + Si Charge Layer, fit to an 8.0 Å EOT Simulation

To quantify the observed capacitance, we performed EOT simulations of MOS capacitors using the industry standard model Synopsys simulation platform. The Hf:Zr:Hf 4:12:4 trilayer stacks vary between 6.5-7.0 Å EOT (Fig. 3f), consistent over many measured capacitors. Notably, this EOT is smaller than the expected thickness of the interfacial SiO2 layer (8.0-8.5 Å), as mentioned above. To investigate further, we performed high-resolution TEM of our gate stacks (Fig. 4a) which illustrates the SiO_2 thickness is indeed ~ 8.5 Å. To supplement this physical characterization, we next implemented electrical characterization of the interfacial layer via standard inverse capacitance vs thickness analysis of conventional dielectric HfO_2 and Al_2O_3 thickness series grown on the same SiO_2, yielding 8 Å (Fig. 4b), consistent with the HR-TEM

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results. Moreover, the consistent interlayer thickness extracted from both material systems indicates that neither Hf nor Al encroaches into the interfacial SiO_2 which would reduce its thickness and/or increase its permittivity. So, considering the interfacial layer thickness as 8 Å, the HfO_2-ZrO_2-HfO_2 multilayer gate stack demonstrates an overall EOT ~1.5 Å lower than the constituent SiO_2 thickness.

To test the ON current capability

y, a L_g = 90 nm device was fabricated on a SOI transistor with 18 nm SOI thickness and the superlattice gate stack. The transfer and output characteristic of a typical transistor are shown in Fig. 5a,b. It is found that at a drain voltage (V_d) and overdrive voltage ($V_{ov} = V_g - V_t$) of 1 V, the drain current exceeds 1 mA/µm. Fig. 5(b) shows the measured transconductance in comparison to state of the art. We note that our devices achieve the record transconductance for 90 nm Lg transistors.

A manuscript summarizing these results are currently in review.

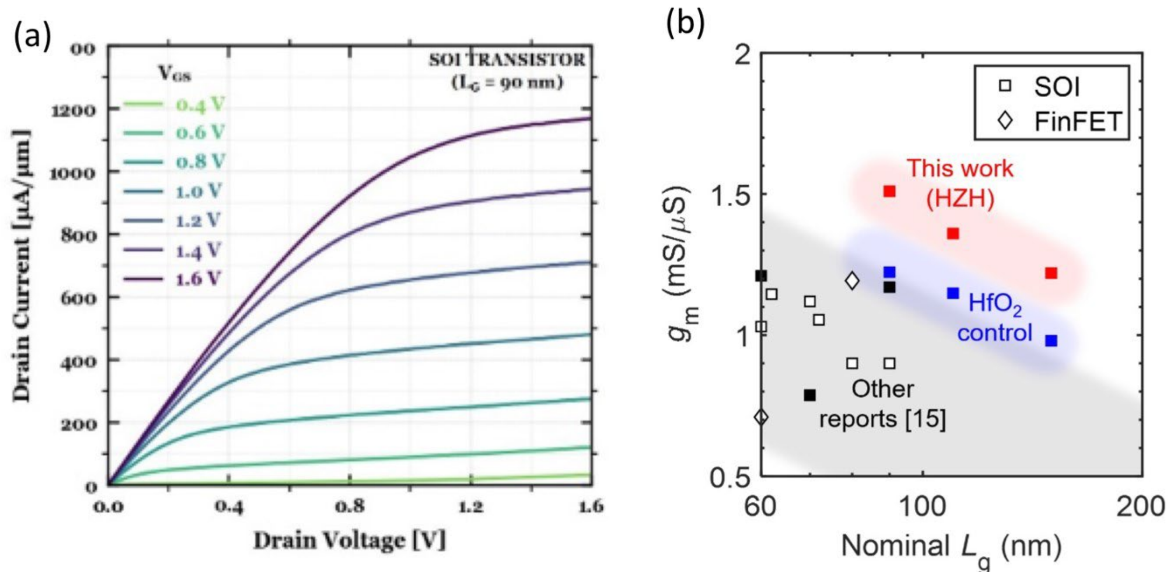

Figure 5: Measured Output Characteristics of the Lg=90 nm Transistors (a) and (b) Measured Transconductance

in comparison with state of the art. NCFETs show a record transconductance.

HZO Tri-gate FET RF Characteristics:

To investigate RF performance improvement in HZO FET, s-parameters are measured on 300nm LG trigate FETs under saturation (|VDS|=1.0V, |VGS|=0.0 to 1.2V) bias conditions from 10MHz to 50GHz. The small-signal circuit model as shown in Fig. 6(a) is used to model the measured S-parameters under saturation condition (VGS at peak transconductance) (Fig. 6(c)-(d)), with excellent agreement for both HZO and HfO2 FETs. The equivalent circuit model parameters are shown. Gate-capacitance (Cgg) and transconductance (gm) extracted from measured Y-parameters, after de-embedding the effect of gate resistance (Y'-parameters), show the improvement in Cgg and gm is preserved up-to GHz range (Fig. 7(a)), indicating the potential

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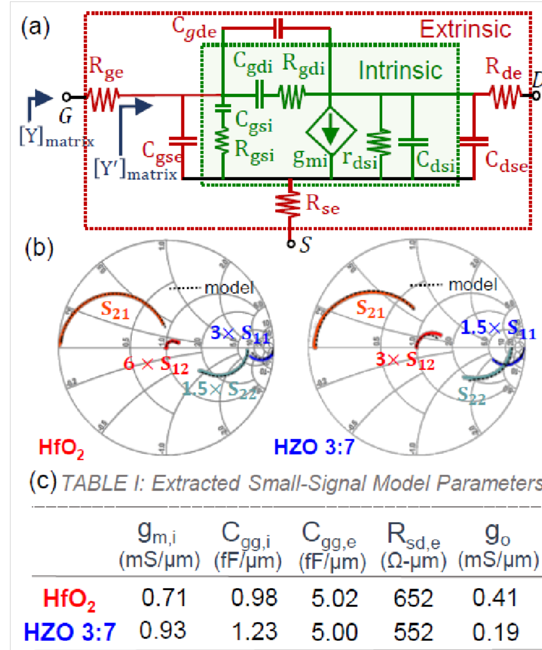
of HZO FETs for high-frequency applications. It is to be noted that the injection velocity of carriers in the channel (vinj) has a dependence on channel charge, as captured by Virtual-source (VS) model in Fig. 7(b). Higher carrier concentration in HZO FET, also contribute to 5% higher vinj (Fig. 7(c)) and additional boost in gm. Furthermore, fT is determined from -20 dB/dec extrapolation of current gain h21 to 0 dB, as shown in Fig.8. fT is boosted by 14% in HZO FET compared to the baseline due to 1) higher gm and 2) increased ratio of internal and external



(c) *TABLE I: Extracted Small-Signal Model Parameters*

	$g_{m,i}$ (mS/µm)	$C_{gg,i}$ (fF/µm)	$C_{gg,e}$ (fF/µm)	$R_{sd,e}$ (Ω-µm)	g_o (mS/µm)
HfO_2	0.71	0.98	5.02	652	0.41
HZO 3:7	0.93	1.23	5.00	552	0.19

Figure 6: Small-Signal Equivalent Circuit Model (a), (b) Measured and Modeled S-Parameters (50MHz-10GHz) and (c) extracted Extrinsic and Intrinsic Model Parameters using S-parameter Fitting

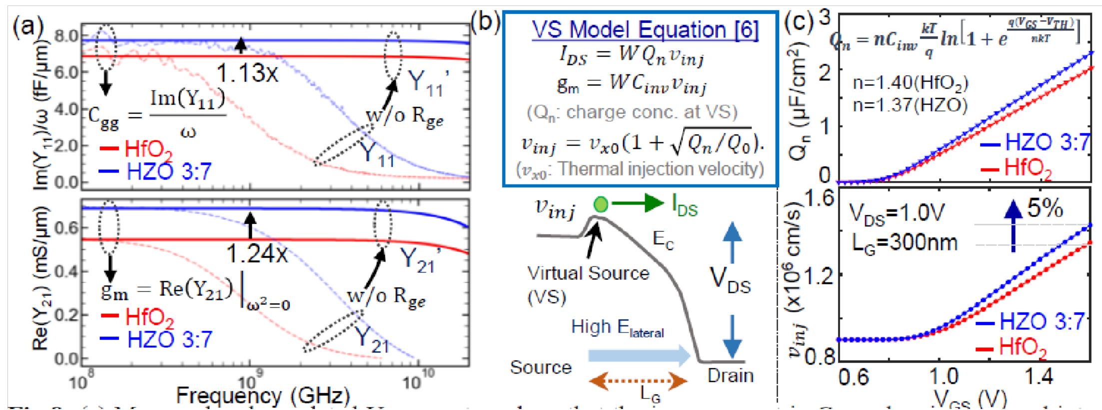


Figure 7: Measured and Simulated Y-parameters show that the Improvement in Cgg and gm is Preserved in GHz Frequency Range (a), (b) VS Model Captures Charge Density Dependence of *v*inj. (c) High Charge Density for same VGS in HZO gives rise to 5% Higher *v*inj at VGS = 1.6, causing Additional Boost in gm

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capacitance in higher-κ HZO FET. Delay-time analysis reveals that external parasitic delay (τ_{ext}) is primarily contributing to the improved fT, due to higher gm in higher-κ HZO FET. Some improvement in transit time (τ_t) is due to improvement in vinj.

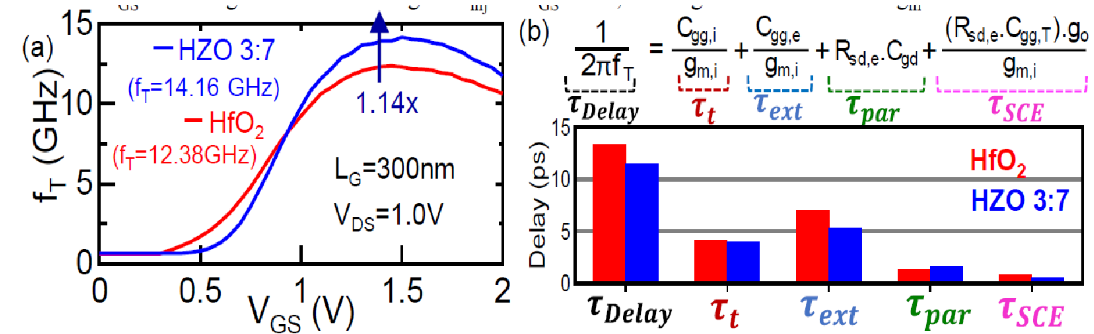

Figure 8: 14% f_T Improvement in HZO FET Due to Higher gm and Increased Internal and External Capacitance Ratio in HZO FET (a), (b) Delay-time Analysis Shows that τ_{ext} has the Higher Impact on the Boost in f_T

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3 List of Publications:

1. Suraj S. Cheema, Nirmaan Shanker, Shang-Lin Hsu et al. and **Sayeef Salahuddin,** "Emergent ferroelectricity in subnanometer binary oxide films on silicon," *Science,* 2022.
2. Cheema, Suraj S., Nirmaan Shanker, Li-Chen Wang, Cheng-Hsiang Hsu, Shang-Lin Hsu, Yu-Hung Liao, Matthew San Jose, … and **Sayeef Salahuddin** . "Ultrathin ferroic HfO2–ZrO2 superlattice gate stack for advanced transistors." *Nature* 604, no. 7904 65-71, 2022
3. W Li and L C Wang and S S Cheema and N Shanker and J H Park and Y H Liao and S L Hsu and C H Hsu and S Volkman and U Sikder and.. and **Sayeef Salahuddin,** **"**Demonstration of Low EOT Gate Stack and Record Transconductance on Lg= 90 nm nFETs Using 1.8 nm Ferroic HfO2-ZrO2 Superlattice," 2021 IEEE International Electron Devices Meeting (IEDM), 13-16, 2021.
4. W. Chakraborty et al, "Higher-k Zirconium Doped Hafnium Oxide (HZO) Trigate Transistors with Higher DC and RF Performance and Improved Reliability", VLSI Symposium 2021
5. S. Cheema, D. Kwon, N. Shanker, R. dos Reis, S.-L. Hsu,J. Xiao, H. Zhang, R. Wagner, A. Datar,

   M. McCarter, C. R. Serrao, A. K. Yadav, G. Karbasian,C.-H. Hsu, A. Tan, L.-C. Wang, V. Thakare, X. Zhang,A. Mehta, E. Karapetrova, R. Chopdekar, P.Shafer, E. Arenholz, C. Hu, R. Proksch; R.

   Ramesh, J. Ciston, **Sayeef Salahuddin,** "Ultrathin-Enhanced Ferroelectrocity Directly on Silicon," *Nature, 580, no. 7804 (2020): 478-482*

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LIST OF ABBREVIATIONS, ACRONYMS, AND SYMBOLS

ACRONYM	DESCRIPTION
AFRL	Air Force Research Labs
ALD	Atomic Layer Deposition
CMOS	Complementary Metal Oxide Semiconductor
DARPA	Defense Advanced Research Projects Agency
DEP	Depolarization Field Energies
EOT	Effective Oxide Thickness
FDSOI	Fully Depleted Silicon Insulator
FE	Ferroelectric
FEAFE	Ferroelectric-Antiferroelectric
NC	Negative Capacitance
NCFET	Negative Capacitance Field Effect Transistors
TEM	Transmission Electron Microscopy

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