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Sub-Millisecond Pulse Power Evaluation of High-Voltage Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) and High-Voltage SiC Insulated Gate Bipolar Transistor (IGBT)

by Aderinto Ogunniyi, Heather O'Brien, and Miguel Hinojosa

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Aderinto Ogunniyi, Heather O'Brien, and Miguel Hinojosa
DEVCOM Army Research Laboratory

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14. ABSTRACT
This work presents the pulse evaluation and characterization of a 10-kV silicon carbide (SiC) metal-oxide-semiconductor field effect transistor (MOSFET) and 27-kV SiC insulated gate bipolar transistor (IGBT). These devices are ideal for high-voltage, fast-switching, and high-power density electronic applications due to their superior material properties compared with their silicon counterpart. The static and transient performance of these devices were investigated and reported. The goal of the evaluation is to assess the sub-millisecond pulse current handling capabilities of these power devices.

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1. Introduction

The US Combat Capabilities Development Command Army Research Laboratory (ARL) is investigating high-voltage (HV) switches for high-power modules essential for robust and reliable high-power, dense, and compact pulsed-power systems. Silicon carbide (SiC) HV power switches have attracted attention as an alternative solution for various Army-specific high-power continuous- and pulsed-power applications. SiC's enhanced material properties such as high critical electric field, low intrinsic carrier concentration, and high thermal conductivity, high saturation velocity, and high Young's modulus compared with its Si counterpart.[1,2]

2. PSPICE Simulation and Pulse-Forming Network (PFN) Circuit

The sub-millisecond pulse-power evaluations of 10-kV SiC metal-oxide-semiconductor field-effect transistor (MOSFET) and 27-kV SiC insulated gate bipolar transistor (IGBT) were implemented at ARL. To study switching performance in sub-millisecond power pulse, a PFN that could generate wider pulse widths was modeled. Using stages of 1-µF capacitors and 80-µH inductors, a relatively square pulse can be generated out to 100 µs. As designed, the circuit is expected to produce a rise time of 5.7 µs, peak current overshoot of 210 A (at 4500-V initial charge), and pulse width of 0.1 ms. The inductor closest to the power switch can be reduced in value to enable faster current rise if desired. Load resistance can be increased to switch less current at higher charge voltage. Ripples at the tail end of the simulated current pulse may be eliminated by pulling the power switch gate negative when the current falls off. A PSPICE-simulated PFN circuit with 5 stages of 1-µF capacitors and 80-µH inductors is illustrated in Fig. 1. The circuit simulation depicts a charge voltage started at 4500 V and load resistance of 15 Ω utilizing an ideal closing switch. The simulated switch current of the PFN has a rise time of 5.7 µs with a peak current overshoot of 210 A (at 4500-V initial charge) and pulse width of 0.1 ms, as shown in Fig. 2.

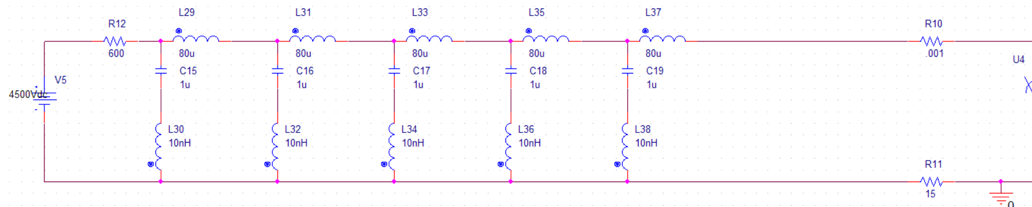

Fig. 1 PSPICE circuit simulation of PFN circuit

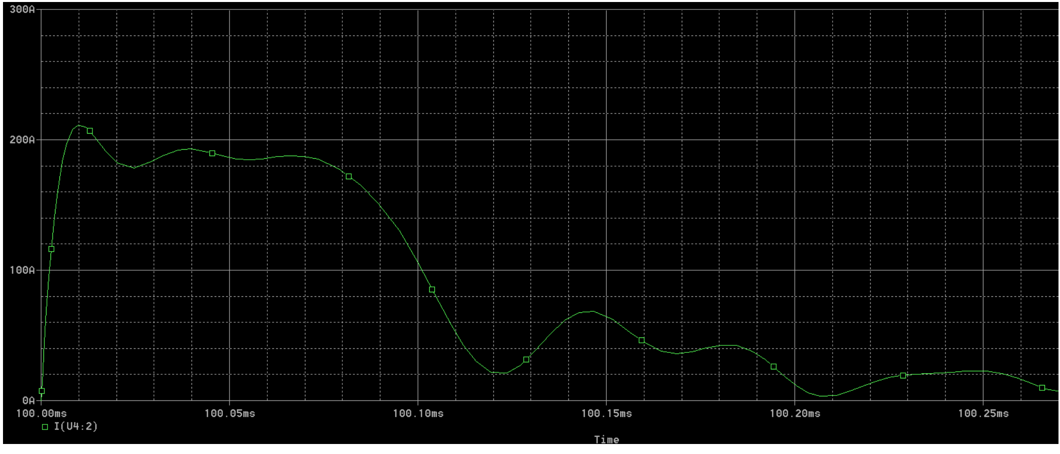

Fig. 2 Pulse current waveform of PSPICE simulation of PFN circuit

Both HV MOSFET and IGBT switches were used to discharge a 5-stage PFN into a 15-ohm resistive load. An image of the PFN used to evaluate the HV switches is shown in Fig. 3.

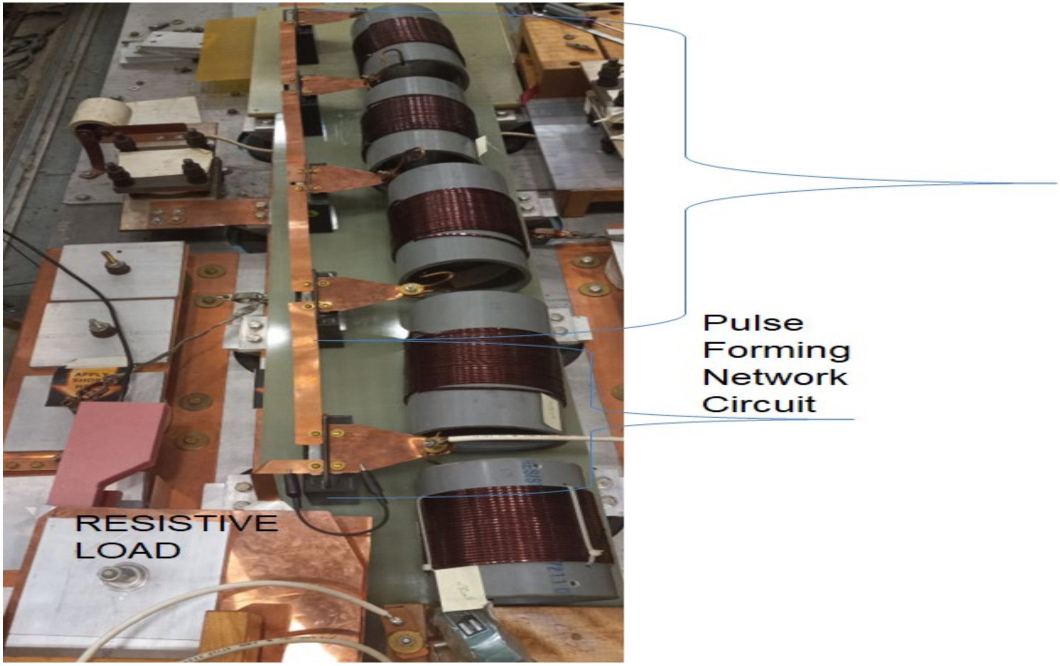

Fig. 3 Pulse-forming network circuit

An in-house custom-designed probe was used to accurately measure the forward voltage drop of both the SiC MOSFET and SiC IGBT to assess the safe operating area of the power devices in the PFN circuit, the pulsed waveform of the device under test (DUT) in PFN is displayed in Fig. 4.

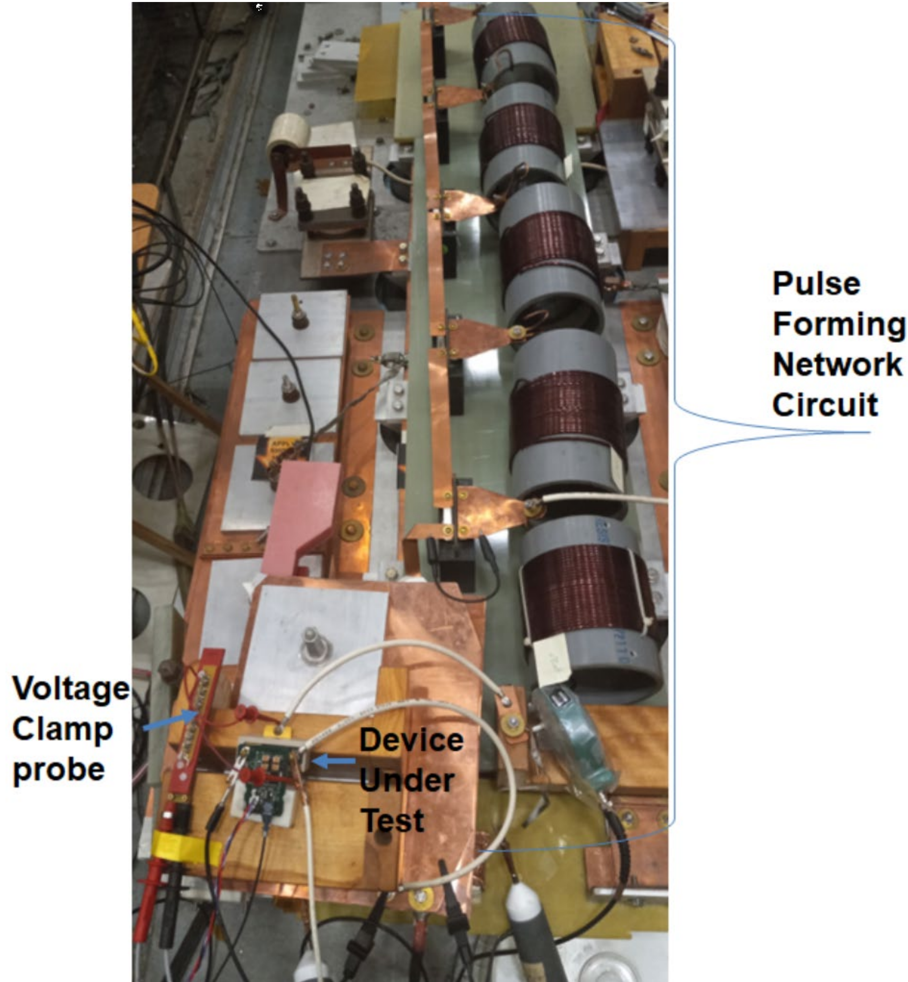

Fig. 4 PFN circuit with DUT and voltage clamping probe

3. Voltage Clamping Probe

The primary purpose of the voltage clamping probe is to accurately acquire the On-state voltage of the DUT. The voltage clamping circuit comprises depletion mode (D-mode) Si-MOSFETs, resistors, Schottky diodes, and a Zener diode. The DUT On-state measurement voltage probe is shown in Fig. 5; the On-state voltage is measured across the Zener diode. The voltage clamping circuit functionality is as follows: When DUT is On, the D-mode Si-MOSFET is in On-state, and the drain and source terminal is essentially the same terminal or a shorted one, enabling a voltage drop solely across the terminal of the Zener diode. Moreover, the Zener diode only reversely conducts a few microamperes, so its conduction loss does not affect the measurement, and DUT On-state voltage can be measured directly. When the DUT is Off, the Zener diode junction capacitance is charged at first, then the D-mode MOSFET is pinched Off and its output interelectrode capacitance (C_{ds}) is charged to withstand the blocking voltage of the device.

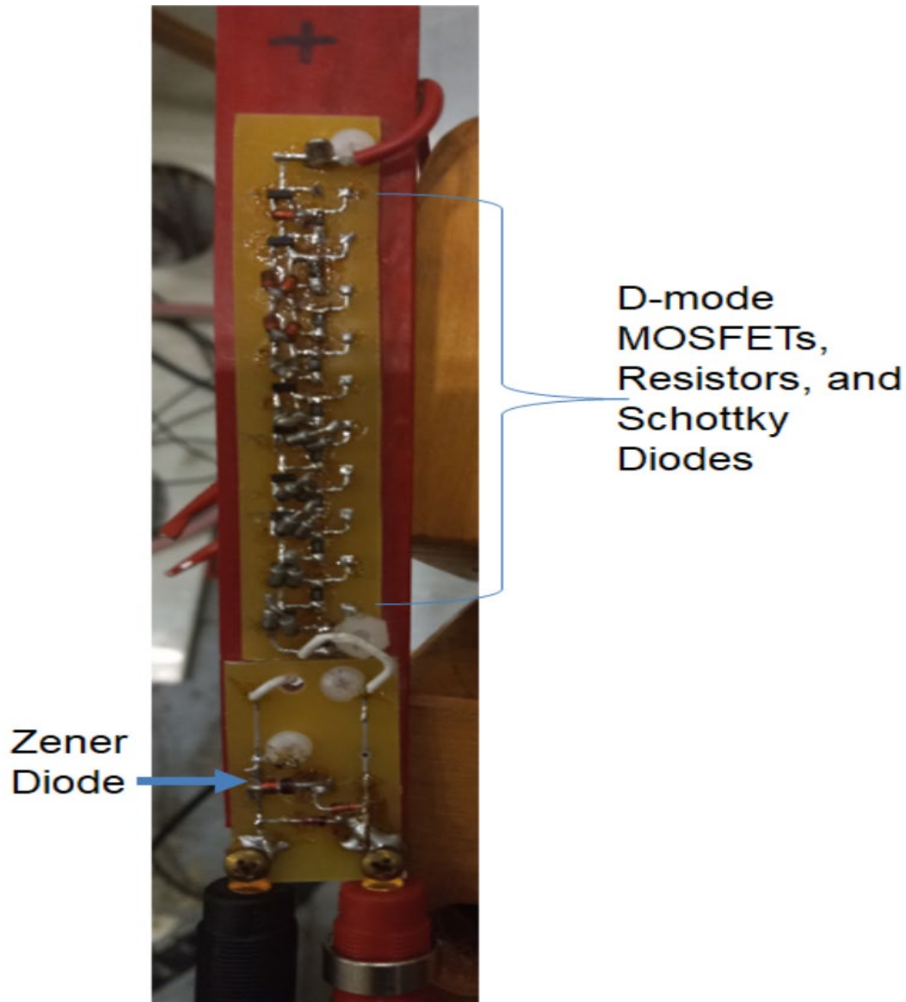

Fig. 5 In-house voltage-clamped probe design

4. High-Voltage SiC MOSFET and SiC IGBT

The 4H-SiC MOSFET evaluated in the PFN circuit is an 8.1- × 8.1-mm chip area with an active area of 21.6 mm^2. A cross-section view of the 10-kV 4H-SiC MOSFET is displayed in Fig. 6. The gate of the device is planar with a double-diffused metal-oxide-semiconductor (DMOS) structure. An epitaxially grown n-type low-doped drift region thickness of 100 µm was grown to enable the 10-kV blocking of the device in the Off-state.[3] Aluminum metallization was implemented on the top surface of the device's gate and source terminals. The device has a continuous current rating of 10 A and was capable of withstanding 10 kV in the Off-state.

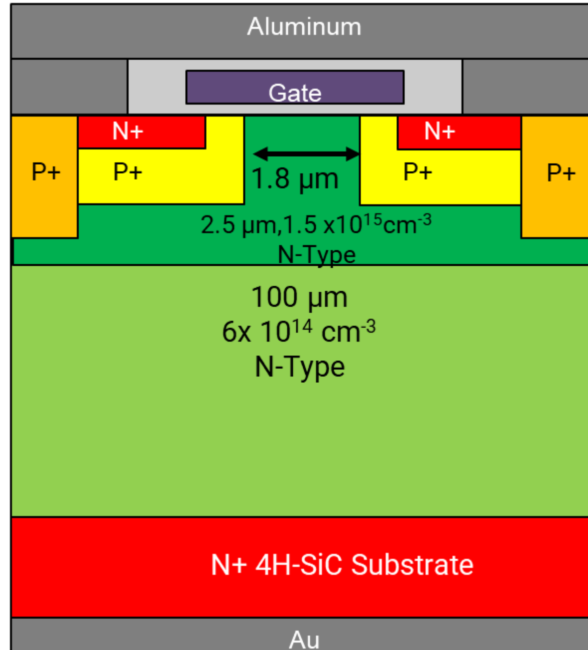

Fig. 6 Cross-section view of 4H-SiC DMOSFET

The forward conduction characteristics of the MOSFET are shown in Fig. 7. The IV characteristics of HV SiC MOSFET are similar, with gate bias ranging from 15 to 25 V due to the drift layer (100 µm) being the primary contributor of the on-resistance of the MOSFET. The HV MOSFET switch is depicted in Fig. 8, which illustrates a 10-kV MOSFET die in which the backside region serves as the die-attach to a gold-plated copper drain terminal. The topside of die consists of four emitter fingers and one gate pad, and these pads are connected to their respective terminals using 10-mil wire-bonds per pad while being epoxied and enclosed in a high-temperature polyethertherketone (PEEK) package.

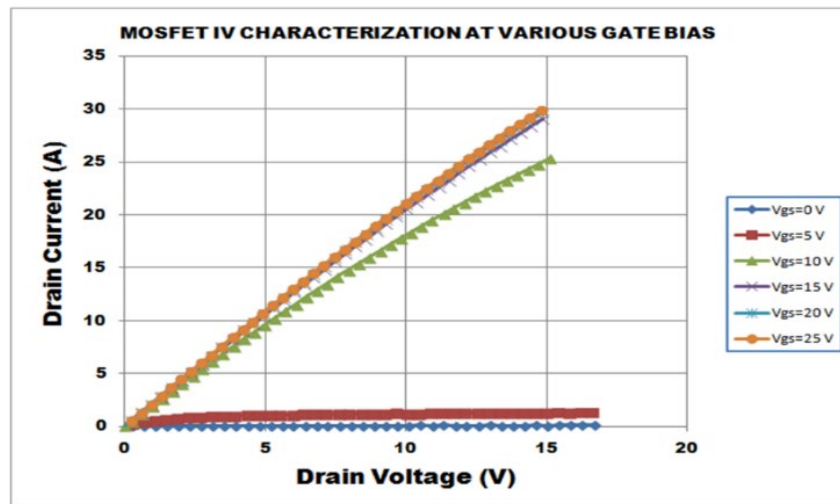

Fig. 7 Forward current-voltage (I-V) characterization of 10-kV SiC MOSFET

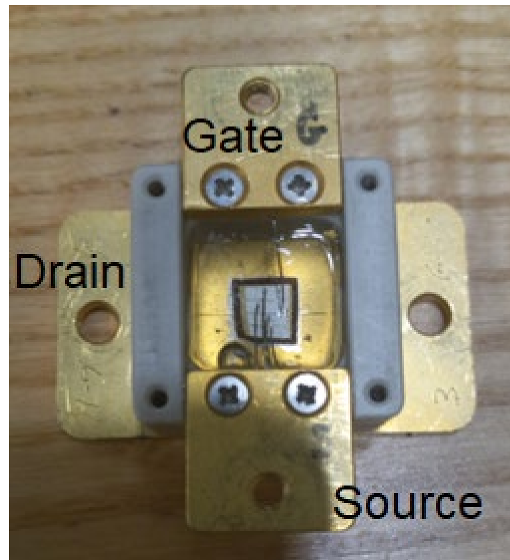

Fig. 8 Packaged 10-kV SiC MOSFET switch

The 4H-SiC IGBTs used in the PFN circuit were vertical power devices with a thin P-type substrate and an epitaxially grown, 230-µm-thick, N-type drift region. The devices have a DMOS structure, an asymmetrical punch-through design, and a field-stop buffer of approximately 2 µm. Their nominal breakdown voltage was 22–24 kV at a leakage current of 10–14 µA. Their active area was 0.28 cm^2 and an 0.81-cm^2 chip area.[4,5] Figure 9 shows the forward-conduction characteristics of the HV SiC IGBT. Figure 10 depicts a 9- × 9-mm chip-area IGBT die where the backside region serves as the die-attach to a gold-plated copper collector terminal. The topside of die consists of four emitter fingers and one gate pad, and these pads are connected to their respective terminals using two 10-mil wire-bonds per pad while being encapsulated and enclosed in a high-temperature PEEK package.

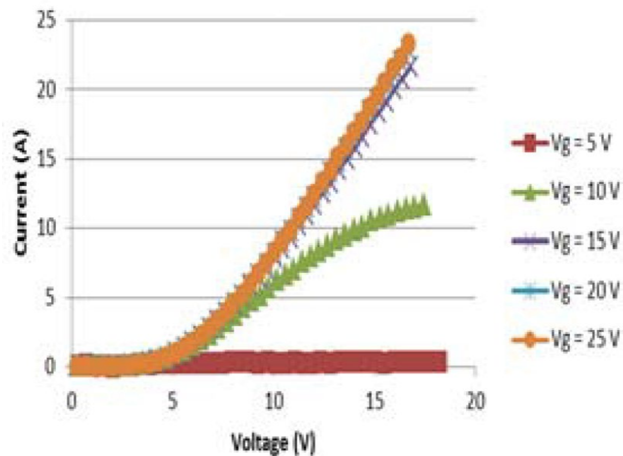

Fig. 9 Forward I-V characterization of HV SiC IGBT

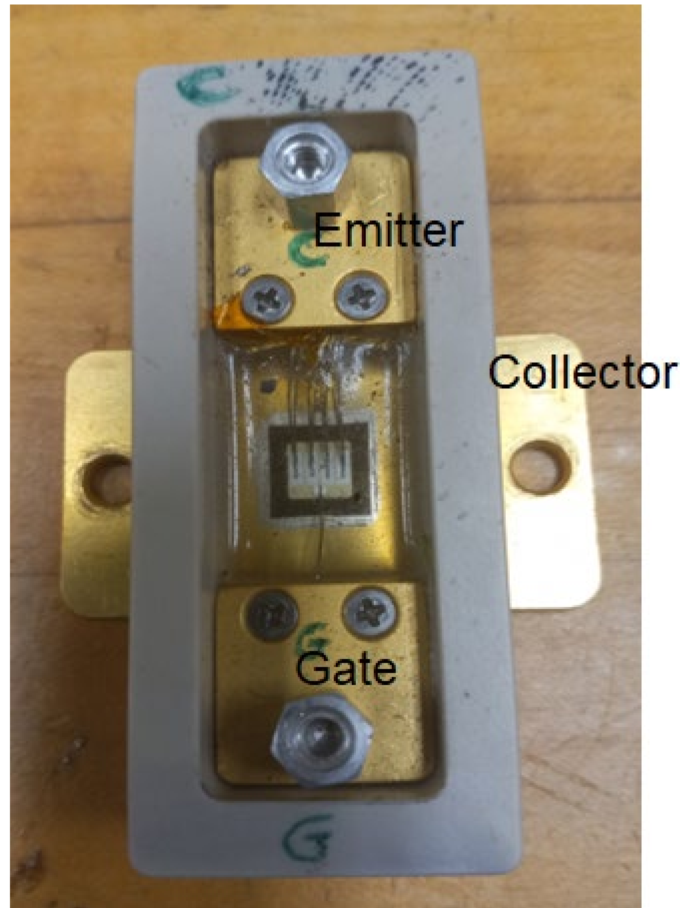

Fig. 10 Packaged HV SiC IGBT

5. Pulse-Power Evaluation Analysis

The gate bias voltage range used to switch the HV IGBT and HV MOSFET was +20 V/–5 V. For these HV devices, a gate bias of 20 V was sufficient to attain the minimal on-resistance while maintaining the integrity of the gate oxide. The –5 V on the gate is used to turn the device off sufficiently. For this evaluation the gate was kept on throughout the duration of the PFN current pulse waveform, ensuring the energy of the PFN was completely discharged. The pulse width of the gate for these devices ranged from 0.5 to 1 ms. The charge voltage on the PFN circuit was increased incrementally to assess the safe operation area of the SiC MOSFET and SiC IGBT. The charge voltage and load voltage were measured using PMK 1000:1 passive HV probes, and the pulse current was measured with a Pearson 10:1 current monitoring probe.

Figure 11 depicts the pulse analysis of SiC MOSFET in the PFN circuit at 40 A. Table 1 displays the pulse evaluation of the die at 40 A in the PFN circuit; the SiC MOSFET withstood a dI/dT of 7 A/µs with a transient peak power of 800 W and

energy dissipation of 6 mJ. The SiC MOSFET was subsequently pulsed over 100 times at this current level with no noticeable variation in the measurement of the forward voltage.

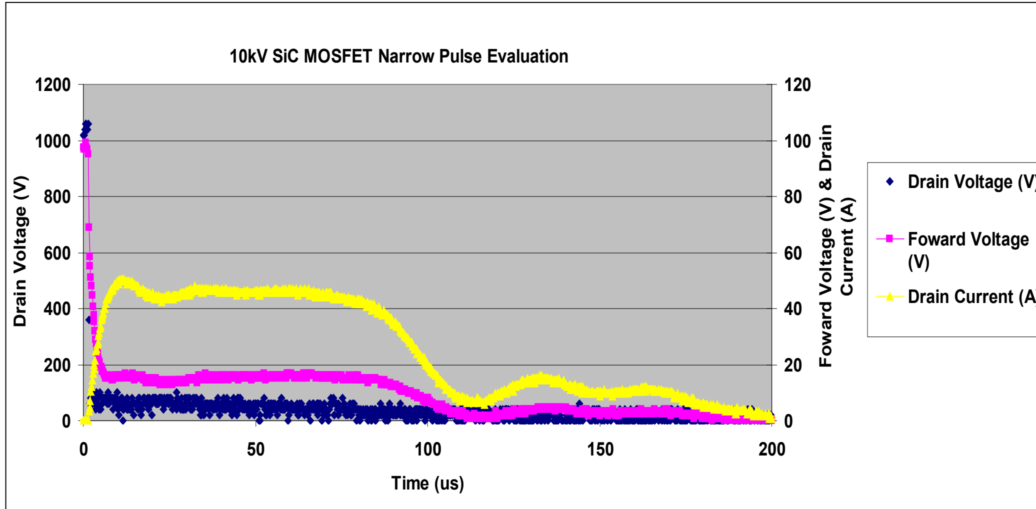

Fig. 11 Narrow pulse evaluation of 10-kV SiC MOSFET at 40 A. Primary axis: blue, drain voltage, and secondary axis: purple, On-state voltage; yellow, current.

Table 1 High-voltage SiC MOSFET analysis at 40 A

Die Analysis:	
dI/dt 10-90: (A/µs)	7.1428571
Current Base Width: (µs)	110
Max Instant Power: (W)	800
Action: (A^2 *S)	0.1837919
Energy: (J)	0.0063426

The SiC MOSFET was successfully evaluated up to 110 A at the plateau region with an overshoot of 120 A at the front edge of the pulse current in the PFN circuit (Fig. 12). The forward voltage of the SiC MOSFET at 110 A approached 62 V toward the tail end of the pulse. Table 2 displays results of the die-pulse evaluation at 110 A; the SiC MOSFET was subjected to a *dI/dT* of 15 A/µs with a transient peak power of 7000 W and energy dissipation of 50 mJ. This HV switch was subsequently pulsed over 100 times at 110 A with no variation in the On-state voltage. The forward voltage hump at 110 A of the SiC MOSFET is an indicator that current crowding is occurring in the device, and there is a higher possibility of catastrophic failure if the drain current magnitude exceeds this level.[6,7]

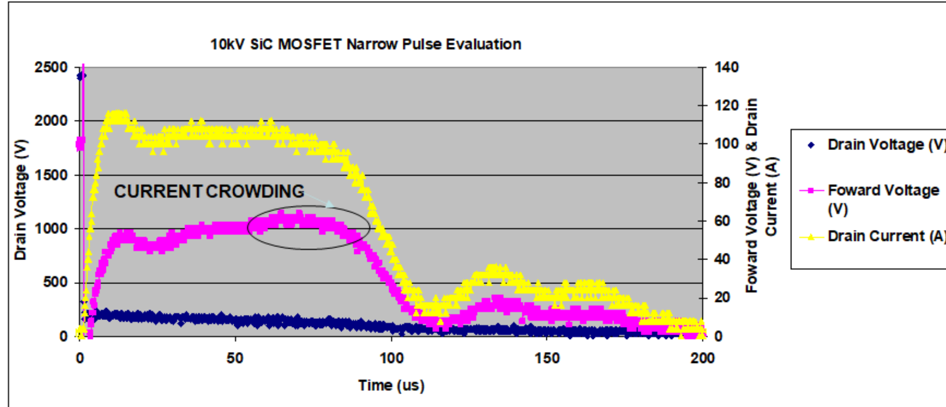

Fig. 12 Narrow pulse evaluation of 10-kV SiC MOSFET at 110 A. Primary axis: blue, drain voltage, and secondary axis: purple, on-state voltage; yellow, current

Table 2 High-voltage SiC MOSFET analysis at 110 A

Die Analysis:	
dI/dt 10-90: (A/µs)	15.714286
Current Base Width:(µs)	110
Max Instant Power: (W)	7000
Action: (A^2 *S)	0.9616
Energy: (J)	0.0499626

An HV SiC IGBT was successfully evaluated in the PFN circuit. A plot of the IGBT evaluated at 40 A along with the charge voltage and On-state voltage utilizing the clamped voltage probe is depicted in Fig. 13. The forward voltage of the IGBT was 20 V, and the charge voltage of the PFN to acquire the 40 A current was 1 kV. This HV IGBT was subsequently pulsed over 100 times at 40 A with no degradation in the forward voltage. Table 3 displays results of the die evaluation at 40 A; the SiC IGBT withstood a dI/dT of 7.1 A/µs with a transient peak power of 960 W and energy dissipation of 7 mJ.

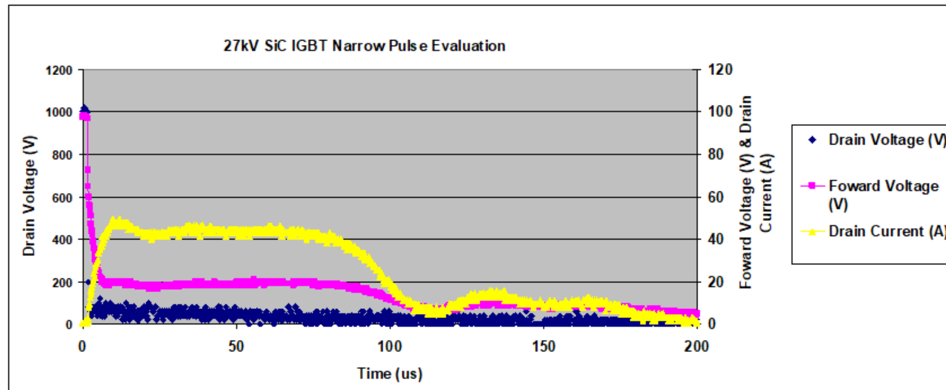

Fig. 13 Narrow pulse evaluation of 20-kV SiC IGBT at 40 A. Primary axis: blue, drain voltage, and secondary axis: purple, on-state voltage; yellow, current.

Table 3 High-voltage SiC IGBT analysis at 40 A

Die Analysis:	
dI/dt 10-90: (A/µs)	7.1428571
Current Base Width: (µs)	110
Max Instant Power: (W)	960
Action: (A^2 *S)	0.1690839
Energy: (J)	0.0076879

A charge voltage of 1.7 kV was used to evaluated IGBT with a collector current of 75 A. At this pulse current level, current crowding occurs in the device, as evidenced by the transient voltage spike at the initial stage of the current pulse (Fig. 14.).[6,7] Table 4 displays results of the die evaluation at 75 A; the SiC IGBT could handle a *dI/dT* of 11.7 A/µs with a transient peak power of 7000 W and energy dissipation of 27 mJ. This HV IGBT was subsequently pulsed over 100 times at 75 A with no noticeable alteration in the ON-state voltage measurement.

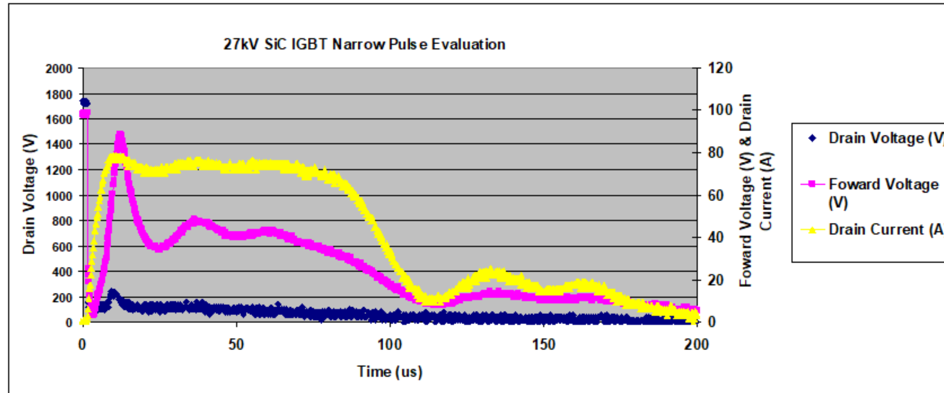

Fig. 14 Narrow pulse evaluation of 20-kV SiC IGBT at 75 A. Primary axis: blue, drain voltage, and secondary axis: purple, on-state voltage; yellow, current.

Table 4 High-voltage SiC IGBT analysis at 75 A

Die Analysis:	
dI/dt 10-90: (A/µs)	11.714286
Current Base Width: (µs)	110
Max Instant Power: (W)	7000
Action: (A^2 *S)	0.4766812
Energy: (J)	0.0275316

The maximum pulse current evaluation of the SiC IGBT was 84 A, shown in Fig. 15. It was decided to stop at this current pulse level due to the current crowding depicted in the forward voltage of the device and the clamped voltage probe limit of 100 V. Table 5 displays results of the die evaluation at 84 A; the SiC IGBT was

subjected to a *dI/dT* of 12 A/µs with a transient peak power of 8640 W and energy dissipation of 56 mJ.

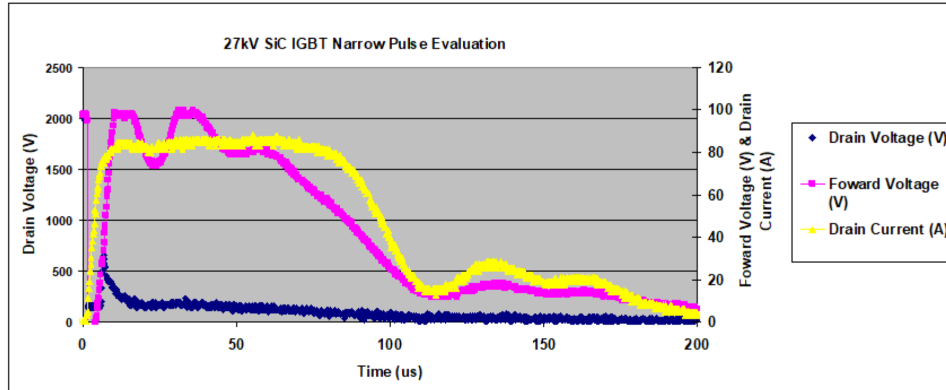

Fig. 15 Narrow pulse evaluation of 20-kV SiC IGBT at 84 A

Table 5 High-voltage SiC IGBT analysis at 84 A

Die Analysis:	
dI/dt 10-90: (A/µs)	12
Current Base Width: (µs)	110
Max Instant Power: (W)	8640
Action: (A^2 *S)	0.6243937
Energy: (J)	0.0564898

6. Conclusion

This research successfully demonstrated the pulse-power evaluation of a single-die HV SiC MOSFET and IGBT with thick drift regions up to 100 µm and beyond. Understanding the safe operation area for this HV MOSFET and IGBT design will enable projections for the pulse-current magnitude, switching frequency, and burst-mode operation anticipated for higher-voltage larger-area devices. Future plans include the fabrication of HV SiC MOSFETs and SiC IGBTs for high-power modules used in high-power dense operation, enabling the demonstration of next-generation SiC technology advances toward Army pulsed power, power conversion, and directed-energy system integration.

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List of Symbols, Abbreviations, and Acronym

C_{ds}	output interelectrode capacitance
D-mode	depletion mode
DUT	device under test
DMOS	double-diffused metal oxide semiconductor
HV	high voltage
IGBT	insulated gate bipolar transistor
I-V	current-voltage
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
PEEK	polyethertherketone
PFN	pulse-forming network
SiC	silicon carbide

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