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**HIGH SPEED DIGITAL-TO-ANALOG CONVERTERS
(DACs) FOR DIGITAL ARRAYS IN DIGITAL PROCESS
TECHNOLOGY**

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**NOVEMBER 2022
Final Report**

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| 14. ABSTRACT The design of high-speed digital-to-analog converters in nano-scale Complementary Metal-Oxide-Semiconductor Technology (CMOS) was investigated, specifically focusing on switched-capacitor-based realizations achieving high integration density. Prototype designs with 8 bits of resolution and update rates of 14, 28 and 56 giga samples per second were designed and fabricated in 16 nm CMOS and experimentally evaluated. The final design occupies an area of only 0.011 square millimeters, corresponding to an area reduction of over ten times relative to the state of the art. | | | | | |
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1 BACKGROUND AND SUMMARY OF SIGNIFICANT ACCOMPLISHMENTS

Digital-to-analog converters (DACs) are crucial building blocks in modern communication systems like wireline transceivers and digital mm-wave phased arrays. These applications drive steady increases in bandwidth, channel count, as well as integration density, which mandates data converters that are compatible with the latest Complementary Metal-Oxide Silicon (CMOS) technology. For analog-to-digital converters (ADCs), this has led to an architectural shift toward time-interleaved successive approximation, which exploits the strengths of modern CMOS while mitigating its weaknesses. On the other hand, DACs have not significantly changed since the 1970s and predominantly rely on the current steering topology.

This project investigated an alternative approach for high-speed (>10 giga samples per second), moderate resolution (6-8 bit) DACs, with the specific goals of reducing chip area and improving compatibility with the latest FinFET (Fin Field Effect Transistor) technology. The family of DACs developed in this program use a switched capacitor (SC) architecture that separates the functions of level generation, timing/combining, and output power delivery, which are lumped into a single node in a conventional current steering architecture. In the investigated design, levels are generated using time-interleaved SC DAC cores with sub-femtofarad unit capacitors, which offer sufficient linearity and noise performance at the 8-bit target resolution. The cores' outputs are combined and re-timed downstream and the final 50 Ohm load is driven by an inverter-based buffer.

To validate this new approach, we implemented a series of 8-bit prototypes in 16 nm FinFET CMOS, operating at 14, 28 (2x time-interleaved) and 56 (4x delta-interleaved) gigasamples per second, respectively. These designs show competitive power and linearity performance while occupying up to ten times less area than state of the art implementations.

1.1 Project Motivation

This project was carried out in the context of DARPA's Millimeter-Wave Digital Arrays (MIDAS) program, which aimed at pushing the frontiers of digital mm-wave transceiver technology by leveraging the integration density and speed of advanced CMOS process technology. Among the key challenges are the high-speed data converters that bridge the digital signal processing modules with the mm-wave transmit/receive circuitry. The system's analog-to-digital converters and digital-to-analog converters must fit within a small fraction of the tile area and operate at power levels that are well below the state of the art. While both types of converters are difficult to realize under the given constraints, the challenge is more pronounced for the DACs. Thus, the effort of this project was focused on an aggressive exploration on the fundamental limits of high-speed DACs in digital FinFET CMOS technology.

1.2 Phase 1 Design [2]

Phase 1 of this program was dedicated to designing a DAC prototype operating at 28 gigasamples per second using a 2x time-interleaved architecture (see Fig. 1). It has a single 0.8 V supply and supply-induced crosstalk is mitigated through on-chip de-coupling capacitors. A differential clock receiver provides onchip 50 Ohm termination and buffering to CMOS levels,

while a serial parallel-interface (SPI) programs the chip. A. on chip static random access memory (SRAM) stores the test pattern and is read with a 1 GHz clock. The 1 GHz data is multiplexed to 14 GHz by a custom 14:1 passing-token digital multiplexer. Two SC DACs are updated on complementary clock phases. The DACs analog outputs are combined and re-timed by a 2:1 analog multiplexer and an output driver that delivers power to 50 Ω double-terminated load.

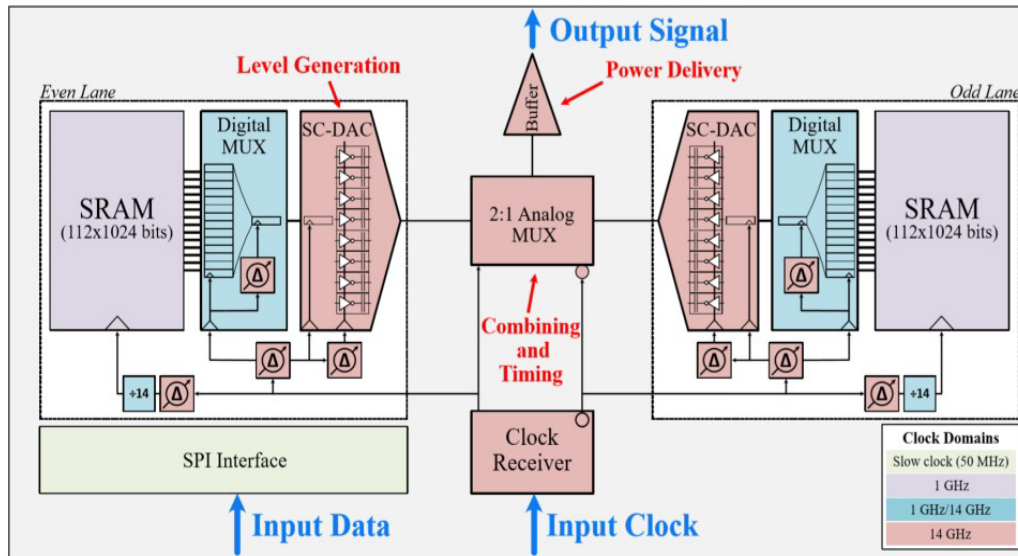


Fig. 1: 2X Time-Interleaved DAC Architecture

A half circuit of the binary-weighted 8-bit SC DAC core is shown in Fig. 2 (a). The actual implementation is pseudo differential. The SC-DAC core consists of 256-unit cells containing a custom 0.5 fF metal-oxidemetal (MOM) capacitor, an inverter-based latch and driver, and MOS attenuation capacitors [see Fig. 2(b)]. The attenuation factor is 1/8 to scale the DAC's rail-to-rail input voltage to a swing that is manageable by the succeeding buffer. The inverter-based latch re-times the data using the 14 GHz clock (CK) at the unit-cell level, resulting in glitch free level generation [see Fig. 2(c)]. Without this re-timing, the relatively large wiring skew (3-5 ps) in the binary input assertion (B7-0) would result in large output glitches and spectral spurs. In contrast, the re-timing clock skew is less than 200 fs for the worst-case transition (MSB B7 and LSBs B6-0). This is achieved using a wide trace of low-resistivity metal [Fig. 2(a) bold line], made feasible by the DAC's small footprint.

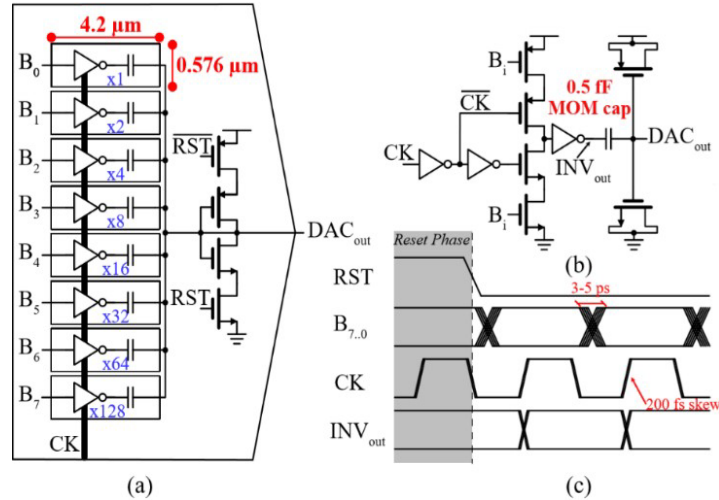


Fig. 2: DAC Building Blocks

Switched-capacitor core (a), (b) unit cell; (c) timing diagram.

The SC DAC is followed by a 2:1 analog multiplexer and output driver that provides power amplification and 50Ω output impedance matching [see Fig. 3(a)]. It is composed of two inverter-based stages with active peaking, providing a voltage gain of 2.5 and more than 20 GHz of on-chip bandwidth (post layout extraction, without package). Primary ESD protection is provided by the parasitic drain junctions of the output inverter. Secondary protection is achieved with diodes added between the second stage's peaking resistor and the inverter's gate oxide. The timing diagram of the analog multiplexer is shown in Fig. 3(b). Each DAC output is retimed by the CK clock into a common output, providing 2x time-interleaving while also avoiding the individual DAC transition periods where glitches could be still present. The analog multiplexer single-ended schematic is shown in Fig. 3(c) consisting of two complementary clocked inverter-based drivers and a common inverter-based diode-connected load. The actual implementation is pseudo-differential.

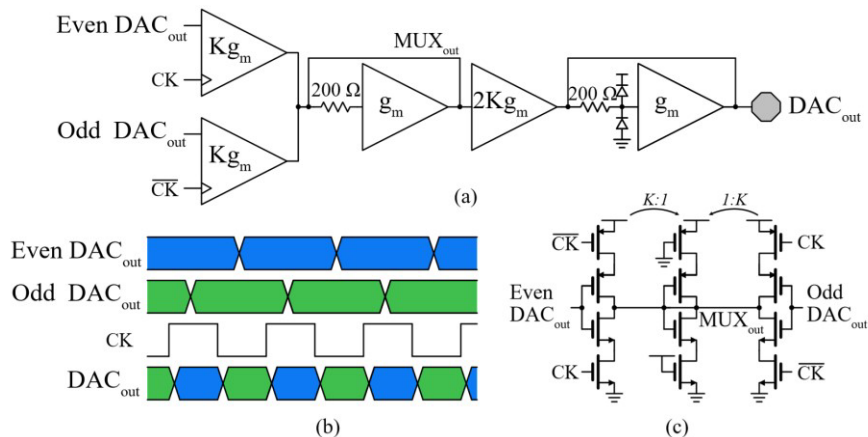


Fig. 3: Analog Multiplexer with Output Buffer

Block diagram (a); (b) timing diagram; (c) single-ended schematic of 2:1 analog multiplexer.

The proof-of-concept DAC was fabricated in 16 nm FinFET CMOS. Fig. 4 shows the die photo and layout. The total DAC area including the clock receiver, the 2:1 analog MUX and the output buffer is only 0.03 square millimeters. The 2.5 mm x 2.5 mm die is flip-chip bonded on a 1.5 cm x 1.5 cm ball-grid-array (BGA) package and surface mounted on a four-layer printed circuit board (PCB) fabricated on a 8 mil thick Rogers 4003 high-seed low-loss substrate. The total measured power consumption is 88 mW (digital MUX: 12 mW, SC DAC section: 24 mW, clock RX: 14 mW, 2:1 analog MUX and buffer: 8 mW) when operating at 28 GS/s update rate from a single 0.8 V supply.

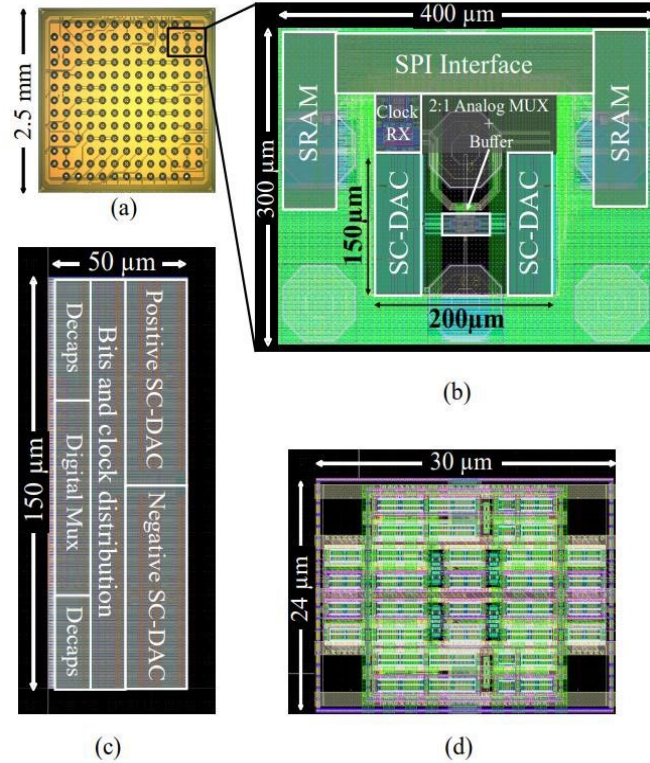


Fig. 4: Physical Implementation

16nm FinFET CMOS die micrograph (a); (b) layout of 2x timeinterleaved 28 GS/s DAC; (c) layout of SC-DAC core; (d) layout of 2:1 analog mux and driver.

The chip was measured with a differential input clock generated by an external balun (Marki Microwave BAL-0212) and a Rohde & Schwarz SMF100A signal generator. The results are summarized in Table I. The power dissipation of our design is on par with the state of the art, while its area is nearly three times smaller than comparable current steering implementations. Further details were documented in a journal publication [2] and a PhD thesis [4].

Table I. Phase 1 Performance Summary and Comparison with the State of the Art

| | Nazemi [5] ISSCC 2015 | Olieman [6] JSSC 2015 | Caragiulo [10] VLSI 2020 | Greshishchev [24] BCICTS 2019 | Zhou [25] ICECS 2016 | Duncan [26] JSSC 2017 | Kim [27] VLSI 2019 | This Work |
|--------------------------------|--------------------------|--------------------------|-----------------------------|----------------------------------|-------------------------|--------------------------|-----------------------|-----------|
| Resolution (bits) | 8 | 9 | 8 | 8 | 6 | 10 | 6 | 8 |
| f_{sample} (GS/s) | 18 | 11 | 14 | 60 | 30 | 3.35 | 28 | 28 |
| V_{supply} (V) | 1/1.5 | 1 | 0.8 | 0.9/1.9 | 3.3/4.5 | 1.5/3.5 | 1.1/1.6 | 0.8 |
| Area (mm ²) | 0.05 | 0.04 | 0.011 | 0.31 | 8.4 | 6.25 | 0.08 | 0.03 |
| Swing ($V_{\text{pp-diff}}$) | 0.8 | 0.425 | 0.32 | 0.8 | 0.75 | 0.63 | 0.2 | 0.32 |
| SFDR (dB) | 43 | 51 | 34 | 30 | 28.5 | 48 | 34.6 | 37 |
| IM3 (dBc) | N/A | -51 | -45.3 | N/A | N/A | -48 | N/A | -45.6 |
| Power (mW) | 84 | 110 | 50 | 560 | 6200 | 1910 | 103 | 88 |
| Technology (nm) | 28 | 28 FDSOI | 16 FinFET | 7 FinFET | 180 SiGe | 130 SiGe | 40 | 16 FinFET |
| Topology | CS | CS | SC | CS | CS | CS | CS | SC |
| Interleaving Factor | 1 | 2 | 1 | 2 | 2 | 1 | 4 | 2 |
| T/I calibration | N/A | Off-chip | N/A | N/A | On-chip | N/A | On-chip | Off-chip |

1.3 Phase 2 Design [3]

Phase 2 of this program was dedicated to pushing the DAC speed further (to 56 gigasamples per second) while also reducing the area more aggressively. The general design approach was kept similar to that of phase 1, but a “delta interleaving approach as used to enable the aggregation of throughput from four DAC cores (see Fig. 5).

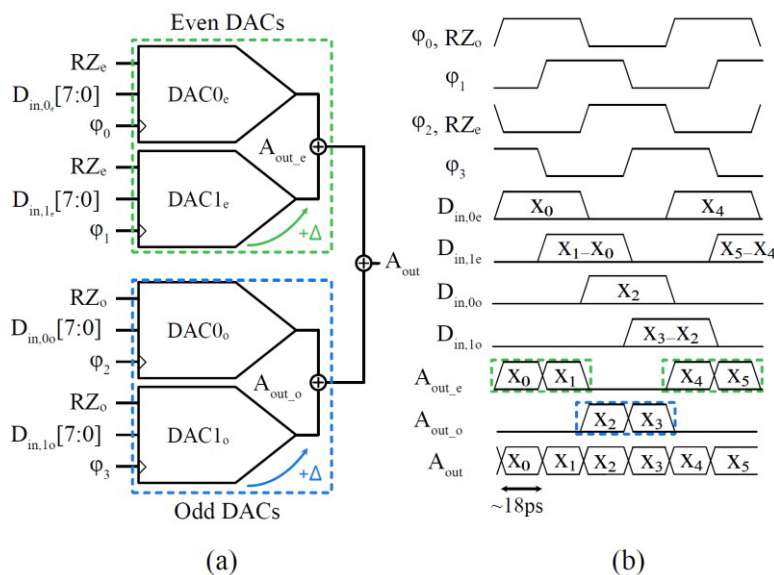


Fig. 5: Block Diagram (a) and (b) Timing Diagram of a Four-times Delta-Interleaved DAC

The converter is composed of four cores, each operating on one phase (of a quarter-rate quadrature clock to achieve an output update interval of about 18 ps. The cores’ outputs hierarchically combine in groups of two [indicated as even/odd in Fig. 5 (a)] and within each group, the output of DAC0 is directly proportional to the input code, while the output of DAC1 adds/subtracts the difference, between two consecutive codes. Each group’s output is returned to zero by asserting the signal RZ e/o and is finally combined to generate the DAC output at the aggregate update rate. Contrary to conventional timeinterleaving, delta interleaving does not require an analog multiplexer and hence does not translate the sub-DAC offsets into a time

varying sequence (no offset interleaving spurs). However, similar to a timeinterleaved DAC, timing nonidealities, such as skew and clock duty cycle mismatch, lead to spurs at the output. Nonetheless, for low signal frequencies, the timing spurs of a delta-interleaved DAC are smaller than in a time-interleaved DAC because two cores process the difference between consecutive samples.

The resulting proof-of-concept DAC was fabricated in 16 nm FinFET CMOS. Fig. 6 shows the die photo and floorplan. The DAC occupies only 0.011mm² excluding the fast memories (needed for testing only). The 1.3 mmx 1.3 mm bare die is directly attached to a four-layer FR4 printed circuit board. Supply, ground and interface control signals are wire-bonded, while the 14 GHz input quadrature clocks and the differential analog outputs are wafer probed using 40 GHz GSGSG 100 micrometer pitch probes. The quadrature input clocks are generated by an external balun (Marki Microwave QH-0440) and a Rohde & Schwarz SMF100A signal generator. The DAC output is measured using a Rohde & Schwarz FSW43 spectrum analyzer via a Marki Microwave BAL-0067 wideband balun.

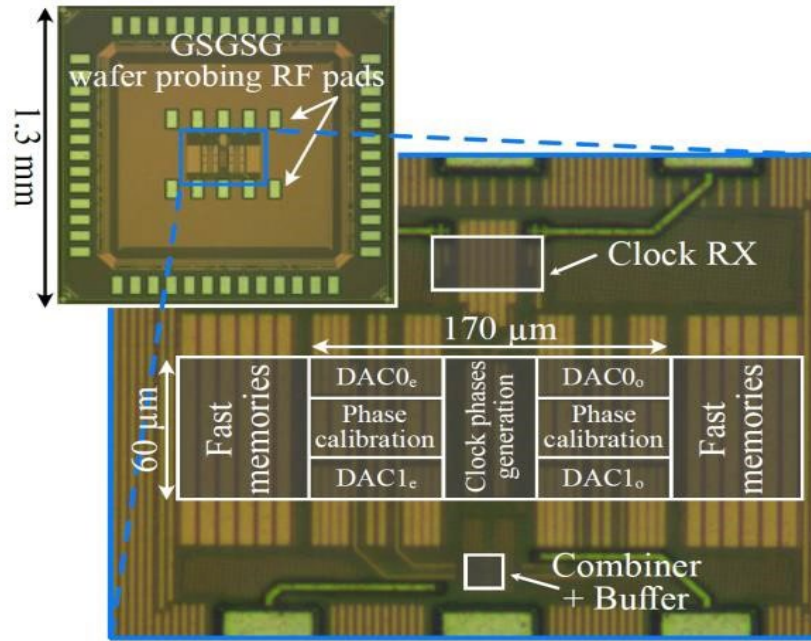


Fig. 6. Die Photo of Phase 2 Design

The results are summarized in Table II. The DAC described in this work is nearly 10 times smaller than its closest competitor while achieving similar spurious free dynamic range (SFDR) within 10 GHz output bandwidth. The power consumption is also competitive, while the output swing is smaller. The latter is partly due to our lower supply voltage and the design choices made in the combiner block. Depending on the application, other combiner architectures can be considered and in a system with heterogeneous integration, additional power gain may be achieved using a different transistor type (e.g., Gallium Nitride layer on top). Further details were documented in a conference publication [3] and a PhD thesis [4].

Table II. Phase 2 Performance Summary and Comparison with the State of the Art

| | Greshishchev [5] BCICTS 2019 | Menolfi [1] ISSCC 2018 | This Work |
|--------------------------------|---------------------------------|---------------------------|-----------|
| Resolution (bits) | 8 | 8 | 8 |
| f_{sample} (GS/s) | 60 | 56 | 56 |
| V_{supply} (V) | 0.9/1.9 | 0.95 | 0.85 |
| Area (mm^2) | 0.31 | 0.095 | 0.011 |
| Swing ($V_{\text{pp-diff}}$) | 0.8 | 0.92 | 0.27 |
| SFDR ≤ 10 GHz (dB) | 33 | 42 | 42 |
| IM3 (dBc) | N/A | N/A | -48 |
| Power (mW) | 560 | 286 | 280 |
| Technology (nm) | 7 FinFET | 14 FinFET | 16 FinFET |
| Topology | CS | SST | SC |
| Interleaving Factor | 2 | 4 | 4 |
| T/I calibration | N/A | On-chip | On-chip |

2 PUBLICATION LIST

- [1] P. Caragiulo, O.E. Mattia, A. Arbabian, and B. Murmann, "A Compact 14 GS/s 8-bit SwitchedCapacitor DAC in 16 nm FinFET CMOS," 2020 Symposium on VLSI Circuits, Jun. 2020, pp. 1-2. URL: <http://dx.doi.org/10.1109/VLSICircuits18222.2020.9162776>
- [2] P. Caragiulo, O.E. Mattia, A. Arbabian and B. Murmann, "A 2x Time-Interleaved 28-GS/s 8-Bit 0.03mm² Switched-Capacitor DAC in 16-nm FinFET CMOS," IEEE J. Solid-State Circuits, vol. 56, no. 8, pp. 2335-2346, Aug. 2021. URL: <http://dx.doi.org/10.1109/JSSC.2021.3057608>
- [3] P. Caragiulo, A. Ramkaj, A. Arbabian, and B. Murmann, "A 56 GS/s 8-bit 0.011 mm² 4x DeltaInterleaved Switched-Capacitor DAC in 16 nm FinFET CMOS," IEEE European Solid-State Circuits Conference, Milan, Italy, Sep. 2022, pp. 1-4 (to appear).
- [4] P. Caragiulo, "High-speed D/A conversion in FinFET CMOS technology," PhD Thesis, Stanford University, 2022. URL: <https://searchworks.stanford.edu/view/14229453>

LIST OF ABBREVIATIONS, ACRONYMS, AND SYMBOLS

| ACRONYM | DESCRIPTION |
|----------------|-----------------------------------|
| ADC | Analog-to-Digital Converters |
| BGA | Ball-Grid-Array |
| CMOS | Complementary Metal-Oxide Silicon |
| DACs | Digital-to-Analog Converters |
| MIDAS | Millimeter-Wave Digital Arrays |
| MOM | Metal-oxidemetal |
| PCB | Printed Circuit Board |
| SC | Switched Capacitor |
| SFDR | Spurious Free Dynamic Range |
| SPI | Serial Parallel-Interface |