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THESIS

COMMON MODE VOLTAGE ELIMINATION IN THREE-PHASE FOUR-LEG INVERTERS UTILIZING PULSE DENSITY MODULATION

by

Ethan B. Foster

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Thesis Advisor: Giovanna Oriti
Co-Advisors: Di Zhang
Alexander Julian,
Engineering Consultant, NPS (Retired)

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Common mode (CM) electromagnetic interference (EMI) is a phenomenon that negatively affects power electronics to include voltage source inverters. Typically, CM EMI reduction is achieved through passive measures such as CM chokes and passive filters. This thesis research explores removing the need for these passive devices in three-phase, four-leg grid-following inverters by eliminating CM EMI using pulse density modulation (PDM) in conjunction with model predictive control (MPC) and delta modulation.

A physics-based model of the equipment under test (EUT), utilizing state-space modeling, was analyzed using computer simulations and a laboratory prototype, utilizing SiC switching devices, was designed to validate the model. The physics-based model of the proposed control system was converted to Verilog, a hardware description language (HDL) utilizing MATLAB HDL coder in order to control the laboratory prototype via a field-programmable gate array (FPGA).

Simulated and experimental results demonstrate that both the unbalanced load requirements in MIL-STD-1399 and the conducted emission limits in MIL-STD-461G are met with the proposed controller, while the grid-following converter supplies a desired current to the load.

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COMMON MODE VOLTAGE ELIMINATION IN THREE-PHASE FOUR-LEG INVERTERS UTILIZING PULSE DENSITY MODULATION

Ethan B. Foster
Lieutenant, United States Navy
BS, University of Maine, 2014

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Approved by: Giovanna Oriti
Advisor

Di Zhang
Co-Advisor

Alexander Julian
Co-Advisor

Douglas J. Fouts
Chair, Department of Electrical and Computer Engineering

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List of Acronyms and Abbreviations

AC	Alternating Current
BESS	Battery Energy Storage System
CM	Common Mode
CMV	Common Mode Voltage
CORDIC	Coordinate Rotation Digital Computer
CSV	Comma-Separated Values
ΔM	Delta Modulation
DC	Direct Current
DM	Differential Mode
DOD	Department of Defense
DON	Department of Navy
EMI	Electromagnetic Interference
EUT	Equipment Under Test
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
IGBT	Insulated-Gate Bipolar Transistor
LISN	Line Impedance Stabilization Network
MIMO	Multiple Input Multiple Output
MPC	Model Predictive Control

NPS	Naval Postgraduate School
PC	Personal Computer
PDM	Pulse Density Modulation
PI	Proportional Integral
PID	Proportional Integral Derivative
Pmod	Peripheral Module Interface
PWM	Pulse Width Modulation
RAM	Random Access Memory
RMS	Root Mean Square
SISO	Single Input Single Output
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
USB	Universal Serial Bus
USN	U.S. Navy
VSI	Voltage Source Inverter
WBG	Wide Band Gap

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CHAPTER 1: INTRODUCTION

1.1 Research Motivation

The Department of Defense (DOD) along with the U.S. Navy (USN) have prioritized modernizing the U.S. fleet, focusing on improving its lethality and overall combat effectiveness. To this end, there has been a significant drive to shift ship and submarine electric distribution systems to Direct Current (DC) grids [1]. While modern Naval vessels are employing a primarily DC distribution system, most equipment including pumps, motors, and electrical equipment still operates on three-phase Alternating Current (AC) power.

In order to gain the benefits of a DC distribution system while still being able to employ ship equipment that utilizes three-phase AC power, the USN traditionally employs a Voltage Source Inverter (VSI) which directly converts ship DC power to the three-phase AC required by individual pieces of equipment. Shipboard power systems typically employ three-phase three-leg inverters for balanced loads, utilizing control schemes such as Space Vector Modulation (SVM) or Pulse Width Modulation (PWM) to accomplish the DC to AC conversion that meets the specifications of the MIL-STD-1399 for Type I power [2]. However, switching power converters introduce conducted and radiated Electromagnetic Interference (EMI) as unwanted side effects. Here the focus is on conducted EMI, with emphasis on Common Mode (CM) emissions, which cause circulating CM currents, ground-fault relay tripping, and accelerated motor bearing aging [3]. For this reason, all naval shipboard power applications must adhere to the guidelines and specifications delineated in the MIL-STD-461G [4].

1.2 Previous Research

Four-leg three-phase VSIs were proposed in [5] to eliminate the CM voltage produced at the output of the inverter by keeping two top switches and two bottom switches on at all times. The use of Model Predictive Control (MPC) and delta modulation to drive four-leg inverters to eliminate CM voltage has been studied and shown to be theoretically possible through the use of computer simulation [6] [7].

Additionally, research has shown in [7] that a continuous time, physics-based model in MATLAB/Simulink of a four-leg inverter employing MPC, delta modulation, and 3D space vector modulation meets the CE101 and CE102 EMI requirements of [4]. While the delta-modulated four-leg inverter model was experimentally validated in [7], the solution using MPC was only demonstrated in simulations [6] [7].

1.3 Research Goals

Typical three-phase VSIs, both in the Navy and in industry, produce CM voltages as an artifact of the power conversion process. As a result, all VSIs employ CM chokes to reduce spurious and unwanted CM currents and to meet the conducted emission limits specified in [4].

The goal of this thesis is to expand upon the work and simulations laid out in [6] and [7] by validating the removal of the large CM choke through MPC in a three-phase four-leg laboratory prototype.

Additionally, this thesis explores the use of MPC to eliminate CM voltage under unbalanced load conditions. Moreover, this thesis works to show that VSIs utilizing MPC can meet Type I power requirements of [2] and the conducted EMI requirements of [4].

1.4 Thesis Structure

This thesis is structured to highlight the results and support the reader in comprehending the motivation behind the research and enable the reader to reproduce the results. Chapter 2 lays the groundwork for the thesis, presents background information, and details the basics engineering concepts and military standards underpinning the research. Chapter 3 illustrates the design of the three-phase four-leg inverter utilized and introduces the physics-based model, including the control scheme, for the system. Chapter 4 depicts the hardware implementation of the physics-based model utilized to validate the model through experimentation and meet military standards. Chapter 5 presents the results for both the physics-based model and the hardware implementation. Chapter 6 concludes the thesis with the conclusion and future work. Following the formal chapters an appendix presents the MATLAB code utilized to produce both the physics-based model/results and post-process

the hardware results.

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CHAPTER 2: BACKGROUND

2.1 Four-Leg Three-Phase Inverters

The four-leg, three-phase inverter topology, seen in Figure 2.2 is an evolution of the three-leg, three-phase inverter topology depicted in Figure 2.1. A fourth leg is created with an additional set of switches that connect the two levels of the VSI to the neutral point of the original three-leg inverter, eliminating the floating neutral line [8]. The four-leg VSI was chosen over the three-leg inverter for this thesis due to a number of factors. First, the four-leg inverter, through the effective use of control and modulation strategy, can be operated in a manner that eliminates the output CM voltage. Equation (2.1) [9] states the definition of CM voltage for the four-leg inverter depicted in Figure 2.2, where S_a, S_b, S_c, S_d are the switching states for each leg and can be either 1 when the top switch is on, or 0 when the bottom switch is on. Choosing a modulation strategy which allows only two top switches on and two bottom switches on at all times, sets the sum of the four switching states equal 2, which in turns makes the CM voltage equal zero according to (2.1) [6], [10].

$$V_{cm} = \frac{V_g}{4}(S_a + S_b + S_c + S_d) - \frac{V_g}{2} \tag{2.1}$$

The use of Pulse Density Modulation (PDM) allows for the simultaneous switch selection on every clock cycle, allowing the switches to be switched in pairs of two, maintaining two switches on the top rail and two switches on the bottom rail at any given time [7], [11], [12] and cancelling the CM voltage. CM conducted EMI elimination using PDM is the focus of this thesis.

The four-leg inverter also isolates a given load from an external power grid, whereby unbalanced loading conditions and effects are not felt by the grid. This allows for the worst case unbalanced loading conditions while still meeting the EMI requirements set-fourth by the MIL-STD-461G [4], [12].

However, one drawback of the four-leg inverter is its increased power losses due to the additional switching losses produced by the addition of a fourth leg.

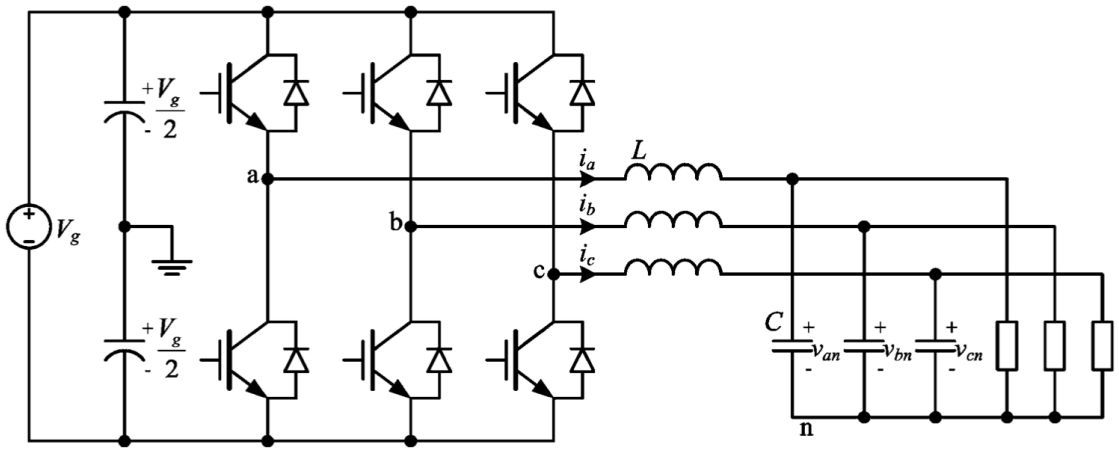


Figure 2.1. Three-leg, three-phase inverter topology. Source: [8]

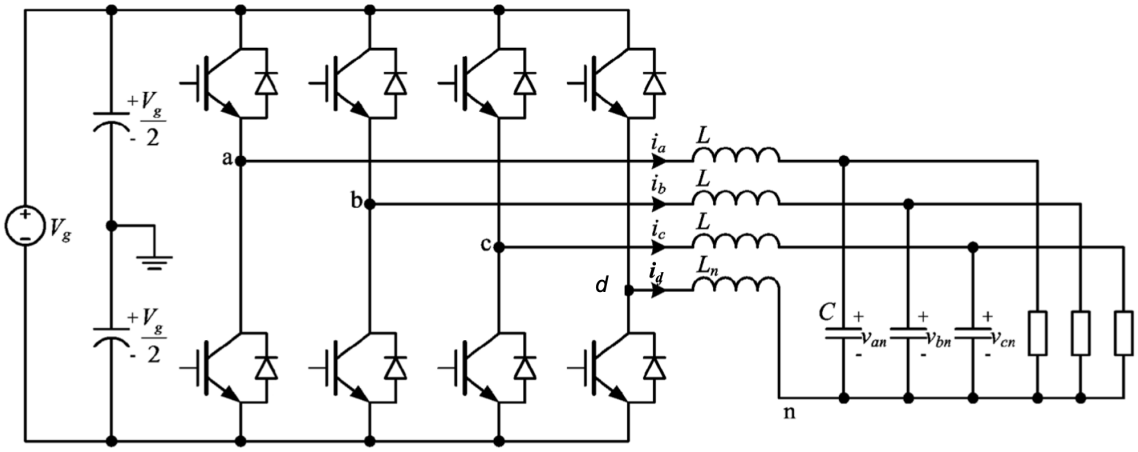


Figure 2.2. Four-leg, three-phase inverter topology. Source: [8]

2.2 Conducted EMI

Switching power converters produce EMI as a byproduct, which result in conducted and radiated emissions, both harmful to nearby electronic and communication devices [13]. Some of this damage can include bearing damage and terminal over-voltages in motors [14]

or other electrical interference and degradation. The focus of this thesis is to eliminate CM EMI via software control. Conducted EMI exist in two forms: differential mode noise and common mode noise.

These EMI emissions negatively effect and can damage various power electronic and motor drives, such as: operational amplifiers, electric motor drives, power inverters/converters. The focus of this thesis is on the damaging effects of EMI emissions on power converters. The Navy requires that all power electronics present aboard naval vessels adhere to the requirements codified in the military standard 461G [4].

2.3 Mitigating Common Mode

While power converters have always been susceptible to the presence of EMI emissions, such as CM, there are well documented methods of reducing the generated EMI to within limits acceptable for safe operation. The following methods are commonly employed to reduce CM emissions:

- Common mode chokes/passive filters [15]–[17]
- Common mode active filters [18]
- Reduce inverter switching frequency [19]
- Control and modulation strategy [6], [7], [9]

CM chokes are an effective and inexpensive way to mitigate, but not completely eliminate, CM EMI. CM chokes are constructed by winding two wires around a toroid ferrite core in such a manner that the magnetic field generated by the flowing current generates constructive magnetic fields and the generated impedance reduces the CM EMI. In practice these CM chokes are quite large and heavy due to their material construction.

The goal of this thesis is to demonstrate novel control methods including PDM and MPC to meet the conducted EMI limits in MIL-STD-461G [4] without the need of large passive CM filters. Specifically, the CM EMI at the switching frequency are completely eliminated, leaving only the EMI noise in the MHz range, which is easily suppressed with small passive filters.

2.4 MIL-STD-1399-300-1 Requirements

2.4.1 Type I, 60Hz Shipboard Power Requirements

The MIL-STD-1399-300B is "Electrical Power, Alternating Current." The DOD defines and standardizes all electrical connections on board US naval vessels, along with their associated designs and sailor run equipment. USN vessels rely heavily on AC machines and equipment, which are typically ungrounded. Ships power systems are typically three-phase, 440 V_{rms}, 60 Hz systems while general purpose receptacles and ships lighting operate three-phase, 115 V_{rms}, 60 Hz [2]. These general requirements fall under the definition of Type I power, as defined MIL-STD-1399-300B. Regardless of use, all ship-service power systems must meet the requirements delineated in reference [2]. This thesis focuses exclusively on Type I power, the limits of which are stated in Table 2.1.

Table 2.1. Characteristics of shipboard electrical power systems - Type I. Adapted from [4].

Frequency	
1. Nominal Frequency	60 Hz
2. Frequency Modulation	0.5 %
3. Frequency Tolerance	±3 % (Submarines: ±5 %)
4. Frequency Transient Tolerance	±4 %
5. Worst Case Frequency Steady-State and Transient Excursion	±5.5 %
6. Recovery Time from Item 4 or 5	2 seconds
Voltage	
7. Designation Nominal User Voltage	440, 115, 115/200 V_{rms}
8. Line-to-Line Voltage Unbalance	3 % (Submarines: 0.5 % for 440 V_{rms}; 1% 115 V_{rms})
9. Voltage Modulation	2 %
10. Average Line-to-Line Voltage from Nominal Tolerance	±5 %
11. Single Line-to-Line Voltage from Nominal Tolerance	±7 % (CVN 78 class: ±10 %)
12. Maximum Voltage Steady-State Departure	±8 % (CVN 78 class: ±10 %)
13. Voltage Transient Tolerance	±16 %
14. Worst Case Voltage Steady-State and Transient Excursion	±20 %
15. Recovery Time from Item 13 or 14	2 seconds
16. Voltage Spike $\pm PeakValue$	2.5 kV_p (440 $V_{rms}sys$) 1.0 kV_p (115 $V_{rms}sys$)
Waveform $(Voltage)$	
17. Maximum Total Harmonic Distortion (THD)	5 %
18. Maximum Single Harmonic	3 %
19. Maximum Deviation Factor	5 % (Submarines: 3 %)

Table 2.1 is adapted directly from DOD reference [2] and applies to all existing and novel electrical devices that are currently on board naval ships or who are pursing DOD approval to operate on board USN vessels. All control strategies, computer models, simulations, and physical devices must meet the specifications and standards defined in [2].

2.5 MIL-STD-461G Requirements

The military standard 461G is entitled "Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment" [4]. MIL-STD-461G codifies the requirements of EMI and establishes the testing requirements for the control of EMI emissions and susceptibility characteristics of equipment utilized by entities that fall subordinate to the DOD [4]. Electronic power converters, by nature of their operation, generate EMI and are thus subjected to the requirements presented in MIL-STD-461G. In this thesis conducted EMI is analyzed and the two requirements of concern are CE101 "Conducted Emissions, Audio Frequency Currents, Power Leads," and CE102 "Conducted Emissions, Radio Frequency Potentials, Power Leads [4].

2.5.1 CE101: Conducted Emissions, Audio Frequency Currents, Power Leads

Emission and susceptibility requirement CE101 covers conducted emissions, audio frequency currents, and power leads, and is applicable to naval submarines, surface ships, and navy aircraft power leads, both supply and return, that operated form 30 Hz to 10 kHz [4]. In this thesis the conducted EMI defined by CE101 are the spectra of the currents at the input of the inverter, which is the Equipment Under Test (EUT). Figure 2.3 depicts the limit that currents at the input of the EUT shall not exceed.

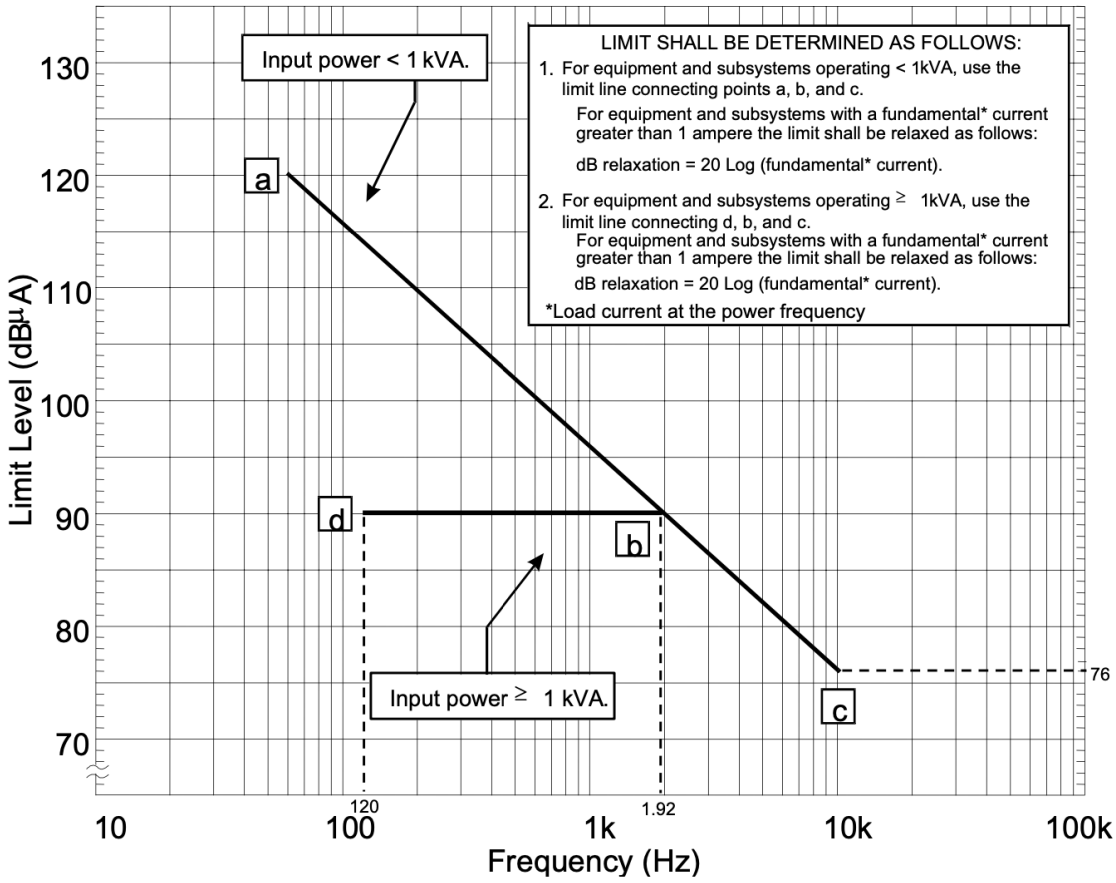


Figure 2.3. CE101 limit for surface ships and submarine applications, 60 Hz. Source: [4], Figure CE101-2.

2.5.2 CE102: Conducted Emissions, Radio Frequency Potentials, Power Leads

Emission and susceptibility requirement CE102 covers conducted emissions, radio frequency potential, and power leads, and is applicable to all power lead applications, both AC and DC, that operate from 10 kHz to 10 MHz [4]. The conducted EMI CE102 are the voltages measured at the Line Impedance Stabilization Networks (LISNs), which are passive networks inserted between the grid and the EUT as described in Chapter 3. Figure 2.4 depicts the limit that power lead conducted emissions shall not exceed. The nominal EUT source voltage utilized by the three-phase four-leg inverter in this thesis was type I

voltage 200 V line-to-line therefore the limit curve can be relaxed by 9 dB per Figure 2.4.

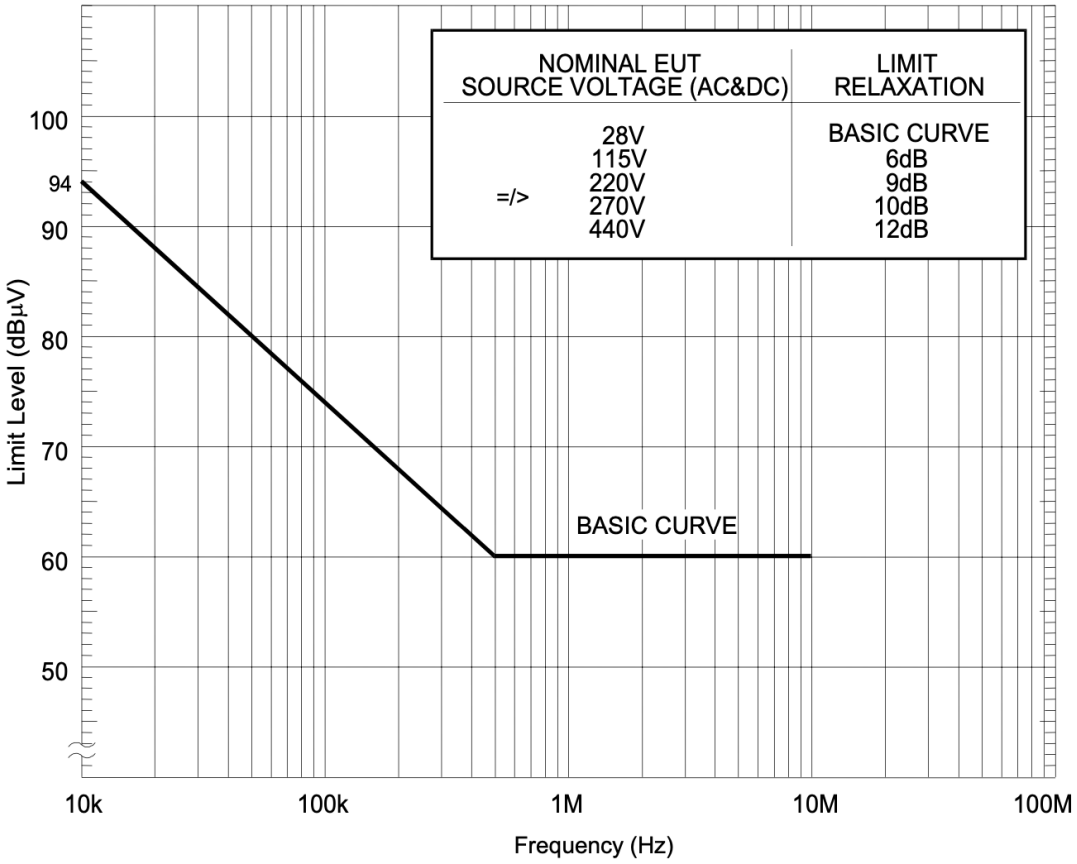


Figure 2.4. CE102 limit (EUT power leads, AC and DC) for all applications. Source: [4], Figure CE102-1.

CHAPTER 3:
ARCHITECTURE AND PHYSICS-BASED MODEL

3.1 Overview

The basic converter model and setup implemented in both the software simulations and in the hardware experiments is depicted in Figure 3.1. The model is constructed with three principle sections: the EUT consisting of the four-leg three-phase inverter and differential-mode filter, the LISNs, and the three-phase AC grid. The focus of this thesis is on the control strategy implemented to drive the four-phase four-leg inverter to eliminate unwanted CM voltage generated by the operation of the inverter. Without CM voltage, it will be demonstrated that the use of a traditional CM choke will not be necessary to meet the conducted EMI limits in [4]. The results are validated with simulations and through hardware implemented testing. The LISNs are placed between the inverter and the three phase AC power source as required by [4] to decouple the EUT from the AC power source so that EMI measurements capture only the conducted emissions of the EUT [4].

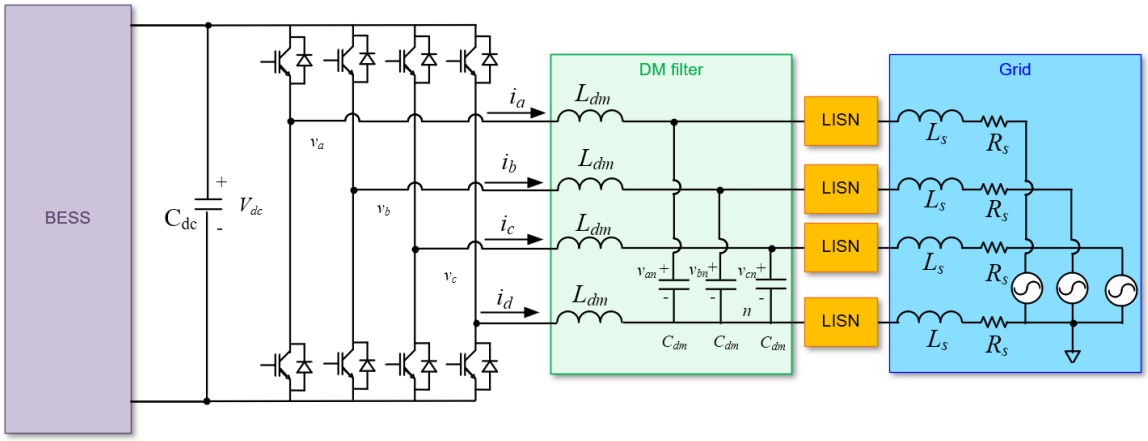


Figure 3.1. Grid connected four-wire four-leg inverter.

3.1.1 Battery Energy Storage System

A grid-following inverter can be connected on the three-phase shipboard power distribution system for various applications, one of them is interfacing an energy storage system, such as batteries. A Battery Energy Storage System (BESS) can act as a source or as a load depending on whether the battery pack is discharging or being charged from the grid, respectively.

3.1.2 Four-Leg Three-Phase Inverter

The four-leg three-phase inverter consists of a traditional three-phase inverter with a fourth leg added to the system, as described in chapter 2. In this thesis this topology is connected to the AC grid and is controlled as a current source, or in grid-following mode. One purpose of a four-leg, grid-following inverter, as seen in [7], is to isolate the AC power grid, which is acting as a source, from unbalanced load conditions which result in unbalanced currents. The inverter can also be used to interface batteries, DC loads or photovoltaic sources.

3.1.3 Differential Mode Filter

The second-order passive Differential Mode (DM) filter, consisting of an inductor and a capacitor per phase, is located between the LISNs/three-phase source and the four-leg three-phase inverter and provides reduction of unwanted DM EMI. As the focus of this thesis is on eliminating CM EMI, the DM emissions produced by the EUT are suppressed with this traditional filter in order to reduce overall measurement noise and to meet the conducted emissions limits in [4]. The DM filter inductance value and capacitance value, both simulated and experimentally validated, for L_{dm} and C_{dm} was 500 μF and 34 μH respectively.

3.1.4 Line Impedance Stabilization Networks (LISNs)

To meet the general testing requirements delineated by MIL-STD-461G [4], four LISNs, one for each of the four legs of the inverter interfacing with the AC grid, were installed between the AC power source and the inverter, as seen in Figure 3.1. Note, Figure 3.3 only shows 2 LISNs for a single phase AC or DC input, while this thesis required four, one for each power lead interfacing with the AC grid. The LISNs are required to set the AC power

source impedance and isolate the AC power source from the inverter, which is the EUT [4]. The LISNs are required by the Navy and [4] when measuring the conducted EMI of an EUT. A schematic of a LISN utilized in this thesis derived from [4] is depicted in Figure 3.2 along with the general test setup utilized for this thesis shown in Figure 3.3 [4].

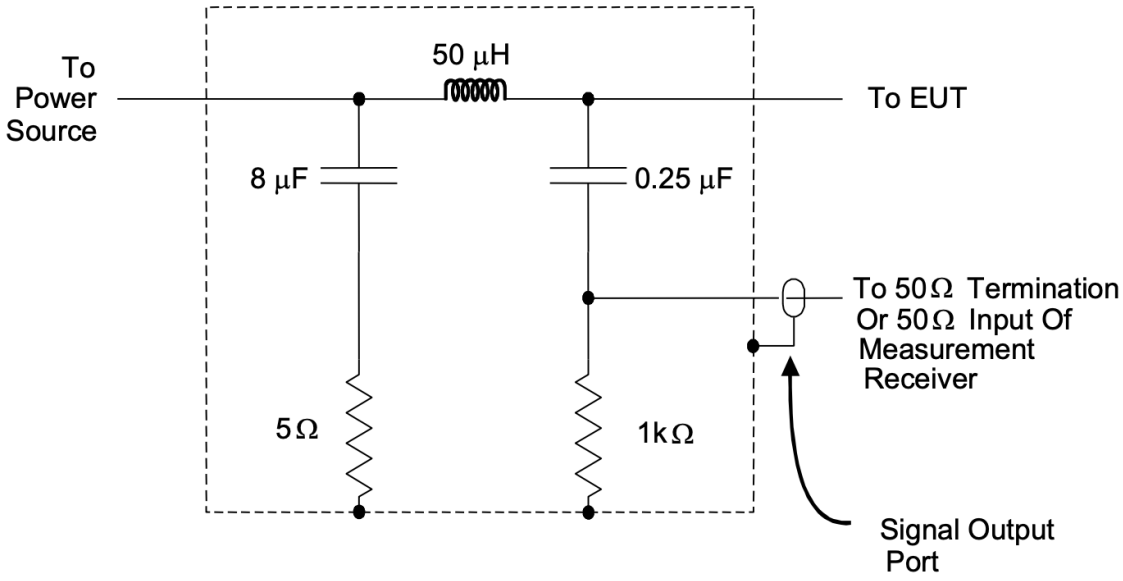


Figure 3.2. LISN schematic. Source: [4]

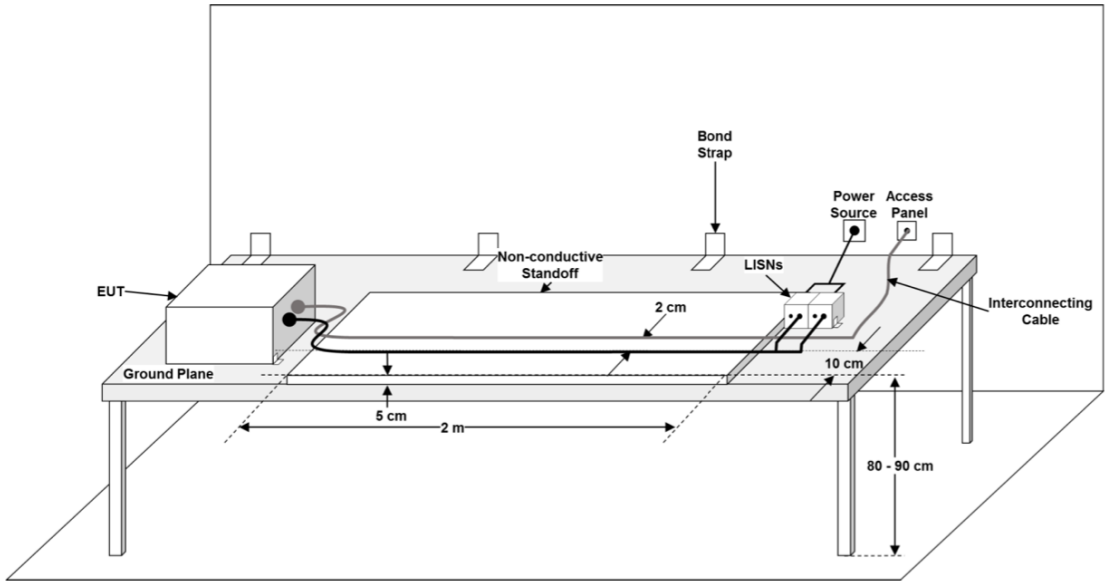


Figure 3.3. General test setup. Source: [4].

3.1.5 AC Grid

In this thesis, an AC source delivering type I power is used for all simulations and laboratory experiments. The four-leg three-phase inverter is connected to the AC grid and is controlled in grid-following mode, where its current is controlled in amplitude and phase in both directions. In the laboratory, the AC grid is obtained from the main grid with a variac. The three phases of the grid and a neutral line are connected to the four LISNs in series with an 500 μH source inductor, L_S, and 10 $m\Omega$ resistor, R_S. The series inductor L_S and resistor R_S depicted as part of the AC voltage source in Figure 3.1 are only present in the physics-based model simulated within MATLAB/Simulink. The hardware implementation built in the lab and discussed in Chapter 4 only has the variac separating the grid and the LISNs.

3.2 Controller Schemes To Eliminate the CM Voltage

The addition of a fourth leg to the standard two-level three-phase inverter topology creates the opportunity to eliminate the CM voltage at the output of the inverter by keeping two top switches on and two bottom switches on at all times. Although many control and modulations strategies have been proposed since the four-leg inverter was introduced in [5] to cancel the CM voltage, this thesis focuses on MPC and Delta Modulation (ΔM) [12]. Since PDM is used with MPC, and ΔM is a form of PDM, the first section introduces PDM.

3.2.1 Pulse Density Modulation

VSIs operate on the principle of controlled switch states. Each switch on the inverter is controlled electronically, through software, and is placed in one of two states. State one: "ON," meaning the switch is shut, voltage is equalized across the switch and current flows through the device. State two: "OFF," the switch is open, there is a voltage difference across the switch and there is no path for current to flow. The manner in which the switch states are selected to achieve a given output voltage is known as inverter modulation.

Some inverter modulation strategies include: PWM, 3D-SVM, SVM, and PDM. Each modulation scheme has its benefits and limitations depending on the power electronics used for switches and inverter application. For the purpose of this thesis, the novel PDM strategy presented in [7] was employed and expanded upon. PDM uniquely allows for multiple inverter switches to be operated simultaneously at any given clock cycle due to its random

pulse train and variable switching frequency, a benefit over the fixed switching frequency of PWM. With variable switching frequency, PDM and MPC are implemented such that there are always only two switches on the top rail and two switches on the bottom rail conducting at any given time. This switch selection drives the CM voltage, generated via Equation 2.1, to zero through software alone. PWM could not have been utilized to effectively eliminate CM EMI due to its fixed switching frequency, which would not facilitate the adaptive and simultaneous switching of two sets of switches provided by PDM.

3.2.2 Model Predictive Control

MPC is a well-researched and understood control algorithm employed in modern, state-of-the-art control systems and it has been widely applied to power converters [20]. MPC takes advantage of the Multiple Input Multiple Output (MIMO) concept where other Proportional Integral Derivative (PID) controllers operate within a Single Input Single Output (SISO) framework. The goal of a traditional MPC scheme is to optimize a cost function while meeting constraints imposed on the controller as seen in [6]. For the purposes of this experiment, a novel MPC strategy for eliminating CM voltage is used, as proposed in [7], where a cost function assessment is not required due to the fact that only a single inverter switch state per tetrahedron is evaluated. The process, including Figure 3.4, lays out the MPC algorithm utilized in this thesis.

First, the four inverter leg currents and the three phase voltages are measured, converted from analog to digital and then fed into the Field Programmable Gate Array (FPGA) where a set of three reference voltages in the a-b-c reference frame is generated utilizing (3.1) along with the DM filter inductance [7]. Once a set of three-phase reference voltages is obtained in the a-b-c reference frame, they are converted into three-phase reference voltages in the α-β-γ reference frame utilizing (3.2) [7], [9], [21]. With the reference voltages converted to the α-β-γ reference frame, a hexagon can be superimposed over the reference frame. The hexagon, depicted in Figure 3.5, includes the bases of six prisms, each prism's base covers 60 degrees of the hexagon. The prism in which the reference voltage vector resides in the α-β-γ is determined based on the angle between α and β, also known as θ^{ref}. For continuous time simulations, the arc tangent 2 function was used to calculate the angle between the α and β vectors directly: $\theta^{ref} = arctan2(\frac{V^r_\beta(k)}{V^r_\alpha(k)})$ [9]. For fixed-point applications the novel process presented in 3.3.2 was utilized. Once the appropriate method for determining

the reference angle was implemented, the appropriate tetrahedron was selected based on the prism determination and the a-b-c reference voltage polarities utilizing Table 3.1 for continuous modeling or Figure 3.17 for fixed-point implementation. From the tetrahedron determination the four inverter leg switch states are set to either open or shut. Because the switches are operated in pairs, two high and two low at all times, the CM voltage is effectively eliminated and the use and minimization of a cost function is not required [7].

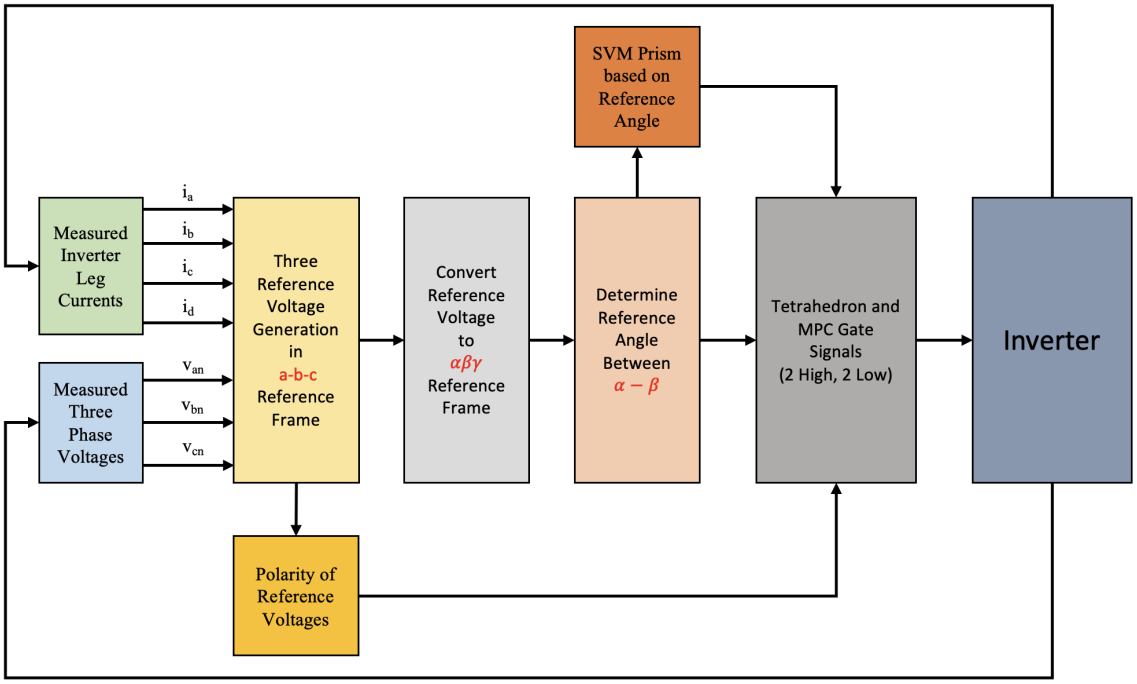


Figure 3.4. MPC block diagram. Adapted from: [6], [7], [9], [21].

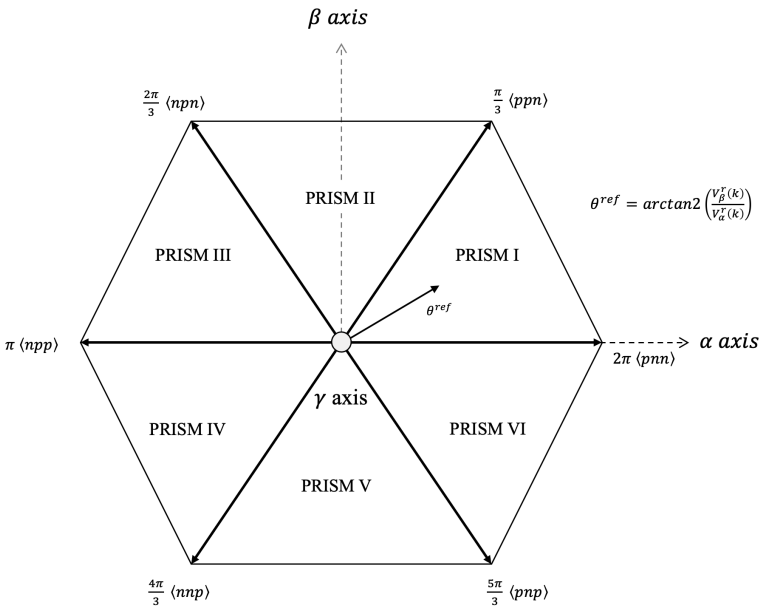


Figure 3.5. Inverter reference angle and prism selection. Adapted from: [6], [9], [12], [21].

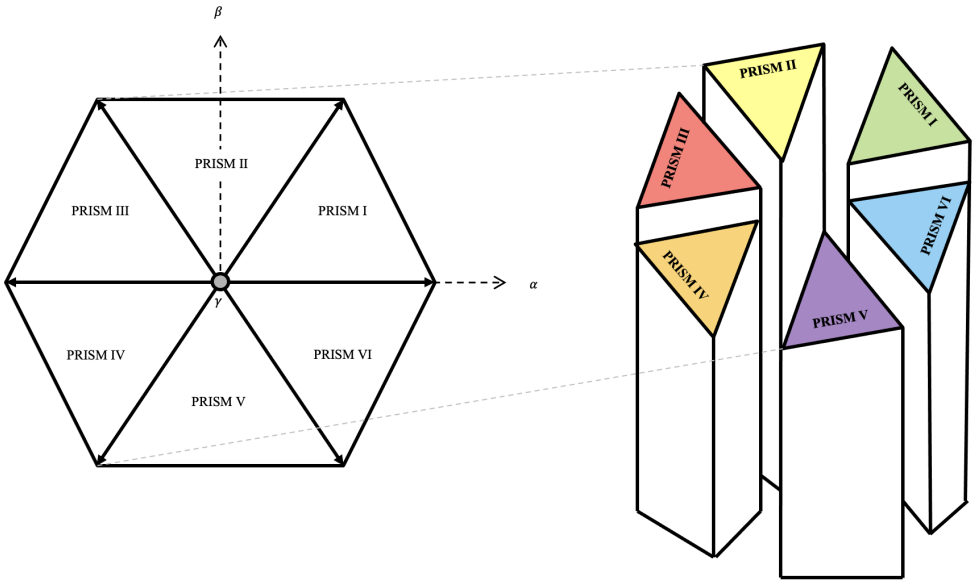


Figure 3.6. Inverter prism top and side view. Adapted from: [6], [7], [9], [21]

3.2.3 Delta Modulation

ΔM is a modified form of PDM and is used in this thesis as the second control strategy to eliminate CM voltage at the output of the inverter. ΔM works on a difference current error, as seen in Figure 3.7, where the four errors are the inputs to a switch selection algorithm which sorts them from the largest to the smallest as described in detail in [7] . The same principle of PDM applies to accomplish the elimination of the CM voltage, where two top rail switches and two bottom rail switches are operated simultaneously, effectively eliminating CM EMI at the converter switching frequency. The two switches chosen to updates are chosen through error comparison, where taking the largest two current errors determine which switches are updated [12].

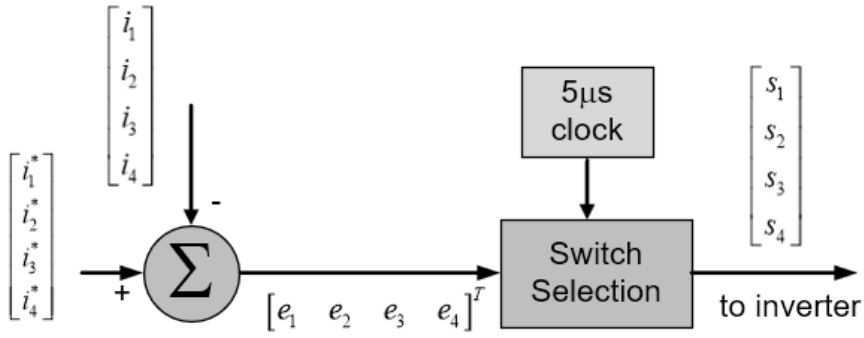


Figure 3.7. Basic ΔM control block diagram. Source: [7].

3.3 Physics-Based Model

A physics-based model of the system, using state space equations and running in continuous time, is presented in [12] for a grid-forming inverter. In [7] that model was adapted to a grid-following converter and is used in this thesis. The model was implemented in Simulink/MATLAB to simulate the system in continuous time and predict its behavior. A second, adapted and modified version of the physics-based model was required to be built utilizing fixed-point math and Simulink blocks so that the Hardware Description Language (HDL)-coder software [22] provided within MATLAB could be used to generate the equivalent Verilog code and, in turn, program an FPGA which was then used to control the

laboratory prototype. The two individual methods are described in 3.3.1 and 3.3.2.

3.3.1 Continuous Time Model

This thesis focuses on the control system to eliminate the CM voltage on a grid-following converter. The Simulink block diagram of the control system is shown in Figure 3.8 and it includes the MPC algorithm to control inverter currents and PDM to send gate signals to the switching devices. The Simulink model solves for all parameters continuously.

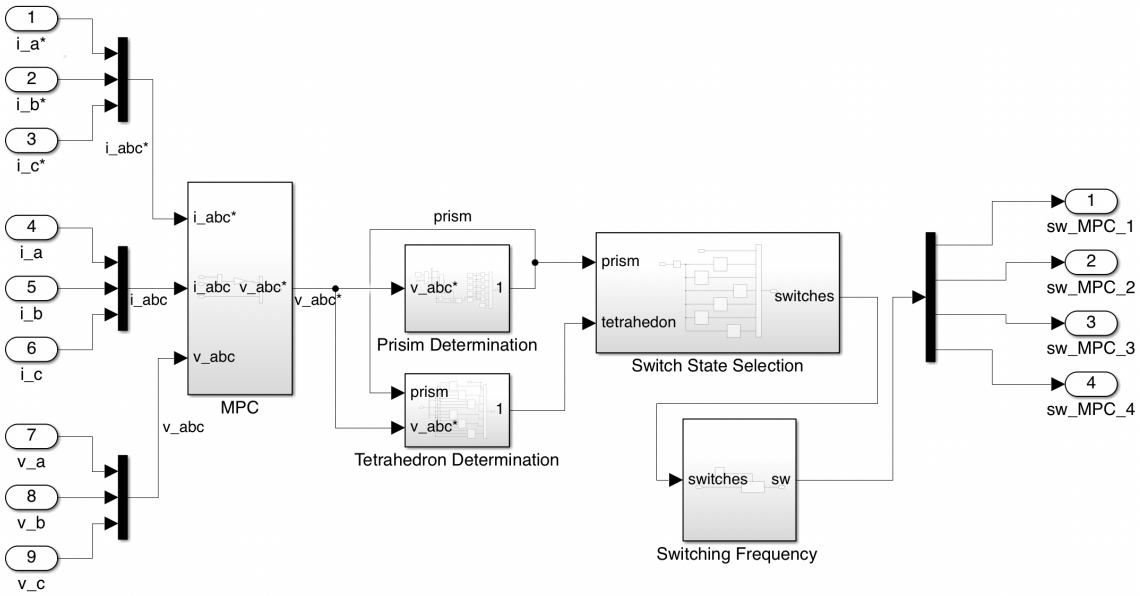


Figure 3.8. MPC continuous time Simulink control schematic.

As Figure 3.8 shows, the three-phase reference currents together with the measured voltages and currents are fed into the MPC block detailed in Figure 3.9 where a set of three-phase reference voltages is derived utilizing Equation (3.1) [6]. These reference voltages are used to determine the prism and the tetrahedron; two fundamental elements of the MPC scheme as seen in Figure 3.8 and described in section 3.2.2. In other words, by identifying in which prism and tetrahedron the reference voltage vector is located, the CM elimination algorithm determines the appropriate gate drive signals.

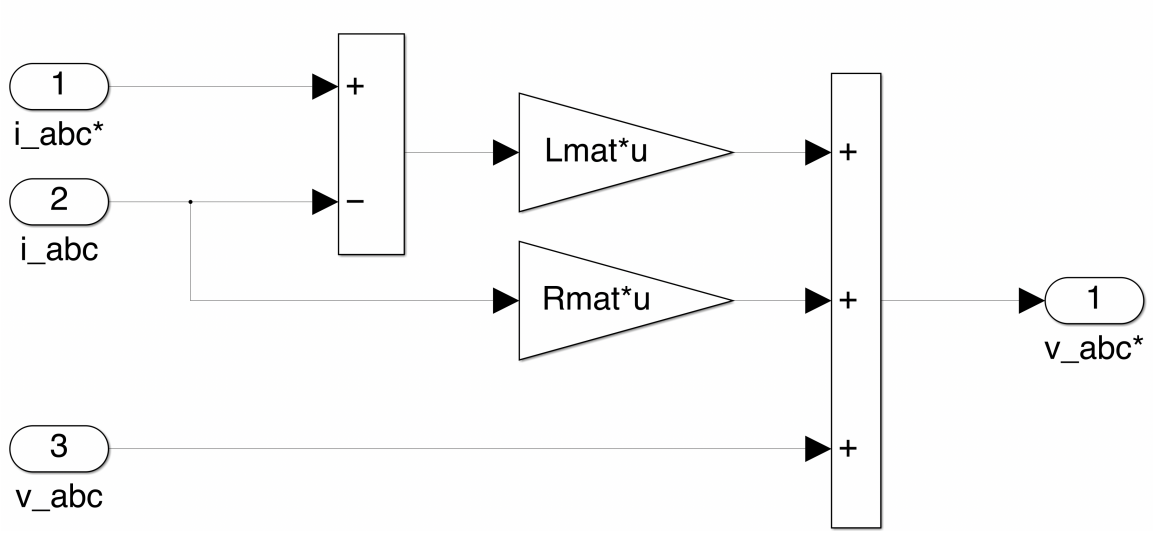


Figure 3.9. MPC continuous Simulink block.

$$\begin{bmatrix} V_{an}^{r}(k) \\ V_{bn}^{r}(k) \\ V_{cn}^{r}(k) \end{bmatrix} = \begin{bmatrix} \frac{L_{fa}}{T_s} & 0 & 0 \\ 0 & \frac{L_{fb}}{T_s} & 0 \\ 0 & 0 & \frac{L_{fc}}{T_s} \end{bmatrix} \begin{bmatrix} i_a^r(k+1) - i_a(k) \\ i_b^r(k+1) - i_b(k) \\ i_c^r(k+1) - i_c(k) \end{bmatrix} + \begin{bmatrix} R_{Ta} & 0 & 0 \\ 0 & R_{Tb} & 0 \\ 0 & 0 & R_{Tc} \end{bmatrix} \begin{bmatrix} i_a(k) \\ i_b(k) \\ i_c(k) \end{bmatrix} \tag{3.1}$$

In the block "Prism Determination", detailed in Figure 3.10, the three-phase reference voltages are converted from the a-b-c reference frame to the α-β-γ reference frame utilizing Equation (3.2) [6], [21]. Once the reference voltages are transformed into the α-β-γ reference frame, the controlling vector's angle is determined by computing the arc tangent 2 of the α and β components of the reference voltage. In the continuous time model the arc tangent 2 function is evaluated continuously unitizing the atan2 function block available in Simulink tool of MATLAB [23]. With the reference control angle between α and β computed explicitly, the appropriate 60°control prism, seen in Figure 3.10, is determined [6], [7].

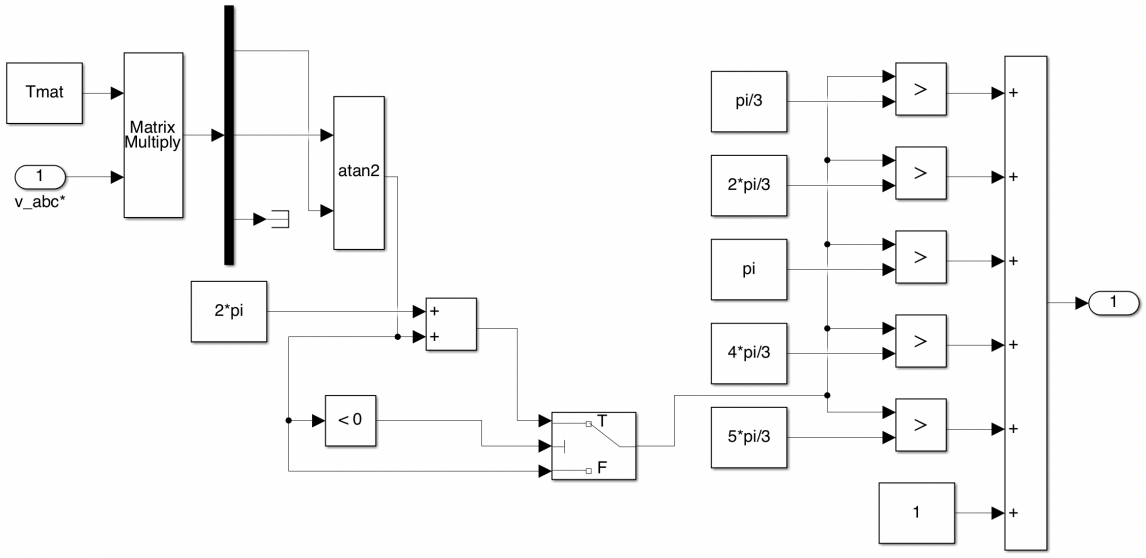


Figure 3.10. Continuous time prism determination.

$$\begin{bmatrix} V_\alpha^r(k) \\ V_\beta^r(k) \\ V_\gamma^r(k) \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_{an}^r(k) \\ V_{bn}^r(k) \\ V_{cn}^r(k) \end{bmatrix} \tag{3.2}$$

The "Tetrahedron Determination" block uses the reference voltages calculated with Equation (3.1) and the prism determination shown in Figure 3.10 to evaluate the reference voltage polarities as seen in Figure 3.11 and Figure 3.12. The polarities of the reference voltages in the *a-b-c* reference frame are used to select the VSI switch states depicted in Figure 3.13 and Figure 3.14. The assigned switch states are continuously passed to the output of the Simulink controller, seen in Figure 3.8, and the MPC controller drives the VSI to maintain zero CM voltage.

Reference [6] presents an exhaustive list of all possible switch states the VSI can assume, given all possible tetrahedron and reference voltage polarity states. While insightful, the switch states that do not result in zero CM are both computationally unnecessary and do not prove useful in eliminating CM EMI. Table 3.1, adapted from [6], [12], presents all possible switch state combinations determined in Figure 3.13.

The determined switch state is passed to the VSI, and the switches are updated at 200 kHz, maintaining two switches high and two switches low at all times, eliminating unwanted CM voltage.

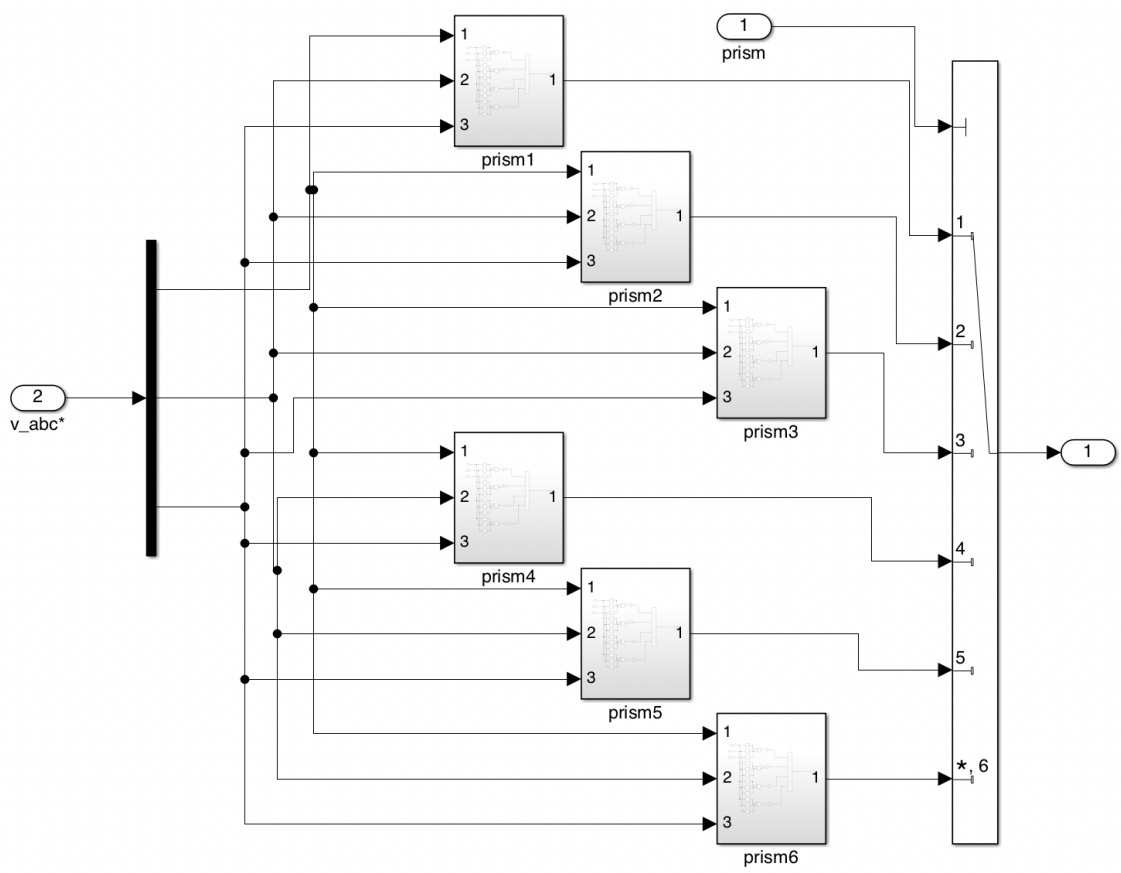


Figure 3.11. Continuous time tetrahedron determination.

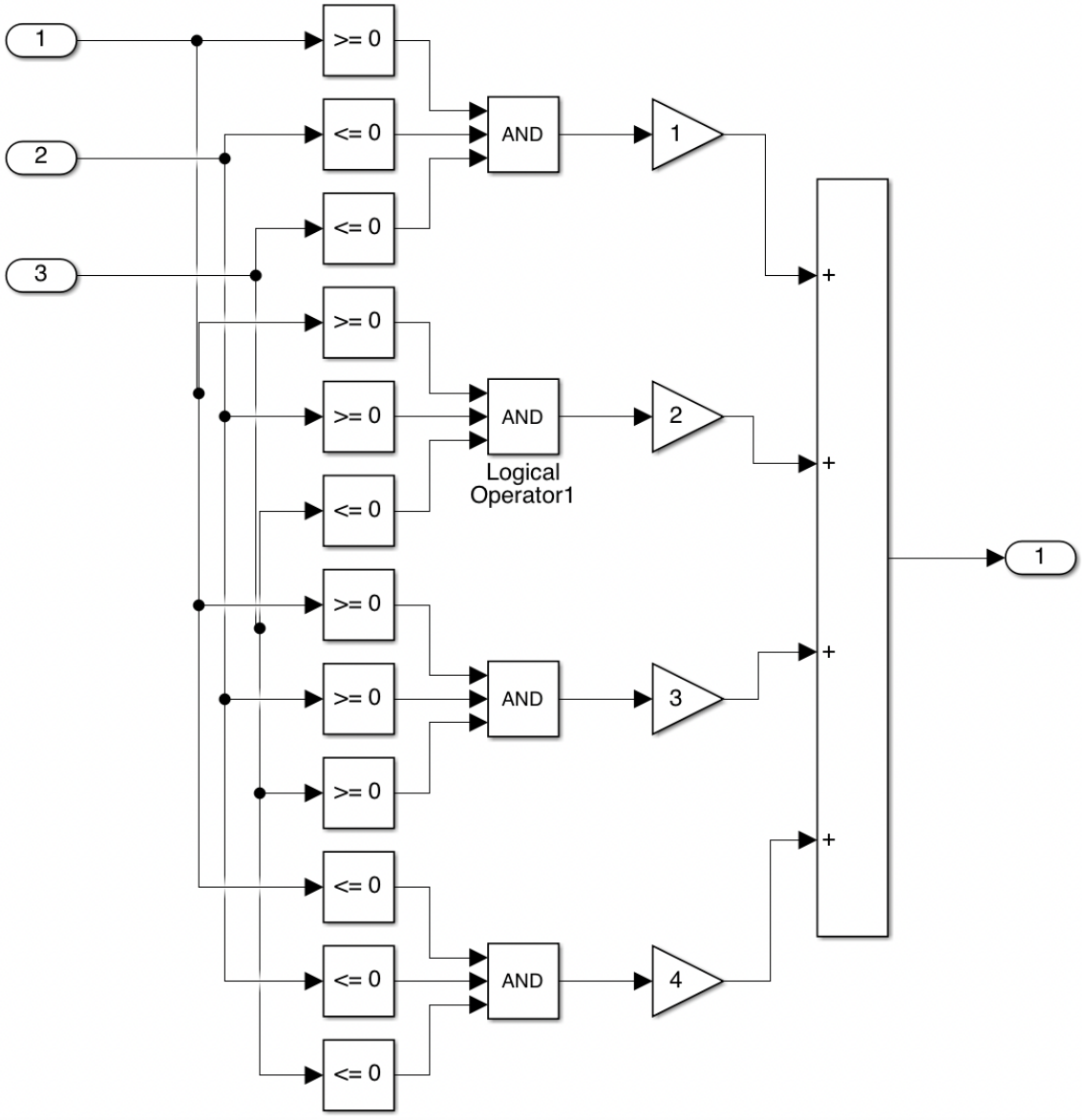


Figure 3.12. Example reference voltage polarity determination for prism 1.

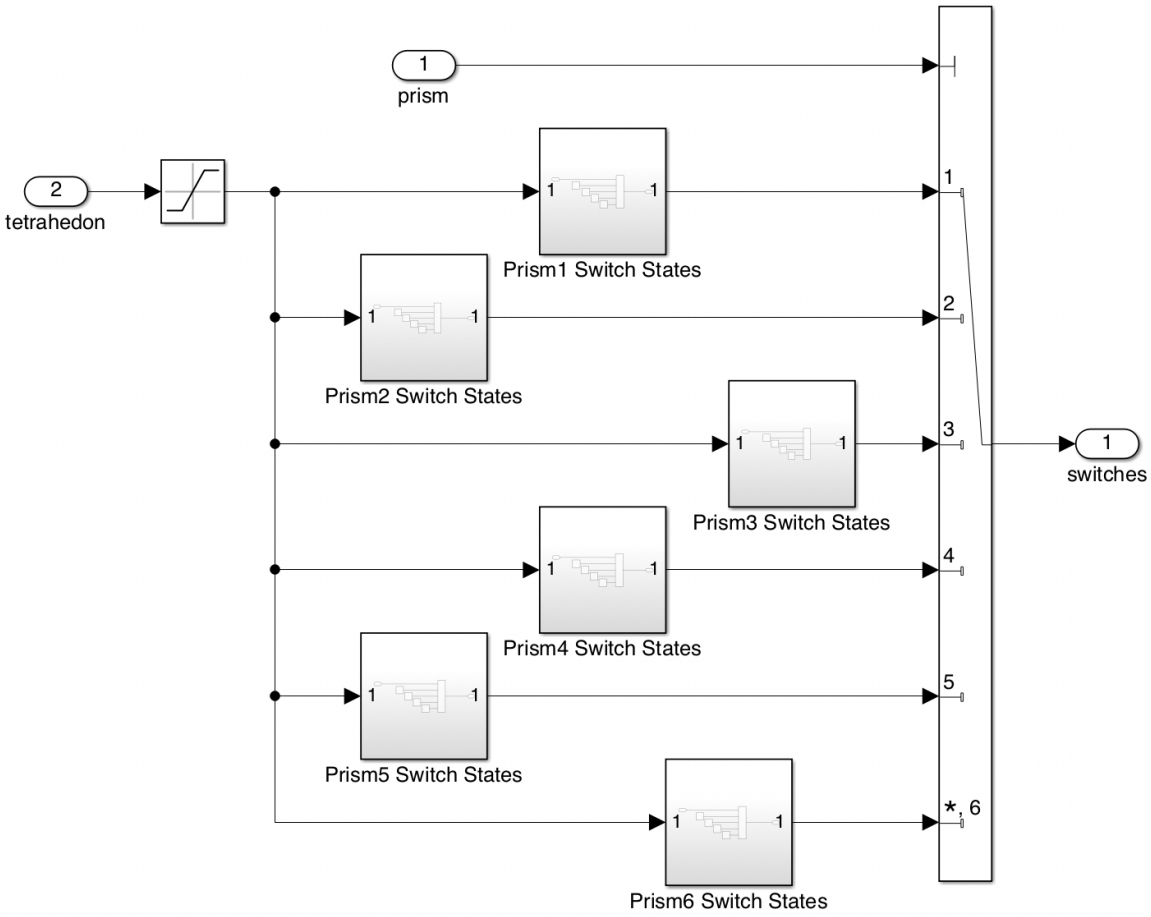


Figure 3.13. Switch state, tetrahedron and prism correlation.

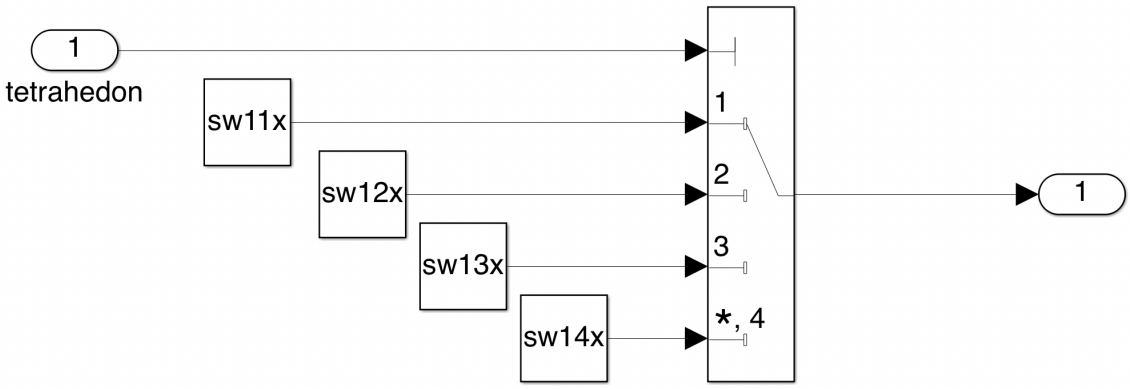


Figure 3.14. Example switch state assignment.

Table 3.1. MPC switch state selection. Adapted from [6], [12].

Prism	Tetrahedron	Reference Voltage Polarity	Switch States
1	1	+ - -	1001
	2	+ + -	1100
	3	+ + +	1100
	4	- - -	1001
2	1	+ + -	1100
	2	- + -	0101
	3	+ + +	1100
	4	- - -	0101
3	1	- + -	0101
	2	- - +	0110
	3	+ + +	0110
	4	- - -	0101
4	1	- + +	0110
	2	- - +	0011
	3	+ + +	0110
	4	- - -	0011
5	1	- - +	0011
	2	+ - +	1010
	3	+ + +	1010
	4	- - -	0011
6	1	+ - +	1010
	2	+ - -	1001
	3	+ + +	1010
	4	- - -	1001

3.3.2 Fixed-Point Model with Novel Arc Tangent 2 Algorithm

In order to experimentally validate the simulated results generated by the continuous physics-based model running in MATLAB/Simulink, the Simulink code for the MPC and PDM was modified to be compatible with the HDL-coder software [22], which generates the code that can be loaded on an FPGA. A Xilinx FPGA, as described in chapter 4, was selected to control the four-leg three-phase inverter laboratory prototype.

Figure 3.15 depicts the Simulink model of the controller, which was converted to operate in a fully fixed-point environment. The reference currents and the currents and voltages measured in the hardware and converted by analog to digital (A/D) converters, are sent into converter blocks which convert the variables from double-precision to fixed-point precision [23]. The MPC functionality described in Section 3.3.1, utilizing the continuous model, is performed by the device under test (DUT) block in Figure 3.15. The model was completely reconstructed utilizing fixed-point and HDL coder block architecture. Although the HDL coder block catalog in MATLAB [23] is fairly exhaustive, in converting the continuous MPC software to a fixed-point architecture capable of operating in and fitting within the memory of an FPGA, some key adjustments were made as follows.

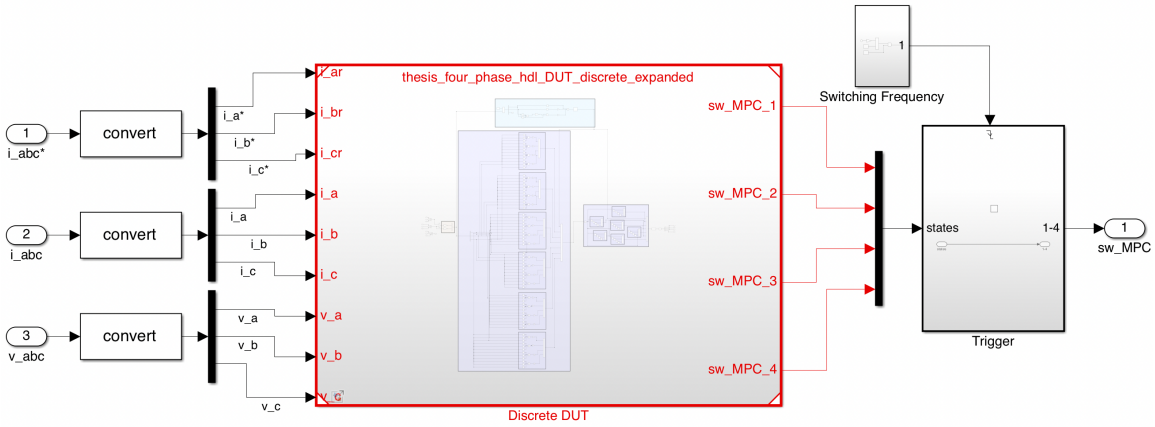


Figure 3.15. MPC fixed-point Simulink control schematic.

Implementing MPC in continuous time, as discussed in Section 3.3.1, requires the arc tangent 2 function to continuously determine the angle between the α and β reference voltage vectors explicitly within the α-β-γ reference frame. In Simulink [23], the arc

tangent 2 function is performed by the atan2 function block. Simulating the fixed-point MPC controller code in Simulink, utilizing the atan2 function block, presents no issue. However, when converting the MPC controller code to Verilog via the MATLAB HDL coder, the atan2 function becomes a computational burden and introduces unnecessary code complexity and file size. To solve this issue, an alternative solution is proposed. However, the angle between α-β only needs to be accurate enough to determine in which of the six prisms the reference voltage vector resides, as seen in [6], [21]. Therefore, the atan2 function can be removed from the Simulink model and replaced by a simple comparison and lookup table which meet the needs of the proposed CM elimination algorithm.

Figure 3.16 and Figure 3.17 present the novel approach to mathematically determining the reference voltage vector angle between the α-β reference voltages and deriving the prism selection of the MPC switch selection, as shown in sections 3.2.1 and 3.3.1. This is completed while maintaining the same functionality of the atan2 function block in MATLAB which the continuous time simulation in section 3.3.1 utilized to find the reference voltage vector angle. The two competing methods to replace the atan2 function with a fixed-point compatible alternative are: the utilization of a simple comparison and exhaustive lookup table and the computationally iterative Coordinate Rotation Digital Computer (CORDIC) algorithm of convergence. Both of these methods require added complexity to the fixed-point Simulink design, such as the use of integrator blocks and added clock cycles, to achieve convergence on a numerical solution. The presented approach eliminates the need for either of these methods. The FPGA executes the HDL code, derived from Figure 3.16 and Figure 3.17, in a single clock cycle, by accurately determining the correct 60°prism the reference voltages resides in, and selecting the unique inverter switch state to drive the CM voltage to zero.

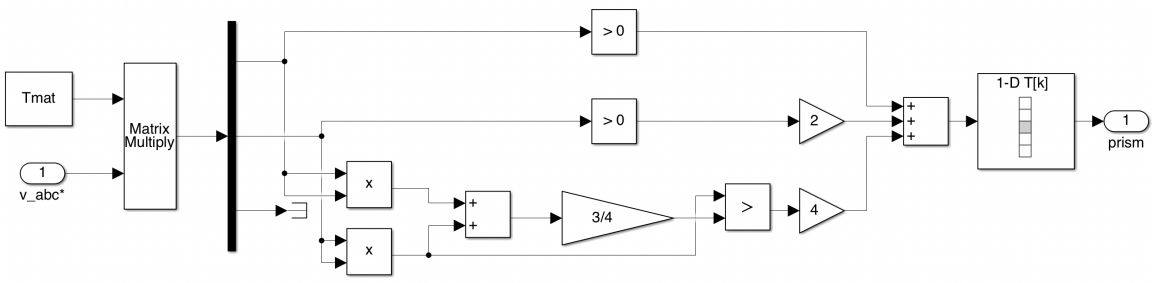
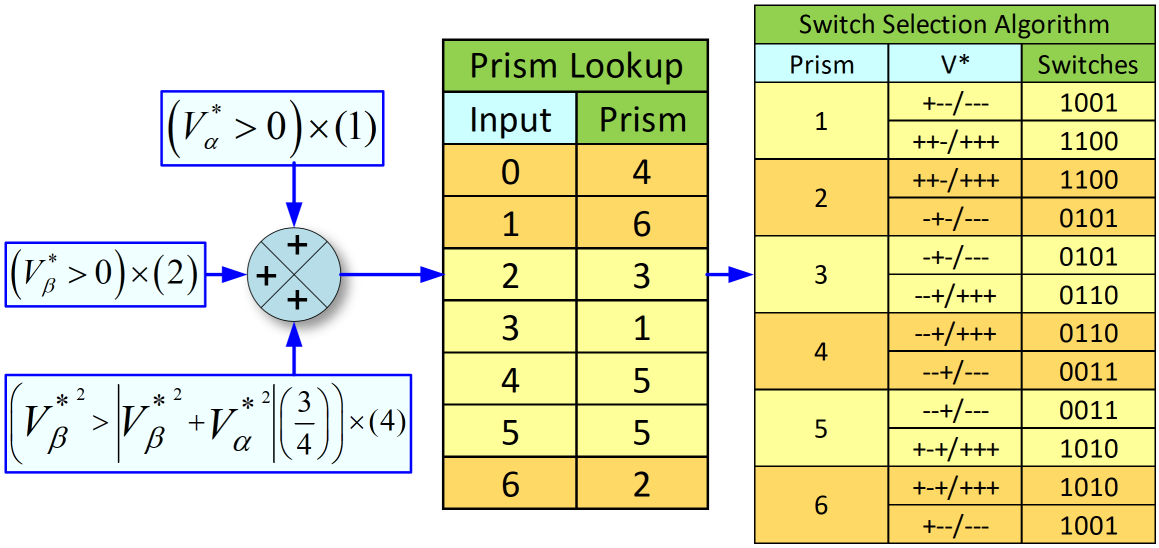


Figure 3.16. Simplified arc tangent 2 function replacement for fixed-point MPC in Simulink.



Prism Lookup	
Input	Prism
0	4
1	6
2	3
3	1
4	5
5	5
6	2

Switch Selection Algorithm		
Prism	V*	Switches
1	+--/---	1001
	++-/+++	1100
2	++-/+++	1100
	-+-/---	0101
3	-+-/---	0101
	--+/+++	0110
4	--+/+++	0110
	--+/---	0011
5	--+/---	0011
	+-+/+++	1010
6	+-+/+++	1010
	+--/---	1001

Figure 3.17. Novel fixed-point MPC switch selection flow path.

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CHAPTER 4:
HARDWARE IMPLEMENTATION

To experimentally validate the results of the physics-based model simulated within a MATLAB/Simulink environment and discussed in chapter 3, a hardware implementation of inverter and controller was constructed in a power electronics laboratory as shown in Figure 4.1. An example of a small CM choke, as indicated in the schematic of Figure 4.1, is shown in Figure 4.2 together with a size comparison. A photograph of the four-leg three-phase inverter and controller prototype is shown in Figure 4.3, including filters and load. As depicted in Figure 4.3 and Figure 4.1 and listed in Table 4.2 the system includes the following major components:

- The four-leg three-phase inverter is constructed using two Infineon EVAL-M5-IMZ120R-SIC boards mounted on top of one another, each providing two legs of the four-leg inverter [12], [24]. The switching devices on the boards are 1200 V SiC Trench MOSFETs.
- The control system was implemented on an FPGA development board, a Xilinx Arty-A7 [25]. The FPGA implemented Verilog code, produced from the HDL coder output of the MATLAB/Simulink model. The FPGA operated the four-leg inverter utilizing MPC and ΔM control in order to eliminate CM. The FPGA was programmed utilizing Vivado, a Xilinx development software package that allows for the design, verification and implementation of HDL code [26].
- A second-order passive LC filter was inserted between the LISNs and the four-leg three-phase inverter. This filter reduced the DM EMI produced by the inverter so that the conducted emission limits in [4] are met. The control methods proposed in this thesis address CM, not DM conducted emissions.
- The BESS system was replaced by a DC bus load consisting of a resistor bank. The fan-cooled resistor bank was utilized to dissipate 3 A of current supplied by the inverter. The bank resistance was sized such that there was no heat or power concerns.
- The AC grid was obtained from the laboratory three-phase source connected to a variac. In the physics-based model the grid was obtained with an ideal three-phase voltage source and series resistor/inductor.

- The placement of a small CM choke, as seen in Figure 4.2, was investigated to reduce the high frequency noise/EMI in the MHz frequency range which are not addressed by the CM elimination methods proposed in this thesis. The number of chokes and positions were varied as seen in Figure 4.1 and described in chapter 5. For comparison, [7] utilized CM chokes sized in the millihenry range for a comparable three-phase inverter. CM chokes, like the one seen in Figure 4.2, are in the microhenry range.

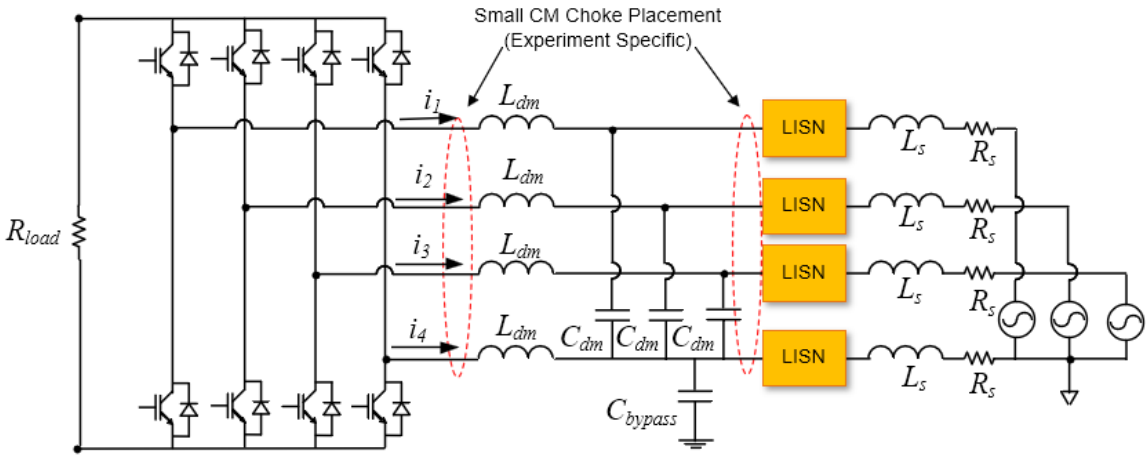

Figure 4.1. Hardware schematic.

Figure 4.2. Small CM choke size comparison with a No.2 pencil.

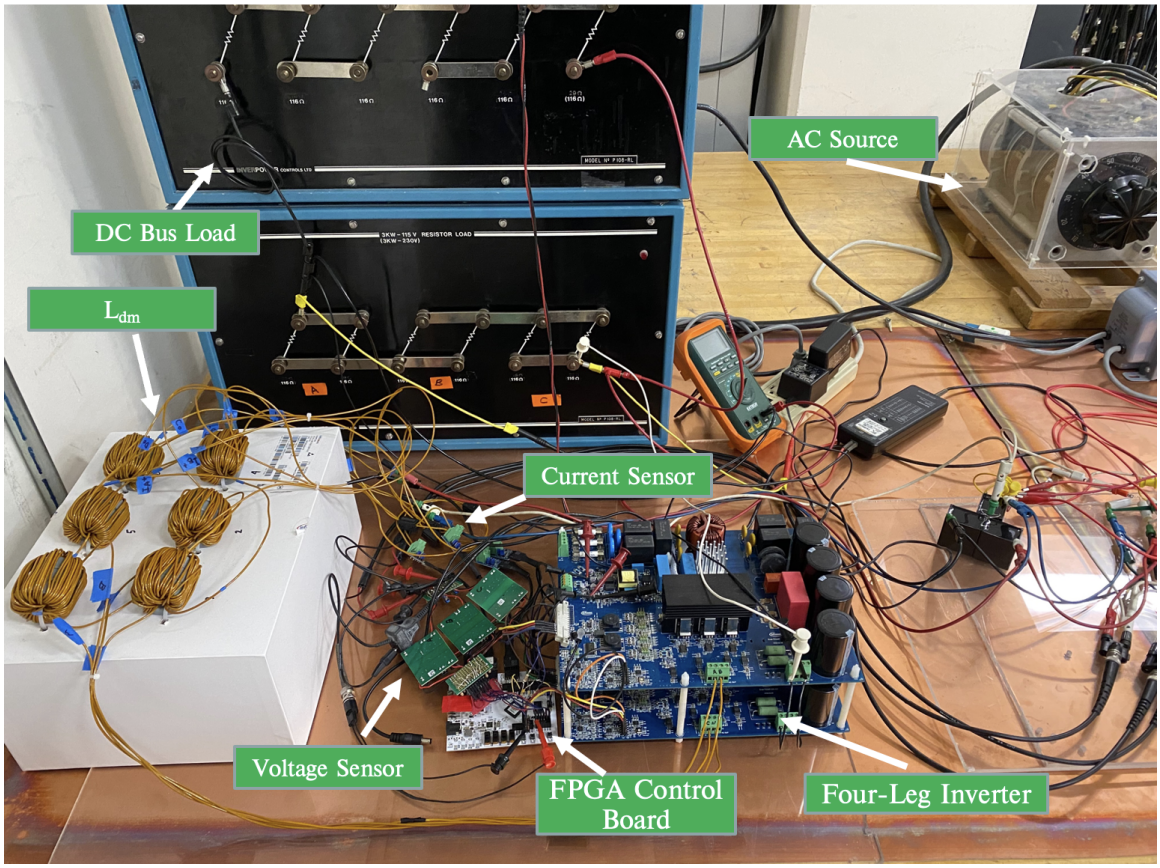

Figure 4.3. Hardware picture of control board and implementation board.

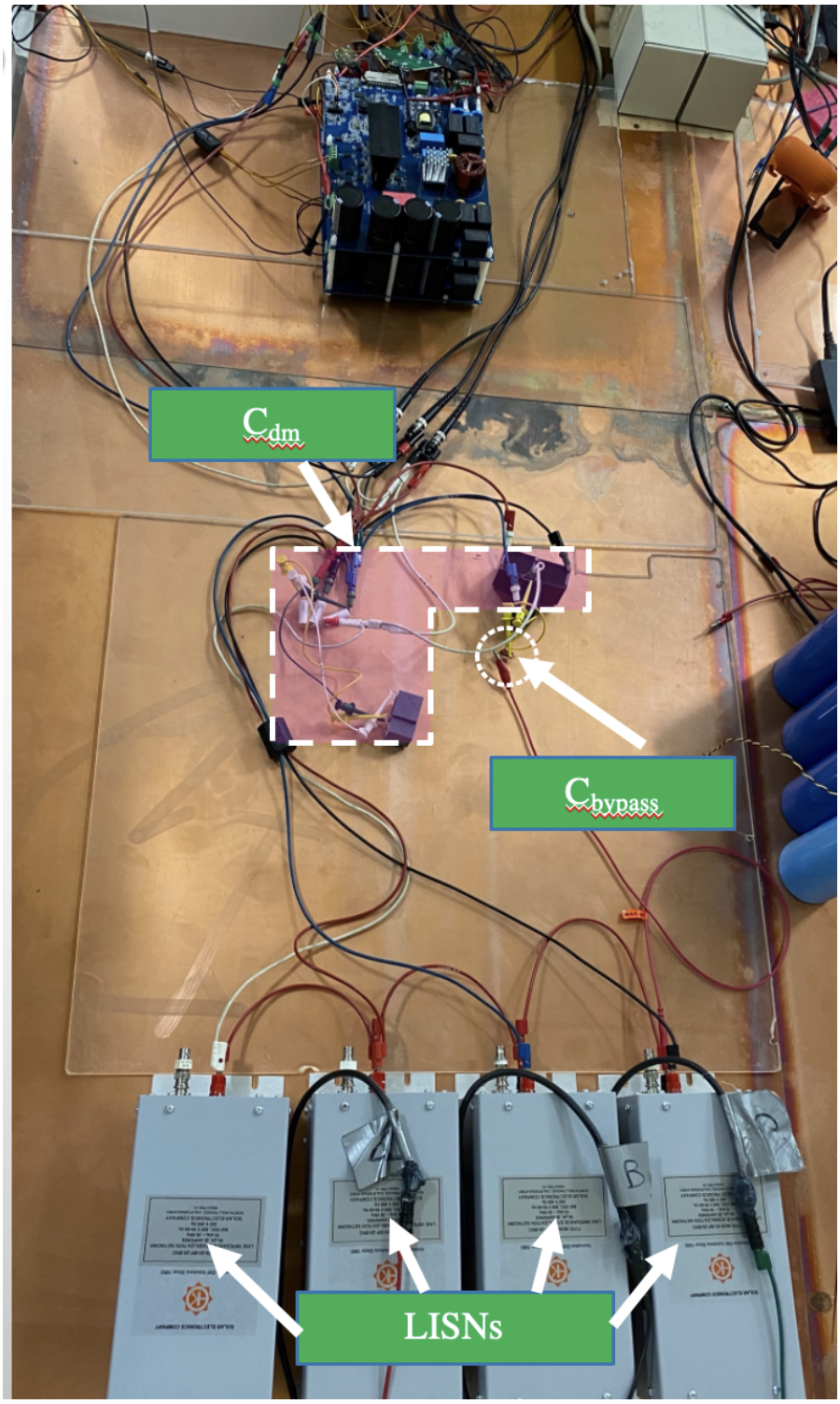

Figure 4.4. Hardware picture of LISNs and DM filter.

4.1 Control Hardware Setup

The block diagram of the inverter control hardware is presented in Figure 4.5 and conveys the major control elements and the connections between them. The four-leg three-phase inverter is comprised of two Infineon development boards, utilizing silicon-carbide devices, each providing two legs of the inverter. The Infineon boards, acting as the inverter, are directly controlled by the Xilinx FPGA control board. The FPGA and development boards continuously communicate with each other. The FPGA sends an enable signal when conditions are met to update the state of the SiC switching devices. When conditions are met to update the inverter switches the FPGA sends 8 gate drive signals to the development board, establishing the new inverter switching states, always maintaining two top rail switches and two bottom rail switches on at all times.

In contrast, the development board will send a fault signal to the FPGA, shutting down operation, whenever an over-voltage condition is experienced or a ten-second timer expires following the commencement of an experiment. The over-voltage shutdown protects the sensitive hardware while the ten-second timer limits the amount of current supplied to the resistor bank, therefore minimizing the power and heat generation. Ten seconds also allows for the collection of current and voltage data via the oscilloscopes.

The FPGA is powered externally by a 12 V, 36 Watt power supply. For the MPC scheme to work correctly, the FPGA must be supplied with the inverter current and voltage phase information. The inverter current is sensed through 12-bit analog to digital converter. The voltage phase is sensed through a precision isolation amplifier to protect the FPGA from experiencing a serious excess voltage far exceeding the board rating. The inverter current and voltage phases are also monitored via current and voltage probes respectively. These probes are then fed to two independent oscilloscopes that monitor the parameters in real time. The oscilloscopes were utilized to capture experimental results presented in Chapter 5. With each experiment in progress the waveforms present on the oscilloscopes were captured, downloaded and post processed with MATLAB.

The FPGA acts as the controller for the inverter. The FPGA is interconnected with a Personal Computer (PC), via a micro Universal Serial Bus (USB) cable, and the control software can be either flashed to volatile memory (lost upon loss of power) or loaded in to fixed memory.

For the initial control software testing, and to aid in making rapid software adjustments, the PC remained connected to the Arty-A7 after flashing the Verilog controller code to FPGA. This allowed for the Verilog code to be adjusted and reloaded onto the FPGA. Once the finalized controller code was established, the Verilog code was loaded into the FPGA non-volatile memory which allowed the controller to be run while the PC was disconnected. This also prevented a loss of software due to a loss of power to the FPGA, requiring the code to be subsequently re-flashed onto the FPGA.

The process of establishing the controller code is described in detail in Section 4.2. To program the FPGA with the MPC code, the FPGA must be connected to the PC via USB. Once connected, Vivado Software was used to mount the FPGA, establishing a serial connection with the board. With the connection established the Verilog code containing the HDL code for the MPC controller scheme was loaded into the FPGA, either in Random Access Memory (RAM) for a temporary solution or in flash memory to support multiple runs over multiple days.

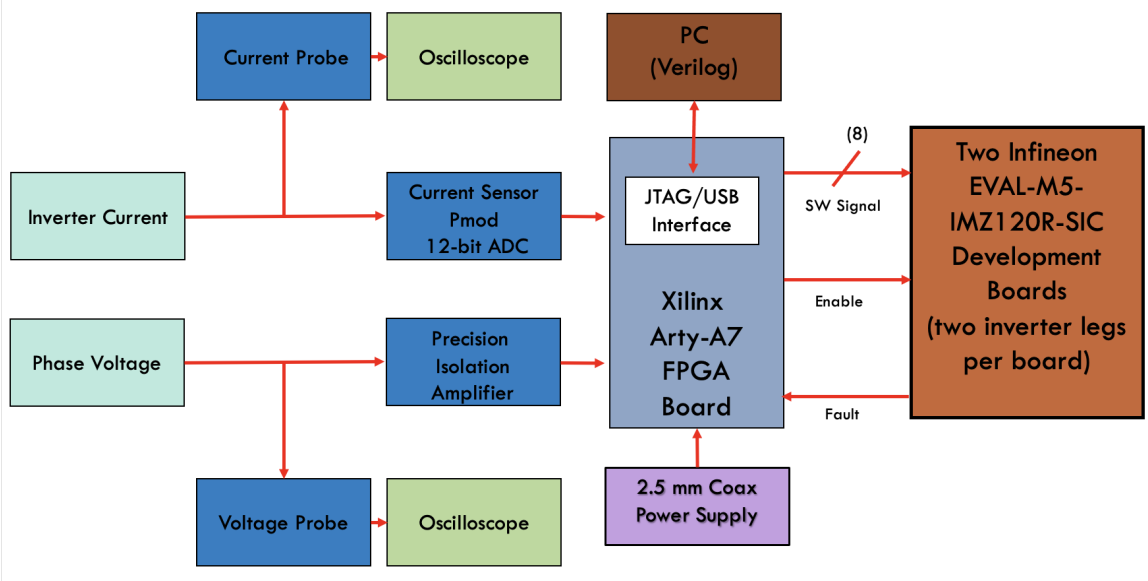

Figure 4.5. Control hardware block diagram.

4.2 HDL Coder and Verilog

Simulating a four-leg, three-phase inverter using MATLAB and Simulink is not limited by the physical space constraints on the FPGA or its limited computing power. Therefore, when designing the inverter control scheme, the computing power afforded by MATLAB and Simulink was exploited, as seen in section 3.3.1. Once a robust model and control scheme was established, the control scheme was reconstructed within the constraints of the MATLAB fixed-point toolbox [23]. Converting the control scheme to fixed-point precision allowed for the use of a powerful tool within MATLAB, HDL Coder [23].

HDL Coder is a built-in MATLAB toolbox that performs the direct conversion of a supported Simulink model, constructed with HDL coder-compatible blocks, to a fully functional Verilog script. Verilog is an HDL language, fully supported by FPGA boards. With the MPC control script converted to Verilog code, it was loaded onto the FPGA and the hardware implementation of the four-leg three-phase inverter was tested to validate the simulated results predicted in MATLAB. Figure 4.6 depicts the MATLAB to Verilog to FPGA flow path.

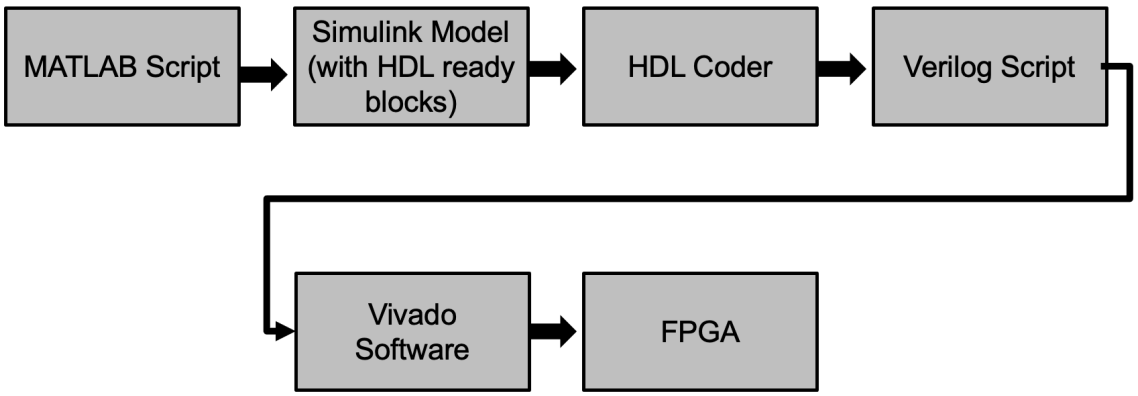

Figure 4.6. Simulink model to Verilog script to FPGA flow path.

4.3 Field Programmable Gate Array

The development board used to drive the control scheme for the four-leg inverter was the Arty-A7 35T by Digilent. The Arty-A7 was designed on the Xilinx Artix-7 FPGA

architecture [25]. The development board was chosen for its seamless integration and support for Verilog HDL. Figure 4.7 and Table 4.1 provide a general visual and description of the Arty-A7.

The current sensor Peripheral Module Interface (Pmod) 12-bit ADCs and the precision isolation amplifiers are connected to the FPGA via the Pmod connectors and allow the FPGA to monitor inverter leg current and phase voltage respectively. The fault, enable, gate drive signals are passed through the Arduino/chipKIT shield connectors. The FPGA is connected to the PC via the shared USB port and is powered externally via the power jack for external supply.

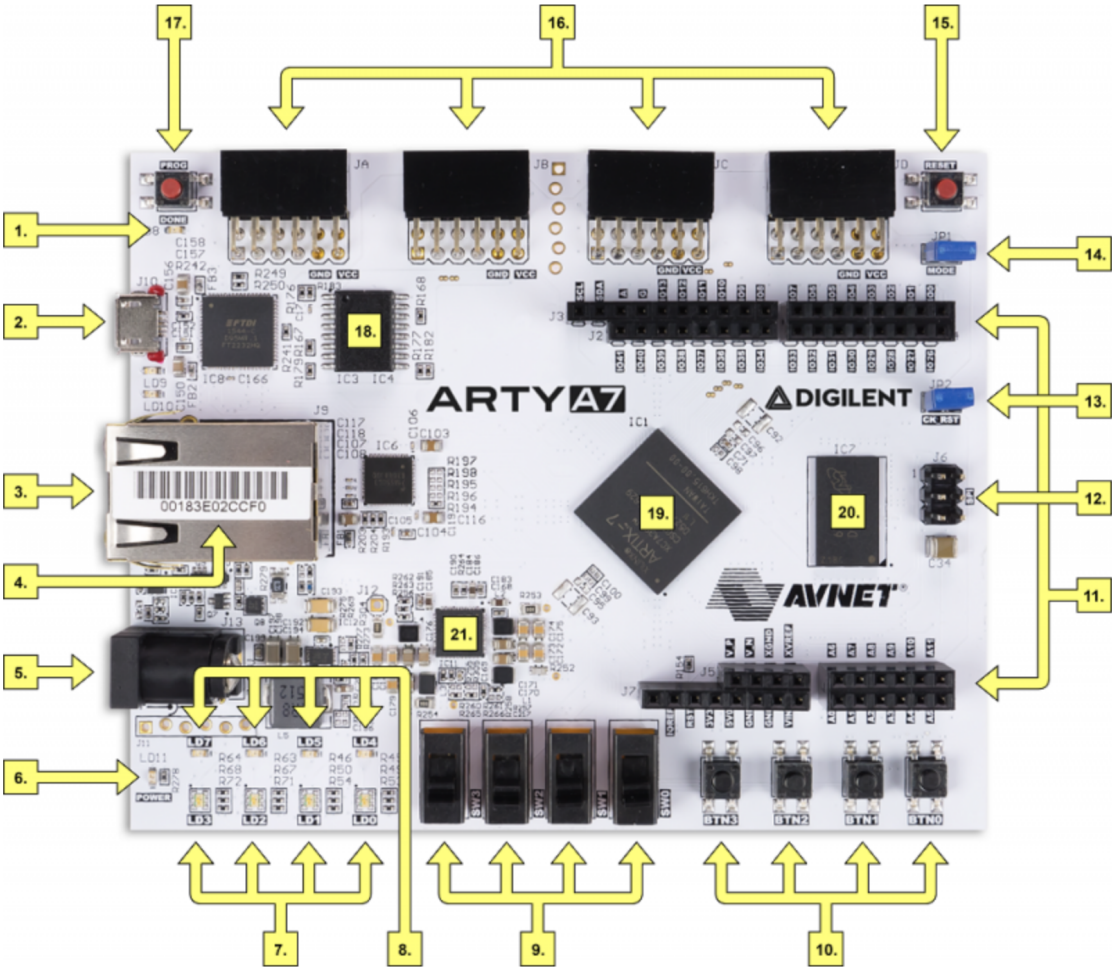

Figure 4.7. Arty-A7 development-board call-out diagram. Source [25]

Table 4.1. Arty-A7 call-out table. Source [25].

Callout	**Description**	**Callout**	**Description**	**Callout**	**Description**
1	FPGA programming DONE LED	8	User RGB LEDs	15	chipKIT processor reset
2	Shared USB JTAG / UART port	9	User slide switches	16	Pmod connectors
3	Ethernet connector	10	User push buttons	17	FPGA programming reset button
4	MAC address sticker	11	Arduino/ chipKIT shield connectors	18	SPI flash memory
5	Power jack for external supply	12	Arduino/ chipKIT shield SPI connector	19	Artix FPGA
6	Power good LED	13	chipKIT processor reset jumper	20	Micron DDR3 memory
7	User LED	14	FPGA programming mode	21	Dialog semiconductor DA9062 power supply

Table 4.2. Hardware Implementation Parameter and Component List.

Component	**Value**	**Measured Parameter**	**Notes**
External Power Supply (Variac)	Type 1 [2]	N/A	Provide three-phase AC power
External Power Supply	15 V	N/A	Tektronix PS280 DC power supply
Oscilloscope	N/A	(4) LISN currents (4) LISN voltages	Tektronix MSO 4034
Current Probe	N/A	(4)LISN Current	(4) Tektronix TCPA300
Voltage Probe	N/A	(4)LISN Voltage	(4) Tektronix P5200
LISN	N/A	N/A	(4) Type 9629-50-BP-25-BNC, Solar Electronic Company
C_{dm}	34 μF	N/A	Inverter DM filter capacitor
L_{dm}	500 μH	N/A	Inverter DM filter inductor
C_{dc}	1.2 μF	N/A	DC bus capacitor
Fully-Differential Isolation Amplifier	N/A	N/A	(3) TI AMC1200B precision isolation amplifiers
Current Sense Module	N/A	N/A	(4) Digilent Pmod ISNS20 12-bit ADC current sensor

CHAPTER 5:
RESULTS

5.1 Simulation Results

The developed physics-based model of the four-leg three phase grid-connected inverter depicted in Chapter 3 was simulated within the MATLAB/Simulink environment to model inverter operation. The objective of the physics-based modeling was to design the inverter controller and to verify that the inverter did not produce any CM voltage, while still maintaining a constant current supply to a simulated load. Simulations were performed using MPC and ΔM as CM elimination methods with two goals; 1) verify that the predicted conducted EMI met the limits in [4] and the power quality requirements in [2] and 2) compare the performance of the two strategies.

The physics-based model does not account for higher order effects like switching transients or parasitic elements between the switching devices and their heat sinks. As an example, the model does not include any noise that would be otherwise produced by the act of blanking time, an artifact of ensuring that the top and bottom rails of the inverter are not cross connected [7]. This is due to the fact that the switching semiconductors in Simulink are modeled as ideal switches and therefore commutate instantly when a control signal is sent to update their status. This simplified modeling method results in simulated conducted emission spectra that have minimum or no noise in the MHz frequency range. Parasitic capacitors were included in the model between the load neutral and ground as well as between the mid-point of the DC bus and ground to provide a path to the CM currents in the system. These components are key to predicting the CM EMI at the converter's switching frequency, which are the emissions that the proposed control methods seek to eliminate.

The simulated results were obtained with the converter connected to the grid and controlled in grid-following mode, with a resistive DC load and with the circuit parameters listed in Table 5.1. As depicted in Figure 4.5, the grid was modeled as an ideal three-phase voltage source with a resistor and inductor in series to represent the laboratory three-phase source, variac and cables connecting to the EUT.

Table 5.1. Simulink Physics-Based Model Parameters.

Component	**Value**
Filter Inductors	10 mH
Filter Capacitors	34 μF
Load Resistors	10 Ω
Load Inductors	1 mH
Grid Resistors	10 mΩ
Grid Inductors	500 μH
DC Bus Capacitance	10 mF

The verification of MPC to eliminate CM EMI was the main goal of this thesis. The MATLAB/Simulink continuous time model, described in section 3.3 was used to simulate the EMI spectra, which were plotted against the CE101 and CE102 limits specified in MIL-STD-461G [4] utilizing MATLAB.

Figures 5.1 and 5.2 depict the simulated CE101 data for MPC and ΔM respectively. They display the four simulated LISN current spectra demonstrating that all four LISN currents are well within the CE101 limits of [4]. Similarly, Figures 5.3 and 5.4 present the simulated LISN voltage spectra for MPC and ΔM respectively, demonstrating that all four LISN voltages are well within the CE102 limits of [4]. From Figure 5.1 through Figure 5.4 it is concluded that both control strategies are capable of reducing the CM EMI below the CE101 and CE102 limits without the use of CM filters. However, as previously noted, the physics-based model does not account for electromagnetic noise at frequencies higher than about 30 kHz, due to the idealization of the switching events and the simplification of the CM paths. Therefore, the displayed spectra do not predict accurately the high frequency noise data which will be measured in the laboratory prototype and which will require small CM filters to meet the CE102 limits.

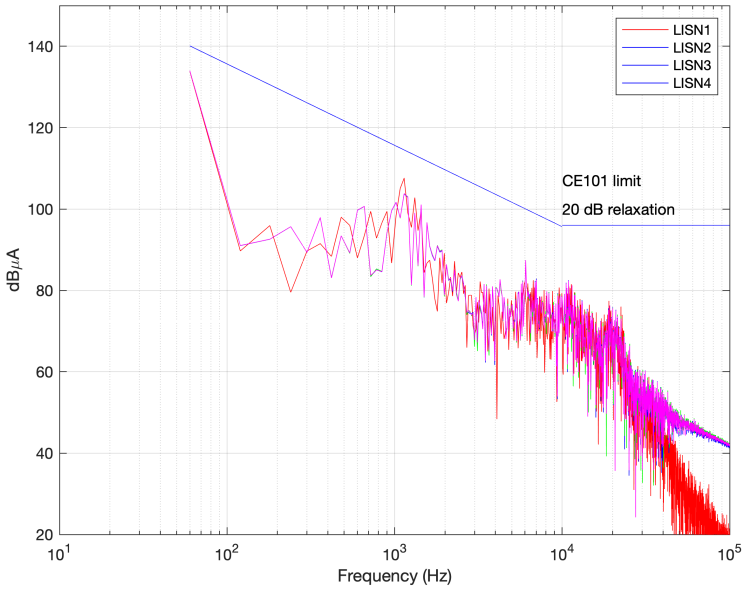

Figure 5.1. Simulated CE101 MPC measurement of LISN current spectrum.

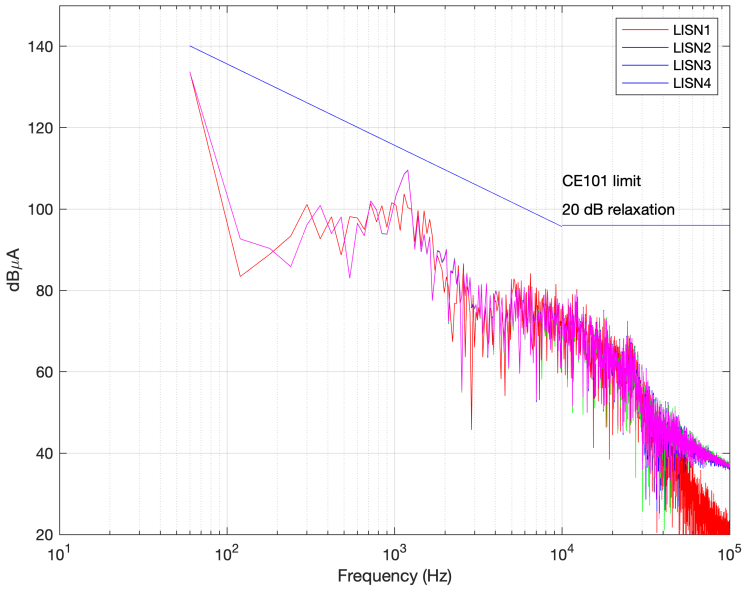

Figure 5.2. Simulated CE101 ΔM measurement of LISN current spectrum.

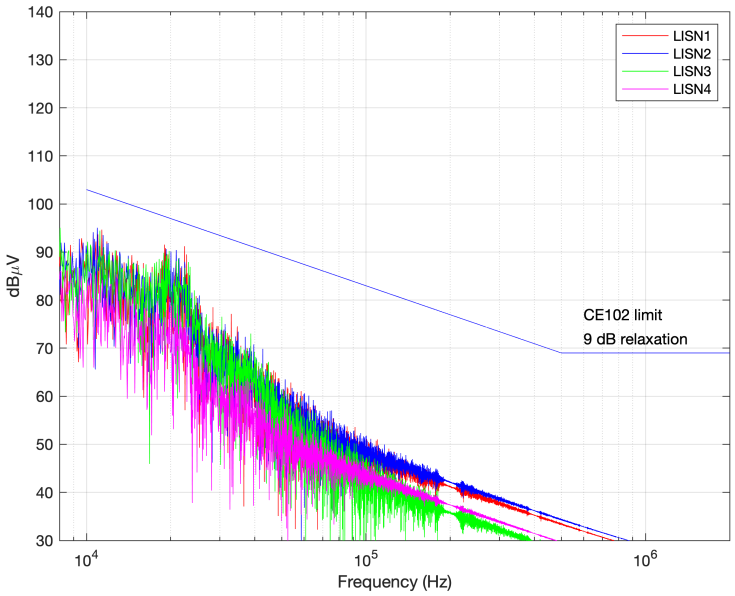

Figure 5.3. Simulated CE102 MPC measurement of LISN voltage spectrum.

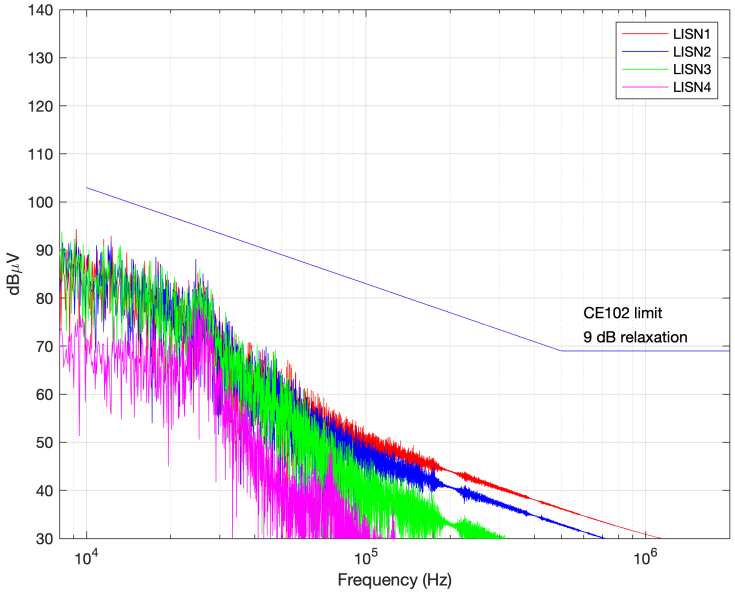

Figure 5.4. Simulated CE102 ΔM measurement of LISN voltage spectrum.

Tables 5.2 and 5.3 present the average switching frequency for MPC and ΔM respectively. As

shown, ΔM exhibits a higher average switching frequency than MPC. It can be observed that PDM is being executed effectively due to the fact that every inverter leg has an independent average switching frequency, unlike the fixed switching frequency which results from using PWM. It can also be noted that in both control strategies the forth leg is preferentially chosen to drive the CM EMI to zero while legs one through three remain fairly consistent.

Tables 5.4 and 5.5 display the calculated losses of the switching semiconductors for MPC and ΔM respectively. The losses were calculated using data sheet information for the Semikron power module SKM50GB12V, which includes silicon 1200 V 50 A Insulated-Gate Bipolar Transistors (IGBTs) with anti-parallel diodes [27]. As expected, the analysis shows that an increased switching frequency results in higher switching losses. Note that the fourth leg features smaller switching losses, even though its switching frequency is higher than the other three legs. This is due to the low current flowing on the fourth leg, because the load is balanced. Overall, the switching losses are expected to be greatly reduced when SiC switching semiconductors are used instead of silicon devices.

Table 5.2. MPC Average Switching Frequency for Physics-Based Model.

Inverter Leg	**Switching Frequency (Hz)**
1	15,000
2	14,600
3	14,225
4	25,900

Table 5.3. ΔM Average Switching Frequency for Physics-Based Model.

Inverter Leg	**Switching Frequency (Hz)**
1	18,825
2	18,775
3	17,825
4	26,675

Table 5.4. MPC Switch Device Losses for Physics-Based Model.

Inverter Leg	**Device Losses (W)**		
	IGBT Losses	Diode Losses	Total Losses
1	5.95	21.54	27.5
2	5.86	20.53	26.4
3	5.89	21.41	27.3
4	7.84	13.04	20.9

Table 5.5. ΔM Switch Device Losses for Physics-Based Model.

Inverter Leg	**Device Losses (W)**		
	IGBT Losses	Diode Losses	Total Losses
1	6.68	27.68	34.36
2	6.86	28.06	34.91
3	6.67	27.64	34.31
4	6.52	1.99	8.51

5.2 Experimental Results

The four-leg three-phase inverter and control system depicted in Figures 4.3 and 4.4 and described in Chapter 3 was used to obtain all the experimental data presented in this section. The three-phase input voltage was set to the Type I voltage 200 V_{rms} line-to-line [2]. The inverter was programmed to draw a constant 3 A from the three-phase source for 10 s and feed a resistive load on the DC bus. Substituting the BESS depicted in Figure 3.1 with a resistive DC load guarantees that only the three-phase four-leg inverter conducted EMI were measured, to verify the performance of the two CM elimination methods. A BESS includes a DC-DC switching converter to regulate the DC bus, and that additional power conversion stage would add CM EMI to the measurements.

The experimental plots were acquired through the use of voltage and current probes con-

nected to the four LISNs and feeding the measured data to two Tektronix MSO 4034 four-channel oscilloscopes. The LISN voltage and current data was downloaded from the oscilloscopes and post-processed using MATLAB to plot the spectra together with the CE101 and CE102 limits specified in MIL-STD-461G [4].

To validate the physics-based model and to verify that MPC is a valid control scheme to eliminate CM voltage while meeting the EMI limits set by MIL-STD-461G [4], several experiments were conducted as listed in Table 5.6. As part of the experimental trials, the following parameters were modified in the laboratory set-up:

- **Scope Resolution:** The oscilloscope resolution in Volts per division (V/div), was adjusted for consecutive trials, where no other parameters were changed, to quantify the affected output data resolution.
- **CM Choke Size and Location:** Although no CM choke was necessary to suppress the switching frequency noise, some CM high-frequency noise in the MHz frequency range was measured outside the CE102 limits. Multiple experiments were run with varying CM choke sizes and CM choke positions to reduce the EMI in the MHz frequency range. The CM chokes were placed before and after the DM filter to identify the minimum CM choke size. Table 5.7 lists the CM choke details, where a "4181" and "8281" core in Table 5.6 correspond to Fair-Rite Snap-It Cores 0475164181 and 0475178281 respectively. Note that both are very small as shown in the photograph of Figure 4.2.
- **Control Strategy:** The simulation results obtained with MPC and ΔM and presented in section 5.1, are experimentally validated to provide a proof of concept and allow for quantitative analysis between the two control schemes.

In addition to the small CM choke, a small 120 nF bypass capacitor was connected between ground and the neutral wire of the capacitors in the filter. This capacitor contributed to the reduction of high frequency EMI in the megahertz frequency range, outside of the CM EMI produced by the inverter switching frequency. These EMI are not eliminated by the proposed control schemes, but they were reduced by passive filtering of small size.

Table 5.6. Experimental Trials

Experiment #	**Modulation**	**Scope Resolution**	**Choke Placement**	**Figure**
1	MPC	1 V/div	3 4181 cores, 2 turns after filter	Figure 5.5
2	MPC	0.5 V/div	3 4181 cores, 2 turns after filter	Figure 5.6
3	MPC	0.5 V/div	None	Figure 5.7
4	MPC	0.5 V/div	5 4181 cores, 1 turn before filter	Figure 5.8
5	MPC	1 V/div	5 4181 cores, 1 turn before filter	Figure 5.9
6	MPC	1 V/div	5 4181 cores, 1 turn before filter & 1 4181 core, 2 turn after filter	Figure 5.10
7	MPC	1 V/div	2 8281 cores, 1 turn before filter & 1 4181 core, 2 turns after filter	Figure 5.11
8	MPC	1 V/div	1 4181 core, 2 turns after filter	Figure 5.12
9	ΔM	1 V/div	1 8281 core, 1 wire turn before filter	Figure5.13
10	MPC			Figure 5.14
11	ΔM	1 V/div	1 8281 core, 1 turn before filter & 1 4181 core, 2 turns after filter	Figure 5.15
				Figure 5.17
	MPC			Figure 5.16
				Figure 5.18
12	ΔM	1 V/div	1 8281 core, 1 turn before filter & 1 4181 core, 1 turns after filter	Figure 5.19
				Figure 5.21
	MPC			Figure 5.20
				Figure 5.22

Table 5.7. Material 75 Fair-Rite Products Corp. Snap-It low frequency suppression cores [28]

Snap-It Cores Part #	**Typical Impedance (Ω)**								
	500 kHz			1 MHz			5 MHz		
	# of turns			# of turns			# of turns		
0475178281	46	430	1200	87	790	2200	74	660	1800
0475164181	58	520	1470	102	890	2500	50	445	1220

5.2.1 Experimental Trial and Error Results

First, an initial verification of the hardware prototype was required to ensure that the control system simulated in Simulink and used to program the FPGA fully functioned in the laboratory. Once it was determined that the inverter constructed in the laboratory was operating as simulated, the trial and error method was utilized to fine-tune the inverter performance with the goal of ensuring that the conducted EMI limits required by [4] were met. The experiments are described in Table 5.6 where the figures presented in this section are also listed.

Experiments 1 and 2 focused on establishing the optimal scope resolution for data collection. The oscilloscope was utilized for collecting the time-domain currents and voltages as Comma-Separated Values (CSV) files, which were then post-processed utilizing MATLAB. The fast Fourier transform (FFT) function was used to obtain the frequency-domain plots from the time-domain currents and voltage, then the spectra were plotted together with the CE101 and CE102 limit lines required by MIL-STD-461G. Figures 5.5 and 5.6 were obtained with the set-up featuring identical filter components and differ only in scope resolution, 1 V/div vs. 0.5 V/div respectively.

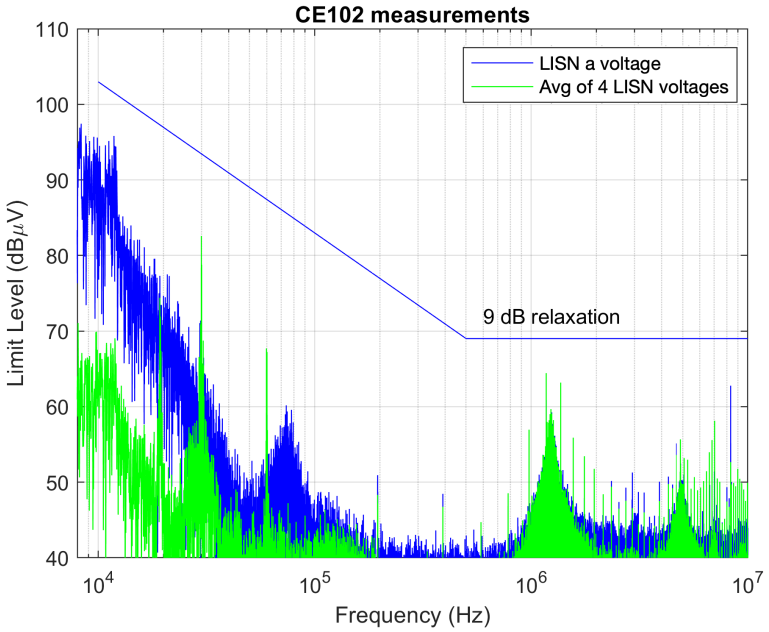

Figure 5.5. Experiment 1: MPC experimental measurement of LISN voltage spectrum.

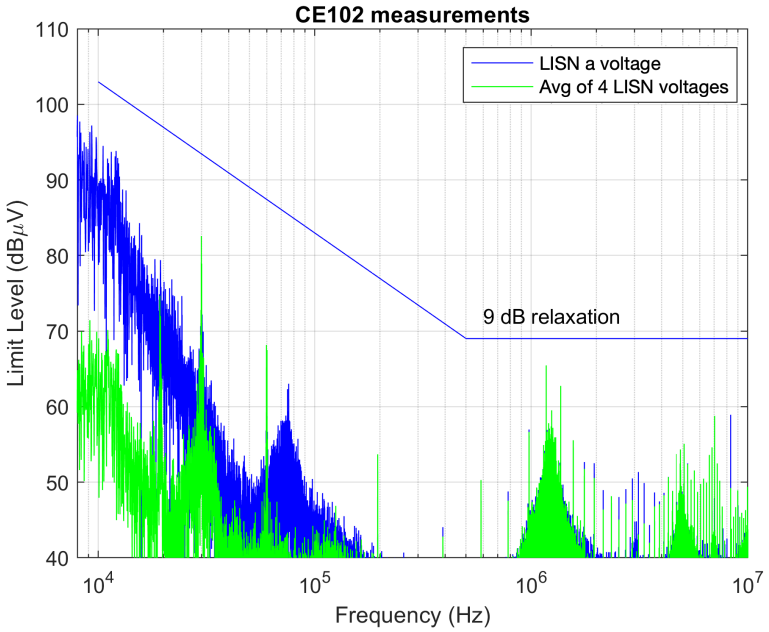

Figure 5.6. Experiment 2: MPC experimental measurement of LISN voltage spectrum.

As a result of increasing the oscilloscope resolution, by reducing the vertical scale from 1 V/div to 0.5 V/div, it was noted that there was a visual change in the post-processed spectral data. The slight difference in spectral data was only noted in the limit level noise, the y-axis. It was noted that there was no noticeable change in the frequency distribution, x-axis, of the CM noise.

It was determined that while there was a slight decrease in the noise registered by the oscilloscope with the resolution set to 0.5 V/div, the difference was not appreciable enough to affect the results of this thesis, which are to determine if the CE101 and CE102 limits of [4] can be met utilizing the MPC and ΔM control strategies. While experiments 3 and 4 utilize a scope resolution of 0.5 V/div, the remainder of the experiments, including the final direct MPC/ΔM comparative measurements utilize a scope resolution of 1 V/div.

Following the establishment of the 1 V/div scope resolution, all CM chokes were removed from the hardware prototype and the system was tested to see if MPC alone, without the assistance of a small CM choke, could meet the EMI limits of [4]. As Figure 5.7 depicts, the MPC controller does not eliminate the high frequency conducted EMI, which exceeds CE102 limits with the 9 dB relaxation set by [4]. The 9 dB relaxation was implemented due to the EUT being capable of operating at 220 V_{rms}, as seen in Figure 2.4 [4].

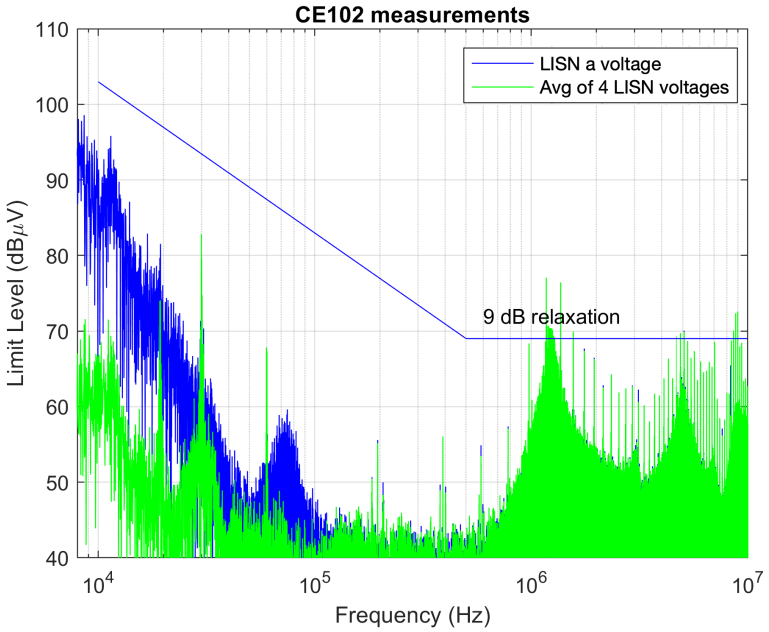

Figure 5.7. Experiment 3: MPC experimental measurement of LISN voltage spectrum.

Once it was established that the EMI requirements of [4] could not be met without CM chokes, the next step was to determine how small of a choke could be used and still meet the EMI limits. The initial CM choke arrangement consisted of 5 4181 cores with a single turn before the DM filter and the measured results are shown in Figures 5.8 and 5.9. The only difference between Figures 5.8 and 5.9 is the scope resolution, 0.5 V/div and 1 V/div respectively. This filtering solution works well, although the limits are not met in the entire CE102 frequency range.

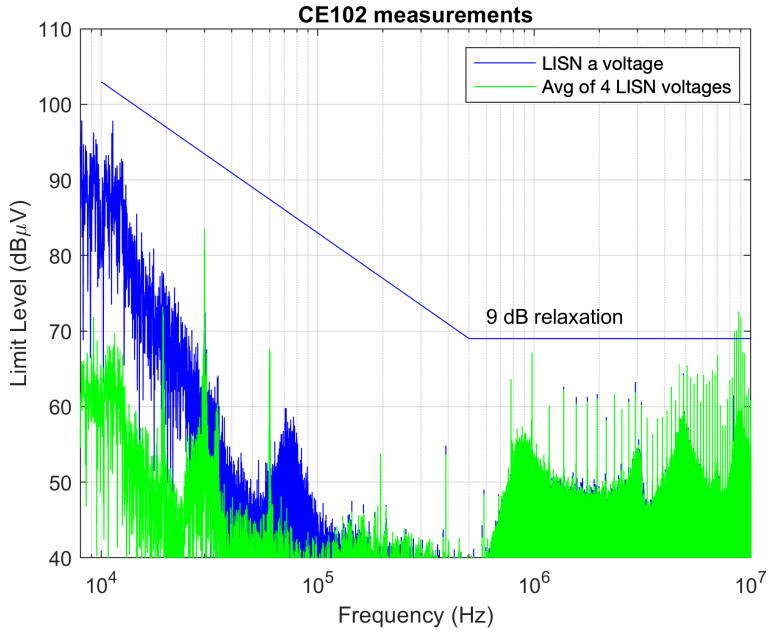

Figure 5.8. Experiment 4: MPC experimental measurement of LISN voltage spectrum.

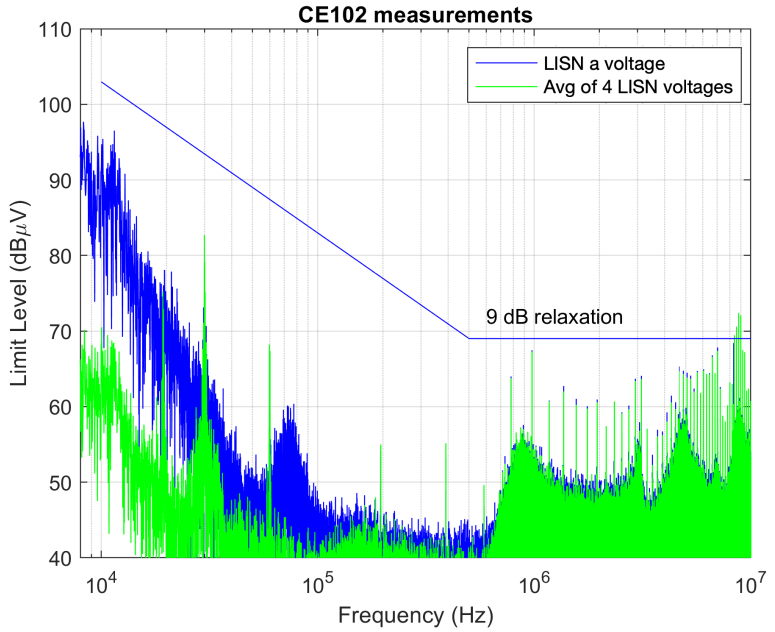

Figure 5.9. Experiment 5: MPC experimental measurement of LISN voltage spectrum.

While adding the arrangement of 5 4181 cores with a single turn before the filter improved the CM EMI, the limits of [4] were not met in the 10 MHz plus range. In order to meet the limits of [4] Experiment 6 added and extra 4181 core with 2 turns with the measured results seem in Figure 5.10. The added choke was placed after the DM filter to start assessing if the placement of the CM chokes before or after the filter improves their overall effectiveness.

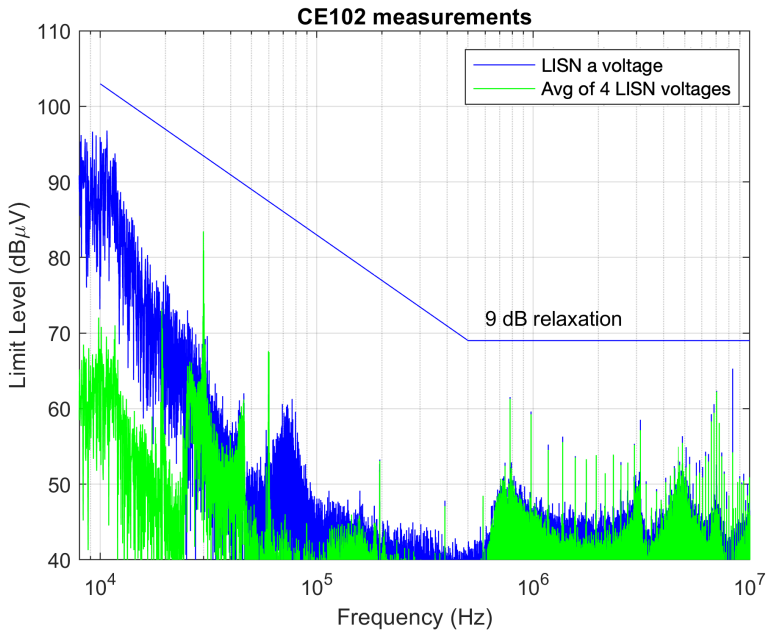

Figure 5.10. Experiment 6: MPC experimental measurement of LISN voltage spectrum.

As seen in Figure 5.10, the hardware prototype was in compliance with the limits of [4] with the addition of a single 4181 choke with 2 turn after the DM filter. The peak at approximately 10 MHz was reduced under the CE102 limit and the entire EMI spectrum was reduced in magnitude.

The next two experiments, labeled 7 and 8 in Table 5.6, explore reducing the number of CM chokes required to meet the CE102 limits. The results of Experiment 7, depicted in Figure 5.11, were obtained with the addition of 2 8281 CM chokes with 1 turn each before the DM filter and 1 4181 CM choke with 1 turn after the DM filter. The results of Experiment 8, shown in Figure 5.12, were obtained by inserting 1 4181 CM choke with 2 turns after the

DM filter. Experiment 7 produces CM EMI significantly under the limits of CE102 while experiment 8 exceeds the 9 dB relaxation limit in the megahertz range, highlighting that a single CM choke, placed before the DM filter, will not help meeting the limits of [4] when MPC is implemented. This also leads to the conclusion that CM chokes before the filter have an effect on reducing CM EMI over the same size choke placed before the filter.

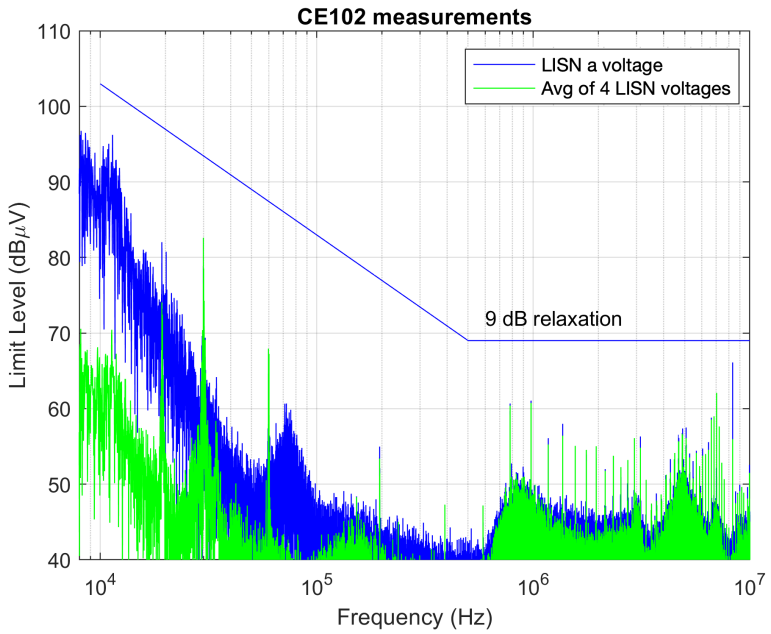

Figure 5.11. Experiment 7: MPC experimental measurement of LISN voltage spectrum.

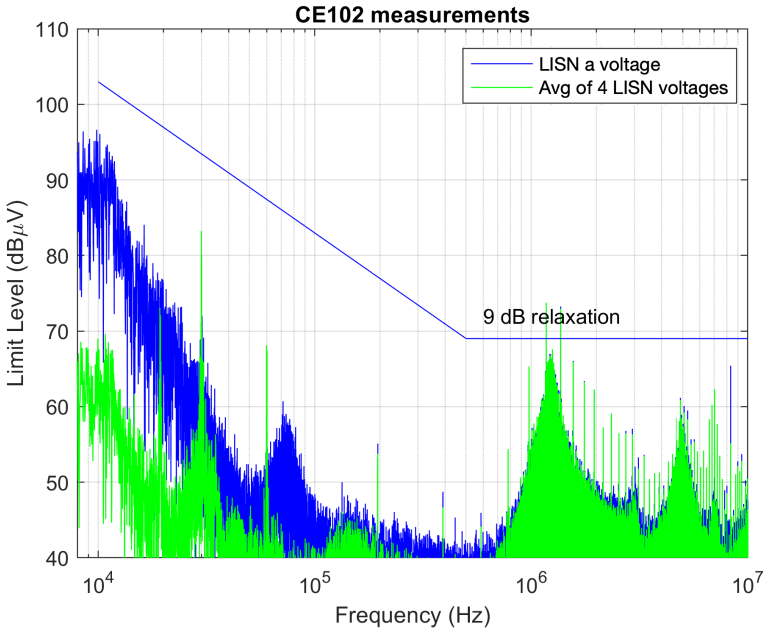

Figure 5.12. Experiment 8: MPC experimental measurement of LISN voltage spectrum.

Upon establishing the optimal oscilloscope resolution of 1 V/div and the requirement that at least 1 CM choke be placed before the DM filter for the hardware prototype to meet the EMI limits of [4] while employing MPC, the two control strategies were compared to ensure they both produced results within the limits of [4]. Experiment 9 and 10 compare the conducted EMI performance of the system with ΔM and MPC respectively. The additional filter consists of 1 8281 core with 1 turn before the filter for both experiments. While both ΔM and MPC meet the CE102 limits, the margin of error is very low. Therefore, it was determined to use at least two CM cores, one placed before the filter and one after the filter, to ensure the EMI limits of [4] were not exceeded.

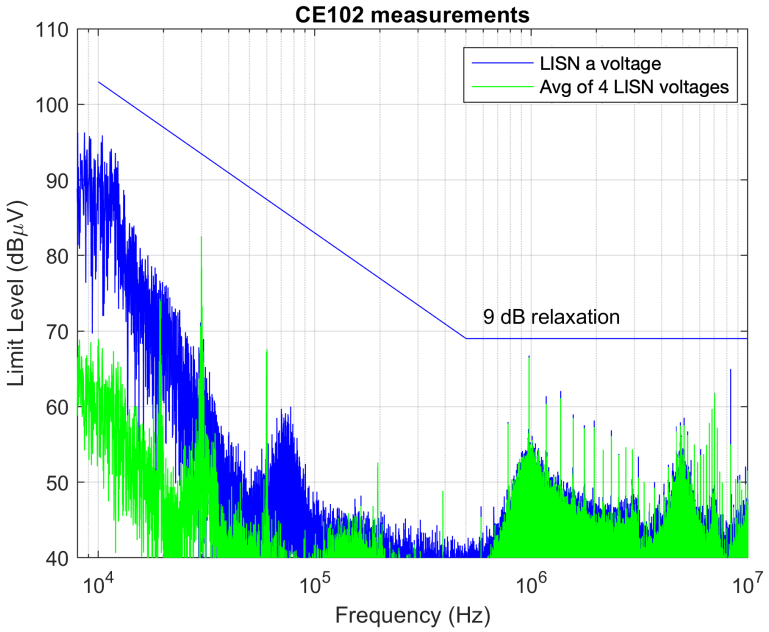

Figure 5.13. Experiment 9: ΔM experimental measurement of LISN voltage spectrum.

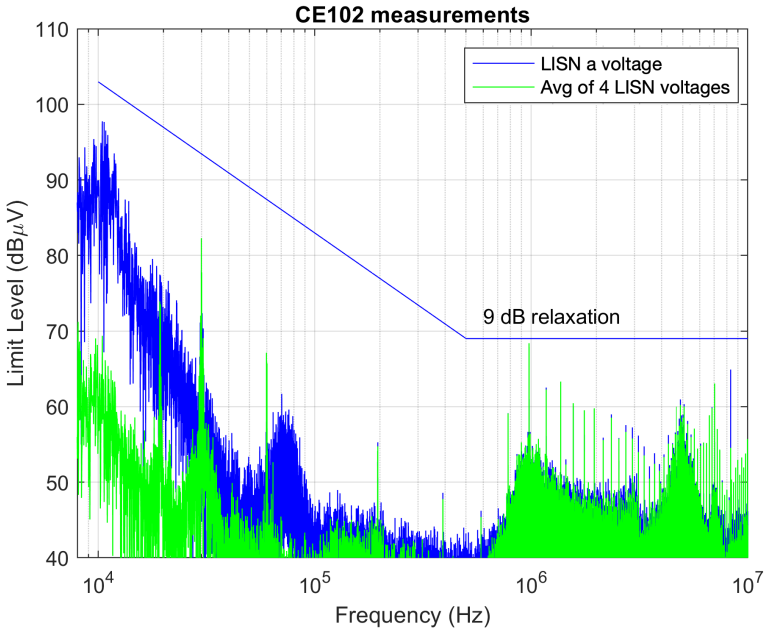

Figure 5.14. Experiment 10: MPC experimental measurement of LISN voltage spectrum.

5.3 Comparative Experimental Results

Experiments 11 and 12 consist of a comprehensive EMI comparison including both CE101 and CE102 limits of [4]. The two experiments directly compare the two competing control strategies MPC and ΔM, under the same loading conditions along with the same CM choke placement. Experiment 11 was performed with 1 8281 core with 1 turn before the DM filter and 1 4181 core with 2 turns after the DM filter. Similarly, experiment 12 was conducted with 1 8281 core with 1 turn before the DM filter and 1 4181 core with 1 turn after the DM filter. Figures 5.15 and 5.16 depict experiment 11 CE101 data for ΔM and MPC respectively and Figures 5.17 and 5.18 depict experiment 11 CE102 data for ΔM and MPC respectively. Figures 5.19 and 5.20 depict experiment 12 CE101 data for ΔM and MPC respectively and Figures 5.21 and 5.22 depict experiment 12 CE102 data for ΔM and MPC respectively.

With respect to the CE101 limits, there was a noticeable degradation in the measured EMI noise present in the LISN current spectrum. The hardware prototype exhibited increased noise in the upper kilohertz range, levels significantly higher then those seen in the physics-based model. The physics-based model did not fully model for every potential noise offender and there could be improvement to simulation to try and replicate the experienced noise in the laboratory with the model.

It was also noted that ΔM was able to maintain two LISN current spectra under the limits of CE101 while MPC was only able to keep one under the limit. The overall magnitude of the CE101 noise in experiments 11 and 12 MPC runs was notably greater then those of the ΔM runs. Also there was no appreciable change in the CE101 data with the manipulation of the the small CM choke placements.

Regarding the CE102 limits, both experiment 11 and 12 demonstrate that the small CM filters provide sufficient EMI reduction to meet the limits imposed by [4]. Therefore, experiment 12 employs the more ideal CM choke arrangement of 1 8281 core with 1 turn before the DM filter and 1 4181 core with 1 turn after the DM filter. This is due to the reduction in complexity by removing the second turn in the CM choke after the DM filter, such that both the chokes only have a single wire turn.

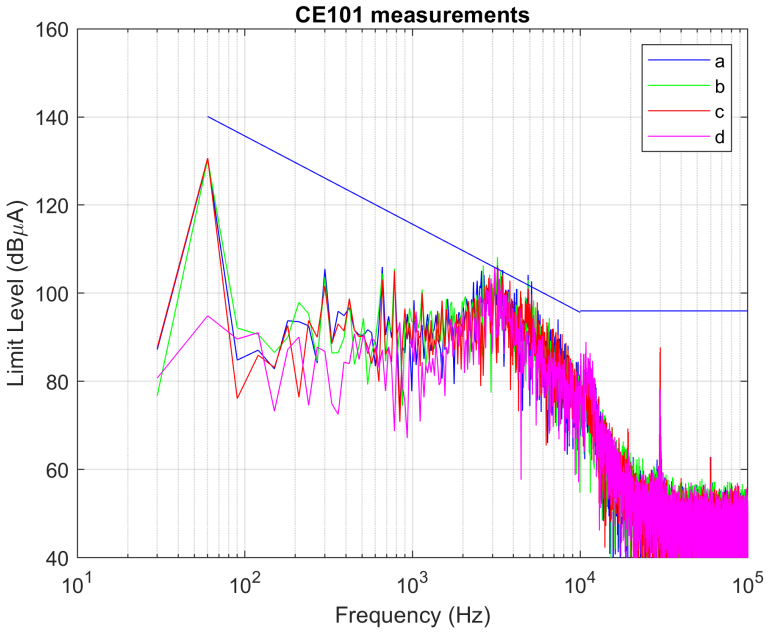

Figure 5.15. Experiment 11: ΔM experimental measurement of LISN current spectrum.

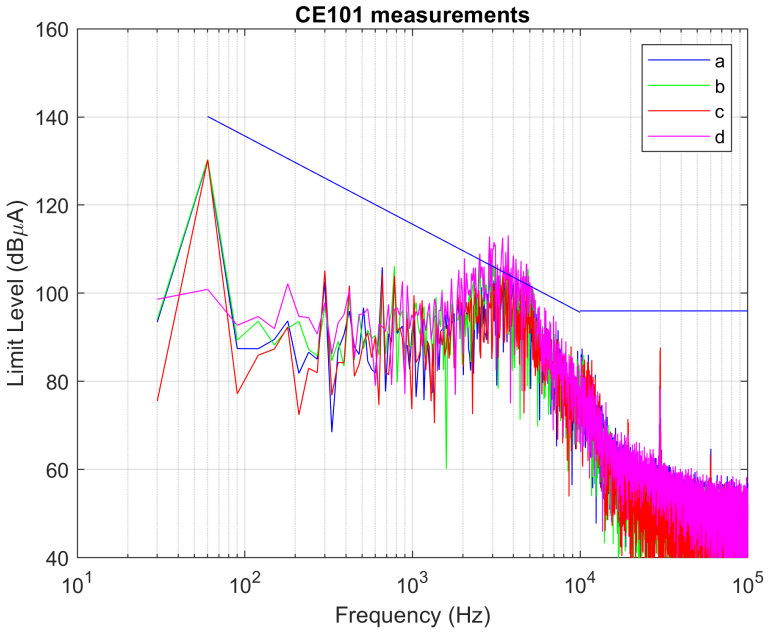

Figure 5.16. Experiment 11: MPC experimental measurement of LISN current spectrum.

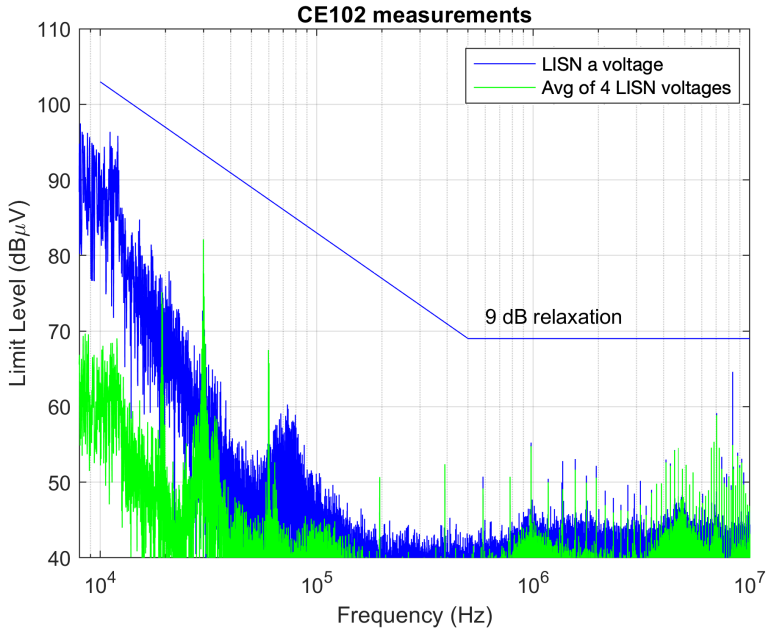

Figure 5.17. Experiment 11: ΔM experimental measurement of LISN voltage spectrum.

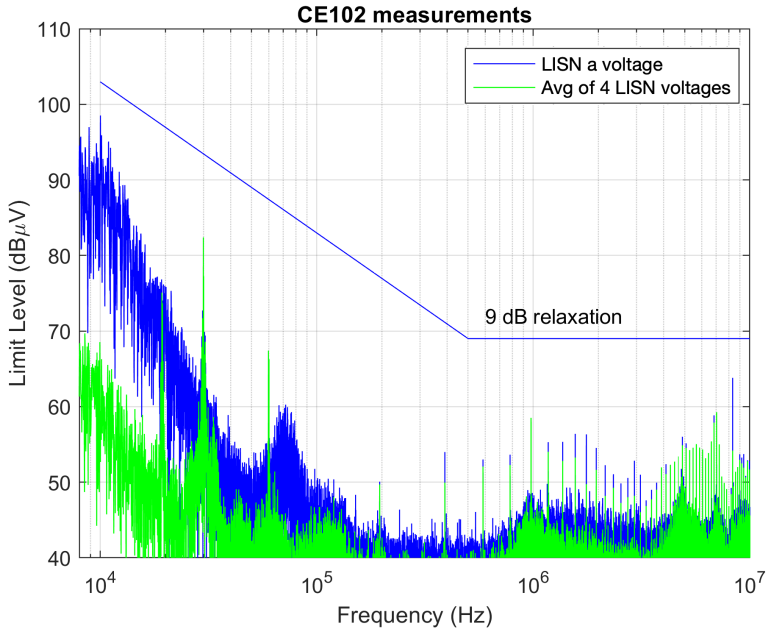

Figure 5.18. Experiment 11: MPC experimental measurement of LISN voltage spectrum.

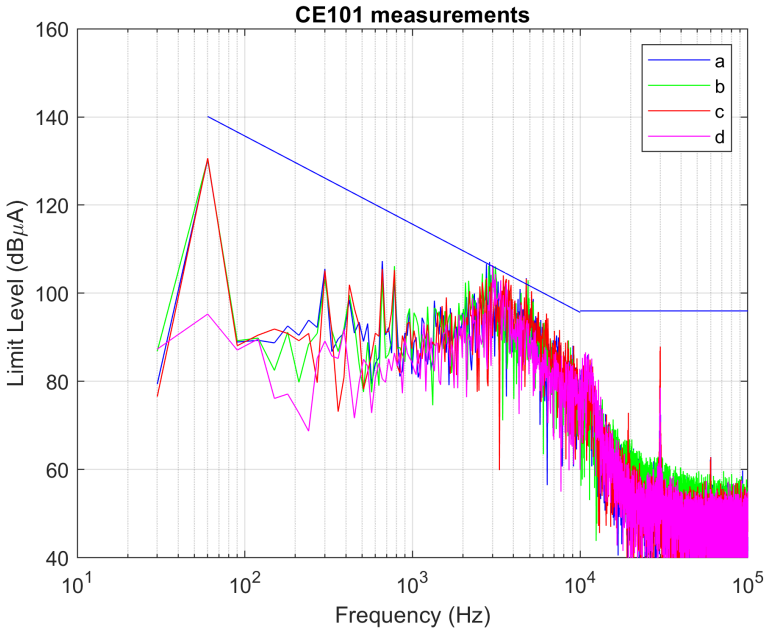

Figure 5.19. Experiment 12: ΔM experimental measurement of LISN current spectrum.

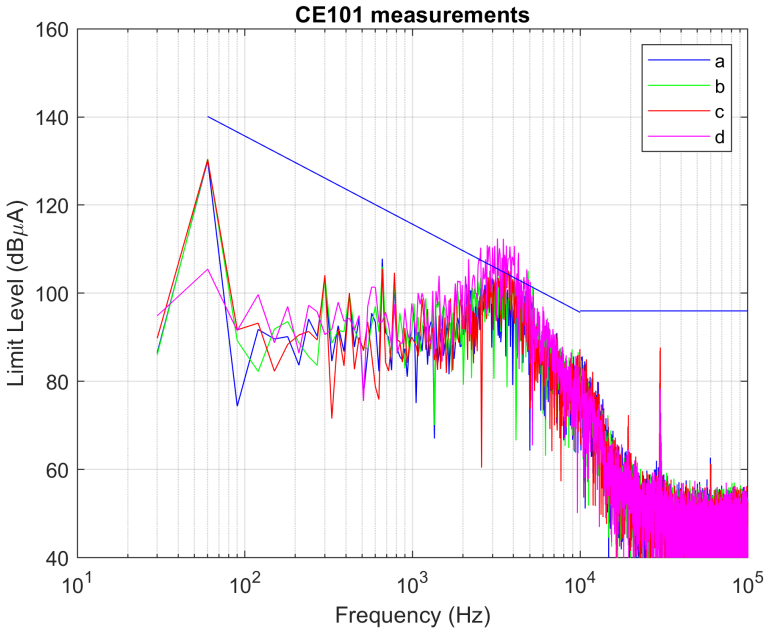

Figure 5.20. Experiment 12: MPC experimental measurement of LISN current spectrum.

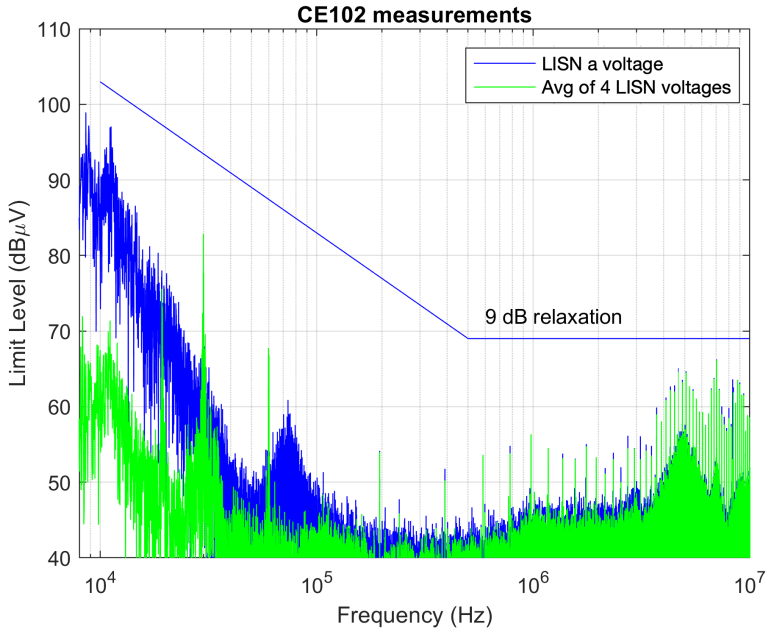

Figure 5.21. Experiment 12: ΔM experimental measurement of LISN voltage spectrum.

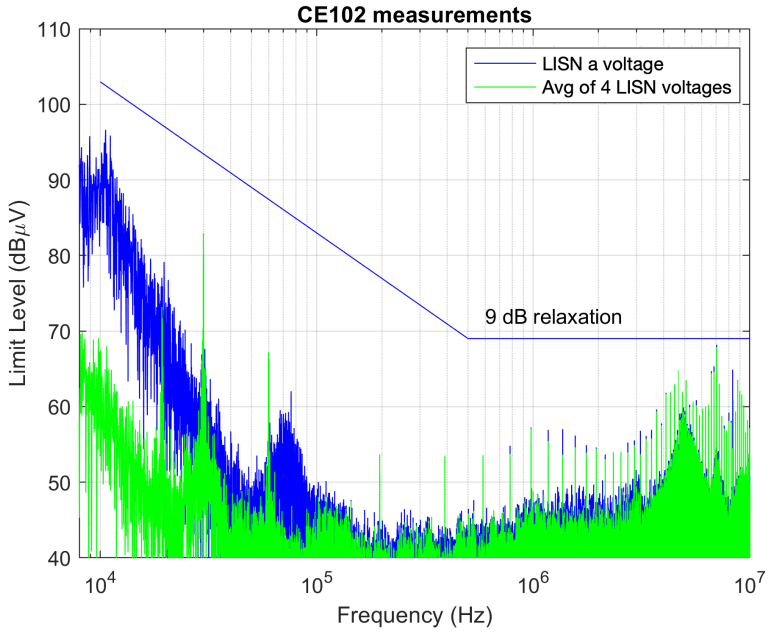

Figure 5.22. Experiment 12: MPC experimental measurement of LISN voltage spectrum.

CHAPTER 6:
CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

This thesis illustrates the effectiveness of reducing CM EMI in four-leg three-phase grid-connected inverters through control methods utilizing PDM; MPC and ΔM. Physics-based modeling, analysis and the experimental measurements on a laboratory hardware prototype have shown that both MPC and ΔM methods can mitigate CM EMI to within the limits of MIL-STD-461G, thus eliminating the need for large CM chokes designed for EMI in the switching frequency range. This result is important for shipboard power converters because meeting the strict limits imposed by MIL-STD-461G [4] without a full-size CM choke or large bypass capacitors could lead to significant size and weight reduction of the power conversion system. The experiments presented in this thesis also demonstrate that, although the higher frequency CM EMI are not suppressed by the proposed control strategies, they can be easily reduced by small and inexpensive off-the-shelf passive filters such as CM chokes and small bypass capacitors.

The thesis also presents a discrete novel algorithm to replace the arc tangent 2 function in MPC. The proposed solution employs a simple seven-entry lookup table and is build utilizing discrete Simulink blocks. This novel function reduces the complexity and need to use the provided discrete atan2 Simulink block, which, when compiled using MATLAB HDL coder requires the use of integrators to process and exhaustive lookup table or convergence through the use of the CORDIC method. The use of an integrator introduces the need for extra clock cycles in the Verilog code and can become computationally heavy for the FPGA.

6.2 Future Work

The integration and utilization of three-phase inverters onboard Navy vessels and throughout the DOD continues to increase as technology advances. The ability for electronic equipment to meet the requirements of MIL-STD-461G while providing reliable Type I power, in accordance with [2], is paramount to mission success and lethality of the force.

Future work, that builds upon the research presented in this thesis, could include the modeling and verification through hardware testing, of the ability of MPC and ΔM to eliminate CM EMI in various other operating conditions. This thesis focused on the four-leg inverter topology operating in grid-following mode while supplying current to a constant DC load. Different loading conditions should be tested as well as other grid-following modes of operation such as those in which the inverter supplies current to AC loads under balanced and unbalanced conditions. This last mode requires the addition of the BESS or other energy resource on the converter DC side, with the addition of another power conversion stage. For the BESS a DC-DC converter is necessary to regulate the DC bus and its switching behavior will add more EMI to the system. To fully characterize a grid-following power conversion system, all components should be added and the measurements repeated under all operating conditions and loads.

Future work could also include expanding the physics-based model to include higher order effects, such as blanking time, and more parasitic components so that the CM EMI in the upper frequency ranges can be accurately predicted in simulation. A model that predicts the exact EMI measured in the laboratory hardware would be very valuable in reducing the time to design EMI filters and future control systems.

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