ONR Biannual OSPRES Review and Technical Exchange

Grant No. N00014-17-1-3016

Distribution Statement A. Approved for public release: distribution unlimited

November 15, 2021

PI:
Anthony Caruso
Missouri Institute for Defense and Energy
University of Missouri-Kansas City
816-235-2505
carusoan@umkc.edu

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*
15-11-2021

2. REPORT TYPE
Technical Summary

3. DATES COVERED *(From - To)*
June 2021 – November 2021

4. TITLE AND SUBTITLE

ONR Biannual OSPRES Review and Technical Exchange
Fall 2021

5a. CONTRACT NUMBER

5b. GRANT NUMBER
N00014-17-1-3016

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
Roy Allen, Wasekul Azad, Bidisha Barman, Steven Bellinger, Jordan Berg, John Bhamidipati, Gyanendra Bhattarai, Sadie Brasel, Deb Chatterjee, Justin Clark, James Currie, Kalyan Durbhakula, Jay Eifler, Spencer Fry, Nicholas Gardner, Mohamed Hamdalla, Ahmed Hassan, Megan Hyde, Sai Indharapu, Faisal Khan, Noah Kramer, D. Noor, Kasey Norris, Thomas Ory, Michelle Paquette, Sourov Roy, Scott Shepard, Sarvenaz Sobhansarbandi, Heather Thompson, Alexander Usenko, Lars Voss, Anthony Caruso

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

University of Missouri-Kansas City
5100 Rockhill Rd.
Kansas City, MO 64110

8. PERFORMING ORGANIZATION REPORT NUMBER

OSPRES_Grant_Biannual_Review_NOV2021

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Office of Naval Research
One Liberty Drive, 875 N. Randolph
Arlington, VA 22203

10. SPONSOR/MONITOR'S ACRONYM(S)

ONR

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT

Distribution Statement A. Approved for public release: distribution unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

The ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study (OSPRES) (Grant Award No. N00014-17-1-3016) Fall 2021 biannual review was held co-incident with the Directed Energy Professional Society (DEPS) Systems Symposium on 29OCT2021 in Washington D.C. This report captures 19 sub-project abstracts, posters, and an executive summary of the event. The program objective is to execute high-risk, high-payoff efforts that mitigate, fill, or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable, and electronically steerable high power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average power space, and includes the kill chain considerations including the target and its responsivity to radio frequency stimuli. Poster presentations covered all of the program's ongoing subprojects spanning prime power, laser alternatives, pulsed power switches, photo switches, pulse forming networks, thermal management, antenna design, and RF coupling

15. SUBJECT TERMS

Pulsed Power Switches, High Power Microwaves, Pulse Forming Networks, Antennas, Arrays, RF Coupling, High Voltage

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Anthony Caruso
U	U	U	UU	49	19b. TELEPHONE NUMBER *(Include area code)* 816-235-2505

Reset

Standard Form 298 (Rev. 8/98)
Prescribed by ANSI Std. Z39.18

1. Table of Contents

2. Administrative

2.1. Program Overview

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

OSPRES Grant Goal: address and transition technologies and capabilities that enable the OSPRES Grant Objective using the OSPRES Grant Approach, while educating the next generation of pulsed power and defense minded, stewards, and innovators.

OSPRES Grant Objective: to execute high-risk, high-payoff efforts that mitigate, fill, or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable, and electronically steerable high power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average power space, and includes the kill chain considerations including the target and its responsivity to radiofrequency stimuli.

OSPRES Metrics of Success: developed technologies and capabilities that are published in the peer review, protected as intellectual property, and/or transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use, as enabling/integratable capability(ies).

OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

OSPRES Grant Security: All efforts should be fundamental and publically releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

2.2. Executive Summary

Scope of Report

The ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study (OSPRES) (Grant Award No. N00014-17-1-3016) Fall 2021 Biannual Review was held co-incident with the Directed Energy Professional Society (DEPS) Systems Symposium on 29OCT2021 in Washington D.C. This report captures the sub-project abstracts, posters, and an executive summary of the event.

The key results and significant impact from the ongoing sub-projects are as follows:

High-Voltage Switch (Azad, Khan)

During the last six months, the MIDE team has developed multiple versions of a custom HV switch that can function as an alternative to the commercial BEHLKE switches in terms of matched performance, reduced cost and greater availability; ruggedness has not been addressed. To this end, a modular series-connected SiC MOSFET architecture has been fabricated with a custom isolated gate driver and precision voltage balancing sub-circuit in the 10-kV and 1-kV/ns class. The voltage balancing method achieves <1.1% voltage mismatch under steady-state and switching transitions.

Fiber Laser (Shepard)

Optical fiber amplifiers are a promising technology for reducing the cost, weight, and size of the laser systems that trigger photoconductive semiconductor switches (PCSS) in directed energy systems. Simulations show that a tubular-core optical power amplifier provides two orders of magnitude improvement in output power over the state-of-the-art circular core fiber lasers from geometric factors alone; further, we discovered a symmetric breaking and accumulation effect which traps energy (which otherwise would be lost via nonlinear scattering) into an air-core mode. Advancements in the very high-power operating point (tens of GW) of our tubular optical amplifier (and the existence, size, and spatial uniformity of its air-core mode) permit a single laser to trigger an array of several (up to 100) silicon PCSSs, reducing the laser system cost and eliminating the optical timing jitter constraint.

Photoconductive Semiconductor Switch (PCSS) Enabled Optical Source Driver (Bhamidipati)

To implement the enabling switch in a multi-stage optical source driver, capable of high current (120-A) and fast rise-time (<200-ps), PCSS and non-PCSS switch technologies are being explored. Based on the target form factor of the subsystem, operating voltage (<50-V), and current requirements (~120-A) of the optical source, a need for a gain-capable switch in the first stage has been determined. PCSS switch technologies such as Si optodiodes and gallium nitride PCSSs are being evaluated to determine their ability to achieve the rise-time and current metrics. Thus far, <350-ps rise time and <15-A output current have been demonstrated experimentally through Si- and GaN PCSSs. We continue to study GaN-PCSSs theoretically to understand factors contributing to avalanche (current gain) conduction and in parallel experimentally evaluate electrically triggered switch technologies to determine their ability to meet the target metrics. Due to lack of promising results and it not residing on the critical path, it is likely that this sub-project will be sunset before the end of CY2021.

Minimizing On-state Resistance in GaN:C PCSS (Thompson)
Towards maximizing GaN:X PCSS efficiency through parameter optimization, on-state resistance measurements were done to determine how incident wavelength and optical pulse energy affect efficiency. It was found that it is not possible to take advantage of midgap energy states, with reduced activation energy, so using a compact, commercially available diode laser below bandgap energy is not an option. Also observed was a saturation point where increasing photon flux does not yield greater efficiency or reduced on-state resistance; this analysis serves as a starting point for optimizing GaN:X PCSS gap length and incident optical pulse energy/wavelength based on needed operating voltage for minimized material and optical energy waste.

TCAD Optimization of DSRDs and Pulser Performance (Eifler)
Using TCAD, optimal drift-step recovery diode (DSRD) doping profiles have been established within DSRD-based pulser circuit topologies incorporating a SPICE MOSFET model developed and usable within TCAD. Also, an LTSPICE DSRD model (for use in LTSPICE) has been developed and tested that represents a significant improvement over earlier models. Together these simulation capabilities allow DSRD-based pulser systems to be better designed and optimized (without adjustments the new LTSPICE model is 1.6 times more accurate than the old one) for peak power and rise time performance metrics.

New Process Flow for Fabricating Drift Step Recovery Diodes (DSRDs) (Usenko)
To push beyond the pulsed power performance limitations of state-of-the-art DSRDs, we have developed a new fabrication scheme based not on traditional deep dopant diffusion, but rather a modern epitaxial technique that results in an optimal doping profile. The resulting estimated improvement in pulse rise time on a load is from current 10^{12}–10^{13} V/s. Additionally, we integrate a new sidewall passivation scheme, specifically a beveled side passivated with a partially oxidized porous silicon layer. Compared to the SOTA vertical sidewalls, which exhibit avalanche surface-limited breakdown at ~10^4 V/cm, our diodes are expected to withstand an electrical field approaching bulk Si electrical breakdown of 3×10^5 V/cm.

Augmented Design of Experiment for DSRD Evaluation (Hyde)
Standardized testing procedures have been developed to evaluate several drift step recovery diodes (DSRDs) to provide a baseline for diode selection in the pulser circuit. The range of turn-on values for the 7-stack deep diffusion DSRDs are 1.5 to 2 V, which is lower than expected since a silicon diode has a typical turn-on voltage of 0.7 per stack. Another example of a deviated measurement includes the zero-junction bias capacitance, where the average of 7-stack DSRDs is 0.46 nF compared to the measured average of 0.66 nF from previous studies. This first round of data has exposed several areas needing improvement in the current process, including the need for a repeatability and reproducibility study, to bolster confidence in the calculated results.

DSRD-Based Pulse Generator Systematic Topological Optimization (Roy)
Pioneering beyond the SOTA of air-cooled inductive energy storage and release pulse generators, the “4×2” permutation of the DRSD-based pulser topology demonstrates a time-aligned parallel–series-stage power-combining and pulse-compression circuit that produces ones-of-megawatts of power at hundreds-of-kilohertz repetition rate. Driven by a single gate driver (trigger input) and a DC booster stage, the 4×2 pulser meets/exceeds the PCSS source performance parameters at a lowered procurement cost through omitting the laser and cooling requirements, while not being limited by the laser PRF. Through demonstration of frequency agile capabilities, the DSRD pulser energy storage time is modulated to achieve frequency waveform

tuneablity in real-time, improving its wholistic capabilities as a threat-agnostic HPM source suitable for Naval afloat ground-based air-defense mission.

All-Solid-State High-Power Pulse Sharpeners (Bhattarai, Gyanendra)
High peak-power pulse production and sharpening, via hydrogen spark-gaps (HSG), inductive energy storage (IES) methods, diode-nonlinear transmission line (DNLTL) networks, magnetic compression lines (MCL), solid-state sharpeners, and photoconductive solid-state switches (PCSS), have been reviewed and compared based on their size, peak voltage, peak power, risetime, pulse repetition rate, and device/shot lifetime. Only a subset of technologies, HSG, IES + MCL, and IES + solid-state sharpeners have been identified as capable of producing >1 GW and sub-nanosecond pulses. While HSG are easily available, their gas-based operation is intrinsically large volume with limited ion-electron recombination, resulting in low PRF and electrode wear; whereas the IES power supplies (based on semiconductor opening switches) with magnetic compression line or semiconductor sharpeners are still in the research phase and have shown comparable SWAP performance metrics. The semiconductor components, such as semiconductor opening switches (SOS) and silicon avalanche sharpeners (SAS) used on these 'IES + sharpener' systems are not available to purchase within the United States.

Computational Intelligence-Design of Effector Systems (Currie)
From antenna development to circuit topology optimization, machine learning (ML), intimate with parameter space studies, can overcome human developed limitations. Such outcomes are manifest in conversion efficiency (>1.5 to 2x). In this effort, we have applied Genetic Algorithm to study the antenna configuration space subject to macro-properties, and combinations of macro-properties of the resulting antenna. This effort is computationally expensive and will require many thousands of CPU hours. In addition to providing an optimal antenna solution, tracking the generational progress of the algorithm will improve intuition into the solution space, a diverse set of training data for future ML efforts, and potentially non-obvious antenna geometry solutions.

Jet Impingement Thermal Management (Berg, Sobhansarbandi)
The high average power of the PCSS system requires low ones-of-kW thermal transfer per cm^2, a major feat for any state-of-the-art heat transfer technology/methodology. Jet impingement (JI) was rigorously studied as a thermal management system (TMS). Computational fluid dynamics (CFD) modeling and experimental analysis of the JI-TMS was performed, showing that the device temperature was maintained well below the maximum desired operating temperature (57.5 °C when using 0.06 kg/s) for 100 W of power. However, for the 200 W average power simulation, the device temperature exceeded the thresholds. Therefore, to increase the performance of the system, the project aimed to develop a nanofluid by entraining ceramic nanoparticles and dispersants within the dielectric base-fluid to increase the thermophysical properties of the nanofluid and cooling density capabilities. The results from CFD modeling showed a 18.8% and 14.9% drop in maximum semiconductor temperature by utilization of 0.25 wt% mixture of silicon carbide with surfactants. These results have been captured in the MS Thesis of Mr. Berg.

Ultra-Compact Cooling System (Clark, Sobhansarbandi)
Geometry and microchannel techniques for the ultracompact cooling system were thoroughly reviewed based on manufacturing tolerances and techniques. A preliminary design consisting of an array of 421 nozzles and 22 microchannel heat sinks embedded onto a semiconductor was devised, following early simulations in ANSYS. The large number of micro-scaled nozzles yielded poor mesh quality, leading to individually face sizing certain bodies within the 3 x 3 mm concept. A high quality mesh simulation will be performed to achieve a heat dissipation rate of 1 kW/cm^2.

Diode-Based Non-Linear Transmission Line (Gardner)
Two D-NLTLs previously shown to be capable of single MW peak power generation and max frequency generation in the L-Band (1–2 GHz) were tested with four pulsed sources of varying rise time, full width at half max, and amplitude. Further, Each D-NLTL demonstrated center frequency generation in the ultra-high-frequency band (0.3–1 GHz). While operation is still limited in conversion efficiency due to non-linear phenomena present in the network, generation of multiple solitons by each D-NLTL represents a first of its kind measurement at MW peak powers.

Electrically Small Antenna (ESA) Arrays (Barman, Chatterjee)
An electronically steerable antenna array in the ultra-high-frequency (UHF) band requires an aperture size that is deemed 'reasonable' by the end user, which in most cases means reducing the size of a classic UHF aperture to at least 60% of its area. In this work, the tradespace of an array composed of wideband, microstrip patch, ESA elements, that are optimized via machine learning (ML) algorithms is evaluated as a function of the antenna performance metrics. A simulation study shows that with ~36% reduction in aperture area, the array gain drops by ~2.5 dBi, maintaining beam-steerability up to 60° from boresight, at the UHF range (640–990 MHz). As a first step to experimentally validate this design approach, a narrowband 2×2 array of microstrip ESA elements has been manufactured and tested, showing good agreement between the simulated and the measured S11-parameters at 900 MHz. Simultaneously, ML algorithms are found to be effective in optimizing array parameters with the objective of mutual coupling reduction between individual array elements. Future work involves showing continued high power (high voltage) operation of the arrays.

Ultra-Wideband (UWB) Antenna Arrays (Brasel, Indharapu, Durbhakula)
UWB array results so far demonstrate that state-of-the-art Vivaldi antennas can trade competitively with the alternative balanced Koshelev antenna. The new balanced Koshelev antenna design helps with achieving wider bandwidth and similar rE/V (compared to the unbalanced Koshelev antenna) without increasing the footprint. We have found the performance of the Shark antenna to drop at a faster rate than the Koshelev antenna with an equivalent reduction in physical aperture area. Our well-trained machine learning models in conjunction with search optimization algorithms were found to be accurate and faster in predicting the metrics of UWB antenna design with reduced physical aperture area.

RF Coupling (Hassan, Hamdalla)
The RF coupling effort has made a major step forward by generating equivalent circuit models for generic UAV wires/PCB layouts to determine the extent to which coupling is affected by factors such as the distribution of the wiring system, the characteristics and the impedance of the linear/nonlinear devices attached to these wires, and the environment in which the wires/devices are embedded. The equivalent circuit models allow us to simulate RF coupling using circuit solvers that are orders of magnitude faster than full-wave simulations. Using these equivalent circuit models, we answered key questions such as "What matters most: traces/wires or the devices? Is it the wires/traces or the devices that control the coupled voltage and power to a specific load under test in a practical system?" Moreover, we integrated our modeling framework into a user-friendly package called Predictive-Package for Electromagnetic Coupling to Nonlinear-Electronics using Equivalent-Circuits and Characteristic-Modes (PECNEC), which can be integrated with higher level models for an overall effects prediction capability at the OSPRES Contract and greater level.

3. Abstracts

3.1 A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Architecture for Pulse Power Applications

W. Azad, F. Khan, S. Roy, S. Fry, and A. N. Caruso

Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO

Commercially available high-voltage solid-state switches made by BEHLKE are the best in SWaP-cooling, but are expensive, have long lead times (2–3 months), and are made outside of the US. For the Navy afloat mission to be successful, we need a sustainable supply of US-manufactured switches at a much lower cost. During the last six months we have fabricated and tested several versions of a replacement modular switch that can achieve high-voltage (~10 kV) and fast (repetition frequency = 100 kHz) switching using a combination of series- and parallel-connected commercially available inexpensive discrete SiC MOSFETs and custom high-voltage (~10 kV) isolated gate drivers. Key challenges were voltage balancing among the series-connected MOSFETs, minimization of gate signal delays, cooling of the individual MOSFETs, balancing resistors, high-voltage isolation required for the power supplies, and the controlling pulse width modulated (PWM) signal as well as differential voltage feedback measurement across individual MOSFETs. The proposed modular high-voltage switch is expected to facilitate controlled hundreds-of-nanosecond charging of an array of transmission lines of pulse forming networks to drive an array of photoconductive semiconductor switches (PCSSs), thereby producing controlled hundreds-of-picosecond scale high-voltage pulses. A modular (two modules) 10 kV rated HV switch has been designed and a prototype has been developed using 1.7 kV rated SMD SiC MOSFETs (C2M1000170J). An in-house 10 kV rated HV gate driver has been designed and incorporated with the HV switch to drive it. The switch has been tested at 6 kV, and it can safely handle the voltage. The proposed voltage balancing method achieves <1.1% voltage mismatch under steady-state and switching transitions. However, testing the voltage withstanding ability of the modular HV switch with a DC supply voltage up to 10 kV and switching frequency up to 50 kHz using a resistive load (5–10 kΩ) and evaluating the effectiveness of the thermal management at its current state is still ongoing as we have had failures at voltage levels higher than 6.4 kV. A new 10 kV gate driver board with radically modified design has been fabricated and tested in September 2021. A new optical fiber link and driver circuit has been used and bigger spacing between transmitter and receiver has been introduced to enhance the breakdown voltage. A manuscript on the HV switch and the custom isolated gate driver has been submitted to IEEE Transaction on Power Electronics.

The biggest problem with the 10 kV design is the voltage breakdown at different locations on the PCB. Through literature study and HV product research, it was evident that a suitable potting material or dielectric oil applied to both sides of the PCB may prevent arcing and provide necessary voltage breakdown ability. We have explored literature for a liquid di-electric material to achieve necessary breakdown ability. So far, an insulating naphthenic dielectric oil has been acquired that meets the ASTM D-3487 specification. The entire MOSFET PCB and the gate driver PCB will be immersed inside this oil to test the circuit at 10 kV. This application of dielectric oil will enable us to continue the alterations without compromising the voltage withstanding capacity. Once the circuit will be fine-tuned and finalized, proper potting materials instead of oil will be used in the final product. The selected dielectric oil can provide us a dielectric strength of 30-40 kV, although the modified MOSFET board has performed flawlessly up to 300 V DC. The full capacity testing of the new board will be conducted in November 2021 using the dielectric oil.

3.2 Tubular Core Optical Power Amplifier

S. Shepard and A. Caruso

Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO

Optical fiber amplifiers are the most promising technology for reducing the cost, weight and size of the laser systems which trigger photoconductive semiconductor switches (PCSSs). Fiber amplifiers with cores of circular cross-section are rapidly reaching a fundamental limit in output power due to the conflicting constraints of thermal lensing (proportional to core area) and nonlinear impairments, such as stimulated Brillouin and stimulated Raman scattering (inversely proportional to core area). Rectangular-core fiber amplifiers radiate heat more efficiently as they have a larger surface area than a circular core of the same enclosed volume. Moreover, the thermal lensing should be limited by the smaller dimension of the rectangle while the larger dimension is permitted to increase in order to mitigate the nonlinearities.

We extend the advantages of the rectangular core into a tubular geometry, by considering a 2.5 mm outer diameter Yb doped tube of 100 micron thickness. Such dimensions permit standard manufacturing techniques yet also increase the surface area (hence the heat transfer) by a factor of 100 and increase the cross-sectional area (hence the nonlinear thresholds) by a factor of 204, with respect to a 50 micron circular-core fiber of the same unit length. In addition to the two orders of magnitude improvement over the SOTA from geometric factors, we discovered a symmetric breaking and accumulation effect which traps energy (which otherwise would be lost via nonlinear scattering) into an air-core mode. Advancements in the very high-power operating point (tens of GW) of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) were shown theoretically to permit a single laser to trigger an array of several (up to 100) Si-PCSS—reducing the laser system cost and eliminating the optical timing jitter constraint. Future work includes improving the output beam quality metrics (less uniform and more Gaussian-like in profile to improve far-field diffraction) for high-energy laser applications.

3.3 Photoconductive Semiconductor Switch Enabled Multi-State Optical Source Driver

J. K. P. Bhamidipati, R. Allen, M. M. Paquette, and A. N. Caruso

Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO

Acute optical pulse energy requirements in linear photoconductive semiconductor switch (PCSS) based HPM applications require high-average-power pulsed laser systems capable of delivering >250–300-μJ per pulse at sub-ns order pulse widths. Despite meeting the energy and pulse-width requirements, state-of-the-art laser systems—being heavy (~125 lbs.), bulky (~10 cu-ft), and expensive (~$120,000)—fall short of the SWaP-C^2 expectations/targets of the HPM systems. Furthermore, these are predominantly Nd:YAG based systems and are tuned to emit 1064-nm laser pulses, which creates an additional need for second and third harmonic generation (SHG/THG) optics to trigger wide bandgap (WBG) switches such as GaN- and SiC-PCSSs. The PCSS-based multi-stage optical source driver effort aims to reduce the size, weight, and overhead costs of the optical source subsystem by ~90%, and potentially circumvent the need for conventional lasers and SHG/THG optics. This is achieved by retrofitting a PCSS exhibiting persistent photoconductivity to function as a seed-laser-diode-driven lock-on switch to drive a high-power laser diode array (LDA) at ps–ns transients. GaN-PCSSs are considered a prime candidate for the LDA enabling switch, capable of switching ~120-A currents with <200-ps rise time. However, off-the-shelf Si-based PCSSs and optodiodes, and electrically triggered avalanche switches such as silicon avalanche shapers (SAS), avalanche transistors (ATs), and GaNFETs are additionally being evaluated as potential alternatives to GaN-PCSSs. Avalanche conduction is a necessary component for switch implementation to achieve the target output current and the form factor for the driver subsystem. In this report, the multi-stage LDA driver design and performance metrics in terms of pulse characteristics are presented along with the initial test results for GaN-PCSS and alternative switch technologies. Upon evaluation, Si-PCSSs and Si-optodiodes, despite their quick rise times, have been deemed unfit to be considered as alternatives to GaN-PCSSs due to their high on-state resistance. On the other hand, in-house testing of GaN-PCSS showed linear conduction at >3kV/cm sustaining fields contrary to the results from published literature. The factors contributing to this discrepancy will be studied theoretically through TCAD modeling and simulation so that the device model or test setup can be modified to demonstrate avalanche conduction in the near future.

3.4 Minimizing On-State Resistance in GaN:X Photoconductive Semiconductor Switches (PCSSs) for Direct RF Modulation

H. Thompson, M. Paquette, and A. Caruso

Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO

Compensated, semi-insulating gallium nitride (GaN:X) is a promising wide-bandgap material for use in applications requiring high operating power, frequency, and temperature, along with small form factor, such as RF generation using photoconductive semiconductor switches (PCSSs). Unfortunately, the immaturity of this material, compared to traditionally used materials (silicon, gallium arsenide, etc.), has limited the use of GaN:X, even as performance needs in such applications push up against the theoretical limits of traditional materials. One key performance metric for efficiency of PCSSs is minimizing on-state resistance during device operation, thus reducing on-state losses that decrease efficiency and lead to increased heating in the device. An important metric affecting not only on-state resistance, but also the overall system cost, is the wavelength of the incident photon source used to activate the PCSS. It was found that an incident photon source of <370 nm is necessary for device activation because above this wavelength there is a dramatic increase in on-state resistance when testing lateral, carbon-compensated PCSSs supplied by NRL. While not completely unexpected that wavelengths below the bandgap would increase on-state resistance, it was anticipated that photocurrent could still be generated by taking advantage of a thicker GaN:X layer (4 μm thickness versus previous PCSS at 1 μm) with incident optical source wavelengths of deeper penetration depths through exploiting midgap states. This finding eliminates the option of using a compact laser diode source in the 400 nm range, which would provide a small, cheap photon source in lieu of a large, costly laser setup with second and triple harmonic generation conversion to achieve incident UV energy.

Incident optical pulse energy, that is, the number of incident photons, is another important factor in photon source cost and size. In linear mode operation, each photon generates one electron–hole pair, so photocurrent is limited by the number of incident photons prior to saturation. For different gap lengths, there is a balance between achieving minimum on-state resistance, using the minimal amount of material possible, and operating at voltages below the material breakdown limits. For a lateral GaN:X PCSS with 500 μm gap length, the maximum theoretical operating voltage is approximately 0.15 MV, when considering the material's critical electric field and the PCSS gap length. It was found that there is no return on investment when using a more costly photon source to obtain incident optical pulse energies >~20 μJ at this gap length. This finding gives a starting point for PCSS geometry and incident optical pulse energy modifications based on needed operating voltages to minimize both material and optical energy waste. These findings, combined with additional experimental results, will be compared with simulation results to refine physics and models to more accurately model lateral devices.

3.5 TCAD Optimization of Epitaxially Grown Drift-Step Recovery Diodes and Pulser Performance

J. Eifler[1], S. Roy[1], M. Hyde[1], G. Bhattarai[1], J. Bhamidipati[1], A. Usenko[1], M. Pederson[1], M. Paquette[1], A. Caruso[1], S. Bellinger[2], L. Voss[3], and R. Allen[1]

[1]Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO
[2]Semiconductor Power Technologies, Manhattan, KS
[3]Lawrence Livermore National Laboratory, Livermore, CA

Drift-step recovery diodes (DSRD) and DSRD-based pulsed power systems must be maximized for peak power while maintaining ns-order DSRD rise times with additional considerations for compactness, low-jitter, cooling required, pulse-sharpening, and application-specific pulse repetition frequency goals. DSRD-based systems are competitive with photoconductive semiconductor switch (PCSS)-based systems but with the advantage of not requiring a heavy and expensive laser. Megawatt peak power and ns-order rise times have been achieved for state-of-the-art DSRD-based pulsed power systems employing DSRD stacks and parallel lines of DSRD to increase current. In addition pulse-sharpening of the DSRD-based pulser can be used, with 100-ps order rise times having been achieved. Simulation (within TCAD and SPICE) in combination with experimental results are used to optimize single-die and stack designs of DSRD within various DSRD-based pulsed power circuit topologies by altering the DSRD device parameters (geometry, doping, irradiation) and circuit component values of the pulser system. More accurate models for the DSRD and primary switch MOSFET within TCAD and/or SPICE have been developed and used for determining optimal DSRD doping profiles for optimal pulser performance based on in-house testing and/or datasheets when available. The optimal DSRD doping profile was determined to be exponential, have no basewidth to the low doped region, use a minimum doping of 5×10^{13} dopants/cm^3, and a junction placement of ~95 µm on a 170 µm thick device, which is most easily manufactured using epitaxy. The DSRD LTSPICE model developed represents a significant improvement over previous models and uses an automated parameter fitting scheme to fit device specific parameters. However, more advanced diode models will allow the DSRD model to more accurately represent experimental pulser results over a range of prime voltages and trigger durations not possible with standard diode models and measurements. Future work will use advanced diode models to improve the DSRD SPICE models for large-scale pulser design along with accurate, quick parameter fitting for the models and improved standard diode experimental testing.

3.6 New Paradigm in Fabrication of Semiconductor Opening Switches for Pulsed Power

A. Usenko[1], J. Eifler[1], S. Roy[1], G. Bhattarai[1], M. Hyde[1], M. Paquette[1], A. Caruso[1], S. Bellinger[2], L. Voss[3], and R. Allen[1]

[1]Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO
[2]Semiconductor Power Technologies, Manhattan, KS
[3]Lawrence Livermore National Laboratory, Livermore, CA

Drift step recovery diodes (DSRDs) and semiconductor opening switches (SOSs) are the base for fabricating pulse generators. These were first made in the 1960's using silicon, and the technology has not changed much since. It is still based on traditional power device processing—deep diffusion into thinned wafer. Thus, it is not surprising that both current and 60-year-old papers show nearly the same major pulsed performance specifications—about 1 nanosecond time for 1000 volt rise on a load. Meanwhile, modern mainstream silicon technology offers new solutions that can be successfully implemented to fabricate better diodes.

This presentation describes a DSRD/SOS process flow which includes several new processes that are currently used in mainstream silicon chipmaking. Deep diffusion is excluded from the process flow, and is instead replaced by a scheme that includes epitaxy, anisotropic etch, wafer bonding, and selective electroless metal deposition. The process starts from epitaxial growth of the n-side of the diode over a heavy As-doped wafer. The doping profile is controlled during epitaxy to form a grade according to the optimal profile predicted by simulation. Next the p-side of the diode is epitaxially grown with the predicted optimal grading. Replacing diffusion by epitaxy bring two advantages: it enables optimal doping profile thus better pulse performance, and it improves process repeatability die-to-die, wafer-to-wafer, and lot-to-lot. Individual diode dies are defined on the wafer by anisotropic etch in TMAH through windows in a lithography mask. Thus, the diode side surfaces are beveled, not vertical as in the traditional technology. This allows for an increase in diode breakdown voltage. The diode side surfaces are passivated by forming a porous silicon layer using a 1000:1 HF/HNO_3 etching solution at room temperature. This also increases breakdown voltage compared to the SOTA process with polyimide passivation of diode sides. Next is selective electroless metal Pd/Ni/Cu/Sn stack plating. Thus, ohmic contacts are formed on both sides of the wafers. Then the wafers are stacked and bonded by heating above the Sn melting temperature, forming a Cu/Sn intermetallic compound. Finally, the wafer stack is mechanically cut into stacked diode dies. Replacing die stacking by wafer stacking decreases number of stacking operations by 100 times or more, thus manufacturing costs are decreased. This new DSRD process integration scheme has been submitted for patenting. Potential advantages of this disruptive technology must be now proven experimentally through comparison of pulse performance with traditional DSRDs.

3.7 Development of an Evaluation Network for Drift Step Recovery Diodes through an Augmented Design of Experiment

M. Hyde[1], J. Eifler[1], G. Bhattarai[1], A. Usenko[1], S. Bellinger[2], S. Roy[1], R. Allen[1], J. Reeve-Barker[1], E. Bozarth[1], L. Voss[3], M. Paquette[1], and A. Caruso[1]

[1]Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO
[2]Semiconductor Power Technologies, Manhattan, KS
[3]Lawrence Livermore National Laboratory, Livermore, CA

Designing ideal inductive energy storage (IES) pulsers is hindered by the low technology readiness level of the drift step recovery diode (DSRD) used in the source. This is exacerbated by the lack of a performance evaluation methodology common between other commercially available diodes. The purpose of this study is to tie the performance metrics of the IES pulser to the fabrication designs of the DSRDs as well as to close the gap between the theoretical models and experiment through a continuously augmenting and evolving design of experiment (DoE). Presented are the results of electrical testing techniques on deep diffusion 7-, 13-, and 26-stack DSRDs. Standardized testing procedures have been developed and all the deep diffusion DSRDs have been measured with the current-voltage and the capacitance-voltage tests. The results of these tests exposed several challenges with the diode testing techniques, such as: the variability in measurements between similar DSRDs, interpretation of results, and the need for developing new methods outside of typical diode testing recommendations. Proper interpretation of these results will build the foundation for evaluating future generations of DSRDs, and the next steps will include a repeatability and reproducibility study for all techniques as well as a re-evaluation of the benefits and the limitations of all the current testing methods.

3.8 Systematic Topological Optimization of DSRD-Based IES Pulse Generator

S. Roy[1], J. Eifler[1], M. Hyde[1], G. Bhattarai[1], D. Noor[1], J. Bhamidipati[1], A. Usenko[1], M. Pederson[1], M. Paquette[1], A. Caruso[1], S. Bellinger[2], L. Voss[3], and R. Allen[1]

[1]Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO
[2]Semiconductor Power Technologies, Manhattan, KS
[3]Lawrence Livermore National Laboratory, Livermore, CA

Drift-step recovery diodes used in inductive energy storage (IES) pulse generators can produce ones of gigawatts in ones of nanoseconds. However, pulsers capable of these performance metrics are traditionally large (>1 m^3), bulky (i.e., >1000's of kgs), and incur order-of-magnitude reductions in volumetric power densities from their hundred(s) of MW/m^3 pulser counterparts. In this study, we present the systematic development of a modular IES pulse generator circuit's architecture to determine the optimal permutation of parallel-branches and series-connected stages which maximizes peak voltage/power without sacrificing the nanosecond risetime desired. Through a combination of numerical and experimental efforts, the optimal trigger length and bias voltage of a 1×1 and 2×2 pulser has been determined. Specifically, the 2×2 pulse generator achieved linear voltage gains of 40.8 which resulted in 1.08 MW pulses with 1.14 ns risetimes into a 50 Ω load. Additionally, for each of the five bursts measured, 100 of the 100 pulses acquired resulted in a 97.8% (2σ) standard deviation of peak voltage without the use of additional shapers/sharpeners as well as any thermal management system.

3.9 All Solid-State High-Power Pulse Sharpeners

G. Bhattarai[1], J. Eifler[1], S. Roy[1], M. Hyde[1], J. Bhamidipati[1], A. Usenko[1], M. Pederson[1], M. Paquette[1], A. Caruso[1], S. Bellinger[2], L. Voss[3], and R. Allen[1]

[1]Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO
[2]Semiconductor Power Technologies, Manhattan, KS
[3]Lawrence Livermore National Laboratory, Livermore, CA

Solutions for sub-nanosecond-risetime gigawatt pulsed power supplies are actively being sought for next-generation high-power microwave (HPM) weapons. Power supplies based on hydrogen spark-gaps and/or magnetic compression lines are poor on SWaP metrics and pulse repetition frequency (<2 kHz). Prototypes of all-solid-state power supplies incorporating semiconductor opening switches and semiconductor sharpeners have been reported to produce sub-nanosecond pulses reaching hundreds of MW. However, such power supplies are not available for purchase. While semiconductor opening switches have been developed for research purposes and are being tested, there are no reports of availability of the semiconductor sharpeners within the United States. This study will provide a roadmap/overview of our research to sharpen high-voltage, high-power (>1 GW) pulses to sub-nanosecond risetime and increase pulse repetition frequency to tens of kHz, through the utilization of semiconductor opening switches, such as the drift-step recovery diodes, and semiconductor sharpeners, such as silicon avalanche shapers, fast ionizing dynistors, and delayed impact ionization diodes, with the application of semiconductor switch design, simulation, and experiment. Within this research period, we have reviewed available research articles on semiconductor sharpeners and studied their reported performance compared to the available solutions based on hydrogen spark-gaps. Based on the physics of semiconductor sharpeners, we have hypothesized that semiconductor opening switches can also perform as the semiconductor sharpeners under a very high input voltage rise rate (>2–10 kV/ns) due to their structural similarity. We are currently exploring such alternatives using experimental drift-step-recovery diodes. In the future, we plan to optimize such sharpener structures using experiments and simulation using simulation package such as Silvaco TCAD. We will study the device performance as a function of device geometry, doping profile, and some specific deep level defects which are considered as the main sources of delayed impact ionization in semiconductor sharpeners.

3.10 A Machine Learning Approach to Antenna Optimization using Genetic Algorithm

J. Currie, K. Durbhakula, R. Allen, and A. Caruso

Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO

In the case of radiated electromagnetic fields where the ideal conditions are known, the optimal antenna geometry to produce that ideal is not always known. We propose a global search optimization approach using genetic algorithm techniques for antenna geometries of the biconical type. This differs from standard gradient descent techniques because the solution space is not guaranteed to be strictly convex. While the scope is narrowly focused on a particular antenna type, it can be extended to other types, or even arbitrary geometrical constructions. Further, because of the exhaustive nature of the optimization algorithm, each iterative step provides multiple datapoints (10's to 1000's) that may be used as training data for more advanced prediction models.

3.11 A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation

J. N. Berg[1], R. C. Allen[1,2], S. Sobhansarbandi[1]

[1]Department of Civil & Mechanical Engineering, University of Missouri-Kansas City, Kansas City, MO
[1]Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO

This study investigates the viability of a liquid jet-impingement (JI) thermal management system (TMS). The JI-TMS was used as a heat dissipation tactic to ensure the temperature of a silicon semiconductor-based pulse-power device was maintained below 80 °C during operation; Otherwise, a large amount of heat gain may result in device degradation or thermal runaway. The JI-TMS design, which is comprised of 27 nozzles (1 mm nozzle diameter), is analyzed by computational fluid dynamics (CFD) modeling, with 100 W and 200 W of average power (i.e., heat generation rate). The heat transfer fluid (HTF) is pure silicone fluid with a viscosity of 20 cSt. The selected HTF has a dielectric constant which provides better electrical insulation than other common HTFs (water, water–glycol, etc.). Validation of the model was performed experimentally to ensure the accuracy of the CFD results. The results show that the temperature of the semiconductor device is maintained well below the maximum desired operating temperature (57.5 °C when using 0.06 kg/s), showing average deviation of 5.89% and 0.99% between numerical and experimental data for the 100 W and 200 W average power tests, respectively. To better understand the measured error, heat capacity analysis of the HTF was investigated by differential scanning calorimetry, which shows an average deviation of 13% with the reported vendor value. The results from this study can be a benchmark for cooling purposes of semiconductor devices in high power densities.

3.12 Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures

J. N. Berg[1], R. C. Allen[1,2], S. Sobhansarbandi[1]

[1]Department of Civil & Mechanical Engineering, University of Missouri-Kansas City, Kansas City, MO
[2]Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO

Dielectric fluids (non-conductive coolant) used in thermal management systems (TMS), while suitable for pulsed-power applications, possess inherent thermophysical fluid properties (low thermal conductivity, high viscosity) that inhibit their ability to achieve >1 GW/m^3 cooling densities. To overcome the poor thermophysical properties of dielectrics, this project aims to develop a nanofluid by entraining ceramic nanoparticles and dispersants within the dielectric base-fluid, pure silicone fluid (PSF), to increase the nanofluid thermophysical properties and cooling density capabilities. Adding nanoparticles may increase the thermal conductivity of the nanofluid, but may result in increased viscosity, i.e., the heat removal rate may increase, but so will the required pumping power along with it. Therefore, the optimal nanoparticle-to-fluid ratio and specific nanoparticle type for the TMS needs to be identified and optimized with an attempt to maintain the viscosity of the mixture as low as possible. Three different ceramic nanoparticles were chosen to be studied: alumina, silicon carbide, and iron (II,III) oxide. Ceramics were chosen to maintain the heat transfer fluid (HTF) dielectric properties. Of the 18 samples tested with different nanoparticle concentrations, the sample that showed the greatest heat capacity decrease was chosen (which is 0.25 wt.% silicon carbide with surfactant), as theoretically, the largest heat capacity decrease correlates with the largest thermal conductivity increase. In order to investigate the performance of the semiconductor, the achieved thermophysical properties of the selected nanofluid was applied into computational fluid dynamics (CFD) modeling software, which resulted in a significant drop in the semiconductor temperature. By applying the measured thermal conductivity of the sample, the results from CFD modeling show a 18.8% and 14.9% drop in maximum semiconductor temperature. The results from this study show that a significant heat transfer enhancement of the TMS is achievable using a small mass fraction of nanoparticles in the heat transfer fluid.

3.13 Ultra-Compact Integrated Cooling System Development

J. T. Clark[1], R.C Allen[1,2], and S. Sobhansarbandi[1]

[1]Department of Civil & Mechanical Engineering, University of Missouri-Kansas City, Kansas City, MO

[2]Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO

Silicon semiconductor-based devices are suitable for use in pulsed-power applications, however generate a significant amount of power (i.e., heat) that must be dissipated. A thermal management system (TMS) is required to maintain the semiconductor device temperature below 80 °C during continuous operation to avoid device degradation or thermal runaway. The ambitious end goal is to create an ultra-compact cooling unit integrated on a semiconductor switch, with the ability to remove 1 kW/cm^2 of heat in a short time frame with minimal pumping power. To achieve such high heat flux, a turbulent flow profile must be achieved. The pumping power will be kept to a minimum since the unit to be prototyped will represent 1 cm^2 surface area. This enables less power to be consumed to create a turbulent flow. An array of micro-sized jet nozzles will provide a turbulent flow onto a microchannel section directly on the semiconductor device. The objective will be reached as the micron scaled cooling unit is to be integrated onto a semiconductor device, letting more heat extraction occur. Micron-scaled manufacturing constraints led to an optimal design using a 1 cm^2 Si-based unit, implementing microchannel and jet impingement cooling technologies. This study compares the viability of the compact microchannel and jet impingement TMS to facilitate the long-term operation of semiconductor devices for high-power applications through performing computational fluid dynamic (CFD) simulations in with ANSYS Fluent. The application of the ultra-compact system proposed in this study will benefit current cooling technologies significantly by cutting the volume, weight and power required to cool high voltage power semiconductor devices.

3.14 Diode-Based Nonlinear Transmission Lines Capable of GHz Frequency Generation at Single MW Peak Powers

N. Gardner, R. Allen, S. Roy, N. Kramer, T. Ory, M. Paquette, and A. Caruso

Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO

The environment aboard a naval vessel necessitates reductions and optimizations in the size, weight, and cost of all systems including those aimed at generating high power RF and microwave content. Diode-based nonlinear transmission lines (D-NLTL) represent a semiconductor-based approach to generating high power microwaves (HPM) in a compact, low cost, low weight design. D-NLTLs are pulse shaping networks (PSN) capable of taking a pre-generated excitation pulse and shifting energy to higher frequencies by breaking the pulse into a sequence of solitons. While D-NLTL devices have achieved center frequencies and maximum frequencies greater than 1 GHz, peak powers greater than 1 MW have yet to be documented due to the low reverse bias hold off potentials of commercially available devices. Two diode models, K50F and K100F, have been identified as possible GHz MW candidates due to large hold off potentials of 6 kV and 12 kV respectively. Two D-NLTL prototypes were constructed, each consisting of 20 cells and either a single K100F model diode in reverse bias or two K50F diodes in series in reverse bias. Results are presented for both D-NLTL prototypes tested with excitation pulses provided by a series of sources: a drift step recovery diode (DSRD) based source, a photoconductive semiconductor switch (PCSS) based source, a Marx generator, and a Megaimpulse pulser. Each prototype produced peak powers up to 1.6 MW, max frequencies of up to 1.6 GHz, and successfully broke waveforms into sequences of solitons with center frequencies in the ultra-high frequency (UHF) regime. Multiple sources are used to demonstrate the effect of excitation pulse geometry on D-NLTL behavior. Results are significant as they represent a newly documented ability of D-NLTLs to generate both MW power and UHF to L-Band frequencies. Future work is focused on achieving a L-Band center frequency as well as achieving electrical or mechanical tuning on a MW D-NLTL.

3.15 Tradespace Analysis of a Phased Array of Microstrip Patch Electrically Small Antennas

B. Barman, K. Durbhakula, D. Chatterjee, and A. Caruso

Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO

High power microwave (HPM) systems are currently envisioned as viable alternatives to conventional kinetic warfighting weapons, due to their capability of producing electromagnetic waves harmful to electronic equipment. The goal of an antenna array, in this application framework, is to deliver effective radiated power (ERP) (in 100s of MW) onto a specified angle in space, to achieve a required power density. The state-of-the-art (SOTA) ultrawideband (UWB) antenna elements used for HPM-capable antenna arrays include horn, reflector, Vivaldi, and Valentine antenna elements. However, all these elements have the common disadvantage of large physical aperture area (Ae). The primary objective of this work is to determine the extent to which the physical aperture area of an antenna array, composed of electrically small antenna (ESA) elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz). A novel wideband, coaxial probe-fed, microstrip patch, ESA element design method, having ~35% impedance bandwidth, has been proposed and experimentally validated at 2.5–5 GHz. Regular and machine learning (ML) based stochastic search algorithms are employed to further optimize the antenna bandwidth. Comparison of the ESA element designed using the proposed methodology at 900 MHz, with the Koshelev, Shark and U-slot antennas, shows that the proposed antenna occupies the least volume, yields higher gain (5 dBi at 900 MHz), with comparable bandwidth (~340 MHz) and rE/V (~0.9) values. Tradespace analysis of the arrays, composed of the proposed wideband ESA elements, on various lattice arrangements, shows that with ~36% reduction in Ae (which is equivalent to 50% element reduction), the gain drops by ~2.5 dBi, with no scan blindness observed between 0 to 60°.

3.16 Efforts to Reduce Physical Aperture Area of Ultra-Wideband Arrays

S. Brasel, K. Norris, R. Allen, A. Caruso, and K. Durbhakula

Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO

Ultra-wideband (UWB) arrays are the primary choice for radio frequency (RF) systems with a requirement to radiate short rise time pulses at high microwave power. However, the physical aperture area of a volumetric UWB array is enormous and can take up a lot of real estate on the platform. The balanced antipodal Vivaldi antenna (BAVA) is the state-of-the-art (SOTA) antenna element due to its exceptional 20:1 impedance bandwidth ratio and ability to handle tens-of-MW input power. A two-fold objective-oriented approach has been developed to achieve a reduction in physical aperture area: (1) Identify and study performance characteristics of UWB antennas (single element) that have been minimally explored or understood in the literature to find an optimum set of design parameters. (2) Select the optimum UWB single element and scale up the single element into various array topologies to identify the array with minimum aperture area while retaining expected performance. Two specific antennas, namely, the Koshelev antenna and the Shark antenna, have been down-selected and studied for the aperture area reduction as described in the two-fold process. We found that non-square antenna array geometries would reduce the physical aperture area up to 50% while only losing an average of 1–3 dBi of peak gain and <5% of aperture efficiency. The time-domain electric field response from the Koshelev antenna array and the Shark antenna array is more sensitive to spacing in the H-plane than in the E-plane. In summary, two unique antenna elements have been extensively studied and achieved at least 50% reduction without a significant decrease in the array metrics. Future work involves 3D printing, metalizing, and testing the optimized antenna array geometries.

3.17 Machine Learning Based Ultra-Wideband Antenna Array Optimization and Prediction

S. Indharapu, A. Caruso, and K. Durbhakula

Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO

Ultra-wideband (UWB) antenna array design optimization and tradespace study is an intricate procedure. State-of-the-art techniques such as heuristic optimization algorithms are accurate but computationally expensive due to their iterative nature. To address this drawback, conventional full-wave EM solvers such as the method of moments (MoM) and finite element method (FEM) can be replaced with well-trained machine learning (ML) models. In this work, radial basis function (RBF), and least squared regression (LSR) models were trained with UWB antenna metrics (S11, gain, E-field) and validated by comparing the output prediction from each ML model against the output from a conventional full-wave EM solver. Trained RBF and LSR models accurately predicted the S11, gain, and electric field outputs 160x faster than traditional EM solvers. Both ML algorithms have good prediction capabilities, however, RBF was found to result in better prediction as well as low root mean square error (RMSE) values. The results obtained from this study showcase the potential to revolutionize EM simulation technology. The application of these ML algorithms will be extended to antenna array geometries following the same procedure.

3.18 The Shielding Effectiveness of UAV Frames to External RF Interference

M. Z. M. Hamdalla[1], A. N. Caruso[2], and A. M. Hassan[1,2]

[1]Department of Computer Science & Electrical Engineering, University of Missouri-Kansas City, Kansas City, MO

[2]Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO

Electronics are typically housed in a metallic or a dielectric enclosure where slots are placed for a wide variety of practical considerations. These slots represent pathways that can compromise the enclosure's shielding effectiveness (SE), allowing interfering electromagnetic radiation to reach the enclosed electronics. Moreover, metallic enclosures with slots can have a high-quality factor causing the penetrating waves to bounce back and forth, creating a standing wave. This standing wave can create large fields at the resonance frequencies of the cavity, i.e., the fields inside the cavity can be higher than the incident field itself. Over the last six months, we studied realistic small quadcopter UAV frames as enclosures to assess their SE. The effect of different UAV frame shapes and materials on the SE were also studied. Carbon fibers (CF) and plexiglass were assigned as common UAV materials and their shielding effectiveness compared to the perfect electric conductor (PEC) case. The results showed that PEC frames provide the best SE except at specific resonance frequencies. These resonance frequencies are caused by the slots in the frame where the fields can penetrate the hollow arms that carry the wires propagating to induce a voltage at the connected loads and electronic components. Also, the studied CF frame shows up to ~20 dB lower SE compared to PEC frames away from the resonance frequencies. However, at the resonance frequencies of the PEC frame, CF shows a better SE. On the other hand, dielectric plexiglass UAV frames (ε_r=2.6, tanδ= 0.0057) show a slight increase in the amplitude of the average induced voltage at the enclosed loads. Using these computational results, we generated guidelines on how RF coupling to UAV enclosed electronics differs from RF coupling to electronics in free space. In future work, we will study the SE of more complex UAV frame shapes due to a wide range of pulsed wave-form excitations.

3.19 A Predictive-Package for Electromagnetic Coupling to Nonlinear-Electronics using Equivalent-Circuits and Characteristic-Modes (PECNEC)

M. Z. M. Hamdalla[1], A. N. Caruso[2], and A. M. Hassan[1,2]

[1]Department of Computer Science & Electrical Engineering, University of Missouri-Kansas City, Kansas City, MO

[2]Missouri Institute for Defense & Energy, University of Missouri-Kansas City, Kansas City, MO

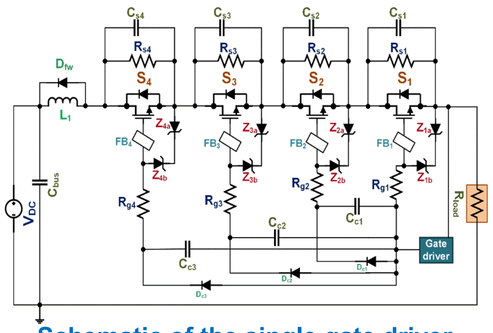
RF coupling to a Device Under Test (DUT) depends on the convoluted properties of its wires and the linear/nonlinear load terminations. The Equivalent Circuit Approach (ECA) provides a unique solution to this convoluted coupling problem by modeling the wires as receiving antennas that can be represented by a Thevenin equivalent circuit terminated with the linear/nonlinear load of interest. The advantages of the ECA are: (i) it provides physical insight into the response of the wiring system. (ii) the ECA involves performing two full-wave simulations. After that, significantly faster circuits simulations can be used to simulate RF coupling to hundreds of different nonlinear loads that can be connected to the wiring system. These simulations will be much faster when performed using a circuits solver such as LTSpice than if they were performed using a full-wave solver. (iii) the ECA facilitates the studying of wires terminated with nonlinear loads over a very long time duration, which is challenging with a full-wave solver. Over the last six months, we developed the Predictive-package for Electromagnetic Coupling to Nonlinear-electronics using Equivalent-circuits and Characteristic-modes (PECNEC). This package is based on the ECA, and it uses simulations with a low computational burden to predict the optimum incident electromagnetic waveform characteristics to cause the coupling to a practical wiring system, with linear/nonlinear electronic terminations, to exceed certain thresholds. Moreover, we initiated the development of a user-friendly Graphical User Interface (GUI) for PECNEC that will facilitate the transfer of PECNEC to ONR and its contractors. We added to PECNEC a UAV model with all its wires and components to be used as a numerical platform for studying RF coupling. In the UAV model, we varied the load impedances by 3 orders of magnitude to quantify the sensitivity of RF coupling to load variations. We studied several other representative examples, to quantify the limitations and strengths of PECNEC and developed a plan for its extension/development to handle additional practical DUTs.

4. Appendix: Posters

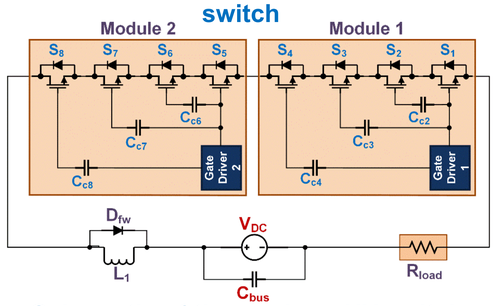
linear-mode photoconductive semiconductor switch (PCSS) based pulse forming network (PFN) for generating high-power microwave (HPM).

- A two-state switching mechanism facilitated by a high-voltage (HV) switch can minimize the power loss, thereby increasing system efficiency.
- Commercially available HV switches (e.g., switches made by German manufacturer BEHLKE) are expensive, have long lead time, require liquid cooling for a switching frequency greater than 10 kHz, and are powered by multiple ancillary DC supplies.
- We are developing an in-house modular HV (~10-kV) switch from inexpensive COTS MOSFETs capable of operating up to a switching frequency of 200 kHz that can be a direct and inexpensive replacement to the HV switches made by BEHLKE
- We have introduced modularity in the HV switch design and HV gate driver design to facilitate voltage withstanding scalability of the switch without complete design overhaul.

Schematic of the Proposed Modular HV Switch



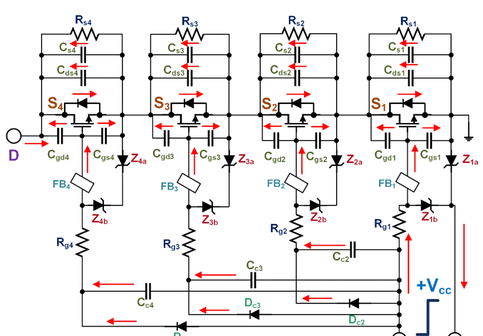
Schematic of the single gate driver-based series-connected in-house HV switch



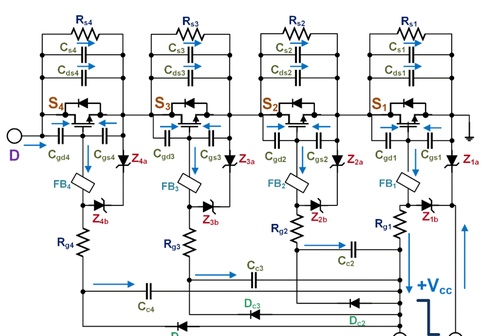
Schematic of the modular HV switch

- Each module consists of four series-connected MOSFETs and one in-house gate driver.
- Two modules are connected in series to increase the voltage rating of the entire switch.
- 1.7 kV rated surface-mount SiC MOSFETs from CREE are used to develop the HV switch.
- The limit of the theoretical breakdown voltage of the HV MOSFET is therefore 13.6 kV.
- Coupling capacitors, snubber capacitors are used to ensure voltage balancing during turn-ON and turn-OFF transients.
- Balancing resistors are used to ensure voltage balancing during the OFF-state.

Switching Transition Dynamics of the HV Switch

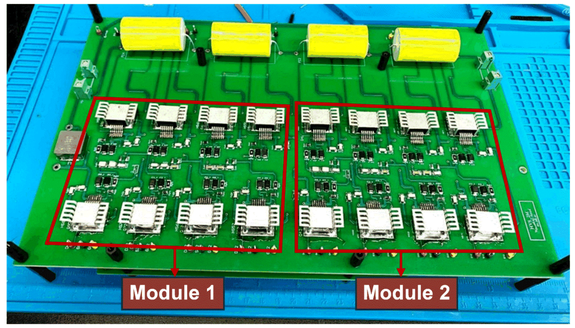


Main current paths during turn-ON transition



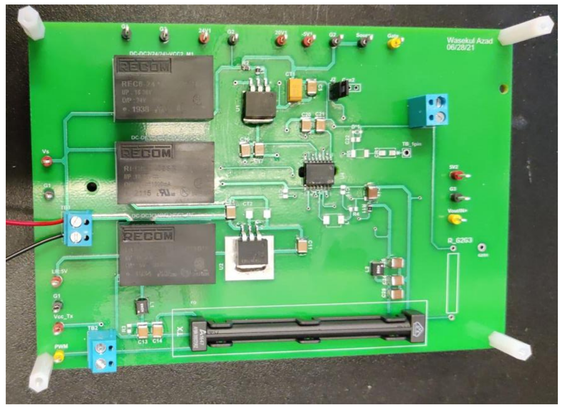
Main current paths during turn-OFF transition

Gate Driver Prototype



An eight-stage in-house modular HV switch (13.6 kV rated)

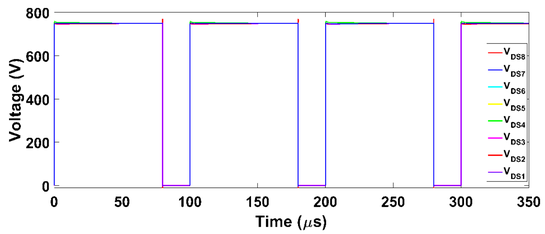
- Two parallel branches of series-connected MOSFETs are incorporated in the modular design to increase the current rating.
- Trace lengths are maintained at minimum to reduce the tray inductance.



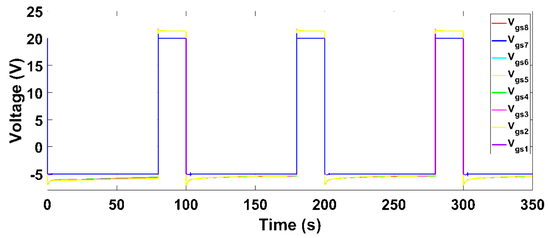
An in-house modular HV (10 kV rated) isolated gate driver

- 10 kV rated isolated DC-DC converters are used to provide galvanic isolation for the power supplies of gate driver ICs in both modules.
- A 5.7 kV_{RMS} rated reinforced isolated gate driver IC with is chosen to fabricate the gate driver modules.
- Each switch module is powered by one gate driver module.
- A galvanic isolation link capable of suppressing 40 kV peak transient voltage is utilized in each gate driver module.

Simulation Results: 6 kV Excitation



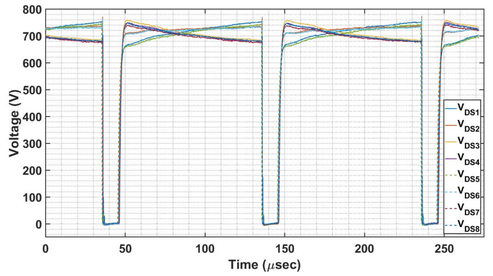
Simulated drain-source (V_{DS}) voltages across the eight individual MOSFETs (V_{DC} = 6 kV, f_{sw} = 20 kHz)



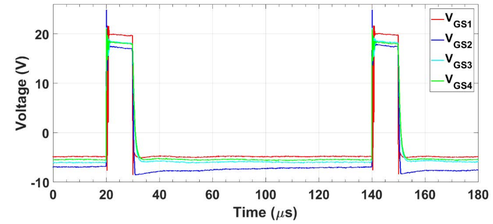
Simulated gate-source (V_{GS}) voltages across the eight individual MOSFETs (V_{DC} = 6 kV, f_{sw} = 20 kHz)

- Simulation shows a maximum voltage imbalance close to 60 V among the series-connected MOSFETs.
- The lowest rise time is measured across the switch farthest from the master switch in each module and is recorded close to 13 ns.
- The master MOSFET of each module exhibits the highest rise time in simulation, close to 19 ns.
- The simulated rise time of the entire modular switch was recorded as 17.8 ns

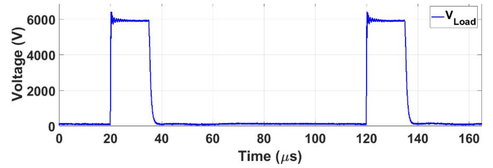
Prototype of a modular 10 kV rat
negative DC p



Experimental V_{DS} measured across the individual MOSFETs (V_{DC}= 6 kV)



Experimental V_{GS} measured across the individual MOSFETs (V_{DC}= 6 kV)



Experimental voltage measured across the resistive load (V_{DC}= 6 kV, f_{sw} = 10 kHz)

Summ

- An in-house modular (2 modules) 8
been designed, fabricated and teste
and switching frequency up to 15 k
driver.
- A modular HV switch with a voltage
and fabricated using new COTS 3.3
- A modular gate driver with higher
designed and fabricated to drive the

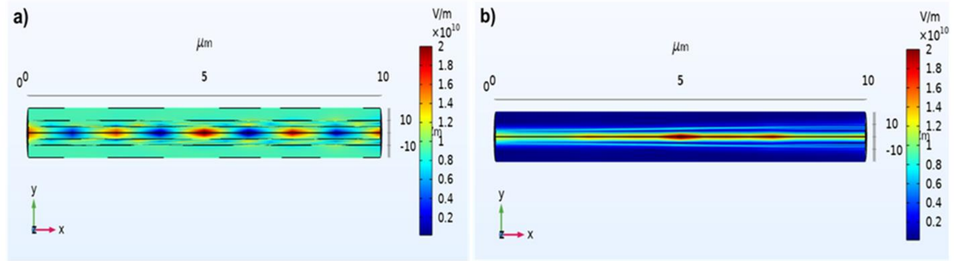
Acknowle

The authors wish to thank the Office o
this work under award no. N00014-17-1

Fiber amplifiers with cores of circular cross-section have reached a fundamental limit due to the conflicting constraints of thermal lensing and self-focusing (SF) both being proportional to core area and nonlinear impairments, inversely proportional to core area.

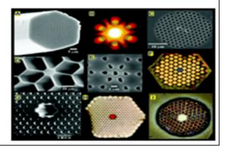
Rectangular-core fiber is better: lensing is limited by the smaller dimension of the rectangle while the larger dimension is permitted to increase in order to mitigate the nonlinearities

Tubular-core fiber is best: light otherwise lost is accumulated in a hollow-core air mode !
COTS realizable operating powers of over 1,000 times the normal fiber limits predicted.

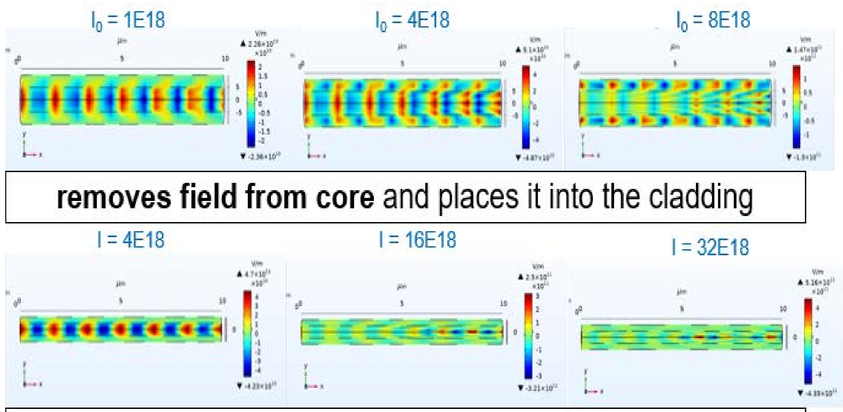


Can support a hollow-core mode in air (like PCF)
Very high power delivery in a very inexpensive embodiment

PCF, in contrast, are expensive



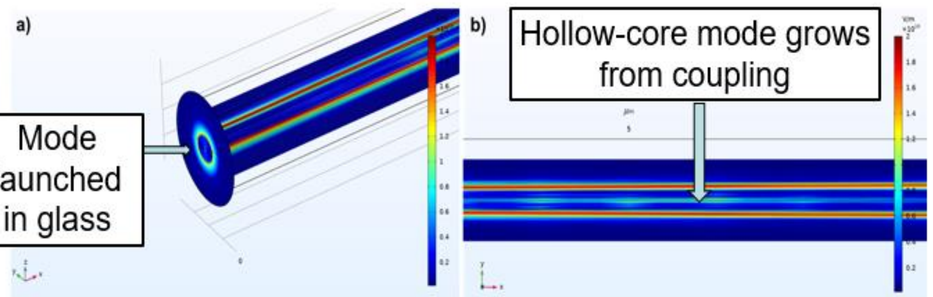
Self-focusing (SF) in Circular-core Optical Fiber



removes field from core and places it into the cladding

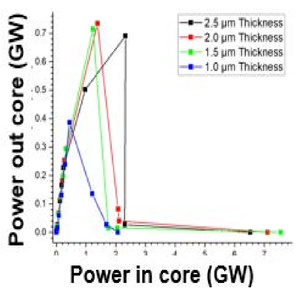
Columns between Case 1 and Case 2 have same power
in contrast to SF in bulk (of same power) we see differences

Glass Tube Surrounded by Air

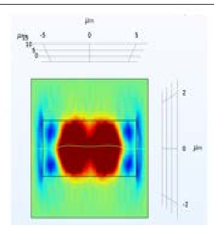


Can not make an amplifier in air.
Fortunately, the mode in glass
(which we dope and pump to make an amplifier)
can couple to the hollow-core mode
in air.

Self-focusing (SF) in Rectangular-core Optical Fiber

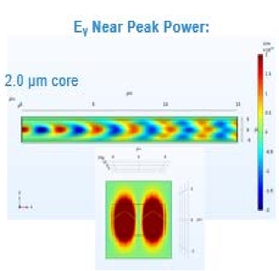


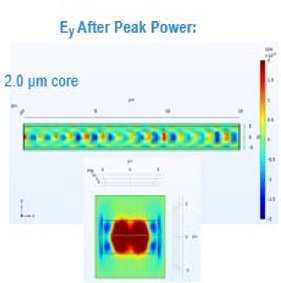
SF scatters light out of slab symmetrically



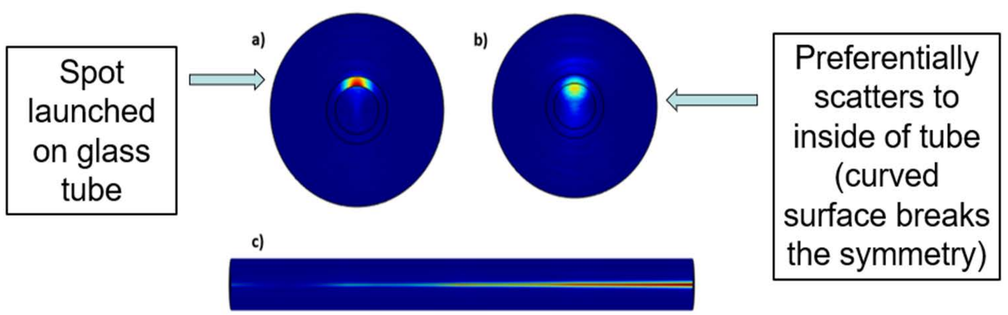
Optimal thickness depends on power.

Mode evolves into 2 spots.
At higher power it radiates into cladding and sides.



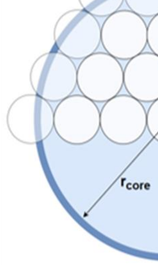


Symmetry Breaking and Accumulation Effect

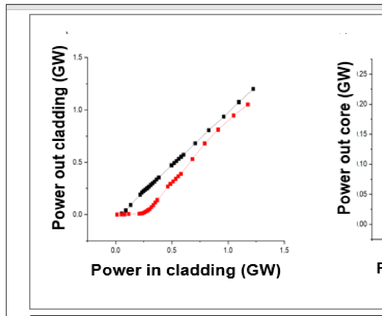


This otherwise would-be-lost energy is accumulated
in the hollow air-core mode.
Optical power tube can operate at powers higher than other waveguides
amplifying in the glass/cladding
while the air/core also carries energy

of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) permit a single laser to trigger an array of N PCSS – reducing the laser system cost, by N and eliminating the optical timing jitter constraint.



Shown: powe
perfectly sync
drive N = 12
to be used as a



Air/core at ¼ GW with glass/cladd
with < 10% power lo

Tube wall thickness of 10 microns

Su

- A **tubular core optical power amp**
than standard circular-core (or even

- **COTS realizable tubes** of 2.5 mm
(1) increase the heat transfer (via the
100; and (2) increase the nonlinear t
sectional area) by a factor of **204** – w
fiber of the same unit length.

- **In addition to** the geometry-based
power tube can **capture and accumu**
otherwise be scattered out of the wa

- The **tubular optical amplifier** supp
like a reservoir for lossless power de

- A single **tubular optical amplifier**
in an array. This also would **eliminate**
well as dramatically reduce the SWP

Ackno

This work was supported by the
N00014-17-1-3016.

Objective

Implement a compact (~1.1 cu-ft), lightweight (10–15 lbs.), and inexpensive (<$15,000) laser diode array (LDA) driver as an alternative for conventional high-average-power laser driver subsystem to improve SWaP-C^2 index of PCSS-based HPM systems.

OSPRES Relevance

PCSS-enabled LDA driver provides an alternative solution for laser driver subsystem(s) used in PCSS activation with enhanced SWaP-C^2 index and a subsequent impact on HPM system cost, volume, and power requirements.

Background

Acute optical pulse energy requirements in linear photoconductive semiconductor switch (PCSS)-based HPM applications require high-average-power pulsed laser systems capable of delivering >250–300-µJ/pulse at sub-ns order pulse widths. Despite meeting the requirements, the state-of-the-art laser systems—being heavy (~125 lbs.), bulky (~10 cu-ft), and expensive (~$120,000)—fall short of the SWaP-C^2 expectations of the HPM systems for navy afloat missions. Furthermore, these are Nd: YAG-based, tuned to emit 1064-nm pulses, and require second and third harmonic generation (SHG/THG) optics to trigger wide bandgap (WBG) PCSSs. This effort aims to reduce the size, weight, and cost of the laser subsystem by ~90% and potentially circumvent the need for conventional lasers in the near future. This is achieved by retrofitting a PCSS to function as a seed-laser-diode-driven lock-on switch to drive a high-power laser diode array (LDA).

State-of-the-art Limitations

The SOTA pulsed LDA drivers with compact form factor satisfy either the output current (>110 Amp) or fast transients (<1 ns FWHM) requirement at ~MHz PRR, but not both. The COTS driver classification is shown below. This work is a one-stop solution that is compact (<0.75cu-ft), capable of >110 Amp output current, <1 ns pulse widths at <200 ps rise time (t_r) and >1 MHz pulse repetition rates (PRR). This provides a SWaP-C^2 optimized solution for the driver subsystem of an LDA-based optical source.

Manufacturers:
AMI – Analog Modules Inc.,
HT – Highland Tech.,
DE – Directed Energy,
AI – Arroyo Instruments

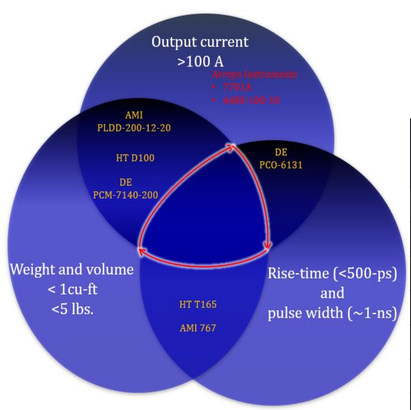


Figure: *COTS SOTA LDA driver classification*

Figure: *(left) NeoLase picosecond Nd:YAG, (right) IPG Photonics fiber laser*

Parameter	SOTA		Objective
	Nd: YAG*	Fiber**	
Weight	125 lbs.	~30 lbs.	~10 lbs.
Pulse width	70 ps	5 ps	< 1 ns
Volume	9.65 cu-ft.	2.43 cu-ft	<1.08 cu-ft.
Power	50 W	Upto 50 W	upto 1200W
(PRR)	50 MHz	2 MHz	1-5 MHz
Cost	>$120,000	$97,500	<$15,000
Pulse energy	250 µJ	50 µJ	>750 µJ

Table: *Parametric comparison b/w SOTA lasers and proposed effort*

Approach

Target metrics in terms of output current, breakdown voltage, PRR, and transient response were determined based on Jenoptik JOLD series LDAs. A feasibility study showed the need for lock-on mode with ~$10^{2.6}$ current gain when PCSSs are used. GaN-PCSSs are considered a prime candidate for the LDA enabling switch.

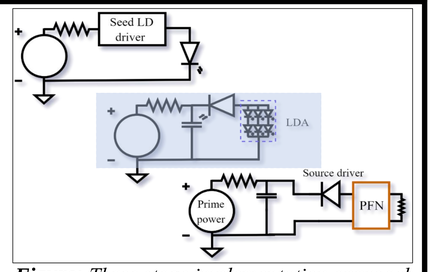


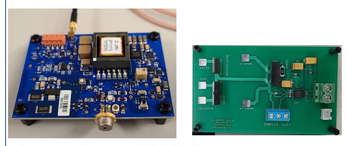
Figure: *Three stage implementation approach*

However, Si-PCSS and COTS Si-optodiodes and avalanche switches such as silicon avalanche shapers (SAS), avalanche transistors (ATs) are being evaluated as potential alternatives to GaN-PCSS.

Stage I
Seed-laser driver (or) SAS/FET module + pulse shaping

→ **Stage II**
PCSS-driven LDA triggering (or) GaNFET driven amplifier + NLTL

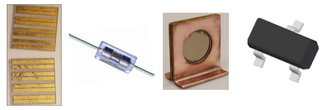
→ **Stage III**
Application



(Left) *150-ps FWHM seed laser driver,* ***(Right)*** *SAS/FET module*

Table: *SLD driver target metrics*

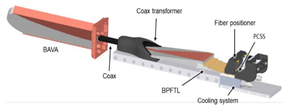
Parameter	Value
Pulse width	<200 ps FWHM
PRR	1-2 MHz



Left to right: *GaN-PCSS, Si-optodiode, Si-PCSS and AT*

Table: *Avalanche switch metrics*

Parameter	Value
Breakdown voltage	< 100 Volts
Pulse width	<1 ns
On-state resistance (R_{on})	<72 mΩ
Output current	>110 Amps



PCSS-based HPM generation

Table: *Driver subsystem metrics*

Parameter	Value
Risetime	< 300-ps
Pulse width	<1 ns
Weight & vol.	<10 lbs <1cu-ft
R_{on}	<72 mΩ
Output current	>110 Amps

Si-PCSS and Si-op

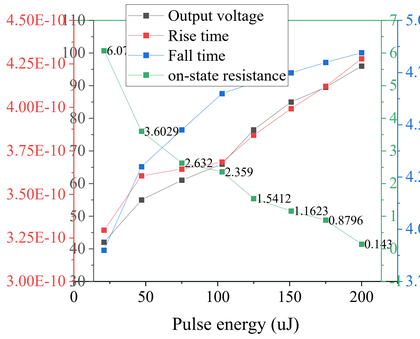
Si-optodiode

- R_{on} of **0.143 Ω** at **200 µJ** and
- t_{rise} of **329.4 ps** with a **6.038** at 21 **µJ**

Si-PCSS

- R_{on} of < **0.325 Ω** at >250 µJ/

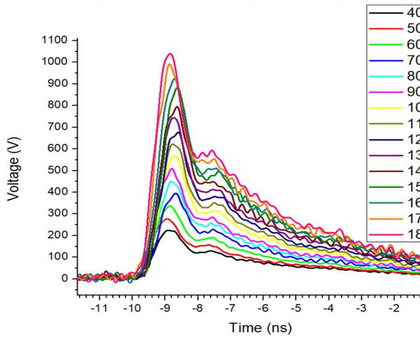
Devices failed to satisfy the m (R_{on} = 72 mΩ and t_{rise} < 200- <40 µJ) and hence consid infeasible as an alternative to PCSS.



Figures: *(Left) Si-optodiode test trends for Outp for output voltage and*

GaN-PC

- Expected persistent condu **>3kV/cm** [2] was not observed
- In-house testing with 365 n linear mode even at **18 kV/cm**



Figures: *(Left)1000 µm gap GaN-PCSS pulse o (Right) output voltage, current an*

Implementation Methodology

Stage I consists of a seed laser diode (SLD) actuated by a driver capable of sub-ns transients. The SLD stimulates a GaN-PCSS from **stage II** in lock-on mode. The current delivered by a PCSS actuates the LDA that emits a laser output ~1 kW, which activates the PCSS driving the application in **stage III.**

Stage I
Seed-laser (or) Gate driver + pulse shaping

Stage II
Avalanche switch triggered LDA + pulse shaping (optional)

Stage III
HPM generation system

Key References

[1] J. Y. Tsao, S. Chowdhury, M. A. Hollis, D. Jena, N. M. Johnson, K. A. Jones, R. J. Kaplar, et al. 2018. "Ultrawide-Bandgap Semiconductors: Research Opportunities and Challenges." *Advanced Electronic Materials* 4 (1): 1–49. https://doi.org/10.1002/aelm.201600501.

[2] E. A. Hirsch *et al.*, "High-Gain Persistent Nonlinear Conductivity in High-Voltage Gallium Nitride Photoconductive Switches," *2018 IEEE International Power Modulator and High Voltage Conference (IPMHVC)*, 2018, pp. 45-50, doi: 10.1109/IPMHVC.2018.8936660.

[3] C. V. Reddy, K. Balakrishnan, H. Okumura, *and* S. Yoshida , "The origin of persistent photoconductivity and its relationship with yellow luminescence in molecular beam epitaxy grown undoped GaN" , Applied Physics Letters 73 , 244-246 (1998) https://doi-org.proxy.library.umkc.edu/10.1063/1.1

[4] M. Zhang, R. Yang, N. Liu, and X. Wang, "Persistent photoconductivity in neutron irradiated GaN", Journal of Semiconductors 34, Vol 9, doi: 10.1088/1674-4926/34/9/093005

Summary &

Linear conduction has been obser Alternative technologies with pot being evaluated. Thus far, Si-PCS and deemed unfit to replace GaN-

Future Work:

- Evaluate ATs and SASs as a pot
- Study GaN device physics to d for lock-on mode and perform a

This work was supported by the Office of Naval Resea

Objective

Compensated, semi-insulating gallium nitride (GaN:X) is a promising wide-bandgap material for use in photoconductive semiconductor switch (PCSS) based cUAV for Navy vessels and vehicles because the material characteristics of GaN:X allow for higher operating power, frequency, and temperature in a smaller form factor than traditionally used materials such as Si or GaAs. However, the immaturity of GaN:X, compared to more commercially available materials, has limited the use of GaN:X, even as performance needs push up against the theoretical limits of traditionally used materials. One key performance metric for maximizing efficiency of PCSS-based systems is minimizing on-state resistance to <1 Ω during device operation, reducing on-state losses and heat generation. Exploring methods to optimize on-state resistance of GaN:X PCSSs will allow for a new generation of compact, efficient PCSS-based cUAV systems with increased SWAP-C^2 capabilities.

PCSS On-State Resistance

On-state resistance for PCSSs is a determining factor in the electrical conversion efficiency of the device during the "on" state, and when on-state resistance is high, heat in the device can lead to premature thermal breakdown. There are several parameters that affect on-state resistance in a PCSS as shown in Figure 1, so there are a lot of parametric studies to be performed for on-state resistance optimization (< 1 Ω). For this presentation, we will focus on experimental results showing how the wavelength of the incident photon source used for device activation and the incident energy (number of photons) affect the on-state resistance of a lateral, carbon compensated GaN:X PCSS (Figure 2).

On-State Resistance Parameters

Figure 1: Flow chart of parameters affecting on-state resistance in GaN:C PCSSs.

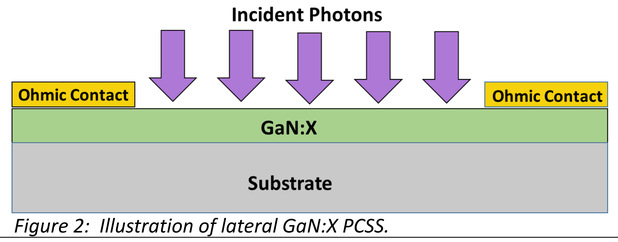


Figure 2: Illustration of lateral GaN:X PCSS.

Results

An important factor for overall system cost and on-state resistance for a PCSS-based system is the wavelength of the incident photon source used for device activation. Due to the band gap of GaN, a UV source is needed. By altering the wavelength used, the absorption depth and how deeply photocarriers are generated in the device there are changes to the overall on-state resistance and current carrying capability of the device. Figure 3 shows the intensity in a GaN:X device as a function of depth, while Figure 4 is an illustration of how the absorption depth affects the current density and absorption depth within the device. Too short of wavelengths can lead to a shallow absorption depth, increasing current crowding and heat generation towards the surface of the device. While too long of wavelengths will have a deeper absorption depth or transmit through the PCSS without generating photocarriers.

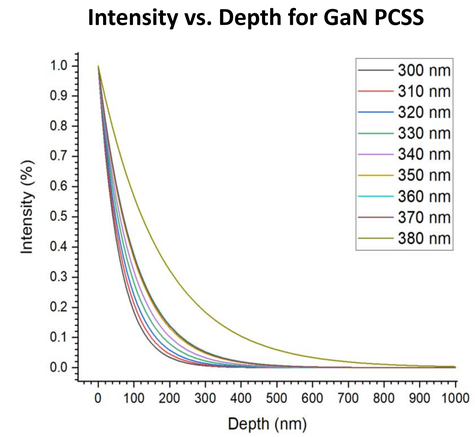


Figure 3: Intensity as a function of depth for different incident wavelengths for GaN [1].

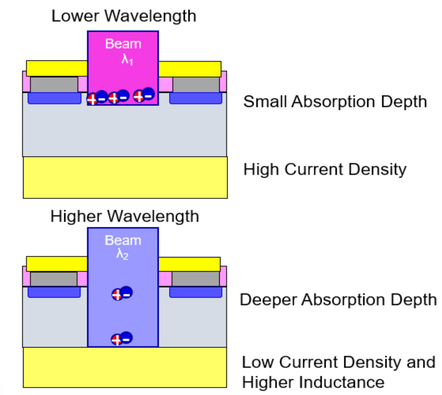


Figure 4: Illustration of how wavelength affects current density and absorption depth in PCSS.

The on-state resistance for lateral GaN:C devices with varying gap lengths and incident photon wavelengths is shown in Figure 5. As the gap length is increased, the minimum on-state resistance achieved is limited but the operating voltage capability is increased due to increased allowed electrical field between the contacts before flashover occurs. At wavelengths >370 nm there is an exponential increase in the on-state resistance for all gap lengths. Because of this result, using diodes or LEDs is the low 400 nm not being a viable option with these specific devices.

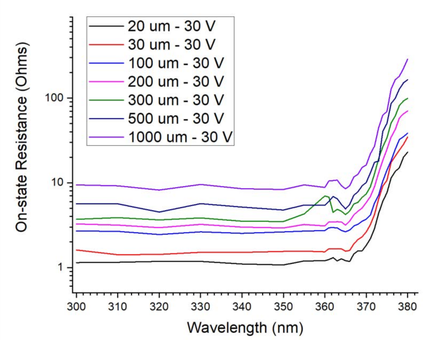


Figure 5: On-state resistance vs incident wavelength for lateral GaN PCSSs with differing gap lengths.

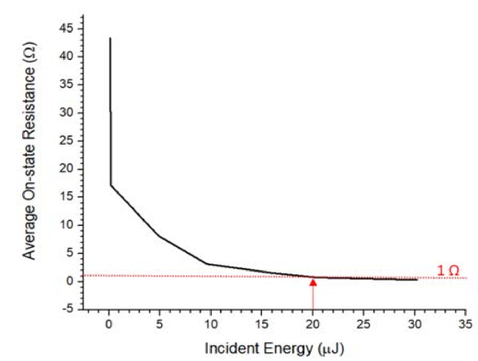


Figure 6: Average on-state resistance vs incident energy.

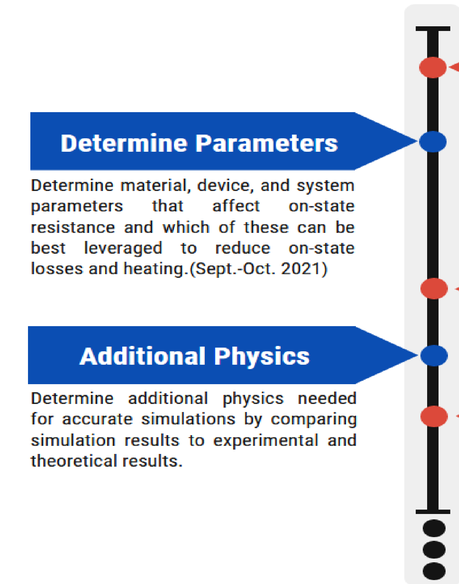
The energy of the incident photon source, or the number of photons incident on the PCSS, determines how many photocarriers are generated until saturation and is also an important factor in dictating laser cost, so generating the maximum number of photocarriers with the least amount of incident energy is ideal and an important factor in optimizing on-state resistance. As shown in Figure 6, the average on-state resistance (for different voltages tested) reached ~1 Ω, at approximately 20 μJ for a 500 μm gap length GaN:C PCSS, meaning energies above this level do not generate excess carriers and instead contribute to device heating. Changes to the material, such as defect density, will be looked at in future work to determine if this could lead to <1 Ω on-state resistance at lower energies.

Summ

GaN:X is a promising material for next genera
vessels and vehicles due to its theoretical mat
operating voltages, frequencies, and temperatur
being pushed up against. A key factor in
traditionally used materials is the on-state resist
conversion efficiency of the PCSS. By studyi
resistance and optimizing those which can be
devices can be designed with greater efficiency
the wavelength and energy of the incident ph
decisions can be made for the ideal laser neede
the overall system. Here, we show that the wav
dramatic increase in on-state resistance with t
there is no return on investment for using ener
gap length. These results will be used to compa
additional physics needed, for these specific pa
for lateral devices.

Future

Project Ti



Due to limited availability of devices, much of
TCAD and/or COMSOL.

Referen

[1] J. F. Muth *et al.*, "Absorption coefficient,
recombination lifetime of GaN obtained from tra
1997.

Acknowled

This work was supported by the Office of Naval R

The objective is to maximize peak power while maintaining ns-order risetime for Drift-Step Recovery Diodes (DSRD) in DSRD-based pulser systems. Other considerations include compactness, low-jitter, cooling requirements, additional pulse sharpening, and application specific pulse repetition frequency goals. Our approach is to develop and iterate upon TCAD and SPICE models to optimize device geometry, doping and device irradiation for performance.

OSPRES RELEVANCE

DSRDs are an alternative to photo-conductive semiconductor switch (PCSS) based solutions, eliminate laser requirements, and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2 cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems. Low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

BACKGROUND

Drift step recovery diodes (DSRD) are fast opening switches used as circuit breakers within inductive energy storage (IES) systems. Our devices are made from silicon due to the ease of manufacturing, and currently epitaxial methods are being used to manufacture our latest DSRD devices.

Stack DSRD die

A number of DSRD pulser circuit topologies exist, and in this poster the designs of Figure 2 are used. A simple explanation of the operation of the DSRD within the pulser circuit is that the DSRD is first forward biased for a few hundred ns and then quickly reverse biased until the DSRD empties of stored charge. After which the current abruptly snaps off, breaking the current in the nearby inductor and causing a voltage spike at the load which the DSRD must holdoff. A primary MOSFET switch is used to forward and reverse pump the DSRD.

TCAD and LTSPICE have been used for modeling and simulating DSRD doping profile designs [1] and DSRD pulser circuit topologies. An example optimized doping profile is shown in Figure 1 for an exponential doping profile. Doping profiles were optimized for maximum doping, minimum doping at the pn-junction, basewidth, and junction placement by simulating the DSRD doping design in various DSRD pulser circuit topologies shown in Figure 2. Circuit A is a simplified pulser circuit with no primary switch and circuit B is a base pulser design used for modular designs incorporating a single DSRD stack. Circuit B uses MOSFET primary switch models [2,3].

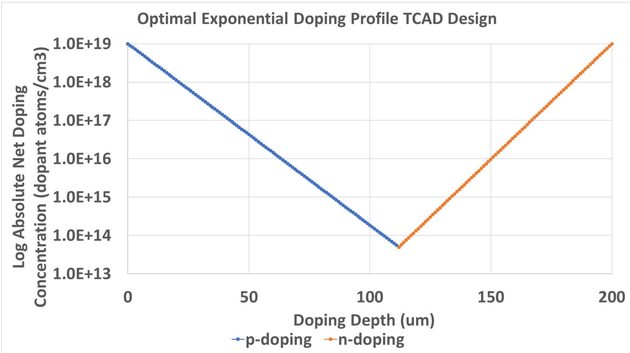


Figure 1. Exponential or log-linear doping profile designed in TCAD and fabricated by Lawrence Semiconductor Research Laboratories (LSRL).

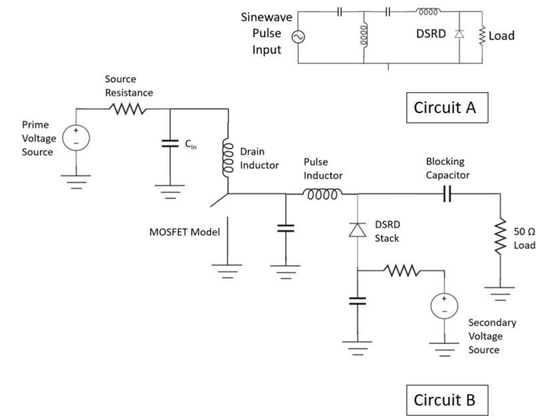


Figure 2. DSRD pulser circuit topologies used in simulation and experiment.

RESULTS

Exponential doping profiles are studied within a comprehensive TCAD doping parameter study with fabrication limits set by Lawrence Semiconductor Research Laboratories (LSRL). Junction placement, basewidth, doping maximum and doping minimums were varied within the LSRL fabrication limits for device performance within circuit A as shown in Figure 3. Device performance within circuit B (not shown) produced similar results. In Figure 3, all the datapoints undergoing breakdown have been excluded and are in a scatter plot for peak voltage vs risetime within the DSRD pulser. The lowest risetime case is for 5×10^{13} dopant atoms/cm^3 minimum doping, no basewidth and 95 µm junction placement on 170 µm thick device. The region circled indicates doping profiles that have optimal peak voltage and risetime tradeoffs. In Figure 4, the results of pulser performance in circuit B but with a SPICE MOSFET model was simulated in both TCAD and LTSPICE to compare the DSRD performance to experiment. The refinement of the pulser simulations is ongoing to include improved models and experimental testing to be predictive of output pulse characteristics over range of inputs, stack heights and pulser circuit topologies.

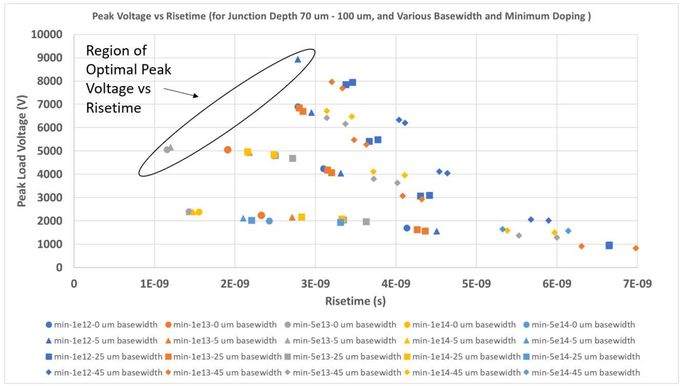


Figure 3. TCAD simulation for peak voltage and risetime of exponential doping with varied minimum doping, basewidth, voltage input and junction placement.

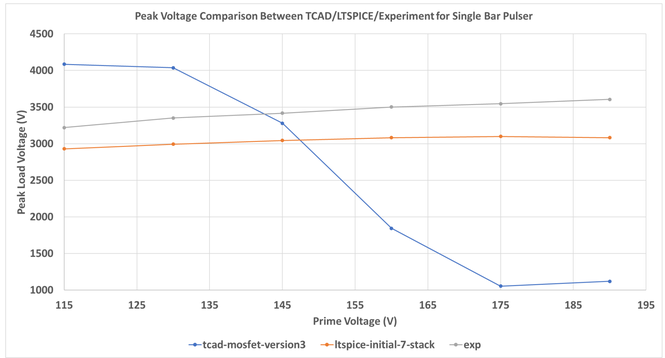


Figure 4. Peak voltage vs prime voltage input compare between TCAD, LTSPICE and experiment.

Exponential dop
TCAD simulation
can only be fabri
currently being m
shown in this po
profile performan
voltage and riset
minimum doping
basewidth and r
doping profile wi
junction placeme
basewidth has b
have the lowest
DSRDs.

TCAD and LTSPIC
earlier modeling
pulser circuit top
breakdown effec
standard diode m
specification of
processing param

- Improve predict
LTSPICE models
- Optimal designs
doping and irrad
- Design and opti
topologies
- Customizing of
lot-specific spec

[1] Lyublinsky, A. G., E.
Experimental Study of a
no. 3 (2019): 373-379
[2] CREE C2M0045170
Technology N-Channel
2018.
[3] Arribas, Alejandro P
Krishna Shenai. "Simple
power MOSFETs." IEEE
(2015): 449-457.

UMKC

This work was supported by the Office of Nava

Problem statement: Develop new process integration scheme for manufacturing Drift Step Recovery Diodes (DSRDs). Experimentally prove technical feasibility of the pioneering process flow. Manufacture pilot lots of DSRDs using SPT, Inc. facilities and other partner vendors. Confirm advantages of new DSRD process over the traditional process by comparing pulse performance of commercially available DSRDs to devices made by the pioneering technology. Compare old and new technologies by device yield, manufacturing costs, distribution of device specs, and other criteria. Upon proof of advantages over existing technologies, license the process to a trusted foundry for mass production.

Relevance to the OSPRES objective: Pulse generators for Navy missions need better than current 10^{12} Volt/s pulse voltage rise on load, as well as higher energy per pulse, faster repetition rate, and longer pulser lifetime. This can be achieved by replacing existing DSRDs in pulsers by DSRDs having better pulse performance. Current DSRD technology is very similar to one used 60 years ago. It must be replaced by new disruptive technology.

State-of-the-art (SOTA): Conventional DSRD manufacturing process flow is based on deep diffusion of dopants through opposite sides of thinned silicon wafer, depositing metal contacts, dicing wafer with diode structures into dies, stacking of dies by soldering, removal of damaged silicon on die sides by etching, and passivating open diode sides by polymer coating. This process was developed for the first time in the 1960s [1]. Small details of the process scheme were optimized, but the major "deep diffusion" paradigm remains.

Deficiency in SOTA: The 60-year-old "deep diffusion" paradigm is totally exhausted. To build DSRDs with better pulsed performance, a new paradigm must be introduced and comprehensively developed.

Solution Space: Replace deep diffusion approach by process integration scheme based on newer techniques as epitaxy, wafer bonding, anisotropic etching, others developed in semiconductor industry.

Objective:

Develop DSRD manufacturing process integration scheme exploring advantages of epitaxy, selective electroless plating, wafer bonding by intermetallic compounds, V-groove etching, silicon surface passivation and others. Experimentally prove advantages of new technology over conventional by manufacturing DSRDs having better pulsed performance.

Fig 1:Example of stacked DSRD commercially available today

27-stack DSRD model H141S made by Voltage Multipliers
Manufacturing process of device is property of manufacturer.
Still, looking on the design one can assume the process:
Wafers thinned to ~ 100 micron
Al+B and P diffusion from top and bottom of wafer
Metallization of whole wafers
Dicing into 6-mm dies
Etching of dicing damages on sides
Soldering into stack
Side passivation by polyimide

Defects are even visible to the eye – say, polymer flakes-off from hot side during diode operation

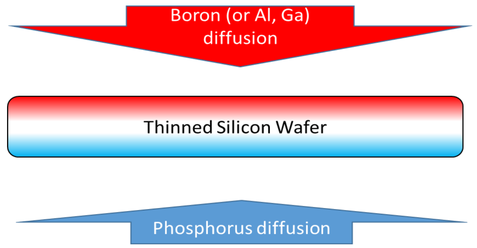


Fig 2: Simplified illustration of traditional "deep diffusion" DSRD concept

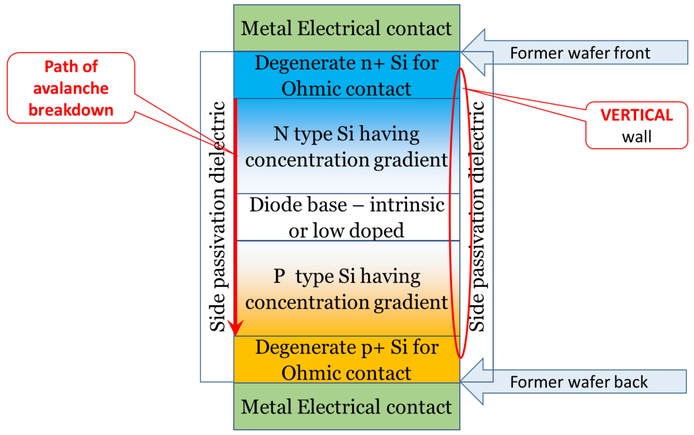
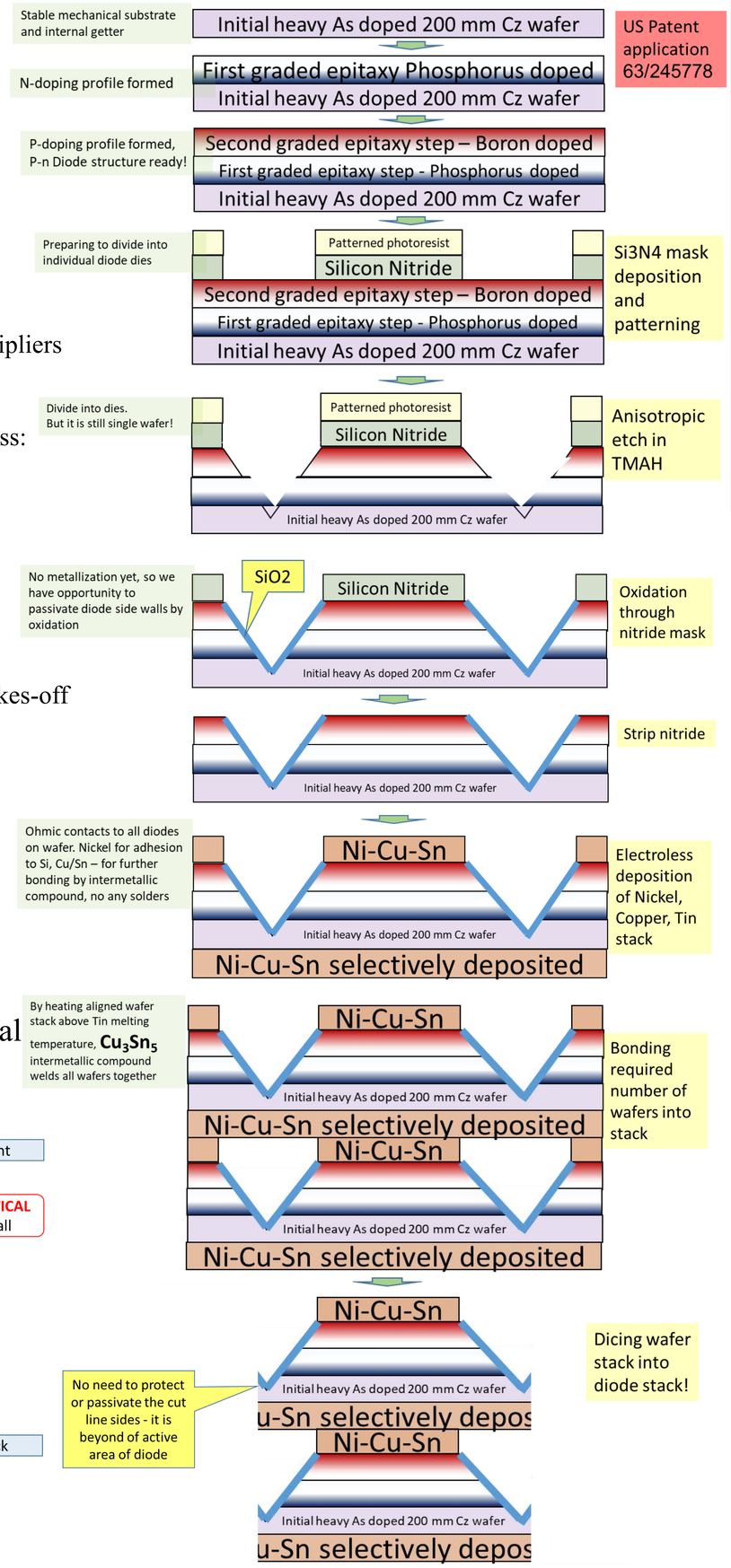


Fig 3: Traditional DSRD Design, Schematized



- Diffusion technology a
(complementary error
→ optimization of the
improve.
- Double simultaneous d
200 – 100 micron
→ thin wafers brake du
- Diffusion driving from
→ diffusion fronts are
therefore diode base (
yield, wide scatter of d
- Diode side is terminate
→ diode breakdown vo
10-time lower vs bulk t
→ incompatible with s
breakdown – either by
- Diode stacking is after
→ wafer contains hund
wafer level, then dicing

Table 1:Wea

New approach
manufacturing DSR
excluded from the
scheme that includ
bonding, and selec
Potential advantag
must be now prove
pulse performance c

We plan to finish
new technology i
compare pulsed p
commercially avail

Ac

This work was su
Research under G
Contract No. N683

[1] Boff, A., J. Mo
effect in solid-state
Solid-State Circuits
Papers, vol. 3, pp. 50
[2]S.Bellinger, A.Ca
Side Passivation an
Provisional Patent Ap

The objective of this project is to develop a methodology for assessing the performance of drift-step recovery diodes (DSRD) through an augmented design of experiments (DOE) to meet the specific needs for inductive energy storage (IES) pulse generating circuits. This augmented DOE will be a continuously evolving model that is designed to remain flexible as the objectives of the DSRD-based systems progress.

OSPRES RELEVANCE

Reducing the gaps between DSRD's theoretical and experimental performance, utilized in within the pulse generator source, enables an increased technology readiness level (TRL). In turn, the DSRD-based IES pulser will produce the waveform parameters and fidelity to compete with the silicon photo-triggered switches (SiPCSS) used in high-power microwave generators due to dimensional scalability.

Figure 1: deep diffusion 7 stack DSRD.

BACKGROUND

DSRDs are planar diodes that are capable of high pulse repetition frequency (10^0 - 10^6 kHz) and are used within a variety of pulsed-powered applications [1]. Unlike most commercial diodes, DSRDs lack a published assessment network that can tie circuit performance back to fabrication or diode characterization tests. (Figure 2).

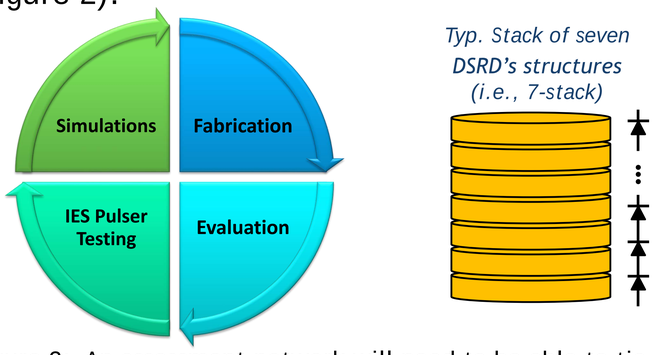


Figure 2: An assessment network will need to be able to tie key metrics from each stage of the DSRD lifecycle to the final IES pulser circuit performance.

Capacitance-voltage (CV) measurements of junction capacitance provide carrier doping profiling, resistivity of the diode material, and the switching capabilities through differential capacitance [2]. Different current-voltage (IV) characteristics are obtained from the DSRDs depending on the direction of the applied DC bias. Forward bias IV measures the forward current which is strongly affected by the carrier lifetimes, whereas the reverse bias IV measures the reverse current and is associated with the breakdown voltages and the leakage current [4]. Reverse recovery time (RRT) is a transient measurement and is used to quantify the removal of plasma from the DSRD as it transitions from a conducting to a blocking state [4, 5]. Refer to Figures 3, 4, and 5 for the testing equipment currently used for the CV, IV, and RRT testing, respectively.

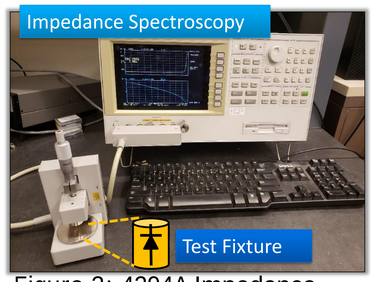


Figure 3: 4294A Impedance Analyzer with 16451B Dielectric Test Fixture (CV Test)

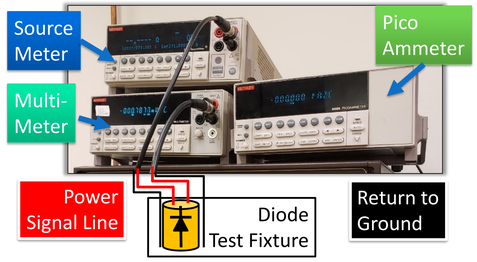


Figure 4: Keithley 2400 Source Meter, 2000 Multimeter, and the 6485 Picoammeter (IV Test)

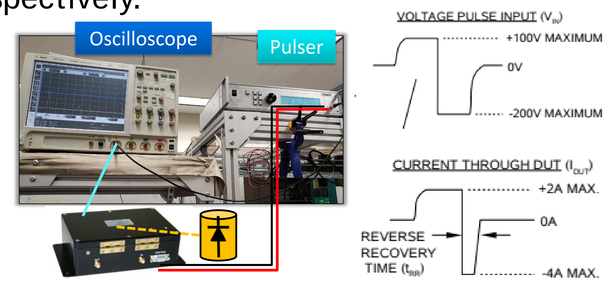


Figure 5: AVR-EB AVtech Pulser with an AVX-TRR-HPOST Jig Test Fixture (RRT Test) with typical output waveform shown on right.

RESULTS

- Preliminary results of the DSRDs show large variability, which may be complicated by several factors (e.g., poor electrical connections, operator bias).
  - ✓ The CV measurements shown in Figure 6 are extracted from real and imaginary components from the data using the Cp-Rp model and is a possible source for variability.
  - ✓ In Figure 7, the 13 stack DSRDs appear to group off in to two separate trends.
- The recommended RRT testing conditions within the Avtech pulser manual limits the RRT bias to 20 V or less and is due to the Avtech pulser risetime being too fast for the attenuators to properly compensate (Figure 8).

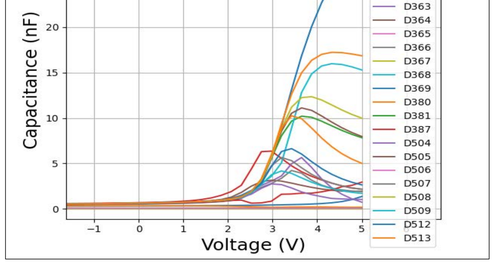


Figure 6: CV measurements for 7 stack deep diffusion DSRDs

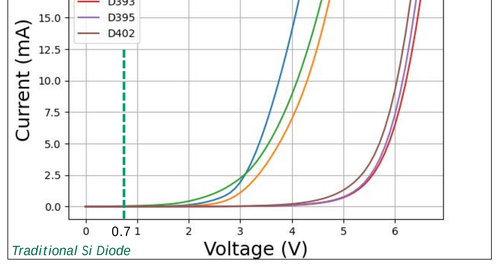


Figure 7: Forward IV measurements for 13 stack deep diffusion DSRDs

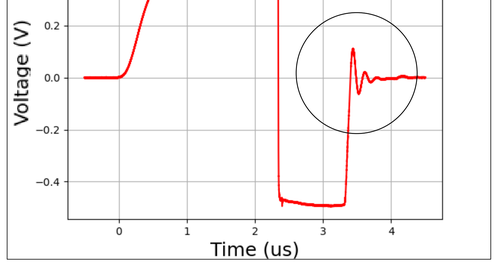


Figure 8: (Right) RRT measurement of a 7 stack DSRD. The intruding(circled) oscillations due to fixture attenuation.

All deep diffusio
and CV testing.
section, several
themselves, suc
measurements.
progress.

Next steps inclu
indicators (KPIs)
diffusion DSRDs
that can be use
generation of di
be used to build
performance ou
(Figure 9).

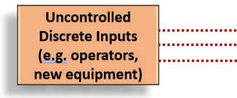


Figure 9: DOEs are r
process and is ofte

- Evaluate the
each experim
through equa
- Perform testi
DSRDs (Figure
- Quantify beha
from deep di
(Figure 1) and
- Begin prelimi
optimized IES

[1] Kozlov, V. A., Smirnova,
June). New generation of d
switching and high repetitio
Fifth International Power M
Workshop. (pp. 441-444). IE
[2] Lutz, J., Schlangenotto,
Semiconductor power devic
Science & Business Media.
[3] Montgomery, D. C. (201
sons.
[4] Schroder, D. K. (2015).
John Wiley & Sons.
[5] Taylor, J. D. (Ed.). (2018

UMKC

This work was supported by the Office of Nava

Systematically develop the greatest peak-power-density permutation of a drift-step recovery diode (DSRD)-based inductive energy storage & release (IES) pulse generator topology, and its circuital component's parameters, leveraging machine learning, diode & circuit model simulations, and experimental analysis.

Key performance indicators (KPI): megawatts of peak power on 50 Ω loads, ≥100 kHz pulse repletion frequency, sub-nanosecond risetime, balanced differential feed to radiating element, compact form-factor (≤5000 cm³) lightweight (≤3 kg).

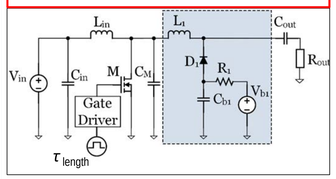
OSPRES RELEVANCE

Air-cooled DSRD-based IES pulse generators, when power combined in series-parallel stage combinations, can achieve the performance metrics of laser-based proto-triggered switching technologies thus improving space weight & performance, cost & cooling (SWaP–C²). DSRD-IES sources are ideal for triggering sub-nanosecond pulse sharpening devices (e.g., silicon avalanche shapers (SAS), dynamic breakdown diodes (DBD), and diode-based nonlinear transmission lines (D-NLTL). Collectively, these pulser generators produce the peak power required, within a small form-factor, necessary to support the Naval afloat cUAV mission.

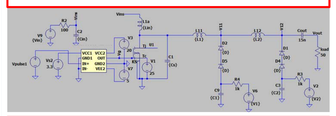
BACKGROUND

Drift-step recovery diodes used in certain IES sources can produce ones of gigawatts in ones of nanoseconds. However, pulsers capable of these performance metrics are traditionally large (>1 m³), bulky (i.e., >1000's of kgs), limited in pulse repetition frequency to tens of kilohertz, utilize non-standard load impedances ill-suited for traditional antennas, and incur order-of-magnitude reductions in volumetric power densities from their hundred(s) of MW/m³ pulser counterparts. Modular power combining stages with 'M' number of branches connected in parallel are used to drive later 'N' number of pulse compression stages in series towards increased peak power output while shortening pulse risetime. Past LTspice simulations provided insight on the M×N combinations' voltage gain, peak power, risetime, and energy efficiency as a function of voltage, inductance, and capacitance for each permutation up to M×N = 4×4. The experimental results of producing 1×1 to 4×2 topology permutations, along with number of diode structures (Si-doped wafer stacked in series) are presented which are used to verify the SPICE model's accuracy and fed to Machine Learning models to determine the IES pulser's optimal permutation.

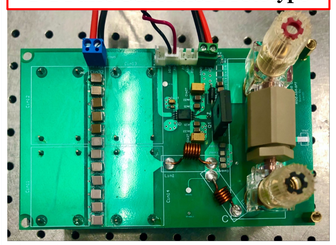
1×1 Pulse Generator Circuit



1×1 Pulse Generator SPICE Model

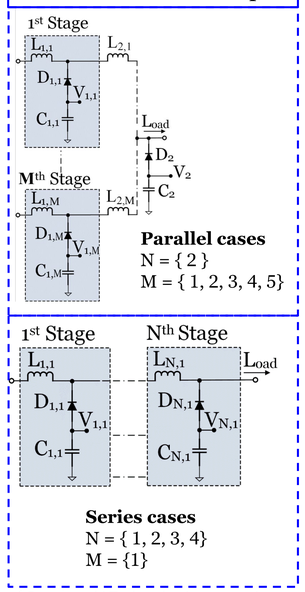


1×1 Pulse Generator Prototype



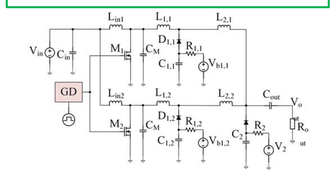
- ✓ Single stage-branch pulser.
- ✓ Used for diode evaluation F(V_{in}, V_{b1}, τ_{length})
- ✓ Informs DSRD product team of KPIs
- ✓ Generates ML training data

M×N Permutation Example

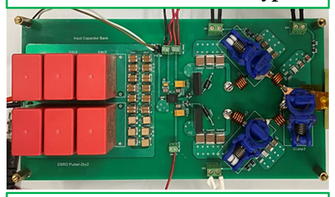


- ✓ Developed LTspice circuit permutations
- ✓ Determines optimal L_{xx} C_{xx} V_{xx} values
- ✓ Simulation results informs Pulser Team
- ✓ Automated data generated to train ML

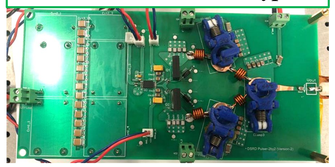
2×2 Pulse Generator Circuit



2×2 Pulse Generator Prototype V1

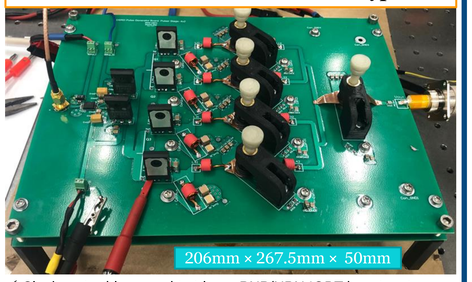


2×2 Pulse Generator Prototype V2



- ✓ Enables verification of SWaP-C
- ✓ Improved PRF capabilities with increased capacity of DC reservoir capacitor bank

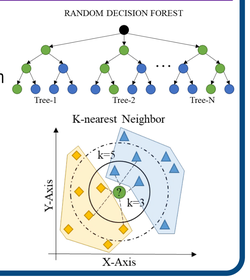
DSRD 4×2 Pulse Generator Prototype



- ✓ Single gate-driver used to trigger PNP/NPN IGBT booster stage
- ✓ Objective: produce 12.3 kV (3 MW) sharpened 500 ps t_{rise} pulses.
- ✓ Prime power rails and DC cap reservoir located under pulser to mitigate EMI/C issues causing spontaneous/spurious triggering.

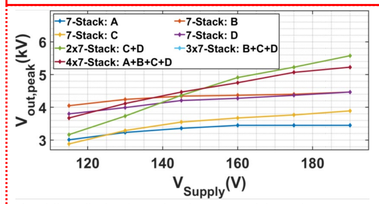
Machine Learning Optimization

M×N pulser simulation data is expedited by automated Python scripting to batch process data generated when sweeping through M, N, V, L, C parameters; fed to machine learning algorithms; training datasets generated to feed ML models; using feature selection the optimal features among input variables which maximize peak voltage and minimize risetime are produced.

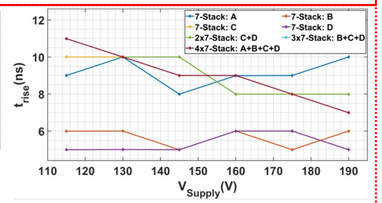


RESULTS

1×1 Pulser Experimental Results:
Individual vs. combination(s) of 7-stack DSRDs

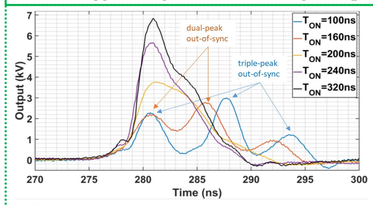


- ✓ Adding diodes in series (A, B, C, D) in series (A+B+C+D) does not result in double the peak voltage output.
- ✓ Optimal supply voltage not found due to MOSFET current limitation (< 102 A).

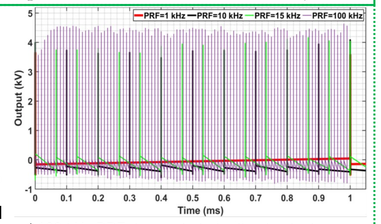


- ✓ Adding diodes in series within single stage does not result in doubled the risetime.
- ✓ Trends show that single diode is limiting risetime factor regardless of number of DSRDs in series. *e.g., @ 150 V, "A" has same risetime as "A+B+C+D"*

2×2 Pulser Experimental Results:
Trigger Length vs. Peak Voltage Output Optimization & 1-100 kHz PRF Study



- ✓ Regardless of single gate driver triggering of parallel branches, varying trigger length enables selection of optimal timing of inductive energy storage and release within the diode structures thus concealing diode-to-diode variability.



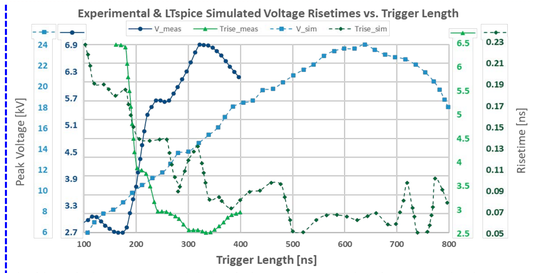
- ✓ 100-kHz PRF demonstrated without output voltage droop (purple) for 100-of-100 pulse burst.
- ✓ Initial voltage increase (purple) attributed to thermal equilibrium effects.

Influence of additional N stages and M series on peak power, risetime, and energy efficiency as a function of V, L, C

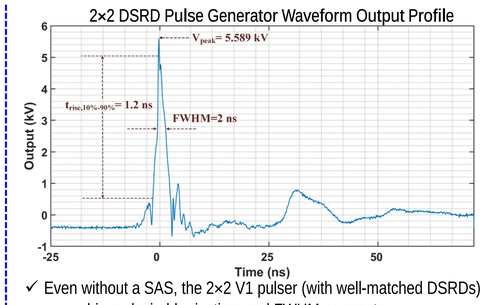
Case-by-Case Varied Parameters Simulated		Base Case ΔV=ΔC=ΔL=0		V Varied ΔV= ↑ ΔC=ΔL=0		C Varied ΔC= ↑ ΔV=ΔL=0		L Varied ΔL= ↑ ΔV=ΔC=0	
Stage-Branch Addition		'N' ↑	'M' ↑	'N' ↑	'M' ↑	'N' ↑	'M' ↑	'N' ↑	'M' ↑
Resulting Change in	Peak Power	↓	↑	↓	≈	↓	↓	↓	↓
	Risetime	↓	↓	↑	↓	↑	≈	↓	↑
	Efficiency	↓	↑	↓	↓	↓	≈	≈	≈

Red arrow indicates decreased performance result (negative)
Green arrow indicates increased performance result (positive)

- ✓ Adding additional stages in parallel in base case shows increased performance results across the board from SPICE simulations.
- ✓ Increasing bias volage and capacitance does not increase performance when adding additional stages in series.

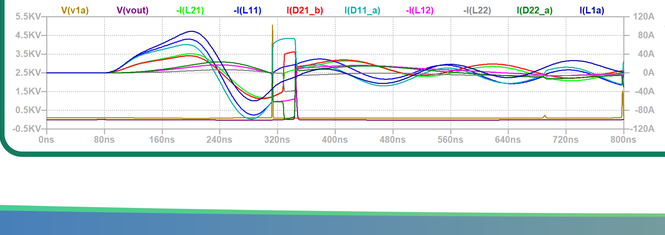


- ✓ Although the SPICE model simulation output's peak voltage and risetime trends match those of experiments, a 4× factor of peak voltage and an order-of-magnitude decrease in risetime of simulations is found and attributed to misrepresented model parameters.



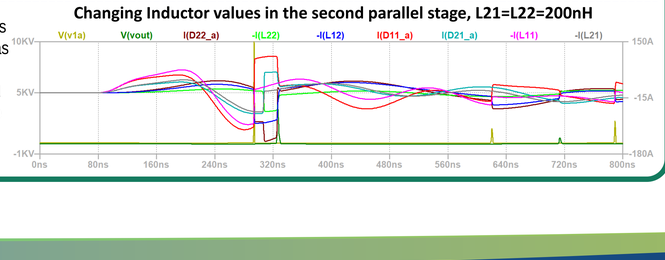
- ✓ Even without a SAS, the 2×2 V1 pulser (with well-matched DSRDs) can achieve desirable risetime and FWHM parameters.

Changing capacitor values in the second parallel stage, C21=300nF



Small changes in the pulsers ancillary components such as the inductor and capacitor values can have significant impact on the peak voltage produced through LTspice simulations.

Changing Inductor values in the second parallel stage, L21=L22=200nH



Shown in Table 1 are specifications in comp by Kesar et al. [1] usin the-shelf (COTS) DSR developed by Megaim DSRDs with silicon av characterization, SPIC analysis, and Machine (pulser parameters) o achieving the highest power density have be primary voltage bias, While each stage's cap matching are still imp consideration, KNN, coefficient) have little pulse generator, shou begin with.

Table 1

KPM	Units	MIDE - V1 Previous	MIDE - V2 Current
V_{supply}	V	225	180
T_{ON}	ns	100	340
V_{peak}	kV	5.59	7.35
Gain	V_{out}/V_{in}	24.8	40.8
$\tau_{rise,20-90\%}$	ns	1.2	1.142
dV/dτ	kV/ns	4.66	6.44
FWHM	ns	2	5.48
PW	ns	5	7
Z_{LOAD}	Ω	50	50
P_{peak}	MW	0.625	1.080
E_{pp}	mJ	0.125	0.154
PRF_{max}	kHz	100	100
Burst	shots	100	100
	%	100	100
SD_{Vpeak}	σ	> 2	> 2
	%	96.5	97.8

Completing the 4×2 p priority. We aim to ach ns risetimes, without to achieve 100 kHz PR density of >1 GW/m³ Next, we intend to m pulser's output with a 4×2 pulse generator a capacitive inver achieve a combined balanced differential This equates to a 12 pulse output with a 2 volumetric form-facto

[1] Kesar, A. S., Sharabani, Characterization of a dri Transactions on Plasma https://doi.org/10.1109
[2] T. Sugai *et al*, "Influence semiconductor opening Electrical Insulation, vo 10.1109/TDEI.2015.00
[3] Rev. Sci. Instrum. 92, 08
[4] P. Rulikowski and J. Bar with single power suppl Conference (IEEE Cat. N

This work was supported by the Office of Nava

[3]Lawrence Livermore National Laboratory, Livermore, CA

OBJECTIVE

Develop sub-nanosecond solid-state pulse sharpeners to produce multi-megawatt energy pulses from inductive energy storage (IES) and semiconductor opening switch (SOS) or drift-step recovery diode (DSRD)-based pulse generators.

OSPRES RELEVANCE

Solid-state sharpeners can replace bulky hydrogen spark-gaps and/or silicon photoconductive solid-state switch (Si-PCSS)-based sharpeners by achieving tens of picoseconds of pulse rise-time while providing >kHz of repetition frequency and more than a billion shots per device without compromising the SWaP–C cooling requirements of HPM cUAS systems.

STATE OF THE ART

- Hydrogen spark-gap (HSG)-based pulsers: ~25 GW, pulse risetime ~80 ps, limited pulse repetition frequency, and poor shot life ~10^3 pulses.
- SOS/DSRD–IES-based pulsers: >10 GW, >1 ns pulses.
- Magnetic compression lines (MCL) on SOS–IES-based pulsers: >54 GW, pulse risetime ~100 ps.
- Delayed breakdown diodes (DBD) and/or fast ionization dynistors (FID) on SOS–IES-based pulsers: >10 GW, >40 ps and pulse repetition rate >1 kHz.

Solid-state sharpeners are not available to purchase within the United States.

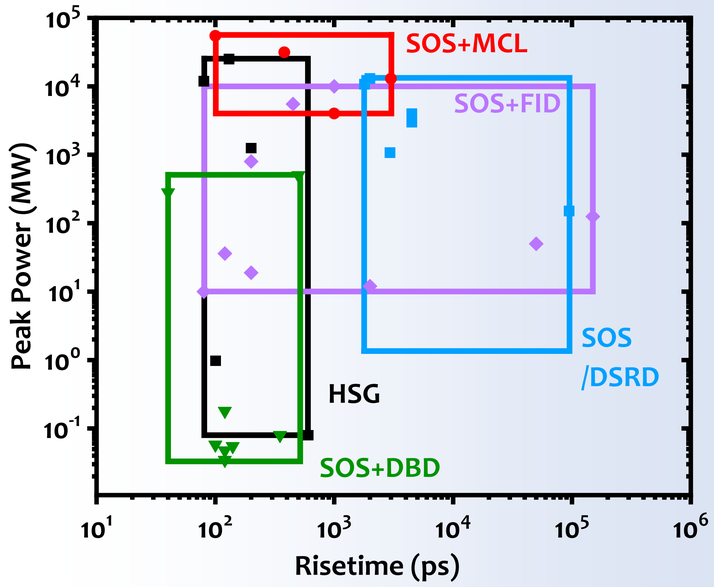


Figure (1). Peak power vs rise time for state-of-the-art devices[4–9]

SUM

Solid-state pulse s
on delayed impact
solutions for s
generation capable
used in HPM cUAS
sharpeners are not
and physics beh
understood. Here,
of a DSRD as a soli
in structure with t
High-voltage puls
generator will b
performance will
TCAD and LTSPI
optimize diode
geometry, size, and

BACKGROUND

Delayed impact ionization breakdown of semiconductor diodes (p^+–n–n^+) and dynistors (p^+–n–p–n^+) was observed by Russian scientist Igor Grekhov[1] in 1979. Such silicon structures, when overvolted by a sharply increasing voltage pulse (>1 kV/ns) in the reverse direction, become conducting due to the generation of a dense electron–hole plasma initiated by the impact ionization wave that sets up at twice the static breakdown voltage. The ionization wave propagates orders of magnitude faster than the carrier saturation velocity, thereby reducing the pulse risetime to tens of ps.

Semiconductor sharpeners such as silicon avalanche sharpeners (SAS) and fast ionization dynistors (FID), which use the delayed impact ionization, have been developed and successfully implemented in solid-state sub-nanosecond pulse generators primarily by IOFFE, Russia. However, the physics behind the initiating carriers for the impact ionization has always been puzzling. Some suggested mechanisms are the field enhanced ionization of deep electron traps (particularly the process induced defects at 0.54 and 0.28 eV)[2], surface state-assisted band-to-band tunneling of carriers, and electron injection from the non-ideal contact of the metal electrode and p^+-layer initiated by the sharp voltage rise rate[3]. These different mechanisms are expected to result in different switching speeds, current densities, and efficiencies. Thus, understanding the origin of initiating carriers and effect of device structure (doping profile, geometry, diode vs. dynistor) can lead to robust and efficient pulse sharpeners.

APPROACH

DSRD-IES based pulse generators producing ~7kV peak voltage with risetime <2 ns have been fabricated in our lab using silicon DSRD structures (p^+–p–n^+) and (p^+–p–n–n^+) prepared by diffusion and epitaxial growth procedures. DSRDs are structurally identical to SAS/DBD.

Use DSRD as DBD for pulse sharpening

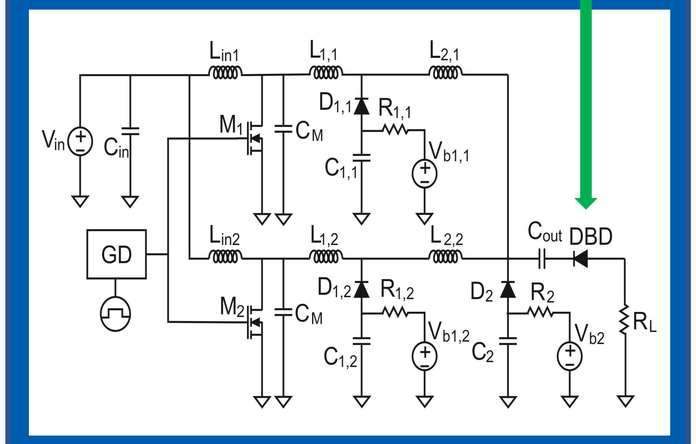


Figure (2). A schematic of DSRD-IES pulser circuit with a delayed breakdown diode as pulse sharpener

To sharpen pulses to sub-nanosecond risetime:

- Use DSRD as DBD
  - they are structurally identical.
- Delayed breakdown in DSRD is expected
  - even in absence of the so-called process induced defects.
  - May need higher input voltage rise rates (>5 kV/ns).
- Use TCAD Simulation to study device physics
  - Impact ionization
  - Doping profile
  - Size, Geometry
- Develop SPICE model of DBDs
- Use LTSPICE for circuit design and simulation
- Optimize Circuit, DBD doping profile, and device geometry to obtain
  - Shorter risetime, higher peak power, higher efficiency, better thermal performance, higher PRF.

REF

1. I. V. Grekhov an
Lett. 5, 395 (1979)
2. A. I. Gusev et a
1067–1078, 2014, d
3. V. Brylevskiy et
doi: 10.1063/1.5004
4. P. Rodin, J. App
doi: 10.1063/1.3465
5. S. N. Rukin, Rev
10.1063/1.5128297
6. I. V. Grekhov et
815, 2017, doi: 10.11
7. C. E. Baum et a
1107, 2004, doi: 10.1
8. E. A. Alichkin et
2020, doi: 10.1063/5

Distro A

This work was supported by the Office of Naval Research, Awar

Abstract

In the case of radiated electromagnetic fields where the ideal conditions are known, the optimal antenna geometry to produce that ideal is not always known. We propose a global search optimization approach using genetic algorithm techniques [1-2] for antenna geometries of the biconical type. This differs from standard gradient descent techniques because the solution space is not guaranteed to be strictly convex. While the scope is narrowly focused on a particular antenna type, it can be extended to other types, or even arbitrary geometrical constructions. Further, because of the exhaustive nature of the optimization algorithm, each iterative step provides multiple datapoints (10's to 1000's) that may be used as training data for more advanced prediction models.

Introduction To Genetic Algorithm

Genetic Algorithm (GA) is a biologically inspired optimization strategy based on the process of natural selection, which differs from traditional gradient descent methods. The principal idea of GA is to maintain a population of candidate solutions that "evolve" based on a given metric of fitness through the processes of crossover (mixing) and mutation (random perturbation). The process begins by defining a measure of fitness, this can be as simple as the maximum or minimum of some property of a solution, or a more complex derived measure of multiple metrics. Next, the tunable variables that affect the measure of fitness are identified, these are referred to as the genome. To start the iterative process, a population of randomly generated candidates is created. Once their fitness is determined, crossover is performed by mixing the genes of the most fit candidates. The iteration is finished by applying a mutation, i.e., a random permutation, to the candidate genes. This process described is visualized below in Figure 1.

1. Determine measure of fitness and genome
2. Randomize initial candidate population

   Begin Iterative Steps

   A. Calculate fitness of each candidate in the current generation
   B. Crossover (mix) most fit of the population
   C. Perform randomized mutation (perturbation) on new generation
   D. Repeat A-D until convergence criteria is met

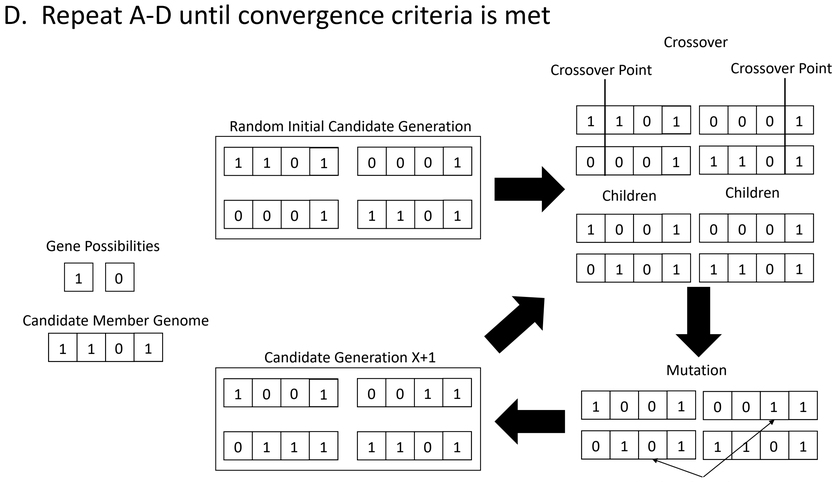


Figure 1: Flow chart of the genetic algorithm process.

Antenna Optimization Approach

The goal is to produce an optimal set of geometric specifications for a biconical antenna, given one or more of the desired properties of the antenna. As an example, we'll assume a single parameter optimization focused on the energy density E_d at some distance R. Figure 2 shows the schematic of one half of the biconical antenna. We note that when given the same input power considerations, the radiated field is dependent on the geometrical considerations of L_1, L_2, D_1, D_2, θ_1, and θ_2, while the other geometrical parameters are uniquely defined by these chosen parameters. These 6 parameters (12 for the whole bi-cone) will define our genome such that:

$$E_d \approx F(L_1, L_2, L_3, L_4, D_1, D_2, D_3, D_4, \theta_1, \theta_2, \theta_3, \theta_4)$$

and our fitness function or MOF is to maximize E_d :

$$MOF = \max E_d \approx \max F(L_1, L_2, L_3, L_4, D_1, D_2, D_3, D_4, \theta_1, \theta_2, \theta_3, \theta_4)$$

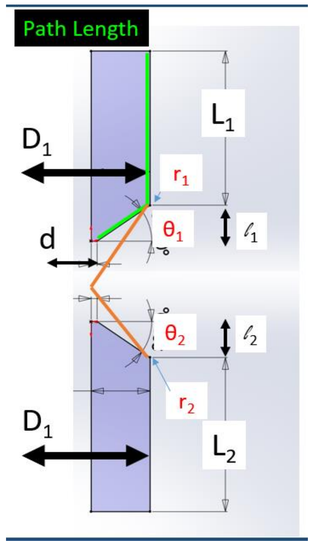


Figure 2: Schematic of one half of a biconical antenna.

The optimization would then proceed as described in the introduction. Unlike in the example, the genome will take on real numbered values associated with the measure of fitness (MOF). Calculating the MOF requires the use of external software packages such as CST or FEKO, and due to their computational complexity, it is recommended to only include the physics necessary for the desired result. We can describe the total computational time needed by the following:

$$T = P_t \cdot G_n$$

Where T is the total time, P_t is the time required to calculate all members of a population, and G_n is the number of generations necessary to achieve convergence. Actual numerical bounds on the required time are highly implementation dependent, as they are functions of the physics included in the simulation, the solver used by the simulation software, and the computational resources available. However, it can be confidently said that this method requires significant computational resources and is meant for larger computing clusters. However, there is significant upside with the generation of geometry candidates in this way. One, potential solutions may arise that would not be considered using conventional wisdom (i.e., non-obvious solutions). More importantly, every candidate generated, even less-fit candidates, will cover the solution space in such a way that will be well-suited for training models of the deep learning type, reducing the need for repeated searches in the future.

Summ

A strategy for optimizing antenna pro
antenna geometry is proposed. Utilizing
method requires the use of external pac
script wrapping the external package
approach has yet to be tested for use w
but has been utilized previously by the
computing packages requiring similar co
exploration remains on the specific probl

Further, with the use of full wave solvers
technique requires much computing tim
of significant disadvantage in the single u
every generation represents a significan
with enough generated data deep learnir
is important to use this method care
simulation results.

Future

- While this method has been implement
  computing packages. It requires Implem
  as outlined.
- Exploration of measures of fitness for d
- Exploration of convergence criterion for
- Exploration of meta-properties of the al
  population size, generations, EM softwa
- Application of generated data to deep-l

Refere

[1] Whitley, Darrell. "A genetic algorithm tu
(1994): 65-85.

[2] Storn, R and Price, K, Differential Evolu
Global Optimization over Continuous Spac
11, 341 - 359.

Acknowle

This work was supported by the Office of Nava

Primary Problem: Laminar-flow-based cooling technologies are limited in their ability to compensate average-power dissipation >1 kW/cm^2 of the thermal load of semiconductor-based pulse-power devices.

Sub-Problem: An order-of-magnitude greater fluid flowrate and two orders greater pressure drop with jet impingement (JI) technique is required without increasing SWaP-cost.

Relevance to OSPRES Grant Objective: Increased cooling performance facilitates semiconductor devices to operate at higher average-power.

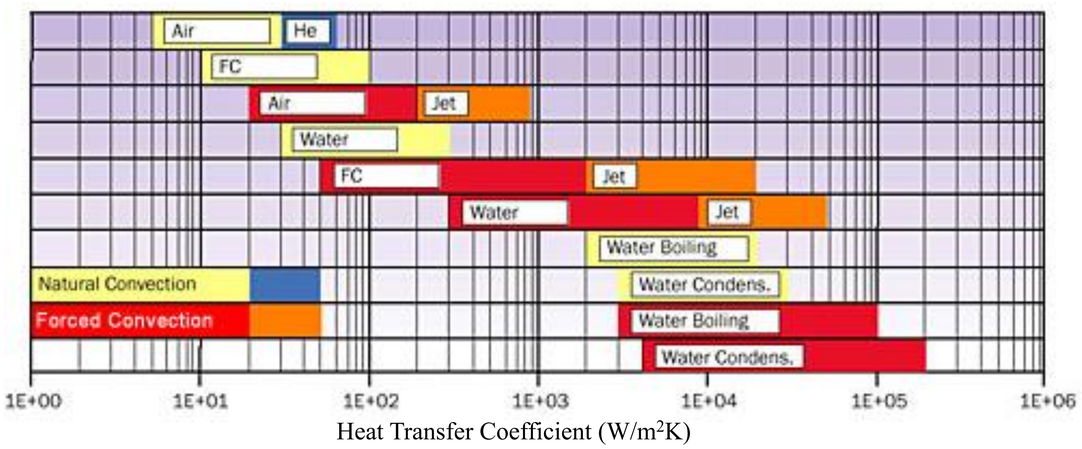
State-of-the-Art (SOTA): High power density electronics employing JI-TMS's have achieved 10's-of-kW of average power handling capabilities.

Deficiency in the SOTA: Chiller/pump systems consumption of power to produce thermal compensation, generate pressures (100's-of-psi) to achieve optimal flow regime and cooling metrics.

Solution Space: Utilize novel cooling technologies which employ non-laminar flow regimes (i.e., jet impingement thermal management system (JI-TMS)). Develop a JI-TMS able to compensate average-power dissipation >1 kW while maintaining the semiconductor temperature < 80 °C.

Background

Order of Magnitude for Heat Transfer Coefficients Depending on Cooling Technology



Methods

- CFD modeling was performed with ANSYS Fluent 2020R2.
- The model was simulated under the transition SST viscous model.
- Mesh sizes of the model ranged from 181k nodes up to 1.639M nodes.

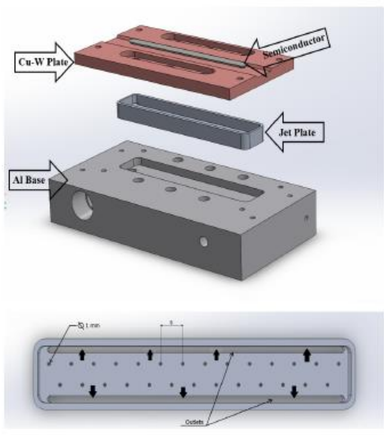


Figure 1. Exploded view of the CAD model in solidworks. The jet plate is shown in more detail beneath the exploded view.

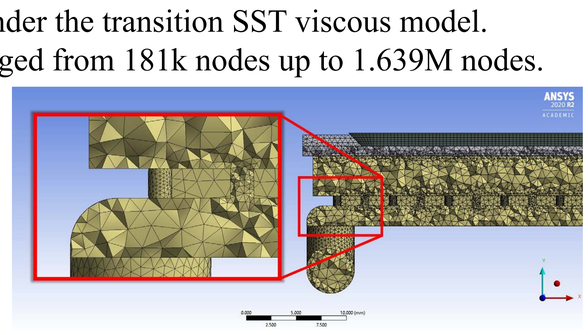


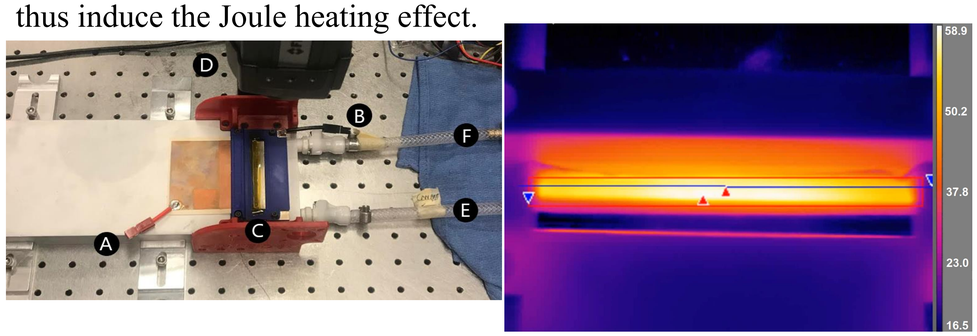
Figure 2. Cross-section of JI-TMS mesh in ANSYS

Table 1. Boundary conditions

Properties	Values
Mass flow rate	0.06 kg/s
Heat flux	100 W, 200 W
Inlet temperature	10°C

20cSt) was employed as heat transfer fluid (HTF).

- The power supply was set to apply 100 W and 200 W to the device and thus induce the Joule heating effect.



(a) (b)

Figure 3. (a) Complete Test Setup. A-Power, B-Earthing, C-semiconductor switch and TMS, D-FLIR Camera, E-Inlet, F-Outlet and (b) FLIR camera, semiconductor data during 100W experimental test

Results and Analysis

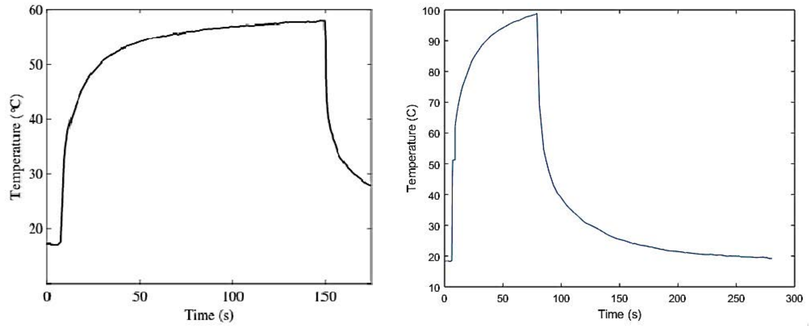


Figure 4. Experimental temperature variation results for 100 W (left) and 200 W (right) avg. power

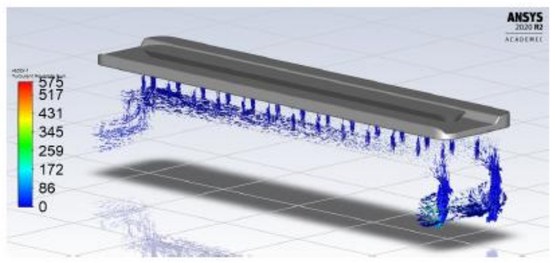


Figure 5. Reynolds number of the jet impingement TMS. The greatest Reynolds number achieved throughout the system is near the outlet, and reaches up to 574.8.

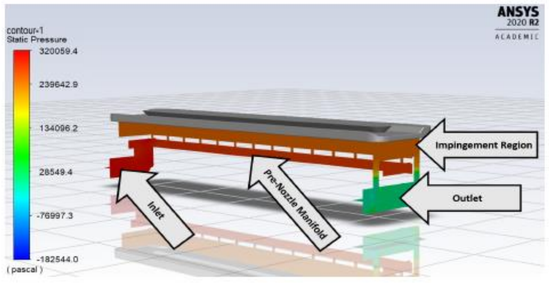
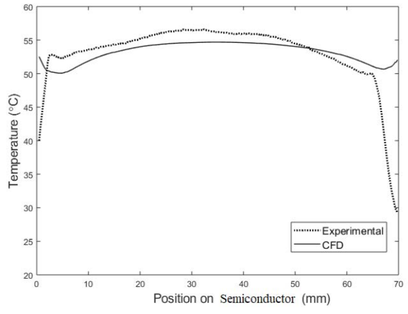


Figure 6. Pressure distribution along semiconductor. The mass flow rate of 0.06 kg/s yielded a pressure drop of 318,660 Pa across the entire TMS. While the pressure drop could be handled by many commercially-available pumps, the model could be improved to accommodate the flow rate.

Figure 7. Spatial temperature distribution along semiconductor for 100 W avg. power test:
The cross-validation results between CFD and experimental analysis show a good agreement with average error of around 5.9%.



	S
100 W Avg. Power	
200 W Avg. Power	

Table 3. Heat capacity value
3 sampl

Results
DSC results
Vendor Values
Deviation percentage

➢ The 13% difference in the
for the difference in the sin

Sur

- The results from this stu
device's temperature is w
operating temperature for 1
proposed JI-TMS.
- The results for 200 W avg
with the numerical data,
exceeds the threshold temp
geometry will not be pursue
- Based on the pressure dr
proposed cooling system is

A more optimized
as the or

Refe

- Berg, J. N., Allen, R. C., & Sobhansar
semiconductor device through a jet impinger
experimental evaluation. International Journa
- M. Angioletti a , E. Nino a , G. Ruocco, 200
its validation by particle image velocimetr
Journal of Thermal Sciences 44 (2005) 349–
- Bovo, Mirko, 2011. "On the numerical mode
Applied Mechanics CHALMERS UNIVERS
- Hosain Lokman, 2013. "CFD Simulation of
GPU". Royal Institute of Technology School

Acknow

The authors wish to thank the
support of this work under Gra

DEPS DE Systems

UMKC School of Computing and Engineering

Office of Naval Science & Tech

in their ability to compensate average-power dissipation >1 kW/cm^2 of the thermal load of semiconductor-based pulse-power devices. The dielectric heat transfer fluids (HTF) utilized in such systems, possess thermophysical fluid properties that inhibit their ability to achieve >1 GW/m^3 cooling densities.

Sub-Problem: Pure silicone fluid with viscosity of 20 cSt (PSF-20cSt) is ~15 times more viscous than water, and therefore requires increased pumping power within the thermal management system (TMS).

Relevance to OSPRES Grant Objective: Increased cooling performance facilitates semiconductor devices to operate at higher average-power.

State-of-the-Art (SOTA): Nanofluids have been shown to increase the thermal conductivity of base-fluids by 12% in comparison to the generic dielectric fluid alone; resulting in greater cooling density and decreased pumping power.

Deficiency in the SOTA: The addition of nanoparticles in base-fluids results in a tradeoff between thermophysical properties, i.e. the addition of nanoparticles can increase the thermal conductivity, while also increasing viscosity of the mixture.

Solution Space: Develop a nanofluid by entraining ceramic nanoparticles in the dielectric base-fluid to increase the nanofluid's thermal conductivity, thereby improving cooling density capabilities. Utilize a nanofluid with desirable thermal properties that can serve as a viable heat transfer fluid (HTF) for TMSs in high power density electronics.

Background

PSF-20cSt vs water
4 times less heat capacity and thermal conductivity!

How to increase thermophysical properties?

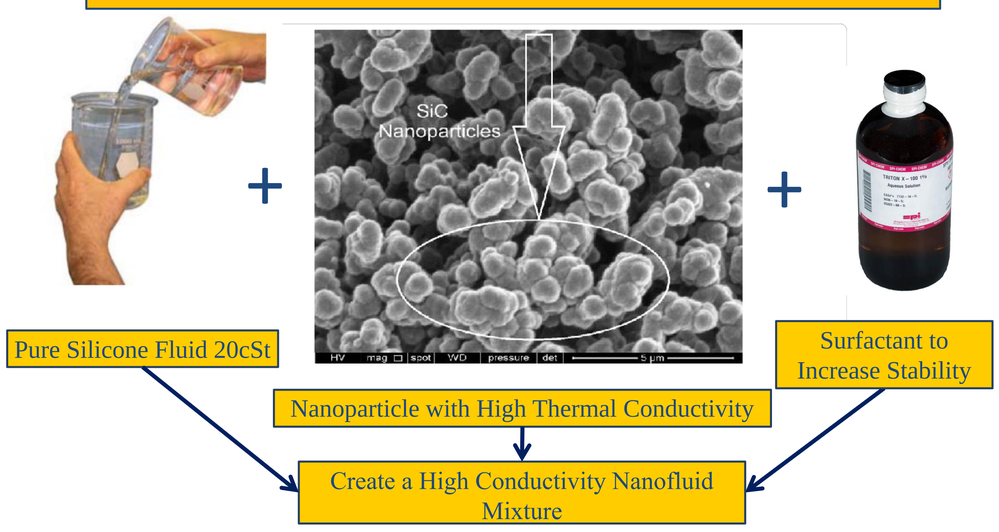


Table 1. Thermal conductivity of nanoparticle chosen

Material	Thermal Conductivity (W/mK)
Silicon Carbide	20.7
Iron(II,III) Oxide	5.8
Aluminum Oxide	38.5
PSF-20cSt	0.142

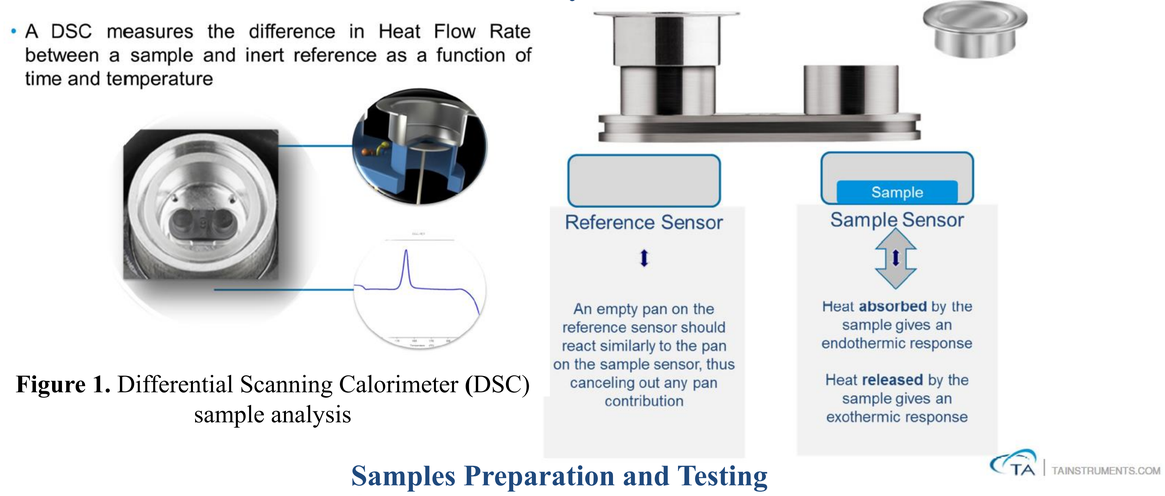
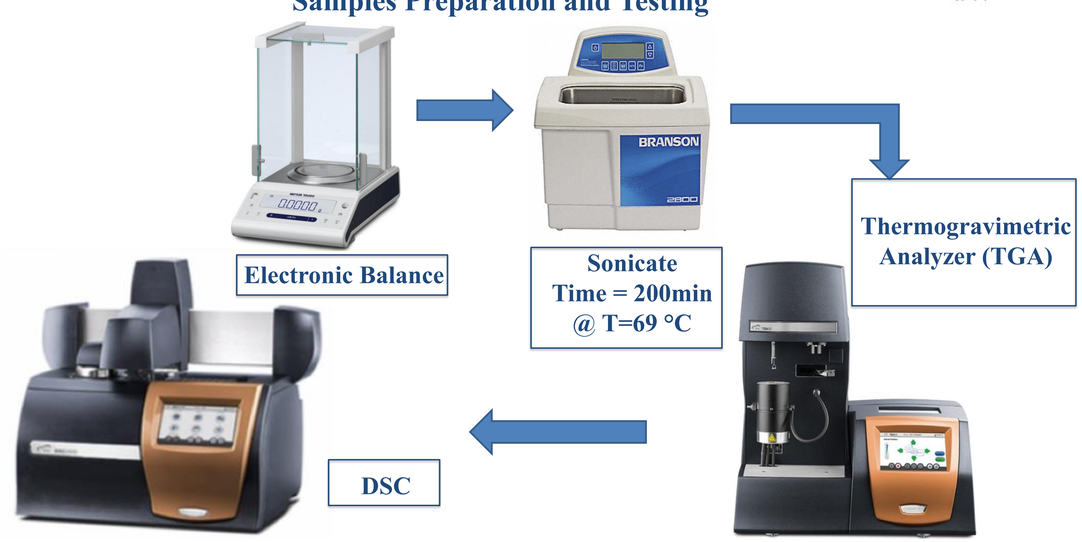


Figure 1. Differential Scanning Calorimeter (DSC) sample analysis

Samples Preparation and Testing



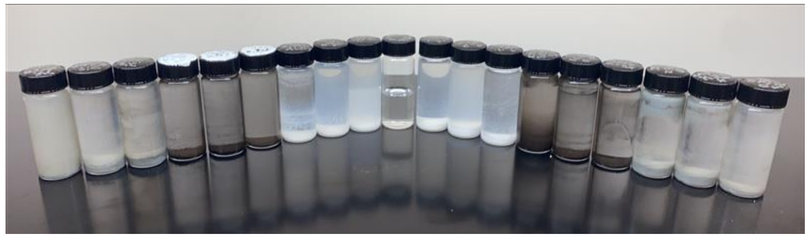


Figure 2. PSF-20cSt plus percentage variation of alumina, silicon carbide and iron (II,III) oxide with and without surfactants

Results and Analysis

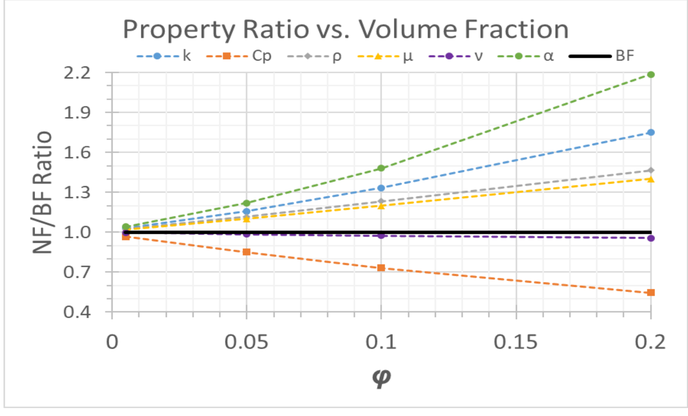
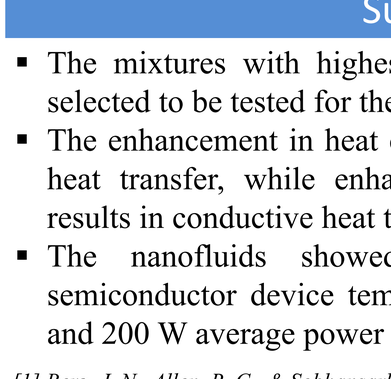


Figure 3. Thermophysical properties of SiC-PSF-20cSt nanofluid vs base fluid at constant temperature for various volume fractions, predicted by theoretical formulations

enhancement of 15.2% an
10.1% compared to pure P



(a)

Figure 4. (a) SiC-PSF-20cSt
nan

- In order to investigate the
the achieved thermophysic
nanofluid was applied into
(CFD) modeling software
results are shown in Table

Table 2. Comparison of heat tra
semiconductor

HTF	100 W
PSF-20cSt	
Sample 1 k value(theory)	
Sample 1 k value(measured)	
% Improvement (theory)	
% Improvement (measured)	

❖ *where Sample 1 HTF is a mix*

Su

- The mixtures with highes
selected to be tested for the
- The enhancement in heat
heat transfer, while enha
results in conductive heat t
- The nanofluids showed
semiconductor device tem
and 200 W average power

*[1] Berg, J. N., Allen, R. C., & Sobhansarl
semiconductor device through a jet imping
and experimental evaluation. Internationa*

Ackno

The authors wish to thank the
support of this work under Gr

DEPS DE Systems

UMKC School of Computing and Engineering

Office of Naval Science & Tec

maintaining the semiconductor device temperature below 80 °C. The goal is to create an ultra-compact cooling unit with the ability to rapidly remove 1 kW/cm^2 of heat.

Sub-Problem: The turbulency formed from the array of nozzles creates an extreme pressure loss. With a large amount of jet nozzles (over 200) and a flow diameter of nearly 100 microns, the pressure across the system will decrease tremendously. The pressure must be sustained to enable proper cooling and circulation processes. Another way to sustain pressure is to use different liquids. Different types of coolant will be simulated to determine effects from fluid density and viscosity. Preliminary studies show that pressure loss can be maintained using DI water or a type of gas while still requiring a small amount of pumping power.

Relevance to OSPRES Grant Objective: Increase cooling densities for high pressure microwave (HPM) systems, while decreasing pumping power requirements, in-line with the SWaP-C^2 objective.

State-of-the-Art (SOTA): Integrated chip cooling, used to dramatically increase the operational power of high voltage silicon-based power devices is reached by increasing the power device heat-removal via an integrated active cooling microelectromechanical system (MEMS) within the power chip device.

Deficiency in the SOTA: The manufacturing techniques of the semiconductor chips have not yet been used for integrated chip cooling systems. These designs are limited due to low tolerance of the manufacturing process. With a proper design implemented, the pressure drop, and heat dissipation rate are large contributors to a properly functioning system.

Solution Space: To achieve such high heat flux, a turbulent flow profile must be achieved. The approach we are going to take is to create an ultra-compact unit integrated onto a semiconductor device, allowing more heat extraction to occur. The pumping power will be kept to a minimum since the unit to be prototyped will represent 1 cm^2 surface area. This enables less power to be consumed to create a turbulent flow. An array of micro-sized jet nozzles will provide a turbulent flow onto a microchannel section directly on the semiconductor device. The ultra-compact design will reach turbulency at a faster rate while requiring less energy consumption.

Background

Enhancing previous jet impingement thermal management system (TMS) research in a smaller scale brings other methods to the table such as micro-channels to increase heat extraction. Common microchannels are basic fin geometries to enable quicker heat dissipation. Forwarding the idea of an integrated jet impingement TMS enables greater contact between the coolant and the high-power switch shown in Figure 1. The objective will be reached as the micron scaled cooling unit is to be integrated onto a semiconductor device, letting more heat extraction to occur.

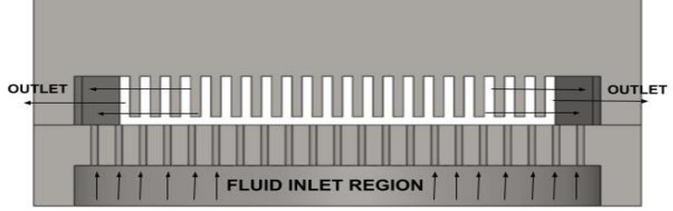


Figure 1. Initial Concept Model Cross-Sectional View

The preliminary design consist of an array of 421 nozzles and 22 microchannel heat sinks embedded onto a semiconductor as shown in Figure 2. An array of micro-sized jet nozzles will provide a turbulent flow onto a microchannel section directly on the semiconductor device. From previous literature, the geometry of the nozzle to microchannel was determined to reach maximum performance with a height/depth ratio of 0.8.

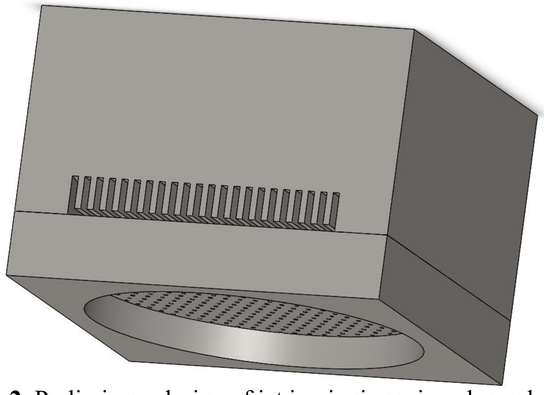


Figure 2. Preliminary design of jet impinging microchannel device

Methods

Each design will be studied using ANSYS Fluent, a computational fluid dynamics (CFD) analysis tool. A CFD analysis was performed where a semiconductor switch had heat applied, and the temperature was monitored. The model that kept the switch the coolest included microchannel fins. Errors arose while meshing this device as the dimensions range from 3 mm to 0.003 mm. Matching the mesh was an issue and led to low orthogonal quality and high skewness. This issue was fixed by individually face sizing certain bodies of the device and fluid domain. A lowest orthogonal quality was reached of 0.172, where the minimum for quality results is 0.1. The fine meshing consists of nearly 1.5 million nodes and nearly 9 million elements spread throughout the 3 x 3 mm TMS.

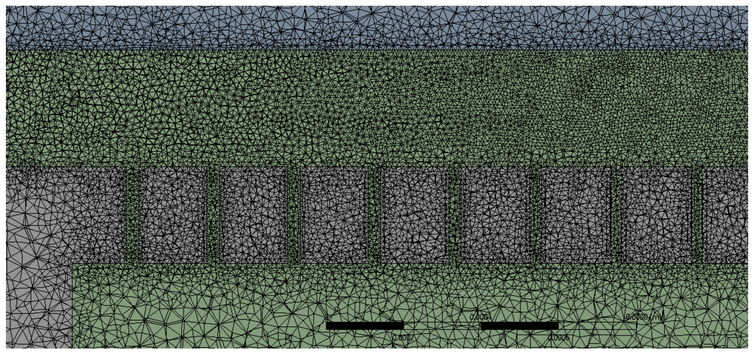


Figure 3. Jet Nozzle Meshing Cross-Sectional View

design process as this thermal managem
the semiconductor itself. The nozzle dia
produce a ratio of 0.8 for the h
microchannel fins are 0.25 mm tall, 0.
.05 mm space to ensure proper flow. Fo
temperature of 360K is applied body of

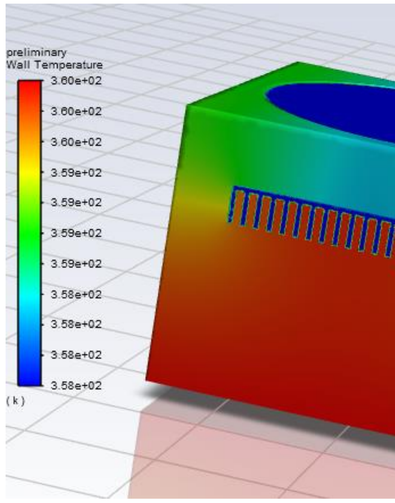


Figure 4. Preliminary Simulation

The contour in Figure 4 shows the effec
as more heat extraction occurs through
of sizing and flow profiles, the pressure
causing more design analysis to reduce

Summa

From previous literature and prelimina
microchannel jet impingement cooli
semiconductor is superior to TMS attac
having microchannel fins resulted in
semiconductor. Following simulations,
future experimental data.

Acknowled

The authors wish to thank the Office of
this work under Grant No. N00014-17-1

DEPS DE Systems Symp

UMKC School of Computing and Engineering

Office of Naval Research Science & Technology

Ansy

Problem Space: System volume, weight, and cost are limited resources in many high-power microwave (HPM) applications necessitating miniaturization of system components.

Solution & Primary Objective: Design a diode-based nonlinear transmission line (D-NLTL) capable of shift in spectral content up to the single GHz regime at single MW peak powers to optimize volume, weight, and cost of the pulse shaping network (PSN) within a larger HPM system similar to the set up shown in Fig. 1.

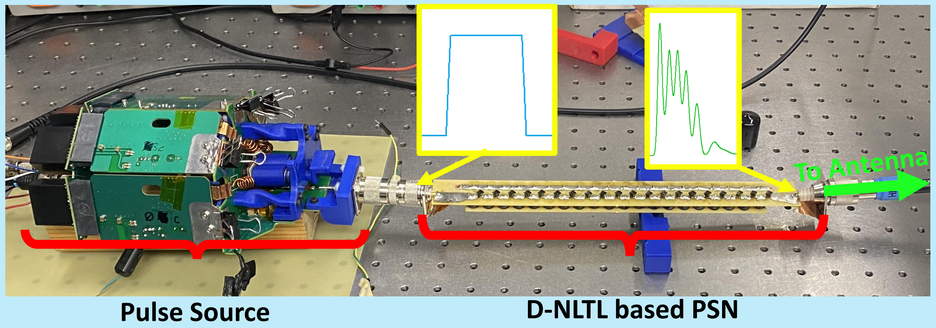


Figure 1: An example HPM system with a D-NLTL PSN. A source generates a pulse, a D-NLTL shapes the pulse increasing frequency content, the pulse is radiated from an antenna

Diode-Based NLTL Background

General: Diode-based nonlinear transmission lines (D-NLTL) represent a class of transmission lines with a nonlinear capacitive reactance provided by the reverse PN junction of a diode. D-NLTLs shift spectral content to higher frequencies by breaking a pulse into sequences of solitons.

The voltage-dependent capacitance provided by a reverse bias PN junction causes high amplitude portions of a signal to propagate at a greater rate than small amplitude portions. The amount a given D-NLTL will reduce a rise time is determined by the chosen components and line geometry. If excitation rise time is small enough for the line to reduce the rising edge below zero, a shockwave is formed in the line. Shockwaves are balanced by dispersion provided by the lumped element structure forming solitons.

Measurements: Fig. 2 shows an example of a D-NLTL waveform. The three waveform characteristics of interest are:

(a) **Center frequency F_c**: Estimated by the inverse of the time between solitons. Gives the peak power in frequency domain.

(b) **Amplitude**: Characterizes peak power generation (P_{peak}), given by the height of the first soliton.

(c) **Bragg frequency F_{Bragg}** : Max frequency, measured as the inverse of the 10-90% rise time of the pulse.

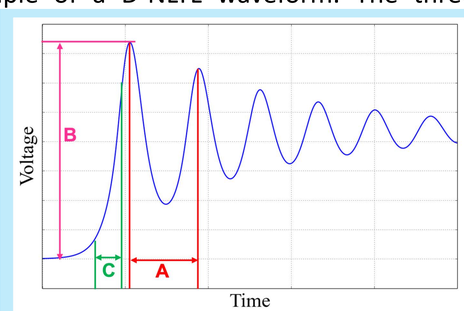


Figure 2: An example waveform generated by a D-NLTL with characteristics of interest labeled. (A) Center frequency, (B) Amplitude, (C) Bragg frequency.

Method:

Four Different excitation sources were chosen to excite D-NLTLs based on K50F and K100F diodes. Varying geometries from each source cause a variety of D-NLTL behaviors, including edge sharpening, soliton formation, and low pass characteristic. In all cases, source waveforms are collected without a D-NLTL attached. In the PCSS and Marx cases, source measurements are at a lower amplitude than with the D-NLTL attached.

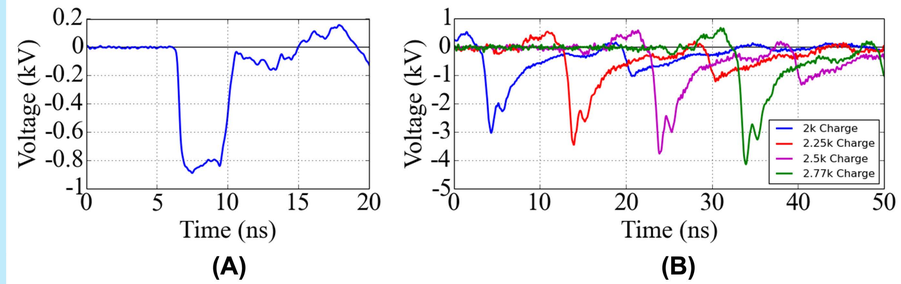


Figure 3: (A) PCSS Pulse geometry. (B) Results on the K50F D-NLTL for 4 charge magnitudes of the PCSS.

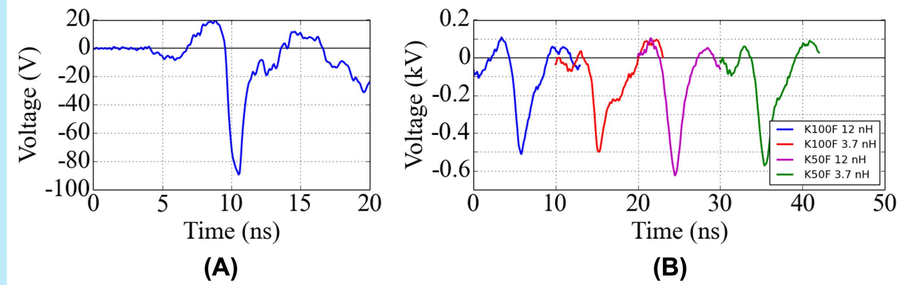


Figure 4: (A) PCSS pulse used for K50F and K100F comparison. (B) Waveforms produced by the K50F and K100F lines for inductances of 12 nH and 3.7 nH

Set up: A PCSS based source was used to excite the D-NLTLs with a square pulse geometry, shown in Fig. 3a. Pulse geometry consisted of a rise time of 440 ps, full width at half max (FWHM) of 3.8 ns and control over excitation amplitude based on the charge on the PCSS transmission line prior to triggering the switch.

Results: Fig. 3b shows the K100F line breaking the pulse from Fig. 3a into solitons with a **F_c of 756 MHz** and **F_{Bragg} of 1.25 GHz**. During K50F-K100F comparison tests the PCSS produced a pulse with geometry shown in Fig. 4a. Due to the steep rise time and narrow geometry both D-NLTLs demonstrated a low pass characteristic filtering significant pulse energy to ground.

Marx Generator

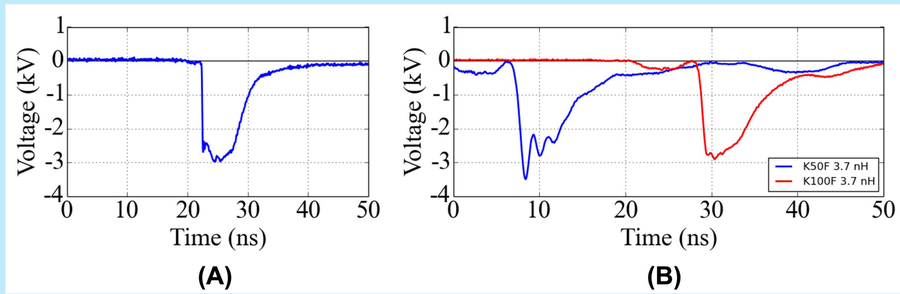


Figure 5: (A) Marx Generator pulse geometry. (B) Results for a 5 kV Marx Generator charge on the K50F (blue) and K100F (red) D-NLTLs.

Set up: A Marx generator was chosen as an excitation source due to a 6.8 ns full width at half max (FWHM), wide enough for each D-NLTL to break into a sequence of solitons. Reflections at the source-line interface caused each D-NLTL to be excited by a 5 V pulse.

Results: The K100F line generated a **F_{Bragg} of 1.19 GHz** but, did not break the pulse into solitons. The K50F line broke the pulse into solitons with a **F_c of 595 MHz** and a **F_{Bragg} of 926 MHz**. Differences between each line shown in Fig. 5b represent the only observed instance of waveform differences other than **F_{Bragg}** or amplitude

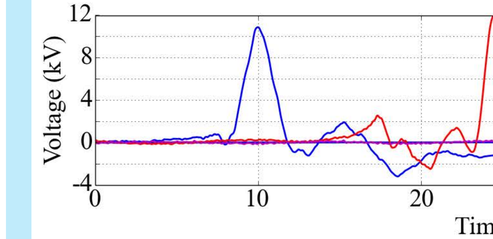


Figure 6: D-NLTL with DSRD excitation. (Blue) D (purple) K100F D-NLTL waveform.

Set up: A DSRD based half barrel source w its ability to fully saturate the diodes in e of 1.2 ns, and a FWHM of 1.75 ns (Fig. 5 b

Results: The K50F line (Fig. 5 red) produ **2.88 MW**. The K100F line (Fig. 5 purpl **P_{peak} of 2.33 MW.**

Megai

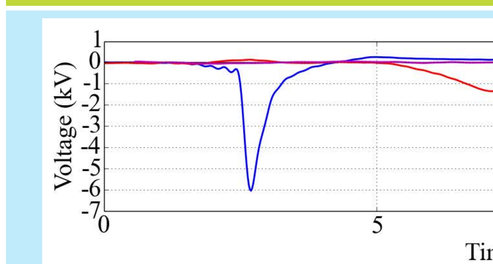


Figure 7: D-NLTL with Megaimpulse excitatio D-NLTL waveform, (purple) K100F D-NLTL wave

Set up: A ppm0732 pulse generator by M pulse of rise time 160 ps and FWHM of 38

Results: The rise time and FWHM of the above the F_{Bragg} of 1.4 – 1.6 GHz meas both D-NLTLs to filter all frequencies abo and purple waveforms displayed in Fig. 7.

Summary and

Summary: D-NLTLs need to demonstr Frequencies above 1 GHz to be a measurements above 1 GHz in PCSS, Ma MW for each line in DSRD testing bot achieve both metrics. However, a GHz lev NLTLs showed progress towards that g generator pulses into solitons with F_c in th line and 595 MHz with the K50F line respe

Future Work: Future research will focus o

1) Retest the lines with the PCSS and M pulse amplitudes. The source amp represents less than half of the 12 tests.
2) Use the average impedance of the matching at the source-line interfa increase the percentage of pulsed e saturating the diodes and increasing

[1] E. G. L. Rangel, J. O. Rossi, J. J. Barroso, F. S. Yamasaki, and E. Schamiloglu, "Practical constraints on nonlinear transmission lines for RF generation," *IEEE Trans. Plasma Sci.*, vol. 47, no. 1, pp. 1000–1016, 2019, doi: 10.1109/TPS.2018.2876020.
[2] D. S. Ricketts, E. Shi, X. Li, N. Sun, O. O. Yildirim, and D. Ham, "Electrical Solitons for Microwave Systems," *Microw. Mag.*, vol. 20, no. 4, pp. 123–134, 2019, doi: 10.1109/MMM.2019.2891382.

This work is supported by the Office of Naval
Di

Dept. Physics and Electrical Engineering, University of Missouri-Kansas City, Missouri Institute for Defense and Energ

OBJECTIVE

Determining the extent to which the physical aperture size of an antenna array, composed of microstrip electrically small antenna (ESA) elements, can be reduced, while maintaining performance in peak power density, bandwidth (BW), and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

STATE-OF-THE-ART

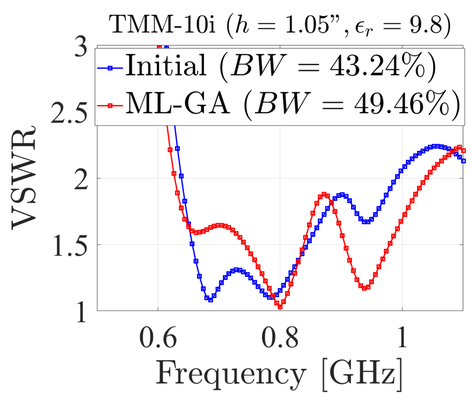
Horn, reflector, Vivaldi, valentine, etc. are commonly used ultra-wide-band antenna elements in a phased array for HPM transmissions. However, these antennas have the disadvantage of ***large physical aperture size***.

SOLUTION PROPOSED

1. Usage of wideband microstrip ESAs as array elements.
2. Performance optimization of antenna elements via Machine Learning (ML) based search algorithms and Pareto Optimality.
3. Arrangement of ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area.
4. Performance optimization of the arrays using ML and Pareto Optimality.

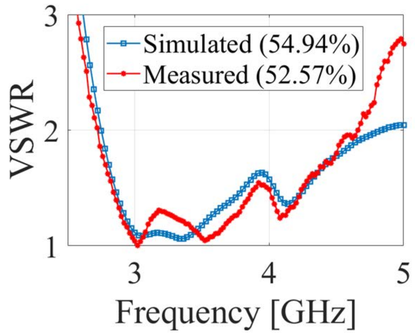
SINGLE ESA ELEMENT DESIGN

- ❑ A simple coaxial probe-fed microstrip ESA element is designed, using FEKO, at the UHF range (0.6-1 GHz), on a circular shaped, 1.05" thick TMM-10i substrate ($\varepsilon_r = 9.8$, $\tan\delta = 0.002$).
- ❑ Around 43% BW is obtained when the probe is placed along 2/3rd of the patch diagonal [1]. (Note: Conventional designs have ~8-10% BW)
- ❑ The BW performance of the ESA element is further improved using ML based Genetic Algorithm (GA), via Altair HyperStudy.
- ❑ Training data taken from FEKO; optimization parameters include ground plane size, probe radius, and probe location.



GA Optimized Antenna Parameters	Value
Aperture Area (m²)	0.0026
Volume (m³)	6.93×10^{-5}
Max. Gain (dBi)	4.97
rE/V at 10 m	0.7895
Avg. power handling capability (W)	120.55

EXPERIMENTAL VALIDATION OF THE ESA DESIGN

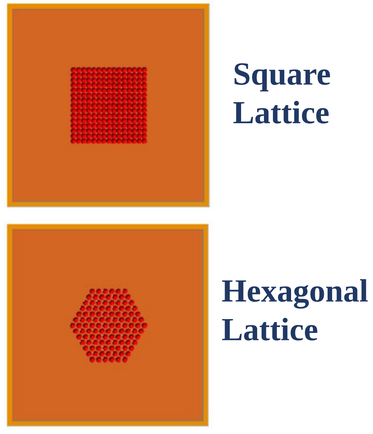


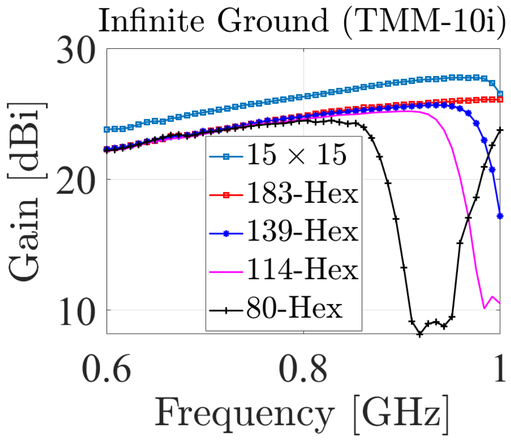
Frequency Range (GHz)	Radiating Aperture Area (mm²)	rE/V (at 10 m)
2.5 – 5	138.58	0.7855

- ❑ Due to availability of sample substrate panels, the design methodology is first validated at the S-band, on a circular shaped 0.25" TMM-10i substrate.
- ❑ The simulated and the measured VSWR data are shown to have good agreement.
- ❑ The rE/V value is computed, via CST, by subjecting the ESA element to Gaussian pulse type voltage excitation.

TRADESPACE ANALYSIS OF ESA ELEMENT ARRAYS

- ❑ Planar arrays, composed of the designed ESA elements at the UHF range, of various lattice formation and size, are investigated.
- ❑ Transformation from square to hexagonal lattice resulted in 30% reduction in aperture area with < 3.5 dBi loss in gain, and no scan blindness spotted as the main beam is steered from boresight to $\pm 60°$ in the 640 – 990 MHz range.





MINIMIZATION OF MU BETWEEN ARRAY ELEM

- ❑ A 5×5 array of microstrip ESAs, with only the center- and the corner-most elements excited.
- ❑ Optimization parameter: Inter-element spacing.

ML optimization resulted in slig frequency end, and at a smalle reduced array aperture area).

SUMMARY

- ❑ A novel, wideband, microstrip > 40% BW) is presented with
- ❑ Around 6% improvement in element parameters via ML alg

Single Antenna Element Type	U- Ante
BW (%)	4
Aperture Area (m²)	0.0
Volume (m³)	5.23
Gain (dBi) at 900 MHz	~
rE/V	Unk

- ❑ Comparison of different array with 30% reduction in the ape elements), the gain drops by <
- ❑ Minimization of a single object a single array parameter h illustrative example.

FUTURE WORK

- ❑ Multi-objective optimization ML algorithms and Pareto Opt
- ❑ Manufacturing and testing prototypes at the UHF range.

ACKNOWLEDGEMENT

This work was supported by th Grant No. N00014-17-1-3016.

REFERENCES

[1] B. Barman, K. C. Durbhakula, B. Bissen, D. Chatterjee and A. N. Caruso, "Performance Optimization of a Microstrip Patch Antenna using Characteristic Mode and D/Q Analysis," *2020 XXXIIIrd General Assembly and Scientific Symposium of the International Union of Radio Science*, 2020, pp. 1-4.
[2] A. K. Shackelford, Kai-Fong Lee and K. M. Luk, "Design of small-size wide-bandwidth microstrip-patch antennas," *IEEE Antennas Propag. Mag.*, vol. 45, no. 1, pp. 75-83, Feb. 2003.
[3] Z. Jian, X. Zhang, and S. Xiao, "Antipodal Vivaldi antenna to detect UHF signals that leaked out of the joint of a transformer," *International Journal of Antennas and Propagation* 2017.

bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power. The BAVA design parameter space has been exhausted over the past couple of decades.

Solution Proposed: We propose integrated impedance transformer & balanced antenna element designs for improved impedance matching. In general, our approach is to design, simulate, validate, and perform a tradespace study on the important design parameters of the UWB antenna elements and arrays that effectively reduce its physical aperture area while maintaining its UWB properties, both in frequency and time domains.

Significance: This study could help identify an unconventional array geometry specific to both antennas with reduced physical aperture area while retaining similar metric values as traditional square geometry.

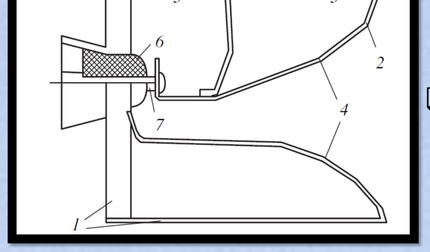
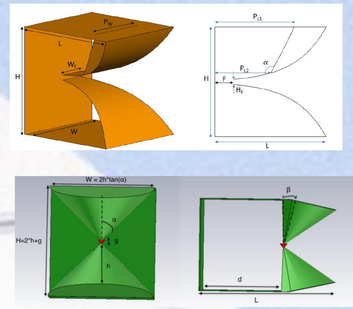


Fig. 1. Geometry of the Koshelev antenna. (1) Body, (2) Electrical monopole, (3) Magnetic dipoles, (4) TEM horn, (5) Plate, (6) Feedthrough insulator and (7) Central electrode.

- The Koshelev antenna combines TEM horn, magnetic dipoles and electrical monopole to yield UWB characteristics.
- The Shark antenna is a modified design of bicone antenna with a back reflector.

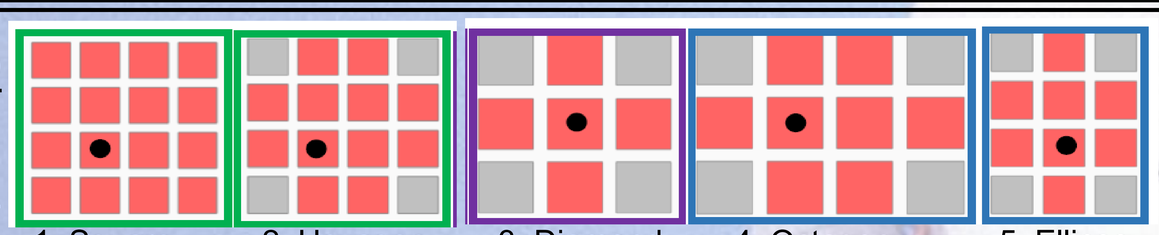
3. METHODOLOGY



CST

Solves for electromagnetic fields in time domain using Maxwell's grid equations

4. SIMULATED ARRAY GEOMETRIES



1. Square 2. Hexagon 3. Diamond 4. Octagon 5. Ellipse

5. RESULTS

Geometry	No. of elements	Aperture area [m²]	Peak Gain 900 MHz [dBi]	Aperture efficiency [%]	rE/V (10 m)
Square	9	0.1504	13.09	120	5.52
Diamond	5	0.074	11.47	167	3.07

Table I. Koshelev antenna array metrics comparison

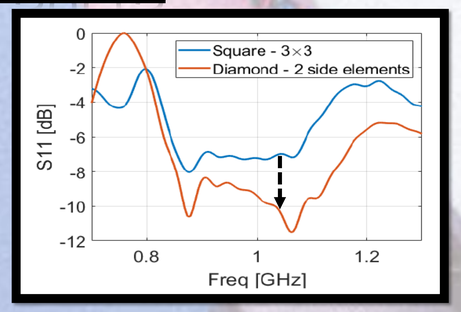


Fig. 3. S11 of center element (black dot)

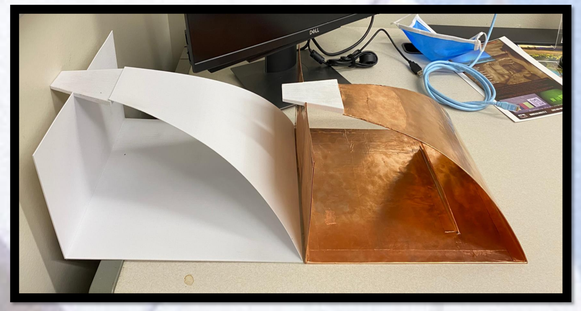


Fig. 4. 3D printed (white) and metalized parts of single element Koshelev antenna

Geometry	No. of elements	Aperture area [m²]	Peak Gain 900 MHz [dBi]	Aperture efficiency [%]	rE/V (10 m)	HPBW (E-plane)	HPBW (H-plane)
Square	9	0.211	12.719	53.13	9.15	40.2	36.2
Hexagon	8	0.197	11.73	52.37	8.12	22	32.4
Ellipse	8	0.21	12.40	52.30	8.05	24	40

Table II. Shark antenna array metrics comparison

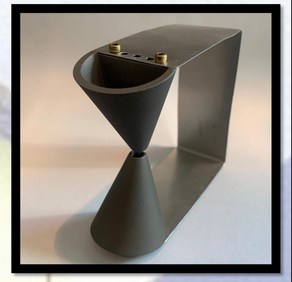


Fig. 5. 3D printed and nickel painted single element Shark antenna

- This study revealed that the diamond array geometry is the optimum shape for the Koshelev antenna, as shown in Table I. Mutual coupling has been reduced, which can be seen in Fig. 3. This leads to improved realized gain. In addition, the interelement spacing value (in E-plane and H-plane) study yielded that the spacing value in E-plane has least effect on most of the antenna array metrics.
- On the other hand, the elliptical Shark antenna was found to be an optimum choice based on the metrics comparison, which can be found in Table II. Furthermore, the Shark antenna array is more sensitive to the interelement spacing variable in the H-plane than in the E-plane.
- 3D printed and metalized single element antenna prototypes (Fig. 4 and Fig. 5) are currently under test.

6. SUMMARY

- Non-square antenna arra coupling significantly wh dBi of peak gain and efficiency. In some cas increased for non-square
- We found that in both ar and Shark), the time do sensitive to spacing in than in the vertical axis (
- Shark antenna array wit the H-plane yielded unconnected/individual b

7. REFE

1. Gubanov, V. P., et al. "Sources of with a single antenna and a multiele *Techniques* 48.3 (2005): 312-320.
2. L. Desrumaux, A. Godard, M. Lalan "An Original Antenna for Transien Antenna," in IEEE Transactions on pp. 2515- 2522, Aug. 2010, doi: 10.1

The authors wish to thank the Office of Naval Research for their support of this work under Grant No. N00014-17-1-3016

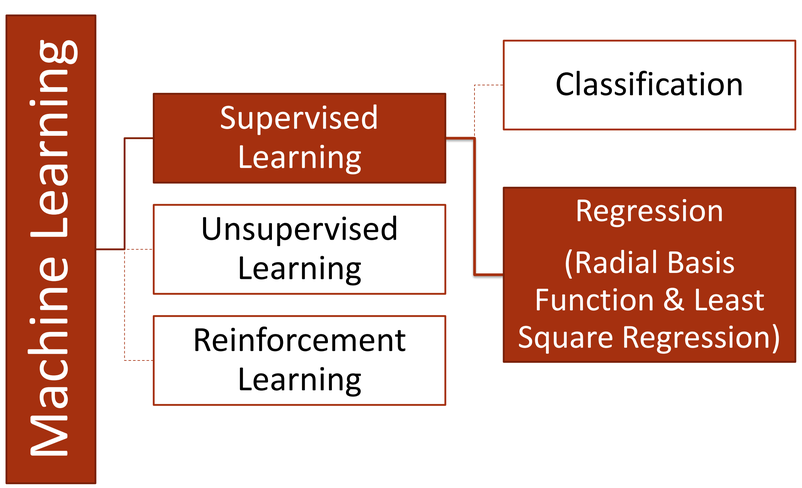
Problem Statement: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Generic Solution Space: UWB antenna array optimization using conventional full-wave electromagnetic (EM) solvers can be replaced by machine learning (ML) models with appropriate and sufficient training.

State-of-the-Art (SOTA): Conventional full-wave EM solvers such as method of moments (MoM), multi-level fast multipole method (MLFMM), finite element method (FEM), and finite difference time domain (FDTD) method are currently being used to study, analyze and assess the performance of UWB antennas. UWB antenna optimization using conventional EM solvers utilizes significant computational time and memory resource.

Specific Solution Space: Use regression models such as radial basis function, and least square regression to train on UWB antenna metrics. The trained models will help with output prediction followed by optimization for reduced physical aperture area.

Objective: Implement, improvise and/or apply existing ML models on UWB antenna geometries and report comparisons for various antenna metrics predicted by traditional EM solver and trained ML models.



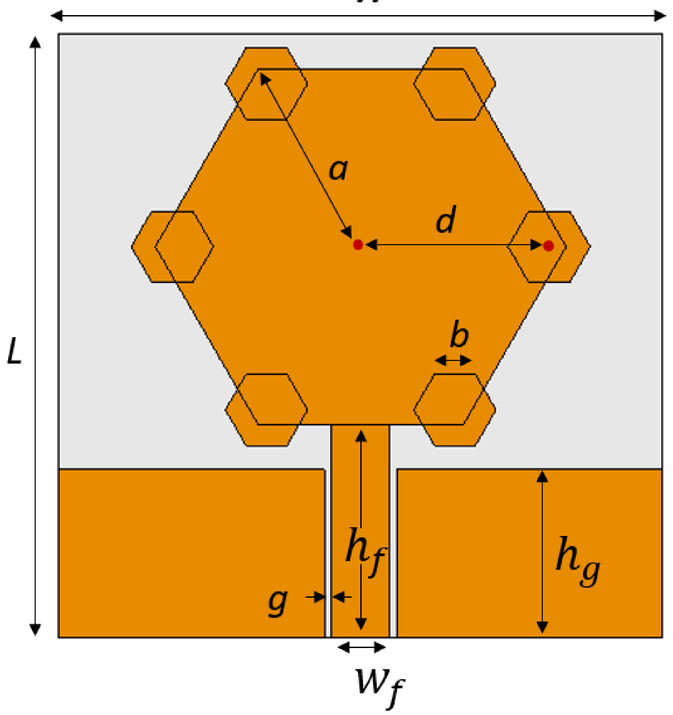


Fig 1: Fractal antenna geometry for ML study.

Setup
- Design fractal antenna geometry using Altair FEKO and re metrics.
- Import antenna design from Altair FEKO into Altair Hyper
- Select adjustable parameters ('a' and 'b') and assign the de antenna parameters.

Training
- Generate 10 different pairs of input ('a' and 'b') and corres response/gain) for 30 different discrete frequency points ov
- Train Radial Basis Function (RBF) and Least Squared Reg independently using training data.

Testing & Validation
- Using unseen test data, test each algorithm independently,
- Compare recorded output response against the FEKO respo
- Finally, calculate root mean square error (RMSE) to unders of each algorithm.

Results

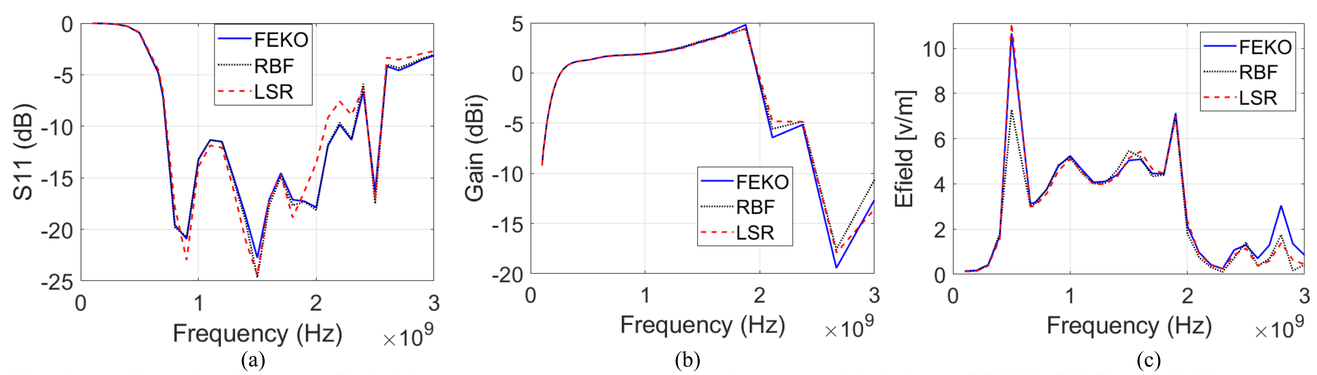


Fig 2: (a) S11, (b) Gain, (c) E-field comparison of an antenna design yielded from FEKO, RBF, and LSR.

Table 1: RMSE Comparison

Antenna response	RMSE values	
	RBF	LSR
S11	0.0430	0.0108
Gain	0.4517	0.5325
E-field	0.3972	0.7249

Table 2: Computational time and memory consumption

Approach	FEKO	ML (RBF, LSR)
Time	18 mins	<5 secs
Memory	33 MB	<4 KB

Key Points:

1. Trained RBF and LSR models accurately predicted S11 (reflection coefficient), gain and electric field outputs 160 times faster than the traditional EM solver (FEKO).
2. Fig 2 also shows that the RBF model is in better agreement with FEKO response than LSR.
3. The training data extracted from the antenna design output is non-linear. RBF performs better in such scenarios.

In this work, two
trained, tested, and
available software
output response fro
been validated us
algorithms have
however RBF was
capabilities as well

Application of thes
to antenna array
procedure.

This work was su
Research under Gr

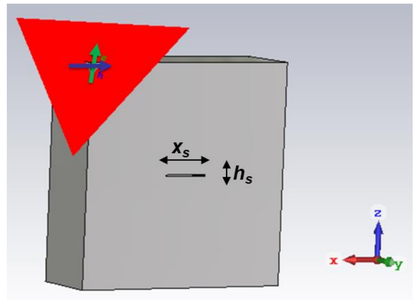
[1] E. Alpaydin, Int
press, 2020.
[2] H. Fallahi and Z.
CPW-Fed Monopole
IEEE Antennas and
pp. 1484-1487, 2013.

- The external field excitation of any perforated metallic enclosures creates internal standing waves that can create large fields at the resonance frequencies of the cavity, i.e., the field inside the cavity can be higher than that outside it.
- OSPRES Relevance: : Provide general guidelines on how the environment, in this case, the enclosure, affects RF coupling and subsequent electromagnetic absorption to UAV wires and integrated circuits.

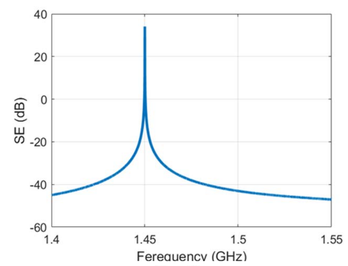
Simple cavities with slot

- In this study, the electric field at the center of the cavity was compared to the incident field and the Shielding Effectiveness (SE) is calculated:

$$SE\ (dB) = 20\ \log_{10}\frac{E_{in}}{E0}$$



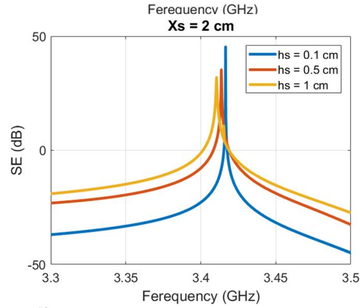
- SE > 0 dB Indicate cavity amplifying incident field.
- Cavity size (15cm X 5cm X 15cm), Slot size (X_s= 3cm, h_s= 0.1cm)



Slot characteristic effect

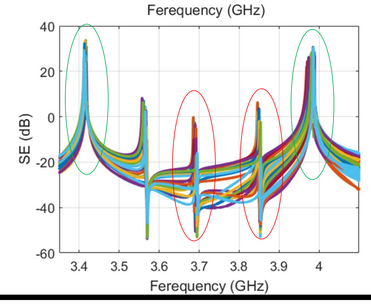
❑ ***Slot Size***

- As the slot size decreases the time it takes for the field inside the cavity to escape increases. Thus, bandwidth of the electric fields decreases with a higher field magnitude.



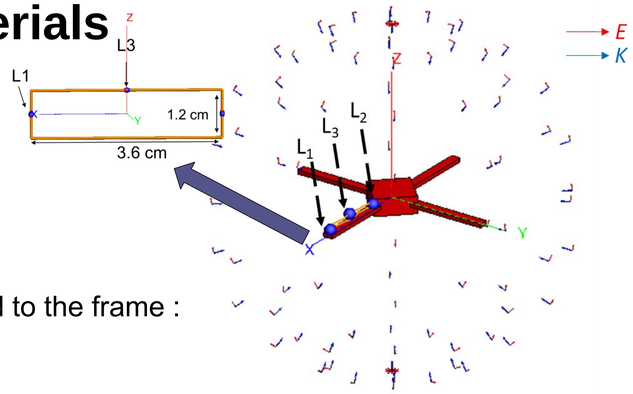
❑ ***Slot Location***

- The effect of the slot position is not significant on the field inside the cavity at 3.4GHz, 4 GHz but sensitive at other resonance frequencies.



Wires Placed on Top of Quadcopter Frames of Different Materials

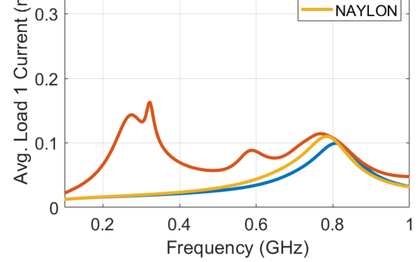
- Wire radius = 0.3 mm, 100 angles, Loop height above frame = 1 mm, L1 = L2 = L3 = 50 Ω, 515 mm X 515 mm frame size

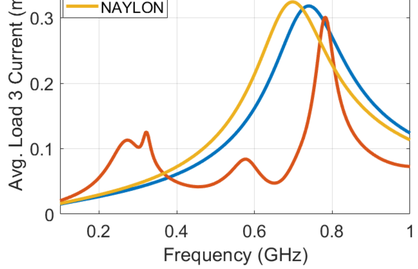


Two materials were assigned to the frame :

1. **PEC**
2. **Naylon 66** ($\varepsilon_r = 3.3$, lossless)

DISTRIBUTION STATEMENT A. This work is funded in part by ONR Award No. N00014-17-1-3016 and ONR Award No. N00014-18-C-1017



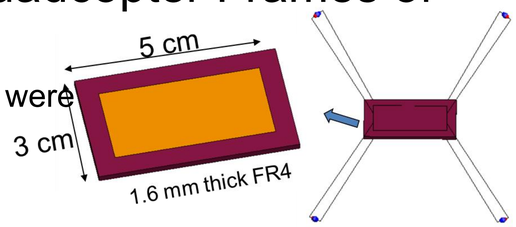


- The metallic frame introduced extra peaks in the induced current at the wire loop's loads at low frequencies.
- These high peaks are due to the geometry and size of the frame
- Dielectric frames red-shift and cause a slight increase in the average coupled current

Wire Placed Inside Quadcopter Frames of Different Materials :

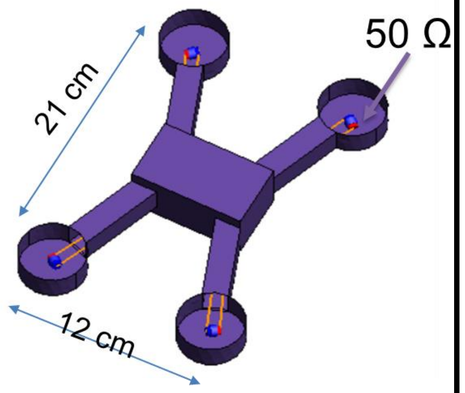
Three materials for the frame were considered:

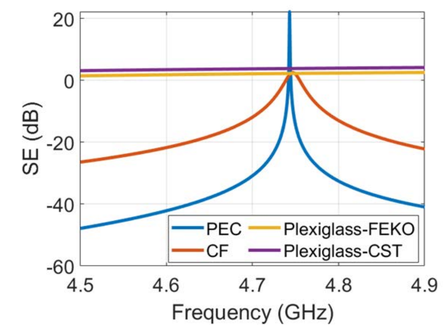
1. **PEC**
2. **Carbon Fiber Composite:** Polymer ε_r =3, Fibers σ = 1000 S/m
3. **Plexi-glass** ($\varepsilon_r = 2.6$, $\tan\delta = 0.0057$, thickness = 5 mm.



❑ ***Empty Frame (No-Wires)***

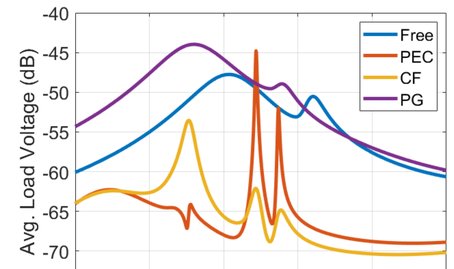
- Lossy dielectric UAV enclosures, Plexiglass, enhance coupling to enclosed wires and electronics by ~ 5 dB, over a wide range of incident field directions compared to free space;
- Perforated PEC and Carbon fiber UAVs shield by more than 20 dB on average except at the resonance frequencies where they amplify the coupling by ~ 5-20 dB over a narrow bandwidth.



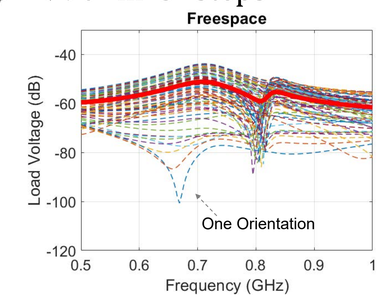


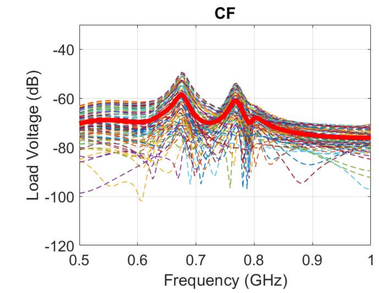
❑ ***Frame with Wires and PCB System shown above***

- At the resonance frequencies, shielding can be compromised (e.g., CF frame 0.66 GHz)
- For PEC frames, fields are amplified in comparison to free space at 0.75 GHz and 0.77 GHz
- Dielectric frames amplify the voltage by > 5dB and shift resonances to lower frequencies



- Angles of incidence were varie
  $\varphi < 90°$ in $5°$ steps





- CF does not have the sha resonances of PEC but yiel comparable shielding
- Given the variations in the couple voltage with orientation, we ca calculate the probability of t voltage exceeding a certa threshold

❑ ***probability of the voltag exceeding -50 dB***

- Three different values of the PC dielectric substrate loss tangent a studied to quantify the effect losses on SE.
- Higher losses lower the intern fields and decrease the probabil of load voltage exceeding t threshold.
- These results were achieved usi incident plane waves at continuo frequencies ,however, it can pred the optimum pulse, to maximize t coupled voltage, by designing t pulse's center frequency a bandwidth to overlap with t frequencies where the probability the figures on the right is highest.

Conclusions:

We studied t coupling to the enclosed wires and electro frames provide a better Shielding Effectiven the large resonances. On the other hand, di shift the resonances of the enclosed wires to

[1]Computer Science Electrical Engineering Department, UMKC [2]Missouri Institute for Defense & Energy, U

Objective and Motivation:

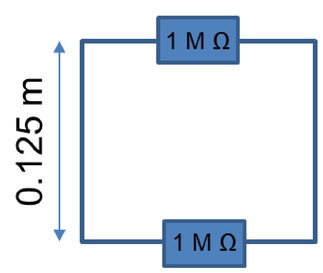
- Predict RF coupling to a complex system of wires with nonlinear loads and develop RF guidelines
- Predict the optimum incident waveform properties to maximize the coupled voltage/currents to a nonlinear load of interest
- OSPRES Relevance: Provide explanation to experimental results, Predict RF coupling results to guide experimental measurements, provide guidance to minimum properties of HPM sources to generate the desired effects
- To achieve the previous goals, we propose to combine the Characteristic-Mode Analysis (CMA) with the Equivalent Circuit Approach (ECA):

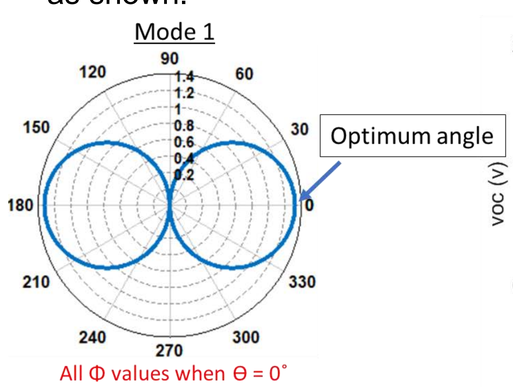
Characteristic-Mode Analysis (CMA)

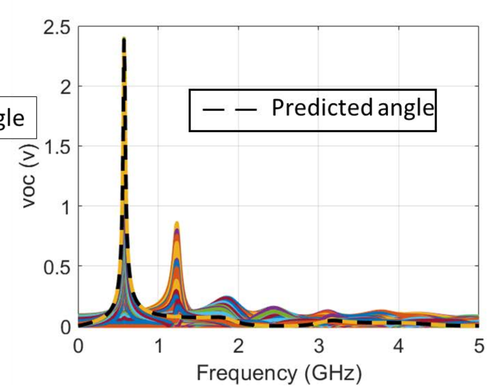
- CMA is a full-wave electromagnetic technique that decomposes the total surface current coupled to a DUT into a set of fundamental modes.
- It also provides the radiation pattern of each Mode
- CMA can provide the optimum field direction by studying radiation pattern of the wire's first mode. Then by reciprocity we estimate the optimum angle to excite this mode.

Representative Example:

- A 10.5 cm by 10.5 cm square loop with a 1 MΩ resistor in both sides is studied
- The radiation pattern of Mode 1 is calculated
- By reciprocity, the optimum excitation angle is estimated.
- The predicted optimum angle is validated as shown.



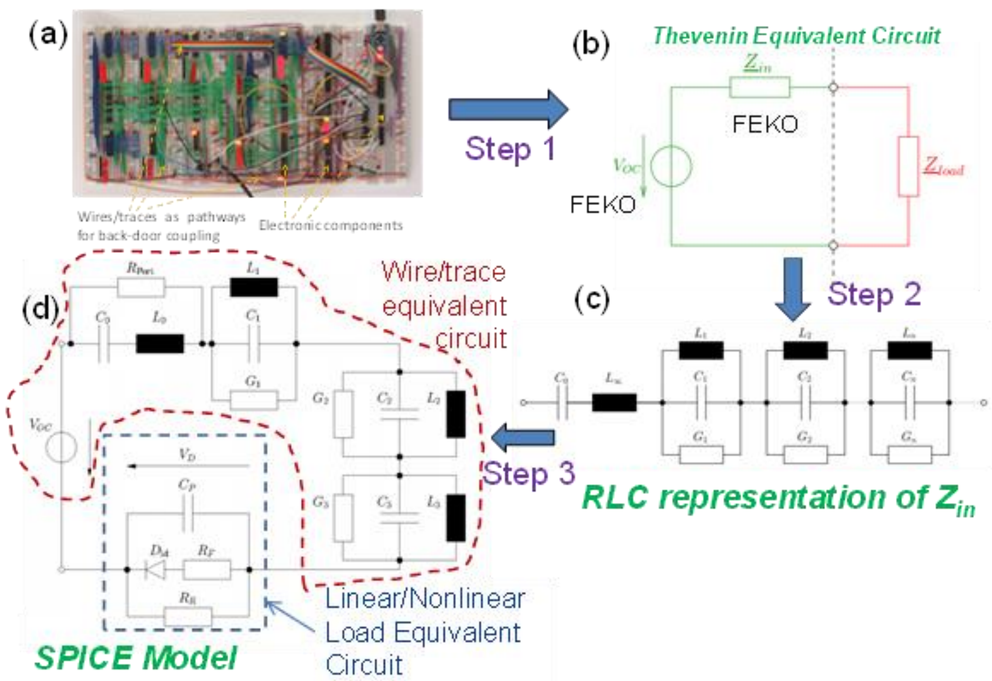




DISTRIBUTION STATEMENT A. Approved for public release: distribution unlimited.
This work is funded in part by ONR Award No. N00014-17-1-3016 and ONR Award No. N00014-18-C-1017

Equivalent Circuit Approach (ECA):

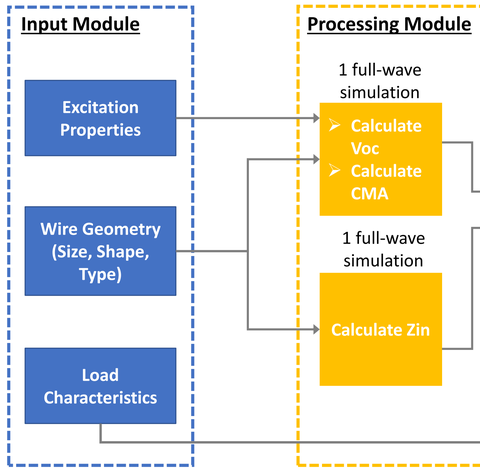
- The Equivalent Circuit Approach (ECA) has been commonly used for quantifying coupling to receiving antennas and wire systems.
- The ECA is based on developing a Thevenin equivalent circuit for the wiring system that involves 3 main components:
  1) Open-circuit voltage, V_{oc}.
  2) Input impedance, Z_{in}, of the wiring/trace system.
  3) Load impedance, Z_L, of the load of interest which can be linear or nonlinear based on the electronic component of interest [1].
- Full-wave electromagnetic solvers are used to calculate (1) & (2).
- A SPICE solver can be used to simulate the entire wire system at a fraction of the computational time with no loss in accuracy.
- The ECA provides physical insight into RF coupling problems



PECNEC

- PECNEC is a hybrid framework that calls a library of computational codes to combine the Equivalent Circuit Approach (ECA) with the Characteristic Mode Analysis (CM) to determine RF induced overvoltage conditions on linear/non-linear circuit elements using SPICE solvers
- ECA is at least 100x faster than full-wave simulations since simulations can be done completely in SPICE with no loss in accuracy when varying the loads or excitation characteristics.
- CM allows us to predict optimum incident angles (θ, ϕ) and polarization (η)

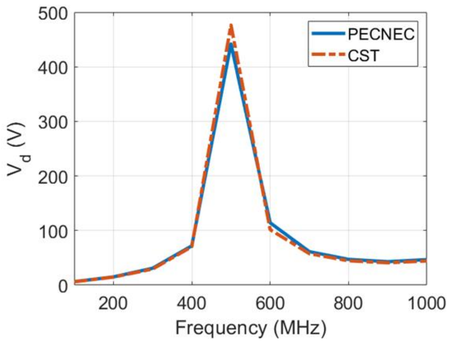
PECNEC Component



- PECNEC is currently limited to two wires and two loads
- Wires can be of any arbitrary shapes and user can define the wires' shapes pixel-by-pixel

PECNEC Validation

- Diode parameters: Cj = 0.2 p 200 Ω, Rr = 125 kΩ.
- Loop excited by 10 gaussian all same amplitude 250 bandwidth 38 MHz, ex direction but different frequencies and we compared maximum coupled voltage V_d



Conclusions:

We develope Characteristic Mode Analysis and the Ec coupling to a complex system of wires wi PECNEC is much faster than full-wave PECNEC will be expanded for more comple

References:
R. Michels *et al.*, "Modeling and Verification of a Parasitic N Electromagnetic Excitation," *IEEE Trans. Electromagn. Com*