ONR Short Pulse Research, Evaluation, and non-SWaP Demonstration for C-sUAV Study (OSPRES)

Grant No. N00014-17-1-3016

2021 Annual Report

Period of performance: October 1 2020 – September 30 2021

Distribution Statement A. Approved for public release: distribution unlimited

PI:
Anthony Caruso
Missouri Institute for Defense and Energy
University of Missouri-Kansas City
816-235-2505
carusoan@umkc.edu

REPORT DOCUMENTATION PAGE

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED	
		START DATE	END DATE
31-01-2023	Annual Report	01-10-2020	30-09-2021

4. TITLE AND SUBTITLE

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study (OSPRES) Grant: Annual Report 2021

5a. CONTRACT NUMBER	5b. GRANT NUMBER	5c. PROGRAM ELEMENT NUMBER
	N00014-17-1-3016	

5d. PROJECT NUMBER	5e. TASK NUMBER	5f. WORK UNIT NUMBER

6. AUTHOR(S)

Allen, R.; Azad W.; Barman, B.; Berg, J.; Bhamidipati, J.; Bhattarai, G.; Brasel, S.; Chatterjee, D.; Durbhakula, K.; Eifler, J.; Gardner, N.; Hamdalla, M.; Hassan, A.; Indharapu, S.; Khan, F.; Shepard, S.; Sobhansarbandi, S.; Thompson, H.; Usenko, A.; Caruso, A.; Paquette, M.

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

University of Missouri-Kansas City
5110 Rockhilll Rd
Kansas City, MO 64110

8. PERFORMING ORGANIZATION REPORT NUMBER

OSPRES_Grant_Annual_Report_2021

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)	11. SPONSOR/MONITOR'S REPORT NUMBER(S)
Office of Naval Research One Liberty Center, 875 N Randolph Arlington, VA 22203	ONR	

12. DISTRIBUTION/AVAILABILITY STATEMENT

Distribution Statement A. Approved for public release: distribution unlimited.

13. SUPPLEMENTARY NOTES

14. ABSTRACT

The technical objective of the ONR Short Pulse Research, Evaluation, and non-SWaP Demonstration for C-sUAS Study (OSPRES) Grant program is to execute high-risk, high-payoff efforts that address elementary gaps to achieving a modular, scalable & electronically steerable high power microwave (HPM) based defense system for the counter UAS mission, with focus on the short-pulse high-average-power space, as well as the responsivity of the target to RF stimuli, while educating the next generation of pulsed power and defense-minded scientists, engineers, and innovators.

15. SUBJECT TERMS

high power microwaves, photoconductive semiconductor switches, fiber laser, drift-step-recovery diodes, pulse forming networks, antennas, RF coupling, thermal management, diode-based nonlinear transmission lines; high voltage switch

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES
a. REPORT	b. ABSTRACT	C. THIS PAGE		
U	U	U	UU	930

19a. NAME OF RESPONSIBLE PERSON	19b. PHONE NUMBER *(Include area code)*
Anthony Caruso	816-235-2505

PREVIOUS EDITION IS OBSOLETE.

STANDARD FORM 298 (REV. 5/2020)
Prescribed by ANSI Std. Z39.18

1 OVERVIEW

OSPRES Grant Goal: Address and transition technologies and capabilities that enable the OSPRES Grant Objective using the OSPRES Grant Approach, while educating the next generation of pulsed power and defense minded, stewards and innovators.

OSPRES Grant Objective: To execute high-risk, high-payoff efforts that mitigate, fill or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable and electronically steerable high-power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average-power space and includes the kill chain considerations including the target and its responsivity to radiofrequency stimuli.

OSPRES Metrics of Success: Developed technologies and capabilities that are published in the peer review, protected as intellectual property, and/or, transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use, as enabling/integrable capability(ies).

OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

OSPRES Grant Security: All efforts should be fundamental and publicly releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

Contents of this Report: This report compiles monthly status reports (MSRs) from October 2020 through September 2021.

ONR HPM Program - Monthly Status Report (MSR) – OCT 2020

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

11/15/2020

Distribution Statement ~A: Distribution authorized to all OSPRES Grant and Contract performers, and any OSPRES uncompensated collaborators. Further dissemination per the Office of Naval Research, Ryan Hoffman (ryan.hoffman@navy.mil, 703-696-3873) or higher DoD Authority.

OSPRES Grant Goal: address and transition technologies and capabilities that enable the OSPRES Grant Objective using the OSPRES Grant Approach, while educating the next generation of pulsed power and defense minded, stewards and innovators.

OSPRES Grant Objective: to execute high-risk, high-payoff efforts that mitigate, fill or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable and electronically steerable high power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average power space, and includes the kill chain considerations including the target and its responsivity to radiofrequency stimuli.

OSPRES Metrics of Success: developed technologies and capabilities that are published in the peer review, protected as intellectual property, and/or, transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use, as enabling/integratable capability(ies).

OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

OSPRES Grant Security: All efforts should be fundamental and publically releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

1.0 Contents

2.0 Executive Summary 3
2.1 Progress, Significant Findings and Impact 3
2.2 Completed, Ongoing and Cancelled Sub-Efforts 4
2.3 Running Total of Academic and IP Program Output 4
3.0 Switch Evaluation and Innovation 5
3.1 Si-PCSS Modeling and Optimization 5
3.2 Lasers and Optics 6
3.3 Si-, SiC- and GaN Modeling and Evaluation 8
3.4 GaN:C Modeling and Optimization 10
3.5 Diode-based NLTLs 12
4.0 Prime Power and Conditioning 15
4.1 HV Switch Pulsed Chargers 15
5.0 Trade Space Analysis of ESAs 18
5.1 Tradespace Analysis of an Array of ESAs. 18
6.0 RF Coupling 22
6.1. Enclosure Effects on RF Coupling 22
7.0 Thermal Management 25
7.1 Jet Impingement Optimization 25
8.0 Program Management 27
8.1 Issues 27
8.2 Interactions with Others 27
8.3 Major Procurement Actions 27
8.4 Travel 27
8.5 Pending or Upcoming Public Release Requests 27
9.0 Appendix A – Academic and IP Output 28
9.1 Conference Publications 28
9.2 Journal Publications 30
9.3 External Presentations/Briefings 31
9.4 IP Disclosures Filed 32
9.5 Provisional Patents Filed 32
9.6 Non-Provisional Patents Filed 32
10.0 Appendix B – Wrap-up Sub-Effort Documentation 33
10.1 *Ab Initio* Informed TCAD and GaN:C Sub-Effort Wrap-up 33

2.0 Executive Summary

2.1 Progress, Significant Findings and Impact

A new format for the OSPRES Grant MSRs was executed in OCT2020 (this report), which includes additional contextualization and relevance to the program objectives. Feedback on the new template usefulness and deficiencies is welcome.

The SiPCSS Modelling Subgroup (Eifler/Utt) found by TCAD simulation that up to a 30% reduction in laser energy/pulse can be realized with optimal contact spacing based enhancement for full thickness (1300-μm) PCSS devices. For high average power lasers, SWaP-C^2 scales almost linearly, which over an array composed of 256 elements could mean ones-of-millions in cost savings and 0.32-m^3 reduction in volume compared with commercially available high average-power 1064-nm laser systems.

The Fiber Laser Design Subgroup (Shepard) generated a concept to overcome fiber laser damage at the threshold for Ytterbium-doped fibers through a hybrid design which stages mode diameters. Once demonstrated, this work would not only have direct application for reducing the SWaP and especially cost of the 1064-nm laser requirement for the Si-PCSS system, but also have dual-use impact for HEL and cutting laser systems.

The Array Antennae Subgroup (Chatterjee/Barman) found by simulation that arranging individual patch elements into a square rather than hexagonal lattice, reduces the effective aperture area and number of elements from 4.4-m^2 to 3.1-m^2 and from 225- to 114-elements with ~λ/2 inter-element spacing with a smaller relative loss in gain (from 27- to 24-dBi). If the results hold for the physical aperture size, in which a finite ground plane converges and is demonstrable, this result would be a major step in realizing an acceptable area ship-deck antenna for use at the upper end of the UHF.

The *ab initio* informed TCAD effort has come to a close this month; full documentation and the impactful findings are captured in Appendix B.

2.2 Completed, Ongoing and Cancelled Sub-Efforts

	Start	End
2.2.1 On-going Sub-Efforts		
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-based Non-Linear Transmission Lines	FEB 2018	Present
Heat Transfer by Jet Impingement	MAY 2018	Present
X-PCSS Comparison (X=Si, SiC, GaN)	NOV 2018	Present
HV Switch Pulsed Chargers	DEC 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
UWB Element Tradespace for Arrays	MAY 2020	Present
2.2.2 Completed Sub-Efforts		
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
2.2.3 Cancelled Sub-Efforts		
Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019

2.3 Running Total of Academic and IP Program Output

See Appendix A for authors, titles and inventors (note: this list is still being updated)

2.3.1 Conference Publications	24
2.3.2 Journal Publications	1
2.3.3 External Presentations/Briefings	18
2.3.4 IP Disclosures Filed	8
2.3.5 Provisional Patents Filed	1
2.3.6 Non-Provisional Patents Filed	0

3.0 Switch Evaluation and Innovation

3.1 Si-PCSS Modeling and Optimization

3.1.1 Problem Statement, Approach and Context

Primary Problem: High-average-power 1064-nm picosecond class lasers are too large (1100-cm^3/W) and monetarily expensive ($1000/uJ*pulse) for the Navy afloat missions;

Solution Space: improve laser power density, or better laser interaction and downstream processes with the photoconductive switch;

Sub-Problem: poor on-state resistance per laser energy during photoconduction process;

State-of-the-art (SOTA): PCSS contact patterns spaced at tens-of-microns for switches and photoconductors optimized for other geometries/objectives;

Deficiency in the SOTA: non-optimized contact patterns and poor On-State Resistance per Laser Energy;

Solution Proposed: optimize contact pattern specific to the OSPRES Si-PCSS dimensions, mechanical shape, electric field shape, doping profile and ARC for a percent laser energy reduction of at least 10%;

Relevance to OSPRES Grant Objective: enhanced SWaP-C^2 for the laser system needed to drive the PCSS or reduced laser requirements, which subsequently meets the modular and scalable volume and cost aim-points.

Risks, Payoffs and Challenges: top contact not most direct impact on CCE, major laser effectiveness and/or smaller laser needed, models do not represent reality and need additional physics. Metallization for optimized top contacts is inexpensive and easy to manufacture.

3.1.2 Tasks / Timeline / Milestones

(A) Develop doping dependent free carrier absorption (DDFA) model for photogeneration in TCAD/ 3-weeks or 21 AUG / TCAD DDPA model significant ~10% required laser energy increase;

(B) Run parameter space study for 1300 μm thick Si-PCSS with DDFA / 12 NOV/ ~30% laser energy reduction;

(C) Fabricate top contacts and test on-state resistance vs incident laser energy/ 15 DEC to fabricate / Top contacts metallized;

(D) TCAD determination of Si-PCSS variability in optimized top contacts dependent on p-doping. More accurate determination of optimal spacing in laser windowing of top contacts and switch geometry dependence for general applicability of optimal top contact.

3.1.3 Progress Made Since Last Report

(A) Parameter space study completed for thicker 1300 µm Si-PCSS device models using DDFA photogeneration model.

(B) Parameter study within the measurement error of experimental on-state resistance vs laser energy for Si-PCSS. As for earlier parameter study of 500 µm thick devices, laser energy was shown to be reduced as much as 29%.(C) Top contacts metallized await bottom metallization, anti-reflective coating, beveling and passivation for delivery to UMKC.(D) Not yet completed.

3.1.4 Significant finding(s) and Mission Impact

TCAD parameter studies have shown a ~30% maximum possible laser energy reduction can be achieved by using the optimal spacing (of the Si-PCSS top contact laser windowing). For example, using the 350 µm optimal spacing only 62 uJ of laser energy is required for 0.3 Ω on-state resistance as compared to 82 uJ with 20 µm spacing or 20 uJ less laser energy (see left Figure 3.1.1). The pump power cost is known to be the main factor in laser costs and reduced laser energy requirement via Si-PCSS top contact optimal spacing greatly impacts pump power cost. Reduced required laser energy also gives flexibility to design more compact and/or less costly switch supporting laser systems.

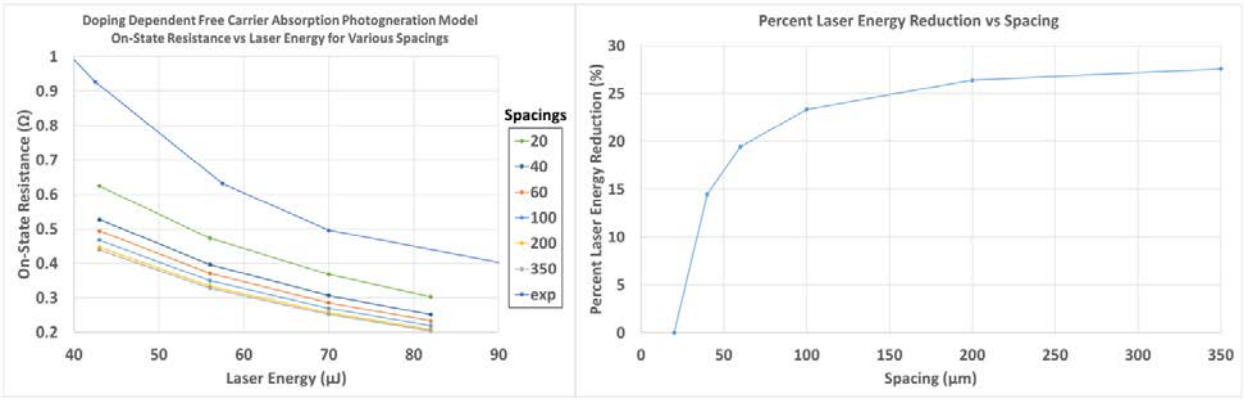


Figure 3.1.1. (Left) At top experimental 20 µm spacing and TCAD spacings within on-state resistance measurement error (Right) TCAD shows ~30% maximum laser energy reduction possible with ~350 µm spacing.

3.2 Lasers and Optics

3.2.1 Problem Statement, Approach and Context

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100-cm^3/W) and too monetarily expensive (over $1000/uJ per pulse) for PCSS embodiments of HPM based defense systems.

Solution Space: Optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight and small-volume solution.

Sub-Problem: Amplified spontaneous emission (ASE) and fiber nonlinearities impede optical amplifier performance, while optical pump power system costs often dominate.

State-of-the-art (SOTA): Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting and other applications.

Deficiency in the SOTA: Optical pump power system costs are prohibitive until reduced by a factor of two.

Solution Proposed: A pre-burst optical pumping scheme can reduce costs by a factor of at least ten.

Relevance to OSPRES Grant Objective: Enhanced SWaP-C^2 for the laser system needed to drive the PCSS which subsequently meets the modular and scalable volume and cost aim-points.

Risks, Payoffs and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE, pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability.

3.2.2 Tasks / Timeline / Milestones

(A) Reduce costs by a factor of two or more / April-May 2021 / Simulations showed that we can drop the pump power costs by a factor of 40 with tolerable pre-burst ASE, hence a UMKC invention disclosure was filed on 02JUN2020.

(B) Reduce the ASE / On-going / A linear gain theory predicts the in-burst ASE would be over our spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by a factor of over 7000, hence a UMKC invention disclosure was filed on 14SEP2020.

(C) Mitigate deleterious nonlinear impacts / On-going / Progressed towards practical devices that exploit gain saturation, while mitigating the deleterious nonlinearities, via staged designs of different mode diameters.

(D) Manage timing jitter / On-going / Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020. The impact of group velocity dispersion assessed as minimal but modal dispersion predicted a pulse width spreading to 175 ps for our 100 ps existing systems. Spreading on the order of this prediction was experimentally observed. Calculations showed that we can limit this to negligible levels via the simple use of a collimating lens.

3.2.3 Progress Made Since Last Report

(A) None.

(B) Further optimization led to a gain saturation induced ASE suppression factor of 9,525 (for the G = 8 10^6 cascaded optical amplifier example).

(C) Demonstrated how (in the example above) each gain stage can suppress ASE without exceeding damage thresholds. Configured COMSOL Wave Optics to model self-focusing in Gaussian beams of intensities utilized in the above example. Performed an initial study.

(D) None.

3.2.4 Significant finding(s) and Mission Impact

We have shown that gain saturation effects can reduce the ASE power levels to far below those predicted by the linear gain theory by adjusting the design parameters so that the critical point power is closer to the operating power of the amplifier. One technique is to lower the gain per length, which results in longer fiber amplifiers. Another technique is to lower the mode diameter, but this can also enhance the damage and other deleterious nonlinear optical effects in the fiber. We utilize a staged design in which the preamp uses a smaller mode diameter (to enhance the gain saturation at lower powers) than the mode diameter of the next stage, etc. In this way we are able to produce sufficient saturation of the gain, while not exceeding the damage threshold, within each stage of higher power.

Modeling the effects of self-focusing we find (for Gaussian beams in silica glass) little beam distortion until we surpass intensities of 6 GW/cm^2 in a minimal beam waist (radius) of 200 microns. For comparison: that intensity is close to the 6.37 GW/cm^2 (peak) damage threshold which we approach at the output of one of our 80 W (average) power amplifiers in a 400 micron fiber core diameter. The mission impact is a positive one – it indicates that, even for a final power amplifier stage, optical fiber amplifiers show promise as a feasible technology.

3.3 Si-, SiC- and GaN Modeling and Evaluation

3.3.1 Problem Statement, Approach and Context

Primary Problem: The screening methods for HPM source driver subsystem are complex due to the wide-range availability of novel materials, switching technologies, topologies and external trigger mechanisms with interdependent properties, leading to problems with down-selection, modeling, and optimization.

Solution Space: Evaluate semi-insulating solids and switching technologies based on theoretical operational limits and trigger requirements, respectively, and explore novel fabrication techniques and/or circuit and switch topologies to push beyond established limitations in terms of peak and average power, repetition rates, and cooling needs. Improve SWaP-C^2 index of the trigger subsystem through compact, cost-effective alternatives.

Sub-Problem: (A) µs-order pulse recovery times observed experimentally for Si-, SiC- and GaN-PCSS in capacitive and microstrip transmission line topologies, limiting the pulse repetition rates (PRR) and the average power subsequently; ***(B)*** expensive and bulky picosecond laser with auxiliary systems required for optical actuation of PCSS.

State-of-the-art (SOTA): (A) High PRR switch carrier lifetime tailored through e-beam irradiation, enabling 2-3x faster recovery (~0.3-0.4 µs); ***(B)*** high average power

picosecond pulsed lasers available up to 50 W output power with a gain factor up to 40 dB (~10,000x power) with laser amplifier.

Deficiency in the SOTA: (A) Increased leakage current in devices (~100 μA at 5kV bias in Si-PCSS) due to uniformly distributed crystal defect profile across the devices despite 250°C anneal; ***(B)*** High average power 1064-nm pulsed lasers for Si are bulky, require auxiliary systems, and additional optics for SHG/THG generation for wide bandgap device triggering.

Solution Proposed: (A) selective lattice damaging in regions with high carrier density through proton irradiation to overcome high leakage currents; ***(B)*** Multi-stage cascaded optical amplifier powered by laser diodes (arrays) and GaN-PCSS as a compact, inexpensive laser replacement capable of ~175°C operation.

Relevance to OSPRES Grant Objective: Determines application-specific SWaP-C^2 optimized solution for source-driver and laser subsystems as a combination of switch material and pulse forming network. Evaluates and potentially enhances the theoretical limitations of source driver subsystem as a combination of switch material and pulse forming network.

Risks, Payoffs and Challenges: (A) proton irradiation simulations show two orders of magnitude lower leakage current (~7.5 μA at 5kV bias in Si-PCSS) with approximately same pulse recovery time as observed in electron irradiation, but potentially result in damage to superficial atomic layers from repeated proton irradiation, leading to premature surface breakdown; ***(B)*** issues with interconnect engineering and thermal management issues at high temperature operation, and unavailability of COTS high power pulsed laser diodes could potentially raise a need for research in laser diodes (arrays).

3.3.2 Tasks / Timeline / Milestones

(A) (i) Evaluate the doping profiles, contact layering, and patterning for SiC-PCSS and explore suitable fabrication techniques to achieve desired optimal doping profile using TCAD-Athena/ Dec 2020-Jan 2021

(ii) Complete parametric study of SiC-PCSS including rise- and recovery-time optimization simulations for varied vanadium and nitrogen concentrations, and high voltage transient response study for varied geometry, optical trigger, contact design, and illumination area / Jan-Feb 2021

(iii) Model carbon compensated GaN-PCSS with vertical and lateral geometries to simulate transient response, including rise- and fall-time, voltage hold-off, and peak- and average powers for performance evaluation against Si- and SiC-PCSS models / Mar-Apr 2021

(B) Complete feasibility study for the cascaded multi-stage optical amplifier design with commercial off-the-shelf optical sources (LDs/LDAs), and model GaN-PCSS with non-complex circuit topology to match the trigger requirement for the light sources. Also, determine if extending the state-of-the-art pulsed optical sources to be further explored to meet the device optical requirements / Nov-Dec 2020

3.3.3 Progress Made Since Last Report

(A) SiC-PCSS models have been refined for lateral (900 x 360-μm), and vertical (1000 x 200-μm) geometry to include acceptor- and donor-type lattice defects caused by vanadium compensation and nitrogen impurities. Optical absorption and carrier generation have been studied for the refined SiC-PCSS device models with 265, 355, 385 and 532 nm wavelengths along with DC and transient performance are being studied to compare peak and average power with the Si-PCSS. 385 nm and 532 nm wavelengths exhibited 2x higher quantum efficiency.

(B) A cascaded optical amplifier of two or more stages has been proposed as a potential replacement for conventional laser subsystem (laser, SHG/THG optics, drivers and cooling) implementing electrically pumped miniature pulsed optical sources (laser diodes and laser diode arrays) with ~MHz order repetition rates, driven by semi-insulating GaN-PCSS. Positive current gain of 10^x is expected at each stage by implementing direct WBG material in lock-on mode to limit the number of optical amplifier stages.

3.3.4 Significant finding(s) and Mission Impact

The cascaded optical amplifier is an inexpensive alternative to conventional laser system, with a potential to miniaturize the pulser sub-system by one-to-two orders of magnitude, enhancing SWaP-C^2 factor of the HPM system. Direct bandgap semiconductors are known to exhibit lock-on mode of operation, enabling photo-gain and potentially limiting the cascaded stages to a minimum, optimizing SWaP parameters.

3.4 GaN:C Modeling and Optimization

3.4.1 Problem Statement, Approach and Context

Primary Problem: Need for a more compact, cost-effective RF pulse generation system for Navy afloat missions on smaller vessels and vehicles.

Solution Space: Improve efficiency and reduce necessary material, size, and thermal requirements by utilizing gallium nitride (GaN) in PCSSs through exploitation of its theoretical material properties which allow for higher operating voltages, center frequencies, and operational temperatures, while also eliminating the need for pulse-shaping transmission lines through direct RF modulation using the laser/photon source driving the PCSS.

Sub-Problem: Lack of maturity in compensated gallium nitride semiconductors (i.e., GaN:X for X=C,Fe) PCSS manufacturing, development, and optimization.

State-of-the-art (SOTA): Si-based PCSS with >10-kV operational voltage, cooling system capacity of 500 W/cm^2, and theoretical breakdown of 1.3-MW/cm.

Deficiency in the SOTA: Si-based technologies requiring ~100 μJ per 4 MW of output power, increasing the size of laser necessary for device triggering; long recovery time (ones-of-μs), limiting quick opening and high PRR operation along with increased heating in the PCSS; critical electric field of 0.3 MV/cm, leading to devices that are ones of cm^2

in area for the target peak power; and operating temperature of <160°C, leading to increased cooling requirements.

Solution Proposed: Direct modulation of optically activated GaN:C PCSS—eliminating the need for a bulky pulse-forming transmission line—capable of handling >3 MW (peak power) with ~20 μJ of incident optical energy, device area <1 cm^2, and operating temperature ~500°C (theoretical temperature—will be limited by circuit components and solder).

Relevance to OSPRES Grant Objective: Reduction in size and cost for cooling system, removal of a pulse-shaping system, and material cost, leading to enhanced SWaP-C^2 capability with greater modularity and scalability.

Risks, Payoffs and Challenges: Due to manufacturing limitations, GaN PCSS devices tend to be limited to lateral (both contacts on the top side of the device) geometries, limiting operating voltage due to current crowding and surface flashover. The recovery time (ones-to-tens-of-ns) may lead to device heating and increased DC content when generating RF with a period on the same order as the recovery time.

3.4.2 Tasks / Timeline / Milestones

Dec 2020 Show GaN:C PCSS high-voltage operation (ones-of-kV to start) using the pulse charger obtained from the HV switch development team.

i. Setup and validate the pulse charger works with GaN:C PCSS

ii. Test using Sylgard 184 covering the GaN:C device to prevent flashover and compare with previous results with this encapsulant.

iii. Repeat HV pulse testing with GaN:C PCSS with SF6 gas, to prevent flashover and attempt reaching higher operating voltages. A small chamber will be designed and fabricated using material offering minimal losses of laser energy.

iv. Seek further solutions to achieve ~10kV depending on success with Sylgard 184 and SF6, including studying the feasibility of vertical GaN:C devices that would eliminate surface flashover seen in lateral devices.

Jan 2021 Demonstrate RF unipolar modulation in the GHz regime with current PCB setup and the automated optical delay system.

March 2021 Demonstrate RF bipolar modulation using two GaN:C devices, along with a positive and negative power source, based on the PSOG based circuit and setup with the automated optical delay system.

May 2021 Complete study of recovery for differing gap lengths, incident energies, and operating voltages and find solutions to reduce the recovery time.

3.4.3 Progress Made Since Last Report

(A) Setup and validated the compatibility of the pulse charger, received from the HV switch development team, with GaN:C PCSS. Testing will begin in November to achieve high-voltage on-state resistance, efficiency, and recovery results.

(B) Automated optical delay system designed, fabricated, and setup for RF modulation testing beginning in November, allowing for repeatability and refined control of the delay time between pulses.

(C) Bipolar pulse modulation and analysis will begin after demonstrating unipolar modulation and once a negative power supply is sourced.

(D) Began recovery analysis by organizing and analyzing previous GaN:C data to understand how recovery changes with voltage, gap length, and incident energy, along with determine additional measurements necessary to accurately measure the full recovery time of GaN:C PCSS. Data collected based on carbon concentration was inaccurate due to the contacts of the newer NRL devices not allowing for full activation of the devices.

3.4.4 Significant finding(s) and Mission Impact

By utilizing a wide, direct bandgap material as a PCSS RF source, reductions in pulse-forming transmission lines, cooling requirements, and material necessary for each PCSS device, leads to a greater HPM SWaP-C^2 factor. Previous measurements showed an increase in recovery time with increasing carbon concentration, but it could not be determined if this was caused solely by the carbon concentration or by undocumented defects caused by changes in the growth process. Most of this month's progress was in the design, fabrication, and setup of equipment necessary for HV testing and direct RF modulation with GaN:C, which will begin in November

3.5 Diode-based NLTLs

3.5.1 Problem Statement, Approach and Context

Primary Problem: Develop a pulse forming network for a modular HPM system capable of center frequency generation in excess of 1GHz and peak power generation in excess of 1 MW;

Solution Space: Develop a lumped element diode based nonlinear transmission line (D-NLTL) to convert pulse energy to the UHF band at MW peak power.

Sub-Problem: Increase D-NLTL center frequency through the selection of COTS components.

State-of-the-art (SOTA): D-NLTLs have shown to generate center frequencies of 2-500 MHz at kV amplitudes in a light weight small footprint circuit.

Deficiency in the SOTA: Diodes present limitations in generating center frequencies beyond 500 MHz peak power beyond 1 MW, and efficiency of energy conversion due to diode junction capacitances ranging from several 100 pF to single nF, reverse bias hold off potentials of single kV, and a nonlinear signal dependent reactance.

Solution Proposed: Characterize and optimize diode parameters affecting the upper limits of frequency generation and identify limits/desired ranges required for UHF generation. Such parameters include, but are not limited to; diode frequency response,

diode reverse bias hold off voltage, diode small signal capacitance, diode chip parasitic, and diode relaxation time.

Relevance to OSPRES Grant Objective: The SWaP-C^2 capabilities of D-NLTLs lend the technology towards a modular, scalable, low cost system.

Risks, Payoffs and Challenges: Utilizing D-NLTLs to convert energy to the UHF band represents a truly mobile RF and Microwave source (shown in Figure 3.5.1) only physically constrained by the volume and cost restrictions of the pulse source. However current COTS components have limited the technology to sub UHF frequencies and sub kV pulse amplitudes.

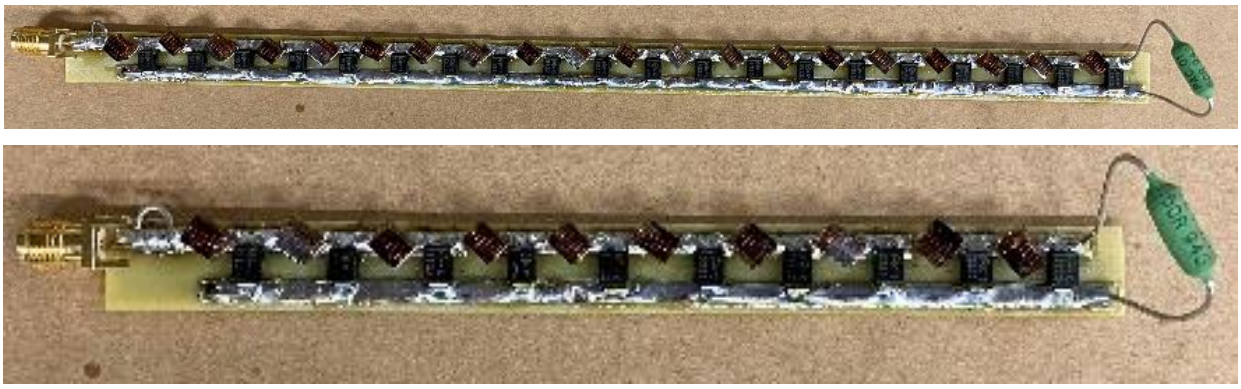


Figure 3.5.1: 10 and 20 Cell lumped element D-NLTLs. (Top) 20 cell D-NLTL of dimensions 1.1 x 23.45 cm. (Bottom) 10 D-NLTL of dimensions 1.1 x 12.45 cm.

3.5.2 Tasks / Timeline / Milestones

(A) Construct a D-NLTL prototype capable of 10^1 – 10^2 MHz frequency generation at signal amplitudes of ~10V and compare with simulation to determine the effect of the dynamic reactance and sources of loss on generated amplitude and frequency. (JUL20 - SEP20)

(B) Identify Diodes capable of UHF generation at LV in simulation. Candidates are identified as having a low signal capacitance of 100-200 pF and a decrease of 1 order of magnitude over a 10V operation range. (OCT20 – NOV20)

(C) Constructed and compare a D-NLTL prototype to simulation using the UHF candidates a with a goal of achieving center frequency generation of 200-500 MHz at amplitudes of ~10V. (NOV20-DEC20)

(D) Fabricate and characterize a D-NLTL prototype capable of voltage biasing the diodes for the purposes of frequency tuning and the use of bipolar excitations. Initial biasing goals include alteration of the center frequency of 20-30% and success in breaking a bipolar pulse into a sequence of solitons. (DEC20-JAN21)

3.5.3 Progress Made Since Last Report

(A) Compete

(B) 2 potential UHF diode candidates were identified based on the characteristics given in 3.4.2 (B), SMV1702 & SL02, and simulated with measured frequency estimations of 526 MHz and 283 MHz under lossless conditions respectively.

(C) Fabricate and characterize prototypes using UHF diode candidates (Current).

(D) Simulation of a LV topology capable of center frequency tuning and driving via a bipolar excitation.

3.5.4 Significant finding(s) and Mission Impact

During initial LV prototype characterization two barriers to efficient UHF generation, as required by the ONR mission, were identified:

(1) impedance mismatch at the source load interface due to the dynamic nature of the reactance of a diode in reverse bias significantly limits successful injection of energy into the network and therefore diode saturation.

(2) The generated solitons must be narrow enough to allow for sufficient separation as the signal propagates in the network.

The source-line impedance mismatch requires large excitation amplitudes – often in excess of the reverse bias hold off potential of the diodes – to achieve adequate diode saturation for soliton generation, limiting the frequency generation and efficiency of the network. At the low line inductances required for GHz frequency generation solitons propagate at large phase velocities limiting their ability to separate prior to reaching the load. Lack of soliton separation negatively impacts the network's ability to shift energy to the high frequency regime. Future work is aimed identifying and characterizing diode parameters that affect the high frequency performance of diodes and using those parameters to select COTS components capable of mitigating and overcoming the above listed barriers.

4.0 Prime Power and Conditioning

4.1 HV Switch Pulsed Chargers

4.1.1 Problem Statement, Approach and Context

Primary Problem: Commercially available High-voltage solid-state switches made by BEHLKE are the best SWaP-cooling, greatest monetary cost, have long lead-time, and are made outside of US a trusted foundry/source. For the Navy afloat mission to be successful, we need a sustainable supply of US manufactured switches at a much lower cost.

Solution Space: Design and demonstrate modular high-voltage (~10-kV) and fast (PRF = 100-kHz) solid-state switches using a combination of series and parallel-connected commercially available inexpensive discrete MOSFETs and custom high-voltage (~10-kV) isolated gate drivers.

Sub-Problem: Voltage balancing among the series connected MOSFETs, minimization of gate signal delays, high-voltage isolation required for the power supplies and the PWM signal as well as differential voltage feedback measurement across individual MOSFETs.

State-of-the-art (SOTA): Direct liquid-cooled solid-state switch from BEHLKE (e.g., HTS-151-30).

Deficiency in the SOTA:

1. BEHLKE made switches are expensive. For instance, a single unit of HTS-151-30 switch costs around $5,000.
2. BEHLKE switches along with direct liquid cooling units occupy a considerable amount of space. For instance, HTS-151-30 switch from BEHLKE has a footprint of approximately 225 mm*85 mm*75 mm without considering liquid cooling system. Some key parameter of this switch are as follows.

   i) Maximum operating voltage = 15kV

   ii) Maximum continuous load current = 2.52 A (without cooling), 30 A (with liquid cooling)
   iii) Maximum turn-ON peak current = 300A (pulse width = 200 µs, duty cycle <1%)

   iv) Turn-ON resistance =1.3 Ω
3. Once switching frequency is greater than 10 kHz, liquid cooling system is required to operate the BEHLKE switch
4. Without liquid cooling, the maximum continuous power dissipation (P_{cont}) of the BEHLKE switche is limited (e.g., for HTS-151-30, P_{cont} is 10 W without liquid cooling).
5. At higher switching frequency (> 20 kHz). the BEHLKE switch requires multiple ancillary DC power supplies, i.e. 5 V, 15 V, and 60 V.
6. Switches made by BEHLKE cannot be reconfigured to withstand a higher voltage exceeding their recommended rating. BEHLKE offers separate products to operate

them at higher voltage/currents. ***Solution Proposed:*** Designing a modular high-voltage (~10kV) switch using a single custom isolated gate driver for each module and having a construction cost lower than the BEHLKE sold switch with equivalent or better performance in all specification categories (Specification of the BEHLKE sold switches can be found in the following link: http://www.behlke.com/separations/separation_c4.htm).

Relevance to OSPRES Grant Objective: The proposed modular high-voltage switch is expected to facilitate controlled hundreds-of-nanosecond charging of an array of transmission lines of pulse forming networks to drive an array of PCSS, thereby producing controlled hundreds-of-picosecond scale high-voltage pulses.

Risks, Payoffs and Challenges:

I. Lack of rigid control over voltage balancing can lead to a cascaded failure among the series-connected MOSFETs.

II. In the absence of an adequate mitigation scheme, voltage overshoot due to the fast switching speed can exceed the voltage rating of an individual MOSFET, thereby damaging the switch.

III. At high voltage (~10-kV) and high repetition rate (>100-kHz), mitigating EMI to safeguard the individual MOSFETs from false turn-ON is a major challenge.

4.1.2 Tasks / Timeline / Milestones

(A) Design an in-house single gate driver based four-stage switch/ 9 weeks or 29 AUG/ four-stage in-house switch successfully tested up to a DC voltage of 2.5-kV and switching frequency up to 50-kHz.

(B) Design a custom high-voltage (~10-kV) isolated gate driver to drive the high-voltage switch/ 10 weeks or 7 NOV/ in-house high-voltage isolated gate driver designed, fabricated and tested successfully.

(C) Design an SMD MOSFET based four-stage switch and control it using the in-house gate driver/ 5 weeks or 12 DEC/ test the voltage withstanding ability of the switch with a DC supply voltage up to 5-kV and evaluate the effectiveness of the thermal management at its current state.

(D) Design a modular HV switch using the concept of the tested four-stage high-voltage switch and driver with the in-house gate driver/ 8 weeks or 23 JAN/ test the voltage withstanding ability of the switch with a DC supply voltage up to 10-kV and evaluate the effectiveness of the thermal management at its current state. (E) Transfer new capability/knowledge to contract effort and document in peer reviewed conference papers and journals. Transition to commercial entity for production/manufacture via ONR ManTech, SBA or equivalent.

4.1.3 Progress Made Since Last Report

(A) An alternate version of the high-voltage (~10-kV) isolated gate driver has been designed, fabricated and tested. As opposed to the H-bridge driver based preliminary

gate driver, this gate driver is capable of isolating the logic side and power side of the gate driver IC.

(B) Separate DC-DC converters have been selected to minimize loading, which can arise from the charging of the gate-source capacitance during the turn-ON period of the MOSFET.

(C) Testing showed that the gate driver successfully produced a level-shifted PWM signal while maintaining fidelity of the original PWM signal.

(D) The HV isolated gate driver is compact, occupying a footprint of 4.4”*4.2”. The design of the SMD based four-stage switch is in progress and it will have a similar footprint to that of the gate driver to facilitate board-board connection, thereby minimizing gate loop parasitics.

4.1.4 Significant finding(s) and Mission Impact

I. Commercial gate drivers are not suitable for applications where switching occurs at 5.7 kV or more. Therefore, the designed in-house HV gate driver can drive in-house multilevel MOSFET structure to switch at 10 kV level

II. Three isolated (10 kV rated) DC-DC converters from RECOM have been used to generate three voltage rails (+20V, +5V, -5V) required to drive the selected gate driver IC (ISO5852S).This isolation protects the input logic side of the gate driver IC from high voltage at the output side of the gate driver. This UMKC developed driver requires only one 24 V ancillary power supply.

III. An optical fiber link was constructed from a transceiver and a receiver made by Broadcom for HV isolation of the PWM signal.

IV. The output from the optical link resembles the input PWM signal, thereby establishing the fidelity of the PWM signal from source up to gate driver input.

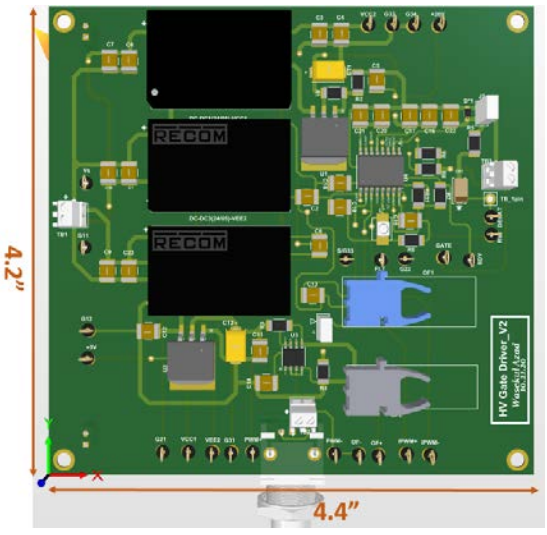


Figure 4.1.1: In-house HV isolated gate driver

5.0 Trade Space Analysis of ESAs

5.1 Tradespace Analysis of an Array of ESAs.

5.1.1 Problem Statement, Approach and Context

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth and electronic beam steerability over the UHF range (0.4 – 1 GHz), compared with present art - high power microwave capable antenna arrays;

Solution Space: An array of patch antenna elements whose feed, two dimensional shape and relative placement (i.e., intra- and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art;

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of Surface Waves (SW). Note, scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays;

State-of-the-art (SOTA): Building arrays of microstrip ESAs and comparing the performance with established reduced surface wave (RSW) microstrip patch antenna arrays;

Solution Proposed: A method to choose substrate parameters (permittivity ε_r, thickness d) that minimizes SW excitations, at any specified frequency range, must be developed, and followed by designing and optimizing antennas using the D/Q (D - Directivity and Q – Quality Factor) ratio;

Relevance to OSPRES Grant Objective: (a) Excitation of SWs cause scan blindness, which limits beam uniformity while being steered – a major objective of OSPRES Grant. (b) Tradespace analysis of ESAs can be performed by optimizing antennas (and arrays) in terms of directivity (or gain) and impedance bandwidth simultaneously, via D/Q technique;

5.1.2 Tasks / Timeline / Milestones

(A) Build a minimum viable validation prototype / 4-weeks / To test a 3×3 microstrip ESA array for basic array metrics (Boresight Gain vs. frequency, Radiation Pattern and VSWR) and electronic beam steering;

(B) Investigation into microstrip patch antenna designs on Ceramic and Polyethylene based substrates (with high power handling capabilities), to achieve better performance for HPM transmissions at UHF range / 8-weeks / >30% impedance bandwidth obtained from microstrip patch antenna modeled on Ceramic at UHF range.

(C) Investigate the effect of array aperture area reduction on different array parameters / 8- weeks / around 50% reduction in the total number of array elements showed just about 3 dB reduction in the array boresight gain;

5.1.3 Progress Made Since Last Report

(A) Investigations into ESA microstrip patch antenna (and array) designs on various substrates suitable for HPM applications:

a. Ceramic ($\varepsilon_r = 9.6$ and $\tan\delta = 0.7 \times 10^{-4}$):

i. Coaxial probe-fed rectangular microstrip patch antenna modeled on a circular shaped (radius $= 5"$) PEC-backed substrate - 38.15% 2:1 VSWR bandwidth (548.3 – 806.8 MHz) with a maximum gain of 5.62 dBi.

ii. Modeled and characterized a 3×3 array on a $6" \times 6"$ square shaped PEC-backed substrate, by integrating the single element mentioned in (i), as a step towards building a minimum viable validation prototype - 12 dBi of average boresight gain obtained over 500 – 800 MHz.

b. Polyethylene ($\varepsilon_r = 2.25$ and $\tan\delta = 0.00025$): Coaxial probe-fed U-slot microstrip patch antenna element modeled on infinite PEC-backed Polyethylene substrate - 26.76% 2:1 VSWR bandwidth (680.1 – 890.5 MHz) with a maximum gain of 6.67 dBi.

(B) Identified a method to choose substrate parameters, which can reduce SW excitations, for microstrip patch antenna designs – a 15×15 array modeled on Ceramic based substrate, using this new technique, did not show scan blindness, as the main beam is electronically steered from 0 to $\pm 60°$, at different frequencies between 548.3 to 806.8 MHz.

(C) Investigations into reduced array aperture area have been initiated – preliminary results on the impact of aperture area shrinkage on array boresight gain, radiation pattern and electronic beam steering obtained.

5.1.4 Significant finding(s) and Mission Impact

Investigations into Reduction of Radiating Aperture Area of the Array: Characterization of a 15×15 array of microstrip patch antennas (on square lattice), modeled on a 26.67 mm thick TMM-10i substrate ($\varepsilon_r = 9.8,\ \tan\delta = 0.002$) at UHF range (0.6 – 1 GHz) had been reported earlier. Around 70% of the array radiating aperture area is reduced by transforming from square to hexagonal lattice, as shown in Figure 5.1.1. Full-wave simulations of all the 3 models have been performed via FEKO on infinite PEC-backed substrates to reduce computation time, and the geometries have been summarized in Table 5.1.1.

Conclusion: Simulated data for the array geometries (on infinite ground plane) shows, $\approx 30\%$ radiating aperture area reduction of the array (i.e., 49.3% reduction in the total number of array elements from 225 to 114) results in ≈ 3 dB decrease in the overall array gain across the entire frequency range (0.6 to 1 GHz).

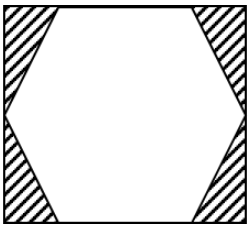


Figure 5.1.1. Transformation from Square to Hexagonal Lattice (Elements in the shaded area removed).

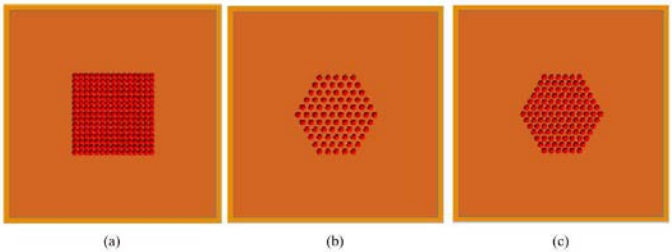


Figure 5.1.2. Array geometry on infinite ground plane for: (a) Array – 1 (b) Array - 2 and (c) Array – 3.

Table 5.1.1: Summary of the Array Geometries (λ calculated at 990.6 MHz.)

Array #	Lattice Type	Radiating Aperture Area (m^2)	Inter-element spacing (d)	Total No. of Elements
1	Square	4.44	0.485λ	225
2	Hexagonal	3.10	0.6λ	80
3	Hexagonal	3.10	0.5λ	114

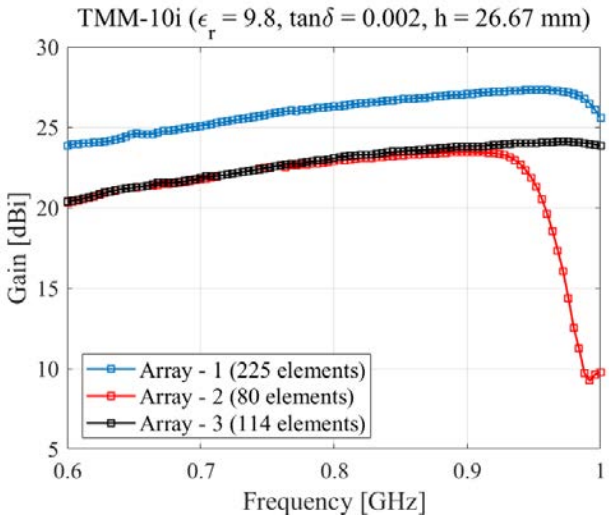


Figure 5.1.3. Gain vs. Frequency for all the three array geometries simulated on infinite ground plane.

6.0 RF Coupling

6.1. Enclosure Effects on RF Coupling

6.1.1. Problem Statement, Approach, and Context

Primary Problem: Slots and gaps are introduced in casings/enclosures due to a variety of practical reasons which might compromise their shielding, creating upset susceptibility to the enclosed electronics. The goal of this work is to quantify how the thresholds for upset susceptibility of enclosed wires and integrated circuits differ from those in free space.

Solution Space: study enclosures with different shapes, material compositions, and slots to quantify their effect on RF coupling to the enclosed wires and electronics typically used in UAVs. The study will focus on the low-frequency range where the incident wavelength is comparable to the size of the enclosure or larger.

Sub-Problem: UAVs are manufactured with a wide variety of shapes and composites to accomplish an exponentially expanding list of missions. The configurations previously reported in the literature have simplistic assumptions regarding the shape and material composition of UAV enclosures that might overestimate or underestimate susceptibility.

State-of-the-art (SOTA): Simple statistical analysis of specific enclosure configurations using either brute force simulations/measurements or pure statistical methods.

Deficiency in the SOTA: Brute force simulations/measurements of the voltages and currents induced in wires and integrated circuits contained in enclosures is computationally or experimentally complex and have several limitations. The computations are complicated by the multiscale nature of the simulations and the experiments are complicated by the cost of the equipment and the extensive time needed to measure every variation to cover all possible scenarios. Statistical methods, such as the Random Coupling Model (RCM) for example [1], are only accurate for high frequencies where the wavelength is much smaller than the size of the enclosure. Another main deficiency of RCM is that it can't predict the exact induced voltages and currents for a specific well-characterized system but it only provides the statistical properties of these induced currents and voltages.

Solution Proposed: Apply Characteristic Mode Analysis (CMA) to identify the fundamental modes of the enclosure, current distribution, and the field pattern of each mode. This will allow us to predict the worst-case RF coupling scenarios without the need of lengthy simulations and/or expensive experimental measurements. The proposed approach can predict measurements at te fraction of the cost/time.

Relevance to OSPRES Grant Objective: provide general guidelines on how the environment, in this case the enclosure, affects RF coupling and subsequent electromagnetic absorption to UAV wires and integrated circuits.

Risks, Payoffs, and Challenges: The modes depend mainly on the shape and material of the enclosure. Since UAVs have a wide variety of shapes and material compositions, a library of several UAVs needs to be studied before quantitative general conclusions can

be drawn. Challenges can be mitigated by the use of the classification techniques of Machine Learning (ML). That is, different ML techniques will be evoked to detect hidden patterns on how the shape, material composition, and the shape/size location of slots correlate with the field enhancement inside the enclosure.

6.1.2. Tasks / Timeline / Milestones

Task	Timeline	Milestone
A. Complete the CMA implementation for studying the shielding effectiveness of metallic enclosures. Validate CMA can predict the worst-case shielding effectiveness of metallic enclosures as a function of their shapes.	2 months 11/15/2020-1/15/2021	A fast full-wave tool that facilitates studying the effect of a metallic enclosure on shielding effectiveness (1 IEEE AWPL Paper)
B. Use CMA tool in (A) to predict the worst case internal field magnitude of metallic and dielectric enclosures of ten COTS UAVs as a function of HPM waveform	4 months 1/15/2021-5/15/2021	A database of worst-case internal fields shielding effectiveness results of the ten COTS UAVs as a function of their shape and HPM waveforms.
C. Use the database in (B) to train a Machine Learning (ML) platform to predict RF coupling to enclosed wires and electronics	5 months 5/15/2021-10/15/2021	Perform blind tests to estimate the induced internal fields of 2 COTS UAVs, not used in the training of the ML platform, and compare them with the measurement.

6.1.3. Progress Made Since Last Report

(A) A simple UAV circuitry model was developed and studied for different enclosures.

(B) Documentation draft started as a manuscript to IEEE AWPL.

6.1.4. Significant Finding(s) and Mission Impact

(A) Lossy dielectric UAV enclosures such as Plexiglass with dielectric permittivity of $\varepsilon_r = 2.6$ and a loss tangent $\tan\delta = 0.0057$ enhances the coupling to the enclosed wires and electronics in by 5 dB on average, over a wide range of incident field directions, comparison to free space;

(B) Perforated Perfect Electric Conducting (PEC) and Carbon fiber UAVs shield the enclosed wires and electronics at most frequencies by more than 20 dB on average

except at the resonance frequencies of the enclosure where the enclosure will act like a cavity that amplifies the coupling by ~ 5-10 dB over a narrow bandwidth.

(C) The susceptibility of most wires and electronics to electromagnetic interference is typically measured/assessed in free space. The analysis above shows that UAV enclosures where these wires/electronics are enclosed can improve/mitigate this susceptibility.

References:

[1] Bisrat Addissie, John Rodgers, Thomas Antonsen, "Extraction of the coupling impedance in overmoded cavities," Wave Motion, Volume 87, Pages 123-131, 2019.

7.0 Thermal Management

7.1 Jet Impingement Optimization

7.1.1 Problem Statement, Approach and Context

Primary Problem: Traditional, laminar-flow-based cooling technologies are limited in their ability to compensate average-power dissipation >1-kW (i.e., >1-GW/m^3 as cooling density) – specifically, the thermal load byproduct – of HPM-based sources within electronically-steered arrays;

Solution Space: utilize novel cooling technologies which employ non-laminar flow regimes (i.e., jet impingement thermal management system, JI-TMS);

Sub-Problem: an order-of-magnitude greater fluid flowrate and two orders greater pressure drop is required over traditional techniques (10-gpm vs. 1-gpm, and 100's-psi vs. 1's-psi) without increasing SWaP-cost;

State-of-the-art (SOTA): high-power electronics employing JI-TMS's have achieved 10's-of-kW of average power handling capabilities using 20℃ dielectric coolant and sub-mm jet diameters while consuming equivalent power to deliver the fluid to the JI-TMS;

Deficiency in the SOTA: chiller/pump systems consumption of power to produce thermal compensation, extreme pressures (100's-of-psi) to achieve optimal flowrate performance and cooling metrics, low SWaP-C[2] fidelity for Navy afloat missions;

Solution Proposed: develop a JI-TMS able to compensate average-power dissipation >1-kW while maintaining the HPM-source's solid-state heat source < 80℃, by flowing dielectric fluid at turbulence-inducing flow rates while not exceeding 100's-of-psi within the system;

Relevance to OSPRES Grant Objective: increased cooling performance facilitates HPM sources' higher average-power operation (>1-kW) deeming specific-power-densities (>1 W/cm^2) at distances >2-km achievable;

Risks, Payoffs and Challenges: high pressures and larger chiller-pump systems, minimizing pressure drop requirements while maintain or improving performance increases cooling form-factor (> 1-GW/m^3), 5× that of traditional cooling techniques.

7.1.2 Tasks / Timeline / Milestones

(A) Initial design of JI-TMS-V1 proposed and simulated using Si-PCSS source's laminar-flow TMS as baseline / 1-year, 4-mo. or MAY18'-OCT19' / initial design-simulation phase completed;

(B) Revised JI-TMS-V1's design (JI-TMS-V2), simulation of parametric study performed, prototype developed and experimentally evaluated / 2-months or DEC19' / establishing design's baseline accomplished;

(C) Design changes applied to JI-TMS-V2 to decrease flowrate and pressure drop requirement / 9-months or SEP20' / design optimization phase completed;

(D) Complete redesign (JI-TMS-V3) of system to increase average-power handling capabilities (>-1kW) by increasing flowrate and convective heat transfer (>40-kW/m·K) without increasing system's volume (~100-cm^3) / 4-months or DEC20' / design phase-II complete.

7.1.3 Progress Made Since Last Report

(A) ANSYS CFD simulations show that, when applying 200-W of average power and flowing 11.75-gpm of silicon oil, the Si-PCSS average temperature is 50℃ and results in a pressure drop of 239-psi;

(B) Flowing silicon oil at 11.75-gpm was numerically verified to induce turbulent flow within the JI-TMS manifold yet achieves a 270% reduction of the pressure drop when compared to the previous design iteration;

7.1.4 Significant finding(s) and Mission Impact

The JI-TMS design's ability to compensate 0.2-kW (i.e., >200-MW/m^3) average power and maintain the Si-PCSS source's average temperature at 50℃ is 10℃ less than the laminar-flow based design of equivalent volumetric form-factor (cross-flow thermal management system) – currently used for the OSPRES Contract's source array demonstrator.

8.0 Program Management

8.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

8.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

8.3 Major Procurement Actions

i. Microsoft Office 365 GCC High (75 seats) - $45,000 (for OSPRES Contract CUI Compliance)

8.4 Travel

Destination	Purpose	Attendees	Estimated Costs

8.5 Pending or Upcoming Public Release Requests

i. N/A

9.0 Appendix A – Academic and IP Output

(Please note that this section is still being updated).

9.1 Conference Publications

Chatterjee

[1] B. Barman, J. Kovarik, D. Chatterjee and A. N. Caruso, “Some Investigations into Mutual Coupling Analysis for Trade Space Studies of Linear Arrays,” accepted for publication in the Proceedings of the *IEEE International Phased Array Systems and Technology Symposium*, Boston, Mass., October 2019.

[2] K. C. Durbhakula, J. Lancaster, A. M. Hassan, D. Chatterjee, A. N. Caruso, J. Hunter, Y. Liu, D. Beetner and V. Khilkevich, “Electromagnetic Coupling Analysis of Printed Circuit Board Traces using Characteristic Mode Analysis,” accepted for publication in the Proceedings of the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, July 7-12, 2019, Atlanta, Georgia, USA.

[3] K. C. Durbhakula, D. Chatterjee and A. M. Hassan, “On the Location of Transverse Electric Surface Wave Poles for Electrically Thick Substrates,” accepted for publication in the Proceedings of the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, July 7-12, 2019, Atlanta, Georgia, USA.

[4] D. Chatterjee, B. Barman. J. Kovarik, and A. N. Caruso, “Studies on Antenna Characterization and Propagation of High Power Pulsed Electromagnetic Waves with Minimal Spatial Dispersion,” presented at the *Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium*, Destin, Florida, USA, April 2019.

[5] J. Kovarik, B. Barman, D. Chatterjee and A. N. Caruso, “Some Investigations into Applications of Electrically Small Antennas as Phased Array Elements,” presented at the *Directed Energy Professional Society* (DEPS) *Annual Science and Technology Symposium*, Destin, Florida, USA, April 2019.

[6] K. C. Durbhakula, D. Chatterjee and A. M. Hassan, “Location of Surface Wave Poles in Sommerfeld Integrals: A Mittag-Leffler Expansion Approach,” accepted for publication in the *Proceedings of the URSI-B International Symposium on Electromagnetic Theory*, URSI Commission, San Diego, USA, May 2019.

[7] B. Barman, D. Chatterjee and A. N. Caruso, “Analytical Models for L-Probe fed Microstrip Antennas,” accepted for publication in the Proceedings of the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, July 7-12, 2019, Atlanta, Georgia, USA. (1 page URSI Abstract).

[8] K. C. Durbhakula, D. Chatterjee and A. M. Hassan, “Analytical Evaluation of Sommerfeld Integral Tails Present in Two-layered Media Green’s Functions,” published in the *Proceedings of the Indian Conference on Antennas and Propagation* (InCAP), Hyderabad, India, December 2018.

[9] K. C. Durbhakula, D. Chatterjee, A. M. Hassan and M. S. Kluskens, “Studies on Numerical Evaluation of Sommerfeld Integrals for Multilayer Topologies,” published in the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, July 7-12, 2018, Boston, Mass., USA.

[10] J. Lancaster, D. Chatterjee and A. N. Caruso, “Some Investigations into the Dispersion Characteristics of Localized Bessel Beams,” published in the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, July 7-12, 2018, Boston, Mass., USA. (1 page URSI Abstract).

Hassan

[1] J. Hunter, S. Xia, A. Harmon, A. M. Hassan, V. Khilkevich, D. Beetner, “Modeling and Statistical Characterization of Electromagnetic Coupling to Electronic Devices,” URSI National Radio Science Meeting, Boulder, CO, January 4-9, 2021.

[2] K. Alsultan, P. Rao, A. N. Caruso, A. M. Hassan, “Scalable Characteristic Mode Analysis: Requirements and Challenges (White Paper),” *Large Scale Networking (LSN) Workshop on Huge Data: A Computing, Networking and Distributed Systems Perspective Sponsored by NSF*, Chicago, IL, 2020.

[3] M. Hamdalla, B. Bissen, A. N. Caruso, and A. M. Hassan, “Experimental Validations of Characteristic Mode Analysis Predictions Using GTEM Measurements,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Montréal, Québec, Canada, July 5-10, 2020*.

[4] M. Hamdalla, A. N. Caruso, and A. M. Hassan, “Predicting Electromagnetic Interference to a Terminated Wire Using Characteristic Mode Analysis,” *Proceedings of the Annual Review of Progress in Applied Computational Electromagnetics (ACES)*, Monterey, CA, March 22-26, 2020.

[5] M. Hamdalla, A. N. Caruso, A. M. Hassan, "Characteristic Mode Analysis of the Effect of the UAV Frame Material on Coupling and Interference," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, 7-12 July 2019.

[6] M. Hamdalla, J. Hunter, Y. Liu, V. Khilkevich, D. Beetner, A. Caruso, A. M. Hassan, "Electromagnetic Interference of Unmanned Aerial Vehicles: A Characteristic Mode Analysis Approach," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, 7-12 July 2019.

[7] K. Durbhakula, J. Lancaster, J. Hunter, Y. Liu, D. Beetner, V. Khilkevich, D. Chatterjee, A. Caruso, A. M. Hassan, "Electromagnetic Coupling Analysis of Printed Circuit Board Traces using Characteristic Mode Analysis," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, 7-12 July 2019.

[8] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, “Scalable characteristic mode analysis using big data techniques,” *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[9] M. Z. M. Hamdalla, W. Al-Shaikhli, J. Lancaster, J. D. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, “Characteristic Mode Analysis of Electromagnetic Coupling to Wires with Realistic Shapes,” *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[10] C. Hartshorn, K. Durbhakula, D. Welty, D. Chatterjee, J. Lancaster, A. M. Hassan, A. N. Caruso, “Crosstalk and Coupling to Printed Circuit Board Metallic Traces with Arbitrary Shapes,” *Proceedings of the AMEREM 2018 Conference*, Aug 27-31, Santa Barbra, CA, 2018.

[11] M. Hamdalla, J. Roacho-Valles, J. Hunter, D. Beetner, A. M. Hassan, A. N. Caruso, “Electromagnetic Analysis of Unmanned Aerial Vehicles Using Characteristic Mode Analysis,” *Proceedings of the AMEREM 2018 Conference*, Aug 27-31, Santa Barbra, CA, 2018.

[12] C. Hartshorn, M. Hamdalla, J. Lancaster, A. M. Hassan, A. N. Caruso, “Electromagnetic Vulnerability of Wires with Arbitrary Shape,” *Proceedings of the AMEREM 2018 Conference*, Aug 27-31, Santa Barbra, CA, 2018.

[13] M. Hamdalla, A. M. Hassan, A. N. Caruso “Characteristic Mode Analysis of Unmanned Aerial Vehicles with Realistic Shapes and Material Composition,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Boston*, MA, 2018.

[14] D. Beetner, V. Khilkevich, A. M. Hassan, J. Hunter, Y. Liu, D. Floyd*, “*Characterization of the Electromagnetic Coupling to UAVs,*” DE Systems Symposium 2018*, September 24-27, 2018

Khan

[1] W. Azad, S. Roy and F. Khan, "A Single Gate Driver-based Four-stage High-voltage SiC Switch Having Dynamic Voltage Balancing Capability," submitted in *2021 IEEE Applied Power Electronics Conference and Exposition* (APEC), Phoenix, AZ, USA, 2020

[2] W. Azad, S. Roy and F. Khan, “A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver” accepted in *47th IEEE Conference on Plasma Science*, 2020.

9.2 Journal Publications

[1] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, “Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field Coupling to Randomly Shaped Wires,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, 2020.

[2] M. Hamdalla, Benjamin Bissen, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, “Characteristic Mode Analysis of Electromagnetic Coupling to Unmanned

Aerial Vehicles," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, 2020.

[3] Khulud Alsultan, Mohamed Hamdalla, Sumitra Dey, Anthony N. Caruso, Praveen Rao, and A. Hassan*, Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform*, *IEEE Open Journal of Antennas and Propagation, In Review*, 2020

[4] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems," *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364-373, 2019.

9.3 External Presentations/Briefings

DEPS Posters and Presentations 2017

[1] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

DEPS Posters and Presentations 2018

[1] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[2] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[3] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

DEPS Posters and Presentations 2019

[1] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[2] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[3] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[4] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[5] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[6] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[7] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[8] Deb Chatterjee, Studies On Antenna Characterization And Propogation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

DEPS Posters and Presentations 2020

[1] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[2] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

GOMAC 2019

[3] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[4] Eliot Myers, Picosecond High Power Switching Technologies

[5] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

9.4 IP Disclosures Filed

Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, 19UMK005, 28SEPT2018

Doynov, “Pulse Differential High-power Microwave Generation”, 19UMK007, 02JAN2019.

Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal”, 19UMK008, 28DEC2018.

Doynov, Caruso, “High-efficiency High-power Microwave Generation using Multipass Non-linear Network Topologies”, 19UMK017, 29AUG2020.

Doynov, “Scalable Modular System for High-power Microwaves Generation”, 20UMK010, 19APR2020.

Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna”, 20UMK011, 19APR2020.

Shepard, “A Novel Optical Fiber Amplifier”, 20UMK012, 02JUN2020.

Shepard, “A Low Noise Optical Amplifier”, 21UMK007, 14SEPT2020.

9.5 Provisional Patents Filed

Doynov, Caruso, “High-efficiency High-power Microwave Generation using Multipass Non-linear Network Topologies”, filed 26NOV2019.

9.6 Non-Provisional Patents Filed

None to date

10.0 Appendix B – Wrap-up Sub-Effort Documentation

10.1 *Ab Initio* Informed TCAD and GaN:C Sub-Effort Wrap-up

What follows is a condensed summary of the sub-group motivation, activity, current results, and suggestions for future work as opposed to a chronological review of reports.

The material properties of gallium nitride (GaN) suggest that, in principle, GaN is well-suited for use in high voltage photo-conductive semiconductor switches (PCSS). The ongoing challenge is to turn the “in principle” performance of GaN into practical performance in device-scale systems. From the literature, progress has been made regarding the fabrication and development of high-quality bulk GaN substrates with the inclusion of dopants to obtain GaN buffer layers with high resistivity. For example, C and Fe are used as dopants to create deep acceptor states to compensate for residual donors in GaN buffer layers. [1,2]

Unfortunately, experimental device design and optimization is usually time-consuming and expensive. In response, the method of Technology Computer-Aided Design (TCAD) for simulating device properties had been widely demonstrated as a powerful tool for rapid design of electronic devices. TCAD simulations combine device geometries and the known electronic properties of the device materials under different conditions (e.g., dopant types, concentrations, and profiles) to produce reliable simulations of device performance. The main input ingredient for TCAD simulation of an arbitrary material is an array of material parameters that describe key electronic response properties. For many common electronic materials (e.g., Si) these parameters are well-known due to decades of experimental and theoretical work. Unfortunately, for relatively new materials such as doped GaN the collection of parameters under different conditions is much less well known. [3] Indeed, there are only a few experiment details about doped GaN that can fulfil the list needed for accurate TCAD device-scale electronics simulation. Therefore, it is necessary to turn to computational and *ab initio* methods to obtain material parameters for use in TCAD simulations.

Such an approach has been demonstrated already for intrinsic GaN among other materials. [4–7] Figure A1 illustrates one proposed organizational flowchart for accumulating the necessary input for a device-scale simulation driven in large part by accumulation of *ab initio* data. In this approach, not all of the data is obtained from a purely *ab initio* approach and empirical and classical molecular dynamics computational methods are used to help check and inform the *ab initio* results. Building a customized approach for doped GaN completely from scratch is well beyond the remit of the sub-effort and would require a much larger and more dedicated effort. However, fortunately, alternative approaches are available that leverage existing technologies (e.g., the Silvaco TCAD application) to enable the development of informed understanding of the device-scale electronic and transport properties of novel doped semiconductors with little if any input from sources beyond *ab initio* calculation.

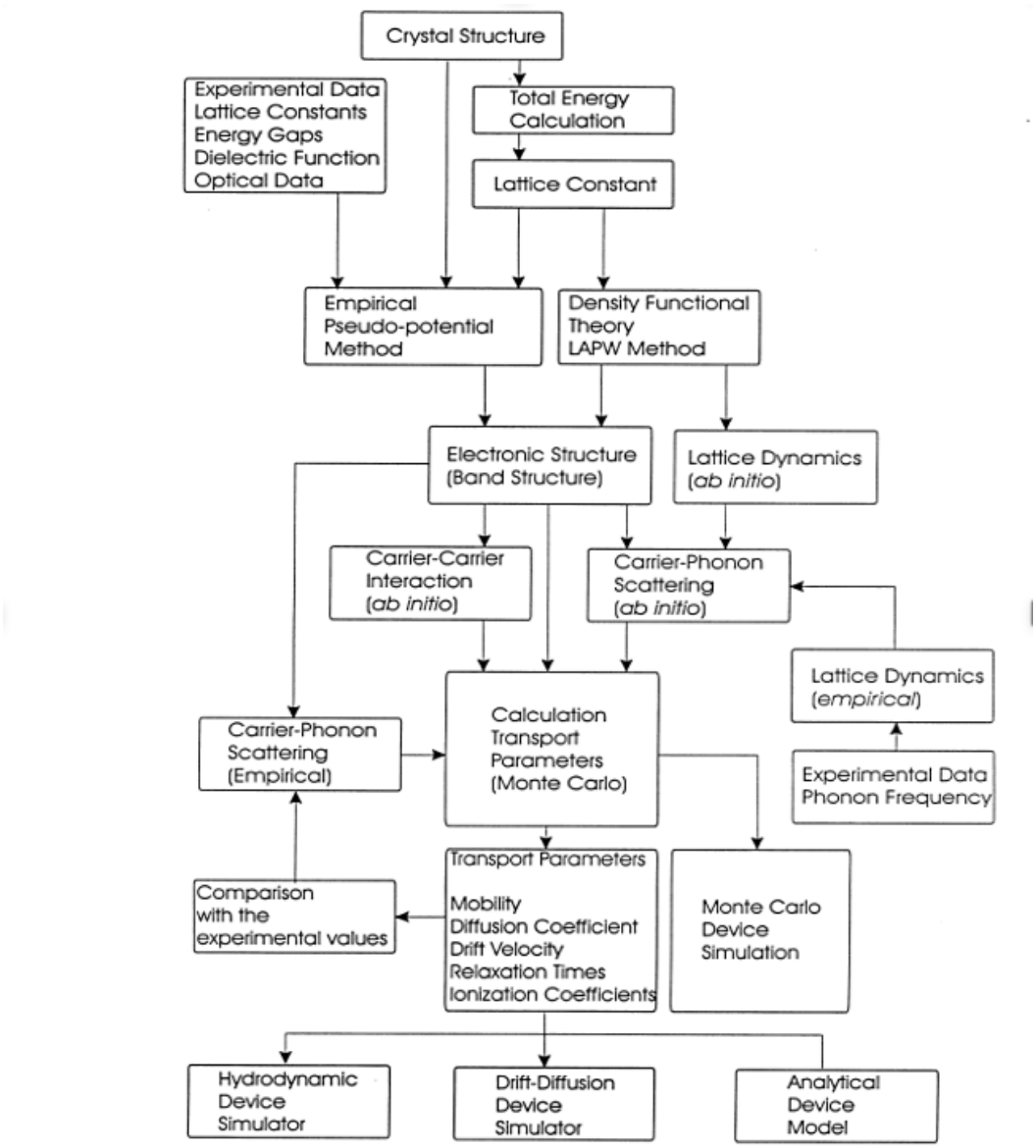


Figure A1: From reference [6]. One proposed method for accumulating the material parameters required for *ab initio* driven simulation of device-scale electronic transport.

As a proposed practical implementation of the flow diagram in Figure A1, intended for the specific input needs of Silvaco TCAD, we brought together the collection of *ab initio* tools shown in Figure A2.

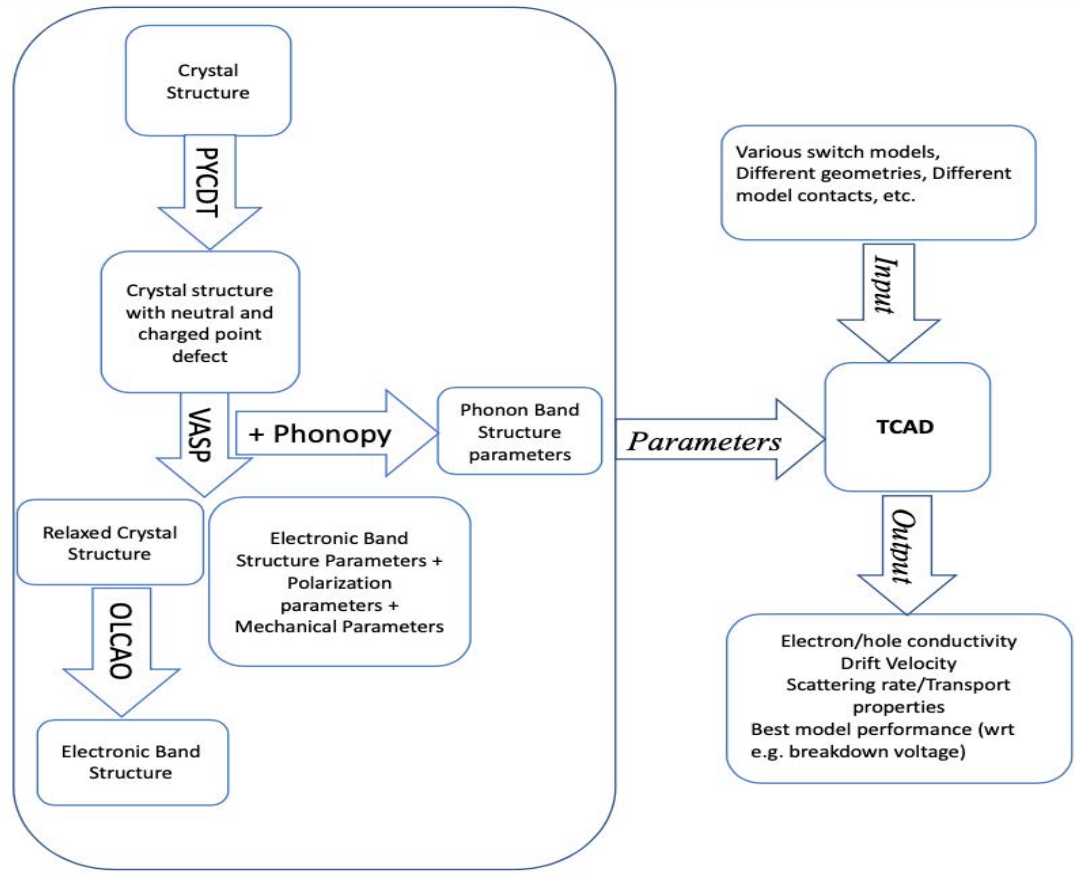


Figure A2: Flow diagram of programs for computing TCAD parameters.

The PyCDT program [8,9] (Python Charge Defect Toolkit) was used to produce models of crystalline GaN with either a C or Fe dopant atom. PyCDT was used instead of manual dopant insertion so that we would have an optimized cell size with limited dopant-dopant interaction, especially for scenarios with non-neutral (charged) dopant atoms. The charge neutral models that were generated are shown in Figure A3.

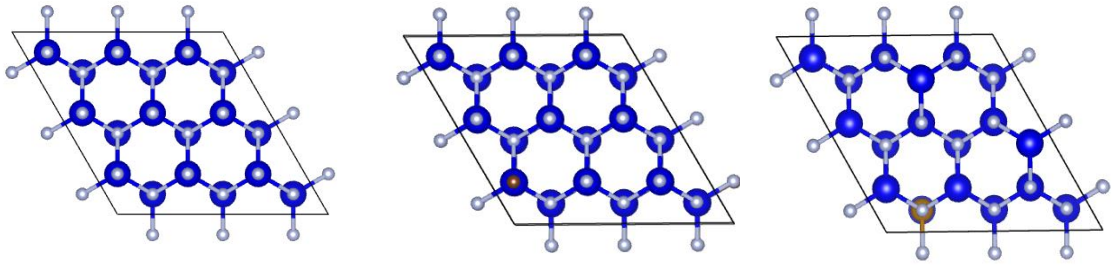


Figure A3: GaN models. Left crystalline GaN, center GaN:C, right GaN:Fe.

The resultant models were subsequently used for computation of the electronic band structure using VASP with a hybrid density functional that includes exact Hartree-Fock exchange [10–12], (a rather computationally intensive calculation for a supercell model). The use of a hybrid density functional is required to be able to obtain a correct band gap. The mixing parameter between the traditional exchange-correlation term and the exact Hartree-Fock exchange was determined for crystalline GaN through iterative trial and error to match the known experimentally determined value. From the relaxed crystal structure for GaN the band structure, band gap, electron/hole effective mass, mobility, polarization parameters, mechanical parameters, dielectric function, and dopant/defect states for GaN were obtained. Those results have been tabulated into Tables A1 and A2. The same mixing parameter could be used for future GaN:C and GaN:Fe calculations, where no experimental value is known. Doped materials require significantly more computational effort because they must be modeled with a supercell approach. Therefore, only some GaN:C and GaN:Fe calculations have been completed to date. Additionally, the shear deformation potentials are currently being calculated but they are also a fairly time consuming type of calculation.

Table A1: Calculated parameters for GaN in comparison to published values along with syntax label used in Silvaco TCAD.

Parameter	Symbol	Syntax	Units	**GaN (**published**)**	**GaN** (This work)	**GaN-C**	**GaN-Fe**
Electron eff. mass (z)	m_{cz}	MZZ	m_0	0.20 [13–15]	0.24		
Electron eff. mass (t)	m_{ct}	MTT	m_0	{0.18, 20} [13–15]	0.23		
Hole eff. mass param.	A1	A1		{-6.56 , -7.24} [13–15]	-6.92		
Hole eff. mass param.	A2	A2		{-0.91, -0.51} [13–15]	-0.674		
Hole eff. mass param.	A3	A3		{5.65 , 6.72} [13–15]	6.02		
Hole eff. mass param.	A4	A4		{-2.83, -3.36} [13–15]	-2.476		
Hole eff. mass param.	A5	A5		{-3.13 , -3.35} [13–15]	-3.21		

Hole eff. mass param.	A6	A6		{-4.86, -4.72} [13–15]	-4.67		
Valence band reference	Ev_0		eV	-2.64 [13–15]	-2.651		
Direct band gap (300K)	$E_g(300)$		eV	{3.44 , 3.42, 3.507,1.74, {3.51, 2.12}, 3.24 [13–15]	2.97		
Spin-orbit split energy	D1	DELTA1	eV	{0.021, 0.019, 0.016} [13–15]	0.020		
Crystal-field split energy	D2	DELTA2	eV	{0.01618, 0.01413, 0.01213} [13–15]	0.01015		
Lattice constant	a_0	ALATTICE		3.190, 3.155, {3.215, 3.182}, 3.197 [13–15]	3.189	3.191	3.194
Elastic constant	C_{33}	C_{33}	GPa	{392, 398, 224}, 354 [13–15]	346.623	338.426	321.574
Elastic constant	C_{13}	C_{13}	GPa	{100, 106, 92}, 68, exp=70 [13–15]	73.369	75.681	62.212
Hydrostatic deformation potential	ac	AC	eV	-4.08 [13–15]			
Shear deform. potential Exp(range)= -9.6 to -3.1	D1	D1	eV	{-0.89, -3.0, 0.7}[1], {-4.9, -5.81, -5.33} [13–15]			
Shear deform. potential Exp(range)= -11.8 to -8.1	D2	D2	eV	4.27, 3.6, 2.1[1],{-11.3,-8.92,-8.84} [13–15]			
Shear deform. potential Exp(range)= 1.4 to 8.2	D3	D3	eV	5.18, 8.82, 1.4 [13–15],{8.2, 5.47, 5.8} [13–15]			
Shear deform. potential Exp(range)= -4.1 to -0.7	D4	D4	eV	-2.59, -4.41, 0.7 [13–15], {4.10, -2.98, -3.09} [13–15]			

Polar optical phonon energy	---------	--------	(meV)				
Acoustic optical phonon energy	---------	--------	V				
Dielectric function		dielectric		9.7, 8.9, 10.4,9.4, 9.5 [13–15]	10.5	10.01	14.185

Tabel A2: Polarization parameters for GaN (C/m^2):

Parameter	**GaN (**published**)**	**GaN**	**GaN-C**	**GaN-Fe**
Spontaneous polarization	-0.034, -0.029 [13–15]			
Piezoelectric constant (z) (e_{33})	0.73, 1.27, 0.67 [13–15]	0.88	0.47	- 0.517
Piezoelectric constant (x,z) (e_{31})	{-0.49,-0.35, -0.34 }, -0.37, -0.22 [13–15]	-0.27	-0.25	- 0.52

The parameters for pure GaN are already incorporated into Silvaco TCAD and so certain TCAD simulations can already be computed such as the breakdown voltage. Computed results are compared to experimental results in Figure A4. Once the ability to compute all of the parameters for GaN has been demonstrated then the same methodologies will be applied to compute the parameters for GaN:C and GaN:Fe followed by the same type of TCAD simulations.

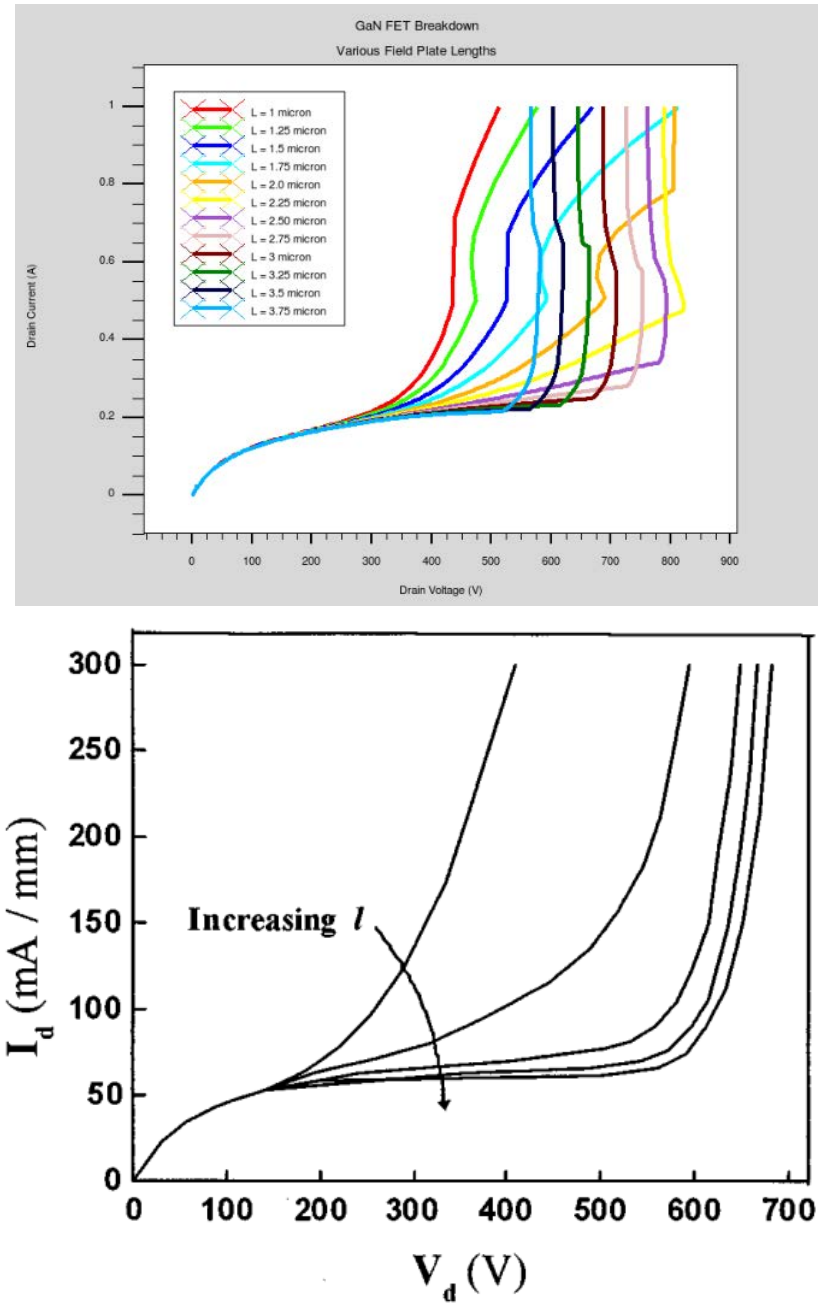


Figure A4: TCAD simulation of breakdown voltage for crystalline GaN compared to experimental data from reference [16].

Additional results were also obtained during the effort leading up to and supporting the progress toward understanding and then computing the parameters in the previously discussed tables. For the sake of brevity those results are not presented here and are instead left within the regular monthly status reports. However, in the most recent months an interest has been developed to understand the role that defects (point and extended)

play in the device-scale properties of doped GaN. The complicated defect structure of GaN is shown in Figure A5 from reference [17].

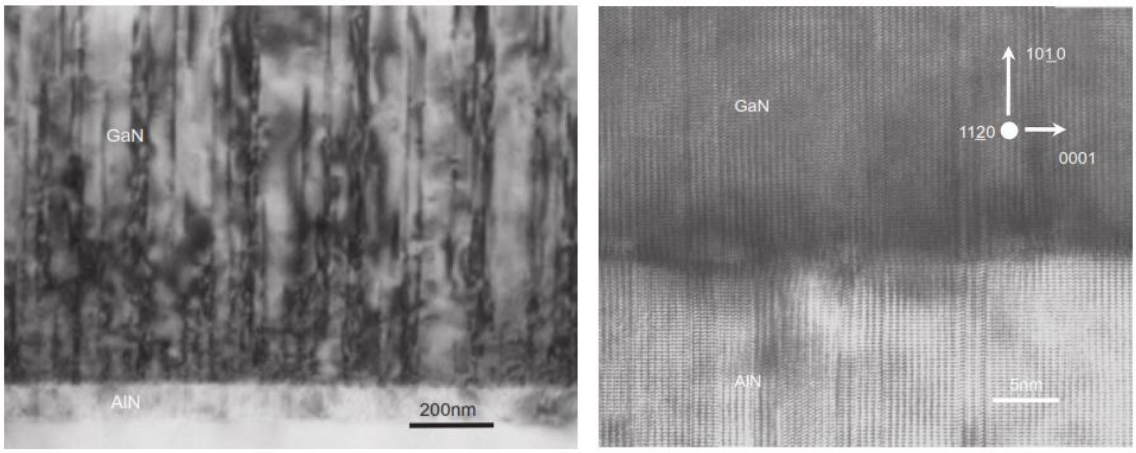


Figure A5: HRTEM images of GaN on an AlN substrate [17]. Extended dislocation defects and interfacial structures are clearly visible.

Regarding the point defects, work was performed to compute preliminary characterizations of the defect structures in GaN:C. The first point of interest was the x-ray absorption near edge structure (XANES) spectra of C-1s orbitals in GaN:C, shown in Figure A6. Although PyCDT was used to evaluate the most likely position for a C point defect, confirmation via experiment would be helpful. The XANES spectra is usually a unique fingerprint of the local atomic environment of the target atom. Therefore, the computed and a measured XANES spectra may be directly compared to definitively identify the most probable C atom position(s) in the crystal cell.

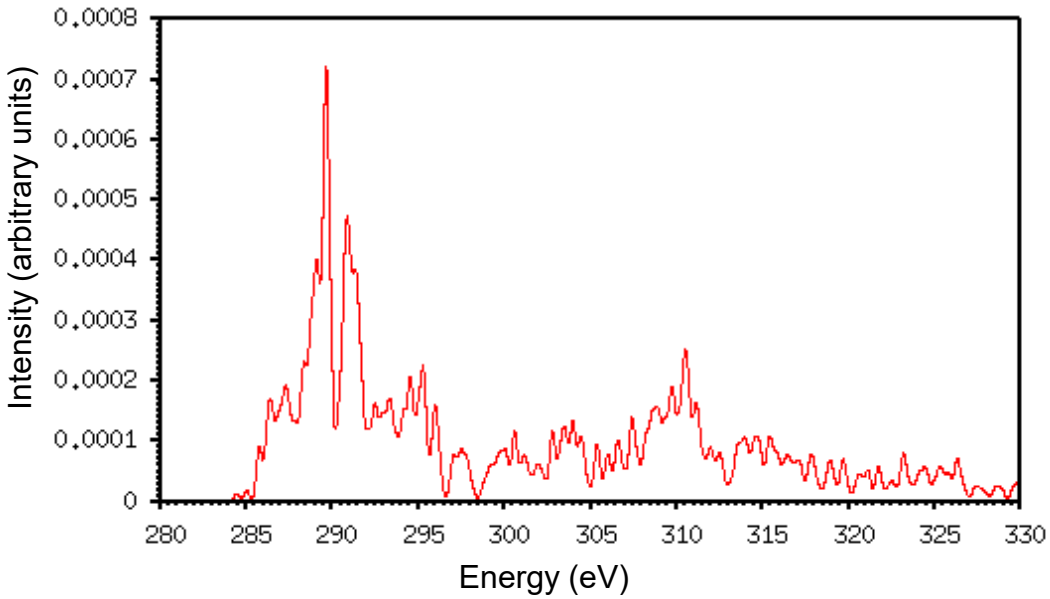


Figure A6: Computed XANES spectrum of C-1s dopant in GaN using the OLCAO method [18].

Beyond the point defects that depend on the dopant choice and concentration, it is expected that extended defects in GaN likely play a crucial role in governing the electronic properties of GaN. However, modeling the extended defects and understanding their collective impact on the bulk properties of GaN under extremely high fields presents a challenging multi-scale problem for which there is limited prior work and for which there are important potential gains in theoretical and practical knowledge.

In summary, the study of doped GaN via *ab initio* methods for the purpose of informing TCAD-level simulations has made significant progress. A methodology has been developed and executed on for crystalline GaN, mostly to the point of completion. The same method is likely to be applicable to GaN:C and GaN:Fe, enabling Silvaco TCAD simulations of device-scale systems with doped GaN. The precise nature of the point defects is accessible and could be confirmed via comparison between computed and experimentally obtained XANES spectra. As the collection of material parameters for point defect containing GaN is nearing completion, the stage is set for potential future exploration of extended defect structures in GaN. Such an effort would require substantial dedicated student time and faculty oversight which is presently outside of the scope of the current broader effort.

References:

1. Hanawa H, Horio K. Increase in breakdown voltage of AlGaN/GaN HEMTs with a high-k dielectric layer. Phys Status Solidi A. 2014;211(4):784–7.

2. Dora Y, Chakraborty A, Mccarthy L, Keller S, Denbaars SP, Mishra UK. High Breakdown Voltage Achieved on AlGaN/GaN HEMTs With Integrated Slant Field Plates. IEEE Electron Device Lett. 2006 Sep;27(9):713–5.

3. Giles MD. TCAD Challenges in the Nanotechnology Era. In: 2005 International Conference On Simulation of Semiconductor Processes and Devices. 2005. p. 7–12.

4. Kamakura Y, Kotani T, Konaga K, Minamitani N, Wakimura G, Mori N. Ab initio study of avalanche breakdown in diamond for power device applications. In: 2015 IEEE International Electron Devices Meeting (IEDM). 2015. p. 5.2.1-5.2.4.

5. Brennan KF, Kolnik J, Oguzman IH, Bellotti E, Maziar F, Ruden PP, Wang R, Albrecht JD. Materials Theory Based Modeling of GaN Devices. In: Pearton SJ, editor. GaN and Related Materials II [Internet]. Singapore: Gordon and Breach Science Publishers; 2000. p. 305–59. Available from: https://books.google.com/books/about/GaN_and_Related_Materials_II.html?id=C6hQ6_lo1o0C

6. Brennan KF, Bellotti E, Farahmand M, Haralson J, Ruden PP, Albrecht JD, Sutandi A. Materials theory based modeling of wide band gap semiconductors: from basic properties to devices. Solid-State Electron. 2000 Feb 1;44(2):195–204.

7. Nilsson H-E, Englund U, Hjelm M, Bellotti E, Brennan K. Full band Monte Carlo study of high field transport in cubic phase silicon carbide. J Appl Phys. 2003 Mar 15;93(6):3389–94.

8. Broberg D, Medasani B, Zimmermann NER, Yu G, Canning A, Haranczyk M, Asta M, Hautier G. PyCDT: A Python toolkit for modeling point defects in semiconductors and insulators. Comput Phys Commun. 2018 May 1;226:165–79.

9. PyCDT: A Python toolkit for modeling point defects in semiconductors and insulators - ScienceDirect [Internet]. [cited 2018 Apr 8]. Available from: https://www.sciencedirect.com/science/article/pii/S0010465518300079

10. Kresse G, Hafner J, Needs RJ. Optimized norm-conserving pseudopotentials. J Phys Condens Matter. 1992;(36):7451.

11. Kresse G, Furthmüller J. Efficient iterative schemes for ab initio total-energy calculations using a plane-wave basis set. Phys Rev B. 1996;54(16):11169.

12. Perdew JP, Ernzerhof M, Burke K. Rationale for mixing exact exchange with density functional approximations. J Chem Phys. 1996 Dec 8;105(22):9982–5.

13. Levinshtein ME, Rumyantsev SL, Shur MS. Properties of Advanced Semiconductor Materials: GaN, AlN, InN, BN, SiC, SiGe. John Wiley & Sons; 2001. 220 p.

14. Barker AS, Ilegems M. Infrared Lattice Vibrations and Free-Electron Dispersion in GaN. Phys Rev B. 1973 Jan 15;7(2):743–50.

15. Abou El-Ela FM, Mohamed AZ. Electron Transport Characteristics of Wurtzite GaN. ISRN Condens Matter Phys. 2013;2013:1–6.

16. Karmalkar S, Mishra UK. Enhancement of breakdown voltage in AlGaN/GaN high electron mobility transistors using a field plate. IEEE Trans Electron Devices. 2001 Aug;48(8):1515–21.

17. Zhou L, Ni X, Özgür Ü, Morkoç H, Devaty RP, Choyke WJ, Smith DJ. Atomic structure of the m-plane AlN/SiC interface. J Cryst Growth. 2009 Mar 1;311(6):1456–9.

18. Wai-Yim Ching, Paul Rulis. Electronic Structure Methods for Complex Materials: The Orthogonalized Linear Combination of Atomic Orbitals [Internet]. Oxford, UK: Oxford University Press; 2012. Available from: http://dx.doi.org/10.1093/acprof:oso/9780199575800.001.0001

ONR HPM Program - Monthly Status Report (MSR) – DEC 2020

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 JAN 2021

Distribution Statement ~A: Distribution authorized to all OSPRES Grant and Contract performers, and any OSPRES uncompensated collaborators. Further dissemination per the Office of Naval Research, Ryan Hoffman (ryan.hoffman@navy.mil, 703-696-3873) or higher DoD Authority.

OSPRES Grant Goal: address and transition technologies and capabilities that enable the OSPRES Grant Objective using the OSPRES Grant Approach, while educating the next generation of pulsed power and defense minded, stewards and innovators.

OSPRES Grant Objective: to execute high-risk, high-payoff efforts that mitigate, fill or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable and electronically steerable high power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average power space, and includes the kill chain considerations including the target and its responsivity to radiofrequency stimuli.

OSPRES Metrics of Success: developed technologies and capabilities that are published in the peer review, protected as intellectual property, and/or, transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use, as enabling/integratable capability(ies).

OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

OSPRES Grant Security: All efforts should be fundamental and publically releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

1.0 Contents

2.0 Executive Summary 3
2.1 Progress, Significant Findings, and Impact 3
2.2 Completed, Ongoing, and Cancelled Sub-Efforts 4
2.3 Running Total of Academic and IP Program Output 5
3.0 Switch Evaluation and Innovation 6
3.1 Si-PCSS Top Contact Modeling and Optimization for Cooling Requirements 6
3.2 Lasers and Optics 8
3.3 Si-, SiC- and GaN Modeling and Evaluation 10
3.4 Multi-Stage Optical Amplifier 11
3.5 GaN:C Modeling and Optimization 12
3.6 Diode-Based NLTLs 14
4.0 Prime Power and Conditioning 18
4.1 HV Switch Pulsed Chargers 18
5.0 Tradespace Analysis of Ultra-Wide-Band Antenna Arrays 21
5.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs). 21
5.2 Tradespace Analysis of Other Ultra-Wide-Band (UWB) Single Elements 23
6.0 RF Coupling 26
6.1 Enclosure Effects on RF Coupling 26
7.0 Thermal Management 30
7.1 Jet Impingement Optimization 30
8.0 Program Management 32
8.1 Issues 32
8.2 Interactions with Others 32
8.3 Major Procurement Actions 32
8.4 Travel 32
8.5 Pending or Upcoming Public Release Requests 32
9.0 Appendix A – Academic and IP Output 33
9.1 Conference Publications 33
9.2 Journal Publications 33
9.3 External Presentations/Briefings 37
9.4 IP Disclosures Filed 38
9.5 Provisional Patents Filed 38
9.6 Non-Provisional Patents Filed 38

2.0 Executive Summary

2.1 Progress, Significant Findings, and Impact

Optimization of SiPCSS top contacts for reduced laser trigger energy, and reduced current density or crowding around the field enhanced contact points/areas is close to a final solution space (reaching a dual local minimum). Shot lifetime measurements will confirm whether the contact spacing design change improves, and this sub-effort will be transitioned for OSPRES contract use.

Nanosecond-scale pulse-to-pulse tunability of GaN:C PCSS from 3.75 to 5.77 ns at low voltages (up to 100 V), for direct RF Modulation, was demonstrated.

The jet impingement-based thermal group found a means to compensate 0.2 kW (i.e., >200 MW/m^3) average power and maintain the Si-PCSS source's average temperature at 50 °C; this temperature result is 10 °C less than the laminar-flow-based design of an equivalent volumetric form-factor (cross-flow thermal management system) as designed for the OSPRES-contract source array demonstrator.

In the fiber laser development effort, self-focusing in Gaussian beams was shown to depend on the power, rather than the intensity, of the beam. A theory formulated to explain this effect predicts that guided modes in fiber can circumvent this limitation. Further, an upper bound on ASE-induced timing jitter was shown to justify the cost of a higher power seed laser diode in the fiber laser designs.

For the diode-based NLTL effort, inclusion of lead inductance and parallel capacitance was found to improve the accuracy between simulation and measurement.

From the RF Coupling group, quantitative measures of microwave losses through penetration of perforated UAV enclosures/casings are reported (building on the qualitative results from last month and for the lossless case).

For the high voltage switch program, a 6.8 kV rated four-stage in-house HV switch has been tested up to a DC supply voltage of 4 kV at a switching frequency up to 10 kHz. Output voltage across the 3.2 kΩ resistive load up to a DC supply voltage of 4 kV was demonstrated.

For the array aperture area reduction effort, a 15×15 array physical aperture area is reduced by ≈30% by changing the grid formation from a square to a hexagonal lattice, with the cost of a slightly decreased gain and loss of electronic steerability. However, these trades are well worth the price, especially in the mobile HPM antenna SWAP missions.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

	Start	End
2.2.1 On-going Sub-Efforts		
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-based Non-Linear Transmission Lines	FEB 2018	Present
Heat Transfer by Jet Impingement	MAY 2018	Present
X-PCSS Comparison (X=Si, SiC, GaN)	NOV 2018	Present
HV Switch Pulsed Chargers	DEC 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
2.2.2 Completed Sub-Efforts		
Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
2.2.3 Cancelled Sub-Efforts		
Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020

2.3 Running Total of Academic and IP Program Output

See Appendix A for authors, titles and inventors (note: this list is still being updated)

2.3.1	*Conference Publications*	31
2.3.2	*Journal Publications*	1 (5 submitted/under revision)
2.3.3	*External Presentations/Briefings*	18
2.3.4	*IP Disclosures Filed*	8
2.3.5	*Provisional Patents Filed*	1
2.3.6	*Non-Provisional Patents Filed*	0

3.0 Switch Evaluation and Innovation

3.1 Si-PCSS Top Contact Modeling and Optimization for Cooling Requirements

3.1.1 Problem Statement, Approach, and Context

Primary Problem: High-average-power 1064-nm picosecond class lasers are too large (1100 cm^3/W) and monetarily expensive ($1000/uJ*pulse) for the Navy afloat missions.

Solution Space: Improve laser power density, or better laser interaction and downstream processes with the photoconductive switch.

New Sub-Problem: Increased current density with increased laser windowing spacings.

State-of-the-Art (SOTA): PCSS contact patterns spaced at tens-of-microns for switches and photoconductors optimized for other geometries/objectives are over-engineered for heat reduction due to high current.

New Deficiency in the SOTA: Non-optimized contact patterns and increased cooling requirements (11% higher between 100 µm and 350 µm spacing, see Figure 3.1.1) due in part to thermal hotspots, current density hotspots, and on-state resistance in balance with previous laser requirements.

Solution Proposed: Optimize contact pattern specific to the OSPRES Si-PCSS dimensions, mechanical shape, electric field shape, doping profile, and ARC to meet reduced required cooling considering previous laser requirements.

Relevance to OSPRES Grant Objective: While maintaining 'enhanced SWaP-C^2 for the laser system needed to drive the PCSS or reduced laser requirements, which subsequently meets the modular and scalable volume and cost aim-points' cooling system requirements are considered that result in maintaining device operation lifetime in excess of 2×10^8 shots/lifetime at medium power.

Risks, Payoffs and Challenges: Top contact not most direct impact on CCE, major laser effectiveness and/or smaller laser needed, models do not represent reality and need additional physics: appropriate physical parameters and applicable physical models. Metallization for optimized top contacts is inexpensive and easy to manufacture.

3.1.2 Tasks / Timeline / Milestones

(A) Fabricate top contacts and test on-state resistance vs incident laser energy/ 15 DEC to fabricate / Top contacts metallized / FEB delivery of new top contacted Si-PCSS.

(B) TCAD determination of Si-PCSS variability in optimized top contacts dependent on p-doping profile peak concentration and doping depth for Boron and Aluminum. More accurate determination of optimal spacing in laser windowing of top contacts and switch geometry dependence for general applicability of optimal top contact.

(C) Optimize laser windowing spacing (less than 350 µm optimal considering only laser energy) using heat removed from the switch in TCAD with addition of temperature hotspots to quantify tradeoff considering reduced cooling vs reduced laser energy for on-state resistance.

3.1.3 Progress Made Since Last Report

(A) Top contacts metallized; await bottom metallization, anti-reflective coating, beveling and passivation for delivery to UMKC.

(B) Not yet completed.

(C) Have performed thermal TCAD simulations for temperature hotspots and heat removed for 100 µm and 350 µm laser windowing spacings for comparison.

3.1.4 Significant Finding(s) and Mission Impact

Heat removed during the output pulse and part of turn-off was higher in the 350 µm case (average power 14 W and integrated energy 1.2 nJ) compared to the 100 µm case (average 12 W and total 1.0 nJ) as shown in Figure 3.1.1 (Right). The average temperature of the Si-PCSS device model (see Left) was higher in the 350 µm case (300.36 K) than in the 100 µm case (300.51 K) consistent with the higher heat removal at the 300 K thermal contact (cathode). Trending oppositely, the maximum temperature hotspot was higher in the 100 µm case due to the end model of the top contact being smaller than in the 350 µm case.

The 100 µm spacing has less heat extracted, less average device temperature but hotter maximum temperature hotpots due to a smaller end model spacing. Overall, the 100 µm spacing reduces cooling requirements at the expense of slightly increased required laser energy for some, fixed on-state resistance (see Oct 2020 MSR).

The optimization of the top contact laser windowing spacing for cooling requirements primarily leads to increases in device operation lifetime while still reducing required laser energy. Including considerations for cooling narrows the range of possible optimal laser windowing spacings and leads to a more optimized spacing than when considering laser requirements alone.

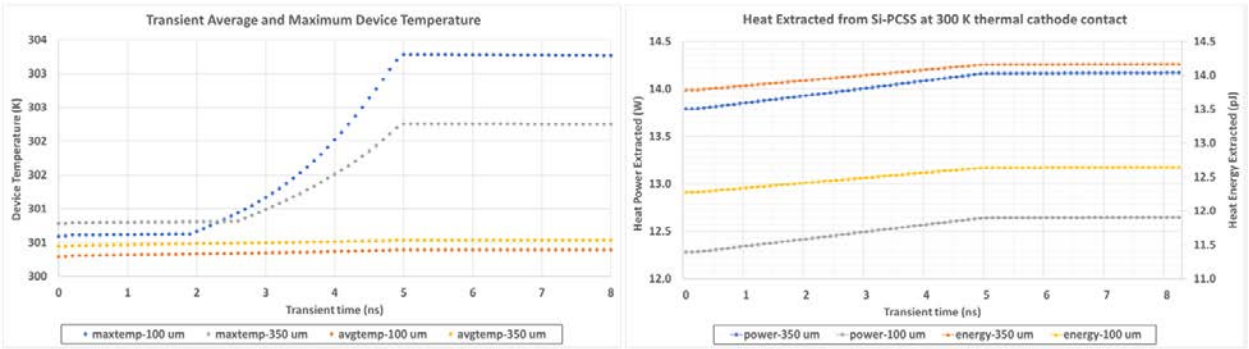


Figure 3.1.1. (Left) Average device temperature only increases slightly over reverse-bias steady-state temperature while maximum device temperature increases more significantly during the power moving through the Si-PCSS. (Right) Heat extracted through 300 K thermal cathode contact increases until power through switch ends and only slowly increases.

3.2 Lasers and Optics

3.2.1 Problem Statement, Approach, and Context

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS embodiments of HPM-based defense systems.

Solution Space: Optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution.

Sub-Problem: Amplified spontaneous emission (ASE) and fiber nonlinearities impede optical amplifier performance, while optical pump power system costs often dominate.

State-of-the-Art (SOTA): Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs are prohibitive until reduced by a factor of two.

Solution Proposed: A pre-burst optical pumping scheme can reduce costs by a factor of at least ten.

Relevance to OSPRES Grant Objective: Enhanced SWaP-C^2 for the laser system needed to drive the PCSS, which subsequently meets the modular and scalable volume and cost aim-points.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability.

3.2.2 Tasks / Timeline / Milestones

(A) Reduce costs by a factor of two or more. / July 2020 / Simulations showed that we can drop the pump power costs by a factor of 40 with tolerable pre-burst ASE. UMKC invention disclosure filed 02JUN2020. Task completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / A linear gain theory predicted the in-burst ASE over our spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020. Task completed.

(C) Design saturable gain devices which avoid nonlinear damage. / On-going / Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Calculate and manage timing jitter. / On-going / Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) Demonstrate a cost-reduced fiber laser. / AUG 2021 / Key parts ordered.

3.2.3 Progress Made Since Last Report

(C) Self-focusing in Gaussian beams was shown to depend on the power, rather than the intensity, of the beam. A theory formulated to explain this effect predicts that guided modes in fiber can circumvent this limitation.

(D) An upper bound on ASE-induced timing jitter was shown to justify the cost of a higher power seed laser diode in the fiber laser designs (relative to those proposed for the normal laser designs of the scaled demonstration).

(E) Specific design of proof of concept (POC) fiber laser prototype initiated.

3.2.4 Significant Finding(s) and Mission Impact

Via COMSOL simulations we have shown that self-focusing in Gaussian beams depends on the power of the beam, rather than its intensity. This is surprising since in self-focusing the index of refraction depends on the local field intensity, I, viz., $n = n_0 + n_2 I$. The intensity-dependent index acts like a lens which focuses the beam into a tighter spot leading to material damage and optical distortions. Simulations with Gaussian beams of different minimal cross-sectional areas, A, however show that the amount of self-focusing depends on the total beam power, $P = I A$, instead of the intensity. Our interpretation of this is that with larger A we, in effect, have a larger lens. The larger lens then counters any hope of reducing self-focusing by distributing power over a larger cross-sectional area to reduce the beam intensity. This result however only applies to Gaussian beams, such as one would have in a “free-space” (i.e., non-fiber) laser implementation, and the guided modes in a fiber will behave differently. The development of simulations for the guided mode case is underway and we anticipate that these can reveal another advantage of fiber (over free-space) laser implementations.

Our simplest model of ASE-induced timing jitter places an upper bound on the jitter arising from propagation through dispersive media, while the ASE induces slight frequency shifts in the overall light. This effect scales with the distance of propagation and thus is typically greater in fiber lasers than in free-space lasers. For example, an optical amplifier of system gain G = 8 million is needed to drive 4 Si-PCSS switches from the 10 pJ/pulse seed laser diode (LD) planned for the scaled demonstration. If we implemented such in 3 km of fiber (with a dispersion parameter of 520 ps/nm-km) the upper bound on timing jitter would be 191.7 ps – substantially over the 40 ps spec. of the laser. That assumes an ASE power level predicted by linear gain theory – which we could suppress via gain saturation or reduce by using a higher power seed LD. For the POC fiber laser prototype we will use a higher power seed LD, resulting in a system gain of G = 12,500 which yields an upper bound of only 0.2995 ps on timing jitter (in 3 km of such fiber). The increased seed LD cost (of $2,300 rather than $960) is justified. As well is as an additional $2,470 for a superior current driver (installed and tested) to maximize performance and to expedite POC fiber laser prototype development.

3.3 Si-, SiC- and GaN Modeling and Evaluation

3.3.1 Problem Statement, Approach, and Context

Primary Problem: Interdependent and unquantified operational parameters (photoabsorption, carrier dynamics, sub-band levels, etc.) of novel photoconductive materials complicate optimization and evaluation of PCSS-based HPM source drivers with external trigger requirements.

Solution Space: Model and simulate Si-, SiC- and GaN-PCSSs with varied geometry, doping profiles, contact layering, and post-processing techniques to evaluate their optical trigger and cooling requirements. Evaluate their performance at theoretical limits and explore novel fabrication techniques to push beyond established state-of-the-art limitations in terms of carrier dynamics, peak and average power, repetition rates, and cooling needs.

Sub-Problem: Incompletely defined dopant-dependent (carbon and nitrogen) sub-band levels and their respective optical absorption parameters for GaN, limiting application-level modeling and implementation of GaN-PCSSs.

State-of-the-art (SOTA): Linear-mode GaN-PCSS switching with sub nanosecond rise and recovery times, requiring >300 mJ/pulse optical energy to obtain ~100 mA output current.

Deficiency in the SOTA: Limited per-pulse HPM power throughput (<MW order) resulting from lack of photoconductive gain and SOTA-limited incident optical energy.

Solution Proposed: Implement lock-on mode of operation in GaN-PCSS with gain to reduce the optical energy requirements.

Relevance to OSPRES Grant Objective: Determines application-specific SWaP-C^2 optimized solution for source-driver subsystem as a combination of switch material and pulse forming network.

Risks, Payoffs, and Challenges: Lock-on operational mode would potentially reduce the optical requirements by a factor of 10, but the operational mechanism is not well understood and has not been defined mathematically. This raises an issue with quantifying the system requirements for repeatability, alongside potential issues with increased turn-off times due to sustained conduction.

3.3.2 Tasks / Timeline / Milestones

(A) Model carbon-compensated GaN-PCSS with vertical and lateral geometries, varied contact layers, carrier dynamics (generation, transport, and recombination) and circuit topologies to verify operational mode and current gain; then, calculate reduction in optical requirements in contrast with linear mode. [Feb-Mar 2021]

(B) Evaluate the doping profiles, contact layering, and patterning for SiC-PCSS and explore suitable fabrication techniques to achieve desired optimal doping profile using TCAD-Athena. [Feb-Mar 2021]

(C) Complete parametric study of SiC-PCSS including rise and recovery time optimization simulations for varied vanadium and nitrogen concentrations, and high voltage transient response study for varied geometry, optical trigger, contact design, and illumination area. [Mar-Apr 2021]

3.3.3 Progress Made Since Last Report

(A) Initial modeling of uncompensated (intrinsic) 10 nm thick lateral GaN-PCSS over SiC substrate with switch gaps of 500 µm and 1000 µm have been completed. Optical absorption profile is being studied for the wavelength range of 355–405 nm. Taking the future availability of GaN devices into account, vertical geometry of GaN-PCSS is also being studied, which would facilitate absorption depth required 402–405 nm optical triggering.

(B) none

(iii) Task scheduled to be studied after (ii)

3.3.4 Significant Finding(s) and Mission Impact

Vertical GaN-PCSS (intrinsic) model simulations showed higher optical absorption compared for 402-405 nm pulse compared with lateral models, owing to the absorption depth requirements. Comprehensive study of GaN's intrinsic and extrinsic optical properties in conjunction with device design provide insight into inter- and intra-band transitions that directly affect conduction mode and help in identifying an optimal path to reducing optical energy/pulse requirement.

3.4 Multi-Stage Optical Amplifier

3.4.1 Problem Statement, Approach, and Context

Primary Problem: Need for heavy (~125 lbs.), bulky (~10 cu-ft), and expensive (~$120,000) conventional laser systems (1064 nm) in PCSS-based HPM applications, with an additional need for second and third harmonic generation (SHG/THG) optics to trigger WBG solids (GaN/SiC).

Solution Space: Design and implement a compact (~1.1 cu-ft), lightweight (10–15 lbs.), and inexpensive (<$15,000) alternative for conventional high average power optical trigger (laser) system to improve SWaP-C^2 index of HPM systems.

Sub-Problem: Unavailability of commercial-off-the-shelf (COTS) miniature optical sources with sub-nanosecond pulse widths and tens-of-µm beam width, delivering >1-Watt power to implement as a makeshift/turnkey solution for the laser system.

State-of-the-art (SOTA): High average power picosecond pulsed lasers available up to 50 W output power with a gain factor up to 40 dB (~10,000x power) with laser amplifier.

Deficiency in the SOTA: High average power 1064-nm pulsed lasers are bulky, require auxiliary systems, and additional optics for SHG/THG generation for wide bandgap (WBG) device triggering.

Solution Proposed: Multi-stage cascaded optical amplifier powered by laser diodes (arrays) and GaN-PCSS as a compact, inexpensive laser replacement capable of ~175°C operation.

Relevance to OSPRES Grant Objective: Provides an enhanced SWaP-C[2] compliant solution for the laser (optical trigger) subsystem, with a subsequent impact on overall HPM system cost, volume, and power (optical and electrical) requirements.

Risks, Payoffs, and Challenges: Complex interconnect and thermal management system (TMS) design at high temperature (130–175°C) operation; unavailability of COTS high power pulsed laser diodes could potentially raise a need for research in laser diodes (arrays).

3.4.2 Tasks / Timeline / Milestones

Complete initial stage experimental implementation of the optical amplifier and demonstrate positive current gain using GaN-PCSS, triggered with a miniature 404 nm laser diode. [Feb 2021]

3.4.3 Progress Made Since Last Report

A feasibility study for the cascaded multi-state optical amplifier design has been completed and the functional requirements have been determined for the laser diodes (arrays) and source driver. We are working towards prototyping the proposed design using a 404 nm laser diode, vertical GaN-PCSS, and 808 nm laser diode array (LDA).

3.4.4 Significant Finding(s) and Mission Impact

Need for lock-on conduction mode has been determined for triggering the laser diode array (LDA) with minimal number of amplification stages. This contributes to maintaining the R&D and implementation costs low (10–12% of the conventional system), while achieving the expected goal of miniaturizing the optical subsystem by 1–2 orders of magnitude.

3.5 GaN:C Modeling and Optimization

3.5.1 Problem Statement, Approach, and Context

Primary Problem: Need for a more compact, cost-effective RF pulse generation system for Navy afloat missions on smaller vessels and vehicles.

Solution Space: Improve efficiency and reduce necessary material, size, and thermal requirements by utilizing gallium nitride (GaN) in PCSSs through exploitation of its theoretical material properties which allow for higher operating voltages, frequencies, and temperatures, while also eliminating the need for pulse-shaping transmission lines through direct RF modulation using the laser/photon source driving the PCSS.

Sub-Problem: Lack of maturity in compensated gallium nitride semiconductor (i.e., GaN:X with X=C,Fe) PCSS manufacturing, development, and optimization.

State-of-the-Art (SOTA): Si-based PCSS with >10 kV operational voltage, cooling system capacity of 500 W/cm^2, and theoretical breakdown of 1.3 MW/cm.

Deficiency in the SOTA: Si-based technologies requiring ~100 µJ optical pulses per 4 MW of RF output power, increasing the size of laser necessary for device triggering; long recovery time (ones-of-µs), limiting quick opening and high pulse-repetition-rate operation along with increased heating in the PCSS; critical electric field of 0.3 MV/cm, leading to devices that are ones of cm^2 in area for the target peak power; and operating temperature of <160°C, leading to increased cooling requirements.

Solution Proposed: Replace Si-PCSS device with GaN:C utilizing direct RF modulation — eliminating the need for a bulky pulse-forming transmission line (~3 ft long) — capable of handling >3 MW (peak power) with ~20 µJ of incident optical energy, device area <1 cm^2, and operating temperature ~500°C (theoretical temperature which will be limited by circuit components and solder).

Relevance to OSPRES Grant Objective: Reduction in size and cost for cooling system, removal of a pulse-shaping system, and decrease in material cost, leading to enhanced SWaP-C^2 capability with greater modularity and scalability.

Risks, Payoffs, and Challenges: Due to manufacturing limitations, GaN PCSS devices tend to be limited to lateral geometries (both contacts on the top side of the device), limiting operating voltage due to current crowding and surface flashover. The recovery time (ones-to-tens-of-ns) may lead to device heating and increased DC content when generating RF content with a period on the same order as the recovery time.

3.5.2 Tasks / Timeline / Milestones

(A) **Jan 2021** Demonstrate RF unipolar modulation in the 1–2 GHz regime and up to 2 kV operating voltage with current PCB setup and the automated optical delay system.

- i. Test using Sylgard 184 covering the GaN:C device to prevent flashover.
- ii. Repeat HV testing with GaN:C PCSS enclosed small with SF_6 gas chamber, to prevent flashover and allow for higher operating voltages. The chamber will be designed and fabricated using material offering minimal losses of laser energy.
- iii. Seek further solutions to achieve ~10 kV operating voltage depending on success with Sylgard 184 and SF6, including studying the feasibility of vertical GaN:C devices that would eliminate surface flashover seen in lateral devices.

(B) **March 2021** Demonstrate RF bipolar modulation using two GaN:C devices, along with a positive and negative power source, based on the pulse-switch-out-generator-based circuit and setup with the automated optical delay system.

(C) **April 2021** Move test setup and show higher center frequency content and repetition frequency of unipolar and bipolar modulation using the neoLASE (70 ps) laser versus the wedge (~1.5 ns) laser.

(D) **May 2021** Complete study of recovery for differing gap lengths, incident energies, and operating voltages and find solutions to reduce the recovery time.

3.5.3 Progress Made Since Last Report

(A) Sourced components (attenuators, pulse chargers, power supplies, etc.) for demonstration of direct bipolar RF modulation.

(B) Demonstration of ns-scale pulse-to-pulse tunability of GaN:C PCSS from 3.75 to 5.77 ns at low voltages (up to 100 V).

(D) Wave optics module purchased for COMSOL, and work began on building a GaN:C PCSS model for comparison to experimental results.

3.5.4 Significant Finding(s) and Mission Impact

By utilizing a wide, direct bandgap material as a PCSS RF source, eliminating the need for bulky pulse-forming transmission lines, cooling requirements, and material necessary for each PCSS device, leads to a greater HPM SWaP-C^2 factor. Towards this end, demonstration shows that direct unipolar modulation is possible at low voltages and work will be done to demonstrate direct unipolar modulation up to 2 kV. COMSOL will be used as a tool to predict future performance of GaN:C devices to help direct testing to conserve the number of devices damaged. COMSOL will also be used to help diagnose thermal and design deficiencies within the devices.

3.6 Diode-Based NLTLs

3.6.1 Problem Statement, Approach, and Context

Primary Problem: Size, weight, and cost of pulse forming/shaping networks (PFNs) need to be reduced and optimized for navy afloat missions.

Solution Space: Develop a lumped-element nonlinear transmission line (LE-NLTL) as a pulse shaping network for the conversion of energy to the ultra-high frequency (UHF) band at single MW peak power.

Sub-Problem: Metrics used for component selection are designed for LE-NLTLs operating at sub 0.1 GHz frequencies. Using such metrics alone to design LE-NLTLs capable of single GHz frequency generation introduces a trial by error nature to the design process wherein frequency/power generation predictions and measurements can differ by a few hundred MHz or the design potentially fails to operate at all.

State-of-the-Art (SOTA): LE-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit. Simulations of LE-NLTLs indicate achievable frequencies in the single GHz range.

Deficiency in the SOTA: Simulation/measurement agreement becomes increasingly sensitive to parameters and factors outside of inductive and capacitive element choice alone. Disparities between measurement and simulation above contribute to a trial by error design process for LE-NLTL networks.

Solution Proposed: Identify and characterize diode parameters affecting frequency generation in the context of a NLTL application and identify limits/desired ranges required for UHF generation. Such parameters include, but are not limited to: diode frequency response, diode reverse bias hold-off voltage, diode small signal capacitance, diode

chip/package parasitics, and diode relaxation time. Inclusion of such parameters increases simulation accuracy and improves the LE-NLTL design/implementation pipeline.

Relevance to OSPRES Grant Objective: The SWaP-C^2 capabilities of LE-NLTLs lend the technology towards applications which require modular, scalable, and low-cost pulse shaping networks (shown in Figure 3.5.1) .

Figure 3.5.1: 20 cell D-NLTL of dimensions 1.1 x 23.45 cm constructed with COTS components.

Risks, Payoffs, and Challenges: There exists a potential tradeoff between power and frequency generation. Devices such as ceramic capacitors may be used in a LE-NLTL to generate high peak power due to their break down potentials in the 10s of kV, however, such devices become highly resistive at 0.1–0.2 GHz frequencies. Diodes have been shown to be operational at frequencies upwards of 0.4 GHz, however, possess low hold off potentials limiting peak output power. The payoff to overcoming these challenges is significant reductions in PFN size and cost.

3.6.2 Tasks / Timeline / Milestones

(A) Construct a LE-NLTL prototype capable of center frequency generation of 0.5–1.5 GHz and peak power generations of single MWs.

(B) Identify and characterize diode parameters beyond junction capacitance, hold off potential, and rate of capacitance drop that impact frequency generation in the LE-NLTL context.

(C) Construct and characterize a low-voltage voltage-tunable LE-NLTL using the SS22T3G and SMV1702 diodes.

(D) Identify candidate discrete components (both inductive and capacitive) for LE-NLTL applications.

3.6.3 Progress Made Since Last Report

(A) Initial tests were performed on a 40-cell LE-NLTL prototype consisting of a SMV1702 diode and 22 nH air core inductor. A 3 V pulse with a 15 ns rising edge produced a center frequency of 253 MHz and a peak voltage of 6.94 V.

(B) Simulations of the SMV1702 line utilized manufacturer provided parasitics for the diode package including lead inductance and parallel capacitance producing the best agreement between simulation and measurement to date (shown in Fig. 3.5.2).

> (i) Simulations including manufacturer parasitics produced a center frequency of 404 MHz when fulling saturating the diodes.

(C) A LE-NLTL topology capable of voltage biasing the diodes was simulated without losses. Voltage biasing the diodes enabled both control over the center frequency generation and the use of bipolar pulses to excite the line. Voltage biasing increased center frequency by 30% of its unbiased value. The use of bipolar excitations allows for greater diode saturation for smaller excitation amplitudes.

(D) A search of potential high voltage (Vr > 10 kV) diode candidates was performed. A model K100UF diode from the manufacturer Voltage Multipliers Inc was identified as a potential candidate with a lossless center frequency generation of ~2 GHz.

3.6.4 Significant Finding(s) and Mission Impact

Significant findings in December were on two fronts: improved simulation techniques and simulations of designs capable of frequency tuning through voltage biasing. Manufacture package parasitics were utilized in simulations with the result of increased agreement between simulated and measured results as shown below in Figure 3.5.2. Improvements in simulation techniques reduce the trial by error aspect of LE-NLTL design, making the process more efficient and cost effective. Designs capable of voltage biasing the diodes allow for both control over the center frequency and the ability to use bipolar waveforms as shown in Figure 3.5.3. The use of bipolar waveforms allows for greater diode saturation with a smaller excitation amplitude. Greater diode saturation increases center and Bragg frequency magnitude due to a decrease in the average capacitance of the network.

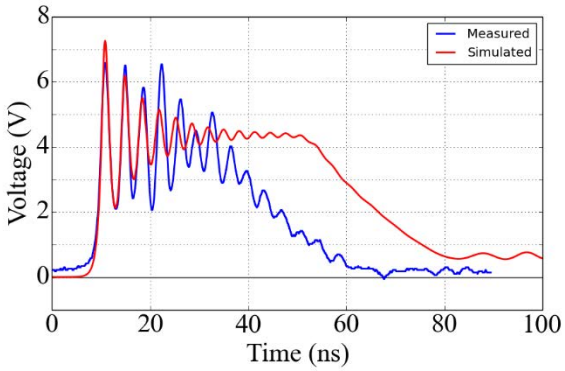


Figure 3.5.2: Shown above is a comparison between the measured (blue) and simulated waveforms (red) produced by a LE-NLTL consisting of 40 cells, each containing a 22 nH air core inductor and one diode (model SMV1702) in reverse bias. The inclusion of the manufacturer provided lead inductance and parallel capacitance shows good agreement with the measured waveform.

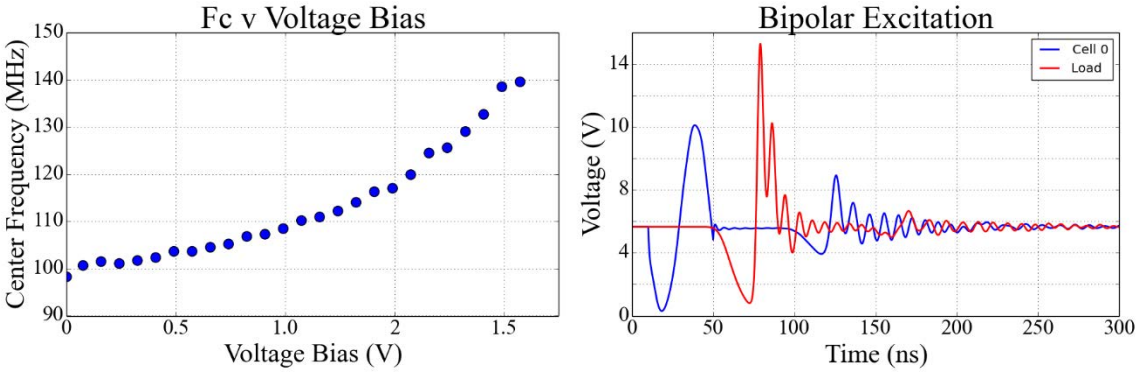


Figure 3.5.3: (Left) Simulated results of voltage tuning on center frequency. (Right) Proof of concept of a bipolar excitation. Both circuits consisted of 20 cells, 22 nH inductance, 1 SS22T3G diode. Voltage biasing was provided by a DC source connected to each cell through a 1 kΩ resistance.

4.0 Prime Power and Conditioning

4.1 HV Switch Pulsed Chargers

4.1.1 Problem Statement, Approach, and Context

Primary Problem: Commercially available high-voltage solid-state switches made by BEHLKE are the best in SWaP-cooling, but are expensive, have long lead times (2–3 months), and are made outside of the US. For the Navy afloat mission to be successful, we need a sustainable supply of US-manufactured switches at a much lower cost.

Solution Space: Design and demonstrate modular high-voltage (~10 kV) and fast (repetition frequency = 100 kHz) solid-state switches using a combination of series- and parallel-connected commercially available inexpensive discrete MOSFETs and custom high-voltage (~10 kV) isolated gate drivers.

Sub-Problem: Voltage balancing among the series-connected MOSFETs, minimization of gate signal delays, cooling of the individual MOSFETs, balancing resistors, high-voltage isolation required for the power supplies, and the controlling pulse width modulated (PWM) signal as well as differential voltage feedback measurement across individual MOSFETs.

State-of-the-art (SOTA): Direct liquid-cooled solid-state switch from BEHLKE (e.g., HTS-151-30).

Deficiency in the SOTA:

1. BEHLKE made switches are expensive. For instance, a single HTS-151-30 switch costs around $5,000.
2. BEHLKE switches along with direct liquid cooling units occupy a considerable amount of space. For instance, a HTS-151-30 switch from BEHLKE has a footprint of approximately 225*85*75 mm without considering the liquid cooling system. Some key parameter of this switch are as follows.

   i) Maximum operating voltage = 15 kV

   ii) Maximum continuous load current = 2.52 A (without cooling), 30 A (with liquid cooling)

   iii) Maximum turn-ON peak current = 300 A (pulse width = 200 µs, duty cycle <1%)

   iv) Turn-ON resistance = 1.3 Ω
3. Once the switching frequency is greater than 10 kHz, a liquid cooling system is required to operate the BEHLKE switch
4. Without liquid cooling, the maximum continuous power dissipation (P_{cont}) of the BEHLKE switch is limited (e.g., for HTS-151-30, P_{cont} is 10 W without liquid cooling).
5. At higher switching frequency (>20 kHz), the BEHLKE switch requires multiple ancillary DC power supplies, i.e., 5, 15, and 60 V.

6. The switches made by BEHLKE cannot be reconfigured to withstand a higher voltage exceeding their recommended rating. BEHLKE offers separate products to operate them at higher voltage/currents.

Solution Proposed: Designing a modular high-voltage (~10 kV) switch using a single custom isolated gate driver for each module and having a construction cost lower than the BEHLKE sold switch with equivalent or better performance in all specification categories (Specifications for the BEHLKE switches can be found in the following link: http://www.behlke.com/separations/separation_c4.htm).

Relevance to OSPRES Grant Objective: The proposed modular high-voltage switch is expected to facilitate controlled hundreds-of-nanosecond charging of an array of transmission lines of pulse forming networks to drive an array of PCSSs, thereby producing controlled hundreds-of-picosecond scale high-voltage pulses.

Risks, Payoffs, and Challenges:

I. Lack of rigid control over voltage balancing can lead to a cascaded failure among the series-connected MOSFETs.

II. In the absence of an adequate mitigation scheme, voltage overshoot due to the fast switching speed can exceed the voltage rating of an individual MOSFET, thereby damaging the switch.

III. At high voltage (~10 kV) and high repetition rate (>100 kHz), mitigating EMI to safeguard the individual MOSFETs from false turn-ON is a major challenge.

4.1.2 Tasks / Timeline / Milestones

(A) (i) Design a surface-mount MOSFET-based four-stage switch (6.8 kV rated) and control it using the in-house gate driver / 5 weeks or 12 DEC

(ii) Test the voltage withstanding ability of the switch with a DC supply voltage up to 4–5 kV and evaluate the effectiveness of the thermal management at its current state / Dec 2020.

(B) Design a modular HV switch (~12 kV rated) using the concept of the tested four-stage high-voltage switch and the in-house gate driver / Jan–Feb 2021.

(C) Test the voltage withstanding ability of the modular HV switch with a DC supply voltage up to 10 kV and switching frequency up to 50 kHz using a resistive load (3–5 kΩ) and evaluate the effectiveness of the thermal management at its current state / Feb–Mar 2021.

(D) Test this modular HV switch coupled with Si PCSS up to a DC supply voltage of 5–6 kV and a switching frequency up to 50 kHz / Mar–April 2021.

4.1.3 Progress Made Since Last Report

(A) Design and fabrication of the four-stage HV switch using the in-house HV gate driver is completed. The switch has been tested up to a DC supply voltage of 4 kV and a

switching frequency up to 10 kHz using a 3.2 kΩ resistive load. The temperature of the balancing resistor went up to 100°C due to the loss caused by leakage current during the OFF period (t_{on}= 15 µs, t_{off} = 85 µs) of the HV switch.

(B) A six-stage modular HV switch composed of two modules where each module is made from three discrete MOSFETs (each 1.7 kV rated) and driven by the in-house HV gate driver is being simulated in LTSpice.

(C), (D) Testing will be accomplished after the fabrication of the modular HV switch.

4.1.4 Significant Finding(s) and Mission Impact

I. The 6.8 kV rated four-stage in-house HV switch has been tested up to a DC supply voltage of 4 kV at a switching frequency up to 10 kHz. We have obtained output voltage across the 3.2 kΩ resistive load up to a DC supply voltage of 4 kV as shown in Fig. 4.1.1(a). This implies the HV switch is properly functioning up to a DC supply voltage of 4 kV. A zoomed version of the output voltage is shown in Fig. 4.1.1(b).

II. The temperature of the balancing resistors connected across each MOSFET of the HV switch was recorded up to 100 °C for continuous operation up to 1 min. 6 W rated SMD resistors were used as the balancing resistors. A series-parallel combination of SMD resistors or through-hole resistors with attached heat sinks will be used as the balancing resistor for improved thermal management (< 60°C across the balancing resistors) of the HV switch.

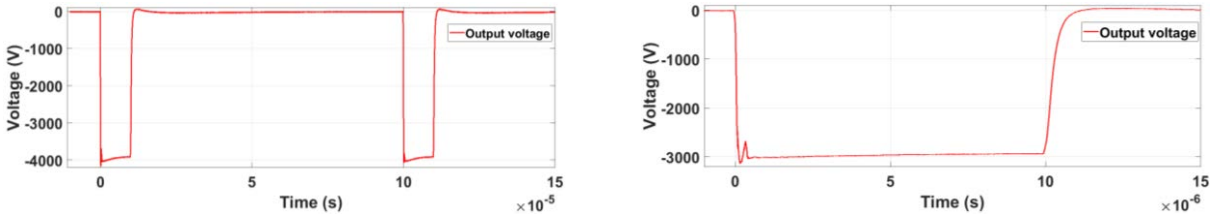


Fig. 4.1.1: Output voltage across a 3.2 kΩ load at (a) 4 kV and (b) 3 kV (zoomed).

5.0 Tradespace Analysis of Ultra-Wide-Band Antenna Arrays

5.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs).

5.1.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two dimensional shape, and relative placement (i.e., intra- and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, vivaldi, valentine, etc. are some of the commonly used ultra-wide-band antenna elements in a phased array for HPM transmissions.

Deficiency in SOTA: Large physical aperture size.

Solution Proposed: Using electrically small antennas (ESAs) as array elements to reduce physical aperture size; followed by optimization of the design in terms of both near-field (quality Factor → bandwidth) and far-field (directivity) parameters, simultaneously, via D/Q ratio.

Relevance to OSPRES Grant Objective: Tradespace analysis of ESAs is being performed by optimizing antennas (and arrays) in terms of directivity (or gain) and impedance bandwidth simultaneously, via D/Q technique.

5.1.2 Tasks / Timeline / Milestones

(A) Investigation into the effect of array aperture area reduction on different array parameters / Jan–Feb 2021 / ≈30% reduction in the radiating aperture area (# of elements reduced from 225 to 183) leads to just about 3 dB reduction in the array boresight gain without any scan-blindness from 0 to $\pm 60°$, over 640 - 990.6 MHz.

(B) Building minimum viable validation prototype on polyethylene and FR-4 substrates (with high power handling capabilities), to achieve better performance for HPM transmissions at UHF range / Jan–March 2021 / So far, 35% impedance bandwidth obtained from microstrip patch antennas modeled on polyethylene and FR-4 substrates in the UHF range.

(C) Time-domain analysis of the antennas subjected to input short pulses / May 2021 / Outputs from the fabricated prototypes (single element and embedded elements in the 3×3 array), subjected to short input pulses, have been obtained and are being analyzed.

5.1.3 Progress Made Since Last Report

(A) Investigations into Aperture Area Reduction:

a. The effect of reducing the number of array elements, in an array modeled on infinite ground plane, by increasing the inter-element spacing (d), on array gain, radiation pattern and steering capability has been studied.

b. Ongoing investigations into the reduced aperture area array on finite grounded substrates.

(B) Building minimum viable validation prototypes:

a. Simulation data shows: To achieve >30% 2:1 VSWR bandwidth with antennas modeled on FR-4/polyethylene substrates in the UHF region (0.6–1 GHz), simple rectangular microstrip patch antennas must be fed by thicker connectors than the commercially available ones (probe radius ≈ 0.65 mm).

b. While U-slot patches on FR-4 substrates were able to produce ≈20% 2:1 VSWR bandwidth (709–905 MHz) with the standard SMA connectors (probe radius ≈ 0.65 mm).

5.1.4 Significant Finding(s) and Mission Impact

Investigations into Reduction of Radiating Aperture Area of the Array:

The aperture area of a 15×15 array is reduced by ≈30% by changing the grid formation from a square to a hexagonal lattice. The number of elements in the reduced aperture area is varied by changing d. Degradation in the array gain and steering capability occurs

Table 5.1.1. Summary of the array geometries on infinite ground planes (λ calculated at 990.6 MHz)

Array #	Lattice Type	Radiating Aperture Area (m^2)	Inter-element spacing (d)	Total No. of Elements
15×15	Square	4.4377	0.485λ	225
183-Hex	Hexagonal	3.0994	0.485λ	183
139-Hex	Hexagonal	3.1252	0.56λ	139
114-Hex	Hexagonal	2.8536	0.6118λ	114
80-Hex	Hexagonal	2.9456	0.75λ	80

at the higher frequency end as *d* is increased to $\geq 0.6118\lambda$. This may be attributed to the appearance of grating lobes in the visible region – a common phenomenon observed when inter-element spacing is too large.

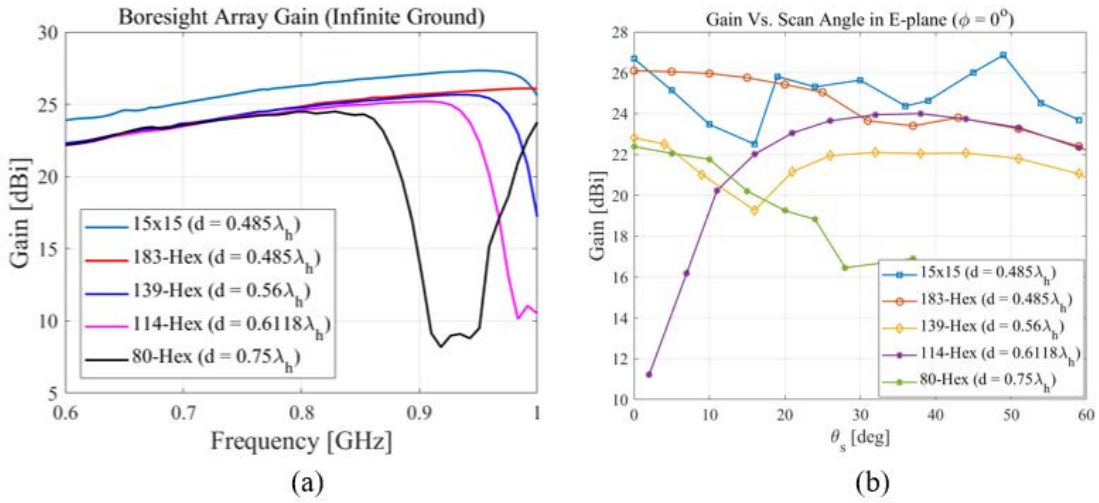


Fig. 5.1.1. (a) Gain vs. frequency and (b) Gain vs. steering angle at 990.6 MHz of the arrays simulated on infinite ground plane.

5.2 Tradespace Analysis of Other Ultra-Wide-Band (UWB) Single Elements

5.2.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: (i) Three new antenna elements (fractal, shark, and Koshelov) have been identified from the survey conducted last month for tradespace study and analysis to try and reduce physical aperture area. (ii) Electromagnetic (EM) techniques (such as side lobe reduction, electromagnetic band-gap ground plane, array configurations, sub-array overlapping etc.) have also been identified which can be incorporated into the antenna element design that could explicitly or implicitly help with physical aperture size reduction. The applicability of each EM technique depends on the antenna element under investigation. A few techniques can only be applied to arrays, whereas most techniques can be applied to single antenna elements, which can be arrayed later.

Sub-Problem: To be identified with respect to each antenna element.

State-of-the-art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered as the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains significantly large and has no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: (i) Explore the antenna design parameter space for the reported antenna elements (fractal, shark and Koshelov) using computational electromagnetic (EM) solvers starting with the simulation of single elements. (ii) Apply suitable EM techniques to each antenna element and evaluate/compare antenna performance with and without application of EM techniques.

Relevance to OSPRES Grant Objective: Satisfies the high-risk and high-payoff technology advancement criteria by exploring the parameter space of certain UWB antenna elements that are minimally explored for HPM applications. Provides educational merit with basic and improved understanding of each selected antenna element as well as understanding of minimally applied EM techniques to UWB antenna elements.

5.2.2 Tasks / Timeline / Milestones

(A) Initial design, simulation, and validation of fractal, shark, and Koshelov antennas (JAN21–FEB21). Perform a preliminary tradespace study on either all or the most important antenna design parameters corresponding to each antenna element. Analyze and identify the antenna design parameters which lead to significant variation in antenna metrics (such as bandwidth, gain, steering angle, peak and average power handling, and physical aperture area). Several other antenna metrics have also been identified from the survey and can be included in the reports for tradespace analysis.

(B) Perform detailed tradespace studies for the three antennas using the pre-identified tradespace antenna design parameters with a goal towards reducing aperture size (MAR21–APR21). The antenna elements will be computationally studied and compared against the BAVA design for a subset of important antenna metrics.

(C) Understand and apply suitable EM techniques to each of the three antenna elements with a goal towards reducing aperture size (JAN21–APR21). Compare antenna metrics of antenna elements (fractal, shark, and Koshelov) before and after application of EM techniques as well as to the SOTA BAVA design.

5.2.3 Progress Made Since Last Report

(A) Carried out a detailed survey (literature search) to compile all antenna elements that satisfy UWB requirements and OSPRES grant objectives.

(B) Down-selected to 3 antenna elements (fractal, shark, and Koshelov) that met the selection criteria mentioned above. The three antenna elements are shown in Fig. 5.2.1. The fractal antenna shown in the top left of Fig. 5.2.1 is one of many possible fractal shapes and does not imply that this fractal shape has been selected for tradespace study. The final fractal shape will be updated in the next MSR. The top right image in Fig. 5.2.1

shows the shark antenna, which has two truncated cones facing each other with a connection to a back plate. Finally, the bottom center image in Fig. 5.2.1 shows the Koshelov antenna, which is a combination of a case (2), electric monopole (1), magnetic dipoles (5,7) and TEM horn (6), and an adjusting plate (4).

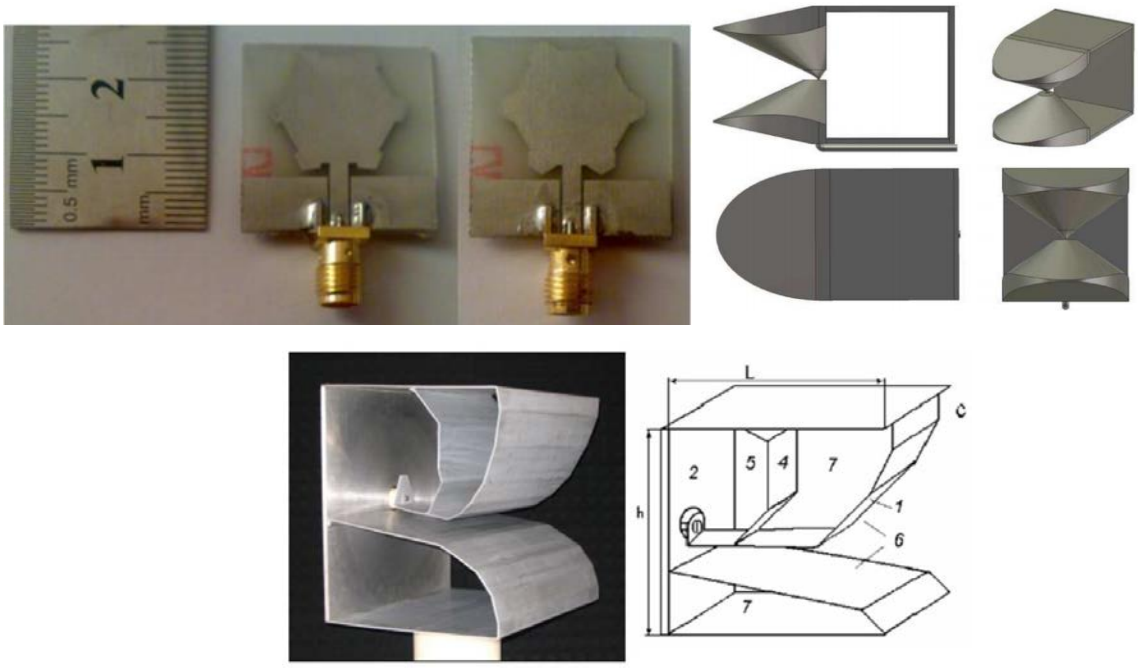


Figure 5.2.1. (Top Left) Fractal antenna; (Top Right) Shark antenna; (Bottom Center) Koshelov antenna.

(C) EM techniques have been identified via survey that can help with physical aperture area reduction.

5.2.4 Significant Finding(s) and Mission Impact

No significant findings yet related to tradespace studies of three antenna elements.

6.0 RF Coupling

6.1 Enclosure Effects on RF Coupling

6.1.1. Problem Statement, Approach, and Context

Primary Problem: Slots and gaps are introduced in casings/enclosures due to a variety of practical reasons which might compromise their shielding, creating upset susceptibility to the enclosed electronics. The goal of this work is to quantify how the thresholds for upset susceptibility of enclosed wires and integrated circuits differ from those in free space.

Solution Space: Study enclosures with different shapes, material compositions, and slots to quantify their effect on RF coupling to the enclosed wires and electronics typically used in UAVs. The study will focus on the low-frequency range where the incident wavelength is comparable to the size of the enclosure or larger.

Sub-Problem: UAVs are manufactured with a wide variety of shapes and composites to accomplish an exponentially expanding list of missions. The configurations previously reported in the literature have simplistic assumptions regarding the shape and material composition of UAV enclosures that might overestimate or underestimate susceptibility.

State-of-the-Art (SOTA): Simple statistical analysis of specific enclosure configurations using either brute force simulations/measurements or pure statistical methods.

Deficiency in the SOTA: Brute force simulations/measurements of the voltages and currents induced in wires and integrated circuits contained in enclosures is computationally or experimentally complex and have several limitations. The computations are complicated by the multiscale nature of the simulations, and the experiments are complicated by the cost of the equipment and the extensive time needed to measure every variation to cover all possible scenarios. Statistical methods, such as the Random Coupling Model (RCM) for example [1], are only accurate for high frequencies where the wavelength is much smaller than the size of the enclosure. Another main deficiency of RCM is that it can't predict the exact induced voltages and currents for a specific well-characterized system but it only provides the statistical properties of these induced currents and voltages.

Solution Proposed: Apply Characteristic Mode Analysis (CMA) to identify the fundamental modes of the enclosure, current distribution, and the field pattern of each mode. This will allow us to predict the worst-case RF coupling scenarios without the need of lengthy simulations and/or expensive experimental measurements. The proposed approach can predict measurements at a fraction of the cost/time.

Relevance to OSPRES Grant Objective: Provide general guidelines on how the environment, in this case the enclosure, affects RF coupling and subsequent electromagnetic absorption to UAV wires and integrated circuits.

Risks, Payoffs, and Challenges: The modes depend mainly on the shape and material of the enclosure. Since UAVs have a wide variety of shapes and material compositions, a library of several UAVs needs to be studied before quantitative general conclusions can

be drawn. Challenges can be mitigated by the use of the classification techniques of Machine Learning (ML). That is, different ML techniques will be evoked to detect hidden patterns on how the shape, material composition, and the shape/size location of slots correlate with the field enhancement inside the enclosure.

6.1.2. Tasks / Timeline / Milestones

Task	Timeline	Milestone
A. Complete the CMA implementation for studying the shielding effectiveness of metallic enclosures. Validate CMA can predict the worst-case shielding effectiveness of metallic enclosures as a function of their shapes.	2 months 11/15/2020-1/15/2021	A fast full-wave tool that facilitates studying the effect of a metallic enclosure on shielding effectiveness (1 IEEE AWPL Paper)
B. Use CMA tool in (A) to predict the worst case internal field magnitude of metallic and dielectric enclosures of ten COTS UAVs as a function of HPM waveform	4 months 1/15/2021-5/15/2021	A database of worst-case internal fields shielding effectiveness results of the ten COTS UAVs as a function of their shape and HPM waveforms.
C. Use the database in (B) to train a Machine Learning (ML) platform to predict RF coupling to enclosed wires and electronics	5 months 5/15/2021-10/15/2021	Perform blind tests to estimate the induced internal fields of 2 COTS UAVs, not used in the training of the ML platform, and compare them with the measurement.

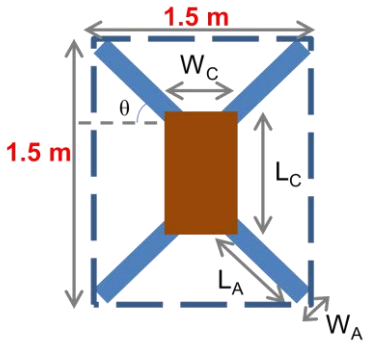


Fig.6.1. Sketch illustrating the parameter space for the UAV analysis.

6.1.3. Progress Made Since Last Report

(A) We have decided to study quadcopters extensively as our DUT for the Machine Learning training setup as it fits the requirements of the project. Therefore, we have prepared a parameter space for our analysis. Fig. 6.1 shows the UAV model that summarizes our parametric space.

(B) To accomplish (a), we have been working on setting up an account on LEWIS, the primary supercomputer for the University of Missouri System, to run in parallel the hundreds of simulations needed to span the parameter space. This task is completed and we upgraded the FEKO license in LEWIS to the most recent version to achieve the best performance.

(C) Before submitting hundreds of computational experiments to the LEWIS supercomputer, we wanted to independently test the accuracy of the FEKO results. Therefore, we re-simulated one UAV configuration on CST Microwave Studio and the results showed excellent agreement with FEKO validating our approach.

6.1.4. Significant Finding(s) and Mission Impact

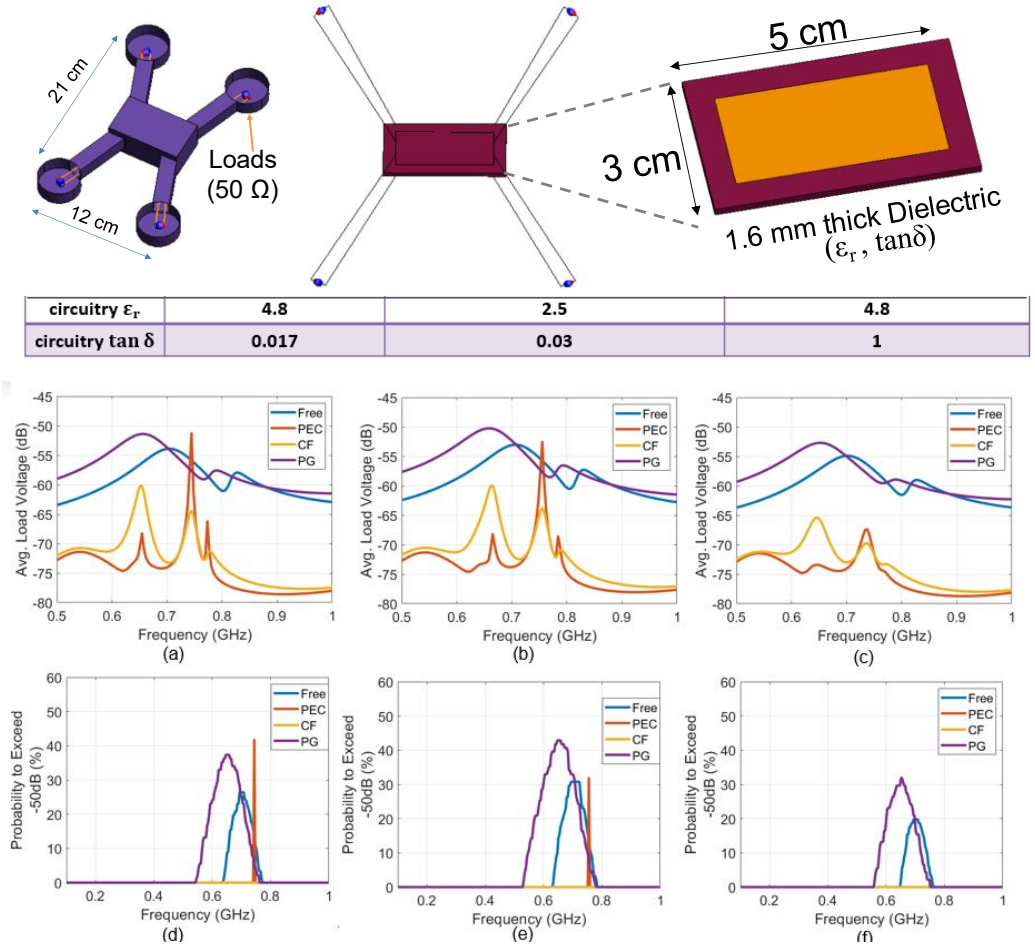
(A) In the last report, we showed that perforated Perfect Electric Conducting (PEC) and Carbon fiber (CF) UAV frames shield the enclosed electronics at most frequencies but can lead to resonance frequencies where the internal fields are amplified. That is, metallic frames shield the enclosed wires and electronics at most frequencies by more than 20 dB in comparison to free-space. On the other hand, at the resonance frequencies, the frame acts as a cavity that amplifies the coupling by ~ 5-10 dB over a narrow bandwidth.

In this report, we investigate how this amplification depends on the losses of the enclosed circuitry. Fig. 6.2 shows a model of the enclosed circuitry which is composed of 4 loads, 4 wires, and a central PCB. The loss tangent, tanδ, of the PCB's dielectric substrate was varied as shown in the Table in Fig. 6.2 increasing from left to right. As the loss of the circuitry increases, Fig. 6.2a to Fig. 6.2c show that the amplifying nature of the PEC frame deteriorates at the resonance frequency of 0.76 GHz. The increase in the losses decrease the quality factor of the resonance causing the peak value of the coupled voltage to decrease. Even for a nonmetallic plexiglass (PG) frame, Fig. 6.2a to Fig. 6.2c show that the coupled voltage decreases slightly with the increase in the loss tangent of the PCB's substrate.

We calculated the probability of the voltage coupled to one of the 4 loads in Fig. 6 to exceed a threshold of -50 dB. The results are shown in Fig. 6.2d, Fig. 6.2e, and Fig. 6.2f, for the 3 loss values considered in the Table. The probability for the metallic PEC frame depends significantly on the loss of the enclosed circuitry. For the PEC frame, the maximum probability is ~45% when the loss tangent is 0.017 but it drops to 0% when the loss tangent increases to unity. However, the probability of the dielectric PG frame is less sensitive to the losses decreasing from a maximum of 40% to 30% as the loss tangent is increased from 0.017 in Fig. 6.2d to 1 in Fig. 6.2f.

(B) The results in Fig. 6 show the importance of accounting for losses in the enclosed circuitry when studying the shielding effectiveness of different UAV

frames/enclosures. Also, the results in Fig. 6.2 show that the optimum coupling can be achieved using a PEC or a CF frame whilst ensuring that the losses of the enclosed electronic circuitry exceed a certain threshold. The PEC or CF frame shield the enclosed electronics at a wide range of frequencies whereas the losses will prevent the emergence of cavity resonances. In future reports, we will show how these conclusions can be incorporated in Engagement Level Simulations.



circuitry ε_r	4.8	2.5	4.8
circuitry $\tan\delta$	0.017	0.03	1

Fig. 6.2. Model of enclosed circuitry showing the wires, loads, and PCB. The table shows the dielectric properties used for the PCB substrate. (a), (b), (c): Average voltage across one load of the simple circuitry model inside a UAV enclosure (d), (e), and (f) The probability of the load voltage exceeding an arbitrary threshold of -50 dB.

References:

[1] Bisrat Addissie, John Rodgers, Thomas Antonsen, "Extraction of the coupling impedance in overmoded cavities," Wave Motion, Volume 87, Pages 123-131, 2019.

7.0 Thermal Management

7.1 Jet Impingement Optimization

7.1.1 Problem Statement, Approach, and Context

Primary Problem: Traditional, laminar-flow-based cooling technologies are limited in their ability to compensate average-power dissipation >1 kW (i.e., >1 GW/m^3 as cooling density) – specifically, the thermal load byproduct – of HPM-based sources within electronically-steered arrays.

Solution Space: Utilize novel cooling technologies which employ non-laminar flow regimes (i.e., jet impingement thermal management system, JI-TMS).

Sub-Problem: An order-of-magnitude greater fluid flowrate and two orders greater pressure drop is required over traditional techniques (10 gpm vs. 1 gpm, and 100's-of-psi vs. 1's-of-psi) without increasing SWaP-cost.

State-of-the-Art (SOTA): High-power electronics employing JI-TMS's have achieved 10's-of-kW of average power handling capabilities using 20 °C dielectric coolant and sub-mm jet diameters while consuming equivalent power to deliver the fluid to the JI-TMS.

Deficiency in the SOTA: Chiller/pump systems consumption of power to produce thermal compensation, extreme pressures (100's-of-psi) to achieve optimal flowrate performance and cooling metrics, low SWaP-C[2] fidelity for Navy afloat missions.

Solution Proposed: Develop a JI-TMS able to compensate average-power dissipation >1 kW while maintaining the HPM-sources' solid-state heat source <80 °C, by flowing dielectric fluid at turbulence-inducing flow rates while not exceeding 100's-of-psi within the system.

Relevance to OSPRES Grant Objective: Increased cooling performance facilitates HPM sources' higher average-power operation (>1 kW) deeming specific-power-densities (>1 W/cm^2) at distances >2 km achievable.

Risks, Payoffs, and Challenges: High pressures and larger chiller-pump systems, minimizing pressure drop requirements while maintaining or improving performance increases cooling form-factor (>1 GW/m^3), 5× that of traditional cooling techniques.

7.1.2 Tasks / Timeline / Milestones

(A) Initial design of JI-TMS-V1 proposed and simulated using Si-PCSS source's laminar-flow TMS as baseline / 1-year, 4-months or MAY18–OCT19 / initial design–simulation phase completed.

(B) Revised JI-TMS-V1's design (JI-TMS-V2), simulation of parametric study performed, prototype developed and experimentally evaluated / 2-months or DEC19 / establishing design's baseline accomplished.

(C) Design changes applied to JI-TMS-V2 to decrease flowrate and pressure drop requirement / 9-months or SEP20 / design optimization phase completed.

(D) Complete redesign (JI-TMS-V3) of system to increase average-power handling capabilities (>1 kW) by increasing flowrate and convective heat transfer (>40 kW/m·K) without increasing system's volume (~100 cm^3) / 4-months or DEC20 / design phase-II complete.

(E) Finalize remaining numerical analysis tradespace study of current JI-TMS design and compile research into academic research journal article for submission / 2-months or DEC20 / Downselect JI-TMS as viable option for thermal mitigation phase in-progress.

7.1.3 Progress Made Since Last Report

(E) Efforts focused on writing journal article for peer review and publication of work performed (see Section 8.5 for details).

7.1.4 Significant Finding(s) and Mission Impact

The JI-TMS design's ability to compensate 0.2 kW (i.e., >200 MW/m^3) average power and maintain the Si-PCSS source's average temperature at 50 °C is 10 °C less than the laminar-flow-based design of equivalent volumetric form-factor (cross-flow thermal management system) – currently used for the OSPRES Contract's source array demonstrator.

8.0 Program Management

8.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

8.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

8.3 Major Procurement Actions

i. Microsoft Office 365 GCC High (75 seats) - $45,000 (for OSPRES Contract CUI Compliance)

8.4 Travel

Destination	Purpose	Attendees	Estimated Costs

8.5 Pending or Upcoming Public Release Requests

i. J. N. Berg, R. C. Allen, and S. Sobhansarbandi, CFD Modeling and Experimental Implementation of a Novel Thermal Management System for a Semiconductor Device [Unpublished manuscript], Int J Heat Mass Transf, pp. 1-12, 2021.

9.0 Appendix A – Academic and IP Output

(Please note that this section is still being updated).

9.1 Conference Publications

[1] W. Azad, S. Roy, and F. Khan, "A Single Gate Driver-based Four-stage High-voltage SiC Switch Having Dynamic Voltage Balancing Capability," submitted in *2021 IEEE Applied Power Electronics Conference and Exposition* (APEC), Phoenix, AZ, USA, June 9-12, 2021.

[2] J. Hunter, S. Xia, A. Harmon, A. M. Hassan, V. Khilkevich, and D. Beetner, "Modeling and Statistical Characterization of Electromagnetic Coupling to Electronic Devices," *IEEE International Symposium on Antennas and Propagation and NSRM USNC-URSI National Radio Science Meeting*, Boulder, CO, January 4-9, 2021.

[3] W. Azad, S. Roy, and F. Khan, "A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver," accepted in *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, 2020.

[4] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, "Scalable Characteristic Mode Analysis: Requirements and Challenges (White Paper)," *Large Scale Networking (LSN) Workshop on Huge Data: A Computing, Networking and Distributed Systems Perspective Sponsored by NSF*, Chicago, IL, April 13-14, 2020.

[5] M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Predicting Electromagnetic Interference to a Terminated Wire Using Characteristic Mode Analysis," *Proceedings of the Annual Review of Progress in Applied Computational Electromagnetics (ACES)*, Monterey, CA, March 22-26, 2020.

[6] W. Azad, F. Khan, and A. Caruso, "Self-sustaining High-power RF Signal Generation Using LDMOS Based Power Amplifier and Nonlinear Transmission Line," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 3567-3572 [doi].

[7] A. Hanif, W. Azad, and F. Khan, "Detection of Bond Wire Lift Off in IGBT Power Modules Using Ultrasound Resonators," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 345-350 [doi].

[8] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, "Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS," *Annual Directed Energy Science and Technology Symposium*, March 2020 (abstract appeared, but talk cancelled due to pandemic).

[9] B. Barman, J. Kovarik, D. Chatterjee, and A. N. Caruso, "Some Investigations into Mutual Coupling Analysis for Trade Space Studies of Linear Arrays," *Proceedings of the IEEE International Phased Array Systems and Technology Symposium*, Boston, Mass., October 2019.

[10] M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of the Effect of the UAV Frame Material on Coupling and Interference," *IEEE International*

Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages), Georgia, USA, July 7-12, 2019.

[11] M. Hamdalla, J. Hunter, Y. Liu, V. Khilkevich, D. Beetner, A. Caruso, and A. M. Hassan, "Electromagnetic Interference of Unmanned Aerial Vehicles: A Characteristic Mode Analysis Approach," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019.

[12] B. Barman, D. Chatterjee, and A. N. Caruso, "Analytical Models for L-Probe fed Microstrip Antennas," *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

[13] K. C. Durbhakula, J. Lancaster, J. Hunter, Y. Liu, D. Beetner, V. Khilkevich, D. Chatterjee, A. N. Caruso, and A. M. Hassan, "Electromagnetic Coupling Analysis of Printed Circuit Board Traces using Characteristic Mode Analysis," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (2 pages)*, Atlanta, Georgia, USA, July 7-12 2019.

[14] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "On the Location of Transverse Electric Surface Wave Poles for Electrically Thick Substrates," Proceedings of the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019.

[15] M. Hamdalla, B. Bissen, A. N. Caruso, and A. M. Hassan, "Experimental Validations of Characteristic Mode Analysis Predictions Using GTEM Measurements," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Montréal, *Québec, Canada, July 5-10, 2020*.

[16] W. Azad and F. Khan, "Sustaining High-power RF Signal Generation in a Positive Feedback Network," *2019 IEEE Pulsed Power and Plasma Science Conference (PPPS)*, Orlando, FL, USA, June 23-28 2019.

[17] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, "Scalable characteristic mode analysis using big data techniques," *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[18] M. Hamdalla, W. Al-Shaikhli, J. Lancaster, J. D. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of Electromagnetic Coupling to Wires with Realistic Shapes," *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[19] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "Location of Surface Wave Poles in Sommerfeld Integrals: A Mittag-Leffler Expansion Approach," *Proceedings of the URSI-B International Symposium on Electromagnetic Theory*, URSI Commission, San Diego, USA, May 2019.

[20] D. Chatterjee, B. Barman. J. Kovarik, and A. N. Caruso, "Studies on Antenna Characterization and Propagation of High Power Pulsed Electromagnetic Waves with Minimal Spatial Dispersion," presented at the *Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium*, Destin, Florida, USA, April 2019.

[21] J. Kovarik, B. Barman, D. Chatterjee and A. N. Caruso, “Some Investigations into Applications of Electrically Small Antennas as Phased Array Elements,” presented at the *Directed Energy Professional Society* (DEPS) *Annual Science and Technology Symposium*, Destin, Florida, USA, April 2019.

[22] K. C. Durbhakula, D. Chatterjee and A. M. Hassan, “Analytical Evaluation of Sommerfeld Integral Tails Present in Two-layered Media Green’s Functions,” *Proceedings of the Indian Conference on Antennas and Propagation* (InCAP), Hyderabad, India, December 2018.

[23] D. Beetner, V. Khilkevich, A. M. Hassan, J. Hunter, Y. Liu, and D. Floyd, “Characterization of the Electromagnetic Coupling to UAVs,” *DE Systems Symposium*, September 24-27, 2018

[24] C. Hartshorn, K. Durbhakula, D. Welty, D. Chatterjee, J. Lancaster, A. M. Hassan, and A. N. Caruso, “Crosstalk and Coupling to Printed Circuit Board Metallic Traces with Arbitrary Shapes,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[25] M. Hamdalla, J. Roacho-Valles, J. Hunter, D. Beetner, A. M. Hassan, and A. N. Caruso, “Electromagnetic Analysis of Unmanned Aerial Vehicles Using Characteristic Mode Analysis,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[26] C. Hartshorn, M. Hamdalla, J. Lancaster, A. M. Hassan, and A. N. Caruso, “Electromagnetic Vulnerability of Wires with Arbitrary Shape,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[27] K. C. Durbhakula, D. Chatterjee, A. M. Hassan, and M. S. Kluskens, “Studies on Numerical Evaluation of Sommerfeld Integrals for Multilayer Topologies,” *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018.

[28] J. Lancaster, D. Chatterjee, and A. N. Caruso, “Some Investigations into the Dispersion Characteristics of Localized Bessel Beams,” published in the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018 (1 page URSI Abstract).

[29] M. Hamdalla, A. M. Hassan, and A. N. Caruso “Characteristic Mode Analysis of Unmanned Aerial Vehicles with Realistic Shapes and Material Composition,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Boston, MA, July 8-13, 2018.

[30] W. Azad, S. Roy, A. S. Imtiaz, and F. Khan, "Microelectromechanical System (MEMS) Resonator: A New Element in Power Converter Circuits Featuring Reduced EMI," *2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, Niigata, May 20-24, 2018, pp. 2416-2420 [doi].

[31] J. Hunter, Y. Liu, D. Floyd, A. Hassan, V. Khilkevich, and D. Beetner, “Characterization of the Electromagnetic Coupling to UAVs,” Annual Directed Energy Science and Technology Symposium, Feb 26-March 2, 2018.

9.2 Journal Publications

9.2.1 In Preparation

[1] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, CFD Modeling and Experimental Implementation of a Novel Thermal Management System for a Semiconductor Device, *Int J. Heat Mass Transf*, pp. 1-12, In Preparation, **2021**.

[2] W. Azad, F. Khan, and A. N. Caruso, "A Series-connected High-voltage SiC Switch Driven by a Compact High-voltage Isolated Gate Driver," In preparation, **2021.**

[3] M. Z. M. Hamdalla, B. Bissen, J. D. Hunter , L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Experimental Evaluation of CMA Predictions and Control of Electromagnetic Interference to UAVs," In Preparation, **2021**.

[4] S. Xia, J. Hunter, A. Harmon, M. Hamdalla, A. Hassan, V. Khilkevich, D. Beetner, "Simulation Driven Statistical Analysis of the Electro-magnetic Coupling to Microstriplines," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[5] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, "Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field Coupling to Randomly Shaped Wires," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[6] W. Azad, F. Khan, and A. N. Caruso, "A Medium Power, Self-Sustaining, Configurable RF Pulse Generation Circuit Using a Nonlinear Transmission Line and Power Amplifier in a Closed Loop Configuration, In Preparation, **2020**.

9.2.2 Submitted / Under Revision

[7] Khulud Alsultan, Mohamed Hamdalla, Sumitra Dey, A. N. Caruso, Praveen Rao, and A. M. Hassan, "Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform," *IEEE Open Journal of Antennas and Propagation,* Submitted, **2020**.

[8] John Keerthi Paul Bhamidipati, Eliot R. Myers, Adam M. Conway, Lars F. Voss, and Anthony N. Caruso, "Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches," *IEEE Transactions on Electronic Devices*, Under Revision, **2020**.

[9] W. Azad, F. Khan, and A. Caruso, "A Medium Power, Self-sustaining, Configurable RF Pulse Generation Circuit Using Nonlinear Transmission Line and a Power Amplifier in Closed Loop Configuration," *IEEE Transaction on Plasma Science*, Submitted, **2020**.

[10] S. Roy, W. Azad, S. Baidya and F. Khan, "A Comprehensive Review on Rectifiers, Linear Regulators and Switched-mode Power Processing Techniques used for Powering Biomedical Sensors and Implants inside Human Body," *IEEE Transactions on Power Electronics*, Submitted, **2020**.

[11] S. Roy, W. Azad, S. Baidya, M. Alam and F. Khan, “Powering Solutions for Biomedical Sensors and Implants inside Human Body–A Comprehensive Review on Energy Harvesting Units, Energy Storage, and Power Transfer Circuits,” *IEEE Transactions on Power Electronics*, Submitted, **2020**.

9.2.2 Published / In Press

[12] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems,” *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364-373, **2019**.

9.3 External Presentations/Briefings

DEPS Posters and Presentations 2020

[1] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[2] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

GOMAC 2019

[3] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[4] Eliot Myers, Picosecond High Power Switching Technologies

[5] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

DEPS Posters and Presentations 2019

[6] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[7] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[8] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[9] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[10] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[11] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[12] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[13] Deb Chatterjee, Studies On Antenna Characterization And Propogation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

DEPS Posters and Presentations 2018

[14] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[15] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[16] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

DEPS Posters and Presentations 2017

[17] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

9.4 IP Disclosures Filed

Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, 19UMK005, 28SEPT2018

Doynov, “Pulse Differential High-power Microwave Generation”, 19UMK007, 02JAN2019.

Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal”, 19UMK008, 28DEC2018.

Doynov, Caruso, “High-efficiency High-power Microwave Generation using Multipass Non-linear Network Topologies”, 19UMK017, 29AUG2020.

Doynov, “Scalable Modular System for High-power Microwaves Generation”, 20UMK010, 19APR2020.

Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna”, 20UMK011, 19APR2020.

Shepard, “A Novel Optical Fiber Amplifier”, 20UMK012, 02JUN2020.

Shepard, “A Low Noise Optical Amplifier”, 21UMK007, 14SEPT2020.

9.5 Provisional Patents Filed

Doynov, Caruso, “High-efficiency High-power Microwave Generation using Multipass Non-linear Network Topologies”, filed 26NOV2019.

9.6 Non-Provisional Patents Filed

None to date

ONR HPM Program - Monthly Status Report (MSR) – JAN 2021

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 FEB 2021

Distribution Statement ~A: Distribution authorized to all OSPRES Grant and Contract performers, and any OSPRES uncompensated collaborators. Further dissemination per the Office of Naval Research, Ryan Hoffman (ryan.hoffman@navy.mil, 703-696-3873) or higher DoD Authority.

OSPRES Grant Goal: address and transition technologies and capabilities that enable the OSPRES Grant Objective using the OSPRES Grant Approach, while educating the next generation of pulsed power and defense minded, stewards and innovators.

OSPRES Grant Objective: to execute high-risk, high-payoff efforts that mitigate, fill or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable and electronically steerable high power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average power space, and includes the kill chain considerations including the target and its responsivity to radiofrequency stimuli.

OSPRES Metrics of Success: developed technologies and capabilities that are published in the peer review, protected as intellectual property, and/or, transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use, as enabling/integratable capability(ies).

OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

OSPRES Grant Security: All efforts should be fundamental and publically releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

1.0 Contents

2.0 Executive Summary 3
2.1 Progress, Significant Findings, and Impact 3
2.2 Completed, Ongoing, and Cancelled Sub-Efforts 4
2.3 Running Total of Academic and IP Program Output 5
3.0 Switch Evaluation and Innovation 6
3.1 Si-PCSS Top Contact Modeling and Optimization for Cooling Requirements 6
3.2 Lasers and Optics 10
3.3 Si-, SiC- and GaN Modeling and Evaluation 11
3.4 Multi-Stage Optical Amplifier 13
3.5 GaN:C PCSS Direct RF Modulation 14
3.6 Bistable Operation of GaN 16
3.7 Diode-Based NLTLs 19
4.0 Prime Power and Conditioning 24
4.1 HV Switch Pulsed Chargers 24
5.0 Tradespace Analysis of Ultra-Wide-Band Antenna Arrays 28
5.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs) 28
5.2 Tradespace Analysis of Other Ultra-Wide-Band (UWB) Single Elements 30
5.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna 34
5.4 Tradespace Analysis of Ultra-Wide-Band (UWB) Fractal Antenna 38
6.0 RF Coupling 43
6.1 Enclosure Effects on RF Coupling 43
7.0 Thermal Management 47
7.1 Jet Impingement Optimization 47
7.2 Nanofluid Heat Transfer Fluid Development 48
8.0 Program Management 51
8.1 Issues 51
8.2 Interactions with Others 51
8.3 Major Procurement Actions 51
8.4 Travel 51
8.5 Pending or Upcoming Public Release Requests 51
9.0 Appendix A – Academic and IP Output 52
9.1 Conference Publications 52
9.2 Journal Publications 55
9.3 External Presentations/Briefings 56
9.4 IP Disclosures Filed 57
9.5 Provisional Patents Filed 57
9.6 Non-Provisional Patents Filed 58

2.0 Executive Summary

2.1 Progress, Significant Findings, and Impact

A method to enable low energy bistable ultrafast switching of carbon compensated gallium nitride (GaN:C) by photostimulation is proposed. Realizing such a breakthrough would yield the best of both: (a) low laser requirements for long pulse lengths; (b) the thermal/electrical/electronic/mechanical benefits of using GaN:C as a high power opening switch.

Higher voltage D-NLTL measurements showed the network successfully increased the peak amplitude from 8.7-kV to 9.1-kV, reduced the rise time from 1.36-ns to 560-ps, and hit a peak power of 1.66-MW. The reduction in rise time gives a maximum frequency of 1.78-GHz. Both values are encouraging as they show the line is capable of shifting energy to the GHz frequency range at single MW peak power.

The HV switched pulse charger group has a high fidelity simulation and design for a 6.8 kV output with 50V difference across four 1700-V Cree MOSFETs, with a rise time of 18-ns. Scaling this design to 10x the voltage is within reach.

The Jet Impingement – Thermal Management System has been a magnanimous effort; however, the fundamental limits to this technology have been exposed and it has been decided to sunset this sub-project. A summary will be produced in the appendix of the 15MAR report.

The nanofluid development effort, toward an enhanced thermal transfer media, is reported for the first time (section 7.2). Development of nanofluids has the potential to be game changing (two-orders greater), but the pragmatic considerations of finding the right ratio and type of nanoparticle/nanofluid to base fluid mixture while minimizing the viscosity for the specific embodiment (channels) requires a focused effort. Given the other major fundamental challenges that face the OSPRES program and resources available, we are evaluating whether to continue this work beyond JUL2021.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

	Start	End
2.2.1 Ongoing Sub-Efforts		
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
Heat Transfer by Jet Impingement	MAY 2018	Present
X-PCSS Comparison (X=Si, SiC, GaN)	NOV 2018	Present
HV Switch Pulsed Chargers	DEC 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Nanofluid Heat Transfer Fluid	NOV 2020	Present
2.2.2 Completed Sub-Efforts		
Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
2.2.3 Cancelled Sub-Efforts		
Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020

2.3 Running Total of Academic and IP Program Output

See Appendix A for authors, titles and inventors (note: this list is still being updated)

2.3.1	*Conference Publications*	34
2.3.2	*Journal Publications*	1 (5 submitted/under revision)
2.3.3	*External Presentations/Briefings*	18
2.3.4	*IP Disclosures Filed*	8
2.3.5	*Provisional Patents Filed*	1
2.3.6	*Non-Provisional Patents Filed*	0

3.0 Switch Evaluation and Innovation

3.1 Si-PCSS Top Contact Modeling and Optimization for Cooling Requirements

(Jay Eifler)

3.1.1 Problem Statement, Approach, and Context

Primary Problem: High-average-power 1064-nm picosecond class lasers are too large (1100 cm^3/W) and monetarily expensive ($1000/μJ*pulse) for the Navy afloat missions. By altering only Si-PCSS device parameters, one can enable both a laser size and cost reduction.

Solution Space: To reduce the size and cost of the laser, the laser energy required by the Si-PCSS is reduced by altering the Si-PCSS top contact laser windowing spacing. In addition, for each spacing, the required cooling and device temperature are compared and optimized to the laser energy reduction.

Sub-Problem: Using laser windowing spacings that require less laser energy to produce a given Si-PCSS on-state resistance, determine to what extent these spacings require more cooling due to device temperature and select the optimal spacing for laser energy reduction and cooling required.

***Sub-Problem 2*:** By altering only the peak doping concentration of the Si-PCSS anode side (p-side), maximize the voltage holdoff while minimizing on-state resistance while satisfying ohmic contact requirements. However, this optimization must also eventually consider the laser energy reduction and cooling required.

State-of-the-Art (SOTA): Si-PCSS top contact pattern designs are not known to have been published in detail. In-house patterns have used only an outer ring for the contact (resulting in high on-state resistance) and were improved by metallizing across the ring with filaments (to reduce current density high-points), similar to solar cell top contact designs. The Si-PCSS laser windowing spacings used were 10- and 20-μm, with 20-μm achieving sufficiently low sub-ohm on-state resistance using in-house laser energy of ~100-μJ delivered to the Si-PCSS.

Deficiency in the SOTA: There is no justification for 20-μm spacing being optimal for producing low sub-ohm on-state resistance with the least required laser energy and cooling (also dependent upon laser and cooling system capabilities).

Solution Proposed: Optimize OSPRES Si-PCSS top contact patterns using TCAD to meet required cooling (maintain <80°C device temperature, including hotspots) and reduce laser energy over a range of possible on-state resistances. Also include correctly modeling device dimensions, internal electric field, thermal hotspots, on-state resistance, doping profile and anti-reflective coating used in the Si-PCSS.

Relevance to OSPRES Grant Objective: Optimized top contact patterns require less laser energy and cooling which enhances $SWaP\text{-}C^2$ for the laser system needed to drive the Si-PCSS and maintain device operation lifetime in excess of $2x10^8$ shots/lifetime at medium power.

Risks, Payoffs, and Challenges: The top contact design does not have the most direct impact on laser system size and cost. A smaller, more effective laser is needed. However, the metallization for optimized top contacts is inexpensive and easy to manufacture. The TCAD models have various limitations: full device size too large, only single-pass laser absorption, limited external thermal bodies and heat flow mechanisms, cannot transiently charge transmission line, and only single to few pulses feasible for Si-PCSS.

3.1.2 Tasks and Milestones / Timeline / Status

(A) RDT will fabricate 2 wafers of variable window Si-PCSS. (20, 40, 60, 100, 200, 350 um) spacings for 1 cm devices, with 6 of each on 1 wafer, will be made. And 60 um and 350 um for 7 cm devices, with 5 of each, will be made on another wafer. Milestone achieved for fabricating and receiving variable window Si-PCSS. / FEB 2021 / Devices delivered to UMKC FEB 4, 2021.

(B) Perform TCAD studies to optimize laser windowing spacing using heat removed from the Si-PCSS with the addition of temperature hotspots. The studies will quantify the tradeoff between reduced laser energy for on-state resistance vs reduced cooling. Additional development of the thermal models will include carrier recombination-generation heating, external thermal bodies, and improve computational efficiency (to enable studies over a range of laser energies). Milestone in determining spacing vs heat removed and device temperature. / First thermal TCAD simulations performed on DEC 4, 2020. Initial thermal spacing study finished JAN 30, 2020. / On-going status (no timeline set yet for continued work).

(C) Perform TCAD studies to determine relationship between peak p-doping concentration (anode side) and device performance (on-state resistance, voltage holdoff and ohmic contact requirements). An optimal p-doping concentration can then be determined. To be consistent with earlier top contact spacings used for reduced laser energy and/or reduced cooling, models include doping dependent free-carrier absorption photogeneration and thermal modeling. / First TCAD simulation performed NOV 11, 2020. Last TCAD simulations finished JAN 30, 2020. / On-going status (no timeline set yet for continued work).

3.1.3 Progress Made Since Last Report

(A) The fabrication of the variable window Si-PCSS were completed by creating an anti-reflective coating, beveling, etching, passivating, and I-V testing the devices, and they were delivered to UMKC for further testing and analysis. 7-cm devices were destroyed during beveling.

(B) Thermal TCAD simulations for cooling required vs top contact spacing (20, 40, 60, 100, 200, 350-μm) have been completed. 100- and 350-μm had been completed in the previous report. Results show cooling required decreases with narrower spacing in contradiction to on-state resistance and switching losses increasing with decreasing spacing past 100-μm. The mechanism for this has not yet been determined.

(C) TCAD simulations show voltage holdoff decreasing with increase p-doping peak concentration and depth. This result is consistent with AUG 2016 result in the STTR

reports where deeper p-doping is used to increase breakdown by preventing punch through (PT) breakdown (a commonly known technique in the fabrication industry for power devices). TCAD simulations also show the Si-PCSS operates in PT mode of operation when at 70% of the maximum holdoff (~7000-V). The mechanism of PT in quantifying the voltage holdoff due to p-doping has not yet been determined.

For the ohmic contacts, experimental and theoretical results for specific contact resistance vs p- or n-doping at the contact have been collected. Data have not yet been found for contact resistance vs metal used to contact silicon (aluminum). Doping level for ohmic contacts is usually given down to 1×10^{18} dopant atoms/cm^3 and imply the p-doping could be lowered more than has been attempted. Data for the I-V ohmicity has not yet been found. TCAD can include distributed contact resistance for the ohmic contact modeling which has not yet been done.

3.1.4 Significant Finding(s) and Mission Impact

Heat power and heat energy extracted during the Si-PCSS voltage output pulse, turn-on and turn-off was higher for wider top contact spacing as shown in Figure 3.1.1. Average Si-PCSS temperature (Figure 3.1.2, open triangles) increases with wider spacing. Initial maximum temperature (open circles), before the sharper increase, also increases with wider spacing. These results are consistent with heat removal at the 300 K thermal contact (cathode). The maximum temperature hotspots have yet to account for spacing discrepancies in the top contact end models and do not follow a clear trend. The initial maximum device temperature, average device temperature and heat extracted linearly increase with spacing (not shown).

The 100 um spacing can be chosen as the optimum spacing (compared to optimal 350 um spacing considering on-state resistance and required laser energy) based on spacings between 100 um and 350 um having the lowest on-state resistance (Oct 2020 MSR) and heat removed being less for narrower spacings. However, this optimum depends on the laser requirement vs cooling requirement weighting which generally favors reduced laser requirements.

The optimization of the top contact laser windowing spacing for cooling requirements primarily leads to increases in device operation lifetime while still reducing required laser energy. Including considerations for cooling narrows the range of possible optimal laser windowing spacings and leads to a more optimized spacing than when considering laser requirements alone.

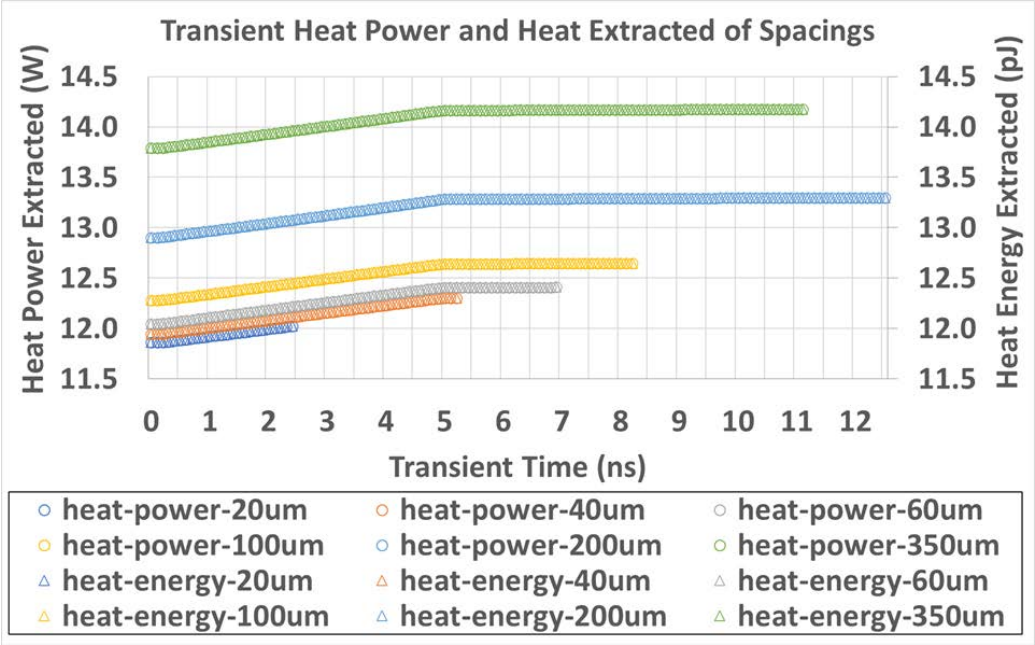


Figure 3.1.1. Heat extracted for various top contact spacings. Heat extracted through 300 K thermal cathode contact increases until power through switch ends and only slowly increases.

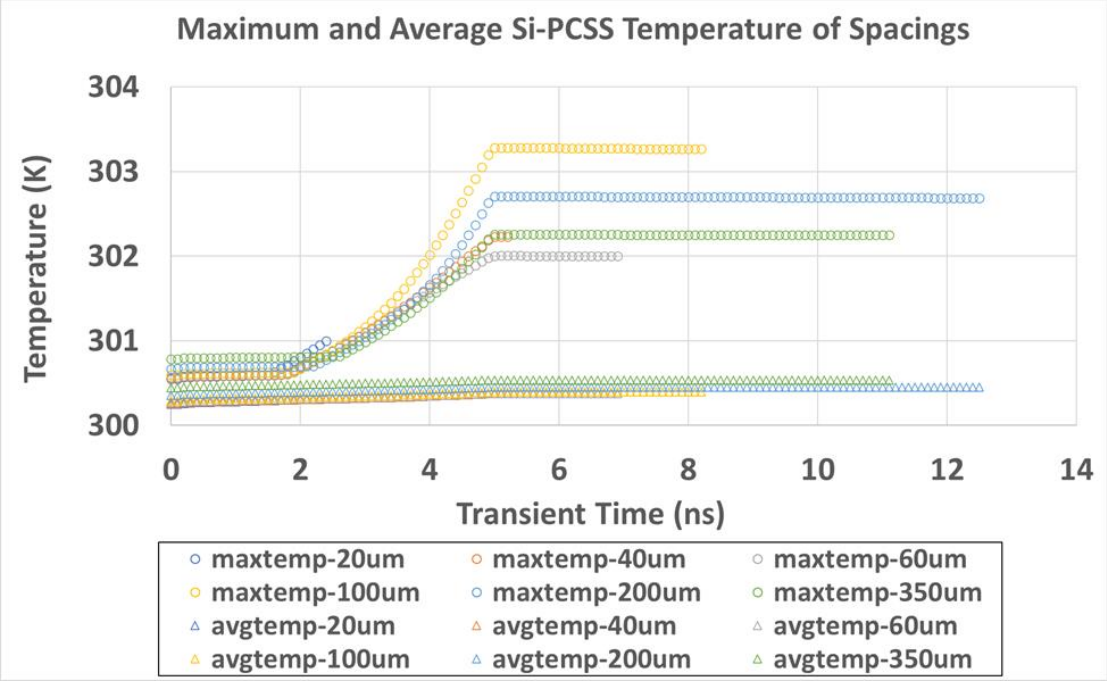


Figure 3.1.2. Device temperature for various top contact spacings. Average device temperature only increases slightly over reverse-bias steady-state temperature while maximum device temperature increases more significantly during the power moving through the Si-PCSS. Device temperatures then decrease slowly.

3.2 Lasers and Optics

(Scott Shepard)

3.2.1 Problem Statement, Approach, and Context

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W).

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution. This way of implementing an optical fiber laser (via an optical fiber amplifier) has SWaP advantages with respect to traditional (fiber and free-space) laser designs.

Sub-Problem (1): Optical pump power system costs are the dominant source of costs (in both normal/free-space lasers and in optical fiber lasers, of this class).

Sub-Problem (2): Amplified spontaneous emission (ASE) and fiber nonlinearities impede the optical amplifier performance.

State-of-the-Art (SOTA): Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs are prohibitive until reduced by a factor of two.

Solution Proposed: A pre-burst optical pumping scheme can reduce costs by a factor of at least ten.

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system needed to drive the PCSS will meet the modular and scalable volume and cost aim-points.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability.

3.2.2 Tasks and Milestones / Timeline / Status

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / Feb-July 2020 / Simulations showed that we can drop the pump power costs by a factor of 40 with tolerable pre-burst ASE. UMKC invention disclosure filed 02JUN2020. Task completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / A linear gain theory predicted the in-burst ASE over our spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020. Task completed.

(C) Design saturable gain devices which avoid nonlinear damage. / On-going / Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / On-going / Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) Demonstrate a cost-reduced fiber laser. / Feb-Aug 2021 / Key parts ordered.

3.2.3 Progress Made Since Last Report

(E) The relation between the unsaturated/initial fiber gain (per meter) and Yb dopant concentration has been established. This enabled calculations which provide reasonable estimates as to the amount of nonlinear impairments we might expect for various amplifier system gains (set in part by the total fiber length). These estimates will be utilized in the final design of our proof of concept (POC) experiment.

3.2.4 Significant Finding(s) and Mission Impact

As we transition from theory to a proof of concept (POC) experiment in task (E) it becomes imperative that the dimensionless parameters of our models map correctly into the absolute numbers corresponding to the materials used. This should have been a simple matter but it was plagued by typos in the references and a variety of different units for variables of the same name. Resolution of those issues resulted in correct formulae for mapping Yb emission cross-sections and dopant concentrations into g_0, the initial gain (per unit length) of the fiber amplifier. That initial (unperturbed) gain will saturate, in accordance with our simulations, but g_0 by itself provides estimates as to the fiber lengths, L, and optical pump powers we will need for a given overall system/amplifier gain. We prefer low dopant concentrations and longer L for efficiency and thermal constraints. Yet we prefer higher concentrations permitting shorter L in order to reduce the impact of the nonlinearities (e.g., Stimulated Raman Scattering).

3.3 Si-, SiC- and GaN Modeling and Evaluation

3.3.1 Problem Statement, Approach, and Context

(John Bhamidipati)

Primary Problem: The evaluation and optimization of PCSS-based HPM source drivers is complicated by interdependent and unquantified operational parameters (photoabsorption, carrier dynamics, sub-band levels, etc.) of novel photoconductive materials with unique external trigger requirements.

Solution Space: Model and simulate Si-, SiC- and GaN-PCSSs with varied geometry, doping profiles, contact layering, and post-processing techniques to evaluate their optical triggering and cooling requirements. Evaluate their performance at theoretical limits and explore novel fabrication techniques to push beyond established state-of-the-art limitations in terms of carrier dynamics, peak and average power, repetition rates, and cooling needs.

Sub-Problem: Incompletely defined dopant-dependent (carbon and nitrogen) sub-band levels and their respective optical absorption parameters for GaN, limiting application-level modeling and implementation of GaN-PCSSs.

State-of-the-art (SOTA): Lateral GaN-PCSS with carbon (C) and iron (Fe) doped variants capable of ~5 kV hold-off in linear- and lock-on (at >3 kV/cm fields) operation modes exhibiting sub nanosecond rise- and nanosecond-order recovery-times.

Deficiency in the SOTA: Limited understanding of GaN material properties/parameters responsible for lock-on/avalanche mode in intrinsic and compensated (C/Fe) GaN has limited repeatability of the observed lock-on/avalanche operation, limiting per-pulse HPM power throughput due to the lack of photoconductive gain and SOTA-limited incident optical energy.

Solution Proposed: Study GaN-PCSS operational parameters for intrinsic and compensated (C/Fe) variants to determine material properties and/or operational parameters (device/circuit based) responsible for lock-on mode of operation to reduce the optical energy requirements.

Relevance to OSPRES Grant Objective: Explores PCSS-based source driver trade space in terms of device operational parameters for HPM systems to determine an application-specific SWaP-C^2 optimized solution for source drivers by leveraging modeling and simulation tools.

Risks, Payoffs, and Challenges: Lock-on operational mode would potentially reduce the optical requirements by a factor of 10, but the operational mechanism is not well understood and has not been defined mathematically. This raises an issue with quantifying the system requirements for repeatability, alongside potential issues with increased turn-off times due to sustained conduction.

3.3.2 Tasks and Milestones / Timeline / Status

(A) Model carbon-compensated GaN-PCSS with vertical and lateral geometries, varied contact layers, carrier dynamics (generation, transport, and recombination) and circuit topologies to verify operational mode and current gain; then, calculate reduction in optical requirements in contrast with linear mode. This task is partially completed and currently put on hold for the months of January and February as we concentrate more on immediate needs of the program. [Apr 2021/ on hold]

(B) Evaluate the doping profiles, contact layering, and patterning for SiC-PCSS and explore suitable fabrication techniques to achieve desired optimal doping profile using TCAD-Athena. [Apr 2021]

(C) Complete parametric study of SiC-PCSS including rise and recovery time optimization simulations for varied vanadium and nitrogen concentrations, and high voltage transient response study for varied geometry, optical trigger, contact design, and illumination area. [Apr-May 2021]

3.3.3 Progress Made Since Last Report

(A) Initial modeling has been completed for intrinsic and nitrogen-compensated GaN-PCSS with lateral and vertical geometries. Switch gaps of 250 µm, 500 µm, and 1000 µm have been investigated for doping concentrations between 1E8–1E16.

3.3.4 Significant Finding(s) and Mission Impact

Dark current (leakage) on the order of tens-of-µA were seen in the vertical and lateral nitrogen-compensated GaN-PCSS models. Effects of carbon and iron compensation in mitigating the dark currents are yet to be studied. Comprehensive study of GaN's intrinsic and extrinsic optical properties in conjunction with device design provide insight into inter- and intra-band transitions that directly affect the conduction mode and help in identifying an optimal path to reducing optical energy/pulse requirement.

3.4 Multi-Stage Optical Amplifier

(John Bhamidipati)

3.4.1 Problem Statement, Approach, and Context

Primary Problem: Need for heavy (~125 lbs.), bulky (~10 cu-ft), and expensive (~$120,000) conventional laser systems (1064 nm) in PCSS-based HPM applications, with an additional need for second and third harmonic generation (SHG/THG) optics to trigger WBG solids (GaN/SiC).

Solution Space: Design and implement a compact (~1.1 cu-ft), lightweight (10–15 lbs.), and inexpensive (<$15,000) alternative for conventional high average power optical trigger (laser) system to improve SWaP-C^2 index of HPM systems.

Sub-Problem: Unavailability of commercial-off-the-shelf (COTS) miniature optical sources with sub-nanosecond pulse widths and tens-of-µm beam width, delivering >1-Watt power to implement as a makeshift/turnkey solution for the laser system.

State-of-the-art (SOTA): High average power picosecond pulsed lasers available up to 50 W output power with a gain factor up to 40 dB (~10,000x power) with laser amplifier.

Deficiency in the SOTA: High average power 1064-nm pulsed lasers are bulky, require auxiliary systems, and additional optics for SHG/THG generation for wide bandgap (WBG) device triggering.

Solution Proposed: Multi-stage cascaded optical amplifier powered by laser diodes (arrays) and GaN-PCSS as a compact, inexpensive laser replacement capable of ~175°C operation.

Relevance to OSPRES Grant Objective: Provides an enhanced SWaP-C^2 compliant solution for the laser (optical trigger) subsystem, with a subsequent impact on overall HPM system cost, volume, and power (optical and electrical) requirements.

Risks, Payoffs, and Challenges: Complex interconnect and thermal management system (TMS) design at high temperature (130–175°C) operation; unavailability of COTS high power pulsed laser diodes could potentially raise a need for research in laser diodes (arrays).

3.4.2 Tasks and Milestones / Timeline / Status

(A) Complete feasibility study for the cascaded multi-state optical amplifier design and determine functional requirements for the laser diodes (arrays) and source driver [Dec 2020 / completed]

(B) Complete initial stage experimental implementation of the optical amplifier and demonstrate positive current gain using GaN-PCSS, triggered with a miniature 404 nm laser diode. [Feb 2021 / on hold]

3.4.3 Progress Made Since Last Report

(B) Experimental implementation is on hold awaiting backordered equipment (laser diodes and drivers) for lab testing.

3.4.4 Significant Finding(s) and Mission Impact

(A) Need for lock-on conduction mode with ~$10^{2.6}$ gain factor has been determined for triggering the laser diode array (LDA) at 1 MHz pulse repetition rate (PRR) to limit the amplification stages to 2. This contributes to maintaining the R&D and implementation costs low (10–12% of the conventional system), while achieving the expected goal of miniaturizing the optical subsystem by ~2 orders of magnitude.

3.5 GaN:C PCSS Direct RF Modulation

(Heather Thompson)

3.5.1 Problem Statement, Approach, and Context

Primary Problem: Need for a more compact, cost-effective RF pulse generation system for Navy afloat missions on smaller vessels and vehicles.

Solution Space: Improve efficiency and reduce necessary material, size, and thermal requirements by utilizing gallium nitride (GaN) in PCSSs through exploitation of its theoretical material properties which allow for higher operating voltages, frequencies, and temperatures, while also eliminating the need for pulse-shaping transmission lines through direct RF modulation using the laser/photon source driving the PCSS.

Sub-Problem: Lack of maturity in compensated gallium nitride semiconductor (i.e., GaN:X with X=C,Fe) PCSS manufacturing, development, and optimization.

State-of-the-Art (SOTA): Si-based PCSS with >10 kV operational voltage, cooling system capacity of 500 W/cm^2, and theoretical breakdown of 1.3 MW/cm.

Deficiency in the SOTA: Si-based technologies requiring ~100 µJ optical pulses per 4 MW of RF output power, increasing the size of laser necessary for device triggering; long recovery time (ones-of-µs), limiting quick opening and high pulse-repetition-rate operation along with increased heating in the PCSS; critical electric field of 0.3 MV/cm, leading to devices that are ones-of-cm^2 in area for the target peak power; and operating temperature of <160°C, leading to increased cooling requirements.

Solution Proposed: Replace Si-PCSS device with GaN:C utilizing direct RF modulation — eliminating the need for a bulky pulse-forming transmission line (~3 ft long) — capable

of handling >3 MW (peak power) with ~20 μJ of incident optical energy, device area <1 cm^2, and operating temperature ~500°C (theoretical temperature which will be limited by circuit components and solder).

Relevance to OSPRES Grant Objective: Reduction in size and cost for cooling system that prevents damage to the PCSS device and components along with eliminating need for a pulse-shaping system, as well as decrease in material cost, leading to enhanced SWaP-C^2 capability with greater modularity and scalability.

Risks, Payoffs, and Challenges: Due to manufacturing limitations, GaN PCSS devices tend to be limited to lateral geometries (both contacts on the top side of the device), limiting operating voltage due to current crowding and surface flashover. The recovery time (ones-to-tens-of-ns) may lead to device heating and increased DC, or zero-frequency, component when generating RF with a period on the same order as the recovery time.

3.5.2 Tasks and Milestones / Timeline / Status

(A) **Feb 2021** Demonstrate RF unipolar modulation in the 1–2 GHz regime and up to 2 kV operating voltage with current PCB setup and the automated optical delay system.

i. Test using Sylgard 184 covering the GaN:C device to prevent flashover. A small "well" was designed and produced to prevent Sylgard from spreading over the entire PCB, causing it to be too thin to completely cover the PCSS. The well will provide a mold for the Sylgard to cure in that will allow for a thicker layer and better prevent flashover between the contacts.

ii. Repeat high-voltage testing with GaN:C PCSS enclosed in a small with SF_6 gas chamber, to prevent flashover and allow for higher operating voltages. The chamber will be designed and fabricated using material offering minimal losses of laser energy. The well, designed for testing with Sylgard, will be modified to allow for a vacuum seal containing SF_6.

iii. Seek further solutions to achieve ~10 kV operating voltage depending on success with Sylgard 184 and SF_6, including studying the feasibility of vertical GaN:C devices that would eliminate surface flashover seen in lateral devices.

(B) **March 2021** Demonstrate RF bipolar modulation using two GaN:PCSSs, along with positive and negative power sources, based on the pulse-switch-out-generator-based circuit and setup with the automated optical delay system.

(C) **April 2021** Move test setup and show higher center frequency content and repetition frequency of unipolar and bipolar modulation using the neoLASE (70 ps) laser versus the wedge (~1.5 ns) laser.

(D) **May 2021** Complete study of recovery for differing gap lengths, incident energies, and operating voltages and find solutions to reduce the recovery time.

3.5.3 Progress Made Since Last Report

(A) Continued collecting unipolar modulation data as a function of optical-delay distance, charge voltage, and incident energy (up to 300 V). To conserve remaining devices, data is collected at each voltage to prevent device damage while still allowing for complete data collection.

Designed and fabricated a well to contain Sylgard to prevent it being too thin and spreading over the entire PCB.

3.5.4 Significant Finding(s) and Mission Impact

Towards demonstrating direct RF modulation at multiple-kV (A), collection of data (waveforms for FFT analysis) as a function of charge voltage, incident energy, optical-delay distance, and gap length continued up to 300 V to prevent damage to remaining GaN:C PCSS devices. It was found that without a mold (or well) for the Sylgard to cure in, it was too thin and spread over the entire PCB, leaving parts of the contact to copper connect exposed and prone to flashover. To remedy this, the Sylgard will be cured in a small well that will be removed once dried. This well design will continue to be altered to build a small SF_6 vacuum sealed chamber for higher voltage operation.

3.6 Bistable Operation of GaN

(Noah Kramer)

3.6.1 *Problem Statement, Approach, and Context*

Primary Problem: The short carrier lifetime of gallium nitride limits the pulse width of intrinsically triggered GaN PCSS to the length of the triggering laser pulse. Generating long pulse widths (> 1 ns) requires a laser system capable of delivering a long pulse with high energy; pulse width agility requires a laser capable of varying its pulse width. Furthermore, GaN PCSS act as a closing switch, and thus cannot be utilized in a system that uses inductive energy storage.

Solution Space: Bistable operation takes advantage of midgap levels, ionized by two laser pulses of differing wavelengths, to modulate the switch between long and short carrier lifetime states; the first laser pulse excites carriers and puts the switch in a long lifetime state, closing the switch, the second laser pulse opens the switch by putting it in a state with short carrier lifetime, enabling frequency agility, bulk conduction, and use as an opening switch for inductive energy storage.[1] To enable bistable switching in semi-insulating GaN via doping/co-doping, it is necessary to survey the capture cross sections of various dopants in GaN (literature/simulation/empirical studies) to determine their suitability for bistable operation and design a co-doping scheme.

Sub-Problem: Bistable switching requires a midgap level that has a large hole capture cross section and a small electron capture cross section; it needs to be determined what dopants in GaN have this property.[2]

State-of-the-Art (SOTA): The SOTA bistable photoswitch is the GaAs “BOSS” switch capable of switching 18 kV (limit of bias-voltage modulator) and varying pulse width from 650 ps – ~1.5 ns with sub-nanosecond opening.[3]

Deficiency in the SOTA: The breakdown field of GaAs is only 12% of that of gallium nitride (0.4 MV/cm vs. 3.3 MV/cm). Furthermore, GaAs has a low thermal conductivity, resulting in larger cooling requirements.

Solution Proposed: Replace bistable GaAs switch with a bistable GaN switch, enabling higher hold-off voltage, higher temperature operation, and lower thermal requirements compared to GaAs.

Relevance to OSPRES Grant Objective: Bistable operation of a PCSS would allow for inductive energy storage and/or pulse width agility.

Risks, Payoffs, and Challenges: GaN growth often incorporates unintentional dopants that necessitate compensation to achieve semi-insulating material. For example, GaN:C switches from NRL are compensated using carbon, but it is unclear whether the midgap levels are capable of bistable operation. Co-doping the PCSS while maintaining midgap levels suitable for bistable operation is the primary challenge of this effort. Another challenge is the requirement of timing two laser pulses of differing wavelengths. Depending on the dopant levels, this may be possible to perform with a frequency-doubled Nd:YAG laser, as the energy of 2.3 eV at 532 nm and 1.1 eV at 1054 nm is equal to the bandgap of GaN, however the bistable level would have to lie very near 1.1 eV.

3.6.2 Tasks and Milestones / Timeline / Status

(E) **Feb 2021** Investigate feasibility of bistable GaN operation.

iv. Review literature on GaN dopants to identify candidates with large hole capture cross section compared to electron capture cross section.

v. Propose possible co-doping schemes for bistable operation (compare to doping of current GaN devices).

(F) **March 2021** Simulate bistable GaN devices and find manufacturers for devices.

(G) **April 2021** Test bistable devices

a. I-V, C-V, CW conductivity, UV-Vis, pulsed testing (single wavelength and dual wavelength).

(H) **May 2021** Complete study of switch operation varying wavelengths, bias voltage, and time delay between the on and off laser pulses.

3.6.3 *Progress Made Since Last Report*

(A) Reviewed literature on bistable GaAs switches; important findings are presented below.

3.6.4 *Significant Finding(s) and Mission Impact*

Bistable operation of a PCSS requires that there be electron-filled midgap states that have a higher hole capture cross section than electron capture cross section.[2]

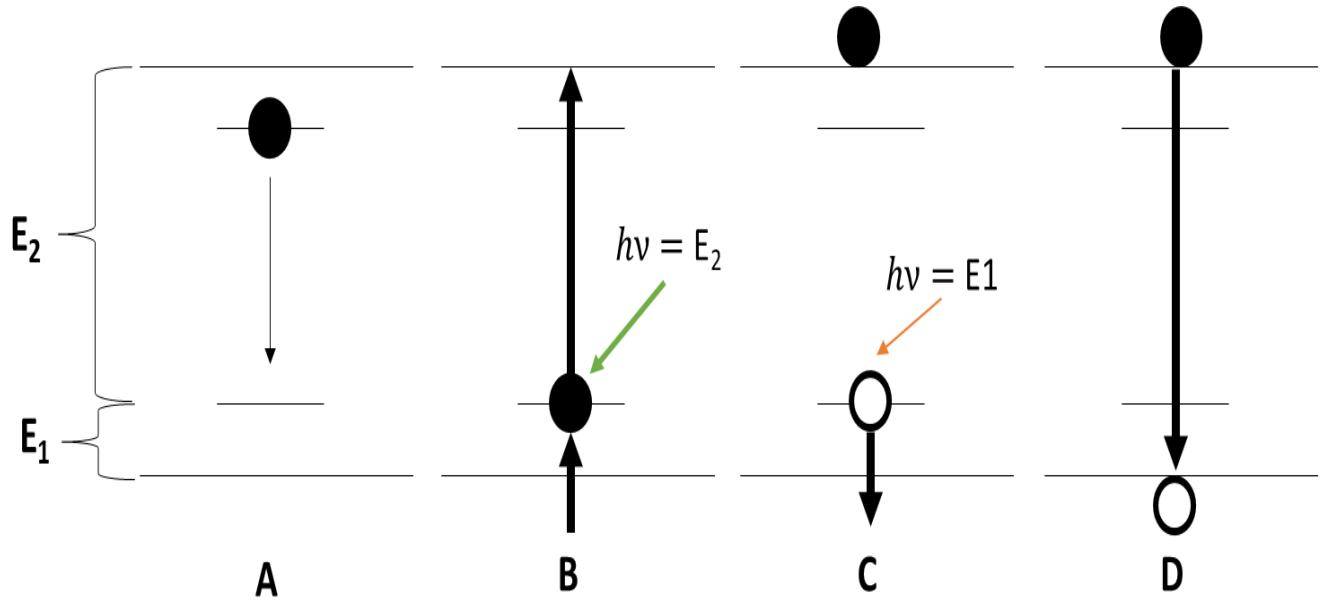


Fig. 3.6.1. Bistable co-doping scheme and mechanism.

In a bistable PCSS, shallow donors (**Fig. 3.6.1.** A) populate a deep level. Electrons can then be excited from this deep level by a wavelength with energy less than that of the bandgap (**Fig. 3.6.1.** B). Electron–hole pairs are also formed by two-photon processes (**Fig. 3.6.1.** B). The holes are captured by the deep level, as it has a higher hole-capture cross-section than electron-capture cross-section and any holes in excess of the deep level concentration will recombine with excited electrons until there are no free holes in the valence band. Because there are no holes in the valence band for the remaining excited electrons to recombine with, conduction is locked on. To stimulate recombination, holes are ionized from the deep level by a wavelength shorter than the initial wavelength (**Fig. 3.6.1.** C), stimulating recombination and opening the switch (**Fig. 3.6.1.** D). The minimum pulse width is dependent on the recombination time for electron–hole pair recombination, as well as the time required for holes to populate the deep level; the maximum pulse width is dependent on carrier lifetime without stimulating electron–hole pair recombination.

One of the main tradeoffs in bistable operation is the number of recombination centers present. More recombination centers will allow for faster opening, but limit the maximum pulse width of the device.[4] With limited recombination centers, the on-state may continue for 100's of nanoseconds, but have a slower opening time, whereas with a high concentration of recombination centers, the maximum pulse width may be limited to <1 ns.

3.6.5 *References*

[1] D. C. Stoudt, J. S. Kenney, and K. H. Schoenbach, "Inductive energy storage using a fast-opening bulk optically controlled semiconductor switch (BOSS)," *IEEE Int. Pulsed Power Conf. - Dig. Tech. Pap.*, vol. 1, pp. 123–126, 1993, doi: 10.1109/ppc.1993.512892.

[2] K. H. Schoenbach, V. K. Lakdawala, R. Germer, and S. T. Ko, “An optically controlled closing and opening semiconductor switch,” *J. Appl. Phys.*, vol. 63, no. 7, pp. 2460–2463, 1988, doi: 10.1063/1.341022.

[3] D. C. Stoudt, M. A. Richardson, H. D. Willie, and D. L. Demske, “High-power, high-repetition-rate operation of a Bistable Optically controlled Semiconductor Switch (BOSS) David C. Stoudt, Michael A. Richardson, Heather D. Willie, and David. L. Demske Dahlgren Division, Naval Surface Warfare Center,” vol. 2343, pp. 135–144, 1994.

[4] D. C. Stoudt *et al.*, “Subnanosecond High-Power Performance of a Bistable Optically Controlled GaAs Switch -ADA637490.”

3.7 Diode-Based NLTLs

(Nicholas Gardner)

3.7.1 Problem Statement, Approach, and Context

Primary Problem: Size, weight, and cost of pulse forming/shaping networks (PFNs) need to be reduced and optimized for Navy afloat missions.

Solution Space: Develop a lumped-element nonlinear transmission line (LE-NLTL) as a pulse shaping network for the conversion of energy to the ultra-high frequency (UHF) band at single MW peak power.

Sub-Problem: Metrics used for component selection are designed for LE-NLTLs operating at sub 0.1 GHz frequencies. Using such metrics alone to design LE-NLTLs capable of single GHz frequency generation introduces a trial by error nature to the design process wherein frequency/power generation predictions and measurements can differ by a few hundred MHz or the design potentially fails to operate at all.

State-of-the-Art (SOTA): LE-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit. Simulations of LE-NLTLs indicate achievable frequencies in the single GHz range.

Deficiency in the SOTA: Simulation/measurement agreement becomes increasingly sensitive to parameters and factors outside of inductive and capacitive element choice alone. Disparities between measurement and simulation above contribute to a trial by error design process for LE-NLTL networks.

Solution Proposed: Identify and characterize diode parameters affecting frequency generation in the context of a NLTL application and identify limits/desired ranges required for UHF generation. Such parameters include, but are not limited to: diode frequency response, diode reverse bias hold-off voltage, diode small signal capacitance, diode chip/package parasitics, and diode relaxation time. Inclusion of such parameters increases simulation accuracy and improves the LE-NLTL design/implementation pipeline.

Relevance to OSPRES Grant Objective: The SWaP-C^2 capabilities of LE-NLTLs lend the technology towards applications which require modular, scalable, and low-cost pulse shaping networks (shown in Figure 3.7.1).

Figure 3.7.1. 20 cell LE-NLTL of dimensions 1.1 x 23.45 cm constructed with COTS components.

Risks, Payoffs, and Challenges: There exists a potential tradeoff between power and frequency generation. Devices such as ceramic capacitors may be used in a LE-NLTL to generate high peak power due to their break down potentials in the 10s of kV, however, such devices become highly resistive at 0.1–0.2 GHz frequencies. Diodes have been shown to be operational at frequencies upwards of 0.4 GHz, however, possess low hold-off potentials limiting peak output power. The payoff to overcoming these challenges is significant reductions in PFN size and cost.

3.7.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Construct/demonstrate a prototype capable of UHF generation at low voltages (1–100 V excitation amplitude)

a. Task – Break a low-voltage pulse into a sequence of solitons (Completed SEP20)

b. Task – Increase frequency generation past 200 MHz (Completed NOV20)

c. Task – Select diode candidate (junction capacitance < 50 pF) and simulate expected results (FEB21)

d. Task – Design/fabricate/test line (MAR21)

(B) Milestone – Tuning of waveform at low voltages using electrical or mechanical means

a. Task – Simulation of a topology capable of biasing the diodes using a DC voltage (Completed)

b. Task – Construct and perform initial tests on prototype (Completed JAN/FEB21)

c. Task – Troubleshoot prototype design and identify differences with simulation (**NEW**)

(C) Milestone – Construct/demonstrate a prototype capable of frequency generation above 1 GHz at single MW peak powers (Completed MW peak power but not GHz center frequency)

a. Task – Identify diode candidates with a hold-off voltage of several kV and a low signal junction capacitance under 100 pF (Completed JAN21)

b. Task – Design/fabricate single diode prototypes (Completed JAN21)

c. Task – Perform initial tests using half-barrel pulse source (Completed FEB21)

d. Task – Compare measurements with simulation and identify discrepancies (FEB21)

e. Task – Design/fabricate/test prototype using two diodes in series and compare measurements with simulation (FEB21-MAR21)

(D) Milestone – Demonstrate scalability (On hold until milestone C is completed)

3.7.3 Progress Made Since Last Report

(A) No new progress to report.

(B) The voltage tunable prototype successfully generated solitons, however there was no correlation observed between bias voltage and center frequency generation as well as an overall drop in center frequency generation when compared to the unbiased line. The network consisted of 40 cells with one 22 nH inductor and one diode (model SMV1702) per cell. Waveform results are shown in Figure 3.7.2.

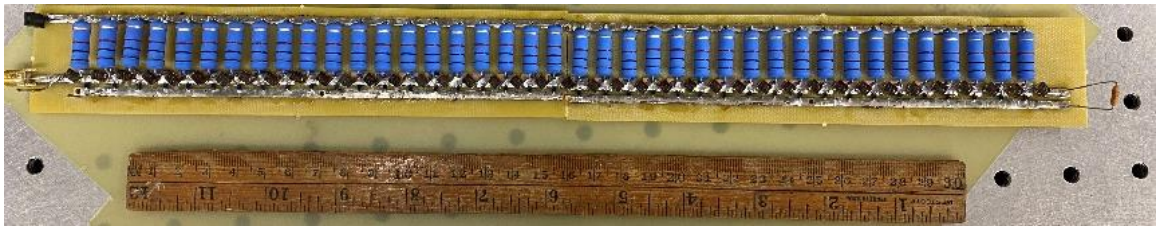
(C) A prototype was successfully tested using a pulse produced by the half-barrel source. The prototype consisted of 20 cells, each containing one 12 nH inductor and one diode (model K100F). The resulting pulse increased the amplitude of the half-barrel source and reduced the rise time of the pulse corresponding to an increase in peak power as well as spectral content. Waveform results are shown in Figure 3.7.3 and are discussed in Section 3.6.4.

(D) No new progress to report.

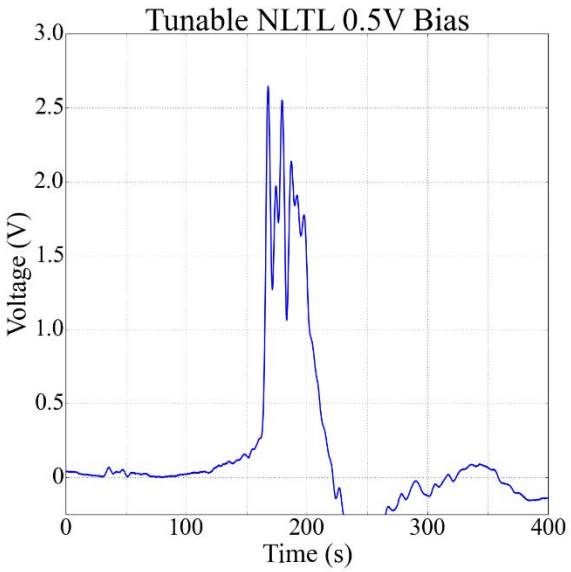
3.7.4 Significant Finding(s) and Mission Impact

Results of the high voltage D-NLTL provide the most significant findings of January. The network successfully increased the peak amplitude from 8.7 kV to 9.1 kV and reduced the rise time from 1.36 ns to 560 ps. The generated amplitude is significant as it corresponds to a peak power of 1.66 MW. The reduction in rise time gives a maximum frequency generatable (also known as the Bragg cutoff frequency) by the line as 1.78 GHz. Both values are encouraging as they show the line is capable of shifting energy to the GHz frequency range at single MW peak power. The shift of energy to higher frequencies is shown in Figure 3.7.3c, with peaks generated at ~400, ~600 and ~750 MHz.

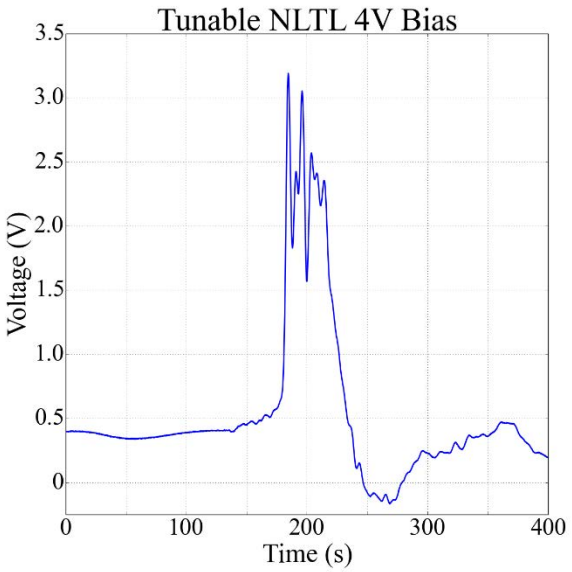
One area that needs further work is the lack of secondary soliton generation. Sequences of solitons are the primary contributor to the center frequency (peak amplitude in frequency domain) of the network with the inverse of the time between solitons strongly correlating with the peak in frequency domain. Factors that could have affected the ability to generate a full sequence of solitons include: excitation pulse width, D-NLTL length, and losses within the network—each will be evaluated as a possible reason for which only a single soliton was formed from the primary pulse. Simulations of the K100F network indicate the possibility of center frequencies above 1 GHz, which is consistent with the measured Bragg frequency.



(a)

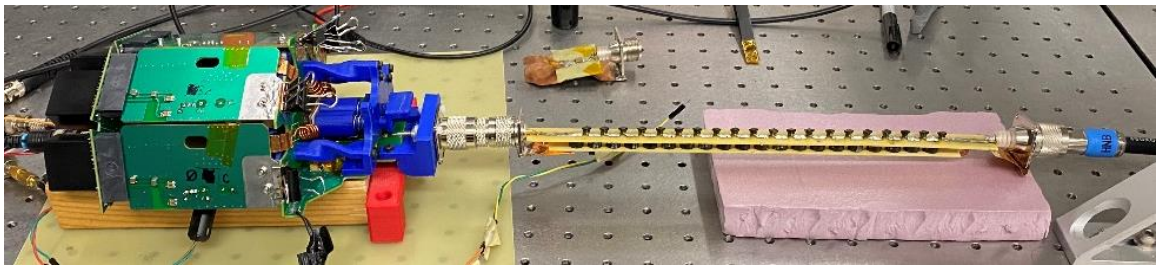


(b)

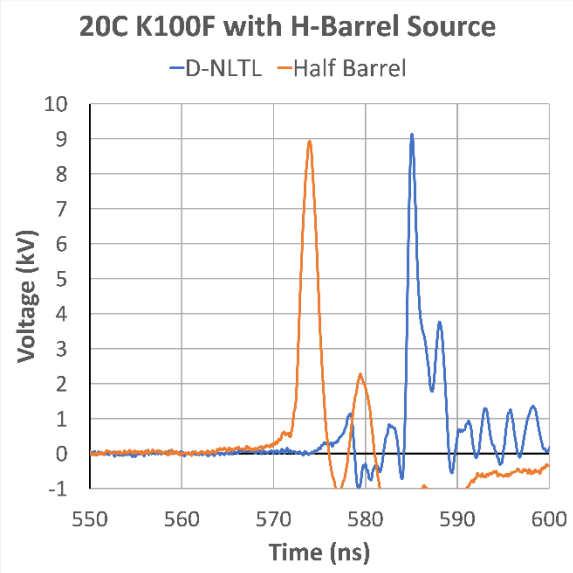


(c)

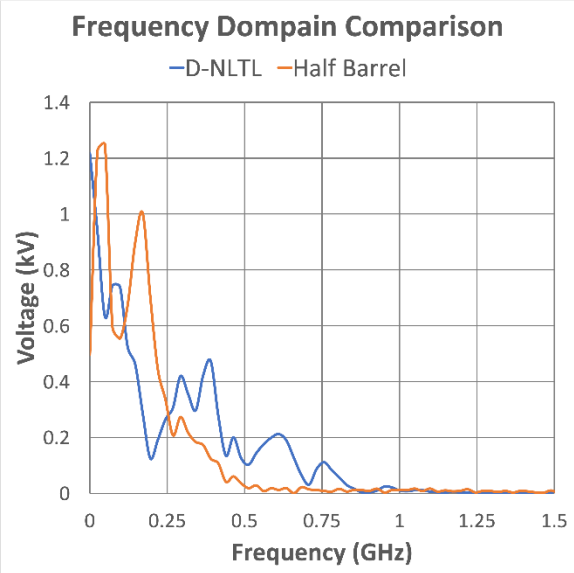
Figure 3.7.2. Results from initial round of tunability testing. (a) Fabricated board with ruler for scale; DC bias is applied to each diode through 1 kΩ resistors. (b) Generated waveform at a bias voltage of 0.5 V. (c) Generated waveform at a bias voltage of 4V.



(a)



(b)



(c)

Figure 3.7.3. Results from testing the K100F D-NLTL using the half-barrel source. (a) Experimental set-up. (b) Waveform results in time domain. (c) Waveform results in frequency domain.

4.0 Prime Power and Conditioning

4.1 HV Switch Pulsed Chargers

(Wasekul Azad and Faisal Khan)

4.1.1 Problem Statement, Approach, and Context

Primary Problem: Commercially available high-voltage solid-state switches made by BEHLKE are the best in SWaP-cooling, but are expensive, have long lead times (2–3 months), and are made outside of the US. For the Navy afloat mission to be successful, we need a sustainable supply of US-manufactured switches at a much lower cost.

Solution Space: Design and demonstrate modular high-voltage (~10 kV) and fast (repetition frequency = 100 kHz) solid-state switches using a combination of series- and parallel-connected commercially available inexpensive discrete MOSFETs and custom high-voltage (~10 kV) isolated gate drivers.

Sub-Problem: Voltage balancing among the series-connected MOSFETs, minimization of gate signal delays, cooling of the individual MOSFETs, balancing resistors, high-voltage isolation required for the power supplies, and the controlling pulse width modulated (PWM) signal as well as differential voltage feedback measurement across individual MOSFETs.

State-of-the-Art (SOTA): Direct liquid-cooled solid-state switch from BEHLKE (e.g., HTS-151-30).

Deficiency in the SOTA:

1. BEHLKE made switches are expensive. For instance, a single HTS-151-30 switch costs around $5,000.
2. BEHLKE switches along with direct liquid cooling units occupy a considerable amount of space. For instance, a HTS-151-30 switch from BEHLKE has a footprint of approximately 225*85*75 mm without considering the liquid cooling system. Some key parameter of this switch are as follows.

   i) Maximum operating voltage = 15 kV

   ii) Maximum continuous load current = 2.52 A (without cooling), 30 A (with liquid cooling)

   iii) Maximum turn-ON peak current = 300 A (pulse width = 200 µs, duty cycle <1%)

   iv) Turn-ON resistance = 1.3 Ω
3. Once the switching frequency is greater than 10 kHz, a liquid cooling system is required to operate the BEHLKE switch.
4. Without liquid cooling, the maximum continuous power dissipation (P_{cont}) of the BEHLKE switch is limited (e.g., for HTS-151-30, P_{cont} is 10 W without liquid cooling).
5. At higher switching frequency (>20 kHz), the BEHLKE switch requires multiple ancillary DC power supplies, i.e., 5, 15, and 60 V.

6. The switches made by BEHLKE cannot be reconfigured to withstand a higher voltage exceeding their recommended rating. BEHLKE offers separate products to operate them at higher voltage/currents.

Solution Proposed: Designing a modular high-voltage (~10 kV) switch using a single custom isolated gate driver for each module and having a construction cost lower than the BEHLKE switch with equivalent or better performance in all specification categories (Specifications for the BEHLKE switches can be found in the following link: http://www.behlke.com/separations/separation_c4.htm).

Relevance to OSPRES Grant Objective: The proposed modular high-voltage switch is expected to facilitate controlled hundreds-of-nanosecond charging of an array of transmission lines of pulse forming networks to drive an array of PCSSs, thereby producing controlled hundreds-of-picosecond scale high-voltage pulses.

Risks, Payoffs, and Challenges:

I. Lack of rigid control over voltage balancing can lead to a cascaded failure among the series-connected MOSFETs.

II. In the absence of an adequate mitigation scheme, voltage overshoot due to the fast switching speed can exceed the voltage rating of an individual MOSFET, thereby damaging the switch.

III. At high voltage (~10 kV) and high repetition rate (>100 kHz), mitigating EMI to safeguard the individual MOSFETs from false turn-ON is a major challenge.

4.1.2 Tasks and Milestones / Timeline / Status

(A) (i) Design a surface-mount MOSFET-based four-stage switch (6.8 kV rated) and control it using the in-house gate driver / 5 weeks or 12 DEC / Completed.

(ii) Test the voltage withstanding ability of the switch with a DC supply voltage up to 4–5 kV and evaluate the effectiveness of the thermal management at its current state / Dec 2020 / Completed.

(B) Design a modular HV switch (~10 kV rated) using the concept of the tested four-stage high-voltage switch and the in-house gate driver / Jan–Feb 2021 / Ongoing.

(C) Test the voltage withstanding ability of the modular HV switch with a DC supply voltage up to 10 kV and switching frequency up to 50 kHz using a resistive load (3–5 kΩ) and evaluate the effectiveness of the thermal management at its current state / Feb–Mar 2021 / Ongoing.

(D) Test this modular HV switch coupled with a Si PCSS device up to a DC supply voltage of 5–6 kV and switching frequency of 50 kHz / Mar–April 2021 / Awaiting results of (C).

4.1.3 Progress Made Since Last Report

(B) An eight-stage modular (two modules) HV switch has been simulated in LTSpice and designed in ALTIUM using 1.7 kV rated SMD MOSFETs (C2M1000170J) made by CREE.

Each module comprises four MOSFETs and is rated for close to 6.8 kV. A modular gate driver has been designed to drive these two modules of the HV switch. The simulation shows a minimum voltage imbalance close to 50 V across the series-connected MOSFETs. The rise time of the HV switch is measured close to 18 ns.

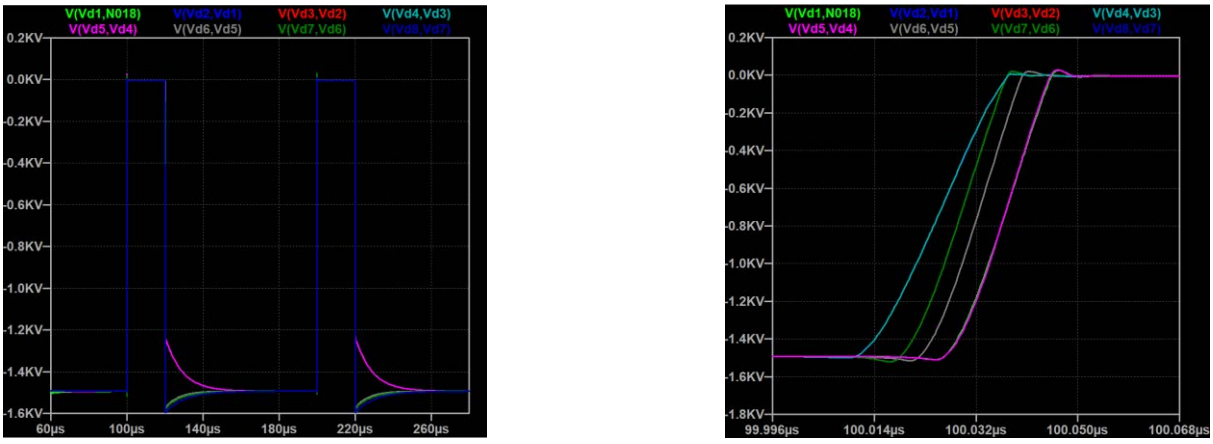
(C) Testing of both the gate driver board and the HV switch will begin after the fabrication of the corresponding PCB boards are completed.

(D) Testing will be accomplished after the fabrication of the modular HV switch and evaluating the test results (e.g., voltage balancing, thermal stability) using the modular HV switch with resistive load.

4.1.4 Significant Finding(s) and Mission Impact

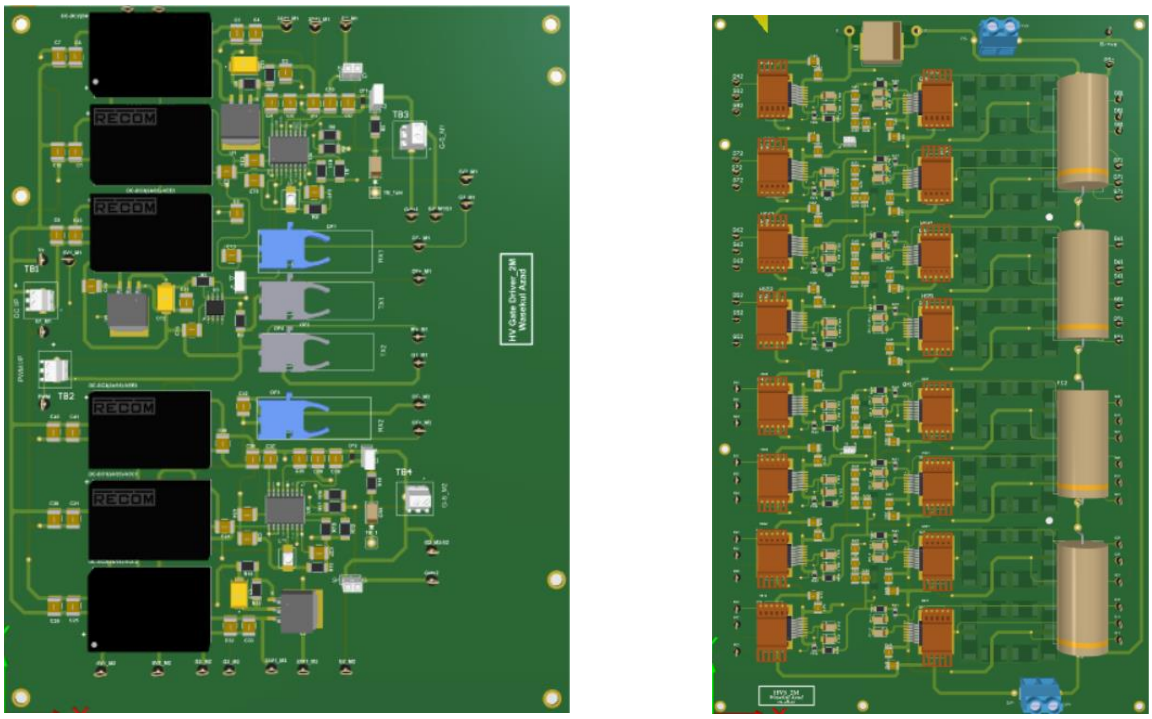
I. Design and fabrication of the four-stage HV switch using the in-house HV gate driver is completed. The switch has been tested up to a DC supply voltage of 4 kV and a switching frequency up to 10 kHz using a 3.2 kΩ resistive load. The 6.8 kV rated four-stage in-house HV switch demonstrated a maximum voltage imbalance close to 50 V which is negligible compared to the breakdown voltage rating (1700 V) of individual MOSFET.

II. The simulated voltages measured across each MOSFET is shown in Fig. 4.1.1. The PCB designs of the modular HV switch and the modular gate driver board are shown in Fig 4.1.2.



(a) (b)

Fig. 4.1.1. Voltage across the eight MOSFETs of the HV switch (a) zoomed out version and (b) rising edge



(a) (b)

Fig. 4.1.2. PCB designs of (a) Modular HV gate driver (b) Modular HV switch

5.0 Tradespace Analysis of Ultra-Wide-Band Antenna Arrays

5.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

5.1.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wide-band antenna elements in a phased array for HPM transmissions.

Deficiency in SOTA: Large physical aperture size.

Solution Proposed: Using electrically small antennas (ESAs) as array elements to reduce physical aperture size, followed by optimization of the design in terms of both near-field (Quality factor → bandwidth) and far-field (Directivity) parameters, simultaneously, via the *Directivity*/*Quality Factor* ratio (*D*/*Q*).

Relevance to OSPRES Grant Objective: Provides design and optimization (in terms of directivity/gain and bandwidth) guidelines for ultra-wideband ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Developing an Array Pattern Tool in the context of lightweight calculations of large antenna arrays (**NEW**) / Jan – Apr 2021 / ongoing.

(B) Investigation into the effect of array aperture area reduction on different array parameters / Jan – Feb 2021 / Investigations into array structures on infinite ground plane – completed; investigations into arrays on finite ground plane – ongoing.

(C) Building minimum viable validation prototypes on polyethylene and FR-4 substrates to achieve better performance for HPM transmissions at UHF range / Jan – March 2021 / ongoing.

(D) Time-domain analysis of the antennas subjected to input short pulses / Feb – May 2021 / ongoing.

5.1.3 Progress Made Since Last Report

(A) Developing Array Pattern Tool:

a. A tool is being developed (via MATLAB) for faster approximation of array radiation pattern.

b. Results from the tool, for a few preliminary test cases, showed good agreement with the results obtained from FEKO.

(B) Investigations into aperture area reduction:

a. Earlier we reported that ~30% reduction in the aperture area of a 15×15 array of microstrip patch antennas on infinite ground plane (by changing the grid formation from a square to a hexagonal lattice) leads to $\sim 3\text{dBi}$ reduction in the overall array gain.

b. A 15×15 array model on finite grounded substrate could not be computed using FEKO on LEWIS due to memory shortage (350 GB memory was requested).

c. A method to compute finite array structures is being investigated to reduce computation time and memory usage.

(C) Building minimum viable validation prototypes:

a. U-slot rectangular microstrip patch antenna designed in the UHF region (709 – 905 MHz), on FR-4 substrate (G10/FR-4: $\varepsilon_r = 5.2, \tan\delta = 0.025$), has been down-selected for fabrication; FR–4 board ordered for prototype manufacturing at UMKC.

5.1.4 Significant Finding(s) and Mission Impact

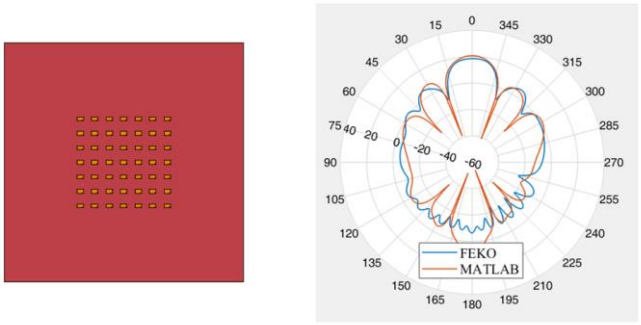
(A) Developing Array Pattern Tool:

Computation of the radiation pattern of large antenna arrays ($> 10 \times 10$) using commercially available EM solvers is a computational bottleneck, in terms of runtime (12 hours to a few days) and memory usage (>125 to 350 GB). A tool is being developed, via MATLAB, for faster approximation of radiation pattern of large arrays. Once fully developed, the tool can be used to estimate and compare the radiation pattern of arrays of different aperture areas, even on finite grounded substrates.

Features of the Array Pattern Tool:

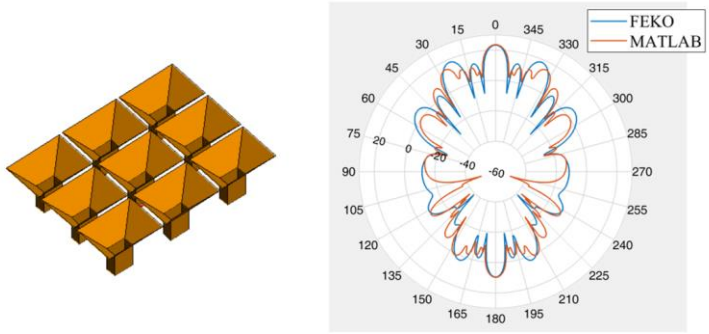
- ❑ Can predict the radiation pattern of an array composed of <u>any</u> type of antenna element (e.g., microstrip patches, Horn, Vivaldi, etc.).
- ❑ Each computation runs in <10 minutes on a standard laptop computer.

Results of some of the preliminary test cases are shown below:



(a) (b)

Fig 5.1.1. (a) Simulation model of a 7 × 7 array of coaxial probe-fed microstrip patch antennas, (b) comparison of radiation pattern of the array in E – plane (XZ - plane) at 815 MHz.



(a) (b)

Fig 5.1.2. (a) Simulation model of a 3 × 3 array of pyramidal horn antennas (b) comparison of radiation pattern of the 3×3 array in E – plane (XZ - plane) at 815 MHz.

5.2 Tradespace Analysis of Other Ultra-Wide-Band (UWB) Single Elements

(Kalyan Durbhakula)

5.2.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelov antenna has a unique design that is capable of generating UWB response by effectively merging the individual input impedance response from the transverse electromagnetic (TEM) horn antenna with an exponential

profile, electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand the parameter space effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via tradespace study.

Sub-Problem: The literature lacks detailed and advanced analysis (including tradeoffs between antenna metrics) on the individual and overall contribution of electric monopole, magnetic dipole, and exponential TEM horn parts to overall output.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered as the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains significantly large and has no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelov antenna that effectively reduces the physical aperture area while maintaining its UWB properties, both in frequency and time domains. The Koshelov antenna (from literature) has been shown to withstand high voltage levels (with careful design of feed) better than many existing horn antennas, thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelov antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the OSPRES objective related to HPM system. In addition, this work can yield a center frequency dependent, bandwidth controlled and electronically steerable Koshelov antenna design that can be quickly modified to the needs of high-rise time of the input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelov antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include library of antenna metrics data for different shapes and sizes of the individual parts within Koshelov antenna.

(iii) Large electrical size (> 5λ) of the Koshelov antenna at its highest operating frequency poses huge computational challenges. Efforts are underway to cleverly select important design parameters for tradespace study.

5.2.2 Tasks and Milestones / Timeline / Status

(A) Carried out detailed literature search in an effort to identify and list antenna elements that satisfy UWB properties and HPM requirements. Identified 14 antenna elements that are being widely used for UWB and HPM applications. Further down selected to 3

antenna elements (Koshelov antenna, Shark antenna and Fractal antenna) based on pre-defined and robust criteria that matches with OSPRES grant objectives to move forward with tradespace study and analysis. Additionally, special EM techniques have been looked into that offer an opportunity to reduce physical aperture area when combined with either single antenna element or as an array. / NOV20–DEC20 / Complete.

(B) Completed initial design, simulation, and validation of Koshelov antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area. Reduce the physical aperture size of the Koshelov antenna to 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / FEB21–MAR21 / Ongoing.

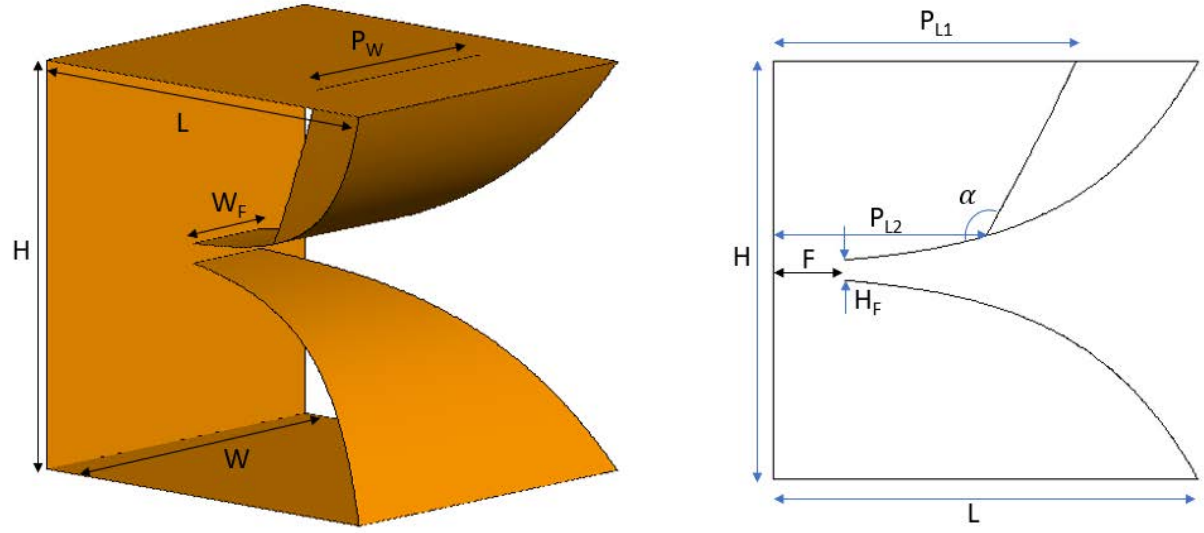
(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of time domain impulse response ($h_{rx/tx}(t,\phi,\theta)$) in receive or transmit mode. The impulse response of an antenna in receive mode can be calculated by applying deconvolution technique between the incident electric field ($e_i(t,\phi,\theta)$) (assuming a plane wave source) and the receive voltage ($V_{rx}(t)$) at the antenna input terminals. Eqn. (1) shows the relation between receive voltage, incident electric field and impulse response in receive mode. In (1), η_0 is the free space wave impedance and Z_C is the characteristic impedance at the antenna's input terminals. An envelope of impulse response ($|h_{rx}^{+}(t,\phi,\theta)|$) yields information about FWHM, ringing, dispersion and Q-factor. Generalize the code to calculate envelope of impulse response of the Koshelov and show how FWHM, ringing changes with change in physical aperture size/FEB21-MAR21/Ongoing.

$$\frac{V_{rx}(t)}{\sqrt{Z_C}} = h_{rx}(t,\phi,\theta) * \frac{e_i(t,\phi,\theta)}{\sqrt{\eta_0}} \quad (1)$$

(E) Continue with the literature search and improving our understanding on the special electromagnetic (EM) techniques to determine their applicability to the antennas under consideration. The special EM techniques are: Inductive loading, Dielectric embedding, Dielectric loading, Electromagnetic bandgap structure, Resistive terminations, Beveling and creating slots, Defected ground structures, Iterative projection method and Dielectric/Metamaterial lens, array lattice configuration (square vs rectangular vs triangular vs hexagonal vs sunflower etc.), subarray overlapping, E-plane and H-plane array and subarray placements./ JAN21–APR21 / Ongoing.

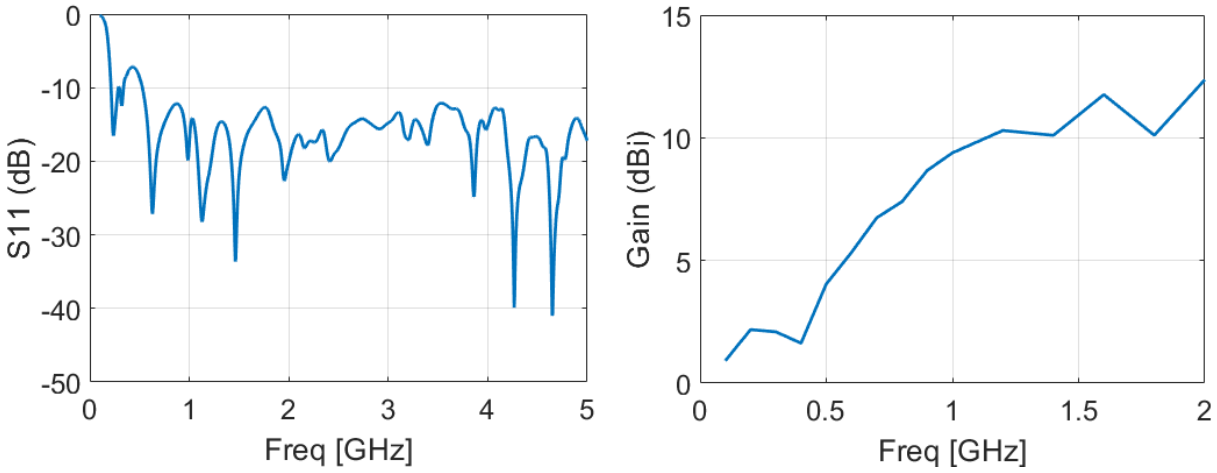
5.2.3 Progress Made Since Last Report

(B) Completed initial design, simulation, and validation of the Koshelov antenna. The initial design of the Koshelov antenna yielded a promising impedance bandwidth response (shown in fig. 5.2.2a) with a bandwidth ratio of at least 10:1. A higher bandwidth ratio can be obtained with further increase in the simulated frequency range. Fig. 5.2.2b shows the peak gain profile as a function of frequency at boresight.



(a) (b)

Fig. 5.2.1. Koshelov antenna with design parameters: H = 293 mm, W = 268 mm, L = 300 mm, W_F = 70 mm, P_W = 169 mm, F = 50 mm, H_F = 14.3 mm, P_{L1} = 150 mm, P_{L2} = 213 mm, and α = 26.86°. (a) 3D view, and (b) side view



1. (b)

Fig. 5.2.2. Koshelov antenna (a) Reflection coefficient/Return loss, and (b) Peak gain (dBi) at boresight.

(C) Achieved detailed understanding on how to determine FWHM and ringing from time domain impulse response function. Gathered required electric field data from initial Koshelov antenna simulation run to determine time domain impulse response.

(E) A decision has been made to carry out literature search only on those EM techniques that are directly applicable to single element antenna design. These include: Inductive

loading, Dielectric embedding, Dielectric loading, Electromagnetic bandgap structure, Resistive terminations, Beveling and creating slots, Defected ground structures, Iterative projection method and Dielectric/Metamaterial lens. Literature search on EM techniques that are specifically applicable to an array topology has been put on hold.

5.2.4 Significant Finding(s) and Mission Impact

(A) The extensive literature search on various UWB antenna elements has resulted in finding three promising antenna elements. The down selected antenna elements are the Koshelov antenna, Shark antenna and Fractal antenna, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the single antenna element first followed by its array configuration.

(B) The initial Koshelov antenna design yields promising output to carry forward the investigation. A comparison of the Koshelov antenna's metrics, which are deemed important in this iteration, are shown and compared against BAVA in Table 5.2.1. The Koshelov antenna is directional in both planes (E-plane & H-plane). Other metrics such as FWHM, ringing, peak and average power handling capability, electronic beam steering capability, effective radiated power (ERP), Q-factor, power spectral density, fidelity factor, rE/V factor, and energy density will be added gradually in the future MSRs.

Table 5.2.1. Antenna metrics

Antenna element type	Dimensions	Physical Aperture area	Bandwidth	Peak gain (1 GHz)	Directionality		Aperture Efficiency (1 GHz)
					E-plane (1 GHz)	H-plane (1 GHz)	
Koshelov [1]	300 mm × 268 mm × 293 mm	0.0785 m^2	10:1	9.4 dBi	51°	53°	80%

5.2.5 References

[1]. Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

5.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna

(Sadie Brasel and Kalyan Durbhakula)

5.3.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the

UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of shark antenna elements whose miniaturization in two dimensions (height and width equal to $\lambda/4$ where λ corresponds to the lowest operating frequency) make it a good candidate for UWB HPM systems while having a reduced aperture area with respect to the current state-of-the-art. In literature, the shark antenna has already shown to achieve wide 20:1 impedance bandwidth, low dispersion, and sectoral (also called as directional) radiation pattern. .

Sub-Problem: The design parameter space of the Shark antenna has not been studied rigorously in the literature and therefore the effect of these parameters on the antenna metrics is not understood. In addition, the shark antenna has been shown to be not very directive with a radiation half-power beamwidth (HPBW) of 252° in the H-Plane and 88° in the E-Plane.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered as the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains significantly large and has no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Explore the design parameter space for the shark antenna element using computational electromagnetic (EM) wave solvers starting with the simulation and validation of a single element.

Relevance to OSPRES Grant Objective: The shark antenna dimensions were established to be frequency dependent and can be readily modulated to the requirements of high-rise time input pulse and its bandwidth.

Risks, Payoffs and Challenges:

(i) Shark antenna is comprised of bicones with a control on its flare angle as well as truncated in the azimuthal angle. This still yields considerably higher HPBW than other antenna elements under investigation. Significant reduction of HPBW in H-plane can be unattainable and can be considered as a major risk.

(ii) Payoffs include library of antenna metrics data for various shapes and sizes of the bicones and reflector plates in the Shark antenna.

(iii) Specific design challenges are yet to be identified; however, computational challenges remain clear with respect to automation of design parameter space on the supercomputer (LEWIS).

5.3.2 Tasks and Milestones / Timeline / Status

(A) Completed initial design, simulation, and validation of the shark, antenna. The shark antenna has been designed and simulated according to [1]. / JAN21 / Complete.

(B) Further validation through LEWIS supercomputer is necessary for wider range of frequency results. / FEB21 / Ongoing.

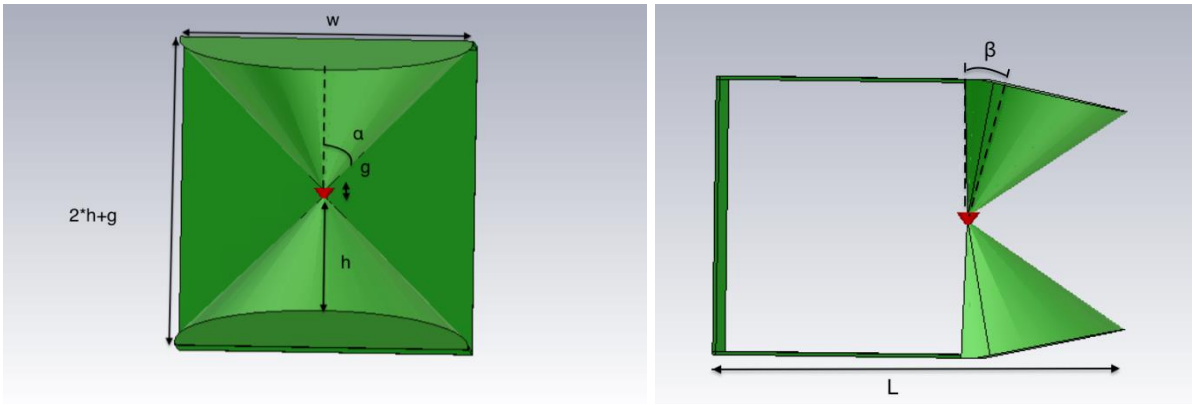
(C Identify shark antenna design parameters which contribute significantly to bandwidth, gain, and physical aperture area. Determine which parameters contribute most to performance improvement/size reduction. Flare angle (α), cone height (h), and feed gap (g) length are initial parameters of interest Provide a preliminary comparison of antenna metrics of the Shark antenna as a function of flare angle, cone height, and feed gap / FEB1-MAR21 / More detailed investigations are underway.

(D) Perform detailed tradespace study by simulating the shark antenna with varying flare angle, cone length, and feed gap length. Show detailed change in impedance bandwidth, rE/V, HPBW in H-plane, full-width half maximum (FWHM), ringing as a function of flare angle (α) / FEB21–APR21 / The relevant performance metrics will be computationally studied and compared against the BAVA design.

5.3.3 Progress Made Since Last Report

(A) Designed the shark antenna using FEKO and CST (Figure 5.3.1). The shark antenna design has been simulated up to 10 GHz using CST. Ongoing efforts are underway to simulate the design up to 20 GHz to validate the 20:1 impedance bandwidth [1].

(C) The flare angle (α), cone length (h), and feed gap length (g) have been identified as having a significant effect on the S11 and Gain performance of the antenna according to [2]. Ongoing efforts are underway to plan a detailed tradespace study and analysis with an emphasis on reducing physical aperture area.

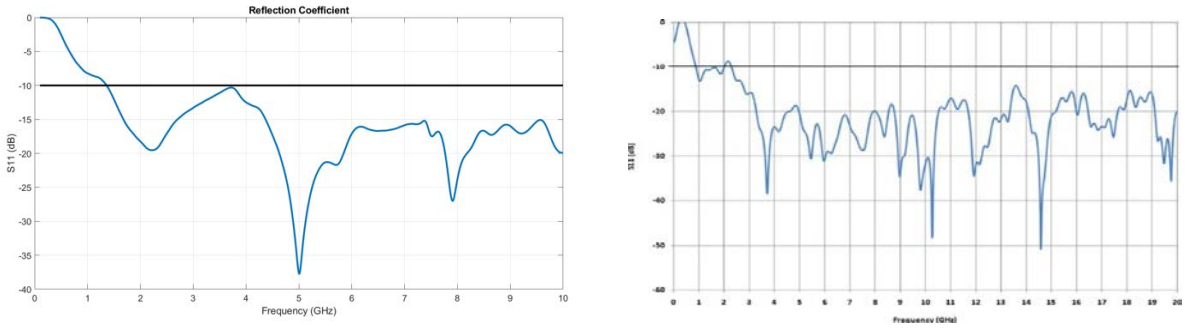


(a) (b)

Figure 5.3.1. Shark antenna design parameters: w = 40 mm, h = 40 mm, g = 4 mm, L = 148 mm, α = 56°, and β = 12°.

5.3.4 Significant Finding(s) and Mission Impact

(A) The reflection coefficient (S11) of the shark antenna has been shown to be well matched to the reference input impedance (i.e., Z_{input} = 50 Ω) from ~1.5–10 GHz (Figure 5.3.2). The max gain over frequency result is promising as well (Figure 5.3.3).



(a) **(b)**

Figure 5.3.2. S11 results (a) CST simulation (b) [1]

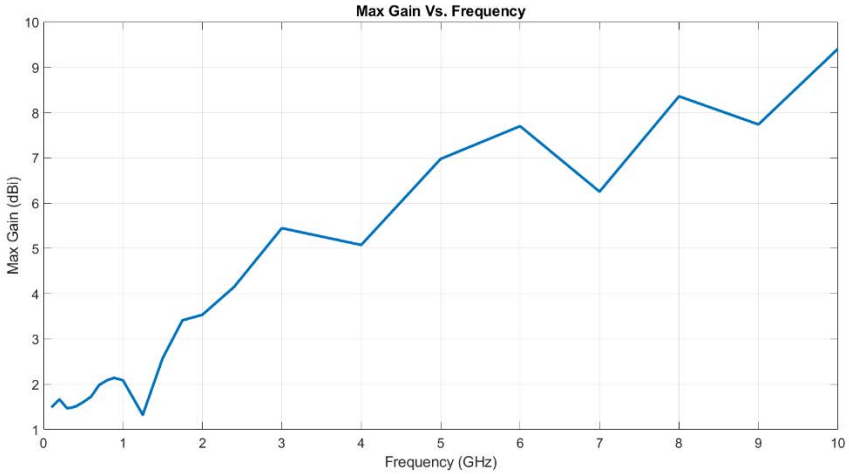


Figure 5.3.3. Gain vs. Frequency

Table 5.3.1. Antenna metrics

Antenna element type	Frequency Dependent Dimensions	Physical Aperture area	Bandwidth	Peak gain (5 GHz)	Directionality		Aperture Efficiency
					E-plane (5 GHz)	H-plane (5 GHz)	
Shark	$\frac{\lambda}{4} \times \frac{\lambda}{4} \times \frac{\lambda}{2}$	~0.00336 m^2	>10:1	7 dBi	45.7°	70.5°	42%

5.3.5 References:

[1] L. Desrumaux, A. Godard, M. Lalande, V. Bertrand, J. Andrieu and B. Jecko, "An Original Antenna for Transient High Power UWB Arrays: The Shark Antenna," in IEEE Transactions on Antennas and Propagation, vol. 58, no. 8, pp. 2515- 2522, Aug. 2010, doi: 10.1109/TAP.2010.2050418.

[2] Francisco Estêvão Simão Pereira, Maurício Henrique Costa Dias, "On the Design of Conical Antennas for Broadband Impedance Matching Performance", *International Journal of Antennas and Propagation*, vol. 2017, Article ID 1691580, 13 pages, 2017. https://doi.org/10.1155/2017/1691580

5.4 Tradespace Analysis of Ultra-Wide-Band (UWB) Fractal Antenna

(Sai Indharapu and Kalyan Durbhakula)

5.4.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. Fractal antenna packs multiple resonances closely spaced together to generate an UWB response thereby effectively utilizing the 2D space (i.e., the radiating patch space). Its high degree of freedom provides an opportunity to develop systematically modified patch shapes which in turn leads to improved bandwidth while retaining high fidelity factor values.

Sub-Problem: Fractal antennas generate omni-directional radiation pattern in H-plane.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered as the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains significantly large and has no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

Relevance to OSPRES Grant Objective: Fractal antennas satisfy the UWB criteria of the OSPRES grant objective in a compact space over other antenna elements, which usually take up significantly larger physical space over the same frequency range.

Furthermore, microstrip design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need for building a separate feed network using external and bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) Majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be considered as a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over its operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

5.4.2 Tasks and Milestones / Timeline / Status

(A) Carried out a detailed literature search on various fractal antenna elements and down selected to one particular fractal shape: hexagon patch with hexagon fractals / JAN21 / Complete.

(B) Completed initial design, simulation and preliminary validation of a coplanar waveguide feed hexagon patch antenna with and without hexagon fractals [1]. The hexagon fractals were added at the 6 sides of the hexagon patch / JAN21 / Complete.

(C) Continue with tradespace study and analysis of the hexagon patch antenna with more emphasis on parameters such as hexagon side length (a), rectangular plate dimensions (P×F), fractal element radius (b), and different fractal shapes. Demonstrate detailed tradespace study results with an emphasis on fractal element radius (b) and its effect on gain as a function of frequency, gain as a function of azimuthal angle, rE/V, and fidelity factor / FEB21-MAR21 / Ongoing.

5.4.3 Progress Made Since Last Report

(A) Detailed literature study of various fractal geometries and shapes has been carried out to deepen our understanding on fractal antennas.

(B) Initial parametric analysis of simple hexagonal patch antenna with and without fractals has been carried out. Fig. 5.4.1 shows the structure of studied fractal antenna with a hexagon patch, hexagon fractal elements at the edge of patch, transmission line feed, two rectangular plates, and a ground plane effectively forming a co-planar waveguide fed patch antenna.

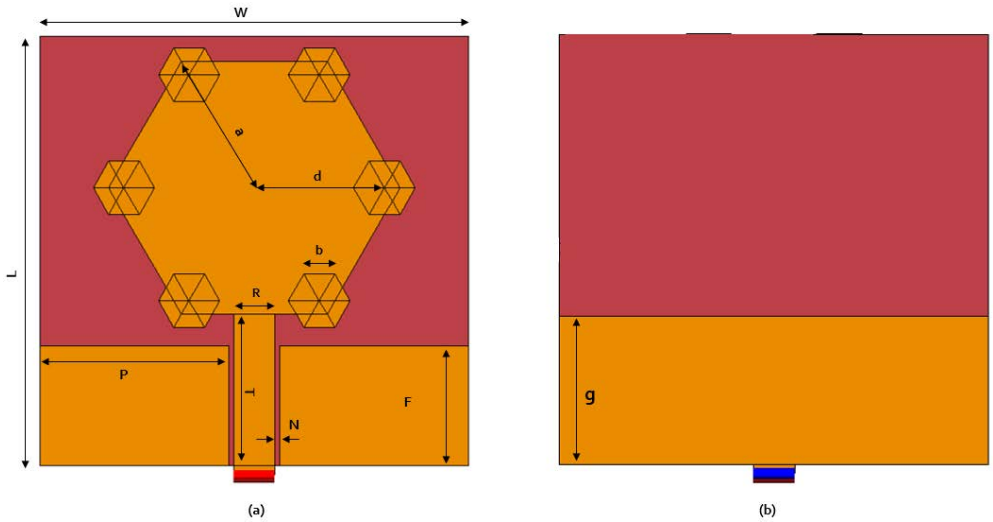


Fig. 5.4.1 Geometry of hexagon patch antenna with hexagon fractals (a)Top view (b) Bottom view. L = 25 mm, W = 25 mm, T = 8.85 mm, N = 0.3 mm, P = 11 mm, F = 7 mm, R = 2.4 mm, a = 8.5 mm, d = 7.6 mm.

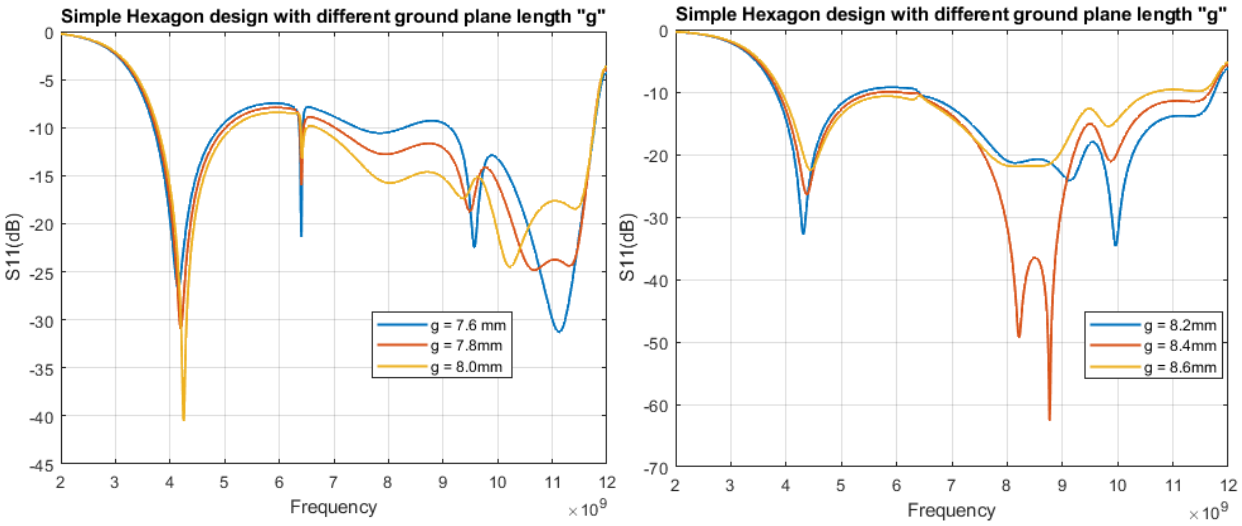
5.4.4 Significant Finding(s) and Mission Impact

(B)

(i) From our initial preliminary study of the selected geometry, the length of the ground plane has been shown to have major impact on the reflection coefficient, which can be observed from fig. 5.4.2. This observation was not reported in [1]. It is observed that increase in ground plane length up to the length of the feed line improves the return loss curve to below -10dB by which the bandwidth increases. However, further increase of ground plane length has impacted reflection coefficient negatively. We think that the further increment in ground plane length will cause disturbance to the intended radiation pattern of the hexagonal patch thereby causing a decrease in reflection coefficient. This is currently under investigation.

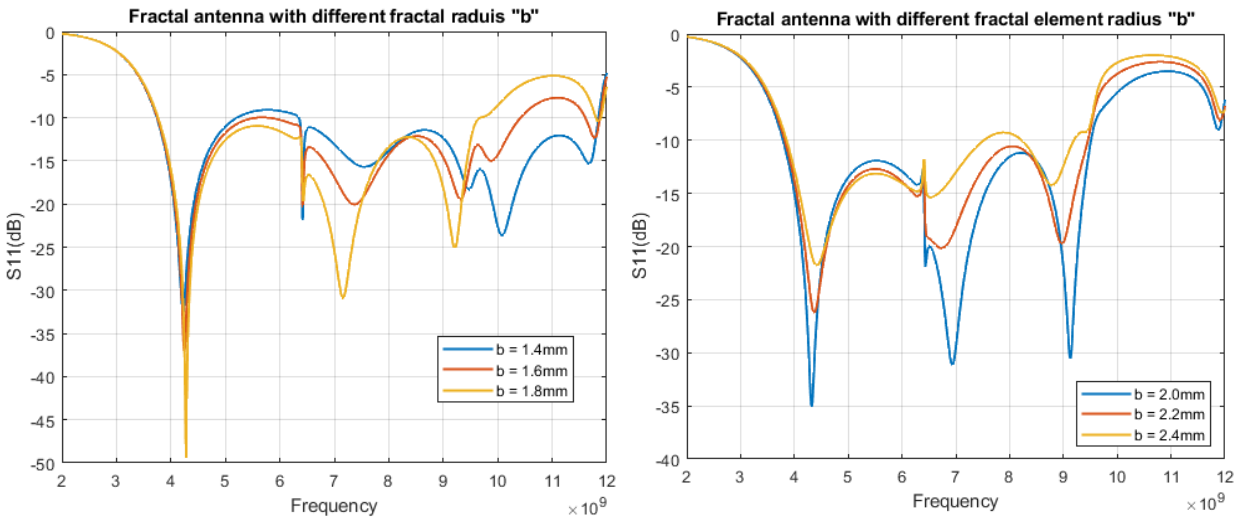
(ii) From our preliminary study of hexagon patch antenna, the increase in bandwidth is caused due to increase in closely spaced resonant frequencies which can be observed from the fig. 5.4.3. Hexagon patch antenna with hexagon fractal element radius equal to 1.8 mm yields multiple resonant frequencies with enhanced bandwidth. The higher the fractal radius (*b*) the narrower the bandwidth and vice-versa. However, it must be ensured to not make *b* too small, which leads to a dual or tri-band resonance, which are much narrower in bandwidth instead of the desired UWB.

(iii) From fig. 5.4.4a, the hexagon patch antenna with hexagon fractals shows better bandwidth over the simple hexagon patch antenna. In addition, results in fig. 5.4.4a follows the multiple resonance trend as shown fig. 5.4.4b. The difference between simulated results and results from [1] could be due to the missing information of ground plane type and its dimensions in [1]. Finally, table 5.4.1 shows the antenna metrics of the simulated hexagon patch antenna with hexagon fractals metrics at the center frequency (7 GHz).



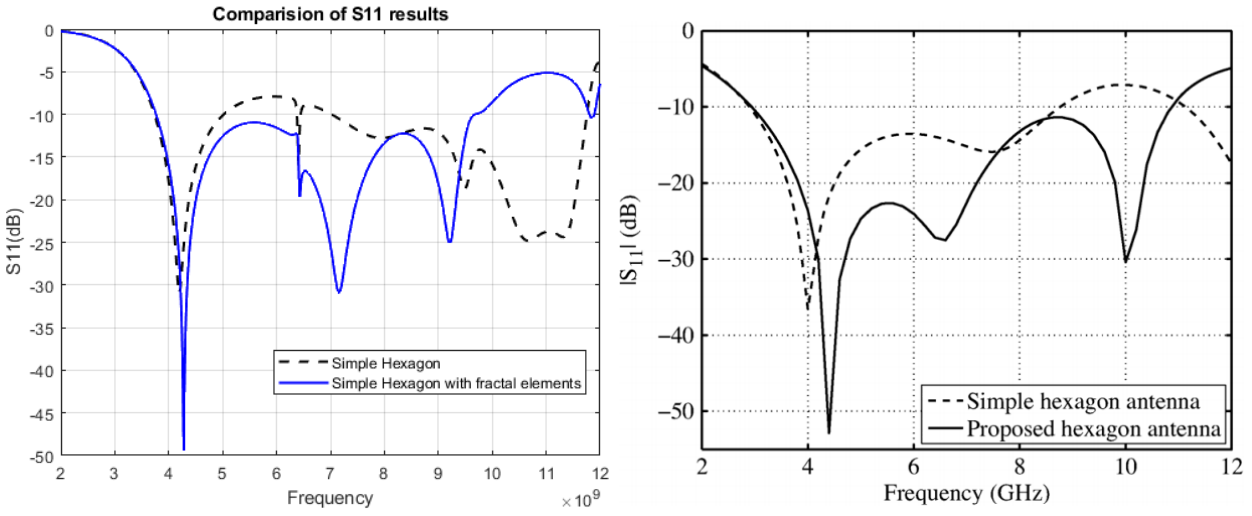
(a) (b)

Figure 5.4.2 Reflection coefficient of simple hexagon geometry with different ground plane lengths.



(a) (b)

Figure 5.4.3 Reflection coefficient of fractal antenna geometry with different fractal element radius.



(a) (b)

Figure 5.4.4 (a) comparison of S11 results with and without fractal elements for g = 7.8 mm & b = 1.8 mm (b) S11 results from the [1].

Table 5.4.1. Antenna metrics

Antenna element type	Dimensions	Physical Aperture area	Bandwidth	Peak gain (7 GHz)	Directionality		Aperture Efficiency (7 GHz)
					E-plane (7 GHz)	H-plane (7 GHz)	
Fractal antenna	25 mm × 25 mm × 1 mm	0.625 mm^2	6:1	3.5 dBi	69°	71°	50%

5.4.5 References

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

6.0 RF Coupling

6.1 Enclosure Effects on RF Coupling

(Mohamed Hamdalla and Ahmed Hassan)

6.1.1. Problem Statement, Approach, and Context

Primary Problem: Slots and gaps are introduced in casings/enclosures due to a variety of practical reasons which might compromise their shielding, creating upset susceptibility to the enclosed electronics. The goal of this work is to quantify how the thresholds for upset susceptibility of enclosed wires and integrated circuits differ from those in free space.

Solution Space: Study enclosures with different shapes, material compositions, and slots to quantify their effect on RF coupling to the enclosed wires and electronics typically used in UAVs. The study will focus on the low-frequency range where the incident wavelength is comparable to the size of the enclosure or larger.

Sub-Problem: UAVs are manufactured with a wide variety of shapes and composites to accomplish an exponentially expanding list of missions. The configurations previously reported in the literature have simplistic assumptions regarding the shape and material composition of UAV enclosures that might overestimate or underestimate susceptibility.

State-of-the-Art (SOTA): Simple statistical analysis of specific enclosure configurations using either brute force simulations/measurements or pure statistical methods.

Deficiency in the SOTA: Brute force simulations/measurements of the voltages and currents induced in wires and integrated circuits contained in enclosures is computationally or experimentally complex and have several limitations. The computations are complicated by the multiscale nature of the simulations, and the experiments are complicated by the cost of the equipment and the extensive time needed to measure every variation to cover all possible scenarios. Statistical methods, such as the Random Coupling Model (RCM) for example [1], are only accurate for high frequencies where the wavelength is much smaller than the size of the enclosure. Another main deficiency of RCM is that it can't predict the exact induced voltages and currents for a specific well-characterized system but it only provides the statistical properties of these induced currents and voltages.

Solution Proposed: Apply Characteristic Mode Analysis (CMA) to identify the fundamental modes of the enclosure, current distribution, and the field pattern of each mode. This will allow us to predict the worst-case RF coupling scenarios without the need of lengthy simulations and/or expensive experimental measurements. The proposed approach can predict measurements at a fraction of the cost/time.

Relevance to OSPRES Grant Objective: Provide general guidelines on how the environment, in this case the enclosure, affects RF coupling and subsequent electromagnetic absorption to UAV wires and integrated circuits.

Risks, Payoffs, and Challenges: The modes depend mainly on the shape and material of the enclosure. Since UAVs have a wide variety of shapes and material compositions,

a library of several UAVs needs to be studied before quantitative general conclusions can be drawn. Challenges can be mitigated by the use of the classification techniques of Machine Learning (ML). That is, different ML techniques will be evoked to detect hidden patterns on how the shape, material composition, and the shape/size location of slots correlate with the field enhancement inside the enclosure.

6.1.2 Tasks and Milestones / Timeline / Status

Task	Timeline	Milestone	Status
A. Complete the CMA implementation for studying the shielding effectiveness of metallic enclosures. Validate CMA can predict the worst-case shielding effectiveness of metallic enclosures as a function of their shapes.	2 months 11/15/2020-1/15/2021	A fast full-wave tool that facilitates studying the effect of a metallic enclosure on shielding effectiveness (1 IEEE AWPL Paper)	Completed, Manuscript for IEEE AWPL paper is being finalized
B. Use CMA tool in (A) to predict the worst-case internal field magnitude of metallic and dielectric enclosures of ten COTS UAVs as a function of HPM waveform	4 months 1/15/2021-5/15/2021	A database of worst-case internal fields shielding effectiveness results of the ten COTS UAVs as a function of their shape and HPM waveforms.	Ongoing
C. Use the database in (B) to train a Machine Learning (ML) platform to predict RF coupling to enclosed wires and electronics	5 months 5/15/2021-10/15/2021	Perform blind tests to estimate the induced internal fields of 2 COTS UAVs, not used in the training of the ML platform, and compare them with the measurement.	Ongoing

6.1.3. Progress Made Since Last Report

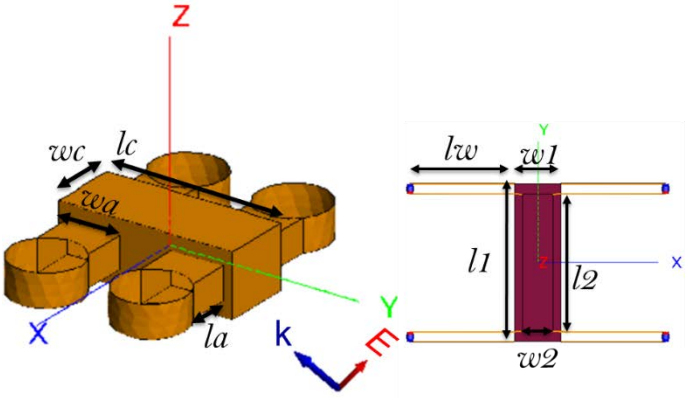
Tasks B & C:

(A) Continue the preparation of the database for different quadcopter UAVs to train a machine-learning algorithm to detect the worst-case coupling to the circuitry of the UAV.

(B) We are still investigating different approaches to extract meaningful conclusions out of the machine learning model. That is, in the last report we have shown the probability of effect in the frequency domain and didn't consider the effect of the excitation waveform. In this month we are investigating the effect of pulsed excitation on the voltages coupled to the 50 Ω loads in the circuitry.

(C) In this report, we study how varying one of the UAV's dimnsions affects the RF coupling to the enclosed circuitry. The metallic quadcopter shown in Fig. 6.1.1 shows a model of the enclosed circuitry, which is composed of four 50 Ω loads, 4 wires, and a central PCB. The loss tangent, tan δ, of the PCB's dielectric substrate is 0.01. A single angle of incidence is chosen as shown in Fig. 6.1.1 where k is the propagation direction, and E is the electric field direction. The UAV is excited with 7 different Gaussian pulses, with the same bandwidth, but with the different center frequencies of 0.6 GHz, 0.7 GHz, 0.8 GHz, 0.9 GHz, 1 GHz, and 1.1 GHz, as shown in Fig. 6.1.2a.

We typically have uncertainty in the dimensions of the UAV. Therefore, for each excitation, the quadcopter arm width w_a was varied from 10 mm to 30 mm in 5 mm steps yielding a total of 5 different arm widths. For each Gaussian pulse excitation, we calculated the probability that the load voltage will exceed an arbitrary threshold of 300 mV given the uncertainty in the arm width w_a. Different threshold values can be tested upon feedback from the effects group. That is, we calculated how many of the 5 w_a values we tested, generated a load coupled voltage that exceeds 300 mV. Fig. 6.1.2b shows that the Gaussian pulse centered at 1.2 GHz has a probability of 100% in exceeding the threshold voltage of 300 mV for all the frame dimensions. That is, at this center frequency, the RF coupling to the load is insensitive to variations in the UAV dimension w_a. At the center frequency of 0.8 GHz, only 20% of the UAV values for w_a, yield a load voltage that exceeds the threshold of 300mV. Therefore, significant coupling to the load can occur at this center frequency, but it is highly sensitive to the UAV dimensions. The analysis in Fig. 6.1.2 needs to be expanded for additional values of w_a and for additional angles of incidence. However, the preliminary analysis in Fig. 6.1.2 shows how we can identify the optimum excitations given the uncertainty in the UAV's dimensions.



Variable	Value (mm)
lw	56.5
$l1$	85
$l2$	57
lc	100
la	50
$w1$	25
$w2$	17
wc	40
wa	[10,15,20,25,30]

Fig. 6.1.1. Model of enclosed circuitry showing the wires, loads, and PCB. The table shows the dimensions of the quadcopter under study.

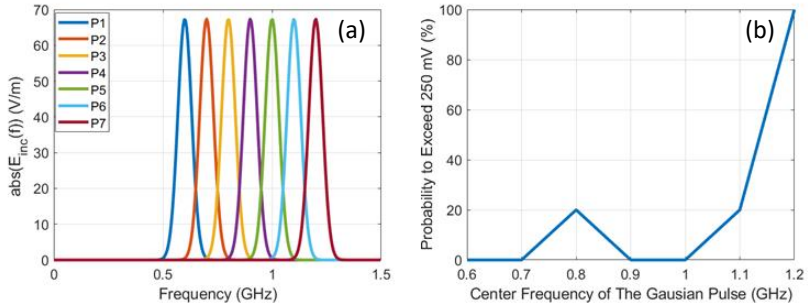


Fig. 6.1.2. (a) The Gaussian pulsed excitations centered at 7 different resonance frequencies, (b) The probability of the load voltage exceeding an arbitrary threshold of 300 mV for the 7 different Gaussian pulsed excitations

A number of future tasks have been defines for which timelines and milestones will be defined in the next report:

1. Study direct RF coupling to boards and electronic components similar to those found in UAVs. We will start this task by preparing a review of the state of the art in direct coupling to boards and electronic components.

2. Study how to extrapolate the conclusions in this MSR to non-quadcopter UAVs, e.g., fixed-wing UAVs.

3. Study simple UAV shielding mechanisms and quantify how they can affect the RF coupling to shielded boards and electronic components.

6.1.4. References

[1] G. Spadacini, T. Liang, F. Grassi, and S. A. Pignari, "Worst Case and Statistics of Waveforms Involved in Wideband Intentional Electromagnetic Attacks," *IEEE Trans. Electromagn. Compat.*, vol. 60, no. 5, pp. 1436–1444, Oct. 2018, doi: 10.1109/TEMC.2017.2778017.

7.0 Thermal Management

7.1 Jet Impingement Optimization

(Jordan Berg, Roy Allen, and Sarvenaz Sobhansarbandi)

7.1.1 Problem Statement, Approach, and Context

Primary Problem: Traditional, laminar-flow-based cooling technologies are limited in their ability to compensate average-power dissipation >1 kW (i.e., >1 GW/m^3 as cooling density) – specifically, the thermal load byproduct – of HPM-based sources within electronically-steered arrays.

Solution Space: Utilize novel cooling technologies which employ non-laminar flow regimes (i.e., jet impingement thermal management system, JI-TMS).

Sub-Problem: An order-of-magnitude greater fluid flowrate and two orders greater pressure drop is required over traditional techniques (10 gpm vs. 1 gpm, and 100's-of-psi vs. 1's-of-psi) without increasing SWaP-cost.

State-of-the-Art (SOTA): High-power electronics employing JI-TMS's have achieved 10's-of-kW of average power handling capabilities using 20 °C dielectric coolant and sub-mm jet diameters while consuming equivalent power to deliver the fluid to the JI-TMS.

Deficiency in the SOTA: Chiller/pump systems consumption of power to produce thermal compensation, extreme pressures (100's-of-psi) to achieve optimal flowrate performance and cooling metrics, low SWaP-C^2 fidelity for Navy afloat missions.

Solution Proposed: Develop a JI-TMS able to compensate average-power dissipation >1 kW while maintaining the HPM-sources' solid-state heat source <80 °C, by flowing dielectric fluid at turbulence-inducing flow rates while not exceeding 100's-of-psi within the system.

Relevance to OSPRES Grant Objective: Increased cooling performance facilitates HPM sources' higher average-power operation (>1 kW) deeming specific-power-densities (>1 W/cm^2) at distances >2 km achievable.

Risks, Payoffs, and Challenges: High pressures and larger chiller-pump systems, minimizing pressure drop requirements while maintaining or improving performance increases cooling form-factor (>1 GW/m^3), 5× that of traditional cooling techniques.

7.1.2 Tasks and Milestones / Timeline / Status

(A) Initial design of JI-TMS-V1 proposed and simulated using Si-PCSS source's laminar-flow TMS as baseline / 1-year, 4-months or MAY18–OCT19 / initial design–simulation phase completed.

(B) Revised JI-TMS-V1's design (JI-TMS-V2), simulation of parametric study performed, prototype developed and experimentally evaluated / 2-months or DEC19 / establishing design's baseline accomplished.

(C) Design changes applied to JI-TMS-V2 to decrease flowrate and pressure drop requirement / 9-months or SEP20 / design optimization phase completed.

(D) Complete redesign (JI-TMS-V3) of system to increase average-power handling capabilities (>1 kW) by increasing flowrate and convective heat transfer (>40 kW/m·K) without increasing system's volume (~100 cm^3) / 4-months or DEC20 / design phase-II complete.

(E) Finalize remaining numerical analysis tradespace study of current JI-TMS design and compile research into academic research journal article for submission / 2-months or DEC20 / Downselect JI-TMS as viable option for thermal mitigation phase in-progress.

(F) Create outbrief report summary of JI-TMS-V3. This report will detail the performance metrics, testing and experimental results achieved, along with the reasons for downselecting the JI-TMS-V3.

7.1.3 Progress Made Since Last Report

(E) Journal article for submission to International Journal of Heat and Mass Transfer completed (see Section 8.5 for details). Current JI cooling topology downselected to not be viable option for continuation.

7.1.4 Significant Finding(s) and Mission Impact

The JI-TMS-V3 design's ability to compensate 0.2 kW (i.e., >200 MW/m^3) average power and maintain the Si-PCSS source's average temperature at 50 °C is 10 °C less than the laminar-flow-based design of equivalent volumetric form-factor (cross-flow thermal management system) – currently used for the OSPRES Contract's source array demonstrator. The analysis of the optimized geometry and dielectric fluid restriction is performance limited (without dramatically increasing system pressures). Further iterations of the current design are unlikely to dissipate the stretch goal cooling requirement of >1 kW (1 GW/m^3) due to the large pressure drop that occurs. While jet impingement as a method of heat transfer is still considered a viable method, the viscosity of the fluid presented a challenge in being able to create turbulent regimes in the JI-TMS. To overcome this challenge, decreasing the JI-TMS nozzle diameters by a factor of 10 and increasing the nozzle count by the same has the potential to increase convection of the coolant, thereby increasing heat extraction capabilities.

7.2 Nanofluid Heat Transfer Fluid Development

(Jordan Berg, Roy Allen, and Sarvenaz Sobhansarbandi)

7.2.1 Problem Statement, Approach, and Context

Primary Problem: Dielectric fluids (non-conductive coolant) used in thermal management systems, while suitable for high-voltage HPM-based technologies, possess inherent thermophysical fluid properties (low thermal conductivity, high viscosity) that inhibit their ability to achieve > 1 GW/m^3 cooling densities.

Solution Space: Develop a nanofluid by entraining ceramic nanoparticles and dispersants within the dielectric base-fluid, pure silicon fluid (PSF), to increase the nanofluid's thermophysical properties and cooling density capabilities with a similar form-factor.

Sub-Problem: While the dynamic viscosity of the dielectric fluid used, PSF-20cSt, is 'low' relative to other silicone-based fluids, it is ~15 times more viscous than water, and therefore requires increased pumping power within the TMS. Compounding this issue is the necessity to increase the flowrate of the fluid to achieve an equivalent heat removal rate compared to that of a water-based coolant.

State-of-the-Art (SOTA): Nanofluids, with optimal ratios of fluid-to-nanoparticles, have been shown to increase the thermal conductivity of dielectric fluids by 87% in comparison to the generic dielectric fluid alone; resulting in either greater cooling density, decreased pumping power, or reduced mass flow rate requirements.

Deficiency in the SOTA: The addition of nanoparticles within a base-fluid results in a tradeoff between one or more thermophysical properties. For example, adding nanoparticles may increase thermal conductivity of the nanofluid but may result in increased viscosity; i.e., heat removal rate may increase, but the required pumping power along with it. To the best of our knowledge, no one has attempted to create a nanofluid mixture with a goal of keeping the viscosity low. Therefore, the optimal nanoparticle-to-fluid ratio and specific nanoparticle type for the HPM thermal management systems needs to be identified and optimized with an attempt to maintain the viscosity of the mixture as low as possible.

Solution Proposed: Develop a nanofluid with both desirable thermal properties and a relatively low viscosity that is viable for TMSs in HPM topologies. Utilize systematic numerical and experimental strategies to evaluate a large sample set of various nanoparticles (with surfactants and dispersants).

Relevance to OSPRES Grant Objective: Increase cooling densities for HPM systems without requiring TMS design permutations while decreasing pumping power requirement which are in-line with the SWaP-C^2 objective.

Risks, Payoffs, and Challenges:

Risk: The pressures incurred by using a silicone-based fluid in a high-flow regime are not insignificant; large pump-chiller systems may still be necessary.

Challenges: Creating low volume-fraction samples of nanoparticles and surfactants is near equipment precision limit. Maintaining accuracy is critical to properly study modified fluids.

Payoff: A modified nanofluid dielectric fluid can be used to increase cooling capacity of any high-power density system. An optimized nanofluid has the potential to extract 20% up to several factors more than the base fluid.

7.2.2 Tasks and Milestones / Timeline / Status

(A) Measure thermophysical properties of currently utilized PSF-20cSt;

Timeline: DEC20–JAN21

Status: completed.

(B) Establish theoretical model of nanofluid compositions;

Timeline: DEC20–JAN21

Status: completed.

(C) Create and test modified PSF-20cSt with Nanoparticles and surfactants;

Timeline: JAN21–MAR21

Status: In progress.

(D) Select the nanofluid mixture with high thermal properties and re-evaluate the CFD modeling;

Timeline: MAR21–APR21

Status: TBD.

7.2.3 Progress Made Since Last Report

This new section has been added to the MSR which summarizes the work done over the last 2 months on a heat transfer fluid performance modification project.

7.2.4 Significant Finding(s) and Mission Impact

Based on literature, the creation of a dielectric nanofluid for use as a coolant in the HPM system could potentially improve cooling performance. The thermal dissipation requirements for HPM systems are not insignificant and could, therefore, benefit from performance enhancement from every aspect (geometric optimization, reduction of thermal resistances, coolant selection, material selection, etc.).

(A) A sample of the PSF-20cSt that was used in the experimental testing of the JI-TMS was tested with a differential scanning calorimeter (DSC). The specific heat of the fluid was found to significantly differ from that of the manufacturer's value. The vendor's reported value of the PSF-20cSt was 1.6 $\frac{J}{gC}$, while DSC measurements showed it to be closer to 1.1 $\frac{J}{gC}$. This difference hinders the accuracy of the CFD results of CFD models.

(B) Given the aforementioned error in specific heat capacity, along with the need for a high thermal performance coolant, nanoparticle-modified PSF-20cSt was determined to be a necessary and useful undertaking. Three different ceramic nanoparticles were chosen to be studied: Alumina, Silicon Carbide, and Iron(II,III) Oxide. Ceramics were chosen to maintain HTF dielectric properties.

(C) Two sample sets have been prepared in various low mass-fraction quantities (0.25 wt%, 0.5 wt%, and 0.75 wt% of each). The different sets were created such that one set that includes surfactants and one set that is purely NP's and PFS-20cSt. The surfactants are intended to aid in a homogeneous mixture. The total number of samples is 19, including the control.

Once the samples are tested, the hope is our team creates a dielectric low-viscosity nanofluid that functions as an ideal heat transfer fluid for the HPM system and other high power density applications.

8.0 Program Management

8.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

8.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

8.3 Major Procurement Actions

i. Microsoft Office 365 GCC High (75 seats) - $45,000 (for OSPRES Contract CUI Compliance)

8.4 Travel

Destination	Purpose	Attendees	Estimated Costs

8.5 Pending or Upcoming Public Release Requests

i. J. N. Berg, R. C. Allen, and S. Sobhansarbandi, CFD Modeling and Experimental Implementation of a Novel Thermal Management System for a Semiconductor Device [Unpublished manuscript], Int J Heat Mass Transf, pp. 1-12, 2021.

9.0 Appendix A – Academic and IP Output

(Please note that this section is still being updated).

9.1 Conference Publications

[1] W. Azad, S. Roy, and F. Khan, "A Single Gate Driver-based Four-stage High-voltage SiC Switch Having Dynamic Voltage Balancing Capability," submitted in *2021 IEEE Applied Power Electronics Conference and Exposition* (APEC), Phoenix, AZ, USA, June 9-12, 2021.

[2] J. Hunter, S. Xia, A. Harmon, A. M. Hassan, V. Khilkevich, and D. Beetner, "Modeling and Statistical Characterization of Electromagnetic Coupling to Electronic Devices," *IEEE International Symposium on Antennas and Propagation and NSRM USNC-URSI National Radio Science Meeting*, Boulder, CO, January 4-9, 2021.

[3] W. Azad, S. Roy, and F. Khan, "A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver," accepted in *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, 2020.

[4] B. Barman, K. C. Durbhakula, B. Bissen, D. Chatterjee, and A. N. Caruso, "Performance Optimization of a Microstrip Patch Antenna using Characteristic Mode and D/Q Analysis," *2020 XXXIIIrd General Assembly and Scientific Symposium of the International Union of Radio Science*, Rome, Italy, Aug 29 - Sept 5, 2020, pp. 1-4 (online conference).

[5] B. Barman, D. Chatterjee, and A. N. Caruso, "Performance Optimization of Electrically Small Microstrip Patch Antennas on Finite Ground Planes," 2020 *IEEE International Symposium on Antennas and Propagation and North American Radio Science Meeting*, Montreal, Quebec, Canada, July 5-10, 2020, pp. 1–2 (online conference).

[6] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, "Scalable Characteristic Mode Analysis: Requirements and Challenges (White Paper)," *Large Scale Networking (LSN) Workshop on Huge Data: A Computing, Networking and Distributed Systems Perspective Sponsored by NSF*, Chicago, IL, April 13-14, 2020.

[7] M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Predicting Electromagnetic Interference to a Terminated Wire Using Characteristic Mode Analysis," *Proceedings of the Annual Review of Progress in Applied Computational Electromagnetics (ACES)*, Monterey, CA, March 22-26, 2020.

[8] W. Azad, F. Khan, and A. Caruso, "Self-sustaining High-power RF Signal Generation Using LDMOS Based Power Amplifier and Nonlinear Transmission Line," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 3567-3572 [doi].

[9] A. Hanif, W. Azad, and F. Khan, "Detection of Bond Wire Lift Off in IGBT Power Modules Using Ultrasound Resonators," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 345-350 [doi].

[10] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, “Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS,” *Annual Directed Energy Science and Technology Symposium*, March 2020 (abstract appeared, but talk cancelled due to pandemic).

[11] B. Barman, D. Chatterjee, and A. N. Caruso, “Some Investigations into Mutual Coupling Analysis for Trade Space Studies of Linear Arrays,” *2019 IEEE International Symposium on Phased Array Systems and Technology (PAST)*, Waltham, MA, October 2019, pp. 1-8.

[12] B. Barman, D. Chatterjee, and A. N. Caruso, “Characteristic Mode Analysis of a straight and an L-probe fed Microstrip Patch,” *2019 IEEE Indian Conference on Antennas and Propogation (InCAP)*, Ahmedabad, India, Dec 2019, pp. 1-3.

[13] M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of the Effect of the UAV Frame Material on Coupling and Interference," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019.

[14] M. Hamdalla, J. Hunter, Y. Liu, V. Khilkevich, D. Beetner, A. Caruso, and A. M. Hassan, "Electromagnetic Interference of Unmanned Aerial Vehicles: A Characteristic Mode Analysis Approach," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019.

[15] B. Barman, D. Chatterjee, and A. N. Caruso, “Analytical Models for L-Probe fed Microstrip Antennas,” *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

[16] K. C. Durbhakula, J. Lancaster, J. Hunter, Y. Liu, D. Beetner, V. Khilkevich, D. Chatterjee, A. N. Caruso, and A. M. Hassan, "Electromagnetic Coupling Analysis of Printed Circuit Board Traces using Characteristic Mode Analysis," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (2 pages)*, Atlanta, Georgia, USA, July 7-12 2019.

[17] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “On the Location of Transverse Electric Surface Wave Poles for Electrically Thick Substrates,” Proceedings of the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019.

[18] M. Hamdalla, B. Bissen, A. N. Caruso, and A. M. Hassan, “Experimental Validations of Characteristic Mode Analysis Predictions Using GTEM Measurements,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Montréal, *Québec, Canada, July 5-10, 2020*.

[19] W. Azad and F. Khan, “Sustaining High-power RF Signal Generation in a Positive Feedback Network," *2019 IEEE Pulsed Power and Plasma Science Conference (PPPS)*, Orlando, FL, USA, June 23-28 2019.

[20] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, “Scalable characteristic mode analysis using big data techniques,” *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[21] M. Hamdalla, W. Al-Shaikhli, J. Lancaster, J. D. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of Electromagnetic Coupling to Wires with Realistic Shapes," *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[22] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "Location of Surface Wave Poles in Sommerfeld Integrals: A Mittag-Leffler Expansion Approach," *Proceedings of the URSI-B International Symposium on Electromagnetic Theory*, URSI Commission, San Diego, USA, May 2019.

[23] D. Chatterjee, B. Barman. J. Kovarik, and A. N. Caruso, "Studies on Antenna Characterization and Propagation of High Power Pulsed Electromagnetic Waves with Minimal Spatial Dispersion," presented at the *Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium*, Destin, Florida, USA, April 2019.

[24] J. Kovarik, B. Barman, D. Chatterjee and A. N. Caruso, "Some Investigations into Applications of Electrically Small Antennas as Phased Array Elements," presented at the *Directed Energy Professional Society* (DEPS) *Annual Science and Technology Symposium*, Destin, Florida, USA, April 2019.

[25] K. C. Durbhakula, D. Chatterjee and A. M. Hassan, "Analytical Evaluation of Sommerfeld Integral Tails Present in Two-layered Media Green's Functions," *Proceedings of the Indian Conference on Antennas and Propagation* (InCAP), Hyderabad, India, December 2018.

[26] D. Beetner, V. Khilkevich, A. M. Hassan, J. Hunter, Y. Liu, and D. Floyd, "Characterization of the Electromagnetic Coupling to UAVs," *DE Systems Symposium*, September 24-27, 2018

[27] C. Hartshorn, K. Durbhakula, D. Welty, D. Chatterjee, J. Lancaster, A. M. Hassan, and A. N. Caruso, "Crosstalk and Coupling to Printed Circuit Board Metallic Traces with Arbitrary Shapes," *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[28] M. Hamdalla, J. Roacho-Valles, J. Hunter, D. Beetner, A. M. Hassan, and A. N. Caruso, "Electromagnetic Analysis of Unmanned Aerial Vehicles Using Characteristic Mode Analysis," *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[29] C. Hartshorn, M. Hamdalla, J. Lancaster, A. M. Hassan, and A. N. Caruso, "Electromagnetic Vulnerability of Wires with Arbitrary Shape," *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[30] K. C. Durbhakula, D. Chatterjee, A. M. Hassan, and M. S. Kluskens, "Studies on Numerical Evaluation of Sommerfeld Integrals for Multilayer Topologies," *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018.

[31] J. Lancaster, D. Chatterjee, and A. N. Caruso, "Some Investigations into the Dispersion Characteristics of Localized Bessel Beams," published in the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018 (1 page URSI Abstract).

[32] M. Hamdalla, A. M. Hassan, and A. N. Caruso "Characteristic Mode Analysis of Unmanned Aerial Vehicles with Realistic Shapes and Material Composition," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Boston, MA, July 8-13, 2018.

[33] W. Azad, S. Roy, A. S. Imtiaz, and F. Khan, "Microelectromechanical System (MEMS) Resonator: A New Element in Power Converter Circuits Featuring Reduced EMI," *2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, Niigata, May 20-24, 2018, pp. 2416-2420 [doi].

[34] J. Hunter, Y. Liu, D. Floyd, A. Hassan, V. Khilkevich, and D. Beetner, "Characterization of the Electromagnetic Coupling to UAVs," Annual Directed Energy Science and Technology Symposium, Feb 26-March 2, 2018.

9.2 Journal Publications

9.2.1 In Preparation

[1] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, CFD Modeling and Experimental Implementation of a Novel Thermal Management System for a Semiconductor Device, *Int J. Heat Mass Transf*, pp. 1-12, In Preparation, **2021**.

[2] W. Azad, F. Khan, and A. N. Caruso, "A Series-connected High-voltage SiC Switch Driven by a Compact High-voltage Isolated Gate Driver," In preparation, **2021.**

[3] M. Z. M. Hamdalla, B. Bissen, J. D. Hunter , L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Experimental Evaluation of CMA Predictions and Control of Electromagnetic Interference to UAVs," In Preparation, **2021**.

[4] S. Xia, J. Hunter, A. Harmon, M. Hamdalla, A. Hassan, V. Khilkevich, D. Beetner, "Simulation Driven Statistical Analysis of the Electro-magnetic Coupling to Microstriplines," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[5] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, "Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field Coupling to Randomly Shaped Wires," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[6] W. Azad, F. Khan, and A. N. Caruso, "A Medium Power, Self-Sustaining, Configurable RF Pulse Generation Circuit Using a Nonlinear Transmission Line and Power Amplifier in a Closed Loop Configuration, In Preparation, **2020**.

9.2.2 Submitted / Under Revision

[7] Khulud Alsultan, Mohamed Hamdalla, Sumitra Dey, A. N. Caruso, Praveen Rao, and A. M. Hassan, "Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform," *IEEE Open Journal of Antennas and Propagation,* Submitted, **2020**.

[8] John Keerthi Paul Bhamidipati, Eliot R. Myers, Adam M. Conway, Lars F. Voss, and Anthony N. Caruso, “Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches,” *IEEE Transactions on Electronic Devices*, Under Revision, **2020**.

[9] W. Azad, F. Khan, and A. Caruso, "A Medium Power, Self-sustaining, Configurable RF Pulse Generation Circuit Using Nonlinear Transmission Line and a Power Amplifier in Closed Loop Configuration,” *IEEE Transaction on Plasma Science*, Submitted, **2020**.

[10] S. Roy, W. Azad, S. Baidya and F. Khan, “A Comprehensive Review on Rectifiers, Linear Regulators and Switched-mode Power Processing Techniques used for Powering Biomedical Sensors and Implants inside Human Body,” *IEEE Transactions on Power Electronics*, Submitted, **2020**.

[11] S. Roy, W. Azad, S. Baidya, M. Alam and F. Khan, “Powering Solutions for Biomedical Sensors and Implants inside Human Body–A Comprehensive Review on Energy Harvesting Units, Energy Storage, and Power Transfer Circuits,” *IEEE Transactions on Power Electronics*, Submitted, **2020**.

9.2.2 Published / In Press

[12] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems,” *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364-373, **2019**.

9.3 External Presentations/Briefings

DEPS Posters and Presentations 2020

[1] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[2] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

GOMAC 2019

[3] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[4] Eliot Myers, Picosecond High Power Switching Technologies

[5] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

DEPS Posters and Presentations 2019

[6] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[7] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[8] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[9] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[10] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[11] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[12] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[13] Deb Chatterjee, Studies On Antenna Characterization And Propogation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

DEPS Posters and Presentations 2018

[14] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[15] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[16] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

DEPS Posters and Presentations 2017

[17] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

9.4 IP Disclosures Filed

Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, 19UMK005, 28SEPT2018

Doynov, “Pulse Differential High-power Microwave Generation”, 19UMK007, 02JAN2019.

Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal”, 19UMK008, 28DEC2018.

Doynov, Caruso, “High-efficiency High-power Microwave Generation using Multipass Non-linear Network Topologies”, 19UMK017, 29AUG2020.

Doynov, “Scalable Modular System for High-power Microwaves Generation”, 20UMK010, 19APR2020.

Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna”, 20UMK011, 19APR2020.

Shepard, “A Novel Optical Fiber Amplifier”, 20UMK012, 02JUN2020.

Shepard, “A Low Noise Optical Amplifier”, 21UMK007, 14SEPT2020.

9.5 Provisional Patents Filed

Doynov, Caruso, “High-efficiency High-power Microwave Generation using Multipass Non-linear Network Topologies”, filed 26NOV2019.

9.6 Non-Provisional Patents Filed

None to date

ONR HPM Program - Monthly Status Report (MSR) – FEB 2021

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 MAR 2021

Distribution Statement ~A: Distribution authorized to all OSPRES Grant and Contract performers, and any OSPRES uncompensated collaborators. Further dissemination per the Office of Naval Research, Ryan Hoffman (ryan.hoffman@navy.mil, 703-696-3873) or higher DoD Authority.

OSPRES Grant Goal: address and transition technologies and capabilities that enable the OSPRES Grant Objective using the OSPRES Grant Approach, while educating the next generation of pulsed power and defense minded, stewards and innovators.

OSPRES Grant Objective: to execute high-risk, high-payoff efforts that mitigate, fill or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable and electronically steerable high power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average power space, and includes the kill chain considerations including the target and its responsivity to radiofrequency stimuli.

OSPRES Metrics of Success: developed technologies and capabilities that are published in the peer review, protected as intellectual property, and/or, transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use, as enabling/integratable capability(ies).

OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

OSPRES Grant Security: All efforts should be fundamental and publically releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

1.0 Contents

2.0 Executive Summary 4
2.1 Progress, Significant Findings, and Impact 4
2.2 Completed, Ongoing, and Cancelled Sub-Efforts 5
2.3 Running Total of Academic and IP Program Output 6
3.0 Switch Evaluation and Innovation 7
3.1 Lasers and Optics 7
3.2 WBG-PCSS Enabled Laser Diode Array Driver 9
3.3 Diode-Based NLTLs 11
3.4 Si-PCSS Top Contact Modeling and Optimization for Cooling Requirements 15
3.5 GaN:C PCSS Direct RF Modulation 21
3.6 Bistable Operation of GaN 23
3.7 Drift-Step Recovery Diode Optimization 26
4.0 Prime Power and Conditioning 36
4.1 HV Switch Pulsed Chargers 36
5.0 Tradespace Analysis of Ultra-Wide-Band Antenna Arrays 41
5.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs) 41
5.2 Tradespace Analysis of Other Ultra-Wide-Band (UWB) Single Elements 44
5.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna 51
5.4 Tradespace Analysis of Ultra-Wide-Band (UWB) Fractal Antenna 58
6.0 RF Coupling 65
6.1 Enclosure Effects on RF Coupling 65
7.0 Thermal Management 70
7.1 Micro-Jet Thermal Management System 70
7.2 Nanofluid Heat Transfer Fluid Development 70
8.0 Program Management 73
8.1 Issues 73
8.2 Interactions with Others 73
8.3 Major Procurement Actions 73
8.4 Travel 73
8.5 Pending or Upcoming Public Release Requests 73
9.0 Appendix B: Academic and IP Output 74
9.1 Students Graduated 74
9.2 Conference Publications 74
9.3 Journal Publications 77

9.4 External Presentations/Briefings 78
9.5 IP Disclosures Filed 79
9.6 Provisional Patents Filed 80
9.7 Non-Provisional Patents Filed 80
10.0 Appendix B: Si-, SiC- and GaN Modeling and Evaluation 81
10.1 Executive Summary 81
10.2 Objective 81
10.3 Technical Background 82
10.4 Tasks, Milestones, and Status 83
10.5 Methods and Approach 85
10.6 Results and Discussion 86
10.7 Summary and Recommendations 92
10.8 Outputs 93
10.9 References 93

2.0 Executive Summary

2.1 Progress, Significant Findings, and Impact

Feasibility calculations of a multi-stage laser diode array (LDA) show that with lock-on conduction mode achieved, the monetary system cost should reduce by 10–12% of a conventional comparator laser system, and reduce the overall volume of the optical subsystem by 90%. Further, inducing lock-on operation at low electric fields (~3–3.5 kV/cm) potentially reduces the risk of high jitter at ~MHz order pulse repetition rates (PRR) and negative current due to ringing during recovery, mitigating the need for a snubber circuit. In turn, achieving 72 mΩ on-state resistance (calculated) while operating PCSS in lock-on mode at low voltages (50-μm device at ~17.5 V bias) reduces the power dissipation (0.08 μJ/pulse), resulting in reduced cooling system requirements. The implication is an optimal middle ground between the best attributes of linear and avalanched based PCSS technologies.

The Si, SiC, and GaN modeling effort is shifting to an indefinite pause state (lowest priority relative to other projects); a summary of the work to date is provided in Appendix B.

The jet impingement thermal management system work is sunset. A summary of this major effort is under revision and will be provided in next month's report.

A new effort on the fundamental development of drift-step recovery diode based pulsed power has been added. The results reported here are in complement to those presented in the OSPRES contract report, and the overall fundamental-applied group works hand-in-hand. The primary objective is to allow for a deeper and more rigorous study of the fabrication, doping, and transient response of the die.

A comparison of important antenna metrics between the originally published/designed Koshelov antenna and our aperture reduced Koshelov antenna variant show that with a 50% physical aperture area reduction, a minimal and potentially acceptable tradeoff in bandwidth (200-MHz in 4.5-GHz) and peak gain (from 9.4- to 7.7-dBi) occur. In addition, by reducing the physical aperture area (0.08- to 0.04-m^2), the aperture efficiency (80 to 100%) and rE/V (1.25 to 1.6) have improved.

The RF coupling group revisited the frequency step in their simulations and found additional resonances in PEC enclosures. Conversely, it was shown that RF coupling to enclosed circuitry is insensitive to the exact dimensions and properties of dielectric enclosures; from this conclusion the group developed approximate but fast RF coupling guidelines, further reducing the computational time, similar to that asked for in the DARPA WARDEN requirements.

A 50% increase (800 to 1200-V) in direct RF modulation of GaN:C PCSS using a 500 μm gap length was achieved. Next month, we will report back on a 1000 μm gap length.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

	Start	End
2.2.1 Ongoing Sub-Efforts		
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
HV Switch Pulsed Chargers	DEC 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Enclosure Effects on RF Coupling	OCT2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
Nanofluid Heat Transfer Fluid	NOV 2020	Present
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization	JAN 2021	Present
Bistable Operation of GaN	FEB 2021	Present
2.2.2 Completed Sub-Efforts		
Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
2.2.3 Cancelled/Suspended Sub-Efforts		
Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020
Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021

2.3 Running Total of Academic and IP Program Output

See Appendix A for authors, titles and inventors (this list is continuously being updated)

2.3.1	*Students Graduated*	6 BS, 5 MS, 2 PhD
2.3.2	*Conference Publications*	34
2.3.3	*Journal Publications*	1 (5 submitted/under revision)
2.3.4	*External Presentations/Briefings*	18
2.3.5	*IP Disclosures Filed*	8
2.3.6	*Provisional Patents Filed*	1
2.3.7	*Non-Provisional Patents Filed*	0

3.0 Switch Evaluation and Innovation

3.1 Lasers and Optics

(Scott Shepard)

3.1.1 Problem Statement, Approach, and Context

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$50K to \$5M.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution. This way of implementing an optical fiber laser (via an optical fiber amplifier) has SWaP advantages with respect to traditional (fiber and free-space) laser designs.

Sub-Problem (1): Optical pump power system costs are the dominant source of costs (in both normal/free-space lasers and in optical fiber lasers, of this class).

Sub-Problem (2): Amplified spontaneous emission (ASE) and fiber nonlinearities impede the optical amplifier performance.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive until reduced by a factor of two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping scheme which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments we are pursuing the use of gain saturation and a staged design of different fiber diameters.

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system needed to drive the PCSS will meet the modular and scalable volume and cost aim-points.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability.

3.1.2 Tasks and Milestones / Timeline / Status

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Ongoing.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Ongoing.

(E) Demonstrate a cost-reduced fiber laser. / Ongoing.

(E1) Finalize design. / MAR2021
(E2) Assemble and test-check seed LDs/drivers. / APR2021
(E3) Measure power vs current transfer function of seed LDs/drivers. / APR2021
(E4) **May–June 2021** Measure ASE and jitter of 1064 nm seed LD/driver.
(E5) **May–June 2021** Measure ASE and jitter of 1030 nm seed LD/driver.
(E6) **May 2021** Assemble and test-check pump LDs/drivers.
(E7) **May 2021** Measure power vs current transfer function of pump LDs/drivers.
(E8) **May 2021** Splice power combiners to Yb doped preamp fiber.
(E9) **May 2021** Connect seed and pumps to power combiners and test-check.
(E10) **June–July 2021** Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle.
(E11) **June–July 2021** Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle.
(E12) **July 2021** Splice power amplifier and its power combiner to best preamp.
(E13) **July–August 2021** Measure gain, ASE and jitter of entire amp assembly.
(E14) **July–August 2021** Analyze data and document.

3.1.3 Progress Made Since Last Report

(E1) The map between the unsaturated/initial fiber gain (per meter) and Yb dopant concentration was resolved. Now accurate calculation of the lengths of doped fiber required and the amount of nonlinear impairments we might expect for various amplifier system gains. This progress enabled the incorporation of gain saturation effects and nonlinearities into the optical pre-amp and optical power amp designs.

3.1.4 Significant Finding(s) and Mission Impact

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with tolerable pre-burst ASE. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E1) Detailed design progress was made as follows. Although there will be further developments, at this stage we can proceed with the ordering of parts. In particular, our

gain saturation model/simulations enabled the design of a pre-amp (of gain = 1000 in a 20 micron diameter core) in a length of 2.4 [m] and a poweramp (of gain = 12.5 in a 25 micron diameter core) in a length of 5.3 [m]. These resulted in an entire amplifier ASE suppression factor of 237.572 (which is admirable). For these lengths and mode areas the threshold powers for the nonlinear impairments of stimulated Brillouin scattering (SBS) and stimulated Raman scattering (SRS) turned out to be (for the poweramp) 39 W – sufficiently above our average power of 10 W – and 14.8 kW – sufficiently above our peak power of 10 kW. Similarly, the pre-amp SBS and SRS threshold powers (55 W and 21 kW) are sufficiently above our operating powers. This is very good news. We do not anticipate any complications from SBS nor SRS in our proof-of-concept experiment. I also recently incorporated pump depletion into the model/simulation (although it will not affect the SBS/SRS result). I found that with bi-directional pumping in the pre-amp, the desired length of 2.4 [m] increased only to 2.9 [m]. With forward pumping alone however, the fiber losses at the signal wavelength make it so that no length of fiber can compensate for the pump depletion losses and hit the desired gain at the pump power used. Fortunately however, the dopant concentrations of our preferred vendor's fiber are sufficient for us to increase the pump power and still achieve the gain of the initial design. Nevertheless, we anticipate that bi-directional pumping in the pre-amp will be advantageous. The bottom-line is that we now are confident that we can proceed to the final ordering of parts.

3.2 WBG-PCSS Enabled Laser Diode Array Driver

(John Bhamidipati)

3.2.1 Problem Statement, Approach, and Context

Primary Problem: Need for heavy (~125 lbs.), bulky (~10 cu-ft), and expensive (~$120,000) conventional laser systems (1064 nm) in PCSS-based HPM applications, with an additional need for second and third harmonic generation (SHG/THG) optics to trigger WBG solids (GaN/SiC).

Solution Space: Design and implement a compact (~1.1 cu-ft), lightweight (10–15 lbs.), and inexpensive (<$15,000) alternative for conventional high average power optical trigger (laser) system to improve SWaP-C^2 index of HPM systems.

Sub-Problem: Unavailability of commercial-off-the-shelf (COTS) miniature optical sources with sub-nanosecond pulse widths and tens-of-μm beam width, delivering >1-Watt power to implement as a makeshift/turnkey solution for the laser system.

State-of-the-Art (SOTA): High average power picosecond pulsed lasers available up to 50 W output power with a gain factor up to 40 dB (~10,000x power) with laser amplifier.

Deficiency in the SOTA: High average power 1064-nm pulsed lasers are bulky, require auxiliary systems, and additional optics for SHG/THG generation for wide bandgap (WBG) device triggering.

Solution Proposed: Multi-stage laser diode array (LDA) driver powered by seed-laser-diode-driven avalanche WBG-PCSS as a compact, inexpensive laser replacement.

Relevance to OSPRES Grant Objective: Provides an enhanced SWaP-C^2 compliant solution for the laser (optical trigger) subsystem, with a subsequent impact on overall HPM system cost, volume, and power (optical and electrical) requirements.

Risks, Payoffs, and Challenges: Complex interconnect and thermal management system (TMS) design at high temperature (130–175°C) operation; unavailability of COTS high power pulsed laser diodes could potentially raise a need for research in laser diodes (arrays).

3.2.2 Tasks and Milestones / Timeline / Status

(A) Complete initial feasibility study for the cascaded multi-stage optical amplifier design and determine functional requirements for the laser diodes (arrays) and source driver [DEC 2020 / completed].

(B) Complete initial stage experimental implementation of the optical amplifier and demonstrate positive current gain using GaN-PCSS, triggered with a 404 nm laser diode. [MAR–APR 2021 / on hold].

(C) Complete numerical calculations for required output current at each stage and corresponding PCSS (GaN/GaAs) operating voltages in light of electric fields required for lock-on/avalanche mode, establish real-time implementation timeline, cost estimates, jitter limitation, and explore ways to protect LDA from PCSS ringing. [MAR 2021 / In progress].

(D) Study the feasibility of using mode-coupling in a slab geometry to bring the laser light into GaN/GaAs devices with reduced laser energy – modeled in COMSOL simulations [MAR 2021 / In progress].

(E) Proof of concept test with a 50 Ω load at 1 kHz pulse repetition rate [MAY–JUN 2021]

(F) Working prototype demonstration at ~MHz PRR with laser diode array/stack and ancillary optics based on HPM source driver needs. [JUL–AUG 2021]

3.2.3 Progress Made Since Last Report

(B) Experimental implementation is on hold awaiting backordered equipment (laser diodes and drivers) for lab testing.

(C) Working backwards from the LDA drive current requirement of 120 Amperes, GaN/GaAs-PCSS operational parameters have been calculated in light of the minimum electric field ($\vec{E}$) required for lock-on/avalanche operation. The minimum operating voltage and threshold on-state resistance requirements have been determined for different device lengths (switch gaps). Also, on-state power dissipation per pulse has been calculated theoretically to estimate the cooling requirements.

(D) Initial simulation results were inconclusive due in part to difficulties in distinguishing multi-mode effects from nonlinear effects. Eliminating the nonlinear effects is enabling progress on identifying the modes in the planar/slab geometry.

3.2.4 Significant Finding(s) and Mission Impact

(A) Preliminary feasibility study of multi-stage laser diode array (LDA) driver has signified the need for lock-on conduction mode with ~$10^{2.6}$ gain factor to drive at 1 MHz pulse repetition rate (PRR) while limiting the amplification stages to 2. This reduces monetary costs to 10–12% of the conventional laser system, while achieving the expected goal of miniaturizing the optical subsystem by 90%.

(C) Inducing lock-on operation at low electric fields (~3–3.5 kV/cm) potentially reduces the risk of high jitter at ~MHz order pulse repetition rates (PRR) and negative currents due to ringing during recovery, which could otherwise damage the optical source (LDA). 72 mΩ on-state resistance (calculated) while operating PCSS in lock-on mode at low voltages (50-µm device at ~17.5 V bias) reduces the power dissipation (0.08 µJ/pulse), resulting in reduced cooling system requirements, retaining the expected SWaP-C^2 factor.

3.3 Diode-Based NLTLs

(Nicholas Gardner)

3.3.1 Problem Statement, Approach, and Context

Primary Problem: Size, weight, and cost of pulse forming/shaping networks (PFNs) need to be reduced and optimized for Navy afloat missions.

Solution Space: Develop a lumped-element nonlinear transmission line (LE-NLTL) as a pulse shaping network for the conversion of energy to the ultra-high frequency (UHF) band at single MW peak power.

Sub-Problem: Metrics used for component selection are designed for LE-NLTLs operating at sub 0.1 GHz frequencies. Using such metrics alone to design LE-NLTLs capable of single GHz frequency generation introduces a trial by error nature to the design process wherein frequency/power generation predictions and measurements can differ by a few hundred MHz or the design potentially fails to operate at all.

State-of-the-Art (SOTA): LE-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit. Simulations of LE-NLTLs indicate achievable frequencies in the single GHz range.

Deficiency in the SOTA: Simulation/measurement agreement becomes increasingly sensitive to parameters and factors outside of inductive and capacitive element choice alone. Disparities between measurement and simulation above contribute to a trial by error design process for LE-NLTL networks.

Solution Proposed: Identify and characterize diode parameters affecting frequency generation in the context of a NLTL application and identify limits/desired ranges required for UHF generation. Such parameters include, but are not limited to: diode frequency response, diode reverse bias hold-off voltage, diode small signal capacitance, diode chip/package parasitics, and diode relaxation time. The improved understanding of the

explored parameters will be used to design and fabricate a LE-NLTL capable of GHz center frequency generation at single MW peak powers.

Relevance to OSPRES Grant Objective: The SWaP-C^2 capabilities of LE-NLTLs (shown in Figure 3.3.1) represent a potential solution to the size, weight, and cost optimization issue for PFNs on Navy afloat missions.

Figure 3.3.1. 20 cell LE-NLTL of dimensions 1.1 x 23.45 cm constructed with COTS components.

Risks, Payoffs, and Challenges: There exists a potential tradeoff between power and frequency generation. Devices such as ceramic capacitors may be used in a LE-NLTL to generate high peak power due to their break down potentials in the 10s of kV, however, such devices become highly resistive at 0.1–0.2 GHz frequencies. Diodes have been shown to be operational at frequencies upwards of 0.4 GHz, however, possess low hold-off potentials limiting peak output power. The payoff to overcoming these challenges is significant reductions in PFN size and cost.

3.3.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Construct/demonstrate a prototype capable of UHF generation at low voltages (1–100 V excitation amplitude)

a. Task – Break a low-voltage pulse into a sequence of solitons (Completed SEP20)

b. Task – Increase frequency generation past 200 MHz (Completed NOV20)

c. Task – Select diode candidate (junction capacitance <50 pF) and simulate expected results (Ongoing MAR–APR21)

d. Task – Design/fabricate/test line (Ongoing MAR–APR21)

(B) Milestone – Demonstrate tuning of waveform at low voltages using electrical or mechanical means

a. Task – Simulate a topology capable of biasing the diodes using a DC voltage (Completed JAN21)

b. Task – Construct and perform initial tests on prototype (Completed JAN–FEB21)

c. Task – Troubleshoot prototype design and identify differences with simulation (Completed FEB21)

d. Task – Collect more data for statistical significance (**NEW MAR21**)

e. Task – Refine topology to reduce loses (**NEW MAR21**)

(C) Milestone – Construct/demonstrate a prototype capable of frequency generation above 1 GHz at single MW peak powers (Completed MW peak power but not GHz center frequency)

a. Task – Identify diode candidates with a hold-off voltage of several kV and a low signal junction capacitance under 100 pF (Completed JAN21)

b. Task – Design/fabricate single diode prototypes (Completed JAN21)

c. Task – Perform initial tests using half-barrel pulse source (Completed FEB21)

d. Task – Compare measurements with simulation and identify discrepancies (Completed FEB21)

e. Task – Design/fabricate/test prototype using two diodes in series (Completed FEB–MAR21)

f. Task – Test both lines with pulses of varying characteristics to determine full line behavior (**NEW MAR21**)

g. Task – Compare single and two diode line results to determine the advantages and trade offs to obtaining increased peak power and frequency through diode stacking (**NEW MAR–APR21**)

(D) Milestone – Demonstrate power scalability using an array of LE-NLTLs (On hold until milestone C is completed)

3.3.3 Progress Made Since Last Report

(A) No new progress to report.

(B) Simulated a tunable D-NLTL topology that demonstrated a positive correlation between center frequency and voltage bias. Initial measurements on the tunable circuit also indicated a positive correlation between center frequency and voltage bias. More data is needed to confirm the trend. Results are shown in Figure 3.3.2 and discussed in Section 3.3.4.

(C) Constructed a D-NLTL based on 2 K50F diodes in series per cell. Device sharpened pulse rise time from 1 ns to 800 ps with no amplification of the amplitude. Results are shown in Figure 3.3.3 and discussed in Section 3.3.4

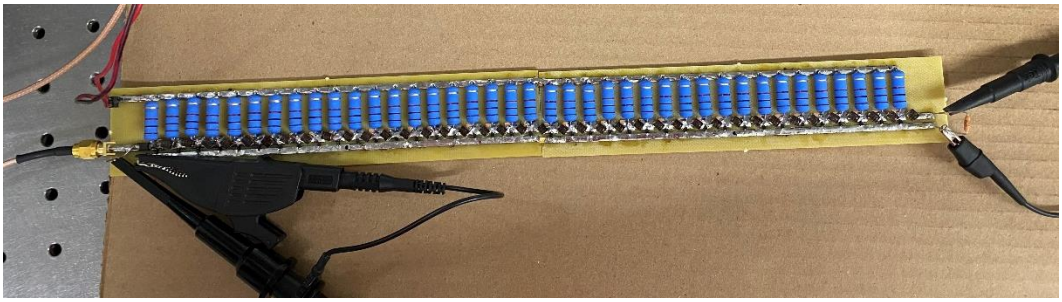
(D) No new progress to report.

3.3.4 Significant Finding(s) and Mission Impact

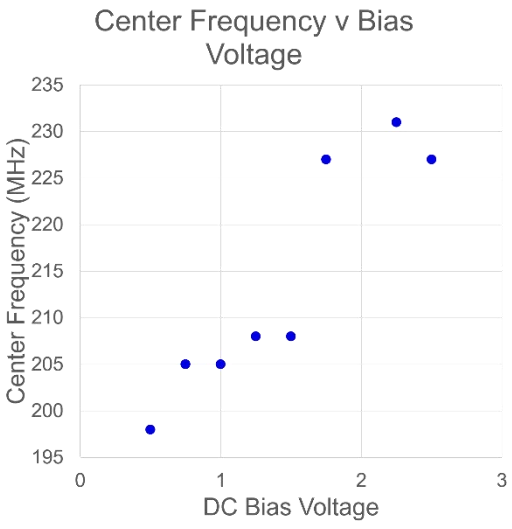
LE-NLTL frequency tuning demonstration (B): The source of the inconclusive results for the tunable line in January was the original DC blocking diode used to minimize DC voltage at the source in the circuit (model SMV1702). The diode was replaced with a model in a physically larger package (model SS22T3G) after which the network exhibited the soliton generation characteristic of LE-NLTLs as well as a positive correlation between the magnitude of DC bias applied to the diodes and center frequency, as shown in Figure 3.3.2. Currently results are preliminary, and more measurements will be taken in the month of March to determine the amount of variability in the signals generated by the

tuned NLTL. The ability to electrically tune the generated waveform is significant to the OSPRES objective as it allows for greater flexibility in HPM system design as a single knob could control the frequency generated by the NLTL.

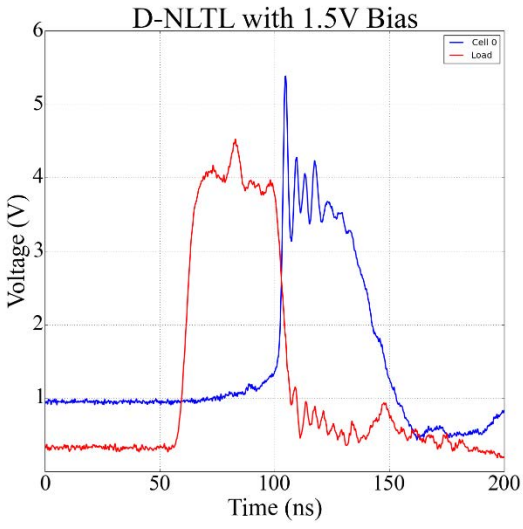
GHz MW D-NLTL prototype (C): Previously in January tests had been performed on the K100F line, composed of a single 10 nH inductance and a single diode of model K100F per cell. We then moved to the K50F line, composed of a single 10nH inductance and two diodes of model K50F wired in series per cell, with the goal of learning the effect stacking diodes has on signal generation. In simulation the 2 K50F diodes performed identically to the single K100F diode. Measurements on the K50F (shown in Figure 3.3.3) showed a reduction in the rise time of the half-barrel waveform from ~1 ns to ~800 ps with no amplitude amplification. When compared to the K100F results (rise time reduction of ~1.5 ns to ~400 ps and slight amplitude amplification), the implication is while GHz frequency generation at MW peak powers is achievable, there are losses introduced that degrade the signal. Characterizing the effects of utilizing multiple diodes in series is important to the OSPRES mission as stacking diodes can in theory increase power generation, increase frequency, and potentially decrease cost for D-NLTL topologies.



(a)

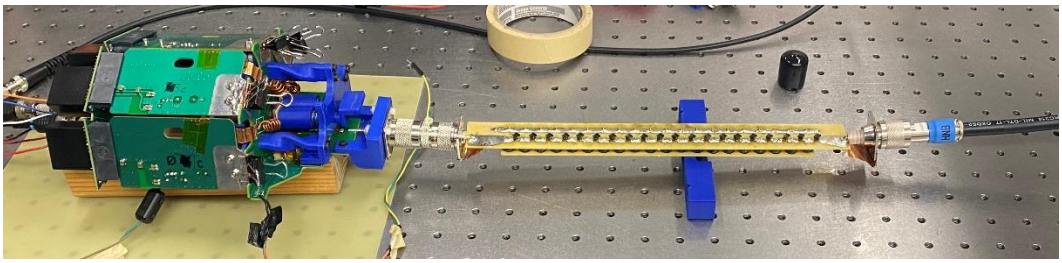


(b)

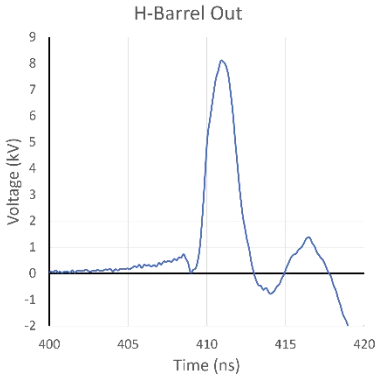


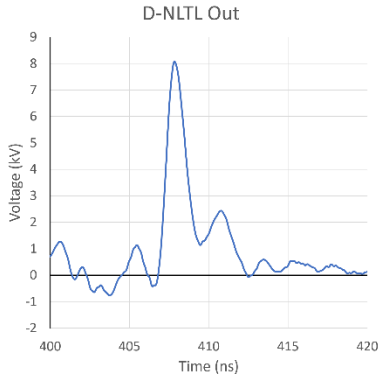
(c)

Figure 3.3.2. Results from initial round of tunability testing. (a) Fabricated board with ruler for scale; DC bias is applied to each diode through 1 kΩ resistors. (b) Example waveform at 1.5V DC bias. (c) Center frequency v applied DC bias.



(a)





(b) **(c)**

Figure 3.3.3. Results from the tests of the K50F based D-NLTL. (a) Fabricated board attached to half-barrel source. (b) Excitation waveform from half-barrel (c) Waveform produced by D-NLTL.

3.4 Si-PCSS Top Contact Modeling and Optimization for Cooling Requirements

(Jay Eifler)

3.4.1 Problem Statement, Approach, and Context

Primary Problem: High-average-power 1064-nm picosecond class lasers are too large (1100 cm^3/W) and monetarily expensive ($1000/μJ*pulse) for the Navy afloat missions. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). And a lab laser will cost $100,000 and deliver 100 μJ of laser energy to the Si-PCSS through fiber with 50% energy losses.

Solution Space: By altering only Si-PCSS device parameters, one can enable both a laser size and cost reduction in the design of a laser. Specifically, to reduce the size and cost of the laser, the laser energy required by the Si-PCSS can be reduced by altering

the Si-PCSS top contact laser windowing spacing. However, the tradeoff between laser energy reduction and device heating (and therefore, required cooling) resulting from the top contact design and geometry must be evaluated and optimized.

***Sub-Problem*:** By altering only the peak doping concentration of the Si-PCSS anode side (p-side), maximize the voltage holdoff while minimizing on-state resistance while satisfying ohmic contact requirements. The ohmic contact requirements are: durability for high current and high power, low resistivity for high frequency, doping-dependent specific contact resistivity of the metal-semiconductor (MS) junction, temperature dependency, and I-V ohmicity of MS junction. However, this optimization must also eventually consider the laser energy reduction and cooling required.

State-of-the-Art (SOTA): Si-PCSS top contact pattern designs are not known to have been published in detail. In-house patterns have used only an outer ring for the contact (resulting in high on-state resistance) and were improved by metallizing across the ring with filaments (to reduce current density high-points), similar to solar cell top contact designs. The Si-PCSS laser windowing spacings used were 10- and 20-μm, with 20-μm achieving sufficiently low sub-ohm on-state resistance using in-house laser energy of ~100-μJ delivered to the Si-PCSS.

Deficiency in the SOTA: There is no justification for 20-μm spacing being optimal for producing low sub-ohm on-state resistance with the least required laser energy and cooling (also dependent upon laser and cooling system capabilities).

Solution Proposed: Optimize OSPRES Si-PCSS top contact patterns using TCAD to meet required cooling (maintain <80°C device temperature, including hotspots) and reduce laser energy over a range of possible on-state resistances.

Relevance to OSPRES Grant Objective: Optimized top contact patterns require less laser energy and cooling which enhances SWaP-C^2 for the laser system needed to drive the Si-PCSS and maintain device operation lifetime in excess of $2x10^8$ shots/lifetime at medium power.

Risks, Payoffs, and Challenges: The top contact design does not have the most direct impact on laser system size and cost. A smaller, more effective laser is needed. However, the metallization for optimized top contacts is inexpensive and easy to manufacture. The TCAD models have various limitations: full device size too large, only single-pass laser absorption, limited external thermal bodies and heat flow mechanisms, cannot transiently charge transmission line, and only single to few pulses feasible for Si-PCSS.

3.4.2 Tasks and Milestones / Timeline / Status

(A1) RDT will fabricate 2 wafers of variable window Si-PCSS. (20, 40, 60, 100, 200, 350 μm) spacings for 1 cm devices, with 6 of each on 1 wafer, will be made. And 60 μm and 350 μm for 7 cm devices, with 5 of each, will be made on another wafer. / FEB 2021 / Devices delivered to UMKC FEB 4, 2021.

- Milestone: achieved for fabricating and receiving variable window Si-PCSS.

(A2) UMKC will measure on-state resistance vs laser energy for Si-PCSS devices with various window spacings. / FEB–MAR 2021 / One 7 cm, 350 μm window Si-PCSS has been tested. 1 cm, variable window devices to be tested.

(B) Perform TCAD studies to optimize laser windowing spacing using heat removed from the Si-PCSS with the addition of temperature hotspots. The studies will quantify the tradeoff between reduced laser energy for on-state resistance vs reduced cooling. Additional development of the thermal models will include carrier recombination–generation heating, external thermal bodies, and improve computational efficiency (to enable studies over a range of laser energies). / First thermal TCAD simulations performed on DEC 4, 2020. Initial thermal spacing study finished JAN 30, 2020. / On-going status (no timeline set yet for continued work, waiting for variable window experimental results).

- Milestone: summary of contact spacing vs heat removed and device temperature at 94 μJ of laser energy (assumes no fiber).

(C) Perform TCAD studies to determine relationship between peak p-doping concentration (anode side) and device performance (on-state resistance, voltage holdoff and ohmic contact requirements). An optimal p-doping concentration can then be determined. To be consistent with earlier top contact spacings used for reduced laser energy and/or reduced cooling, models include doping-dependent free-carrier absorption photogeneration and thermal modeling. / First TCAD simulation performed NOV 11, 2020. Last TCAD simulations finished JAN 30, 2020. / On-going status (no timeline set yet for continued work).

3.4.3 Progress Made Since Last Report

(A2) On-state resistance for the single surviving 7 cm, 350 um window Si-PCSS was lower than for earlier 20 um versions for moderate laser energies.

(B) No progress since last report.

(C) Previously obtained results for on-state resistance and voltage holdoff (DC) vs peak p-doping concentration are shown in Figures 3.4.1 and 3.4.2, respectively. Figure 3.4.3 is an example of ohmic contact requirements showing the specific contact resistivity vs p-doping concentration. The results indicate lower p-doping (3.4×10^{19} – 2.1×10^{18} dopant atoms/cm^3) improves both operating voltage (70% breakdown) and on-state resistance by a few hundred volts and about 100 mΩ. The lower limit of p-doping is set by the ohmic contact requirements which is primarily ohmicity (or free flow of current in either direction across the metal-semiconductor junction or contact).

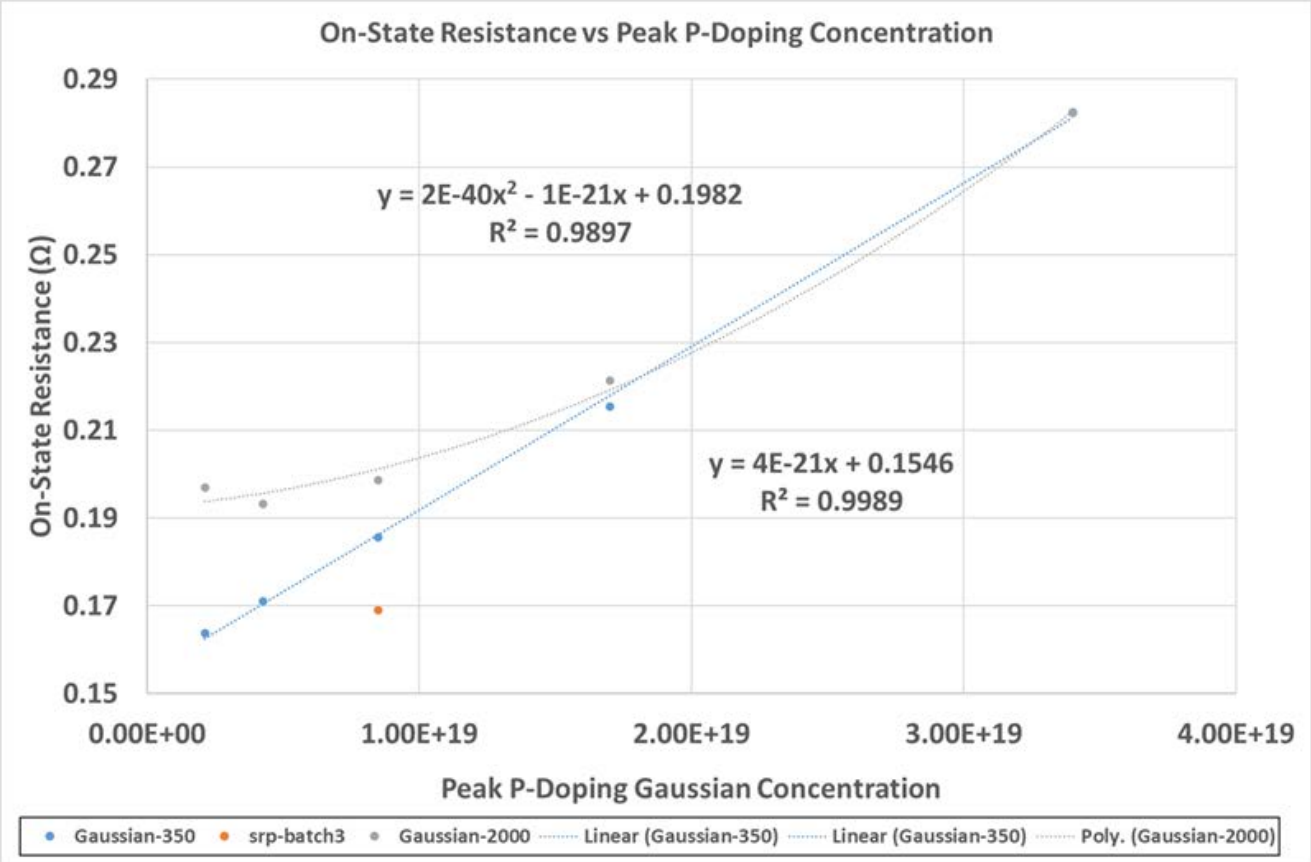


Figure 3.4.1. On-state resistance vs peak p-doping for optimal 350 μm window and wide 2000 μm window showing tradeoff. The 2000 μm window has a minimum on-state resistance at p-doping of 4.25×10^{18} dopant atoms/cm^3 due to tradeoff between increased resistance in p-doped top layer underneath the metallized contact and increased photogeneration from doping-dependent laser absorption. The 350 μm continues to reduce on-state resistance down to 2.125×10^{18} dopants/cm^3 of p-doping.

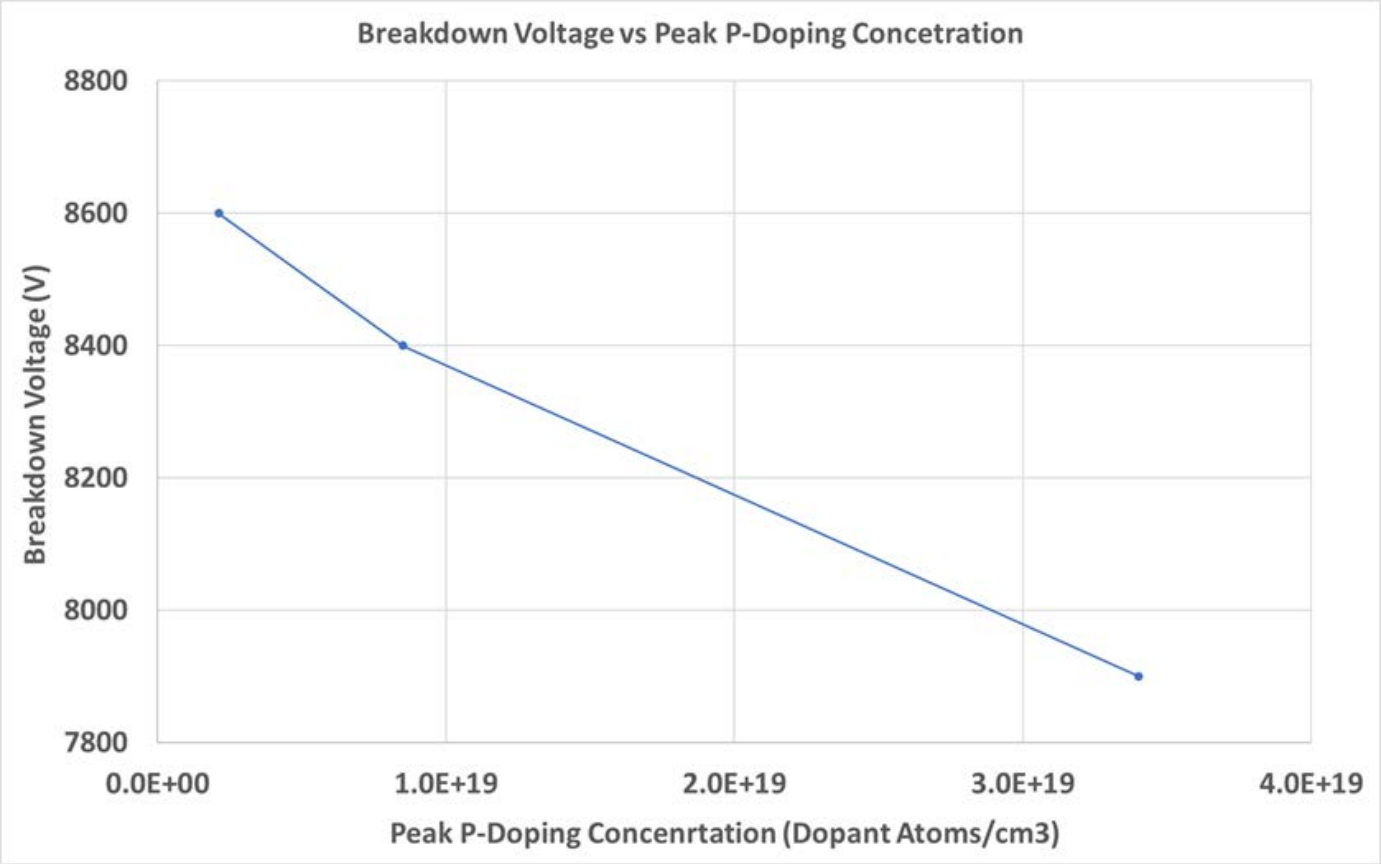


Figure 3.4.2. The DC breakdown voltage vs the peak p-doping concentration. Lower doping results in 700 V of increased breakdown.

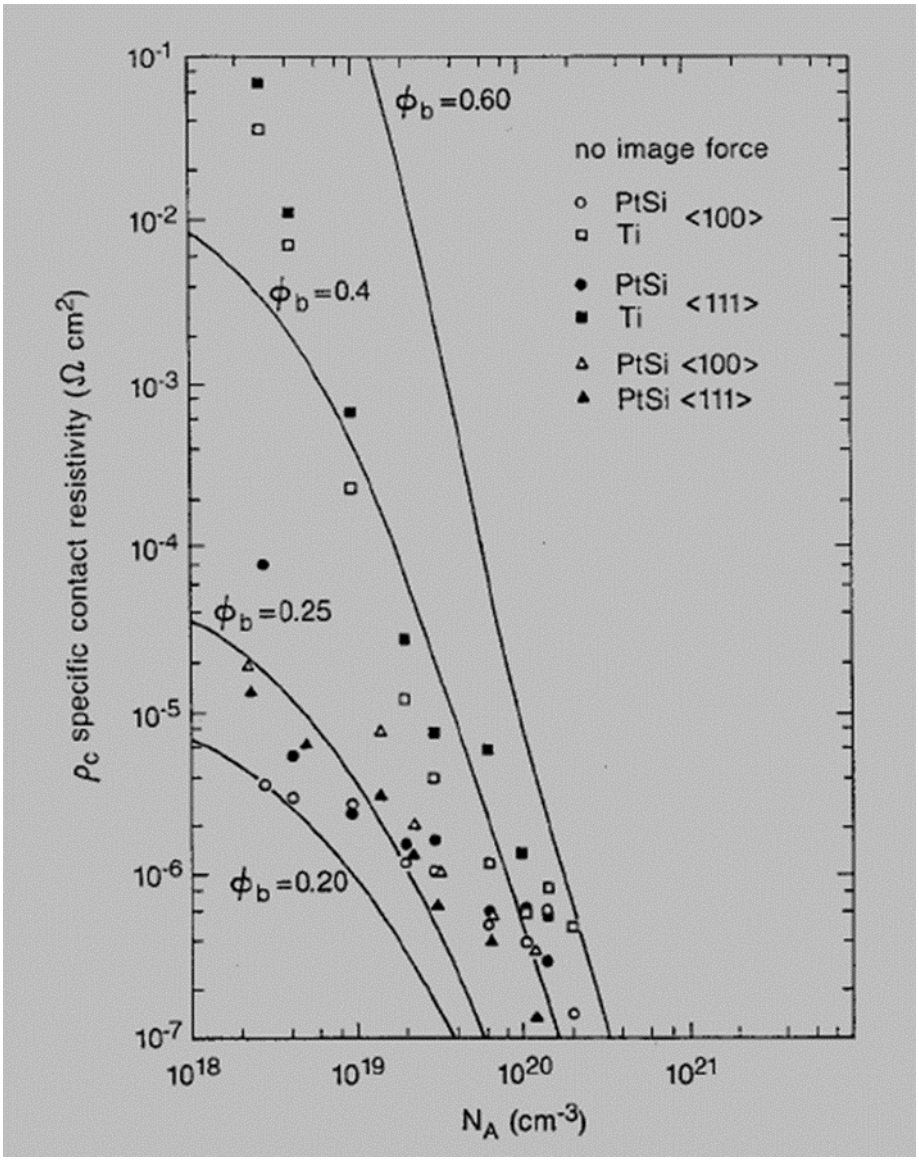


Figure 3.4.3. Specific contact resistivity vs p-doping concentration for ohmic contacts on silicon with titanium or platinum silicide [1].

3.4.4 Significant Finding(s) and Mission Impact

(A2) Experimental tests on a single 7 cm, 350 µm window Si-PCSS have been completed. The new data is shown with the earlier 7 cm, 20 µm window Si-PCSS in Figure 3.4.4. The 20 µm data is fit to a power law and can be compared to the 350 µm data for one device. The 20 µm data is for 8 different 20 um devices. Considering the device variability of 20 um device, the 350 µm data for one device could be fortuitously good but shows 20% laser energy reduction at ~0.8 Ω on-state resistance between 100 uJ and 80 uJ of switch incident laser energy (see circled region in inset). The switch was badly damaged

but worked. The TCAD simulations have predicted 30% laser energy reduction for 1 cm devices. 1 cm devices in quantity of various spacings will be tested next. The on-state resistance measurements may be improved by comparing shot-to-shot laser energy and on-state resistance instead of averaging of a pulse train. 1 cm device testing should yield power fitted curves of several devices for comparison between different spacings between 20–350 µm. From this a percent laser energy reduction vs spacing curve for experimental and TCAD simulation will be produced.

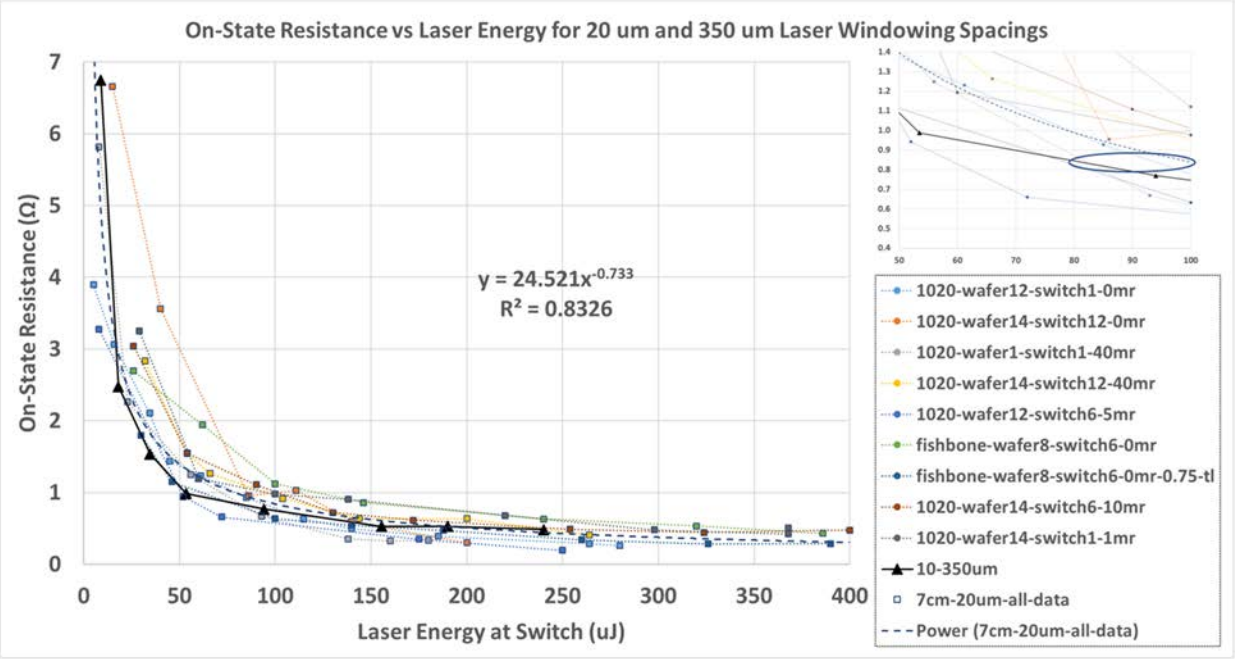


Figure 3.4.4. On-state resistance vs laser energy incident at switch for eight 7cm, 20 µm window Si-PCSS and a single 7 cm, 350 µm Si-PCSS (large black triangles). Half of the 20 µm curves are nearly the same as the 350 µm curve. Dotted dark blue line is the power law fit to the 20 µm data. The inset is a magnification of the region comparing laser energy used at ~0.8 Ω on-state resistance between the 350 µm device and the 20 µm data. The circled region in the inset shows the 20 uJ laser energy reduction.

[1] S. Swirhun, Electrochemical Society, Oct. 1988.

3.5 GaN:C PCSS Direct RF Modulation

(Heather Thompson)

3.5.1 Problem Statement, Approach, and Context

Primary Problem: Need for a more compact, cost-effective RF pulse generation system for Navy afloat missions on smaller vessels and vehicles.

Solution Space: Improve efficiency and reduce necessary material, size, and thermal requirements by utilizing gallium nitride (GaN) in PCSSs through exploitation of its theoretical material properties which allow for higher operating voltages, frequencies, and temperatures, while also eliminating the need for pulse-shaping transmission lines through direct RF modulation using the laser/photon source driving the PCSS.

Sub-Problem: Lack of maturity in compensated gallium nitride semiconductor (i.e., GaN:X with X=C,Fe) PCSS manufacturing, development, and optimization.

State-of-the-Art (SOTA): Si-based PCSS with >10 kV operational voltage, cooling system capacity of 500 W/cm^2, and theoretical breakdown of 1.3 MW/cm.

Deficiency in the SOTA: Si-based technologies requiring ~100 μJ optical pulses per 4 MW of RF output power, increasing the laser energy (per pulse) required for device triggering; long recovery time (ones-of-μs), limiting quick opening and high pulse-repetition-rate operation along with increased heating in the PCSS; critical electric field of 0.3 MV/cm, leading to devices that are ones-of-cm^2 in area for the target peak power; and operating temperature of <160°C, leading to increased cooling requirements.

Solution Proposed: Replace Si-PCSS device with GaN:C utilizing direct RF modulation — eliminating the need for a bulky pulse-forming transmission line (~3 ft long) — capable of handling >3 MW (peak power) with ~20 μJ of incident optical energy, device area <1 cm^2, and operating temperature ~500°C (theoretical temperature which will be limited by circuit components and solder).

Relevance to OSPRES Grant Objective: Reduction in size and cost for cooling system that prevents damage to the PCSS device and components along with eliminating need for a bulky pulse-shaping system, as well as decrease in material cost and needed incident laser energy, leading to enhanced SWaP-C^2 capability with greater modularity and scalability.

Risks, Payoffs, and Challenges: Due to manufacturing limitations, GaN PCSS devices tend to be limited to lateral geometries (both contacts on the top side of the device), limiting operating voltage due to current crowding and surface flashover. The recovery time (ones-to-tens-of-ns) may lead to device heating and increased DC, or zero-frequency, component when generating RF with a period on the same order as the recovery time.

3.5.2 Tasks and Milestones / Timeline / Status

(A) **Jan-March 2021** Demonstrate RF unipolar modulation in the 1–2 GHz regime and up to 2 kV operating voltage with current PCB setup and automated optical delay system. Achieving 2 kV operating voltage should allow for preliminary effects testing before (or in conjunction with) striving towards higher operating voltages. **Ongoing**

(B) **Start March 2021** Demonstrate RF bipolar modulation using an advanced test setup with two GaN:C PCSSs triggered using the same optical delay, but with the second device connected to a negative power supply.

(C) **Start April 2021** Achieve higher center frequency content in unipolar and bipolar modulation by using a faster (rise-time and pulse-width) laser to activate GaN:C PCSS.

(D) **Start May 2021** Complete study of recovery for differing gap lengths, incident energies, and operating voltages and find solutions to reduce the recovery time.

(E) **Start June 2021** Complete study on the feasibility of using mode-coupling to bring the laser light into GaN:C devices allowing for a possible reduction of laser energy, and pulse shaping within the laser-coupler/GaN:C composite structure.

3.5.3 Progress Made Since Last Report

(A) Demonstrated unipolar modulation using a 500 μm gap length GaN:C PCSS of up to 1.2 kV using Sylgard 182 to prevent flashover. Failure occurred due to air bubbles being present in the Sylgard, allowing flashover to occur. Next step in testing will be using a 1000 μm gap length GaN:C device and vacuum cure the Sylgard at low temperature, to prevent it bubbling along the PCB trace.

(B) Demonstration of bipolar modulation will occur once a new PCB is designed/fabricated that works with the necessary pulse chargers.

(E) A study of mode-coupling has been initiated in COMSOL. Some challenges arose in setting up the model due to inexperience with COMSOL and difficulties in distinguishing multi-mode effects from nonlinear effects. Work is progressing by eliminating the nonlinearities from the simulations in order to more clearly identify the electromagnetic mode structure within the cylindrical coupler.

3.5.4 Significant Finding(s) and Mission Impact

Towards demonstrating direct RF modulation at multiple-kV (A), 1.2 kV unipolar modulation was achieved using a 500 μm (gap length) GaN:C PCSS with failure occurring due to air bubbles in the Sylgard. This operating voltage is increased from 800 V previously achieved using this gap length device. The next step will be retesting with a 1000 μm GaN:C PCSS that is vacuum cured at low temperature to prevent flashover via air bubbles while preventing bubbling along the trace from curing at the higher, recommended temperature.

3.6 Bistable Operation of GaN

(Noah Kramer)

3.6.1 *Problem Statement, Approach, and Context*

Primary Problem: The short carrier lifetime of gallium nitride limits the pulse width of intrinsically triggered GaN PCSSs to the length of the triggering laser pulse. Generating long pulse widths (>1 ns) requires a laser system capable of delivering a long pulse with high energy; pulse width agility requires a laser capable of varying its pulse width. Furthermore, a GaN PCSS acts as a closing switch, and thus cannot be utilized in a system that uses inductive energy storage.

Solution Space: Bistable operation takes advantage of midgap levels, ionized by two laser pulses of differing wavelengths, to modulate the switch between long and short carrier lifetime states; the first laser pulse excites carriers and puts the switch in a long lifetime state, closing the switch, the second laser pulse opens the switch by putting it in a state with short carrier lifetime, enabling frequency agility, bulk conduction, and use as an opening switch for inductive energy storage.[1] To enable bistable switching in semi-insulating GaN via doping/co-doping, it is necessary to survey the capture cross sections of various dopants in GaN (literature/simulation/empirical studies) to determine their suitability for bistable operation and design a co-doping scheme.

Sub-Problem: Bistable switching requires a midgap level that has a large hole capture cross section and a small electron capture cross section; it needs to be determined what dopants in GaN have this property.[2]

State-of-the-Art (SOTA): The SOTA bistable photoswitch is the GaAs "BOSS" switch capable of switching 18 kV (limit of bias-voltage modulator) and varying pulse width from 650 ps – ~1.5 ns with sub-nanosecond opening.[3]

Deficiency in the SOTA: The breakdown field of GaAs is only 12% of that of gallium nitride (0.4 MV/cm vs. 3.3 MV/cm). Furthermore, GaAs has a low thermal conductivity, resulting in larger cooling requirements.

Solution Proposed: Replace bistable GaAs switch with a bistable GaN switch, enabling higher hold-off voltage, higher temperature operation, and lower thermal requirements compared to GaAs.

Relevance to OSPRES Grant Objective: Inductive energy storage has two orders of magnitude higher energy density than capacitive storage.[4] However, inductive energy storage requires an opening switch to discharge the stored energy. As a bistable switch can operate as either an opening or a closing switch, it would enable the use of inductive energy storage to reduce the system size. When used as a closing switch, a bistable switch would allow for dynamically changing the output pulse-width, eliminating the need for a pulse-forming transmission line.

Risks, Payoffs, and Challenges: GaN growth often incorporates unintentional dopants that necessitate compensation to achieve semi-insulating material. For example, GaN:C switches from NRL are compensated using carbon, but it is unclear whether the midgap levels are capable of bistable operation. Co-doping the PCSS while maintaining midgap levels suitable for bistable operation is the primary challenge of this effort. Another challenge is the requirement of timing two laser pulses of differing wavelengths. Depending on the dopant levels, this may be possible to perform with a frequency-doubled Nd:YAG laser, as the energy of 2.3 eV at 532 nm and 1.1 eV at 1054 nm is equal to the bandgap of GaN, however the bistable level would have to lie very near 1.1 eV.

3.6.2 Tasks and Milestones / Timeline / Status

(F) **Feb 2021** Investigate feasibility of bistable GaN operation.

a. Review literature on GaN dopants to identify candidates with large hole capture cross section compared to electron capture cross section.

b. Propose possible co-doping schemes for bistable operation (compare to doping of current GaN devices).

(G) **March 2021** Simulate bistable GaN devices and find manufacturers for devices.

a. Test on-hand GaN;C devices for persistent photoconductivity.

b. Simulate bi-stable GaN devices (if Sentaurus trial/license is available).

c. Discuss with device manufacturers (Kyma/NRL)

(H) **April 2021** Test bistable devices

a. I-V, C-V, CW conductivity, UV-Vis, pulsed testing (single wavelength and dual wavelength).

(I) **May 2021** Complete study of switch operation varying wavelengths, bias voltage, and time delay between the on and off laser pulses.

3.6.3 Progress Made Since Last Report

(A) Reviewed literature to find examples of persistent photoconductivity in GaN caused by differences in electron and hole capture cross-sections.

(B) Considered feasibility of studying extrinsic excitation in Silvaco TCAD; it appears that Silvaco is not well suited for simulating optical excitation of midgap states. Sentaurus may be able to perform the desired simulations.

3.6.4 Significant Finding(s) and Mission Impact

Persistent photoconductivity (PPC) was observed in unintentionally doped GaN, and attributed to the small electron capture cross-section compared to the faster hole capture rate.[6] PPC has also been related to a defect that produces a yellow luminescence (YL) band in GaN; this defect has been identified in later literature as the C_N defect.[6][7] PPC has also been observed in unintentionally doped, neutron irradiated GaN with no YL band, which has been attributed to threading dislocations.[8] It is still unclear whether the carbon defect can produce persistent photoconductivity alone, or if it requires additional co-dopants or other defects, such as screw dislocations. Because PPC was observed in Ref. 6. as only occurring in material with a YL band, GaN:C devices supplied by NRL and Kyma may be able to produce the effect when illuminated with the correct wavelength. Empirical studies of on-hand GaN:C devices will be performed to determine if they exhibit PPC under extrinsic excitation.

3.6.5 *References*

[1] D. C. Stoudt, J. S. Kenney, and K. H. Schoenbach, “Inductive energy storage using a fast-opening bulk optically controlled semiconductor switch (BOSS),” *IEEE Int. Pulsed Power Conf. - Dig. Tech. Pap.*, vol. 1, pp. 123–126, 1993, doi: 10.1109/ppc.1993.512892.

[2] K. H. Schoenbach, V. K. Lakdawala, R. Germer, and S. T. Ko, “An optically controlled closing and opening semiconductor switch,” *J. Appl. Phys.*, vol. 63, no. 7, pp. 2460–2463, 1988, doi: 10.1063/1.341022.

[3] D. C. Stoudt, M. A. Richardson, H. D. Willie, and D. L. Demske, “High-power, high-repetition-rate operation of a Bistable Optically controlled Semiconductor Switch (BOSS) David C. Stoudt, Michael A. Richardson, Heather D. Willie, and David. L. Demske Dahlgren Division, Naval Surface Warfare Center,” vol. 2343, pp. 135–144, 1994.

[4] J. Mankowski and M. Kristiansen, “A review of short pulse generator technology,” *IEEE Trans. Plasma Sci.*, vol. 28, no. 1, pp. 102–108, 2000, doi: 10.1109/27.842875.

[5] F. Binet *et al.*, “Mechanisms of recombination in GaN photodetectors Mechanisms of recombination in GaN photodetectors,” vol. 1202, pp. 45–48, 1996, doi: 10.1063/1.117411.

[6] S. Y. C. V. Reddy, K. Balakrishnan, H. Okumura, “The origin of persistent photoconductivity and its relationship with yellow luminescence in molecular beam epitaxy grown undoped GaN,” *Appl. Phys. Lett.*, vol. 73, no. 244, 1998, doi: https://doi.org/10.1063/1.121769.

[7] S. G. Christenson, W. Xie, Y. Y. Sun, and S. B. Zhang, “Carbon as a source for yellow luminescence in GaN: Isolated CN defect or its complexes,” *J. Appl. Phys.*, vol. 118, no. 13, 2015, doi: 10.1063/1.4932206.

[8] Z. Minglan, Y. Ruixia, and L. Naixin, “Persistent photoconductivity in neutron irradiated Persistent photoconductivity in neutron irradiated GaN,” pp. 0–3, 2013, doi: 10.1088/1674-4926/34/9/093005.

3.7 Drift-Step Recovery Diode Optimization

(Jay Eifler)

3.7.1 Problem Statement, Approach, and Context

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS but do not require a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times require optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening head. Additional goals for PRF/BRF are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies.

Sub-Problem 1: TCAD and SPICE models of the DSRD are 40% accurate and must be improved.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD device parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetime have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies difficult to the level of tens of MW of peak power while maintaining ns-order risetime. In addition, DSRD fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power, minimum risetime but also for low-jitter, reduced cooling, and compactness.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening the DSRD-based systems can produce comparable risetimes. The SWaPC^2·cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities (for diffused diode, >100 A/cm^2 [1]). DSRD and Silicon Avalanche Sharpeners (SAS) must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD modeling.

3.7.2 Tasks and Milestones / Timeline / Status

(A) Develop accurate models for DSRD (TCAD and SPICE models are 40% accurate)

(A1) Develop accurate DSRD TCAD models / JAN-APR 2021 / TCAD models have been replicated in new code but must be compared to experimental data and improved as necessary.

(A2) Develop accurate SPICE models / MAR-JUN 2021 / DSRD SPICE model research has not begun outside of partly converting MOSFET model to TCAD spice.

(A3) Develop parasitic capacitance, inductance, and resistance models for single die and stacked DSRD. / MAR-JUN 2021 / Parasitic model research has not begun.

(B) Explore TCAD modeling to advance DSRD research

(B1) Study carrier lifetime effect on risetime / FEB-APR 2021 / No directly attributable effect of lifetime on risetime was found. Future more systematic studies including DSRD and circuit topology parameters will include lifetime and show its effect on performance.

(B2) Avalanche and device operation study / FEB-MAY 2021 / Avalanche limited peak power but models do not correspond to experiment and must be improved.

(B3) Study effect of the width of outer edge contact on current density and breakdown in device. / MAR-MAY 2021 / No research begun.

(C) Silicon Avalanche Sharpener (SAS) modeling

(C1) Begin TCAD modeling of SAS / DEC 2020 / Preliminary SAS research begun replicating published work [3] but further work to continue.

(C2) Determine current carrying capacity of SAS and SAS stacks / MAR-JUN 2021 / SAS research to resume.

3.7.3 Progress Made Since Last Report

(A1) To begin TCAD studies, an epitaxial DSRD study was replicated or benchmarked in Silvaco TCAD [2]. Using a DSRD model of an in-house device, charge extraction timing was studied for varied input pulse periods in a simple circuit without an inductor (see Figure 3.7.1a). The study showed sufficiently long forward pump time resulted in near perfect 50% charge extraction timing, which allows for the maximum reverse current in the DSRD. This was the only study using the simpler simulation circuit and all other DSRD TCAD studies used the circuit of Figure 3.7.1b.

Two TCAD studies of stacked DSRD for metal resistance and doping variability were performed to observe the change in risetime. Increased risetime in in-house DSRD stacks has been attributed to increased metal resistance and/or device variability. Altering the in-house DSRD SRP doping profile for less p-doping concentration at depth showed an increased TCAD risetime for a single DSRD die. Two DSRD with decreased p-doping were incorporated into a 5 stack with 3 normally p-doped DSRD. The risetime of the stack of variable doping devices was between the 5 stack risetimes for all decreased p-doping and all normally p-doped DSRD. This result confirms the expected effect of device variability on stack risetime from doping variability: incorporating DSRD with higher risetimes due to doping variability increases stack risetime in proportion to number of increased-risetime DSRD incorporated. The metal resistance used between dies in 5 stacks (1 μΩ and 1 mΩ) did not significantly alter the risetime, however further increases in resistance should produce increased risetime. As well, a more complete model of the parasitics for capacitance, inductance, and resistance for single die and stacked DSRD is needed.

TCAD studies for risetime of less than 2 ns, indicative of DSRD operation of the diode, were performed using the in-house SPT Gen 1 SRP doping profile and a typical DSRD p-π-n gaussian doping profile. The SPT DSRD risetimes were 3.9 ns. The gaussian profile produced risetimes of 2 ns and less (for example Figure 3.7.4). Further study for the effects on risetime from the doping profile will be necessary but should incorporate realistic achievable doping fabrication (earlier work for triple-cocktail p-doping doping profile of RDT replicated in Silvaco TCAD process software).

(A2) The SPICE simulations for design of the DSRD inductive pulser circuit topologies (including in Figure 3.7.1b) use SPICE models for a primary switch including a MOSFET and driver. The MOSFET model was converted halfway to the TCAD form of SPICE.

The E sources in the MOSFET model of LTSPICE/PSPICE were eliminated in the code and successfully produced identical output. To convert to TCAD SPICE the code must be rewritten and an expression for the charge must be developed from the capacitance using numerical integration or another expression. The driver model may be convertible (by converting the E sources to G sources and a 1 MΩ parallel resistance) and prove identical. However, the SPICE models for MOSFET and driver are currently modeled as producing a sine input to later stages of the pulser or instead with simple, variable resistance switch models replacing the MOSFET and driver.

(B1) An SPT SRP-based doping profile was studied for effect of carrier lifetime on risetime within the circuit of Figure 3.7.1b. Results showed the main effect of the lifetime is to initiate the recovery process earlier in time with lower lifetimes. Otherwise the peak voltage and risetime are slightly lowered with decreasing lifetime but are likely caused by recovering earlier in the reverse current swing producing decreased load output. Decreased lifetime was also found to moderately lower impact generation at sufficient levels of bias but had minimal effect on the load output waveform. Lifetime studies should still be a part of any systematic device parameter study to determine its effect and optimal amount.

(B2) DSRD breakdown limitations had previously been studied as DC breakdown as is standard practice. Breakdown during transient simulation of the DSRD within the inductive pulser circuit (Figure 3.7.1b) was studied by including impact ionization modeling in the TCAD transient simulation. Cross-sections of the device and the spatially dependent impact generation rate were collected and compared to DSRD output pulse peak voltage and risetime. Including impact ionization or avalanche showed peak voltage is limited to ~1000 V on a 200 μm device (also dependent on doping profile). The current density was limited to 100 A/cm^2 in the 0.7 cm^2 area simulation device before IMPATT oscillations occured. Results for varying input voltage magnitude of the sine wave pulse for maximum impact ionization generation rate, peak load voltage, and risetime are shown in Figures 3.7.2-3.7.4. Figures 3.7.5 shows the load output pulse waveforms over a range of input voltages. Figure 3.7.6 shows an experimental result from the literature for comparison to TCAD simulations.

(C1) Replicated Kesar published work on SAS [3].

3.7.4 Significant Finding(s) and Mission Impact

(B2) Impact ionization was included in TCAD models of the DSRD and simulated in an inductive pulser circuit (see Figure 3.7.1b). The voltage input V1 is a single sine wave pulse (180 degrees out of phase) and 200 ns in period. The voltage input magnitude is varied from 2-250 V while the device operation for peak voltage and risetime at the load is observed. Cases for including impact ionization and no impact ionization are also simulated to determine the role of avalanche or impact ionization on the device operation, especially peak voltage and risetime.

The device models used are for a 200 μm thick Si-DSRD. The doping is p-π-n gaussian (P+ 125 μm deep and N+ 40 μm deep). The intrinsic region is a p$^-$ base with 1×10^{14}

concentration and 35 μm thick. The 1D-style model in 2D Silvaco ATLAS has the area set to 0.7 cm^2.

The carrier generation from impact ionization or avalanche has been collected vs device depth and shows avalanche occurs in the p^- base and starts near the junctions at sufficiently high input voltage magnitude. The maximum impact ionization generation rate has been collected vs voltage input magnitude in Figure 3.7.2. The impact generation rate increases dramatically (or has a knee) at 50 V and is seen to be S-shaped and knees again at around 150 V. In Figure 3.7.5, the 50 V grey pulse is seen to have a smooth and symmetrical shape due to minimal impact ionization. These load waveforms show increasing amounts of so-called IMPATT (impact avalanche transit time) oscillations up to 680 V [1,4,5], see Figure 3.7.6.

The peak voltage and risetime vs voltage input magnitude are shown in Figures 3.7.3 and 3.7.4. After 50 V, the generation rate increases after its knee and the peak voltage levels off for the impact ionization case only. The risetime is the same for the two cases except that at 75 V the risetime has a minimum of 1.7 ns for the impact ionization case. After 50-75 V the amount of avalanche inhibits the device performance by limiting peak voltage while remaining relatively flat in risetime.

DSRD good operation is defined at having a risetime of less than 2 ns and switching as much power/energy as possible. The DSRDs modeled in TCAD are limited to about 20 kW peak power on a 50 Ω load or about 1000 V and have less than 2 ns risetimes. Comparison to experimental results and adjustment of the impact ionization parameters are necessary for the TCAD models to be accurate. Whether a TCAD model can capture the DSRD operation to predict limits on performance has not been understood.

Adjusting the area larger can allow the voltage applied to be larger while maintaining current density levels below 100 A/cm^2 without causing significant enough avalanche to degrade pulse quality and/or produce IMPATT oscillations. This has yet to be verified in TCAD simulation and there are limits on how large or small an area should be for a given thickness of DSRD and maximize peak power and minimize risetime.

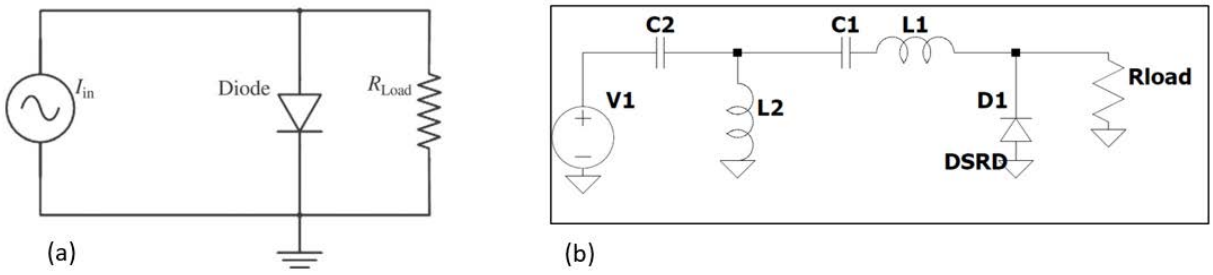


Figure 3.7.1. TCAD simulation circuits for DSRD (diode, D1). (a) Simple circuit consisting of DSRD diode in parallel with resistive load supplied by a current source for modeling inductor current output and intended for DSRD recovery studies. (b) Inductive pulser circuit with sine wave pulse input. L1 is the pulse inductor while C1, C2 and L2 are

responsible for forward pumping and reverse biasing the DSRD with a higher reverse voltage slew rate tuned for a 200 ns period sine wave pulse input.

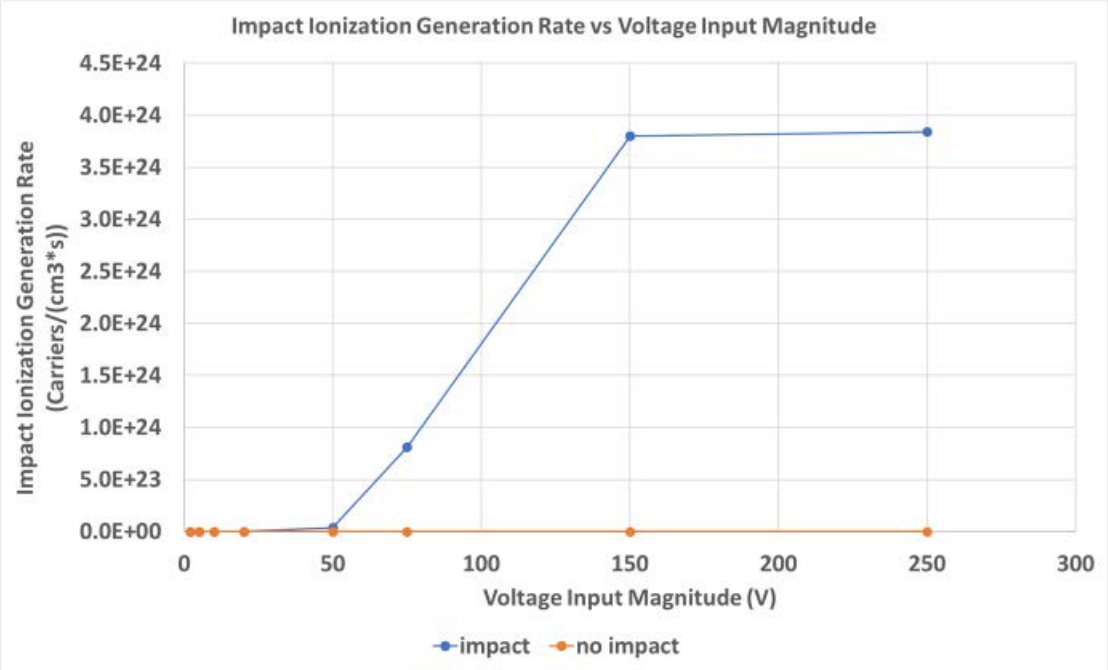


Figure 3.7.2. Variation of maximum impact generation rate with magnitude of the voltage input. After ~50 V the rate of avalanche becomes significant. After 75 V IMPATT oscillations begin to dominate the load output. After 150 V the impact generation rate levels off.

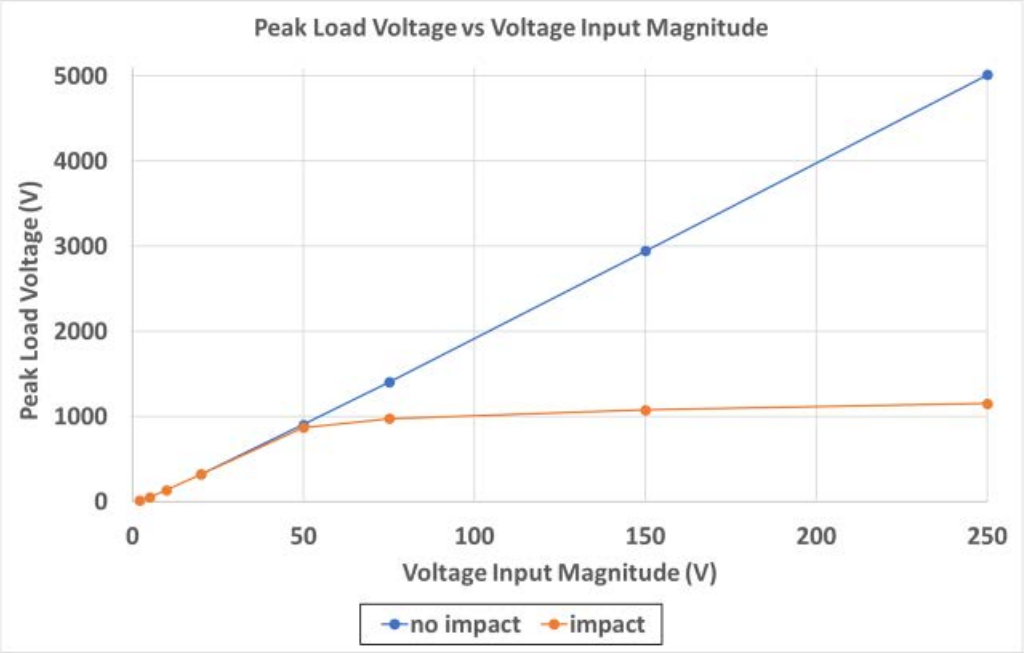


Figure 3.7.3. Peak load voltage vs voltage input magnitude shows peak voltage levels off after 50 V when impact ionization is included.

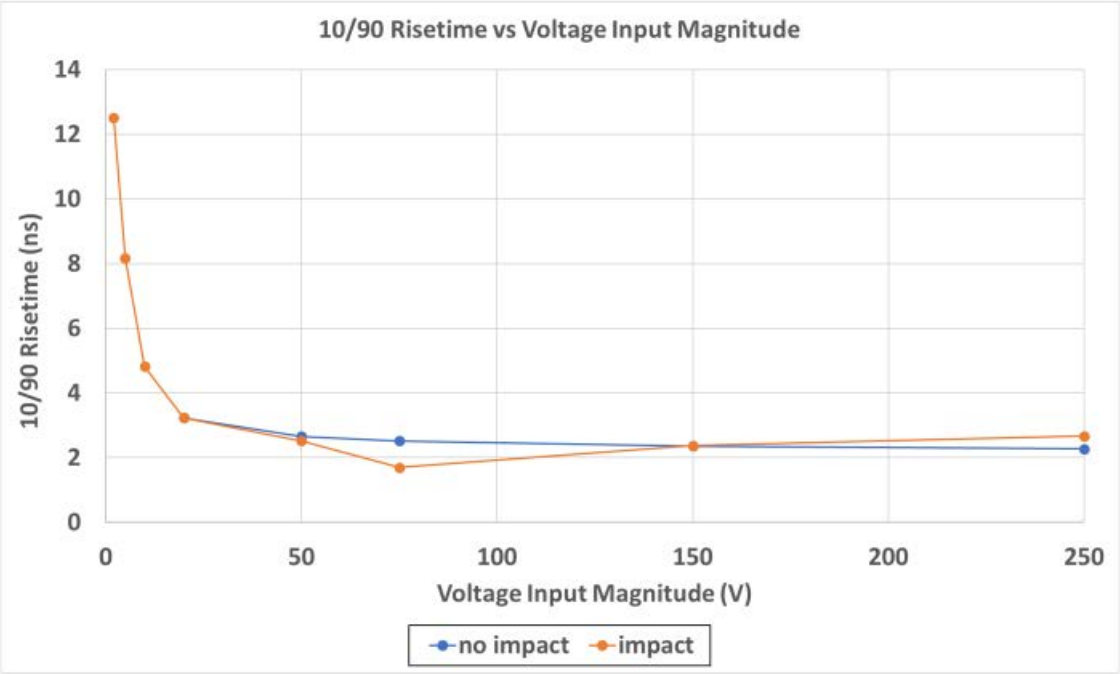


Figure 3.7.4. The risetime (defined as the time from 10% to 90% of the peak voltage) vs voltage input magnitude shows overall risetime flattens after 20 V. After 50 V avalanche becomes significant causing the peak voltage waveform to sharpen until IMPATT oscillations dominate the pulse waveform.

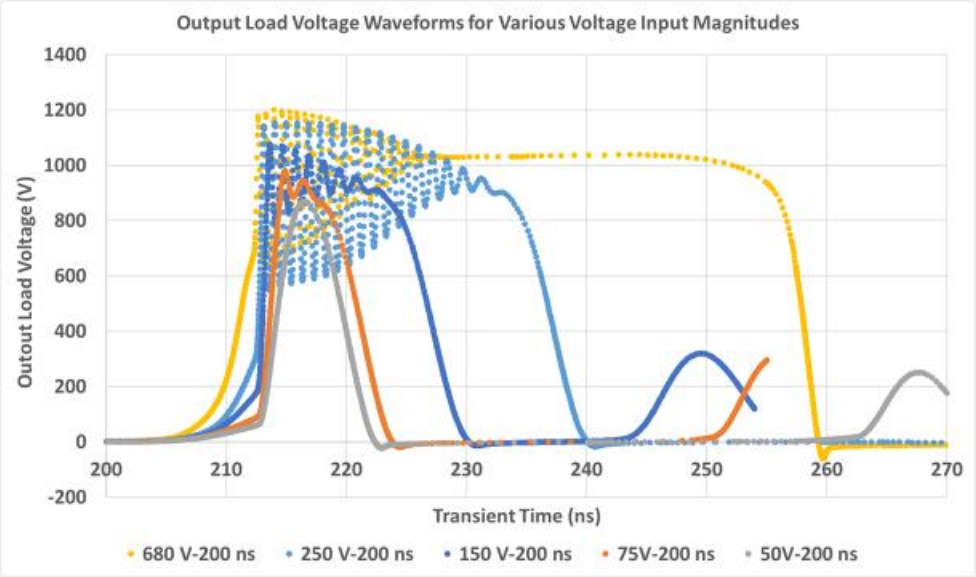


Figure 3.7.5. Load output voltage waveforms for 200 ns period sine wave input of varied voltage input magnitude. At 50 V, the output waveform is symmetrical and smooth (grey). At 75 V (orange), the waveform is sharpened and shows some oscillations (oscillations not distinct up to 60 V). IMPATT oscillations become more larger and dampen over longer times up to 680 V (yellow) after which they increasingly begin to disappear.

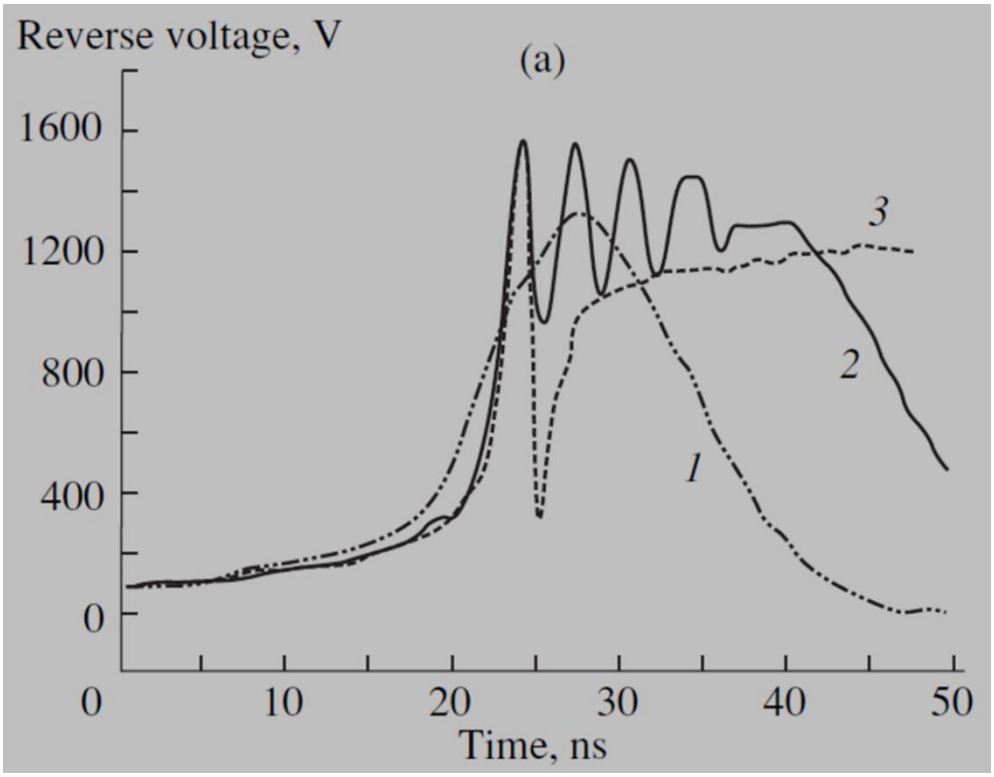


Figure 3.7.6. Experimental curves for DSRD load output in an inductive pulser circuit taken from [1]. Curve 1 is the load output with no sharpening or IMPATT oscillations at 100 A/cm^2 maximum reverse DSRD current density. Curve 2 is 250 A/cm^2 showing IMPATT oscillations. Curve 3 is for 350 A/cm^2 after IMPATT oscillations cease.

3.7.5 References

[1] Kozlov, V. A., A. F. Kardo-Sysoev, and V. I. Brylevskii. "Impact ionization wave breakdown of drift step recovery diodes." *Semiconductors* 35, no. 5 (2001): 608-611.

[2] Sharabani, Y., Y. Rosenwaks, and D. Eger. "Mechanism of Fast Current Interruption in p− π− n Diodes for Nanosecond Opening Switches in High-Voltage-Pulse Applications." *Physical Review Applied* 4, no. 1 (2015): 014015.

[3] Kesar, Amit S., Arie Raizman, Gil Atar, Shoval Zoran, Svetlana Gleizer, Yakov Krasik, and Doron Cohen-Elias. "A fast avalanche Si diode with a 517 μ m low-doped region." *Applied Physics Letters* 117, no. 1 (2020): 013501.

[4] Yang, Xiudong, Yongdong Li, Hongguang Wang, Zhongjie Li, and Zhenjie Ding. "Numerical investigation of the nanosecond opening-mechanism of drift step recovery diodes." *Journal of Applied Physics* 109, no. 1 (2011): 014917.

[5] Kyuregyan, A. S. "High-Voltage Diffused Step Recovery Diodes: I. Numerical Simulation." *Semiconductors* 53, no. 7 (2019): 962-968.

4.0 Prime Power and Conditioning

4.1 HV Switch Pulsed Chargers

(Wasekul Azad and Faisal Khan)

4.1.1 Problem Statement, Approach, and Context

Primary Problem: Commercially available high-voltage solid-state switches made by BEHLKE are the best in SWaP-cooling, but are expensive, have long lead times (2–3 months), and are made outside of the US. For the Navy afloat mission to be successful, we need a sustainable supply of US-manufactured switches at a much lower cost.

Solution Space: Design and demonstrate modular high-voltage (~10 kV) and fast (repetition frequency = 100 kHz) solid-state switches using a combination of series- and parallel-connected commercially available inexpensive discrete MOSFETs and custom high-voltage (~10 kV) isolated gate drivers.

Sub-Problem: Voltage balancing among the series-connected MOSFETs, minimization of gate signal delays, cooling of the individual MOSFETs, balancing resistors, high-voltage isolation required for the power supplies, and the controlling pulse width modulated (PWM) signal as well as differential voltage feedback measurement across individual MOSFETs.

State-of-the-Art (SOTA): Direct liquid-cooled solid-state switch from BEHLKE (e.g., HTS-151-30).

Deficiency in the SOTA:

1. BEHLKE-made switches are expensive. For instance, a single HTS-151-30 switch costs around $5,000.
2. BEHLKE switches along with direct liquid cooling units occupy a considerable amount of space. For instance, an HTS-151-30 switch from BEHLKE has a footprint of approximately 225*85*75 mm without considering the liquid cooling system. Some key parameters of this switch are as follows.

   i) Maximum operating voltage = 15 kV

   ii) Maximum continuous load current = 2.52 A (without cooling), 30 A (with liquid cooling)

   iii) Maximum turn-ON peak current = 300 A (pulse width = 200 µs, duty cycle <1%)

   iv) Turn-ON resistance = 1.3 Ω
3. Once the switching frequency is greater than 10 kHz, a liquid cooling system is required to operate the BEHLKE switch.
4. Without liquid cooling, the maximum continuous power dissipation (P_{cont}) of the BEHLKE switch is limited (e.g., for HTS-151-30, P_{cont} is 10 W without liquid cooling).
5. At a higher switching frequency (>20 kHz), the BEHLKE switch requires multiple ancillary DC power supplies, i.e., 5, 15, and 60 V.

6. The switches made by BEHLKE cannot be reconfigured to withstand a higher voltage exceeding their recommended rating. BEHLKE offers separate products to operate them at higher voltage/currents.

Solution Proposed: Designing a modular high-voltage (~10 kV) switch using a single custom isolated gate driver for each module and having a construction cost lower than the BEHLKE switch with equivalent or better performance in all specification categories (Specifications for the BEHLKE switches can be found in the following link: http://www.behlke.com/separations/separation_c4.htm).

Relevance to OSPRES Grant Objective: The proposed modular high-voltage switch is expected to facilitate controlled hundreds-of-nanosecond charging of an array of transmission lines of pulse forming networks to drive an array of PCSSs, thereby producing controlled hundreds-of-picosecond scale high-voltage pulses.

Risks, Payoffs, and Challenges:

I. Lack of rigid control over voltage balancing can lead to a cascaded failure among the series-connected MOSFETs.

II. In the absence of an adequate mitigation scheme, voltage overshoot due to the fast switching speed can exceed the voltage rating of an individual MOSFET, thereby damaging the switch.

III. At high voltage (~10 kV) and high repetition rate (>100 kHz), mitigating EMI to safeguard the individual MOSFETs from false turn-ON is a major challenge.

4.1.2 Tasks and Milestones / Timeline / Status

(A) Design a surface-mount MOSFET-based four-stage switch (6.8 kV rated) and control it using the in-house gate driver, then test its voltage-withstanding ability with a DC supply voltage up to 4–5 kV and evaluate the effectiveness of the thermal management at its current state / DEC 2020 / Completed.

(B) Design and develop a modular HV switch (~10 kV rated) using the concept of the tested four-stage high-voltage switch module and an in-house modular gate driver to drive the modular switch /JAN–FEB 2021 / Completed.

(C)

(i) Test the voltage withstanding ability of the modular HV switch with a DC supply voltage up to 10 kV and switching frequency up to 50 kHz using a resistive load (5–10 kΩ) and evaluate the effectiveness of the thermal management at its current state / FEB–MAR 2021 / Ongoing.

(ii) Test the isolation capability and evaluate the synchronization accuracy of the gate drive signal generated from the modular in-house gate driver / FEB–MAR 2021 / Ongoing.

(iii) Encapsulate the gate driver board with potting material with a high (~15–20 kV) breakdown voltage rating to prevent possible flashover/arcing in between the HV switch and this board / MAR–APR 2021 / **NEW**

(D) Test this modular HV switch coupled with a Si PCSS device up to a DC supply voltage of 5–6 kV and a switching frequency of 50 kHz / MAR–MAY 2021 / On hold until milestone (C) is completed.

(E)

(i) Design and develop a 20 kV rated modular (two modules, each with four MOSFETs) HV switch based on the design concept of the 10 kV rated modular switch using 3.3 kV rated SiC MOSFETs (new product made by GeneSiC Semi) / APR–MAY 2021 / **NEW**

(ii) Design and develop a 20 kV rated modular gate driver based on a WPT based planar transformer topology to ensure adequate galvanic isolation (~30–40 kV) for the power supplies of the gate driver APR–MAY 2021 / **NEW**

4.1.3 Progress Made Since Last Report

(B)

(i) A modular (two modules) 10 kV rated HV switch has been designed and a prototype has been developed using 1.7 kV rated SMD MOSFETs (C2M1000170J). Each module comprises four MOSFETs and is rated for close to 6.8 kV. The fabricated prototype is shown in Fig 4.1.1(a).

(ii) A modular (two modules) HV (10 kV rated) isolated gate driver has been designed and a prototype has been developed. This prototype is shown in Fig 4.1.1(b). The identical gate drive signals obtained from two modules are shown in Fig. 4.1.1(c)

To minimize the parasitic inductance in the gate drive loop, the HV switch and the gate driver are connected back to back using two board–board connectors as shown in Fig. 4.1.1(d).

(C)

(i) The modular HV switch along with the modular gate driver has been successfully tested up to a DC supply voltage of 6 kV and at a repetition frequency of 15 kHz using a 9.6 kΩ resistive load (continuous mode). The lowest and the highest rise times among individual switches are measured as 11 and 23 ns respectively at a voltage level of 6 kV. Therefore, the rise time of the entire switch can be approximated close to 23 ns.

(ii) Flashover occurred between the HV switch and the gate driver while testing at a voltage level exceeding 6 kV. Inadequate clearance between the gate driver board and the HV switch board is the probable cause of this incident.

(iii) Exploration is ongoing to identify suitable potting materials with adequate dielectric breakdown strength (≈15–20 kV) to encapsulate the gate driver board to prevent flashover.

(D) Testing of the in-house HV switch as the power conditioner unit for the PCSS based pulse forming network will be accomplished after successful testing of the modular HV

switch coupled with the custom gate driver at a DC supply voltage of 10 kV and evaluation of the test results (e.g., voltage balancing, thermal stability) are accomplished.

(E) Design of the 20 kV rated HV switch using the new 3.3 kV rated SiC MOSFETs will commence once suitable potting material is found for the gate driver and the 10 kV rated modular HV switch is tested at a DC supply voltage up to 10 kV.

4.1.4 Significant Finding(s) and Mission Impact

(A) The 6.8 kV rated four-stage surface-mount MOSFET developed in-house was successfully tested up to a DC supply voltage of 4 kV and at a switching frequency up to 20 kHz with a 3.2 kΩ resistive load.

I. Design and fabrication of the modular eight-stage HV switch and the modular in-house HV isolated gate driver are completed. The switch has been tested up to a DC supply voltage of 6 kV and a switching frequency up to 10 kHz using a 9.5 kΩ resistive load. This modular switch demonstrated a low rise time (≈23 ns) which can be a fast and scalable HV solid-state switching solution for many pulsed power applications (Task-C).

II. The simulated voltages measured across the load at 5 kV and 6 kV are shown in Fig. 4.1.2(a) and 4.1.2(b) respectively. The visible overshoot in the load voltage waveform during the turn-ON period at 6 kV can be attributed to the long ground wire of the probe and the long trace leading to the test pins. Switching transient of the fastest (rise time ≈ 11ns) and slowest (rise time ≈ 23ns) individual switches in the HV module during the turn-ON period are shown in Fig. 4.1.3.

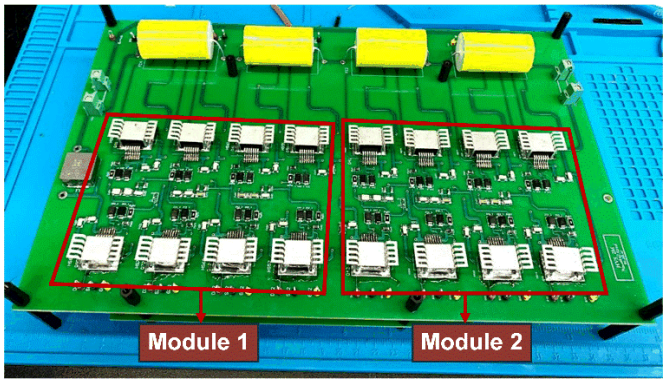


Fig. 4.1.1. (a) Modular HV switch

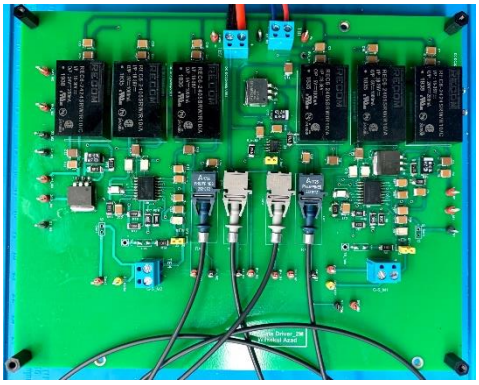


Fig. 4.1.1. (b) Modular HV isolated gate driver

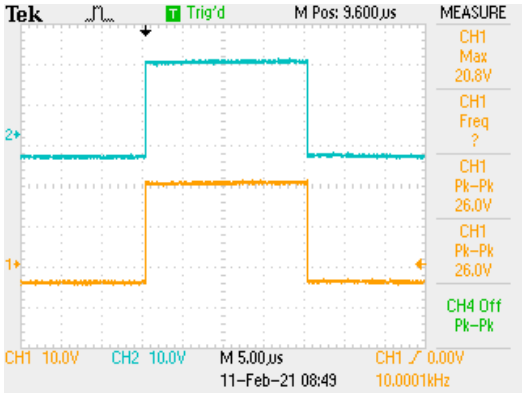
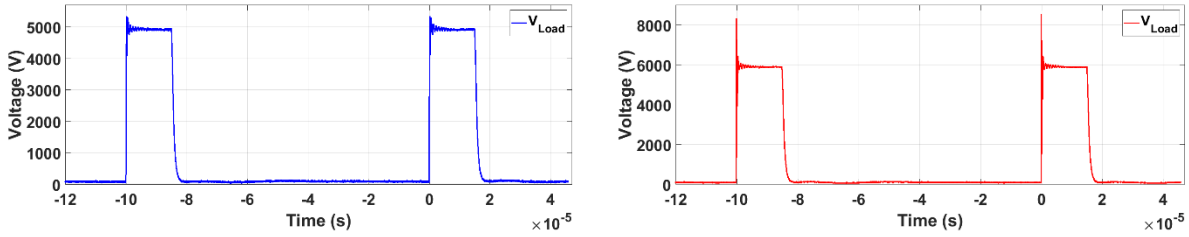


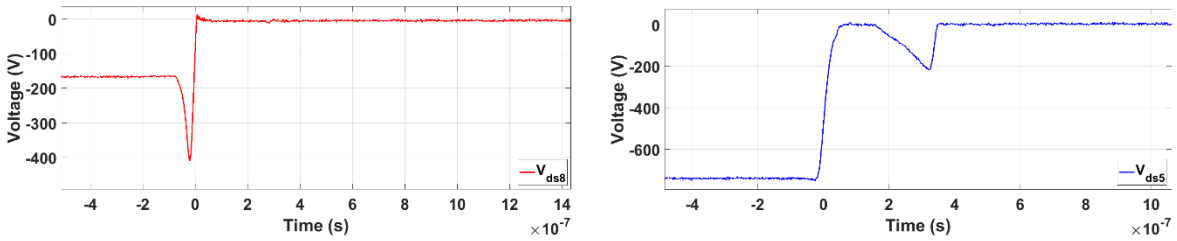
Fig. 4.1.1. (c) Identical gate drive signals originating from the modular gate driver

Fig. 4.1.1. (d) Compact assembly of HV switch and HV gate driver



(a) (b)

Fig. 4.1.2. Voltage measured across a 9.6 kΩ resistive load at (a) 5 kV (b) 6 kV



(a) (b)

Fig. 4.1.3. Turn-ON transient at 4 kV of the (a) 4th and 8th switch (rise time ≈ 11 ns) (b) 1st and 5th switch (rise time ≈ 23 ns)

5.0 Tradespace Analysis of Ultra-Wide-Band Antenna Arrays

5.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

5.1.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wide-band antenna elements in a phased array for HPM transmissions.

Deficiency in SOTA: Large physical aperture size.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters – via a D/Q (Directivity/Quality Factor) technique; followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area.

Relevance to OSPRES Grant Objective: Provides design and optimization (in terms of directivity or gain and bandwidth) guidelines for ultra-wideband ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN–APR 2021 / Code complete; testing initiated.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN–MAY 2021 / ongoing.

(C) Build minimum viable validation prototypes on polyethylene and FR-4 substrates that have good power handling capabilities for HPM transmissions at UHF range / JAN–MAY 2021 / Completed modeling antenna on FR-4 substrate; ongoing investigations into polyethylene substrate based antennas.

(D) Complete time-domain analysis of the antennas subjected to input short pulses / FEB–MAY 2021 / Ongoing.

5.1.3 Progress Made Since Last Report

(A) Developing Array Pattern Tool:

a. The MATLAB tool, developed for faster approximation of array radiation pattern, is currently being tested for different array aperture areas and lattice types (triangular and/or hexagonal lattice).

b. Preparing Invention Disclosure form.

(B) Investigations into aperture area reduction:

a. Completed investigations into aperture area reduction of array structures on infinite ground plane and on various lattice types (square/rectangular and hexagonal).

b. A method to characterize large microstrip patch antenna array structures ($\geq 15 \times 15$) on finite grounded substrates is being investigated to reduce computation time and memory usage.

(C) Building minimum viable validation prototypes:

a. U-slot rectangular microstrip patch antenna has been modeled, via FEKO, at a center frequency of 1.1 GHz on a 0.7-inch G10/FR4 substrate ($\varepsilon_r = 5.2, \tan\delta = 0.025$).

b. The prototype is currently being manufactured.

c. Preparing manuscript for IEEE AP-S Magazine based on bandwidth enhancement technique of probe-fed wideband electrically small microstrip patch antenna elements.

5.1.4 Significant Finding(s) and Mission Impact

(B) Building minimum viable validation prototypes:

The geometry of the U-slot microstrip patch antenna, designed to operate at a center frequency of 1.1 GHz, is shown in Fig. 5.1.1. Using this antenna, a 21.76% 2:1 VSWR bandwidth and 4.57 dBi of maximum gain has been achieved. The FEKO simulated VSWR and gain of the antenna, as functions of frequency, are illustrated in Fig. 5.1.2.

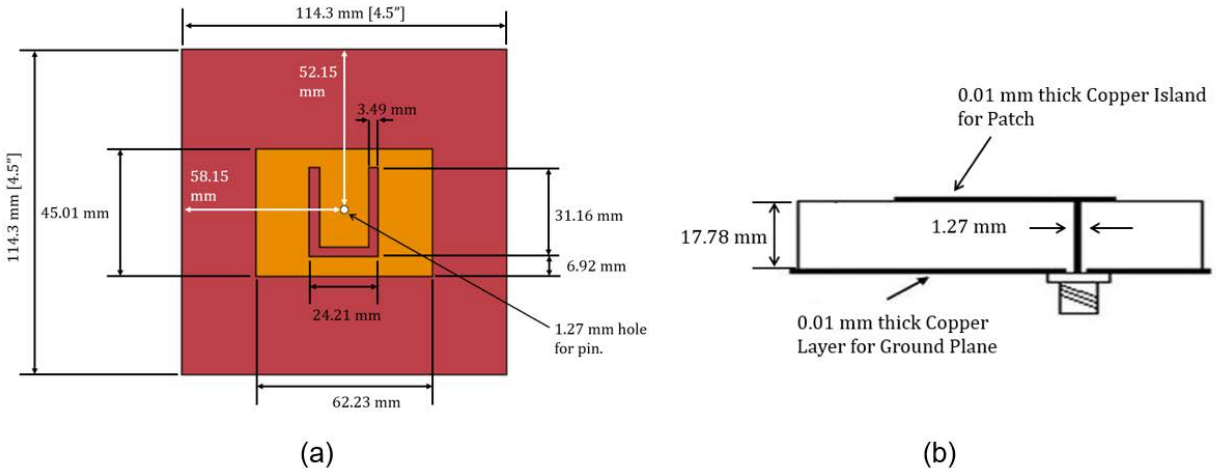


Fig. 5.1.1. (a) Top- and (b) side-view of the simulation model of the coaxial probe-fed U-slot microstrip patch antenna on G10/FR-4 substrate.

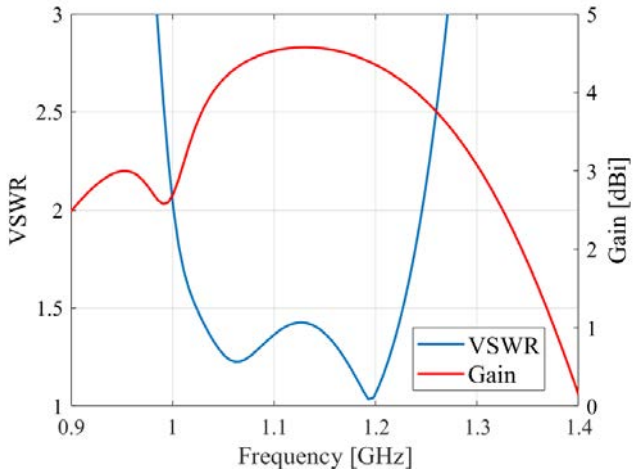


Fig. 5.1.2. Simulated VSWR and gain of the U-slot patch antenna.

Manufacturing of the antenna has been initiated. The partially manufactured prototype is shown in Fig. 5.1.3. The measured S_{11} parameter of the partially manufactured prototype is compared against the corresponding simulated S_{11} results (see Fig. 5.1.4).

Comparison of the measured and the simulated antenna parameters (VSWR and gain) will be furnished in the next report.

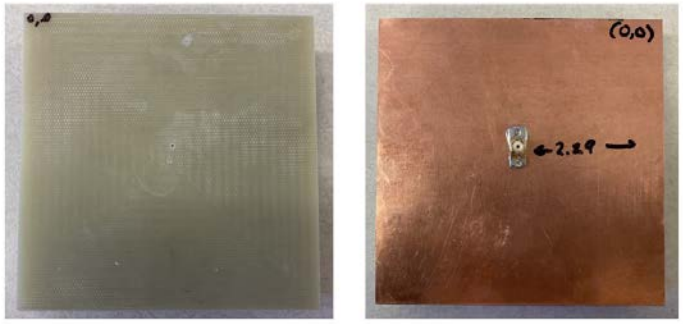


Fig. 5.1.3. (a) Top and (b) Bottom view of the partially manufactured prototype (which has a copper plate backed G10/FR-4 substrate along with the SMA connector – the U-slotted copper patch will be attached next).

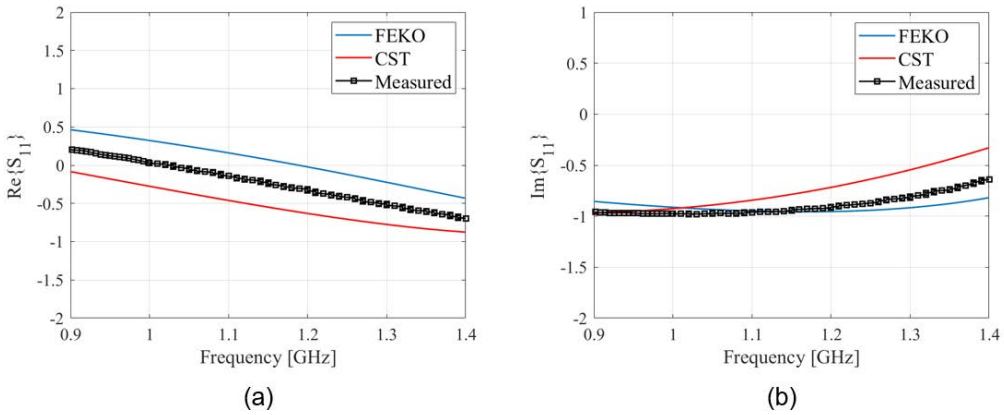


Fig. 5.1.4. Comparison of the simulated and the measured (a) real and (b) imaginary S_{11} parameters of the partially manufactured prototype of Fig. 5.1.3.

5.2 Tradespace Analysis of Other Ultra-Wide-Band (UWB) Single Elements

(Kalyan Durbhakula)

5.2.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelov antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up

an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem: The total surface currents on the Koshelov antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not clearly understood yet.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelov antenna that effectively reduces its physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelov antenna has been shown in the literature to withstand higher voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelov antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelov antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelov antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelov antenna.

(iii) The large electrical size (>5λ) of the Koshelov antenna at its highest operating frequency poses huge computational challenges. Efforts are underway to cleverly select important design parameters for the tradespace study.

5.2.2 Tasks and Milestones / Timeline / Status

(A) Complete literature search in an effort to identify and list antenna elements that satisfy UWB properties and HPM requirements, and downselect accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelov antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB-MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelov antenna to at least 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t, \phi, \theta)$) in receive or transmit mode.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelov antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size. This code should work for any type of antenna element given the input excitation signal and radiated electric field signal with its observation distance, elevation, and azimuth angles. This feature is currently not available in commercial electromagnetic solvers such as CST and FEKO. / FEB–MAR21 / 90% Complete.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze (**NEW**) / MAR–APR21 / Ongoing.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 7:1 bandwidth, rE/V greater than 1, peak gain around 13 dBi, aperture efficiency of 90% at center frequency, FWHM less than 300 ps, and ringing less than 300 ps.

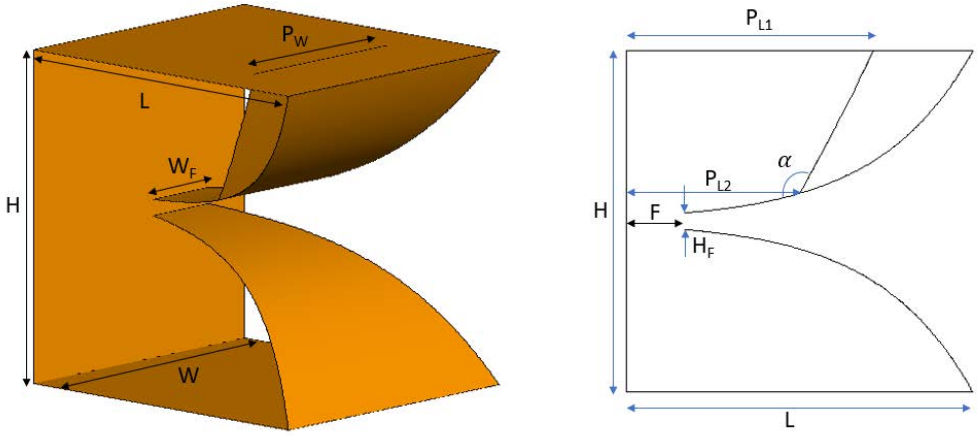
Milestone: Build an array model using the optimized design parameters.

(F) Continue with the literature search and improving our understanding on special electromagnetic (EM) techniques to determine their applicability to the antennas under consideration. The special EM techniques include: inductive loading, dielectric embedding, dielectric loading, electromagnetic bandgap structure, resistive terminations, beveling and creating slots, defected ground structures, iterative projection method, dielectric/metamaterial lens, array lattice configuration (square vs rectangular vs triangular vs hexagonal vs sunflower, etc.), subarray overlapping, E-plane and H-plane array, and subarray placements./ JAN–APR21 / Ongoing.

5.2.3 Progress Made Since Last Report

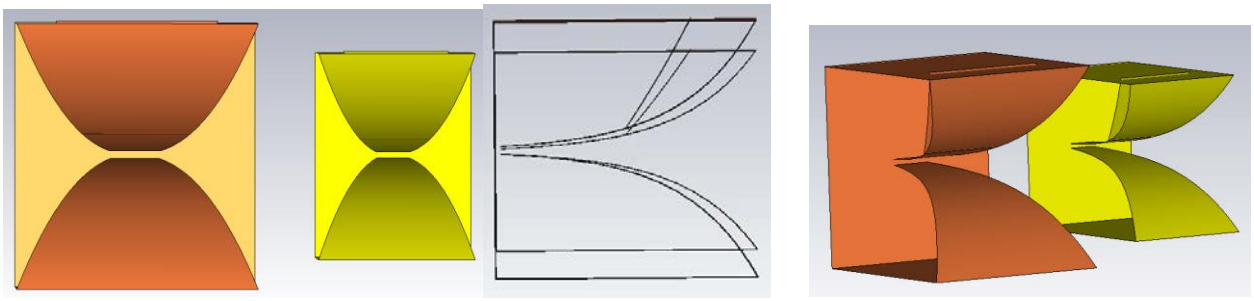
(C) In February, a preliminary tradespace study has been carried out for multiple design parameters of the Koshelov antenna, which is shown in Fig. 5.2.1. Those design parameters are the width, length, feed position, and the angle (alpha) between center adjusting plate and the top exponential flare. Initial results confirmed that the width (W) parameter has significant impact on the antenna metrics. The value of width reported in the previous MSR was 300 mm. Therefore, the width value has been decreased from 300 mm to 150 mm with an interval of 50 mm. In Fig. 5.2.2, the orange Koshelov antenna has

a width of 300 mm, which gives a physical aperture area of 0.0785 m^2 and the yellow Koshelov antenna has a width of 150 mm, which gives a physical aperture area of 0.0395 m^2. The other two widths (250 mm and 200 mm) yield a physical aperture area between 0.0785 m^2 and 0.0395 m^2. All other design parameters were kept constant and are listed in the Fig. 5.2.1 label/caption.



(a) (b)

Fig. 5.2.1. Koshelov antenna with design parameters. Width (W) has been varied for tradespace study, which also varies H. Other parameter values which are considered to be constant are reported here: L = 300 mm, W_F = 70 mm, P_W = 169 mm, F = 50 mm, H_F = 14.3 mm, P_{L1} = 150 mm, P_{L2} = 213 mm, and α = 26.86°. (a) 3D view, and (b) side view



(a) (b) (c)

Fig. 5.2.2. The orange Koshelov antenna is the original antenna shown in [1] and Fig. 5.2.1, whereas the yellow Koshelov antenna is the proposed one with reduced physical aperture area. (a) Front view, (b) side view, and (c) 3D view.

(D) Substantial progress was made on scripting a MATLAB/Python code that can import excitation signal and radiated electric field signal from CST simulations for the Koshelov antenna and calculate impulse response, FWHM, and ringing.

5.2.4 Significant Finding(s) and Mission Impact

(A) The extensive literature search on various UWB antenna elements has resulted in finding three promising antenna elements. The down selected antenna elements are the Koshelov, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the single antenna element. Later, the single antenna element will be converted into a planar array.

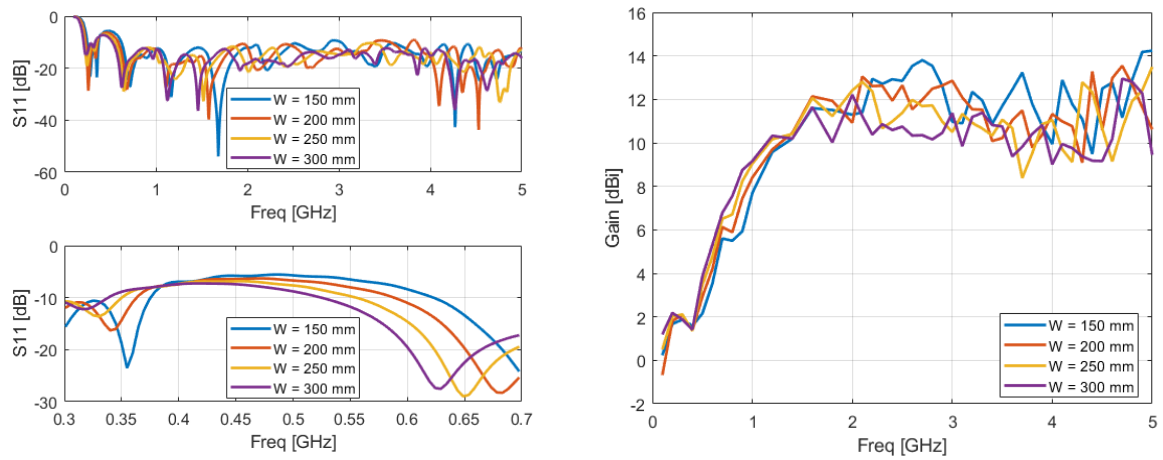
(B) The initial tradespace study and analysis of the Koshelov antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between Koshelov antenna in [1] and aperture reduced Koshelov antenna are shown in Table 5.2.1. From Table 5.2.1, it is evident that the physical aperture area has been reduced by 50% with a minimal and potentially acceptable tradeoff in bandwidth (200-MHz in 4.5-GHz) and peak gain (from 9.4- to 7.7-dBi). In addition, by reducing the physical aperture area (0.08- to 0.04-m^2), the aperture efficiency (80 to 100%) and rE/V (1.25 to 1.6) have improved.

Other antenna metrics such as peak and average power handling capability, electronic beam steering capability, effective radiated power (ERP), Q-factor, power spectral density, fidelity factor, and energy density will be added gradually in future MSRs.

Table 5.2.1. Antenna metrics

Antenna element type		Koshelov [1] & JAN MSR	Koshelov Proposed 1	Koshelov Proposed 2	Koshelov Proposed 3
Dimensions (L×H×W)		300 mm × 268 mm × 293 mm	300 mm × 268 mm × 245 mm	300 mm × 240 mm × 219 mm	300 mm × 208 mm ×190 mm
Physical Aperture area		0.0785 m^2	0.0659 m^2	0.0527 m^2	0.0395 m^2
Bandwidth		10:1 f_L = 0.5 GHz, f_U = 5 GHz	8.33:1 f_L = 0.6 GHz, f_U = 5 GHz	7.69:1 f_L = 0.65 GHz, f_U = 5 GHz	7.14:1 f_L = 0.7 GHz, f_U = 5 GHz
Peak gain (1 GHz)		9.4 dBi	9.06 dBi	8.41 dBi	7.69 dBi
Half-Power Beamwidth (HPBW)	E-plane (1 GHz)	51°	59°	66.7°	71.9°
	H-plane (1 GHz)	53°	59°	64°	64.7°
Aperture Efficiency (1 GHz)		80%	87.40%	94.04%	100%
rE/V		1.25	1.35	1.49	1.6
FWHM		302 ps	329 ps	331 ps	338 ps
Ringing ($T_{ringing}$ = 0.1)		277 ps	405 ps	407 ps	362 ps

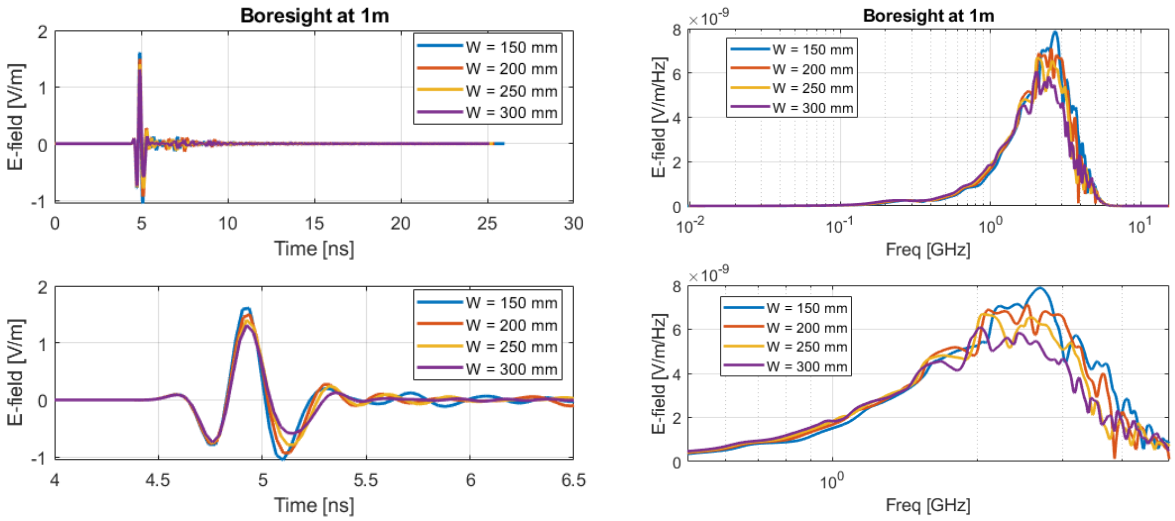
(C) The width of the Koshelov antenna has been varied over a pre-selected range and the corresponding reflection coefficient (S11) and gain as a function of frequency are shown in Fig. 5.2.3. Fig. 5.2.3a shows the full frequency range and a zoomed in (0.3 GHz to 0.7 GHz) frequency range to notice the shift in S11 as the width value increases. In Fig. 5.2.3a, as the width decreases from 300 mm (purple curve) to 150 mm (blue curve), the –10 dB lower frequency shifted from 0.5 GHz to 0.7 GHz. The S11 response above 0.7 GHz for all four width values have been relatively constant and stayed under –10 dB. In Fig. 5.2.3b, the gain at lower frequencies did not differ a lot when compared against each other, however, at high frequencies, some difference can be noticed. Overall, the gain curve did not vary drastically when the physical aperture area has been reduced by 50%.



(a) (b)

Fig. 5.2.3. (a) Reflection coefficient (S11) in dB and (b) Gain in dBi for four different width (W) values.

(C) The time domain electric field response to a Gaussian pulse at 1-meter distance from the aperture of Koshelov antenna is shown in Fig. 5.2.4a. The FFT of time domain E-field is shown in Fig. 5.2.4b. The maximum E-field can be seen for W = 150 mm and the minimum for W = 300 mm. Since the bandwidth for W = 150 mm is narrower than for W = 300 mm, the energy is more concentrated in a narrow bandwidth case, whereas the energy is spread out in the wider bandwidth case. The same observation can be deduced from Fig. 5.2.4b, which shows a spread out FFT for W = 300 mm and the opposite for W = 150 mm.



(a) (b)

Fig. 5.2.4. (a) Time domain electric field response to a Gaussian input pulse at 1-meter distance and (b) FFT of time domain electric field at 1-meter distance.

(D) The impulse response ($h_{rx/tx}(t, \phi, \theta)$) and the envelope of the impulse response ($|h_{rx}^{+}(t, \phi, \theta)|$) for the original Koshelov antenna shown in [1] at boresight are shown in Fig. 5.2.5. In Fig. 5.2.5, the top figure shows the full-time scale whereas the bottom figure shows the response between 4 ns and 6 ns to accurately calculate FWHM and ringing. To calculate ringing, a threshold value of 0.1 ($T_{ringing}$) has been assumed. From the envelope curve shown in Fig. 5.2.5, the FWHM is 302 ps and the ringing is 277 ps. The FWHM and ringing for the reduced aperture area Koshelov antennas can be found in Table 5.2.1.

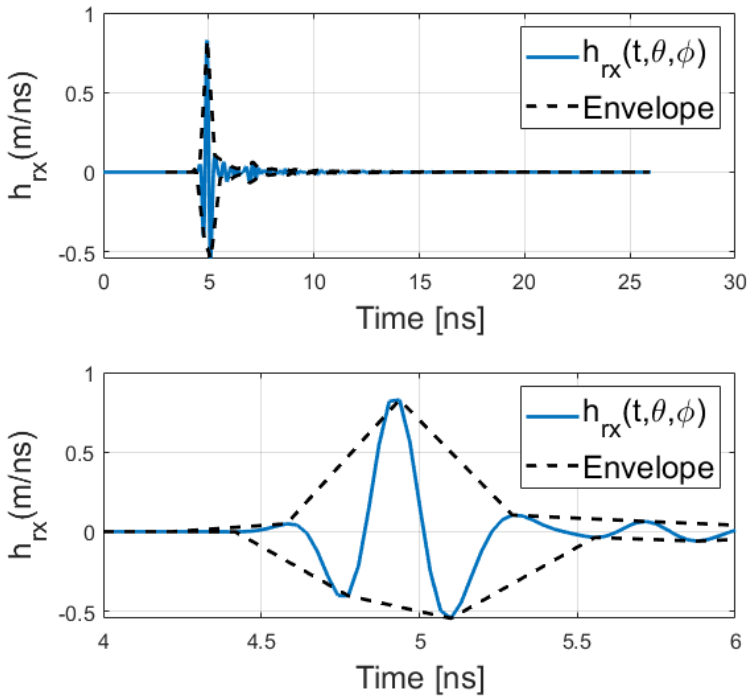


Fig. 5.2.5. Impulse response and the envelope of the impulse response for the original Koshelov antenna shown in [1] & JAN MSR.

5.2.5 References

[1] Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

5.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna

(Sadie Brasel and Kalyan Durbhakula)

5.3.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of Shark antenna elements whose miniaturization in two dimensions (height and width equal to $\lambda/4$ where λ corresponds to the lowest operating frequency) make it a good candidate for UWB HPM systems while having a reduced aperture area with respect to the current state-of-the-art. In the literature, the Shark antenna has already been shown to achieve a wide 20:1 impedance bandwidth, low dispersion, and a sectoral (also referred to as directional) radiation pattern.

Sub-Problem: The design parameter space of the Shark antenna has not been studied rigorously in the literature and therefore the effect of these parameters on the antenna metrics is not understood. In addition, the Shark antenna has been shown to be not very directive in the H-Plane. Preliminary studies have shown that aperture efficiencies at low frequencies are much better than at higher frequencies.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Explore the design parameter space for the Shark antenna element using computational electromagnetic (EM) wave solvers starting with the simulation and validation of a single element.

Relevance to OSPRES Grant Objective: The Shark antenna dimensions were established to be frequency dependent and can be readily modulated to fit the spectrum characteristics of an ultra-fast rise time input pulse.

Risks, Payoffs and Challenges:

(i) The Shark antenna is comprised of flare-angle-dependent bicones that are truncated in the azimuthal angle. This still yields considerably higher half power beam width (HPBW) than other antenna elements under investigation. The significant reduction of HPBW in the H-plane may be unattainable and can be considered a major risk.

(ii) Payoffs include the development of a library of antenna metrics data for various shapes and sizes of the bicones and reflector plates in the shark antenna.

(iii) Specific design challenges are yet to be identified; however, computational challenges remain clear with respect to automation of design parameter space on our currently used supercomputer (LEWIS).

5.3.2 Tasks and Milestones / Timeline / Status

(A) Complete initial design, simulation, and validation of the Shark antenna / JAN21 / Complete.

(B) Validate Shark antenna design through LEWIS supercomputer over a wider range of frequency results (up to 20 GHz) / FEB–MAR21 / Ongoing.

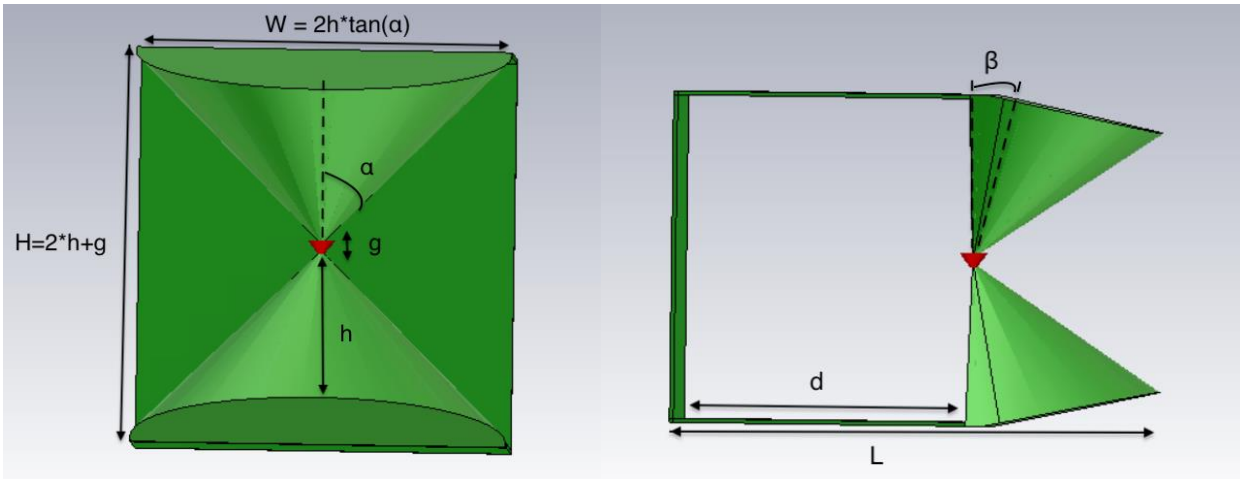
(C) Identify Shark antenna design parameters which contribute significantly to bandwidth, gain, and physical aperture area. Determine which parameters contribute most to performance improvement/size reduction. Flare angle (α), cone height (*h*), and distance to backplane (*d*) are initial parameters of interest / FEB–MAR21 / Parameters of interest have been chosen; determining which parameters contribute most to performance is ongoing.

(D) Perform a preliminary tradespace study by simulating the Shark antenna with the extreme cases of flare angle, cone length, and distance to backplane. Gain a general

understanding of how these parameters affect impedance bandwidth, rE/V, gain and HPBW / FEB21 / Complete.

(E) Perform a detailed tradespace study by simulating the Shark antenna with several cases of varying flare angle, cone length, and feed gap length.

- Milestone: produce a detailed summary of change in impedance bandwidth, rE/V, HPBW in H-plane and E-plane, full-width half maximum (FWHM), and ringing as a function of flare angle (α), cone height (*h*), and distance to backplane (*d*) / FEB–APR21 / Ongoing.



(a) (b)

Figure 5.3.1. Shark antenna design parameters: *d, h, g*, α, β

5.3.3 Progress Made Since Last Report

(D) A focused tradespace study for the Shark antenna has been planned and completed. Two extreme cases have been chosen for the cone height (*h*) and distance to backplane (*d*), and three cases have been chosen for the flare angle (α) (Table 5.3.1). The cases where $\alpha = 70°$, *H* = 60 mm, *d* =45 and 75 mm were electrically large, and not enough memory was available to simulate them, so results for these cases are not included. The frequency dependent dimensions and physical aperture areas are listed in Table 5.3.1 for each case. These parameters are functions of the total height (*H*), total width (*W*), and total length (*L*) of the Shark antenna, where $H = 2 * h + g$ and $W = 2 * R_b = 2h * \tan(\alpha)$. There is not a closed-form expression for the total length (*L*), so it is measured directly in the computational EM solver. The aperture efficiency is calculated for each case at the center frequency of 5.5 GHz. Aperture efficiency = $e = \frac{A_e}{A_{phs}}$ where $A_e = G * \frac{\lambda^2}{4\pi}$ is the effective aperture area and *G* is the max gain at the center frequency. $A_{phs} = W * H$ is the physical aperture area. The aperture efficiency is a measure of how well an antenna is radiating EM power.

(E) A plan for a more detailed tradespace study and analysis with an emphasis on reducing physical aperture area has been proposed (Table 5.3.2). This table is subject to change as we learn more about the Shark antenna design space and can identify certain cases as superfluous or choose to add more cases.

5.3.4 Significant Finding(s) and Mission Impact

(A) The Shark antenna has been designed and simulated according to [1]. (Figure 5.3.1)

(D) From Figure 5.3.2 it can be seen that the Shark antenna cases with a large flare angle (α) value are not well matched to the reference impedance of 150Ω. The more detailed parametric study will help determine an upper limit on the flare angle. The α = 20° and α = 45° cases are both well matched to the reference impedance over a wide range. From Figure 5.3.2, it can be seen that the smaller α values perform better at low as well as high frequencies.

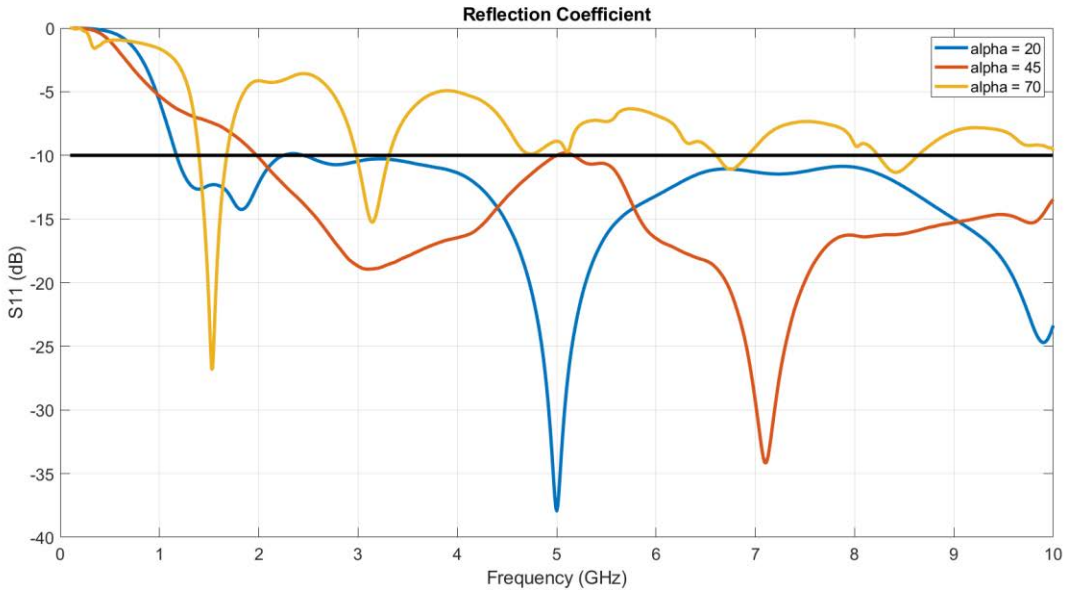
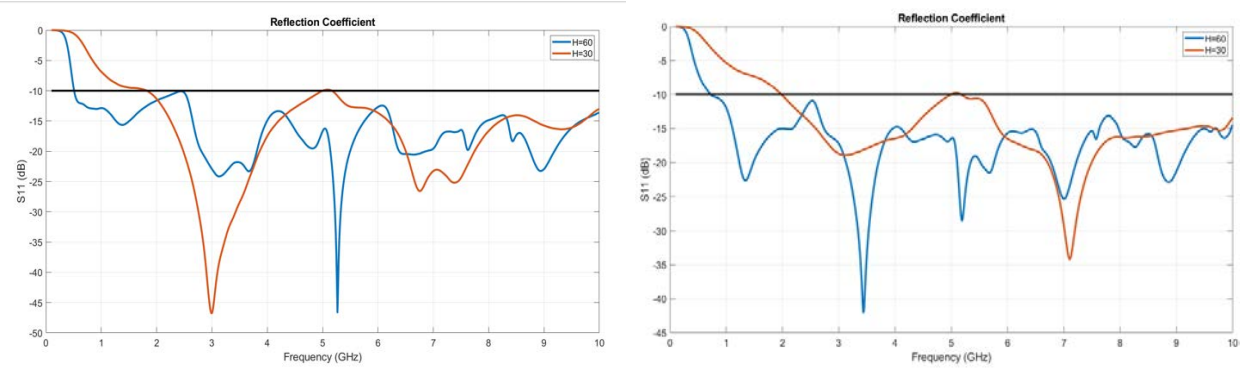


Figure 5.3.2. Reflection coefficient for *h* = 30 mm and *d* = 7 mm cases



(a) (b)

Figure 5.3.3. Reflection coefficient: (a) α = 45° *d* = 45 mm (b) α = 45° *d* = 75 mm

(D cont.) From Figure 5.3.3. the *h* = 60 mm case performs better than the *h* = 30 mm case for both values of *d*, as the reflection coefficient curve is below the –10dB line for a wider range of frequencies. The detailed parametric study will reveal if larger *H* values are consistently performing better than smaller ones. Based on Figure 5.3.4. the change in *d* values does not affect the reflection coefficient significantly. The *d* = 45 mm case performs slightly better at low frequencies. From the preliminary parametric study of the Shark antenna, it seems that the thinner the antenna is, the better it is matched to the reference impedance of 150Ω. Hence, smaller alpha values and larger *h* values result in better performance.

The thinner Shark antenna cases are also more directive in the H-plane, which is shown in Figure 5.3.5 and Figure 5.3.6. Figure 5.3.5. shows the directivity pattern in the H-Plane. Directivity is a ratio of the power density radiated in each direction to the power density emitted by an ideal isotropic radiating element. Figure 5.3.6. on the other hand is a transient radiation pattern. The field range product per volt accepted (rE/V) is plotted at various azimuth angles. The field range product per volt is the ratio of the peak radiated electric field 1 m away from the antenna to the maximum voltage level of the input pulse. The HPBW values calculated from Figure 5.3.5 are (a) 228.5° (b) 79.5°. The HPBW values calculated from Figure 5.3.6 are (a) (b) 200°.

From Table 5.3.1 it is clear that Shark antenna cases with a larger physical area have a larger maximum gain at the center frequency (5.5 GHz) and have smaller average aperture efficiencies. Therefore, the case with the most optimal aperture efficiency is the case with the smallest overall size (highlighted in green in Table 5.3.1).

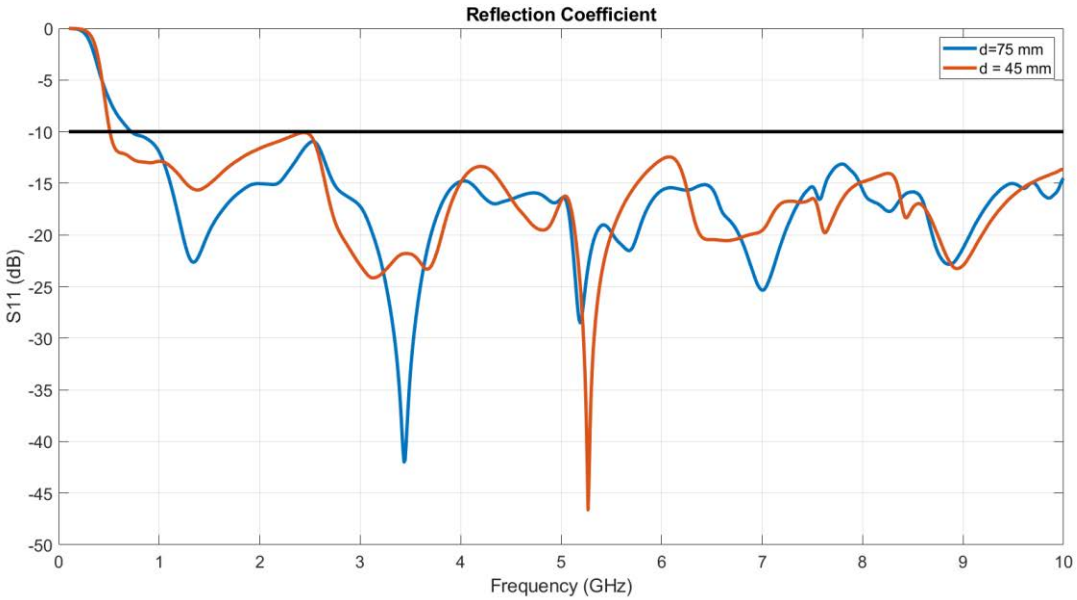
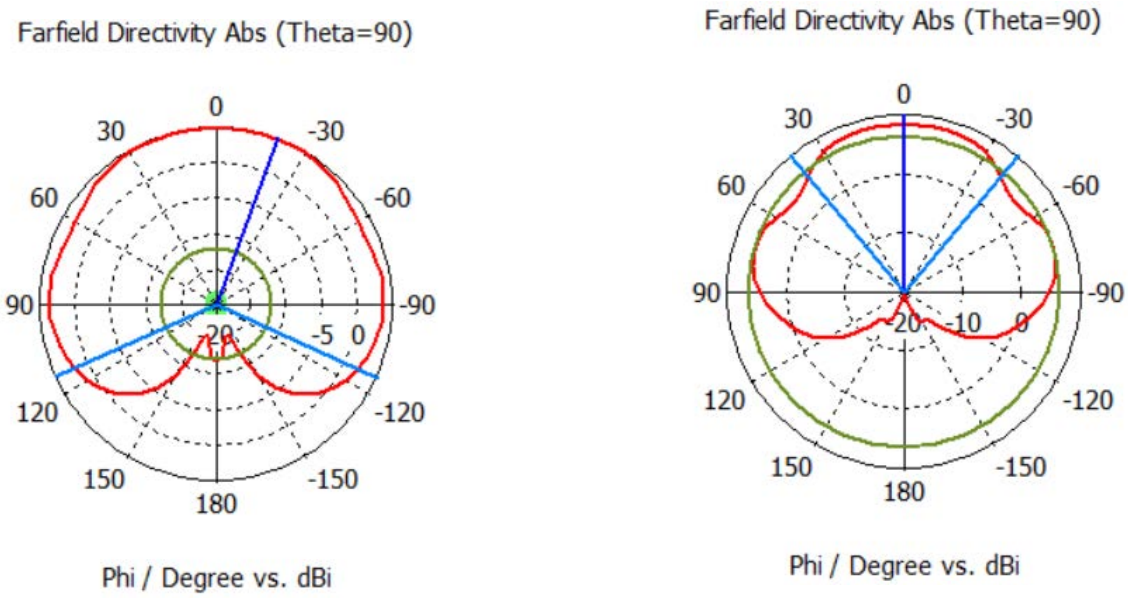


Figure 5.3.4. Reflection coefficient: α = 45° h = 60 mm



(a) (b)

Figure 5.3.5. H-Plane Radiation Pattern: (a) α = 45° h = 30 mm d = 45 mm

(b) α = 45° h = 60 mm d = 45 mm

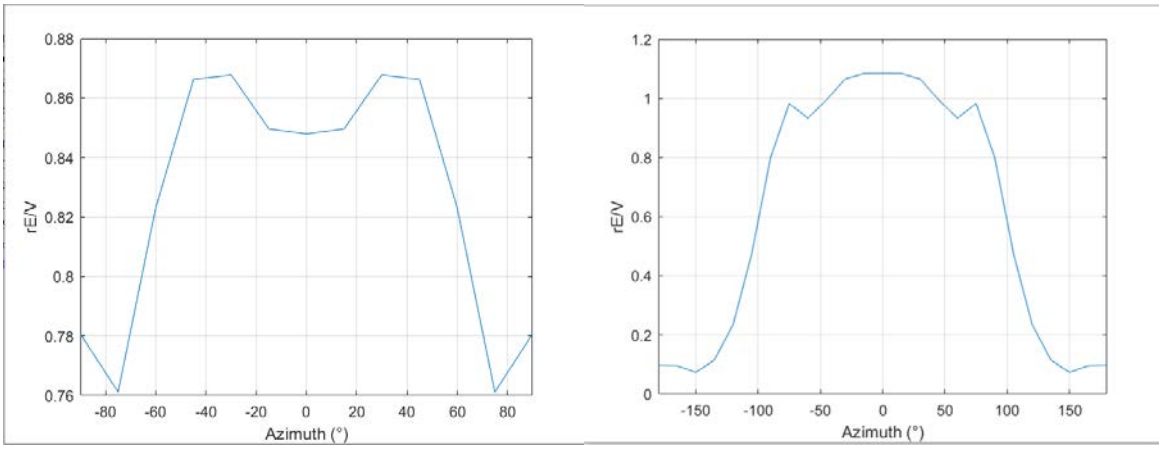


Figure 5.3.6. H-Plane transient radiation pattern: (a) α = 45° *h* = 30 mm *d* = 45 mm (b) α = 45° *h* = 60 mm *d* = 45 mm

Table 5.3.1 Shark parametric study results

H	d	Flare Angle	Frequency Dependent Dimensions (W,H,L) $\lambda = \frac{c}{5.5e9}$	Physical Aperture area $A_{phs} = W * H$	Bandwidth	Lowest Cutoff Frequency	Peak gain (5.5 GHz)	Directionality (5.5 GHz)		Aperture Efficiency (%) (5.5 GHz)
								E-plane	H-plane	
30 mm	75 mm	20°	$\frac{\lambda}{2.497}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.59177}$	~0.001354 m^2	>10:1	1.168 GHz	3.534 dBi	48.7°	188.2°	61.79525764
		45°	$\frac{\lambda}{0.909}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.492}$	~0.00372 m^2	>10:1	2 GHz	4.874 dBi	89.1°	97.8°	31.02057555
		70°	$\frac{\lambda}{0.3349}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.337}$	~0.01022 m^2	Poor BW	1.39 GHz	5.573 dBi	49°	200°	12.91056991
60 mm	75 mm	20°	$\frac{\lambda}{1.249}, \frac{\lambda}{0.447}, \frac{\lambda}{0.5}$	~0.00533 m^2	>10:1	0.625 GHz	5.196 dBi	107.4°	69.4°	23.08071189
		45°	$\frac{\lambda}{0.455}, \frac{\lambda}{0.447}, \frac{\lambda}{0.373}$	~0.01464 m^2	>10:1	0.731 GHz	6.813 dBi	30°	54.4°	11.01804594
		70°	$\frac{\lambda}{0.165}, \frac{\lambda}{0.447}, \frac{\lambda}{0.220}$	~0.0402 m^2						
30 mm	45 mm	20°	$\frac{\lambda}{2.497}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.59857}$	~0.001354 m^2	>10:1	1.219 GHz	3.959 dBi	39.8°	125.6°	69.22677561
		45°	$\frac{\lambda}{0.909}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.492}$	~0.00372 m^2	>10:1	1.793 GHz	4.850 dBi	46.3°	228.5°	30.86782754
		70°	$\frac{\lambda}{0.331}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.413}$	~0.01022 m^2	Poor BW	1.453 GHz	5.402 dBi	120.1°	73.9°	12.51442646
60 mm	45 mm	20°	$\frac{\lambda}{1.249}, \frac{\lambda}{0.447}, \frac{\lambda}{0.699}$	~0.00533 m^2	>10:1	0.644 GHz	4.653 dBi	82.8°	73.6°	20.66869754
		45°	$\frac{\lambda}{0.455}, \frac{\lambda}{0.447}, \frac{\lambda}{0.473}$	~0.01464 m^2	>10:1	0.512 GHz	8.425 dBi	37.1°	79.5°	13.62498708
		70°	$\frac{\lambda}{0.165}, \frac{\lambda}{0.447}, \frac{\lambda}{0.249}$	~0.0402 m^2						

Table 5.3.2. Detailed Shark antenna parametric cases to be run .

h (mm)	Flare Angle (α)											d (distance from cones to backplane)	Feed Gap (g)	β	wire radius
30	20	25	30	35	40	45	50	55	60	65	70	75 mm	2 mm	12°	0.3 mm
35	20	25	30	35	40	45	50	55	60	65	70				
40	20	25	30	35	40	45	50	55	60	65	70				
45	20	25	30	35	40	45	50	55	60	65	70				
50	20	25	30	35	40	45	50	55	60	65	70				
55	20	25	30	35	40	45	50	55	60	65	70				
60	20	25	30	35	40	45	50	55	60	65	70				
30	20	25	30	35	40	45	50	55	60	65	70	45 mm			
35	20	25	30	35	40	45	50	55	60	65	70				
40	20	25	30	35	40	45	50	55	60	65	70				
45	20	25	30	35	40	45	50	55	60	65	70				
50	20	25	30	35	40	45	50	55	60	65	70				
55	20	25	30	35	40	45	50	55	60	65	70				
60	20	25	30	35	40	45	50	55	60	65	70				

5.3.5 References:

[1] L. Desrumaux, A. Godard, M. Lalande, V. Bertrand, J. Andrieu and B. Jecko, "An Original Antenna for Transient High Power UWB Arrays: The Shark Antenna," in IEEE Transactions on Antennas and Propagation, vol. 58, no. 8, pp. 2515- 2522, Aug. 2010, doi: 10.1109/TAP.2010.2050418.

5.4 Tradespace Analysis of Ultra-Wide-Band (UWB) Fractal Antenna

(Sai Indharapu and Kalyan Durbhakula)

5.4.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. The fractal antenna packs multiple resonances closely spaced together to

generate an UWB response, thereby effectively utilizing the 2D space (i.e., the radiating patch space). Its high degree of freedom provides an opportunity to develop systematically modified patch shapes which in turn leads to improved bandwidth while retaining high fidelity factor values.

Sub-Problem: Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

Relevance to OSPRES Grant Objective: Fractal antennas satisfy the UWB criteria of the OSPRES grant objective relatively in a smaller aperture area when compared against SOTA BAVA, dual ridge horn antennas etc., which usually take up significantly larger physical space over the same frequency range. Furthermore, the microstrip design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need for building a separate feed network using external and bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be considered to be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

5.4.2 Tasks and Milestones / Timeline / Status

(A) Complete tradespace analysis of the fractal element radius *b* over the desired frequency range (4 GHz to 12 GHz) using genetic algorithm (GA) optimization available in FEKO with the goal to minimize reflection coefficient (< –10 dB) / FEB21 / Complete.

(B) Perform tradespace study on different fractal shapes by changing the number of segments of fractal elements to understand the segment effect on the impedance bandwidth / FEB21 / Complete.

(C) Continue with GA optimization of fractal side length *b* over a wide frequency range (2 GHz to 12 GHz with 201 discrete frequency points), and number of fractal segments using OPTFEKO on LEWIS cluster. The goal is to reduce physical aperture area by 10% of its present design and demonstrate minimal or no change in S11, gain, and fidelity factor values / MAR21 / Ongoing.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a*, to further reduce the aperture area and improve aperture efficiency (>50%). / MAR21 / Ongoing.

(E) Demonstrate correlation between transmitted and radiated signals, by calculating fidelity factor using (1) where $S(t)$ and $r(t)$ are transmitted and radiated signals, respectively. The goal is to achieve and maintain fidelity factor values equal to or greater than 0.9 / MAR21 / Ongoing.

$$F = max \left| \frac{\int S(t) r(t-r) dt}{\int S(t)^2 . \int r(t)^2 dt} \right| \quad (1)$$

5.4.3 Progress Made Since Last Report

(A) Fractal element radius optimization

(A1) The optimizer OPTFEKO is used for optimizing value *b* to achieve a predefined response by using the search-based optimization method GA.

(A2) Results from the OPTFEKO showed that the optimum value for *b* is 1.66 mm as opposed to 1.8 mm obtained from preliminary parametric study.

(B) Trade space study on different fractal shapes

(B1) Number of fractal segments (*N*) in fractal structure is varied from 3 to 14 with radius *b* (= 1.66) as shown in Figure 5.4.1.

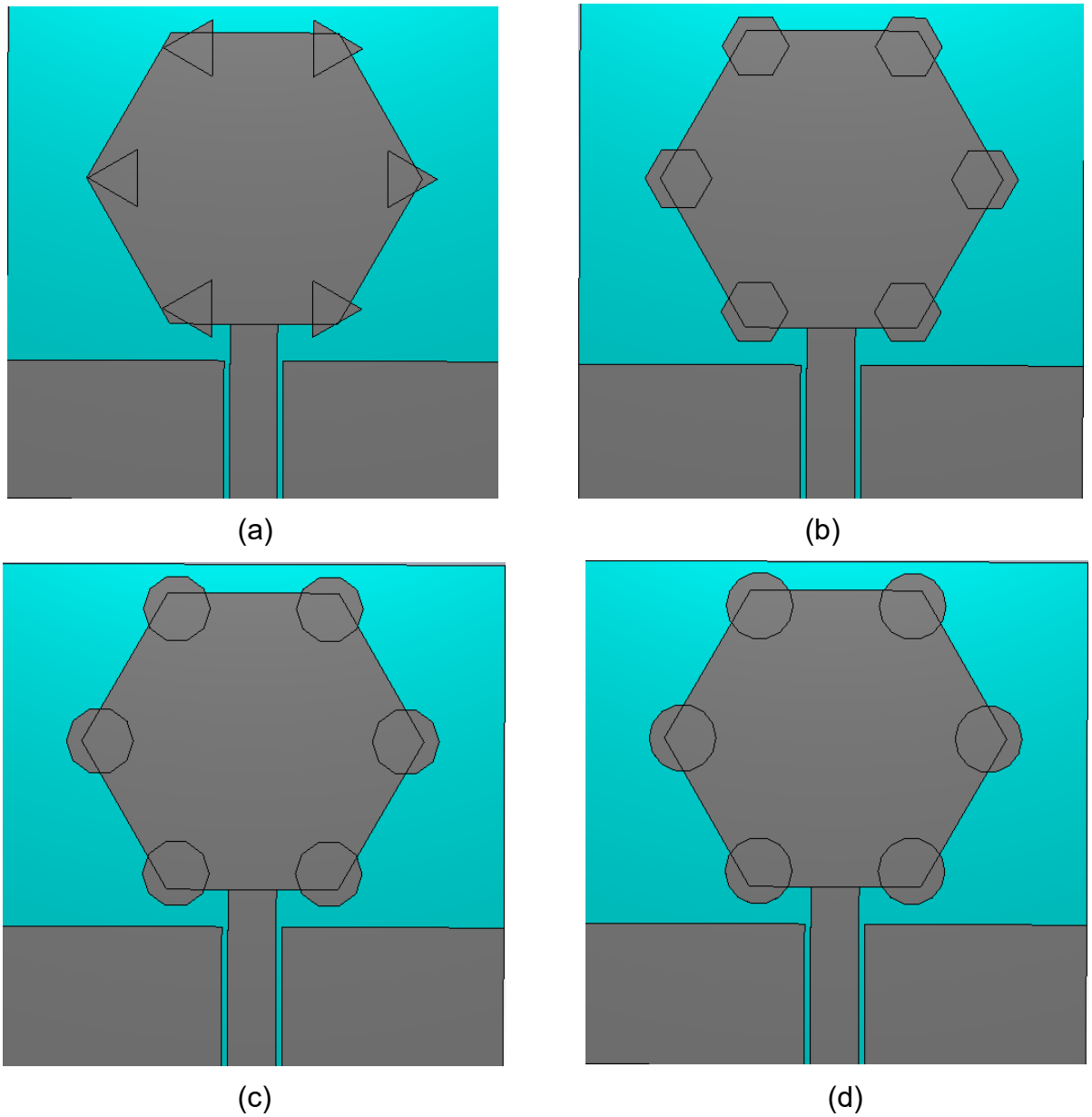


Figure 5.4.1. Fractal antenna with (a) *N* = 3, (b) *N* = 6, (c) *N* = 10, and (d) *N* = 14.

5.4.4 Significant Finding(s) and Mission Impact

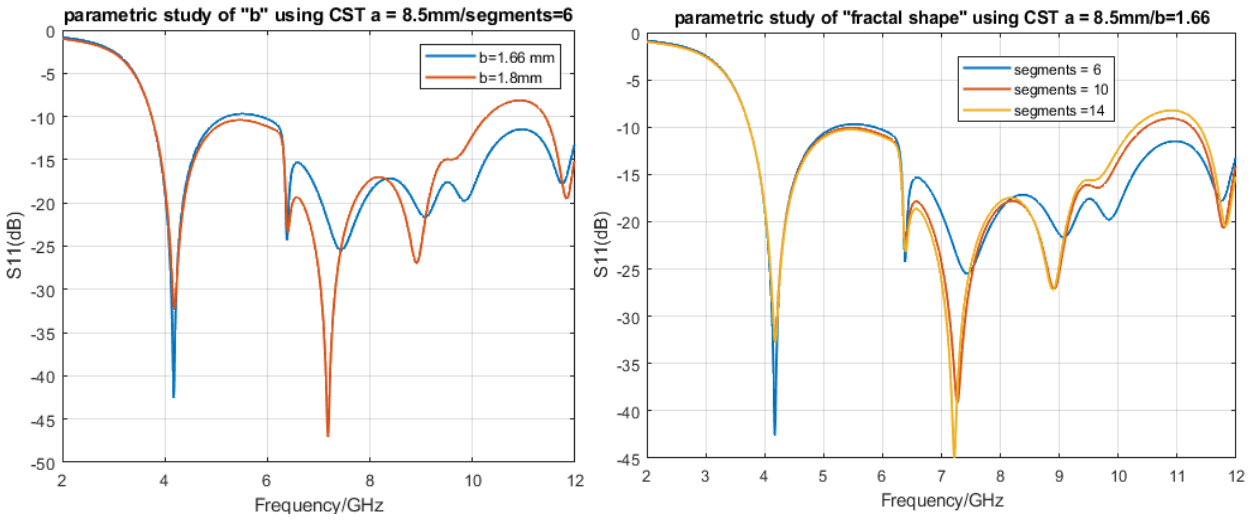
(A) The initial analysis of the simulation results with fractal radius *b* equal to 1.8 yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO has been used as an optimization tool with fractal radius *b* as the optimization variable. The optimum value for *b* is found to be 1.66 mm. The optimization is carried out over 51 discrete frequency points. Figure 5.4.1 (a) illustrates the improvement in bandwidth with optimum *b* value, i.e., 1.66 mm.

(B) The addition of fractal elements to the simple hexagon improved antenna metrics such as return loss. To further investigate and understand the fractal elements, the number of

segments in the fractal geometry has been varied. S11 response for antenna with *N* = 6, 10, and 14 is shown in Figure 5.4.1 (b) to illustrate the improvement. With increase in value of *N* from 6 to 14 the curve peak at 5 GHz shifts below –10 dB line. Conversely, the S11 shifts above –10 dB line between 10 GHz and 12 GHz as the value of *N* is increased from 6 to 14.

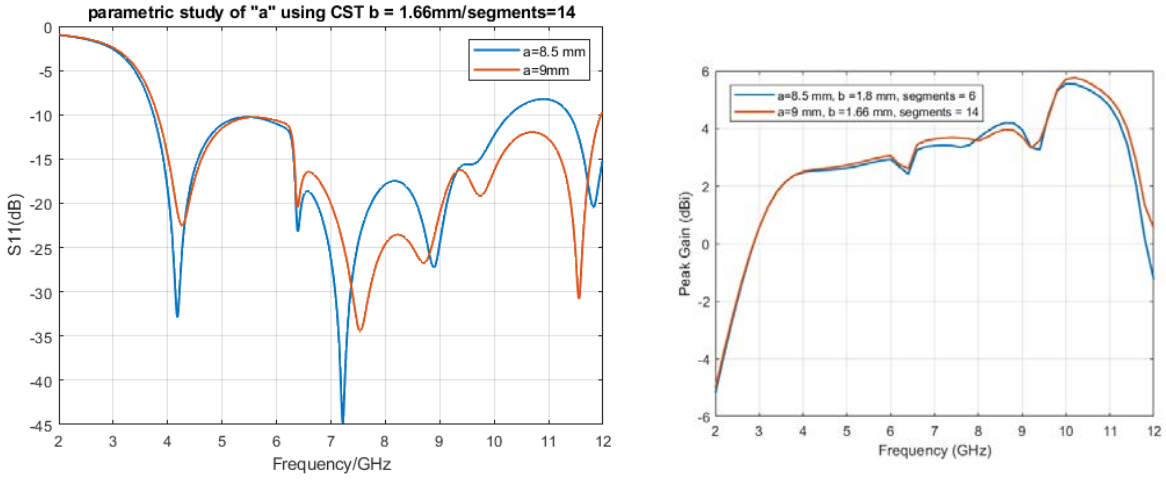
(D) In order to further increase the bandwidth, the hexagon radius *a* has been slightly increased, which resulted in improved response as shown in Figure 5.4.3 (a). Other parameters such as fractal radius *b* and number of fractal segments in fractal geometry are kept same (i.e. *b* = 1.66 and *N* = 14). Finally, Fig. 5.4.3 (b) shows the peak gain over frequency for the parameter values (*a* = 8.5 mm, *b* = 1.8 mm, *N* = 6) reported in JAN MSR and optimized parameter values (*a* = 9 mm, *b* = 1.66 mm, *N* = 14). Furthermore, Fig. 5.4.4 (a) shows time domain electric field response to a Gaussian input pulse at boresight 1-meter distance for *b* = 1.66 mm *and b* = 1.8 mm. Similarly, Fig. 5.4.4 (b) shows FFT of the time domain E-field.

(D) Antenna metrics comparison between original fractal antenna design (reported in JAN MSR) and the optimized fractal antenna is shown in Table 5.4.1. From Table 5.4.1 third column, it is evident that the impedance bandwidth ratio, and peak gain values (at center frequency) have reasonably improved. However, the aperture efficiency reduced by about 28%. The FWHM and ringing values in both cases are below 300 ps.



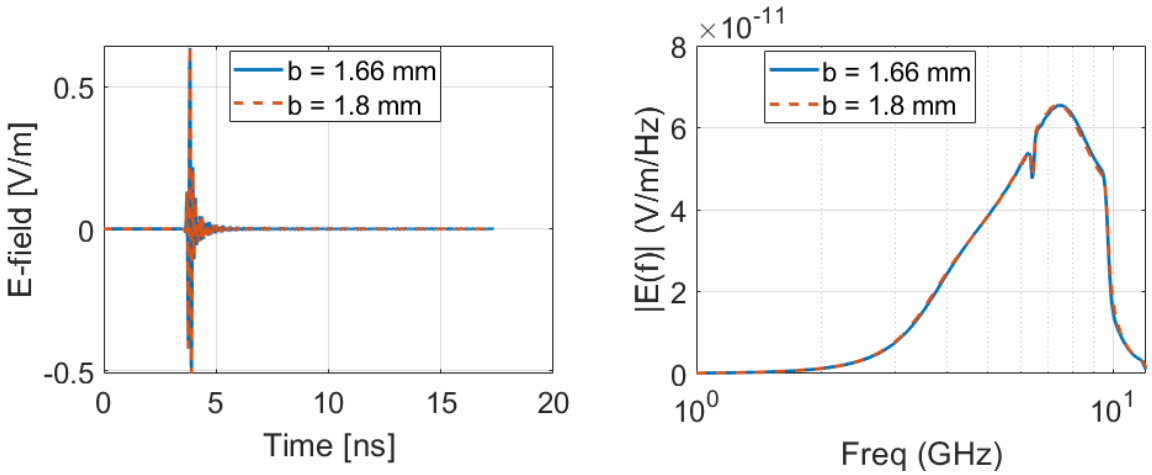
(a) (b)

Figure 5.4.2. Reflection coefficient of (a) antenna geometry with different *b* values, and (b) antenna geometry with different number of fractal segments (shapes).



(a) (b)

Figure 5.4.3. (a) Reflection coefficient of antenna geometry with two *a* values, and (b) gain vs. frequency.



(a) (b)

Figure 5.4.4. (a) Time domain electric field at boresight 1-meter and (b) FFT of time domain E-field at boresight 1-meter.

Table 5.4.1. Antenna metrics

Antenna element type	Original fractal antenna (a = 8.5 mm, *b* = 1.8 mm, N = 6 & fc = 6.65 GHz) [Reported in JAN MSR]	Optimized fractal antenna (a = 9 mm, *b* = 1.66 mm, N = 14 & fc = 7.8 GHz)

Substrate Dimensions (mm)		25 × 25 × 1	25 × 25 × 1
Radiating Patch Dimensions (mm)		18.8 × 16.28	18.52 × 16.4
Physical Aperture area (mm^2)		0.306	0.303
Bandwidth		2.5:1 f_L = 3.8 GHz, f_U = 9.5 GHz	3:1 f_L = 4 GHz, f_U = 12 GHz
Peak gain (dBi) at f_C		3.56	3.98
Half-Power Beamwidth (HPBW)	E-plane (f_C)	69°	63.4°
	H-plane (f_C)	71°	57.5°
Aperture Efficiency (f_C)		120%	92%
rE/V		0.6	0.6
		225 ps	243 ps
Ringing ($T_{ringing}$ = 0.05)		235 ps	248 ps

5.4.5 References

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

6.0 RF Coupling

6.1 Enclosure Effects on RF Coupling

(Mohamed Hamdalla and Ahmed Hassan)

6.1.1. Problem Statement, Approach, and Context

Primary Problem: Slots and gaps are introduced in casings/enclosures due to a variety of practical reasons which might compromise their shielding, creating upset susceptibility to the enclosed electronics. The goal of this work is to quantify how the thresholds for upset susceptibility of enclosed wires and integrated circuits differ from those in free space.

Solution Space: Study enclosures with different shapes, material compositions, and slots to quantify their effect on RF coupling to the enclosed wires and electronics typically used in UAVs. The study will focus on the low-frequency range where the incident wavelength is comparable to the size of the enclosure or larger.

Sub-Problem: UAVs are manufactured with a wide variety of shapes and composites to accomplish an exponentially expanding list of missions. The configurations previously reported in the literature have simplistic assumptions regarding the shape and material composition of UAV enclosures that might overestimate or underestimate susceptibility.

State-of-the-Art (SOTA): Simple statistical analysis of specific enclosure configurations using either brute force simulations/measurements or pure statistical methods.

Deficiency in the SOTA: Brute force simulations/measurements of the voltages and currents induced in wires and integrated circuits contained in enclosures are computationally or experimentally complex and have several limitations. The computations are complicated by the multiscale nature of the simulations, and the experiments are complicated by the cost of the equipment and the extensive time needed to measure every variation to cover all possible scenarios. Statistical methods, such as the Random Coupling Model (RCM) for example [1], are only accurate for high frequencies where the wavelength is much smaller than the size of the enclosure. Another main deficiency of RCM is that it can't predict the exact induced voltages and currents for a specific well-characterized system but it only provides the statistical properties of these induced currents and voltages.

Solution Proposed: Apply Characteristic Mode Analysis (CMA) to identify the fundamental modes of the enclosure, current distribution, and the field pattern of each mode. This will allow us to predict the worst-case RF coupling scenarios without the need for lengthy simulations and/or expensive experimental measurements. The proposed approach can predict measurements at a fraction of the cost/time.

Relevance to OSPRES Grant Objective: Provide general guidelines on how the environment, in this case the enclosure, affects RF coupling and subsequent electromagnetic absorption to UAV wires and integrated circuits.

Risks, Payoffs, and Challenges: The modes depend mainly on the shape and material of the enclosure. Since UAVs have a wide variety of shapes and material compositions,

a library of several UAVs needs to be studied before quantitative general conclusions can be drawn. Challenges can be mitigated by the use of the classification techniques of Machine Learning (ML). That is, different ML techniques will be evoked to detect hidden patterns on how the shape, material composition, and the shape/size location of slots correlate with the field enhancement inside the enclosure.

6.1.2 Tasks and Milestones / Timeline / Status

Task	Timeline	Milestone	Status
A. Complete the CMA implementation for studying the shielding effectiveness of metallic enclosures. Validate CMA can predict the worst-case shielding effectiveness of metallic enclosures as a function of their shapes.	2 months 11/15/2020-1/15/2021	A fast full-wave tool that facilitates studying the effect of a metallic enclosure on shielding effectiveness (1 IEEE AWPL Paper)	Completed, Manuscript for IEEE AWPL paper is being finalized
B. Use CMA tool in (A) to predict the worst-case internal field magnitude of metallic and dielectric enclosures of ten COTS UAVs as a function of HPM waveform	4 months 1/15/2021-5/15/2021	A database of worst-case internal fields shielding effectiveness results of the ten COTS UAVs as a function of their shape and HPM waveforms.	Ongoing
C. Use the database in (B) to train a Machine Learning (ML) platform to predict RF coupling to enclosed wires and electronics	5 months 5/15/2021-10/15/2021	Perform blind tests to estimate the induced internal fields of 2 COTS UAVs, not used in the training of the ML platform, and compare them with the measurement.	Ongoing

6.1.3. Progress Made Since Last Report

Tasks B & C:

a. Continue the preparation of the database for different quadcopter UAVs to train a machine-learning algorithm to detect the worst-case coupling to the circuitry of the UAV.

b. The resonances of the PEC enclosures have an extremely high quality factor i.e. a narrow bandwidth. We suspected that our frequency step might have been too large leading to undetected resonances because they fell between 2 frequency points. Therefore, we revisited the PEC enclosure cases using 501 frequency points instead of 251 frequency points in the 0.5 GHz to 1 Ghz frequency range. We also increased the number of incident angles (from 91 angles to 1369 angles to cover the $0 < \theta < 180$ and $0 < \varphi < 180$ range. Fig. 6.1.1 shows a model of the enclosed circuitry which is composed of 4 loads, 4 wires, and a central PCB. The loss tangent, tanδ, of the PCB's dielectric substrate was varied as shown in the Table in Fig. 6.1.1 increasing from left to right.

6.1.3 Significant Finding(s) and Mission Impact

a. Due to the limitation of the frequency resolution of the previously reported results the load voltage at only one resonance of the Perfect Electric Conductor (PEC) enclosure was higher than the dielectric case. The updated Fig. 6.1.1 shows that there are multiple resonance frequencies where the PEC cavity will enhance the coupling. These will be the optimum frequencies to maximize the coupling to the enclosed circuitry.

b. The loss of the circuitry has a negligible effect on the coupling to loads inside dielectric frames as Fig. 6.1.1 indicates when the loss tangent is increased from 0.01 in Fig. 6.1.1a to 1 in Fig. 6.1.1c. On average, the coupled voltage to the circuitry inside a Plexiglass (PG) frame is higher than the load voltage of the same circuitry in free space by 3 dB on average regardless of the circuitry loss.

c. The computational time for studying a dielectric frame is 66.3 hours versus 36.5 hours for the circuitry in free space. However, for dielectric frames there is little sensitivity to the dimensions and the properties of the frame. That is, for dielectric enclosures, regardless of their exact shape and properties, we can assume that the coupled load voltage will increase by 3 dB in comparison to when the circuitry is placed in free-space. The resonance frequencies of the circuitry will also experience a redshift of ~ 10-20 %. To validate this estimate, we re-simulated the configuration in Fig. 6.1.1 but using a relative dielectric permittivity ε_r = 26 instead of ε_r = 2.6 which was used to generate the results in Figure 6.1.1. The relative dielectric permittivity of 26 was chosen as an extreme value to validate that the dielectric estimate is applicable for all possible dielectric enclosures. The orientation-averaged coupled voltage had a peak of -55.2 dB when the dielectric frame had an ε_r value of 26 versus a peak of -54.8 dB when the dielectric frame had an ε_r value of 2.6 validating the insensitivity. The approximations provided herein for the dielectric frames are acceptable considering the computational time saving and the small range of practical dielectric constants of the UAV frames. In future experiments, we will focus mostly on PEC and Carbon Fiber

frames. Moreover, we will study additional UAV configurations where the frame is more of a cover and not a cavity by removing, for example, the top wall in the model in Figure 6.1.1.

Current/Future Work:

We are currently creating a full-wave model of a complete UAV with all the wires and all the IC components to use as a numerical platform for studying effects and validating predictions. Figure 6.1.2a shows the UAV we are currently modeling and Fig. 6.1.2b shows its wiring diagram with the different IC components. We are building an accurate replica of the UAV in Fig. 6.1.2 using the full-wave electromagnetic solver CST MWS which is shown in Fig. 6.1.2c. The wires' length and diameters match the values in the actual UAV in Fig. 6.1.2a. Moreover, we will enforce practical considerations such as the attachments of the wires to the frame when studying different wire shapes in the CST model. Over the coming few weeks, the CST model should have all the components and the wires in Fig. 6.1.2a and then we can run exhaustive numerical experiments to study the response to different incident electromagnetic waveforms. More importantly, we will test the validity of the simple RF coupling guidelines and models we previously developed for predicting the RF coupling to the ***complete*** UAV in Fig. 6.1.2. The different electronics and components in Fig. 6.1.2c, i.e. the motors, the ESCs, and the PX4 board, will be replaced by equivalent circuits obtained via direct experimental measurements or from the components' datasheets. Upon completion, the currents and voltages in at the terminals of different components will be compared to the experimental measurements from the same UAV for validation.

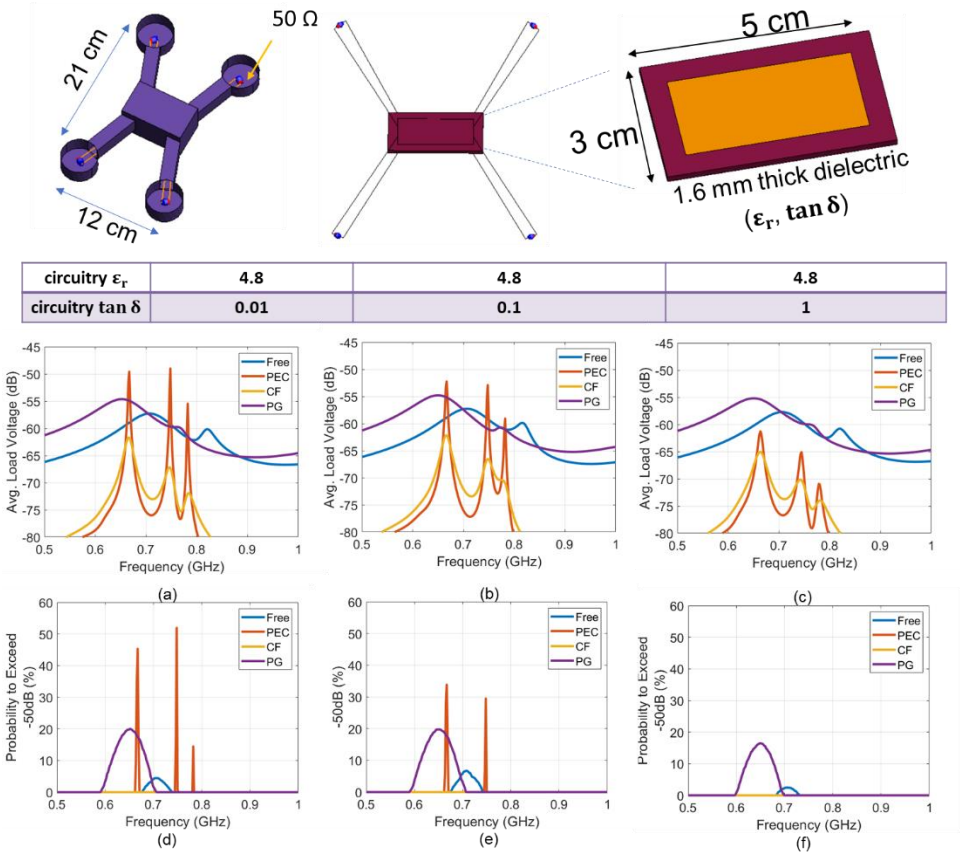


Fig. 6.1.1. Model of enclosed circuitry showing the wires, loads, and PCB. The table shows the dielectric properties used for the PCB substrate. (a), (b), (c): Average voltage across one load of the simple circuitry model inside a UAV enclosure (d), (e), and (f) The probability of the load voltage exceeding an arbitrary threshold of -50 dB.

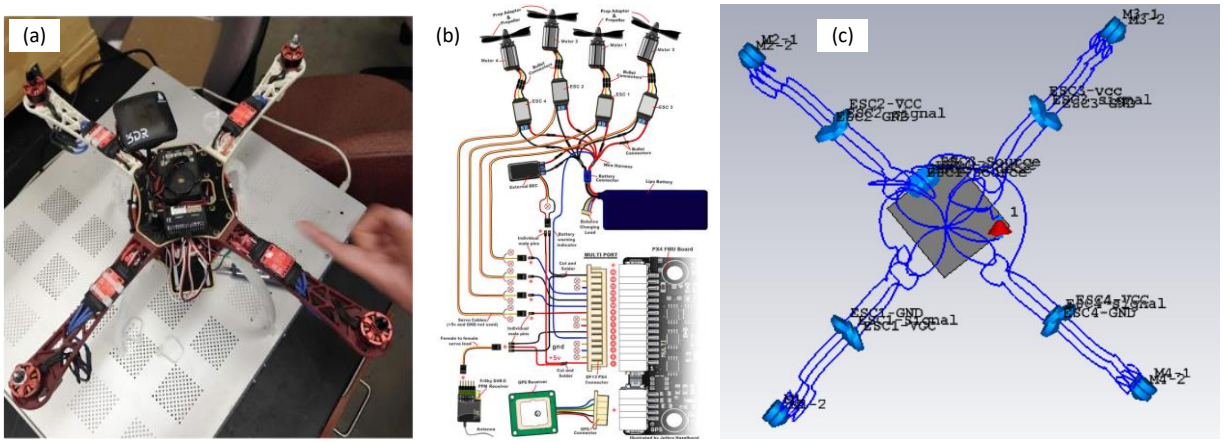


Fig. 6.1.2. (a) Model of the realistic UAV circuitry showing the wires, components, and frame, (b) the UAV wiring diagram showing all the wires and components, (c) the CST MWS model of the UAV in (a) and (b).

7.0 Thermal Management

7.1 Micro-Jet Thermal Management System

(Jordan Berg, Roy Allen, and Sarvenaz Sobhansarbandi)

7.1.1 Problem Statement, Approach, and Context

After wrapping up our assessment on the initial jet impingement thermal management system (TMS) technology and concluding that this is not a viable option moving forward, we are currently evaluating the possibility of future work on alternative TMSs for HPM systems in support of the Naval afloat mission. This sub-section is being included as a placeholder.

7.2 Nanofluid Heat Transfer Fluid Development

(Jordan Berg, Roy Allen, and Sarvenaz Sobhansarbandi)

7.2.1 Problem Statement, Approach, and Context

Primary Problem: Dielectric fluids (non-conductive coolant) used in thermal management systems, while suitable for high-voltage HPM-based technologies, possess inherent thermophysical fluid properties (low thermal conductivity, high viscosity) that inhibit their ability to achieve >1 GW/m^3 cooling densities.

Solution Space: Develop a nanofluid by entraining ceramic nanoparticles and dispersants within the dielectric base-fluid, pure silicon fluid (PSF), to increase the nanofluid's thermophysical properties and cooling density capabilities with a similar form-factor.

Sub-Problem: While the dynamic viscosity of the dielectric fluid used, PSF-20cSt, is 'low' relative to other silicone-based fluids, it is ~15 times more viscous than water, and therefore requires increased pumping power within the TMS. Compounding this issue is the necessity to increase the flowrate of the fluid to achieve an equivalent heat removal rate compared to that of a water-based coolant.

State-of-the-Art (SOTA): Nanofluids, with optimal ratios of fluid-to-nanoparticles, have been shown to increase the thermal conductivity of dielectric fluids by 87% in comparison to the generic dielectric fluid alone; resulting in either greater cooling density, decreased pumping power, or reduced mass flow rate requirements.

Deficiency in the SOTA: The addition of nanoparticles within a base-fluid results in a tradeoff between one or more thermophysical properties. For example, adding nanoparticles may increase thermal conductivity of the nanofluid but may result in increased viscosity; i.e., heat removal rate may increase, but the required pumping power along with it. To the best of our knowledge, no one has attempted to create a nanofluid mixture with a goal of keeping the viscosity low. Therefore, the optimal nanoparticle-to-fluid ratio and specific nanoparticle type for the HPM thermal management systems needs to be identified and optimized with an attempt to maintain the viscosity of the mixture as low as possible.

Solution Proposed: Develop a nanofluid with both desirable thermal properties and a relatively low viscosity that can serve as a viable heat transfer fluid (HTF) for TMSs in HPM topologies and other high power density applications. Utilize systematic numerical and experimental strategies to evaluate a large sample set of various nanoparticles (with surfactants and dispersants).

Relevance to OSPRES Grant Objective: Increase cooling densities for HPM systems without requiring TMS design permutations, while decreasing pumping power requirements, in-line with the SWaP-C^2 objective.

Risks, Payoffs, and Challenges:

Risk: The pressures incurred by using a silicone-based fluid in a high-flow regime are not insignificant; large pump-chiller systems may still be necessary.

Challenges: Creating low volume-fraction samples of nanoparticles and surfactants is near equipment precision limit. Maintaining accuracy is critical to properly study modified fluids.

Payoff: A modified nanofluid dielectric fluid can be used to increase cooling capacity of any high power density system. An optimized nanofluid has the potential to extract 20% up to several factors more than the base fluid.

7.2.2 Tasks and Milestones / Timeline / Status

(A) Measure thermophysical properties of currently utilized PSF-20cSt / DEC20–JAN21 / Completed.

(B) Establish theoretical model of nanofluid compositions / DEC20–JAN21 / Completed.

(C) Create and test modified PSF-20cSt with nanoparticles and surfactants / JAN–MAR21 / In progress.

(D) Select the nanofluid mixture with optimal thermal properties and re-evaluate the CFD modeling / MAR–APR21 / TBD.

7.2.3 Progress Made Since Last Report

(A) Nineteen total nanofluid samples have been prepared. Nanofluid samples were created by varying mass fractions (0.25–0.75 wt. %) of various ceramic nanoparticles (Fe_2O_3, SiC, and Al_2O_3) in the PSF-20-cSt HTF mixed with two surfactants, as well as a set of samples with no surfactants added. The purpose of surfactants in each of the mixtures is to help with the even dispersion of the nanoparticles in the HTF. Justification in testing samples with no surfactants comes from the realization that the surfactants chosen (based off of the literature) are much more viscous than the PSF. Though the volume fraction of the surfactant additives is on the order of 0.01 wt % of the sample, adding viscous fluids in the mixtures directly opposes the goal of creating a low-viscosity HTF. The addition of surfactants may be superfluous since the HTF with be in circulation. This circulation could agitate the mixture well enough so as to not need additional dispersants. Initial differential scanning calorimeter (DSC) testing has begun as well. The initial results are shown in Figure 7.2.1. Each sample was run

in a range of ~10–35 °C. As yet unknown issues with the 0.25 wt. % #1 sample ended data logging prematurely; this is currently being retested. It is too early to draw any conclusions about HTF thermal performance increases until all samples have their specific heat capacity (as well as thermal conductivity and dynamic viscosity) determined.

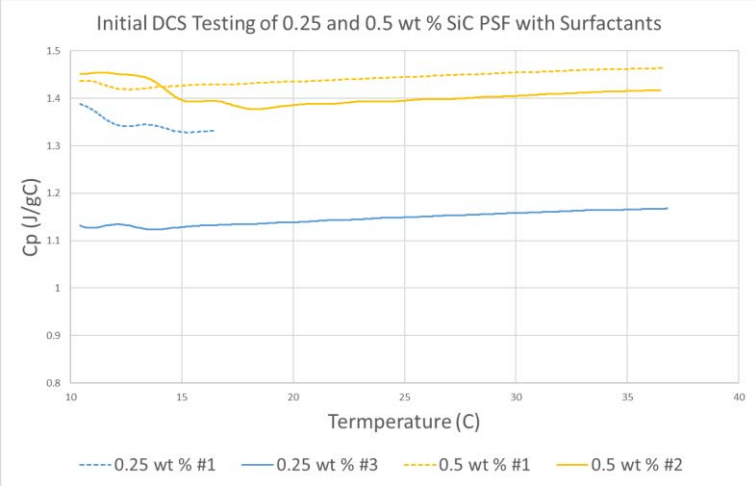


Figure 7.2.1. Preliminary DSC measurements of samples.

7.2.4 Significant Finding(s) and Mission Impact

Based on literature, the creation of a dielectric nanofluid for use as a coolant in the HPM system could potentially improve cooling performance. The thermal dissipation requirements for HPM systems are not insignificant and could, therefore, benefit from performance enhancement from every aspect (geometric optimization, reduction of thermal resistances, coolant selection, material selection, etc.).

(A) A sample of the PSF-20cSt that was used in the experimental testing of the JI-TMS was tested with a DSC. The specific heat of the fluid was found to significantly differ from that of the manufacturer's value. The vendor's reported value of the PSF-20cSt was 1.6 $\frac{J}{gC}$, while DSC measurements showed it to be closer to 1.1 $\frac{J}{gC}$. This difference hinders the accuracy of the CFD results of CFD models.

(B) Given the aforementioned error in specific heat capacity, along with the need for a high thermal performance coolant, nanoparticle-modified PSF-20cSt was determined to be a necessary and useful undertaking. Three different ceramic nanoparticles were chosen to be studied: alumina, silicon carbide, and iron(II,III) oxide. Ceramics were chosen to maintain HTF dielectric properties.

(C) Two sample sets have been prepared in various low mass-fraction quantities (0.25 wt%, 0.5 wt%, and 0.75 wt% of each). The different sets were created: one that includes surfactants and one that is purely NP's and PFS-20cSt. The surfactants are intended to aid in creating a homogeneous mixture. The total number of samples is 57, including the control. Testing and analysis is currently underway.

8.0 Program Management

8.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

8.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

8.3 Major Procurement Actions

i. Microsoft Office 365 GCC High (75 seats) - $45,000 (for OSPRES Contract CUI Compliance)

8.4 Travel

Destination	Purpose	Attendees	Estimated Costs

8.5 Pending or Upcoming Public Release Requests

i. J. N. Berg, R. C. Allen, and S. Sobhansarbandi, CFD Modeling and Experimental Implementation of a Novel Thermal Management System for a Semiconductor Device [Unpublished manuscript], Int J Heat Mass Transf, pp. 1-12, 2021.

9.0 Appendix B: Academic and IP Output

9.1 Students Graduated

Name	Degree	Currently
Al-Shaikhli, Waleed	MS	Kansas City National Security Campus, Honeywell
Bissen, Bear	MS	UMKC/MIDE (Staff)
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Hanif, Abu	PhD	
Harmon, Aaron	BS	Missouri University of Science & Technology
Harp, Joshua	MS	Small Business
Hauptman, Cash	BS	University of Nebraska-Lincoln
Labrada, Dario	BS	UMKC/MIDE (MS Student)
Lancaster, John	MS	Lawrence Livermore National Laboratory
Renzelman, Jeff	MS	Kansas City National Security Campus, Honeywell
Roy, Sourov	PhD	UMKC/MIDE (Postdoc)
Wagner, Adam	MS	Kansas City National Security Campus, Honeywell
Xia, Shengxuan	BS	Missouri University of Science & Technology

9.2 Conference Publications

[1] W. Azad, S. Roy, and F. Khan, "A Single Gate Driver-based Four-stage High-voltage SiC Switch Having Dynamic Voltage Balancing Capability," submitted in *2021 IEEE Applied Power Electronics Conference and Exposition* (APEC), Phoenix, AZ, USA, June 9-12, 2021.

[2] J. Hunter, S. Xia, A. Harmon, A. M. Hassan, V. Khilkevich, and D. Beetner, "Modeling and Statistical Characterization of Electromagnetic Coupling to Electronic Devices," *IEEE International Symposium on Antennas and Propagation and NSRM USNC-URSI National Radio Science Meeting*, Boulder, CO, January 4-9, 2021.

[3] W. Azad, S. Roy, and F. Khan, "A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver," accepted in *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, 2020.

[4] B. Barman, K. C. Durbhakula, B. Bissen, D. Chatterjee, and A. N. Caruso, "Performance Optimization of a Microstrip Patch Antenna using Characteristic Mode and D/Q Analysis," *2020 XXXIIIrd General Assembly and Scientific Symposium of the International Union of Radio Science*, Rome, Italy, Aug 29 - Sept 5, 2020, pp. 1-4 (online conference).

[5] B. Barman, D. Chatterjee, and A. N. Caruso, "Performance Optimization of Electrically Small Microstrip Patch Antennas on Finite Ground Planes," 2020 *IEEE International Symposium on Antennas and Propagation and North American Radio*

Science Meeting, Montreal, Quebec, Canada, July 5-10, 2020, pp. 1–2 (online conference).

[6] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, “Scalable Characteristic Mode Analysis: Requirements and Challenges (White Paper),” *Large Scale Networking (LSN) Workshop on Huge Data: A Computing, Networking and Distributed Systems Perspective Sponsored by NSF*, Chicago, IL, April 13-14, 2020.

[7] M. Hamdalla, A. N. Caruso, and A. M. Hassan, “Predicting Electromagnetic Interference to a Terminated Wire Using Characteristic Mode Analysis,” *Proceedings of the Annual Review of Progress in Applied Computational Electromagnetics (ACES)*, Monterey, CA, March 22-26, 2020.

[8] W. Azad, F. Khan, and A. Caruso, "Self-sustaining High-power RF Signal Generation Using LDMOS Based Power Amplifier and Nonlinear Transmission Line," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 3567-3572 [doi].

[9] A. Hanif, W. Azad, and F. Khan, "Detection of Bond Wire Lift Off in IGBT Power Modules Using Ultrasound Resonators," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 345-350 [doi].

[10] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, “Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS,” *Annual Directed Energy Science and Technology Symposium*, March 2020 (abstract appeared, but talk cancelled due to pandemic).

[11] B. Barman, D. Chatterjee, and A. N. Caruso, “Some Investigations into Mutual Coupling Analysis for Trade Space Studies of Linear Arrays,” *2019 IEEE International Symposium on Phased Array Systems and Technology (PAST)*, Waltham, MA, October 2019, pp. 1-8.

[12] B. Barman, D. Chatterjee, and A. N. Caruso, “Characteristic Mode Analysis of a straight and an L-probe fed Microstrip Patch,” *2019 IEEE Indian Conference on Antennas and Propogation (InCAP)*, Ahmedabad, India, Dec 2019, pp. 1-3.

[13] M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of the Effect of the UAV Frame Material on Coupling and Interference," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019.

[14] M. Hamdalla, J. Hunter, Y. Liu, V. Khilkevich, D. Beetner, A. Caruso, and A. M. Hassan, "Electromagnetic Interference of Unmanned Aerial Vehicles: A Characteristic Mode Analysis Approach," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019.

[15] B. Barman, D. Chatterjee, and A. N. Caruso, “Analytical Models for L-Probe fed Microstrip Antennas,” *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

[16] K. C. Durbhakula, J. Lancaster, J. Hunter, Y. Liu, D. Beetner, V. Khilkevich, D. Chatterjee, A. N. Caruso, and A. M. Hassan, "Electromagnetic Coupling Analysis of Printed Circuit Board Traces using Characteristic Mode Analysis," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (2 pages)*, Atlanta, Georgia, USA, July 7-12 2019.

[17] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "On the Location of Transverse Electric Surface Wave Poles for Electrically Thick Substrates," Proceedings of the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019.

[18] M. Hamdalla, B. Bissen, A. N. Caruso, and A. M. Hassan, "Experimental Validations of Characteristic Mode Analysis Predictions Using GTEM Measurements," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Montréal, *Québec, Canada, July 5-10, 2020*.

[19] W. Azad and F. Khan, "Sustaining High-power RF Signal Generation in a Positive Feedback Network," *2019 IEEE Pulsed Power and Plasma Science Conference (PPPS)*, Orlando, FL, USA, June 23-28 2019.

[20] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, "Scalable characteristic mode analysis using big data techniques," *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[21] M. Hamdalla, W. Al-Shaikhli, J. Lancaster, J. D. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of Electromagnetic Coupling to Wires with Realistic Shapes," *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[22] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "Location of Surface Wave Poles in Sommerfeld Integrals: A Mittag-Leffler Expansion Approach," *Proceedings of the URSI-B International Symposium on Electromagnetic Theory*, URSI Commission, San Diego, USA, May 2019.

[23] D. Chatterjee, B. Barman. J. Kovarik, and A. N. Caruso, "Studies on Antenna Characterization and Propagation of High Power Pulsed Electromagnetic Waves with Minimal Spatial Dispersion," presented at the *Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium*, Destin, Florida, USA, April 2019.

[24] J. Kovarik, B. Barman, D. Chatterjee and A. N. Caruso, "Some Investigations into Applications of Electrically Small Antennas as Phased Array Elements," presented at the *Directed Energy Professional Society* (DEPS) *Annual Science and Technology Symposium*, Destin, Florida, USA, April 2019.

[25] K. C. Durbhakula, D. Chatterjee and A. M. Hassan, "Analytical Evaluation of Sommerfeld Integral Tails Present in Two-layered Media Green's Functions," *Proceedings of the Indian Conference on Antennas and Propagation* (InCAP), Hyderabad, India, December 2018.

[26] D. Beetner, V. Khilkevich, A. M. Hassan, J. Hunter, Y. Liu, and D. Floyd, "Characterization of the Electromagnetic Coupling to UAVs," *DE Systems Symposium*, September 24-27, 2018

[27] C. Hartshorn, K. Durbhakula, D. Welty, D. Chatterjee, J. Lancaster, A. M. Hassan, and A. N. Caruso, “Crosstalk and Coupling to Printed Circuit Board Metallic Traces with Arbitrary Shapes,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[28] M. Hamdalla, J. Roacho-Valles, J. Hunter, D. Beetner, A. M. Hassan, and A. N. Caruso, “Electromagnetic Analysis of Unmanned Aerial Vehicles Using Characteristic Mode Analysis,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[29] C. Hartshorn, M. Hamdalla, J. Lancaster, A. M. Hassan, and A. N. Caruso, “Electromagnetic Vulnerability of Wires with Arbitrary Shape,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[30] K. C. Durbhakula, D. Chatterjee, A. M. Hassan, and M. S. Kluskens, “Studies on Numerical Evaluation of Sommerfeld Integrals for Multilayer Topologies,” *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018.

[31] J. Lancaster, D. Chatterjee, and A. N. Caruso, “Some Investigations into the Dispersion Characteristics of Localized Bessel Beams,” published in the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018 (1 page URSI Abstract).

[32] M. Hamdalla, A. M. Hassan, and A. N. Caruso “Characteristic Mode Analysis of Unmanned Aerial Vehicles with Realistic Shapes and Material Composition,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Boston, MA, July 8-13, 2018.

[33] W. Azad, S. Roy, A. S. Imtiaz, and F. Khan, "Microelectromechanical System (MEMS) Resonator: A New Element in Power Converter Circuits Featuring Reduced EMI," *2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, Niigata, May 20-24, 2018, pp. 2416-2420 [doi].

[34] J. Hunter, Y. Liu, D. Floyd, A. Hassan, V. Khilkevich, and D. Beetner, “Characterization of the Electromagnetic Coupling to UAVs,” Annual Directed Energy Science and Technology Symposium, Feb 26-March 2, 2018.

9.3 Journal Publications

9.3.1 In Preparation

[1] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, CFD Modeling and Experimental Implementation of a Novel Thermal Management System for a Semiconductor Device, *Int J. Heat Mass Transf*, pp. 1-12, In Preparation, **2021**.

[2] W. Azad, F. Khan, and A. N. Caruso, “A Series-connected High-voltage SiC Switch Driven by a Compact High-voltage Isolated Gate Driver,” In preparation, **2021.**

[3] M. Z. M. Hamdalla, B. Bissen, J. D. Hunter , L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, “Experimental Evaluation of CMA Predictions and Control of Electromagnetic Interference to UAVs,” In Preparation, **2021**.

[4] S. Xia, J. Hunter, A. Harmon, M. Hamdalla, A. Hassan, V. Khilkevich, D. Beetner, "Simulation Driven Statistical Analysis of the Electro-magnetic Coupling to Microstriplines," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[5] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, "Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field Coupling to Randomly Shaped Wires," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[6] W. Azad, F. Khan, and A. N. Caruso, "A Medium Power, Self-Sustaining, Configurable RF Pulse Generation Circuit Using a Nonlinear Transmission Line and Power Amplifier in a Closed Loop Configuration, In Preparation, **2020**.

9.2.2 Submitted / Under Revision

[7] Khulud Alsultan, Mohamed Hamdalla, Sumitra Dey, A. N. Caruso, Praveen Rao, and A. M. Hassan, "Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform," *IEEE Open Journal of Antennas and Propagation,* Submitted, **2020**.

[8] John Keerthi Paul Bhamidipati, Eliot R. Myers, Adam M. Conway, Lars F. Voss, and Anthony N. Caruso, "Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches," *IEEE Transactions on Electronic Devices*, Under Revision, **2020**.

[9] W. Azad, F. Khan, and A. Caruso, "A Medium Power, Self-sustaining, Configurable RF Pulse Generation Circuit Using Nonlinear Transmission Line and a Power Amplifier in Closed Loop Configuration," *IEEE Transaction on Plasma Science*, Submitted, **2020**.

[10] S. Roy, W. Azad, S. Baidya and F. Khan, "A Comprehensive Review on Rectifiers, Linear Regulators and Switched-mode Power Processing Techniques used for Powering Biomedical Sensors and Implants inside Human Body," *IEEE Transactions on Power Electronics*, Submitted, **2020**.

[11] S. Roy, W. Azad, S. Baidya, M. Alam and F. Khan, "Powering Solutions for Biomedical Sensors and Implants inside Human Body–A Comprehensive Review on Energy Harvesting Units, Energy Storage, and Power Transfer Circuits," *IEEE Transactions on Power Electronics*, Submitted, **2020**.

9.3.2 Published / In Press

[12] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems," *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364-373, **2019**.

9.4 External Presentations/Briefings

DEPS Posters and Presentations 2020

[1] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[2] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

GOMAC 2019

[3] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[4] Eliot Myers, Picosecond High Power Switching Technologies

[5] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

DEPS Posters and Presentations 2019

[6] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[7] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[8] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[9] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[10] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[11] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[12] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[13] Deb Chatterjee, Studies On Antenna Characterization And Propogation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

DEPS Posters and Presentations 2018

[14] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[15] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[16] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

DEPS Posters and Presentations 2017

[17] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

9.5 IP Disclosures Filed

Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, 19UMK005, 28SEPT2018

Doynov, “Pulse Differential High-power Microwave Generation”, 19UMK007, 02JAN2019.

Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal”, 19UMK008, 28DEC2018.

Doynov, Caruso, “High-efficiency High-power Microwave Generation using Multipass Non-linear Network Topologies”, 19UMK017, 29AUG2020.

Doynov, “Scalable Modular System for High-power Microwaves Generation”, 20UMK010, 19APR2020.

Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna”, 20UMK011, 19APR2020.

Shepard, “A Novel Optical Fiber Amplifier”, 20UMK012, 02JUN2020.

Shepard, “A Low Noise Optical Amplifier”, 21UMK007, 14SEPT2020.

9.6 Provisional Patents Filed

Doynov, Caruso, “High-efficiency High-power Microwave Generation using Multipass Non-linear Network Topologies”, filed 26NOV2019.

9.7 Non-Provisional Patents Filed

None to date

10.0 Appendix B: Si-, SiC- and GaN Modeling and Evaluation

(John Bhamidipati)

10.1 Executive Summary

High-power ultrafast switching fundamentals and switching technologies have been comprehensively studied in the context of optically and electrically stimulated switching technologies and pulse forming networks (PFNs), and factors inhibiting the transient response (rise-time, fall-time, etc.) and device lifetime have been identified for further study. Existing power electronics based figures of merit (FoM) proposed by Baliga, Johnson, Keyes, Kim, Shigekane, Wang, Huang, and Shenai over a period of 40 years have been comprehensively studied, and a need for new FoM based on photoconductive semiconductor switches (PCSSs) for pulsed power applications has been identified. A FoM has been derived for material-level evaluation of high-power linear-mode PCSSs in a capacitive circuit based on a power dissipation model for adiabatic and non-adiabatic heating cases, which has been submitted to the IEEE T-ED journal for publication (currently under revision).

Building upon the material-level evaluation of photoconductive solids, the effort has been extended to include device evaluation to compare the performance of Si-, SiC- and GaN-PCSSs. Si-PCSS carrier lifetime control techniques like Au-diffusion, Pt-diffusion, and electron-beam irradiation have been studied, and selective crystal damage with proton irradiation has been proposed as an alternative with two orders of magnitude lower leakage current due to selective localization and better lifetime control (faster recovery) due to larger trap cross-section. These results have been demonstrated through TCAD simulations, but not empirically verified. Non-isothermal simulations have been performed to study heat dissipation trends in Si-PCSS, but the results were inconclusive with 2D models. The heat dissipation trends need to be studied in 3D models to accurately quantify the heat dissipation and temperature rise rates in pulsed mode operation.

Lateral- and vertical- geometries of GaN- and 4H-SiC PCSS have been simulated and intrinsic carrier generation at optical wavelengths of 355-, 365-, 385- and 532-nm have been studied. A comprehensive study needs to be done to better understand the effects of device geometry, doping levels and distribution, crystal defect types, defect energy levels, and concentration/densities on transient photocarrier generation, mobility, scattering, and recombination, requiring enormous number of man-hours and computational time. However, keeping the program's immediate needs in mind, this effort is being deprioritized and suspended for the time being.

10.2 Objective

To evaluate semi-conducting/insulating solids and device technologies through performance-based, application-specific figure(s) of merit (FoM) for high power photoconductive ultrafast switches and circuit topologies for linear/lock-on/avalanche modes of operation based on switching frequency, power dissipation, and cooling needs. This effort also aims to explore possibilities of pushing the state-of-the-art limitations of each technology through novel fabrication techniques and recommend coherent SwaP-

C^2 compliant solution through a near-ideal combination of PCSS driver and pulse forming networks (PFNs) for a pulsed-power system to achieve high power conversion efficiency with minimal spatial and capital footprint.

This involves evaluation of semiconducting/semi-insulating solids in the context of photo-stimulated switching technologies to determine an optimal source driver material to achieve tens-of-kV switching at near-zero jitter, sub-nanosecond rise-time, sub-unity Ω impedance, and nanosecond-order recovery, yielding GHz order bandwidth with enhanced reliability. This involves a comprehensive study of the effects of device geometry, doping levels and distribution, crystal defect types, defect energy levels, and concentration/densities on transient photocarrier generation, mobility, scattering, and recombination.

10.3 Technical Background

High-power microwave (HPM) generation primarily pertains to the generation of high peak power bursts of narrowband electromagnetic radiation based on pulsed power, spanning the frequency range of approximately 1 to 100 GHz.[1] The ideal driver waveform would be an impulse generator—in other words, a high voltage spike with picosecond-order rise-time, operated at high repetition rate.[1] For decades, conventional pulsed power systems have primarily implemented vacuum-tube based klystrons, magnetrons, ignitrons, and spark gaps as sources by converting electron beam kinetic energy into electromagnetic radiation for HPM generation.[2] Despite the successful implementation in HPM systems, source drivers were limited by size, complexity, ~μs jitter, tunability, and failure rates, fostering research for alternative solutions in solid-state electronics using photoconductive switches.[3]

Nevertheless, the efforts have been constricted to relatively narrow bandgap (NBG) semiconductors Si and GaAs with <150°C safe operational temperatures, implemented in a pulse forming network. Continuously evolving application trade-space in the realm of pulsed power applications, advancement in the material science research, and commercialization of semi-conducting/insulating materials have given scope to novel materials like GaN, SiC, BN, AlN, Ga_2O_3, and diamond, capable of photo- and electro-conductivity to implement high power opening and closing switches.[4] Their unique properties including, but not limited to, thermal conductivity, electron saturation velocity and electric field breakdown translate into higher operating voltages on the order of tens-of-kV, operating temperatures (>150ºC), and pulse repetition frequencies (PRF) of hundreds-of-kHz making them superior to Si in high power ultrafast switching.[4] A near-ideal ultra-wide-band (UWB) HPM source driver is expected to have ~mΩ-cm and ~MΩ-cm on- and off-state resistivity, respectively, with minimal stray capacitance and inductance (from switch-leads, geometry, and p-n junction), high PRF (~500 kHz) and picosecond-order rise- and fall-time. [6]

Each of these expectations is influenced by a combination of material, device, and circuit parameters, including, but not limited, to geometry, conductivity (electro/photo), field, carrier generation, mobility, scattering, and recombination, parasitics, surface termination, thermal radiation coefficient, conductivity, carrier lifetime, and surface area.

Historically, the solid-state HPM sources have been demonstrated using Si, GaAs and SiC,[5] but SiC has not been extensively studied in comparison with other solids.

To effectively navigate this high-degree-of-freedom optimization, a figure of merit (FoM) can be used to screen and compare material capabilities quantitatively before attempting expensive empirical development campaigns. Johnson,[7] Keyes,[8] and Baliga[9] originally proposed figures of merit that enabled gross comparison of semiconductor materials for power electronics applications. Kim,[10] Wang,[11] Huang,[12] Shigekane,[13] and Shenai[14] have extended the effort to accommodate increased peak power density, average power density, operational frequency, heat removal, and the device-level implications of back-end processes, respectively.[14] While these FoM have been broadly successful, they are built for gate-based junction transistors and fall short in evaluating optically-stimulated photoconductive semiconductor switch (PCSS) technology where carrier generation and operational cutoff frequencies are limited by inherent material characteristics, device geometries, and incident spatiotemporal optical pulse intensity, raising a need for a PCSS-based FoM.

The results from this project contribute to implementing solid-state source drivers for HPM generation and many other pulsed-power applications. This is achieved by quantitatively screening and comparing the source-driver material and device technology capabilities in conjunction with pulse forming networks for a given application requirement before attempting expensive empirical implementation. Furthermore, this research explores novel fabrication techniques for parameter tailoring and post processing techniques that potentially contribute to push the theoretical performance limitations of the photoconductive devices. With the anticipated result of this effort, the multifaceted application-specific SWaP-C^2 compliant HPM source driver development can be completed with device design using the optimal semi-conducting/insulating solid and switching technology.

10.4 Tasks, Milestones, and Status

10.4.1 High Power Ultrafast Switch Fundamentals

i. Explore switching technologies capable of high-power ultrafast switching in optical- and electrical-actuation domains and study the micro and macro properties of semiconductors inhibiting switches' transient response and performance. *[DEC 2018 / completed]*

ii. Survey novel switching technologies (diodes, transistors and 2DEG-based switches) for down-selection in fast-rise pulsed power applications, study semiconductor(s) capable of implementation and refine performance metrics with quantitative reasoning *[FEB-MAR 2019 / completed]*

iii. Review existing power electronics figure(s) of merit (FoM)[7-14] to verify their suitability for evaluating optically triggered switches (PCSSs). *[APR 2019 / completed]*

10.4.2 Figure of Merit

iv. Recognize deficiencies in the existing FoM and derive a new FoM to address the deficit areas in light of the fundamental physics essential for high power linear-mode PCSS operation. *[JUN 2019 / completed]*

v. Explore tunable pulse forming networks (PFNs) with high efficiency suitable for high power ultrafast switching *[JUN 2019 / partially completed, expected to be done along with device-level evaluation]*

vi. Refine linear-mode PCSS FoM for on- and switching-states using power dissipation model (PDM) *[AUG 2019 / completed]*

vii. Quantitatively analyze the derived power loss equations for switching stages of the devices for Si, SiC, GaN, and diamond with varied geometry and illumination conditions as next step to defining figure of merit for PCSS without PFN *[OCT 2019 / completed]*

viii. Numerical analysis for turn-on and turn-off power loss equations to quantify the switching losses and combine with thermal conductivity for material FoM *[JAN-FEB 2020 / completed]*

ix. Refine numerical analysis for a generalized operational scenario across the photoconductive solids for on- and switching-states for adiabatic and non-adiabatic heating *[MAR 2020 / completed / Linear-PCSS FoM derived]*

x. Complete cost-effectiveness analysis to determine optimal material for PCSS implementation in a given application using material FoM in comparison with SWaP-C^2 requirements and complete drafting the manuscript 'Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches' *[APR-MAY 2020 / completed / manuscript submitted for journal publication]*

10.4.3 Device-Level Evaluation (Si-, SiC-, and GaN-PCSS)

xi. Evaluate Si-PCSS performance as a function of temperature by studying temperature dependence of band parameters and carrier dynamics (generation, transport, velocity saturation and recombination) through TCAD simulations. *[APR 2020 / completed]*

xii. Study photo-illuminated recovery of a 2-D, 1000×500-μm Si-PCSS device with a p-i-n doping profile (p^+,n^-,n^+) = (10^{19},10^{12},10^{19}) and a 500-μm optical window to map recovery time as a function of defect/trap type, density, level and cross sectional area. *[APR-MAY 2020 / completed]*

xiii. Study and compare the effects of defect-inducing fabrication processes/techniques such as gold (Au) diffusion and platinum (Pt) diffusion and compare with electron-beam irradiation on Si-PCSS recovery (carrier lifetime control). *[MAY-JUN 2020 / completed]*

xiv. Study the effects of proton-irradiation and γ-irradiation on carrier lifetime control and compare the study with electron-beam irradiation. *[JUL-AUG 2020 / completed]*

xv. Simulate different defect localization profiles, and complete numerical calculations for proton-irradiation dosage (fluence rates) and beam acceleration voltages (for penetration depth) using SRIM and TRIM models to experimentally verify the simulation results obtained in (xiv) *[SEP-OCT 2020]*

xvi. Experimentally validate the obtained simulation results for proton-irradiation induced defect profiles *[OCT 2020 / on hold – could not find a reasonable accelerator for proton-irradiation]*

xvii. Simulate and study 4H-SiC PCSS optical absorption profile and carrier generation at 265-, 355-, 385- and 532-nm incident wavelengths for optical energies between 250-μJ and 2.5-mJ at varied voltage bias (3–10kV) *[JAN 2021 / incomplete].*

xviii. Perform Si-PCSS non-isothermal simulations to quantify heat dissipation and temperature rise per pulse due to joule heating, generation-recombination, and Peltier-Thomson effect. *[SEP 2020 / results inconclusive]*

xix. Study optical and electrical performance of P-N doped and undoped semi-insulating vanadium compensated SiC-PCSS including optical absorption profile characterization, geometric (vertical and lateral) and doping profile optimization, and their effects on carrier dynamics. *[OCT-NOV 2020 / partially complete]*

xx. Simulate 3D Si-PCSS models at varied defect density and localization and optical energy to quantify their effects on power throughput, output pulse width, heat dissipation and temperature rise. *[DEC-2020 / incomplete]*

xxi. Complete parametric study of SiC-PCSS including rise- and recovery-time optimization simulations for varied vanadium and nitrogen concentrations, and high voltage transient response study for varied geometry, optical trigger, contact design, and illumination area *[Jan-Feb 2021 / incomplete]*

xxii. Model carbon- and iron-compensated GaN-PCSS with vertical and lateral geometries to simulate transient response, including rise- and fall-time, voltage hold-off, and peak- and average powers for performance evaluation against Si- and SiC-PCSS models. *[MAR 2021 / suspended]*

xxiii. Model carbon-compensated GaN-PCSS with vertical and lateral geometries, varied contact layers, carrier dynamics (generation, transport, and recombination) and circuit topologies to verify operational mode and current gain; then, calculate reduction in optical requirements in contrast with linear mode. *[MAR-APR 2021 / partially complete, on hold]*

xxiv. Evaluate the doping profiles, contact layering, and patterning for SiC-PCSS and explore suitable fabrication techniques to achieve desired optimal doping profile using TCAD-Athena. *[FEB-MAR 2021 / suspended]*

xxv. Evaluate the doping profiles, contact layering, and patterning for SiC-PCSS and explore suitable fabrication techniques to achieve desired optimal doping profile using TCAD-Athena. *[APR 2021 / suspended]*

xxvi. Complete parametric study of SiC-PCSS including rise and recovery time optimization simulations for varied vanadium and nitrogen concentrations, and high voltage transient response study for varied geometry, optical trigger, contact design, and illumination area. *[MAR-APR 2021 / suspended]*

10.5 Methods and Approach

Evaluation efforts started as a survey/exploration of optically (e.g. PCSSs) and non-optically stimulated (e.g. MOSFETs, IMPATT diodes, HEMTs, etc.) high power ultrafast switching technologies that may enable breakthroughs in solid-state source-enabled microwave generation. The first priority of this effort was exploring the factors (micro and

macro) that inhibit the transient response and limit the performance of both PCSS and non-optically stimulated devices. Micro- and macro- switch properties that influence performance irrespective of the stimulation mechanism and some properties exclusive to PCSS have been identified and switching technologies suitable for the application (HPM generation) criteria have been down-selected. During this process, we came across multiple figure(s) of merit proposed by researchers [7-14] over time that have classified semi-conducting/insulating solids through the lens of electrically actuated switching technologies such as JFETs and MOSFETs, but not PCSSs. After a comprehensive review of figures of merit, a need for evaluation of the semi-conducting/insulating materials in the context of optical pulse stimulation was recognized.

This involved a two-stage evaluation: (i) standalone material-level evaluation by deriving a FoM for linear-mode PCSS operation, followed by (ii) device-level evaluation based on the results from (i) along with pulse forming networks.

Taking fundamental PCSS operational parameters into account, material-level evaluation across photoconductive solids has been implemented using a power dissipation model for on- and switching-states. From the material-level evaluation results, Si, 4H-SiC and 3C-GaN are considered as viable candidates for PCSS device-level evaluation based on their performance and manufacturing maturity.

Long carrier lifetimes have been identified as a limiting factor in Si-PCSS, resulting in increased heat dissipation and limited pulse repetition rates (PRR). Historically, fabricated Si devices are processed through Au-diffusion, Pt-diffusion, and electron-beam irradiation to generate sub-band traps for lifetime control, but with high leakage current across all of the techniques. Localized proton-irradiation defect profiles have been simulated and studied to demonstrate better carrier lifetime control at reduced leakage current. However, experimental verification has not been performed due to unavailability of a beam accelerator with required beam energy.

Initial studies on fundamental photoconductivity parameters like absorption, photoresponsivity, and doping profiles of SiC- and GaN-PCSSs have been studied for vertical and lateral geometries. However, in the interest of the program's more pressing needs, this project is being deprioritized and suspended for the time being. As time permits, this subproject may be revisited in the future.

10.6 Results and Discussion

10.6.1 Material-Level Evaluation

Based on the macro and micro properties influencing semiconductor switch performance, the material-level evaluation for photoconductive solids has been performed by deriving a new linear PCSS figure of merit (FoM). The macro and micro properties taken into account are listed in Table 10.1 (A & B) below.

Table 10.1. (A). *Macro and micro properties influencing semiconductor switch performance,* ***(B)*** *Macro and micro properties affecting PCSSs specifically.*

General Semiconductor Properties	
Macro Properties	**Micro Properties**
Rise-time	Carrier generation
Hold-off voltage	Carrier recombination
Heating	Traps/crystal defects
Recovery	Scattering
Conductance	Dopants
Impedance	Carrier transport
Dark current	Drift and diffusion
Contacts	Injection inefficiency
Geometry	

PCSS Specific Properties	
Macro properties	**Micro Properties**
Incident energy	Absorption
Wavelength	Phonon assist vs. direct transition
Contact geometry	Sub bandgap states
AR coatings	

A FoM based on material power handling and capacity to resist temperature rise, based on fundamental parameter tuning has been derived through a power dissipation model (PDM). A PDM evaluates switching (turn-on and turn-off) and on-states to calculate power-dissipation rates across the photoconductive materials; the rates are then employed to calculate trends of temperature rise for adiabatic and non-adiabatic heating in the materials. It should be noted that PCSS conductance is contingent on photon absorption and breaks the tradeoff between V_{BD} and R_{ON} in electrically triggered devices. Figure 10.1 shows a spider chart that represents the numerical material parameters used in this analysis.

Figure 10.2 highlights the tradeoff between carrier lifetime and required optical power at 1Ω on-state resistance across photoconductive solids using Equation 1 below, for an assumed 100% photoabsorption efficiency and the material thickness optimal for a 10 kV device. The wavelength is chosen with respect to the solid's bandgap. For any given carrier lifetime, silicon is found to require the greatest optical power of all the considered solids, followed by GaAs. BN requires the least, as presented.

$$P = \frac{L^2 h\vartheta}{q\tau\mu_{\mathrm{T}} R_{\mathrm{on}}} \qquad \textit{(Eq. 1)}$$

Where P is required optical power, $h\vartheta$ is incident photon energy, L is device thickness $\left(L = \frac{10^4}{E_C}\right)$, E_C is the solid's critical field, μ_T is the mobility of holes and electrons, τ is the carrier lifetime, and R_{on} is on-state resistance.

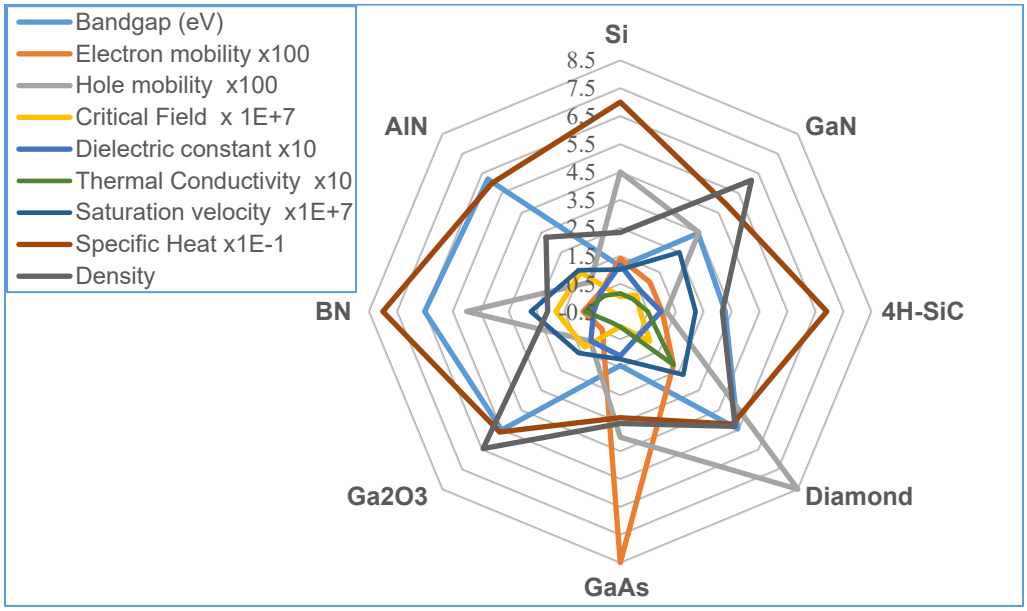


Figure 10.1. *Spider chart showing electrical and thermal properties used to calculate power dissipation and high-power figure of merit.*

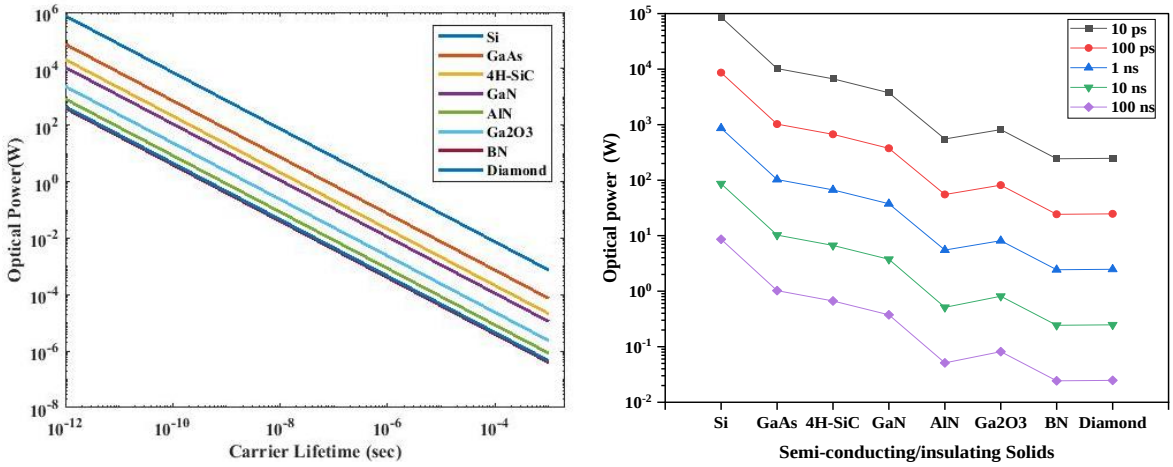


Figure 10.2. (Left) *Tradeoff between carrier lifetime and required optical power across photoconductive materials and* ***(Right)*** *optical power requirement trends across photoconductive solids at different carrier lifetimes.*

10.6.1.1 On-State Linear PCSS FoM

The on-state linear PCSS FoM facilitates the material evaluation of PCSS in systems driven at ~kHz PRR and tens-to-hundreds of μs pulse-width with negligible switching losses. Based on Equation 2 and the material parameters reported in Table 10.1, Figure 10.3 returns 4H-SiC as the highest rated WBG material (200 times superior to silicon),

and diamond as the highest for an UWBG material (24,000 times superior to silicon) operated in linear mode.

$$\textit{On-state FOM} = \frac{E_C^2\, E_g \eta \mu t_r k_{th}}{h\nu} \qquad \textit{(Eq 2)}$$

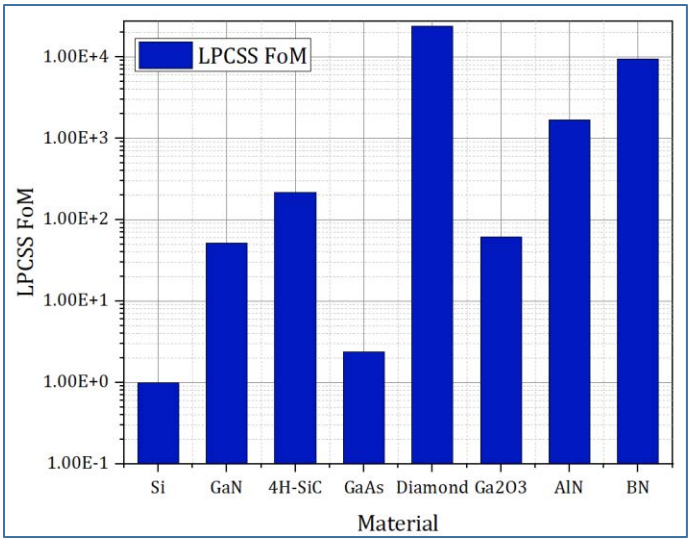


Figure 10.3. *Comparison of the on-state L-PCSS FoM across photoconductive materials, normalized to silicon in the limit of kHz PRR, hundreds of μs pulse width and low loss assumed.*

10.6.1.2 Switching FoM

Power dissipation equations during turn-on and turn-off (shown in Equations 3 and 4 below) have been derived using a PDM across photoconductive solids based on Nunnally's photoconductivity equations [15]

$$P_{turn\text{-}on} = \frac{\mu_T E_c^2 l^3}{R_L \mu_T I_0} \int_{t_0}^{t_1} \frac{\left(1 - e^{\frac{-t}{T_{net}}}\right)}{e^{-2.77*\frac{t}{\tau_p}\left[2 + R_L q\, \mu_T \frac{I_0}{E_\lambda L} T_{net}\right] - 2R_L\, q \mu_T \frac{I_0}{E_\lambda L} T_{net}\left[e^{-5.54\left(\frac{t}{\tau_p}\right)^2 - \frac{t}{\tau_p}}\right]}} dt \qquad \textit{(Eq 3.)}$$

$$\textit{and } P_{turn\text{-}off} = I_0 T_{net} q\, \mu_T E_c^2 L^3 \int_{t_2}^{t_3} \frac{e^{-2.77\left(\frac{t}{\tau_p}\right)^2 - \frac{-t}{T_{net}}}}{\left\{E_\lambda^3 + 2R_L q\, \mu_T I_0 T_{net}\; e^{\left[-2.77\left(\frac{t}{\tau_p}\right)^2 - \frac{-t}{T_{net(on)}}\right]}\right\}} dt \qquad \textit{(Eq 4.)}$$

where the limits t_0 and t_1 signify turn-on transition time limits, while t_2 and t_3 pertain to the turn-off transition. $I = I_0 e^{-4ln2\left(\frac{t}{\tau_p}\right)^2}$ is the temporal Gaussian light pulse with peak optical intensity I_0, $n(t)$ is the carrier generation function, E_c is the operational electric field, L is

the thickness of the device (carrier path length/switch gap), d, w are the length and width of the solid, hv is the incident photon energy, R_{on} is on-state resistance, R_L is load resistance, q is the charge of the electron , μ_T is the mobility of holes and electrons, t_r is the inherent device-recombination time, t_T is the transit time of carriers given by $t_T = \frac{L}{\mu_T E_c}$, $T_{net} = \frac{t_r * t_T}{(t_r + t_T)}$, $T_{net}(on) = t_T$, and τ_p is the FWHM of the optical pulse.

Calculations were done assuming a monochromatic temporal-Gaussian pulse chosen with bandgap-dependent wavelength for each photoconductive solid to facilitate 100% quantum efficiency. FWHM τ_p = 2 ns and pulse intensity capable of generating 10^{17} photoelectron and photo-hole pairs per pulse have been considered with an assumed 100% absorption and 100% contact injection efficiency to alter device resistance from GΩ to mΩ order at 30kV/mm electric field, adequate to trigger saturation velocity in charge carriers across all materials with a 50 Ω load resistance. Figure 10.4 (left) shows the temperature rise-rate across the photoconductive solids for adiabatic and non-adiabatic operation and Figure 10.4 (right) shows the respective figure of merit numbers for the same.

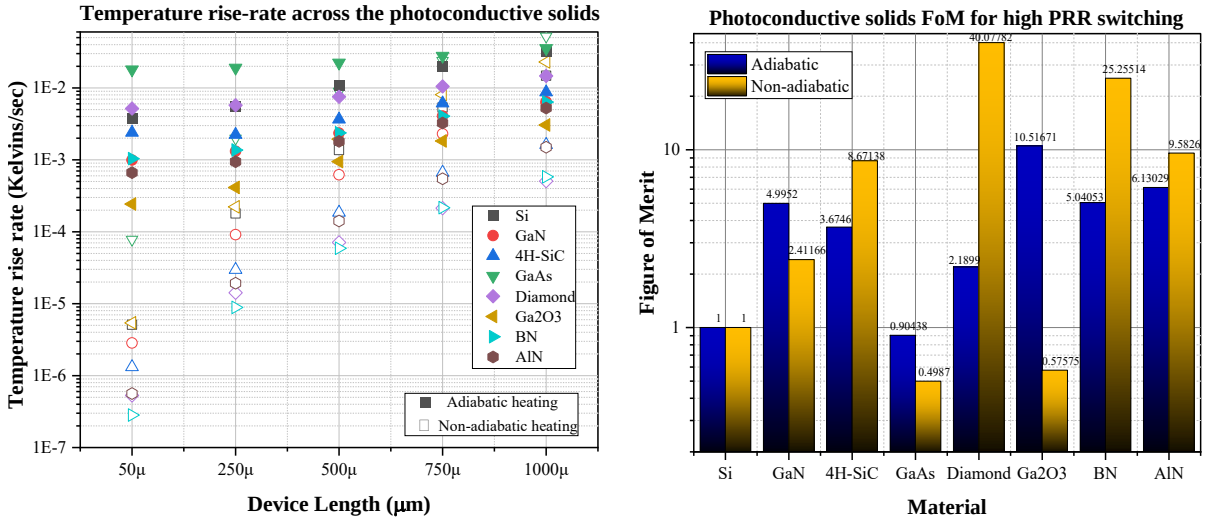


Figure 10.4. (Left) *Temperature-rise rate (Kelvin/sec) across materials at 50 kHz PRF and 30kV/mm electric field at 50 µm, 250 µm, 500 µm, 750 µm, and 1000 µm carrier path lengths for adiabatic and non-adiabatic heating; and (**Right)** Switching-mode linear PCSS FoM normalized to Si for adiabatic (blue) and non-adiabatic (yellow) heating across NBG, WBG, and UWBG photoconductive materials switched at 50 kHz PRR.*

UWBG-material Ga_2O_3 is found to perform five times better than diamond for adiabatic heating, owing to its specific heat constant; under non-adiabatic heating, however, diamond's thermal conductivity recompenses for incurred losses (~80 times Ga_2O_3), resulting in a ~10^{-6} temperature rise rate for high-PRR operation. However, based on the device fabrication maturity, Si-, SiC-, and GaN- device technologies have been selected for device-level evaluation.

10.6.2 PCSS Device-Level Study (Si-, SiC-, and GaN-PCSS Evaluation)

10.6.2.1 Si-PCSS

Au-diffusion, Pt-diffusion, e-beam irradiation,[17] and proton irradiation[18] effects on the carrier lifetime of silicon have been studied. While Au- and Pt-diffusion have drawbacks in the fabrication process, electron irradiation is a widely followed post-processing technique that creates uniform defects across the crystal. However, it results in increased leakage current (dark current) across the device due to distributed defects across the device, contributing to heat dissipation and affecting device lifetime. Simulations have shown faster recovery with localized defect profiles caused by proton-irradiation and at 3 orders of magnitude lower leakage currents as shown in Figure 10.5. Figure 10.6 shows a simulated proton irradiation defect profile and photo illuminated recovery comparison between electron irradiation and proton irradiation at different dominant trap levels. The defect penetration depth and distribution parameters have been calculated using SRIM (Stopping and Range of Ions in Matter) and TRIM (Transport of Ions in Matter) models.[19] *Note:* dominant trap-levels depend upon the anneal and operational temperatures.

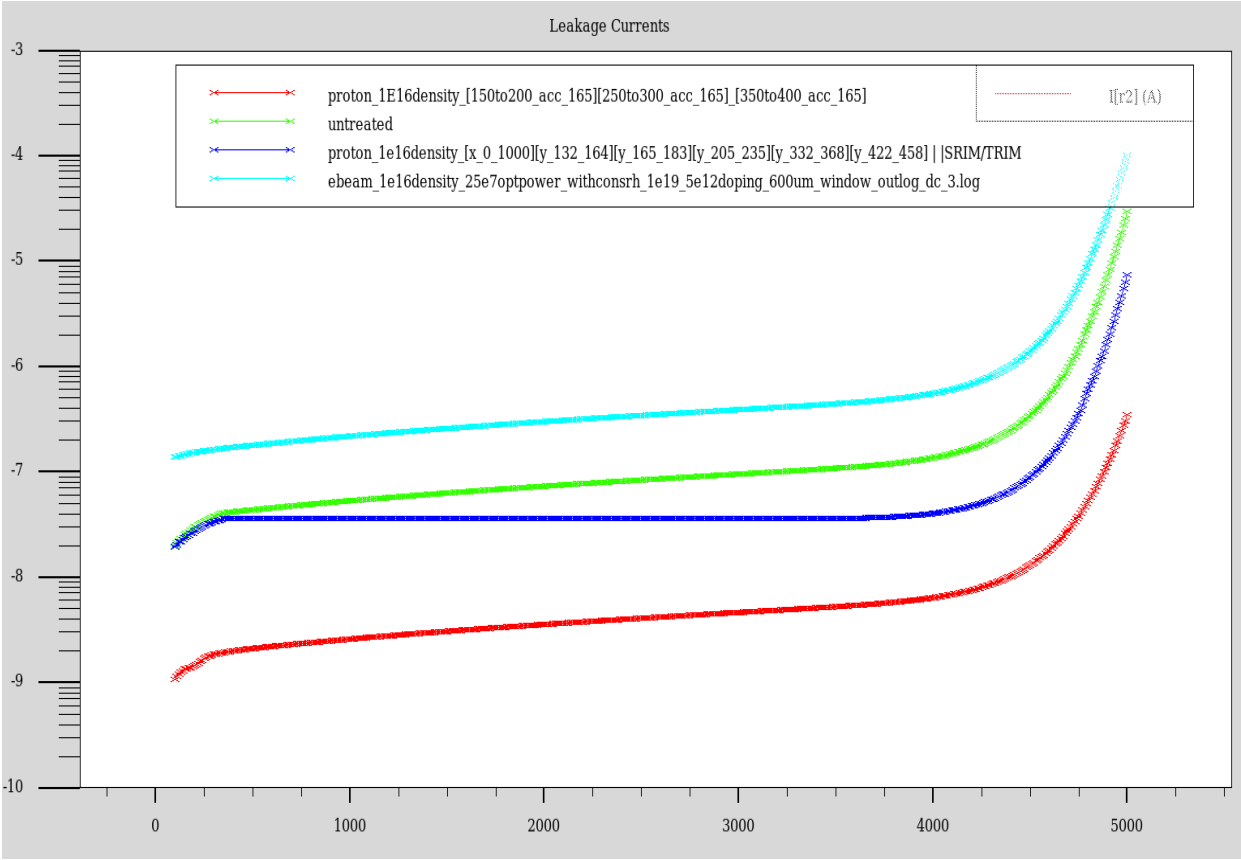


Figure 1.5. *Leakage current trends across Si-PCSS with defect densities of 1E16 cm^{-3} when treated with proton irradiation: profile I (red), unirradiated (green), proton irradiation; profile II (navy) and electron irradiation (aqua)*

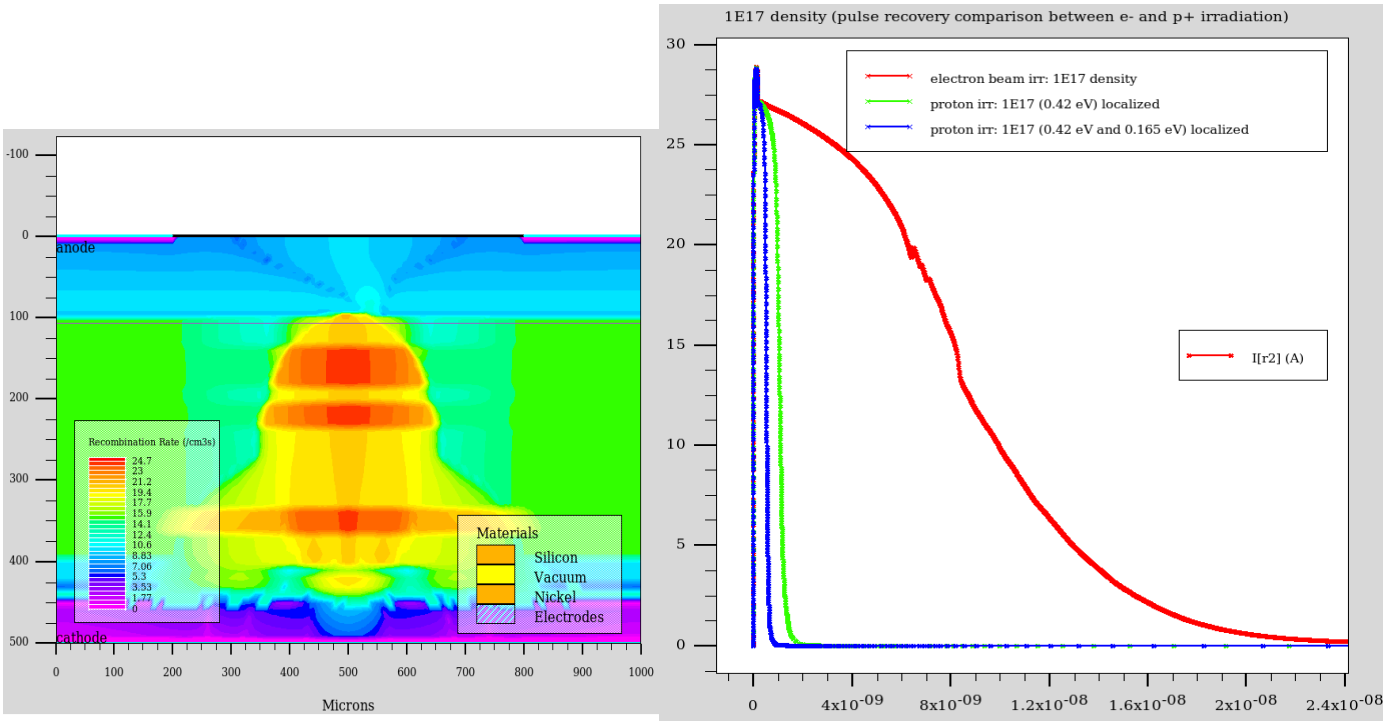


Figure 10.6. (Left) *Simulation result showing localized defect densities (in red) induced in Si-PCSS through proton irradiation;* ***(Right)*** *Photo-illuminated recovery comparison between electron irradiation (red) with dominant trap-level E_t = Ec–0.41 eV and proton irradiation with different dominant trap-levels E_c–0.42 and Ec–0.165 and E_c–0.42 eV (two dominant levels) at 1E17 cm^{-3} defect density.*

10.6.2.2 SiC- and GaN-PCSS

Detailed study of intrinsic and extrinsic SiC- and GaN-PCSS optical properties in lateral and vertical geometries, along with PFN-based analysis and non-isothermal power dissipation analysis of Si-PCSS simulations have not been completed. Unfortunately, a detailed study is time-consuming and computationally expensive. The time-consuming nature of this simulation study alongside more immediate needs of the program have led to deprioritizing and suspending this project for the time being.

10.7 Summary and Recommendations

High-power ultrafast switching fundamentals and technologies have been comprehensively studied in the context of HPM source drivers. A new figure of merit based on PCSSs has been derived and results have been submitted for a journal publication. This figure of merit can be extended in the future to include PFN- and device-based evaluation.

Via TCAD simulations, Si-PCSS recovery optimization has been studied and a potential solution has been proposed with better carrier lifetime control (1–2 ns vs. 16 ns recovery, from Figure 10.6) at two orders of magnitude lower leakage current compared with Au-diffusion, Pt-diffusion, and electron beam irradiation. However, an experimental validation of proton-irradiation-induced carrier lifetime control is recommended as it would prove to be a huge asset in enhancing the average power throughput while reducing the cooling requirements of PCSSs. A heat dissipation study via 3D device modeling needs to be conducted to estimate the cooling requirements for different operational conditions.

A comprehensive study of SiC- and GaN-PCSS photoconductive parameters in conjunction with pulse forming networks has to be completed. A study of C- and Fe-compensation effects on GaN-PCSS photoresponsivity is recommended to understand mid-gap optical excitation and for bistable operation.

10.8 Outputs

10.8.1 Journal Articles

John Keerthi Paul Bhamidipati, Eliot R. Myers, Adam M. Conway, Lars F. Voss, and Anthony N. Caruso, “Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches,” *IEEE Transactions on Electronic Devices*, Under Revision, **2020**.

10.8.2 IP disclosures

Bhamidipati, “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources”, 21UMK009, 04NOV2020

10.9 References

[1] G. Caryotakis, 1998. “The Klystron: A Microwave Source of Surprising Range and Endurance.” *Physics of Plasmas* 5 (5): 1590–98. doi: 10.1063/1.872826

[2] A. S. Gilmour, (2011). “Klystrons, Traveling Wave Tubes, Magnetrons, Cross-Field Amplifiers, and Gyrotrons”. Artech House. pp. 3–4. ISBN: 978-1608071845.

[3] E. Schamiloglu, *et al.* 2004. “High Power Microwave Sources and Applications.” *IEEE MTTS International Microwave Symposium Digest* 2: 1001–4.doi: 10.1109/mwsym.2004.1339150.

[4] J. Y. Tsao, S. Chowdhury, M. A. Hollis, D. Jena, N. M. Johnson, K. A. Jones, R. J. Kaplar, et al. 2018. “Ultrawide-Bandgap Semiconductors: Research Opportunities and Challenges.” *Advanced Electronic Materials* 4 (1): 1–49. doi: 10.1002/aelm.201600501.

[5] M.D. Pocha, W. W. Hofer. 1990. “Photoconductive Switching for HPM Generation.”

[6] J. Burger, J. S. J. Schoenberg, J. Scott Tyo, J. P. Hull, M. D. Abdalla, et al. 1997. “Photoconductive Semiconductor Switches Used for Ultrawideband, High-Power Microwave Generation.” *SPIE* 3158. doi: 10.1117/12.279424

[7] E. O. Johnson, "Physical limitations on frequency and power parameters of transistors," RCA Review, vol. 26, 163–177, (1965)

[8] R. W. Keyes, "Figure of Merit for Semiconductors for High Speed Switches," *Proc. IEEE*, vol. 60, 225–232, (1972)

[9] B. J. Baliga, “Power Semiconductor Device Figure of Merit for High-Frequency Applications.” *IEEE Electron Device Letters* 10 (10): 455–57. (1989). 10.1109/55.43098.

[10] H. Kim *et al.*, **“**Relationship between thermoelectric figure of merit and energy conversion efficiency**”,** *Proceedings of the National Academy of Sciences*, (2015), 112 (27) 82058210; 10.1073/pnas.1510231112

[11] H. Wang, F. Wang, and J. Zhang, "Power Semiconductor Device Figure of Merit for High-Power-Density Converter Design Applications," *IEEE Transactions on Electron Devices*, vol. 55, no. 1, 466-470, (2008)

[12] A. Q. Huang, "New unipolar switching power device figures of merit," *IEEE Electron Device Letters*, vol. 25, no. 5, pp. 298–301, (2004). 10.1109/LED.2004.826533.

[13] H. Shigekane, H. Kirihata, and Y. Uchida, "Developments in modern high-power semiconductor devices," *Power Semiconductor Devices and ICs*, 1993. ISPSD '93, Proceedings of the 5th International Symposium on, Monterey, CA, 16-21, (1993) doi: 10.1109/ISPSD.1993.297099

[14] K. Shenai, “True Figure of Merit (FOM) of a Power Semiconductor Switch.” *ECS Transactions* 58 (4): 199–210 (2013). 10.1149/05804.0199ecst.

[15] W. C. Nunnally and R. B. Hammond, “Optoelectronic switch for pulsed power”, edited by Chi. H. Lee, Orlando, Florida: Academic Press, Inc., 1984. ISBN: 978-0-12-440880-7. doi: 10.1016/B978-0-12-440880-7.X5001-9

[16] M. D. Miller, "Differences between platinum- and gold-doped silicon power devices," in *IEEE Transactions on Electron Devices*, vol. 23, no. 12, pp. 1279-1283, Dec. 1976, doi: 10.1109/T-ED.1976.18650.

[17] R. O. Carlson, Y. S. Sun and H. B. Assalit, "Lifetime control in silicon power devices by electron or gamma irradiation," in *IEEE Transactions on Electron Devices*, vol. 24, no. 8, pp. 1103-1108, Aug. 1977, doi: 10.1109/T-ED.1977.18884.

[18] M. W. Hüppi, “Proton irradiation of silicon: Complete electrical characterization of the induced recombination centers”, *Journal of Applied Physics*, vol. 68, no. 6, pp. 2702–2707, 1990. doi:10.1063/1.346470.

[19] J. F. Ziegler, J. P. Biersack, M. D. Ziegler, "The Stopping and Range of Ions in Matter”, *Lulu Press Co,* Morrisville, NC

ONR HPM Program - Monthly Status Report (MSR) – MARCH 2021

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 APRIL 2021

Distribution Statement ~A: Distribution authorized to all OSPRES Grant and Contract performers, and any OSPRES uncompensated collaborators. Further dissemination per the Office of Naval Research, Ryan Hoffman (ryan.hoffman@navy.mil, 703-696-3873) or higher DoD Authority.

OSPRES Grant Goal: address and transition technologies and capabilities that enable the OSPRES Grant Objective using the OSPRES Grant Approach, while educating the next generation of pulsed power and defense minded, stewards and innovators.

OSPRES Grant Objective: to execute high-risk, high-payoff efforts that mitigate, fill or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable and electronically steerable high power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average power space, and includes the kill chain considerations including the target and its responsivity to radiofrequency stimuli.

OSPRES Metrics of Success: developed technologies and capabilities that are published in the peer review, protected as intellectual property, and/or, transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use, as enabling/integratable capability(ies).

OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

OSPRES Grant Security: All efforts should be fundamental and publically releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

1.0 Contents

2.0 Executive Summary 3
2.1 Progress, Significant Findings, and Impact 3
2.2 Completed, Ongoing, and Cancelled Sub-Efforts 4
2.3 Running Total of Academic and IP Program Output 5
3.0 Switch Evaluation and Innovation 6
3.1 Lasers and Optics 6
3.2 WBG-PCSS Enabled Laser Diode Array Driver 9
3.3 Diode-Based NLTLs 11
3.4 Si-PCSS Top Contact Modeling and Optimization for Cooling Requirements 16
3.5 GaN:C PCSS Direct RF Modulation 21
3.6 Drift-Step Recovery Diode and Pulse Shaping Device Optimization 23
4.0 Prime Power and Conditioning 33
4.1 HV Switch Pulsed Chargers 33
5.0 Tradespace Analysis of Ultra-Wide-Band Antenna Arrays 37
5.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs) 37
5.2 Tradespace Analysis of Other Ultra-Wide-Band (UWB) Single Elements 43
5.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna 50
5.4 Tradespace Analysis of Ultra-Wide-Band (UWB) Fractal Antenna 55
6.0 RF Coupling 62
6.1 Enclosure Effects on RF Coupling 62
7.0 Thermal Management 67
7.1 Micro-Jet Thermal Management System 67
7.2 Nanofluid Heat Transfer Fluid Development 67
8.0 Program Management 75
8.1 Issues 75
8.2 Interactions with Others 75
8.3 Major Procurement Actions 75
8.4 Travel 75
8.5 Pending or Upcoming Public Release Requests 75
9.0 Appendix B: Academic and IP Output 76
9.1 Students Graduated 76
9.2 Conference Publications 76
9.3 Journal Publications 80
9.4 External Presentations/Briefings 81
9.5 IP Disclosures Filed 82
9.6 Provisional Patents Filed 82
9.7 Non-Provisional Patents Filed 82

2.0 Executive Summary

2.1 Progress, Significant Findings, and Impact

The tunable diode-based nonlinear transmission line demonstrated a linear relationship between the DC bias potential and center frequency up to the saturation of the diode's CV curve after which the frequency no longer changes. It was also demonstrated that diodes can be stacked in series to achieve larger center frequencies and power output if diode parasitics (lead inductance and shunt capacitance) are minimized.

Weak initial results suggest that operating GaN:C in a bistable mode may be possible, as persistent photoconductivity has been observed it needs to be determined if persistent photoconductivity/lock-on is achievable at higher currents. This work is being put on hold to support OSPRES contract efforts.

Previously elusive pulse sharpening device (PSD) TCAD simulations showed pulse-sharpening capability on the 100-ps order, as observed experimentally; this capability now serves as a platform for optimizing PSD design/fabrication, and, modeling DSRD-based systems in full.

A power conditioner circuit, featuring a 12-kV rated SiC MOSFET, as a BEHLKE replacement, has been designed and fabricated.

The novel method to design wide-bandwidth microstrip ESA elements, presented in earlier reports, has been experimentally validated (in terms of S-parameters and gain).

The antenna metrics comparison between SOTA BAVA and Koshelev antenna for similar physical aperture area have shown promising results from the Koshelev antenna. The aperture efficiency of the Koshelev antenna is much higher than the SOTA BAVA for a similar physical aperture area. The parametric study of Shark antenna yielded a complete understanding of its parameters and their effect on the bandwidth. This study produced Shark antenna design parameters, whose physical aperture area is less than the SOTA BAVA and yielded significantly high aperture efficiency.

Two versions of a complete UAV with all the wires and all the lC components to use as a numerical platform for studying effects and validating predictions have been built. Version 1 is the accurate replica of the UAV has all the components modeled as a linear 50-Ω load, as a first approximation of the model. Version 2 is the simplified UAV model where all the wires of the UAV arm are replaced by an equivalent single wire. We run exhaustive numerical Frequency domain experiments to study the response to different incident electromagnetic waveforms for both versions. Our analysis shows that the simplified version, version 2, can accurately model the response of the actual UAV wiring system. Moreover, it saves computational time significantly.
.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

	Start	End
2.2.1 Ongoing Sub-Efforts		
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
HV Switch Pulsed Chargers	DEC 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Enclosure Effects on RF Coupling	OCT2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
Nanofluid Heat Transfer Fluid	NOV 2020	Present
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization	JAN 2021	Present
2.2.2 Completed Sub-Efforts		
Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
2.2.3 Cancelled/Suspended Sub-Efforts		
Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020
Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021
Bistable Operation of GaN	FEB 2021	MAR 2021

2.3 Running Total of Academic and IP Program Output

See Appendix A for authors, titles and inventors (this list is continuously being updated)

2.3.1	*Students Graduated*	5 BS, 6 MS, 2 PhD
2.3.2	*Conference Publications*	36
2.3.3	*Journal Publications*	2 (4 submitted/under revision)
2.3.4	*External Presentations/Briefings*	18
2.3.5	*IP Disclosures Filed*	9
2.3.6	*Provisional Patents Filed*	1
2.3.7	*Non-Provisional Patents Filed*	0

3.0 Switch Evaluation and Innovation

3.1 Lasers and Optics

(Scott Shepard)

3.1.1 Problem Statement, Approach, and Context

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$50K to \$5M.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution. This way of implementing an optical fiber laser (via an optical fiber amplifier) has SWaP advantages with respect to traditional (fiber and free-space) laser designs.

Sub-Problem (1): Optical pump power system costs are the dominant source of costs (in both normal/free-space lasers and in optical fiber lasers, of this class).

Sub-Problem (2): Amplified spontaneous emission (ASE) and fiber nonlinearities impede the optical amplifier performance.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive until reduced by a factor of two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping scheme which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments we are pursuing the use of gain saturation and a staged design of different fiber diameters.

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system needed to drive the PCSS will meet the modular and scalable volume and cost aim-points.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability.

3.1.2 Tasks and Milestones / Timeline / Status

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Ongoing.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Ongoing.

(E) Demonstrate a cost-reduced fiber laser. / Ongoing.

(E1) **March 2021** Finalize design.
(E2) **April 2021** Assemble and test-check seed LDs/drivers.
(E3) **April 2021** Measure power vs current transfer function of seed LDs/drivers.
(E4) **May–June 2021** Measure ASE and jitter of 1064 nm seed LD/driver.
(E5) **May–June 2021** Measure ASE and jitter of 1030 nm seed LD/driver.
(E6) **May 2021** Assemble and test-check pump LDs/drivers.
(E7) **May 2021** Measure power vs current transfer function of pump LDs/drivers.
(E8) **May 2021** Splice power combiners to Yb doped preamp fiber.
(E9) **May 2021** Connect seed and pumps to power combiners and test-check.
(E10) **June–July 2021** Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle.
(E11) **June–July 2021** Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle.
(E12) **July 2021** Splice power amplifier and its power combiner to best preamp.
(E13) **July–August 2021** Measure gain, ASE and jitter of entire amp assembly.
(E14) **July–August 2021** Analyze data and document.

(F) Design a new type of higher power, tubular core, fiber amplifier. / Ongoing.

3.1.3 Progress Made Since Last Report

(E1) A vendor suggested that we consider using their new improved fiber (30 micron core instead of 25 microns, and increased pump absorption). Recalculation of the resulting gain at the fiber lengths of the previous design surprisingly predicted a drop in overall gain by 3. However, an overall improvement in the final design was achieved by changing the pump wavelength (from 976 to 915 nm). Re-optimization of the design at 915 nm led to a restoral of the overall gain at new fiber lengths (now 2 [m] for the pre-amp and 6 [m] for the poweramp). The larger core fiber and new pump wavelengths constitute an improved final design (in pump efficiency and nonlinearity thresholds).

(E8) To splice fiber (required since connectors are not viable at our high power levels) we unsuccessfully searched for a fusion splicer of cost less than the $50k version. However, we found a power combiner vendor who is willing to do our splicing for us (at a total cost of $7k). This fortunate negotiation resulted, in part, from the vendor's interest in partnering on the development of the technology of our new tubular core fiber amplifiers.

(F) Conceived a new tubular core fiber amplifier wherein (with standard manufacturing techniques) we can increase the surface area (hence the heat transfer) by a factor of 100 and increase the cross-sectional area (hence the nonlinear thresholds) by a factor of 200, with respect to a 50 micron core fiber of the same unit length.

3.1.4 Significant Finding(s) and Mission Impact

3.1.4.1 Summary to Date

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with tolerable pre-burst ASE. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

3.1.4.2 Since Last Report

(E1) The design of the proof-of-concept experiment was finalized in March on schedule. Incorporating a newly offered, similarly priced larger core fiber (30 microns instead of 25) improves our nonlinearity thresholds. More significantly, changing our pump wavelength (from 976 to 915 nm) permits the use of such and increases our pump efficiency as follows. Ytterbium's absorption peak (in a silica glass host) peaks near 976 nm – which is why early work pumped at that wavelength. Yet, that also is at the peak of its emission cross-section so that pumping at 976 nm also creates more stimulated emission. The result is that only 50% population inversion can be achieved. A lower absorption peak near 915 nm corresponds to a lower pump absorption rate, but the stimulated emission is less at 915 nm, so that a higher population inversion (hence higher gain) can ultimately be achieved. The lower pump absorption rate at 915 nm enabled the optimization which restored our desired output power at lengths similar to the original design (the pre-amp changed from 2.4 [m] to 2 [m] and the poweramp changed from 5.3 [m] to 6 [m]). Whereas blindly accepting the new improved fiber (at the same lengths) would have reduced our output power by a factor of 3. This illustrates the extreme sensitivity of fiber amplifier design on its interrelated underlying parameters.

(F) Fiber amplifiers with cores of circular cross-section have reached a fundamental limit due to the conflicting constraints of thermal lensing (proportional to core area) and nonlinear impairments (inversely proportional to core area). Rectangular-core fiber amplifiers radiate heat more efficiently as they have a larger surface area than a circular core of the same enclosed volume. Moreover, the thermal lensing is limited by the smaller dimension of the rectangle while the larger dimension is permitted to increase in order to mitigate the nonlinearities. We extend the advantages of the rectangular core into a tubular geometry – increasing the larger dimension of the rectangle. With manufacturable dimensions of a 2.5 [mm] outer diameter tube, of 100 [μm] thickness, we have shown that we can increase both the heat transfer (by a factor of 100) and the nonlinearity thresholds (by a factor of 200) with respect to a 50 micron circular-core fiber of the same unit length.

3.2 WBG-PCSS Enabled Laser Diode Array Driver

(John Bhamidipati)

3.2.1 Problem Statement, Approach, and Context

Primary Problem: Need for heavy (~125 lbs.), bulky (~10 cu-ft), and expensive (~$120,000) conventional laser systems (1064 nm) in PCSS-based HPM applications, with an additional need for second and third harmonic generation (SHG/THG) optics to trigger wide bandgap (WBG) solids (GaN/SiC).

Solution Space: Design and implement a compact (~1.1 cu-ft), lightweight (10–15 lbs.), and inexpensive (<$15,000) alternative for conventional high average power optical trigger (laser) system to improve SWaP-C^2 index of HPM systems.

Sub-Problem: Unavailability of commercial-off-the-shelf (COTS) miniature optical sources with sub-nanosecond pulse widths and tens-of-μm beam width, delivering >1-Watt power to implement as a makeshift/turnkey solution for the laser system.

State-of-the-Art (SOTA): High average power picosecond pulsed lasers available up to 50 W output power with a gain factor up to 40 dB (~10,000x power) with laser amplifier.

Deficiency in the SOTA: High average power 1064-nm pulsed lasers are bulky and require auxiliary systems as well as additional optics for SHG/THG generation for WBG device triggering.

Solution Proposed: Multi-stage laser diode array (LDA) driver powered by seed-laser-diode-driven avalanche WBG-PCSS as a compact, inexpensive laser replacement.

Relevance to OSPRES Grant Objective: Provides an enhanced SWaP-C^2 compliant solution for the laser (optical trigger) subsystem, with a subsequent impact on overall HPM system cost, volume, and power (optical and electrical) requirements.

Risks, Payoffs, and Challenges: Complex interconnect and thermal management system (TMS) design at high temperature (130–175°C) operation; unavailability of COTS high power pulsed laser diodes could potentially raise a need for research in laser diodes (arrays).

3.2.2 Tasks and Milestones / Timeline / Status

(A) Complete initial feasibility study for the cascaded multi-stage optical amplifier design and determine functional requirements for the laser diodes (arrays) and source driver [DEC–JAN 2020 / completed].

(B) Complete initial stage experimental implementation of the PCSS-based driver and demonstrate positive current gain using GaN-PCSS, triggered with a 404 nm laser diode. [APR–MAY 2021 / in progress].

(C) Define performance metrics for PCSS-based driver and complete numerical calculations for required output current at each stage and corresponding PCSS (GaN/GaAs) operating voltages in light of electric fields required for lock-on/avalanche mode, establish real-time implementation timeline, cost estimates, jitter limitation, and

explore ways to protect LDA from PCSS ringing. [MAR 2021 / partially complete / revisit after completing (B)].

(D) Study the feasibility of using mode-coupling in a slab geometry to bring the laser light into GaN/GaAs devices with reduced laser energy – modeled in COMSOL simulations [MAR–APR 2021 / in progress].

(E) Proof of concept test with a 50 Ω load at 1 kHz pulse repetition rate (PRR) [JUN–JUL 2021]

(F) Working prototype demonstration at ~MHz PRR with laser diode array/stack and ancillary optics based on HPM source driver needs including thermal management system (TMS). [AUG-SEP 2021]

3.2.3 Progress Made Since Last Report

(A) A comprehensive review of SOTA COTS laser diode drivers has been done in terms of output current, transient response and form factor to determine the metrics required for the WBG PCSS-based driver to overcome the SOTA limitations.

(B) Laser diodes and driver module have been procured for experimental implementation and initial testing of lateral GaN-PCSS (sourced through NRL) with switch gaps of 50 and 100 μm is underway.

(C) Numerical calculations were done to estimate output current requirement at each stage, corresponding operating voltages, and on-state resistance at varied pulse repetition rates. Impedance matching networks and rectifier circuits have been studied to mitigate power reflections and PCSS ringing, respectively. SPICE modeling is underway to finalize the components. Numerical calculations, cost estimates and jitter limitations will be revisited after the completion of (B).

(D) Mode coupling simulations were done via COMSOL for models with two dielectric slabs with dimensions 1 μm x 1 μm x 1 mm mounted one over the other with (i) silica (SiO_2)-over-SiO_2 and (ii) SiO_2-over-GaN geometries, leaving an airgap of 0.1 μm between the slabs and excited with a 25 μm optical pulse along the boundary of the top slab (silica). Better mode coupling has been seen in SiO_2-over-GaN geometry at airgaps ≤0.1 μm, but the simulation results were inconclusive due in part to the induction of higher order modes that need to be reduced by better matching the input field amplitude to the anticipated fundamental mode.

3.2.4 Significant Finding(s) and Mission Impact

3.2.4.1 Summary to Date

(A) State-of-the-art COTS laser drivers' specifications and limitations have been comprehensively studied and target performance metrics have been determined in terms of output current (>120 A), PRR (>1 MHz), transient response (<200 ps risetime and <1 ns pulse width) and volume (<0.75 cu-ft). A preliminary feasibility study has signified the need for lock-on conduction mode with ~$10^{2.6}$ gain factor to drive at >1 MHz pulse repetition rate (PRR) while limiting the amplification stages to 2. This

reduces monetary costs to 10–12% of the conventional laser system, while achieving the expected goal of miniaturizing the optical subsystem by 90%.

(C) Numerical calculations have been completed to estimate the electric fields and corresponding voltage bias required to induce lock-on operation while exploring ways to minimize the potential risks of high jitter at ~MHz order PRR switching, power reflections due to impedance mismatch and negative ringing currents during PCSS recovery. Expected on-state resistance and power dissipation for 50 µm and 100 µm devices in lock-on conduction mode have been calculated to estimate cooling system requirements while retaining the expected SWaP-C^2 factor.

(D) Kerr-induced self-focusing in silica fibers has been studied to understand beam characteristics and to deliver the laser light into the PCSS with reduced laser energy. However, initial results were inconclusive due in part to difficulties in distinguishing multi-mode effects from effects. In the interest of enabling progress, we have eliminated nonlinear effects and focused on mode-coupling study via COMSOL simulations for dielectric slab geometries separated by gap of µm/sub-µm order to reduce the required laser energy for GaN/GaAs device triggering. Thus far, simulation studies have been performed for SiO_2-SiO_2 and SiO_2-GaN dielectric slabs with 0.1-µm air gap. Better mode coupling has been seen in SiO_2-over-GaN geometry, at airgaps ≤0.1 µm, however the simulation results showed induction of higher order modes and phase shifts raising a need to quantify the phenomena mathematically.

3.2.4.2 Since Last Report:

(A) A comprehensive review of SOTA COTS laser diode drivers has been done in terms of output current, transient response and form factor to determine the metrics required for the WBG PCSS-based driver to overcome the SOTA limitations.

(C) Possibility of pulse reflections due to impedance mismatch in pulse forming networks (PFNs) and negative currents during PCSS recovery have been investigated and techniques to mitigate them have been proposed.

(D) COMSOL simulations in dielectric slabs have shown the existence of mode coupling when the slabs are separated by ≤0.1 µm. However, the mode coupled slab has shown higher order modes which need to be reduced by better matching the input field amplitude to the anticipated fundamental mode.

3.3 Diode-Based NLTLs

(Nicholas Gardner)

3.3.1 Problem Statement, Approach, and Context

Primary Problem: The size, weight, and cost of pulse forming/shaping networks (PFNs) need to be reduced and optimized for Navy afloat missions.

Solution Space: Develop a lumped-element nonlinear transmission line (LE-NLTL) as a pulse shaping network for the conversion of energy to the ultra-high frequency (UHF) band at single MW peak power.

Sub-Problem: Metrics used for component selection are designed for LE-NLTLs operating at sub 0.1 GHz frequencies. Using such metrics alone to design LE-NLTLs capable of single GHz frequency generation introduces a trial by error nature to the design process wherein frequency/power generation predictions and measurements can differ by a few hundred MHz or the design potentially fails to operate at all.

State-of-the-Art (SOTA): LE-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit. Simulations of LE-NLTLs indicate achievable frequencies in the single GHz range.

Deficiency in the SOTA: Simulation/measurement agreement becomes increasingly sensitive to parameters and factors outside of inductive and capacitive element choice alone at frequencies above ~100 MHz. Disparities between measurement and simulation above contribute to a trial by error design process for LE-NLTL networks.

Solution Proposed: Identify and characterize diode parameters affecting frequency generation in the context of a NLTL application and identify limits/desired ranges required for UHF generation. Such parameters include, but are not limited to: diode frequency response, diode reverse bias hold-off voltage, diode small signal capacitance, diode chip/package parasitics, and diode relaxation time. The improved understanding of the explored parameters will be used to design and fabricate a LE-NLTL capable of GHz center frequency generation at single MW peak powers.

Relevance to OSPRES Grant Objective: The SWaP-C^2 capabilities of LE-NLTLs (shown in Figure 3.3.1) represent a potential solution to the size, weight, and cost optimization issue for PFNs on Navy afloat missions.

Figure 3.3.1. 20 cell LE-NLTL of dimensions 1.1 x 23.45 cm constructed with COTS components.

Risks, Payoffs, and Challenges: There exists a potential tradeoff between power and frequency generation. Devices such as ceramic capacitors may be used in a LE-NLTL to generate high peak power due to their break down potentials in the 10s of kV, however, such devices become highly resistive at 0.1–0.2 GHz frequencies. Diodes have been shown to be operational at frequencies upwards of 0.4 GHz, however, possess low hold-off potentials limiting peak output power. The payoff to overcoming these challenges is significant reductions in PFN size and cost.

3.3.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Construct/demonstrate a prototype capable of UHF generation at low voltages (1–100 V excitation amplitude)

   a. Task – Break a low-voltage pulse into a sequence of solitons (Completed SEP20)

   b. Task – Increase frequency generation past 200 MHz (Completed NOV20)

c. Task – Select diode candidate (junction capacitance <50 pF) and simulate expected results (Ongoing MAR–APR21)

d. Task – Design/fabricate/test line (Ongoing MAR–APR21)

(B) Milestone – Demonstrate tuning of waveform at low voltages using electrical or mechanical means

a. Task – Simulate a topology capable of biasing the diodes using a DC voltage (Completed JAN21)

b. Task – Construct and perform initial tests on prototype (Completed JAN–FEB21)

c. Task – Troubleshoot prototype design and identify differences with simulation (Completed FEB21)

d. Task – Collect data to show electrical tuning with a positive DC bias (**Completed MAR21**)

e. Task – Refine topology to reduce loses (**Completed MAR21**)

f. Task – Collect data on the effect of using a negative DC bias on the line (**NEW APR21**)

(C) Milestone – Construct/demonstrate a prototype capable of frequency generation above 1 GHz at single MW peak powers (Completed MW peak power but not GHz center frequency)

a. Task – Identify diode candidates with a hold-off voltage of several kV and a low signal junction capacitance under 100 pF (Completed JAN21)

b. Task – Design/fabricate single diode prototypes (Completed JAN21)

c. Task – Perform initial tests using half-barrel pulse source (Completed FEB21)

d. Task – Compare measurements with simulation and identify discrepancies (Completed FEB21)

e. Task – Design/fabricate/test prototype using two diodes in series (Completed FEB–MAR21)

f. Task – Test both lines with pulses of varying characteristics to determine full line behavior (**MAR–APR21**)

g. Task – Compare single and two diode line results to determine the advantages and tradeoffs to obtaining increased peak power and frequency through diode stacking (**MAR–APR21**)

(D) Milestone – Demonstrate power scalability using an array of LE-NLTLs (On hold until milestone C is completed)

3.3.3 Progress Made Since Last Report

(B) Constructed a refined tunable prototype to reduce sources of resistive and inductive losses. Measurements show a linear relationship between applied DC bias and generated

center frequency up to the point where the diode becomes saturated. At the saturation point the applied DC bias ceases to affect the generated center frequency. Further discussion is presented in 3.3.4.2 with results shown in figure 3.3.2.

(C) Both the K100F based NLTL and K50F based NLTL were tested back to back with a half barrel DSRD (HB source) based pulsed source for comparison. 15 different tests were run; 5 shots of the HB source pulse, 5 shots of the pulse after the K100F line, and 5 shots after the K50F line. Results showed similar rise times generated by each line reducing the rise time of the pulse from ~1ns to ~600-700 ps. Further discussion is presented in 3.3.4.2 with results shown in figure 3.3.3.

3.3.4 Significant Finding(s) and Mission Impact

3.3.4.1 Summary to Date

(A) After a failure of the high-voltage diode-based nonlinear transmission lines (D-NLTLs) to reproduce simulated results, work refocused on low-voltage D-NLTLs to determine the source of the discrepancy. In NOV2020 a center frequency of ~250 MHz was achieved using a D-NLTL design based on the diode model SMV1702.

(B) Following the success of the SMV1702 D-NLTL a circuit was designed capable of electrically tuning the center frequency utilizing DC biasing of the diodes. In FEB-MAR2021 the circuit demonstrated a linear relationship between DC bias up to a limiting potential.

(C) In JAN2021 two diode candidates (models K100F and K50F) were identified for a HV D-NLTL design. FEB2021 saw successful tests of both D-NLTLs with each sharpening the rise time of a pulse produced by a DSRD based source down from ~1 ns to ~600 ps.

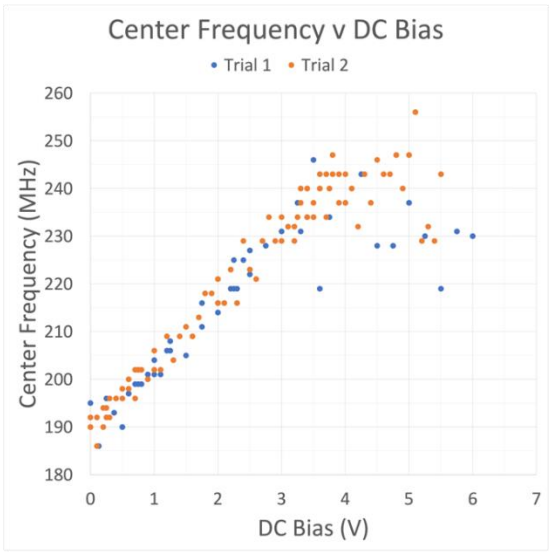
3.3.4.2 Since Last Report

LE-NLTL frequency tuning demonstration (B): A linear relationship was found between applied DC bias and center frequency up to a point where DC bias no longer affected the center frequency. These results indicate that it is possible to alter the behavior of the network without physical alterations to the network. Full results acquired for the initial design are shown in Figure 3.3.2b followed by a revision of the design, shown in Figure 3.3.2c. Both designs show a linear relationship between applied DC bias and generated center frequency up to a limiting potential. At this limiting potential (around 3.5–4 V) the diode becomes saturated, the line ceases to be strongly nonlinear, and the applied DC bias no longer changes the center frequency.

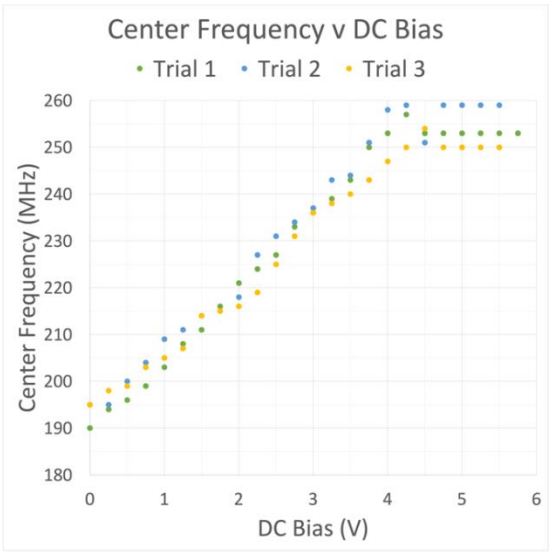
GHz MW D-NLTL prototype (C): The K100F based D-NLTL and K50F based D-NLTL were tested back-to-back with the DSRD half-barrel source to ensure as much similarity as possible between the pulses that excited each line. On average the HB source generated pulses with a rise time of 1.12 ns and an amplitude of 1.09 kV. The K100F network reduced the rise time of these pulses down to an average of 632 ps with little change in amplitude. The K50F network reduced the rise time of the pulses down to an

average of 696 ps with an average amplitude of 1.2 kV. The larger rise time of the K50F network was expected due to greater losses introduced when using diodes stacked in series. Ideally the K100F network should have produced a larger amplitude than the K50F network for the same reason, however the connections used to connect the board to the HB source needed to be re-soldered in between tests. A better solder connection on the K50F line can account for the ~1% different in amplitudes between the two lines.

(A)

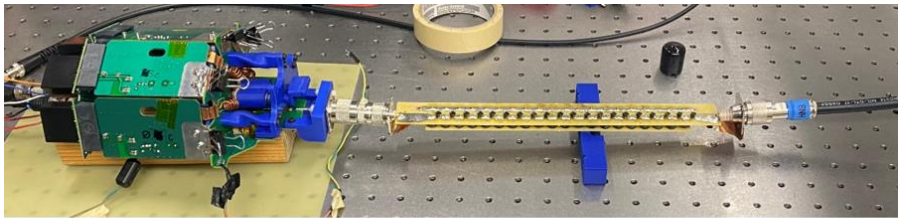


(B)

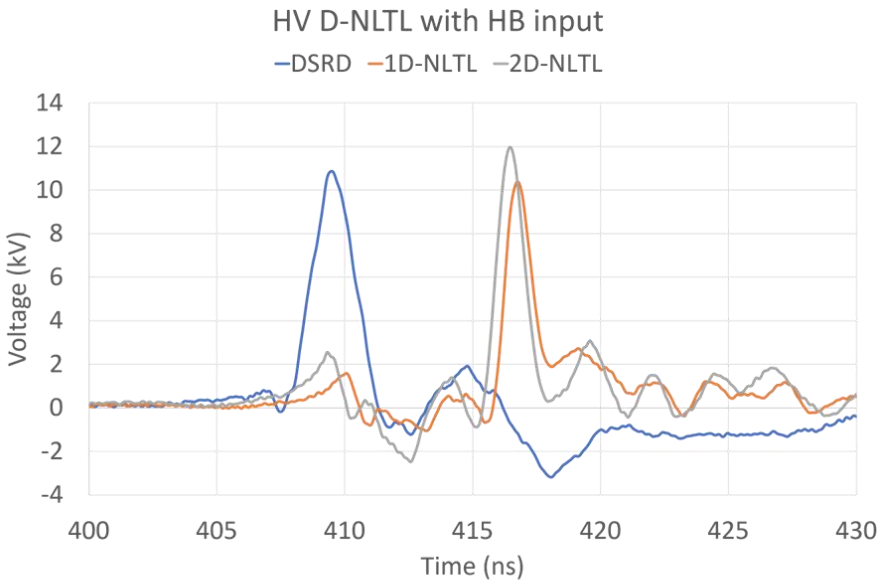


(C)

Figure 3.3.2. Results for tunable D-NLTLs in March. (a) The refined tunable circuit: through hole 1 kΩ resistors have been replaced with surface mount resistors to reduce excess inductive losses, the single DC input has been replaced with 2 DC inputs for reduction in resistive losses. (b) Results for the original tunable circuits. (c) Results for the refined circuit. Both sets of results show a linear relationship between DC bias and center frequency up to a point where the diode saturates, and DC bias no longer affects center frequency.



(A)



(B)

Figure 3.3.3. (A) K50F based D-NLTL connected to the half barrel DSRD based source. (B) Results for each line; blue represents the pulse initially generated by the HB source, orange represents the waveform generated by the K100F based D-NLTL, grey represents the K50F based D-NLTL.

3.4 Si-PCSS Top Contact Modeling and Optimization for Cooling Requirements

(Jay Eifler)

3.4.1 Problem Statement, Approach, and Context

Primary Problem: High-average-power 1064-nm picosecond class lasers are too large (1100 cm^3/W) and monetarily expensive ($1000/µJ*pulse) for the Navy afloat missions. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). And a lab laser will cost $100,000 and deliver 100 µJ of laser energy to the Si-PCSS through fiber with 50% energy losses.

Solution Space: By altering only Si-PCSS device parameters, one can enable both a laser size and cost reduction in the design of a laser. Specifically, to reduce the size and

cost of the laser, the laser energy required by the Si-PCSS can be reduced by altering the Si-PCSS top contact laser windowing spacing. However, the tradeoff between laser energy reduction and device heating (and therefore, required cooling) resulting from the top contact design and geometry must be evaluated and optimized.

***Sub-Problem*:** By altering only the peak doping concentration of the Si-PCSS anode side (p-side), maximize the voltage holdoff while minimizing on-state resistance while satisfying ohmic contact requirements. The ohmic contact requirements are: durability for high current and high power, low resistivity for high frequency, doping-dependent specific contact resistivity of the metal-semiconductor (MS) junction, temperature dependency, and I-V ohmicity of MS junction. However, this optimization must also eventually consider the laser energy reduction and cooling required.

State-of-the-Art (SOTA): Si-PCSS top contact pattern designs are not known to have been published in detail. In-house patterns have used only an outer ring for the contact (resulting in high on-state resistance) and were improved by metallizing across the ring with filaments (to reduce current density high-points), similar to solar cell top contact designs. The Si-PCSS laser windowing spacings used were 10- and 20-µm, with 20-µm achieving sufficiently low sub-ohm on-state resistance using in-house laser energy of ~100-µJ delivered to the Si-PCSS.

Deficiency in the SOTA: There is no justification for 20-µm spacing being optimal for producing low sub-ohm on-state resistance with the least required laser energy and cooling (also dependent upon laser and cooling system capabilities).

Solution Proposed: Optimize OSPRES Si-PCSS top contact patterns using TCAD to meet required cooling (maintain <80°C device temperature, including hotspots) and reduce laser energy over a range of possible on-state resistances.

Relevance to OSPRES Grant Objective: Optimized top contact patterns require less laser energy and cooling which enhances SWaP-C[2] for the laser system needed to drive the Si-PCSS and maintain device operation lifetime in excess of $2x10^8$ shots/lifetime at medium power.

Risks, Payoffs, and Challenges: The top contact design does not have the most direct impact on laser system size and cost. A smaller, more effective laser is needed. However, the metallization for optimized top contacts is inexpensive and easy to manufacture. The TCAD models have various limitations: full device size too large, only single-pass laser absorption, limited external thermal bodies and heat flow mechanisms, cannot transiently charge transmission line, and only single to few pulses feasible for Si-PCSS.

3.4.2 Tasks and Milestones / Timeline / Status

(A1) RDT will fabricate 2 wafers of variable window Si-PCSS. (20, 40, 60, 100, 200, 350 µm) spacings for 1 cm devices, with 6 of each on 1 wafer, will be made. And 60 µm and 350 µm for 7 cm devices, with 5 of each, will be made on another wafer. / FEB 2021 / Devices delivered to UMKC FEB 4, 2021.

- Milestone: achieved for fabricating and receiving variable window Si-PCSS.

(A2) UMKC will measure on-state resistance vs laser energy for Si-PCSS devices with various window spacings. / FEB–MAR 2021 / One 7 cm, 350 µm window Si-PCSS has been tested. 1 cm, variable window devices to be tested.

(B) Perform TCAD studies to optimize laser windowing spacing using heat removed from the Si-PCSS with the addition of temperature hotspots. The studies will quantify the tradeoff between reduced laser energy for on-state resistance vs reduced cooling. Additional development of the thermal models will include carrier recombination–generation heating, external thermal bodies, and improve computational efficiency (to enable studies over a range of laser energies). / First thermal TCAD simulations performed on DEC 4, 2020. Initial thermal spacing study finished JAN 30, 2020. / On-going status (no timeline set yet for continued work, waiting for variable window experimental results).

- Milestone: summary of contact spacing vs heat removed and device temperature at 94 µJ of laser energy (assumes no fiber).

(C) Perform TCAD studies to determine relationship between peak p-doping concentration (anode side) and device performance (on-state resistance, voltage holdoff and ohmic contact requirements). An optimal p-doping concentration can then be determined. To be consistent with earlier top contact spacings used for reduced laser energy and/or reduced cooling, models include doping-dependent free-carrier absorption photogeneration and thermal modeling. / First TCAD simulation performed NOV 11, 2020. Last TCAD simulations finished JAN 30, 2020. / On-going status (no timeline set yet for continued work).

3.4.3 Progress Made Since Last Report

(A2) Fourteen 1 cm Si-PCSS devices were tested for on-state resistance vs laser energy. Devices showed variability for cases where there was more than one device. Si-PCSS with 100 µm windows or greater as a group had lower on-state resistance than with windows less than 100 µm.

3.4.4 Significant Finding(s) and Mission Impact

3.4.4.1 Summary to Date

Variable window Si-PCSS were fabricated and delivered to UMKC and testing began for on-state resistance vs laser energy. The 7 cm devices were badly damaged and a single device was testable and showed a 15-20% possible laser energy reduction from the data, but due to possible device variability the results are inconclusive. 1 cm devices have been tested and show a possible 22% laser energy reduction between devices with 100 µm and greater window spacing vs less than 100 µm window spacing. Additional 1 cm device fabrication and testing will reduce contributions from device variability and improve the results for the experimental laser energy reduction vs spacing. The improvement will allow for a simulation and experiment comparison of laser energy reduction vs individual spacings rather than the grouping into 100 µm or greater spacing vs less than 100 µm spacing.

3.4.4.2 Since Last Report

(A2) A new measurement method for the on-state resistance vs laser energy on Si-PCSS devices was carried out. These were for the variable window devices. The new method related laser pulse energy to transmission charge and load voltage on a pulse-per-pulse basis rather than averaged over a train of pulse as was done in earlier measurements. This new method was used to improve the measurement accuracy, but has not resulted in an improvement to the measurement.

In Figure 3.4.1 is shown the on-state resistance vs laser energy for 14 variable window Si-PCSS. Open symbols are for the 100 µm and greater window spacing and closed for the less than 100 µm spacing. Excluding the 60um-s5 case (60 µm window spacing of switch 5), all the lower on-state resistances belong to open symbols which have 100 µm or greater window spacing and in TCAD simulation all had low optimal on-state resistance. The 60um-s5 Si-PCSS device along with the other two devices with 60 µm spacing show the device variability alone results in a wide range of on-state resistance (closed triangles).

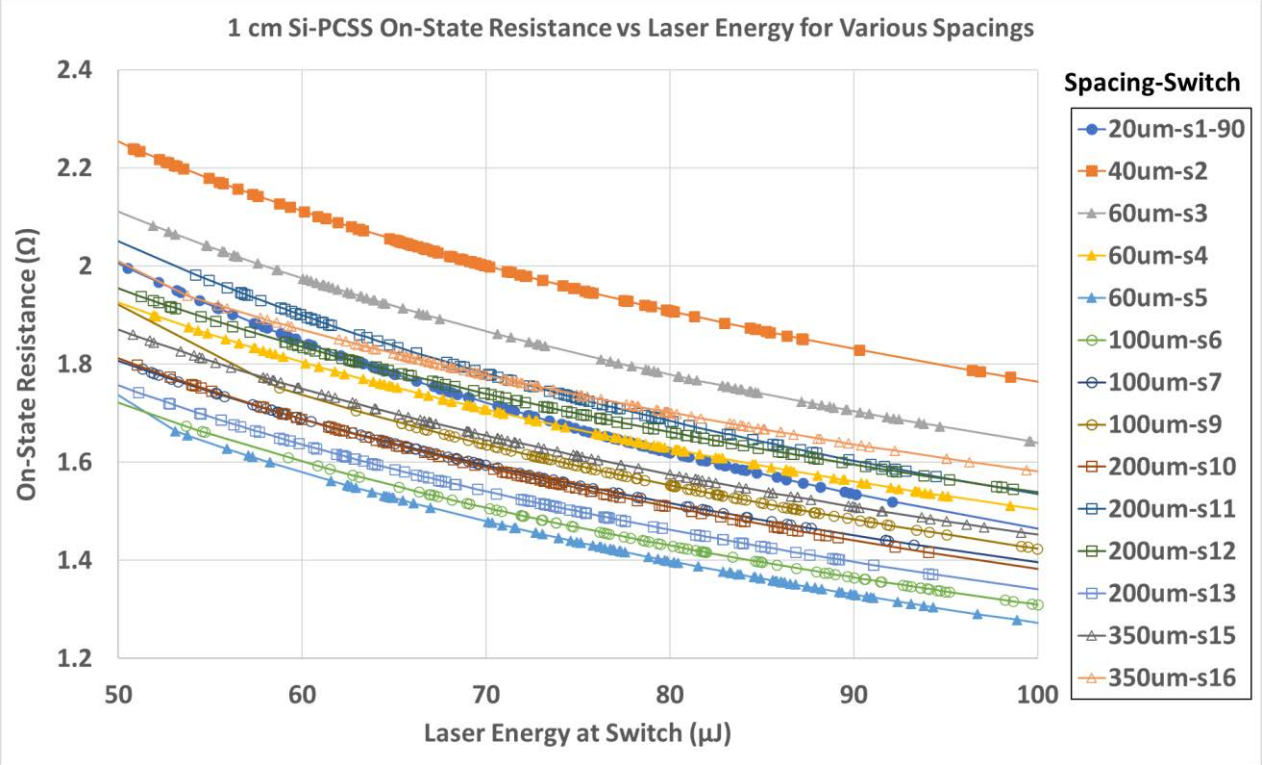


Figure 3.4.1. New experimental measurements of on-state resistance vs laser energy for the variable window Si-PCSS. Open symbols are the majority of lower on-state resistance devices and are the 100 µm or greater window spacings.

In Figure 3.4.2 the same data are shown but the power law data fit is for the 100 µm and greater devices (orange) and less than 100 µm devices (grey), rather than each spacing

due to the number of devices. Comparing the 100 µJ laser energy used on the smaller windows (grey), at the same on-state resistance but for larger windows (orange) the laser energy is 78 µJ or a 22% laser energy reduction. If the same spacings and number of devices per spacing is used from the TCAD simulated data, the predicted laser energy reduction between the larger and small window groups would be 13%.

The experimental data set contains device variability in addition to the effect of variable windows on Si-PCSS on-state resistance even with devices grouped into the two groups. There are only single devices for the 20 µm and 40 µm spacings which skews the result. More devices need to be fabricated and tested to determine a quantitative experimental verification of the simulation prediction for laser energy reduction vs spacing. Simulation showed a maximum 30% possible laser energy reduction. The latest experimental results show qualitatively that the 100 µm and greater window spacing (100, 200, 350 µm) has lower on-state resistance, over 5 µJ – 250 µJ of laser energy tested, than the less than 100 µm window spacings (20, 40 60 µm). Due to the device variability and the number of devices tested the quantitative laser energy reduction of 22% is over-estimated when compared to the simulation results, predicting 13% for the same numbers of devices at each spacing into the two groups. However, all the experimental results for 7 cm and 1 cm devices have fallen within the simulation maximum predicted 30% possible laser energy reduction. It should also be noted that the 1 cm devices tested were not good sub-ohm Si-PCSS but had ohm-level on-state resistance due to the damage from dicing with a new in-house dicing saw. In part due to this fabrication error, two wafers of 1 cm devices are recommended for future experimental verification.

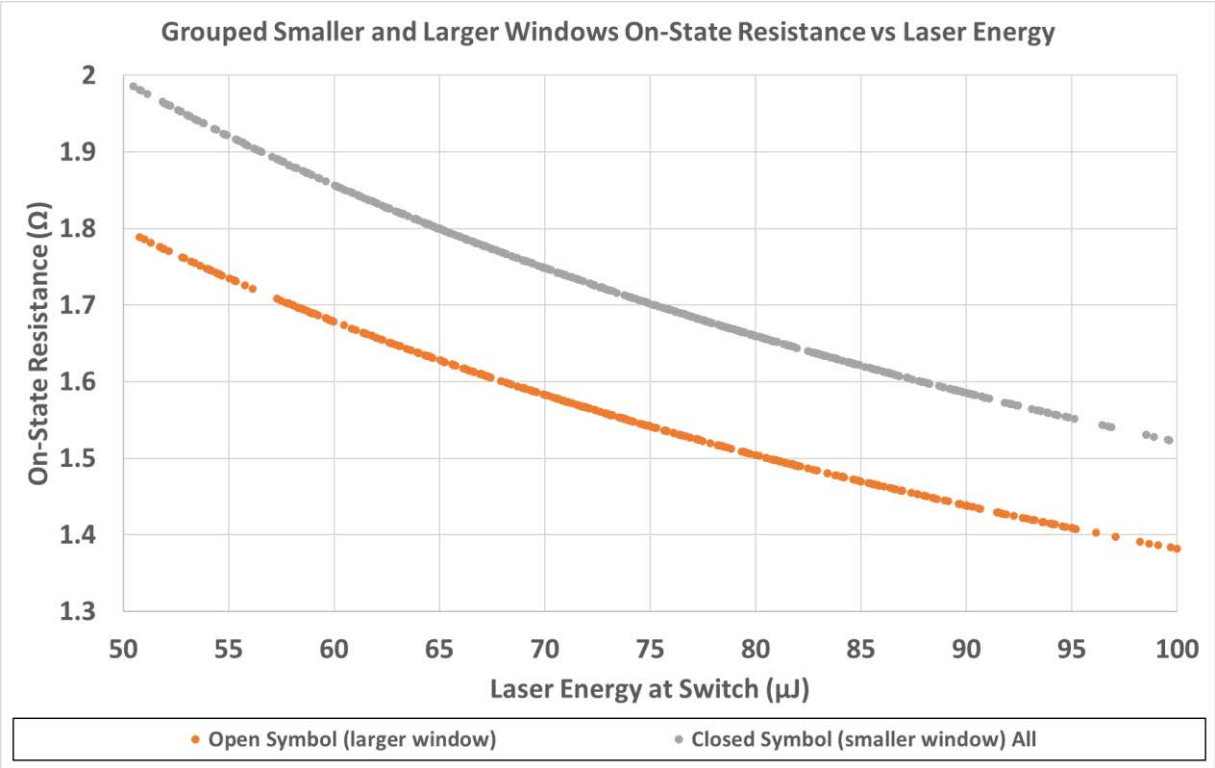


Figure 3.4.2. On-state resistance vs laser energy with Si-PCSS grouped into 100 μm and greater window spacings and less than 100 μm window spacings. An over-estimated laser energy reduction of 22% can be seen at fixed on-state resistances which also contains contributions from device variability.

3.5 GaN:C PCSS Direct RF Modulation

(Heather Thompson)

3.5.1 Problem Statement, Approach, and Context

Primary Problem: Need for a more compact, cost-effective RF pulse generation system for Navy afloat missions on smaller vessels and vehicles.

Solution Space: Improve efficiency and reduce necessary material, size, and thermal requirements by utilizing gallium nitride (GaN) in PCSSs through exploitation of its theoretical material properties which allow for higher operating voltages, frequencies, and temperatures, while also eliminating the need for pulse-shaping transmission lines through direct RF modulation using the laser/photon source driving the PCSS.

Sub-Problem: Lack of maturity in compensated gallium nitride semiconductor (i.e., GaN:X with X=C,Fe) PCSS manufacturing, development, and optimization.

State-of-the-Art (SOTA): Si-based PCSS with >10 kV operational voltage, cooling system capacity of 500 W/cm^2, and theoretical breakdown of 1.3 MW/cm.

Deficiency in the SOTA: Si-based technologies requiring ~100 μJ optical pulses per 4 MW of RF output power, increasing the laser energy (per pulse) required for device triggering; long recovery time (ones-of-μs), limiting quick opening and high pulse-repetition-rate operation along with increased heating in the PCSS; critical electric field of 0.3 MV/cm, leading to devices that are ones-of-cm^2 in area for the target peak power; and operating temperature of <160°C, leading to increased cooling requirements.

Solution Proposed: Replace Si-PCSS device with GaN:C utilizing direct RF modulation — eliminating the need for a bulky pulse-forming transmission line (~3 ft long) — capable of handling >3 MW (peak power) with ~20 μJ of incident optical energy, device area <1 cm^2, and operating temperature ~500°C (theoretical temperature which will be limited by circuit components and solder).

Relevance to OSPRES Grant Objective: Reduction in size and cost for cooling system that prevents damage to the PCSS device and components along with eliminating need for a bulky pulse-shaping system, as well as decrease in material cost and needed incident laser energy, leading to enhanced SWaP-C^2 capability with greater modularity and scalability.

Risks, Payoffs, and Challenges: Due to manufacturing limitations, GaN PCSS devices tend to be limited to lateral geometries (both contacts on the top side of the device), limiting operating voltage due to current crowding and surface flashover. The recovery time (ones-to-tens-of-ns) may lead to device heating and increased DC, or zero-frequency, component when generating RF with a period on the same order as the recovery time.

3.5.2 Tasks and Milestones / Timeline / Status

(A) **Jan-April 2021** Demonstrate RF unipolar modulation in the 1–2 GHz regime and up to 2 kV operating voltage with current PCB setup and automated optical delay system. Achieving 2 kV operating voltage should allow for preliminary effects testing before (or in conjunction with) striving towards higher operating voltages. **Ongoing**

(B) **Start April 2021** Demonstrate RF bipolar modulation using an advanced test setup with two GaN:C PCSSs triggered using the same optical delay, but with the second device connected to a negative power supply.

(C) **Start April 2021** Achieve higher center frequency content in unipolar and bipolar modulation by using a faster (rise-time and pulse-width) laser to activate GaN:C PCSS.

(D) **Start May 2021** Complete study of recovery for differing gap lengths, incident energies, and operating voltages and find solutions to reduce the recovery time.

(E) **March-June 2021** Complete study on the feasibility of using mode-coupling to bring the laser light into GaN:C devices allowing for a possible reduction of laser energy, and pulse shaping within the laser-coupler/GaN:C composite structure.

3.5.3 Progress Made Since Last Report

(A) The 1000 μm device has been vacuum cured using Sylgard and is ready for testing.

(B) A PCB was fabricated for bipolar modulation.

(E) A study of mode-coupling has been initiated in COMSOL with a model of coupling between two cylindrical and two slab waveguides being built. Initial studies revealed the mode coupling effect between the two waveguides. Within each waveguide however we still observe higher-order modes perhaps due to mesh effects or mismatched boundary conditions.

3.5.4 Significant Finding(s) and Mission Impact

3.5.4.1 Summary to Date

(A) Towards showing direct RF modulation in the 1–2 GHz range, unipolar modulation has been demonstrated using an open-space time-optical delay using one GaN:C PCSS (lateral device with 500 μm gap length) of up to 1.2 kV charge voltage. The limiting factor to achieving higher charge voltage was flashover occurring in air-bubbles formed during curing of the Sylgard encapsulant. Previously, ~1.8 kV charge voltage was achieved using a 1 μm gap length GaN:C PCSS, so demonstration will continue using the wider gap length to achieve 2 kV+ charge voltage, with this being limited by the power supply being used to 2.5 kV.

3.5.4.2 Since Last Report

(A) For March, demonstrating high-voltage (2 kV) unipolar modulation was delayed, but the 1000 μm device, mentioned in last month's report, has been vacuum cured using Sylgard, and is ready for testing.

(B) The PCB necessary to show bipolar modulation has been fabricated and is ready for testing as well.

(E) To show the feasibility of using optical fiber coupling with GaN:C PCSS for the reduction of needed incident laser energy and direct RF modulation through incident pulse modulation, simulations were built using COMSOL. For an initial study we wish to show how the coupling between two waveguides changes as a function of the distance between the two guides (separated by an air gap). The results show single-mode energy coupling back and forth between the two waveguides. Yet challenges still occur in achieving purely single-mode results (in slab or cylindrical geometries). Collaboration with COMSOL technical support is being utilized to remedy the presence of additional modes to refine the results, so that they can be more accurately analyzed.

3.6 Drift-Step Recovery Diode and Pulse Shaping Device Optimization

(Jay Eifler)

3.6.1 Problem Statement, Approach, and Context

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS but do not require a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times require optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening device within the pulse shaping head circuit. Additional goals for PRF/BRF are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies. Also optimize the pulse sharpening device (PSD) within the pulse shaping head circuit.

Sub-Problem 1: TCAD and SPICE models of the DSRD are 40% accurate and must be improved. PSD models have not been developed.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetime have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current. PSD have sharpened DSRD pulses to 100 ps-order.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power, minimum risetime but also for low-jitter, reduced cooling, and compactness. Additionally, optimize pulser with PSD and pulse shaping head circuit.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2·cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities. DSRD and PSD must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD and PSD modeling.

3.6.2 Tasks and Milestones / Timeline / Status

(A) Develop accurate models for DSRD (TCAD and SPICE models are 40% accurate)

(A1) Develop accurate DSRD TCAD models / JAN-APR 2021 / TCAD models have been replicated in new TCAD scripts but must be compared to experimental data and improved as necessary. Need to develop and test dynamic breakdown model in TCAD.

(A2) Develop accurate SPICE models / MAR-JUN 2021 / DSRD SPICE model research has not begun outside of partly converting MOSFET model to TCAD spice. DSRD SPICE models on the SPICE side already in use have been studied.

(A3) Develop parasitic capacitance, inductance, and resistance models for single die and stacked DSRD. / MAR-JUN 2021 / Parasitic model research has not begun.

(B) Explore TCAD modeling to advance DSRD research using available DSRD models

(B1) Study carrier lifetime effect on risetime / FEB-APR 2021 / No directly attributable effect of lifetime on risetime was found. Future more systematic studies including DSRD and circuit topology parameters will include lifetime and show its effect on performance.

(B2) Avalanche and device operation study / FEB-MAY 2021 / Avalanche models limit peak power and risetime but do not correspond to experiment and must not be included or included and improved and calibrated to experiment.

(B3) Study effect of the width of outer edge contact on current density and breakdown in device. / MAR-MAY 2021 / No research begun.

(B4) Begin TCAD process modeling in Silvaco Athena and Victory Process of diffused and epitaxial processes for DSRD (and pulse sharpening device) fabrication and DSRD device modeling. / MAR-JUNE 2021 / P-side implantation and diffusion process steps

modeled in process TCAD and further DSRD fabrication steps under study in TCAD process.

(C) Pulse sharpening device (PSD) modeling

(C1) Begin TCAD modeling of PSD / DEC 2020 and APR-JUN 2020 / (a) Preliminary PSD research begun replicating published work but further work to continue. (b) More standard PSD device modeled in TCAD than as used in published work. (c) PSD simulated with DSRD 3-stack for more complete DSRD-based system modeling excluding only the primary switch model.

(C2) Determine current carrying capacity of PSD and stacks / MAR-JUN 2021 / PSD literature review begun. Current carrying capacity relates to area optimization of PSD.

(D) Receive and study DSRD-based pulser circuit topologies in SPICE with the DSRD and primary switch SPICE models. / MAR-APR / LTSPICE code and models received and understood.

3.6.3 Progress Made Since Last Report

(B1) Literature states the DSRD with short lifetimes can be operated without a forward pump current but operated with constant current pumping. Use of constant current pumping allows for different pulser designs. This has not been verified in TCAD.

(B2) TCAD simulations were performed for SPT spreading resistance profile measured doping profile, Gaussian (received from Nick Flippin), error function (received from Ron Focia), and TCAD process generated (process steps received from Alex Usenko) doping profiles without including avalanche modeling to estimate peak voltage and risetime more in accord with experiment. Avalanche models need to be calibrated for dynamic breakdown (approximately twice) and compared and modified as necessary to available experimental pulse data. Calibration (by model and/or data) should allow for optimization of the area with realistic peak power and risetime. The error function doping profile had the fastest risetime.

(B4) Modeled tentative SPT p-side doping implantation and diffusion steps for DSRD in TCAD process and modeled the device operation using this profile in the TCAD device simulator. N-side protocol still missing. Began TCAD process modeling of epitaxial designs but lacking enough information yet to complete simulation.

(C1) (b) As in the literature, a standard PSD (rather than previous non-standard PSD) was studied in TCAD for its device pulse sharpening capability. (c) The PSD was also studied using TCAD within a DSRD-based pulser circuit including a 3-stacked DSRD. Both results showed sharpened risetimes as reported in literature.

(D) Several circuit topologies are used for the DSRD-based pulsers. DSRD device designs historically in the lab have been optimized in TCAD using two circuit topologies and DSRD-based systems built and tested for a couple other designs. A few other topologies have been collected from the literature. Additional circuit topologies can be used in TCAD optimization of the DSRD and/or PSD and produce consistency between the different modeling methods. SPICE simulations using the various circuit topologies have been tested in LTSPICE.

3.6.4 Significant Finding(s) and Mission Impact

3.6.4.1 Summary to Date

Last month, DSRD TCAD simulation started by replicating published TCAD DSRD results and then simulating devices similar with actual in-house DSRD. The variation of the sinewave pulse voltage input magnitude and period on DSRD output and variations in DSRD carrier lifetime on DSRD output were collected. Charge storage timing (when the diode empties charge stored from forward pulsing) of ~50% was achievable with sufficiently long voltage input period which is necessary for maximum reverse current. And lifetime had no significant effect on risetime. DSRD stacks were simulated showing reduced risetime from single die to 5-stacked DSRD consistent with published and earlier in-house data. Series resistance to model metal resistance between DSRD in stacks and doping variability in stacks was also modeled in TCAD showing metal resistance must be large to have an impact on peak voltage and risetime and doping variations proportionally effect risetime. Work on DSRD SPICE models has been done for the primary switch model with conversion of the code for TCAD SPICE being partly completed to allow for modeling the complete DSRD-based pulser system.

DSRD peak voltage and risetime were simulated in TCAD to include avalanche modeling or not. TCAD avalanche models limited peak voltage and risetime at the load over a range of voltage input magnitudes. The default avalanche TCAD models are not accurate and limited DSRD peak voltage and risetime to less than seen in experimental pulse data. A TCAD parameter study for voltage input magnitude and DSRD area for several doping profiles without avalanche modeling are being performed. The avalanche model and model parameters are also being modified to account for dynamic breakdown rather than static and then will be compared to the no avalanche case and experimental data. From the improved avalanche modeling and TCAD parameter study, the optimal area of the DSRD can be obtained.

TCAD process and device modeling for the development of process steps and their resultant doping profiles and device operation has begun. This modeling will enable a connection between the fabrication parameters and the device operation for DSRD (and PSD). Pulse sharpening has been verified for PSD devices for the standard design and another non-conventional design. The PSD was also modeled within a DSRD-based pulser circuit combining for the first time TCAD modeling of both DSRD and PSD together within the same circuit with only the primary switch model not included.

3.6.4.2 Since Last Report

(B2) TCAD simulations without avalanche models set were performed for SPT SRP, Gaussian, error function and TCAD process-generated doping profiles. The avalanche models are not accurate and were not included to operate at voltages as in experiment. The voltage input was a sinewave pulse of 100 V magnitude and 200 ns period.

For the Gaussian profile (P^+ doping concentration of 1×10^{19} dopant atoms/cm^3 with 125 µm depth, N^+ doping concentration of 1×10^{19} dopant atoms/cm^3 with 40 µm depth, and p^- base doping concentration of 1×10^{14} dopant atoms/cm^3 with 35 µm width) both 0.7 cm^2 and 0.33 cm^2 areas were tested. The peak voltage and risetime are improved with smaller

area. For 0.7 cm^2 area, the reverse current maximum was 119 A (170 A/cm^2), peak voltage 1914 V, risetime of 2.44 ns. For the 0.33 cm^2 area, reverse current maximum of 115 A (348 A/cm^2), peak voltage 2332 V, and risetime 1.78 ns. Improved avalanche models and experimental pulse data can set the limits for area and realistic peak power and risetimes for DSRD.

The SPT SRP doping profile used an area of 0.33 cm^2 and had a peak voltage of 688 V and risetime of 3.24 ns. The P^+-doping depth in the SRP does not achieve the depth desired and the p^- base is much wider than intended and results in the poorer performance.

The optimized error function doping profile, using a 0.33 cm^2 area, had a peak voltage of 2461 V and a risetime of 1.64 ns. This was the highest peak voltage and fastest risetime DSRD doping profile.

The TCAD process-generated diffused DSRD doping profile did not have correct DSRD operation and had a p^- base region of ~1×15 dopant atoms/cm^3. The correct process protocol will correct the doping for good DSRD operation.

Plots of the dv/dt for SRP, Gaussian and Error function doping profiles are shown in Figure 3.6.1. Both the Gaussian and error function doping profiles have a greater than 1×10^{12} V/s dynamic voltage riserate on the DSRD for ~ 2 ns which is during the risetime of the voltage across the DSRD and load. This may be within the limits of the non-avalanche requirement for DSRD operation. Further development of the breakdown TCAD models to change the parameter from static to dynamic settings and in accordance with experimental DSRD pulse data will allow the TCAD breakdown model to be predictive of the optimal area of a device with a particular doping profile, voltage operation, and thickness, and stacking of DSRD devices.

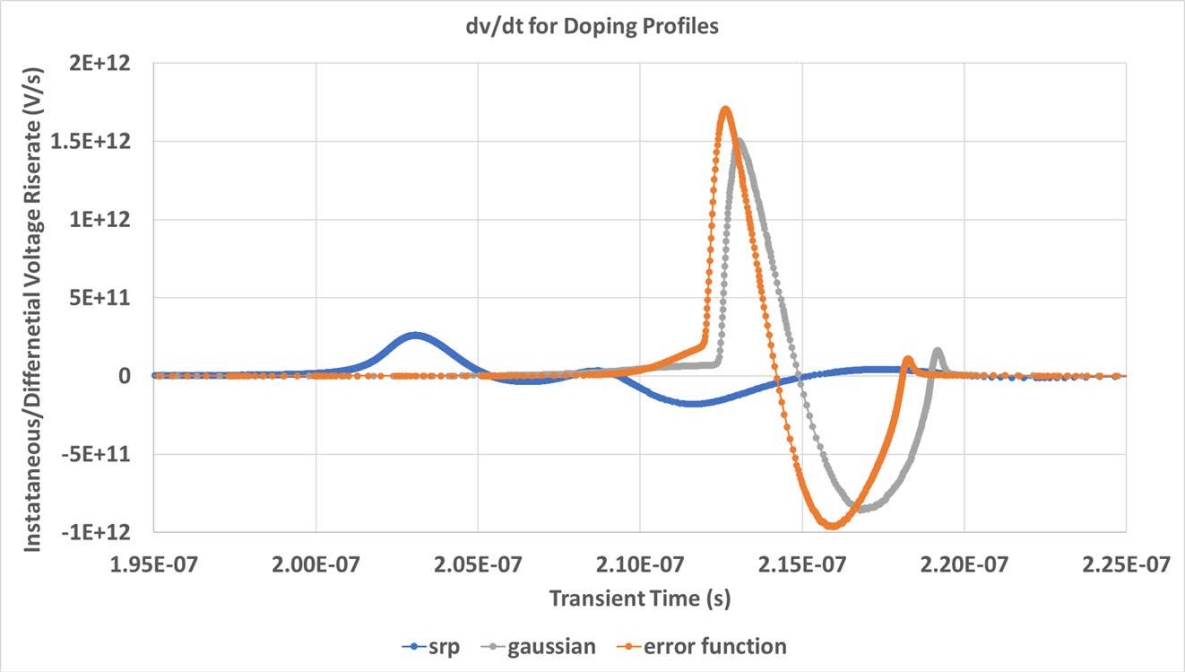


Figure 3.6.1. dv/dt vs transient simulation time for spreading resistance profile (SRP), Gaussian, and error function type doping profiles. Both SRP and Gaussian doping profiles show greater than 1×10^{12} V/s riserate for about 2 ns across the DSRD close to the margin for dynamic breakdown.

(B4) Some beginning exchange of process fabrication steps and details for the diffused and epitaxial DSRD has begun. The diffused DSRD fabrication steps were completed in the TCAD process software Silvaco Athena. The process steps modeled included: starting wafer parameters (crystal orientation, type and concentration of initial wafer doping), p-side boron implantation (energy, dose), nitride deposition (thickness), boron drive-in (temperature, time), removal or etching of nitride layer, n-side aluminum implantation, nitride deposition, aluminum drive-in, etch nitride. The process steps were not included for n-side. Steps for n-side predeposition and drive-in, oxidation steps, photoresist, metallization have yet to be well specified but are in planning.

The TCAD process modeling was used to generate a 1-D doping profile for simulation in the TCAD device simulator, Silvaco ATLAS, for DSRD operation. The profile had a p^- base with too high a doping concentration which can be corrected with improved process steps. The device operation did not show DSRD operation. Epitaxial process steps have also been exchanged and modeling begun. TCAD process modeling of the diffused and epitaxial process steps can be improved. The modeling of aluminum dopants and higher diffusion temperatures also pose a challenge and custom process parameters may be necessary. Figure 3.6.2 shows the doping profile from the TCAD process simulation, where the net doping profile is shown in green.

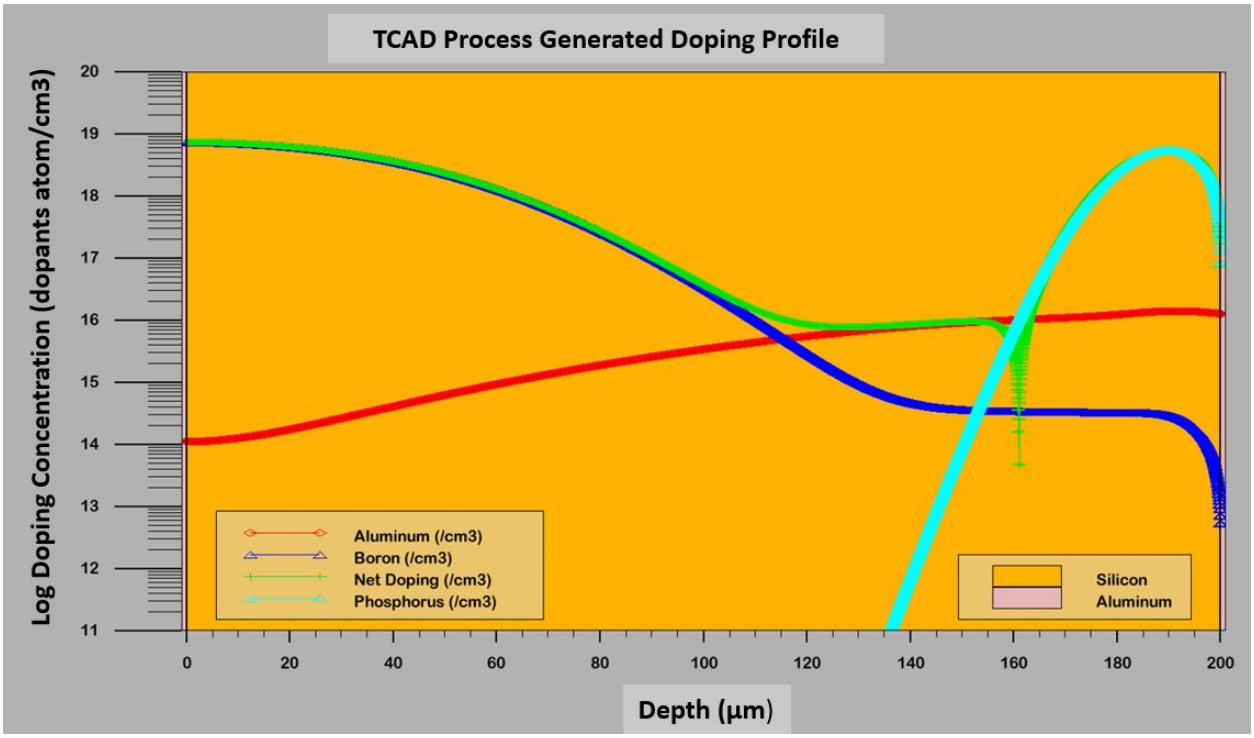


Figure 3.6.2. TCAD process generated doping profile following initial SPT p-side doping protocol for DSRD.

(C1a) Published work on a PSD device was replicated. A PSD device was simulated in TCAD for a circuit consisting of a PSD device in series between a voltage source and a 50 Ω load. The voltage source was modeled as a ns-order high voltage input pulse with a sinusoidal function (14 kV peak voltage, 2 ns half period). Figure 3.6.3 shows the input pulse and sharpened output pulse for a 520 µm thick, 4 mm^2 area PSD device. The published PSD device relies on a fast ionization mode different than the standard PSD devices. Electric fields from the PSD TCAD structures showed a uniform field developed across the low-doped n^- base before avalanche. Displacement current was also seen in the TCAD structures and can be used in the analysis of PSD device operation. A 10% to 90% risetime is taken between the load peak voltage and the knee of the pre-pulse (prepulse-peak risetime). The prepulse-peak risetime was 80 ps (7.8×10^{13} V/s). A number of delayed breakdown devices exist in the literature relying on varying modes of fast ionization.

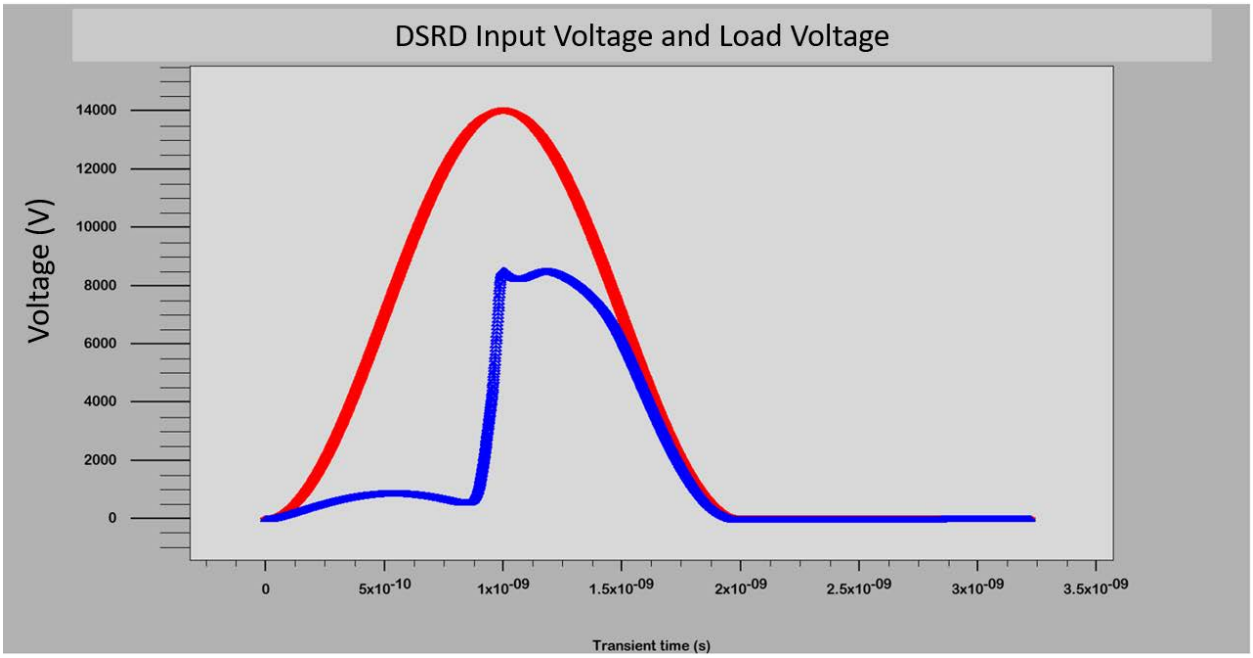


Figure 3.6.3. Input voltage to final PSD compression stage (red) and load voltage (blue) are overlayed vs transient simulation time.

(C1b) The more standard published model of PSD devices uses a 200 μm thick device with an area of 2 mm^2 area and a more highly doped 100 μm thick n^- base and deeply diffused junctions. In Figure 3.6.4 is shown the 3000 V, 2 ns half-period sinewave pulse voltage input (red), voltage across PSD device (green), and load output (blue). The resulting risetime is 175 ps, over a voltage rise of 1676 V (9.6×10^{12} V/s riserate). Such a device can be readily manufactured, tested, simulated in TCAD and/or SPICE, stacked and compared to COTS high voltage diodes often substituted for PSD devices.

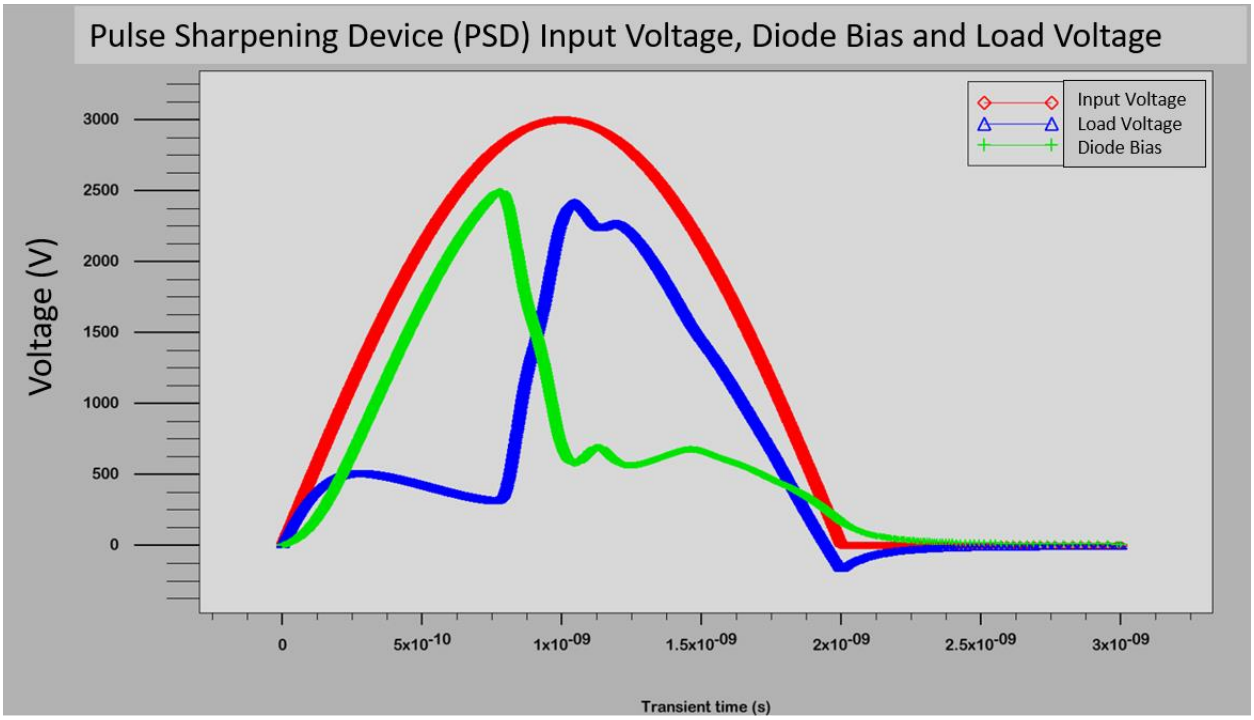
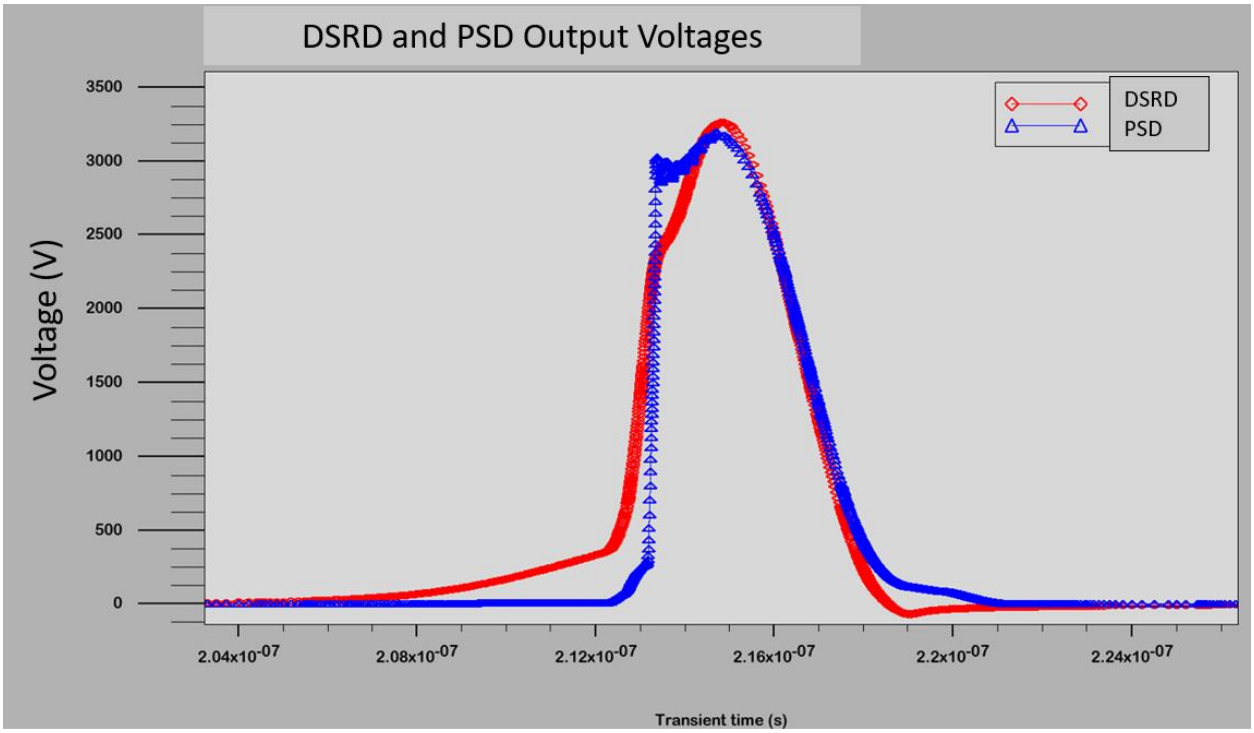


Figure 3.6.4. PSD input voltage (red) modeled in TCAD as 2 ns half sinewave pulse input with voltage across PSD (diode bias, green) and output load voltage (blue).

(C2c) The standard PSD device was added to a 3-stack DSRD-based pulser which was driven with a sinewave pulse input indicative of the output from the primary switch stage of the pulser. The PSD device was within the circuit of the pulse shaping head and was the final pulse compression stage. Figure 3.6.5 shows the voltage waveforms overlayed for the 3-stacked DSRD output to the PSD stage, and the PSD output at a 50 Ω load. The DSRD output has a risetime of 2.24 ns and the PSD of 177 ps. By adding modeling of the primary switch, a complete model of the DSRD-based pulse-sharpened system can be modeled. TCAD modeling can then be used to model the DSRD-based pulser and aid in the development of DSRD and PSD spice models using TCAD, Utmost and SmartSpice. Using TCAD process modeling the fabrication parameters can be connected to the complete operation of the DSRD-based pulser system with sharpening.



3.6.5. TCAD simulation of DSRD and PSD pulse compression stages showing the sharpened risetime. The voltage across the DSRD (red) serves as input to the PSD within the final pulse sharpening head or pulse compression stage. The load output after pulse sharpening is shown in blue.

4.0 Prime Power and Conditioning

4.1 HV Switch Pulsed Chargers

(Wasekul Azad and Faisal Khan)

4.1.1 Problem Statement, Approach, and Context

Primary Problem: Commercially available high-voltage solid-state switches made by BEHLKE are the best in SWaP-cooling, but are expensive, have long lead times (2–3 months), and are made outside of the US. For the Navy afloat mission to be successful, we need a sustainable supply of US-manufactured switches at a much lower cost.

Solution Space: Design and demonstrate modular high-voltage (~10 kV) and fast (repetition frequency = 100 kHz) solid-state switches using a combination of series- and parallel-connected commercially available inexpensive discrete MOSFETs and custom high-voltage (~10 kV) isolated gate drivers.

Sub-Problem: Voltage balancing among the series-connected MOSFETs, minimization of gate signal delays, cooling of the individual MOSFETs, balancing resistors, high-voltage isolation required for the power supplies, and the controlling pulse width modulated (PWM) signal as well as differential voltage feedback measurement across individual MOSFETs.

State-of-the-Art (SOTA): Direct liquid-cooled solid-state switch from BEHLKE (e.g., HTS-151-30).

Deficiency in the SOTA:

1. BEHLKE-made switches are expensive. For instance, a single HTS-151-30 switch costs around $5,000.
2. BEHLKE switches along with direct liquid cooling units occupy a considerable amount of space. For instance, an HTS-151-30 switch from BEHLKE has a footprint of approximately 225*85*75 mm without considering the liquid cooling system. Some key parameters of this switch are as follows.

   i) Maximum operating voltage = 15 kV

   ii) Maximum continuous load current = 2.52 A (without cooling), 30 A (with liquid cooling)

   iii) Maximum turn-ON peak current = 300 A (pulse width = 200 µs, duty cycle <1%)

   iv) Turn-ON resistance = 1.3 Ω
3. Once the switching frequency is greater than 10 kHz, a liquid cooling system is required to operate the BEHLKE switch.
4. Without liquid cooling, the maximum continuous power dissipation (P_{cont}) of the BEHLKE switch is limited (e.g., for HTS-151-30, P_{cont} is 10 W without liquid cooling).
5. At a higher switching frequency (>20 kHz), the BEHLKE switch requires multiple ancillary DC power supplies, i.e., 5, 15, and 60 V.

6. The switches made by BEHLKE cannot be reconfigured to withstand a higher voltage exceeding their recommended rating. BEHLKE offers separate products to operate them at higher voltage/currents.

Solution Proposed: Designing a modular high-voltage (~10 kV) switch using a single custom isolated gate driver for each module and having a construction cost lower than the BEHLKE switch with equivalent or better performance in all specification categories (Specifications for the BEHLKE switches can be found in the following link: http://www.behlke.com/separations/separation_c4.htm).

Relevance to OSPRES Grant Objective: The proposed modular high-voltage switch is expected to facilitate controlled hundreds-of-nanosecond charging of an array of transmission lines of pulse forming networks to drive an array of PCSSs, thereby producing controlled hundreds-of-picosecond scale high-voltage pulses.

Risks, Payoffs, and Challenges:

I. Lack of rigid control over voltage balancing can lead to a cascaded failure among the series-connected MOSFETs.

II. In the absence of an adequate mitigation scheme, voltage overshoot due to the fast switching speed can exceed the voltage rating of an individual MOSFET, thereby damaging the switch.

III. At high voltage (~10 kV) and high repetition rate (>100 kHz), mitigating EMI to safeguard the individual MOSFETs from false turn-ON is a major challenge.

4.1.2 Tasks and Milestones / Timeline / Status

(A) Design a surface-mount MOSFET-based four-stage switch (6.8 kV rated) and control it using the in-house gate driver, then test its voltage-withstanding ability with a DC supply voltage up to 4–5 kV and evaluate the effectiveness of the thermal management at its current state / DEC 2020 / Completed.

(B) Design and develop a modular HV switch (~10 kV rated) using the concept of the tested four-stage high-voltage switch module and an in-house modular gate driver to drive the modular switch /JAN–FEB 2021 / Completed.

(C)

(i) Test the voltage withstanding ability of the modular HV switch with a DC supply voltage up to 10 kV and switching frequency up to 50 kHz using a resistive load (5–10 kΩ) and evaluate the effectiveness of the thermal management at its current state / FEB–April 2021 / Ongoing.

(ii) Test the isolation capability and evaluate the synchronization accuracy of the gate drive signal generated from the modular in-house gate driver / FEB–April 2021 / Ongoing.

(iii) Encapsulate the gate driver board with potting material with a high (~15–20 kV) breakdown voltage rating to prevent possible flashover/arcing in between the HV switch and this board / MAR–APR 2021 / Ongoing.

(D) Test this modular HV switch coupled with a Si PCSS device up to a DC supply voltage of 5–6 kV and a switching frequency of 50 kHz / MAR–MAY 2021 / On hold until milestone (C) is completed.

(E) Design and fabricate a compact power conditioner circuit based on a 12 kV rated SiC switch made by BEHLKE (HTS 121-15) / March 2021 / **NEW**.

(F)

(i) Design and develop a 20 kV rated modular (two modules, each with four MOSFETs) HV switch based on the design concept of the 10 kV rated modular switch using 3.3 kV rated SiC MOSFETs (new product made by GeneSiC Semi) / APR–MAY 2021 / On hold until milestone (C) is completed.

(ii) Design and develop a 20 kV rated modular gate driver based on a WPT based planar transformer topology to ensure adequate galvanic isolation (~30–40 kV) for the power supplies of the gate driver APR–MAY 2021 / On hold until milestone (C) is completed..

4.1.3 Progress Made Since Last Report

(B)

Wrote and submitted a paper based on the design of the in-house modular HV switch in IEEE Kansas Power and Energy Conference 2021, and the paper is accepted for lecture presentation.

(C)

(ii) The gate driver started malfunctioning at a voltage level close to 5.6 kV. We are investigating the root cause of this issue. One of the probable reasons is the floating ground at the control/input side of the gate driver.

(iii) Potting material has been applied to coat the exposed pads in the PCB of the HV switch to insulate the interface between the HV switch and the gate driver and prevent potential flashover.

(E) Designed and fabricated a compact (165 × 85 mm) power conditioner circuit based on the switch made by BEHLKE.

4.1.4 Significant Finding(s) and Mission Impact

4.1.4.1 Summary to Date

(A) The 6.8 kV rated four-stage surface-mount MOSFET developed in-house was successfully tested up to a DC supply voltage of 4 kV and at a switching frequency up to 20 kHz with a 3.2 kΩ resistive load.

(B) A modular (two modules) 10 kV rated HV switch has been designed and a prototype has been developed using 1.7 kV rated SMD MOSFETs (C2M1000170J). An in-house 10 kV rated HV gate driver has been designed and incorporated with the HV switch to drive it.

(C) The HV switch has been tested using a supply voltage up to 5.6 kV at an operating frequency of 15 kHz.

4.1.4.2 Since Last Report

(C) At a DC supply voltage around 5.6 kV, we observed arcing on the HV switch board that led to gate driver malfunctioning. One of the potential reasons causing the arcing might be insufficient creepage/clearance between exposed conducting surfaces. Conformal coating can be applied to mitigate the aforementioned issue to some extent. Therefore, a conformal coating (419D from MG Chemicals) with a dielectric strength of 1000 V/mil was applied to the exposed pads in the HV switchboard to provide additional insulation to safeguard against potential flashover. However, at a voltage level close to 5.6 kV, the gate driver starts to malfunction. We are assuming the primary reason behind the malfunction is the floating ground at the input/control side of the gate driver Integrated Circuit (IC) ISO5852S. When the HV switch turns ON, all the source terminal potentials of the series connected MOSFETs, thereby the output ground potentials of two gate driver ICs are pulled up to the level of the supply voltage in high-side configuration. The input ground potentials of the gate driver ICs may not proportionally increase, thereby leading to a voltage difference between the grounds of the gate driver IC that exceeds the maximum voltage withstanding capability (5.7 kV) of the driver IC. Connecting a large resistor (tens to hundreds of MΩ) with sufficient voltage rating in between the input and output grounds of the gate driver IC can be a potential solution. Another potential solution under consideration is connecting a capacitor (in the range of picofarads) in between the grounds of the gate driver IC. The troubleshooting related to the in-house gate driver design will allow us to design a 10 kV HV switch module that can be potentially scaled up to higher voltage levels. We will furnish the results pertaining to the HV gate driver after further troubleshooting in the next monthly report.

(E) A compact (165 × 85mm) power conditioner circuit featuring a 12 kV rated SiC MOSFET made by BEHLKE has been designed and fabricated.

5.0 Tradespace Analysis of Ultra-Wide-Band Antenna Arrays

5.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

5.1.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wide-band antenna elements in a phased array for high-power microwave (HPM) transmissions.

Deficiency in SOTA: Large physical aperture size.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters via a D/Q (directivity/quality) factor technique, followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area.

Relevance to OSPRES Grant Objective: Provides design and optimization (in terms of directivity or gain and bandwidth) guidelines for ultra-wideband ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN – MAY 2021 / Code complete. Ongoing literature search for filing Invention Disclosure form.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN – MAY 2021 / Ongoing.

(C) Build minimum viable validation prototypes on substrates that have good power handling capabilities for HPM transmissions at UHF range (such as polyethylene, FR-4, TMM-10i, TMM-6) / JAN – MAY 2021 / Completed modeling, manufacturing, and

preliminary testing of antennas designed on TMM-10i, TMM-6, and G10/FR-4 substrates; ongoing investigations into antennas based on polyethylene substrates.

(D) Complete time-domain analysis of the antennas subjected to input short pulses / FEB – MAY 2021 / Ongoing.

5.1.3 Progress Made Since Last Report

(B) Investigations into aperture area reduction:

a. A method for characterizing large microstrip patch antenna array structures ($\geq 15 \times 15$) on finite grounded substrates is being investigated to reduce computation time and memory usage.

(C) Building minimum viable validation prototypes:

a. Three coaxial probe-fed microstrip patch antennas have been designed, manufactured, and tested (S_{11}-parameter/VSWR and gain). Note: Voltage Standing Wave Ratio or $VSWR = \frac{1+|S_{11}|}{1-|S_{11}|}$.

b. Preparing manuscript for IEEE AP-S Magazine based on bandwidth enhancement and optimization techniques of probe-fed wideband electrically small microstrip patch antenna elements.

(D) Time-domain analysis of the antennas:

a. Time-domain analysis of the coaxial probe-fed rectangular microstrip patch antenna designed on TMM-10i substrate has been initiated via CST simulations.

b. Time domain electric field response, at different distances from the antenna, when subjected to a Gaussian input pulse have been studied.

c. Short input pulses will be considered next.

5.1.4 Significant Finding(s) and Mission Impact

5.1.4.1 Summary to Date

(C) Building minimum viable validation prototypes:

One of the ways to reduce the overall array aperture area is to use electrically small antenna (ESA) elements. Although coaxial probe-fed microstrip patch antenna is a popular choice for designing ESAs, it has the inherent drawback of low impedance bandwidth (<10%).

To enhance the bandwidth of microstrip ESAs, two design approaches have been considered. First, a novel method to increase the bandwidth (>=30%) has been proposed, by strategically placing the coaxial probe along 2/3rd the patch diagonal. Second, by introducing U-slots on microstrip patches.

To validate the design approaches, two simple rectangular patch antennas (using the proposed bandwidth enhancement technique) on TMM-6 and TMM-10i substrates and a U-slot patch antenna on G10/FR-4 substrate have been manufactured and tested.

5.1.4.2 Since Last Report

(C) Building minimum viable validation prototypes:

To validate our design approach, three ESA elements have been designed, manufactured, and tested on various substrates. The manufactured antennas and their corresponding operating frequency range are enlisted in Table 5.1.1.

Table 5.1.1. Antenna Designs

Antenna	Antenna Type	Substrate used	Radiating Aperture Area $L \times W$ (mm^2)	Frequency Range (GHz)
#1	Coaxial probe-fed rectangular microstrip patch on circular shaped ground	TMM-10i ($\varepsilon_r = 9.8, \tan\delta = 0.002, h = 6.35$ mm)	$9.61 \times 14.42 = 138.5762$	2.5 – 5.0
#2	Coaxial probe-fed rectangular microstrip patch on circular shaped ground	TMM-6 ($\varepsilon_r = 6, \tan\delta = 0.0023, h = 6.35$ mm)	$12.77 \times 19.155 = 244.6094$	2.5 – 4.5
#3	Coaxial probe-fed U-slot microstrip patch on square shaped ground	G10/FR-4 ($\varepsilon_r = 5.2, \tan\delta = 0.025, h = 17.78$ mm)	$45.0139 \times 62.23 = 2801.2$	0.9 – 1.3

The manufactured prototypes are shown below, along with their measured and simulated VSWR and gain data.

Antenna #1:

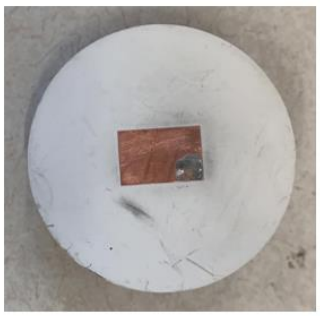


Fig. 5.1.1. Fabricated prototype – coaxial probe-fed simple microstrip patch antenna on circular shaped TMM-10i substrate (Antenna #1).

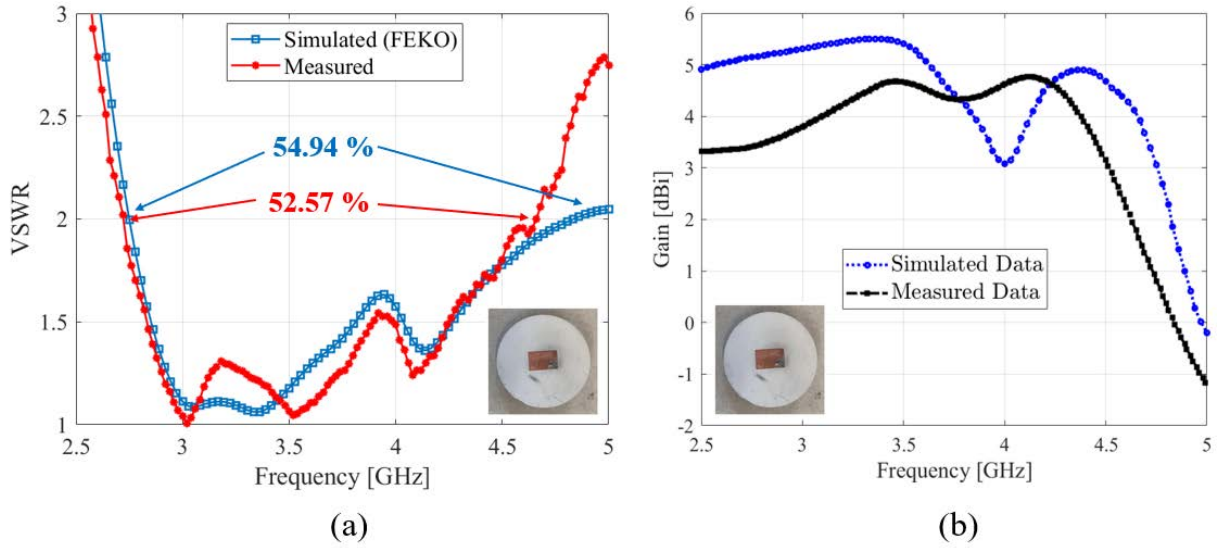


Fig. 5.1.2. Simulated and measured (a) VSWR and (b) gain of coaxial probe-fed simple microstrip patch antenna on circular shaped TMM-10i substrate (Antenna #1).

Antenna #2:

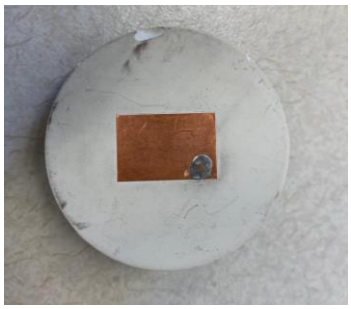


Fig. 5.1.3. Fabricated prototype – coaxial probe-fed simple microstrip patch antenna on circular shaped TMM-6 substrate (Antenna #2).

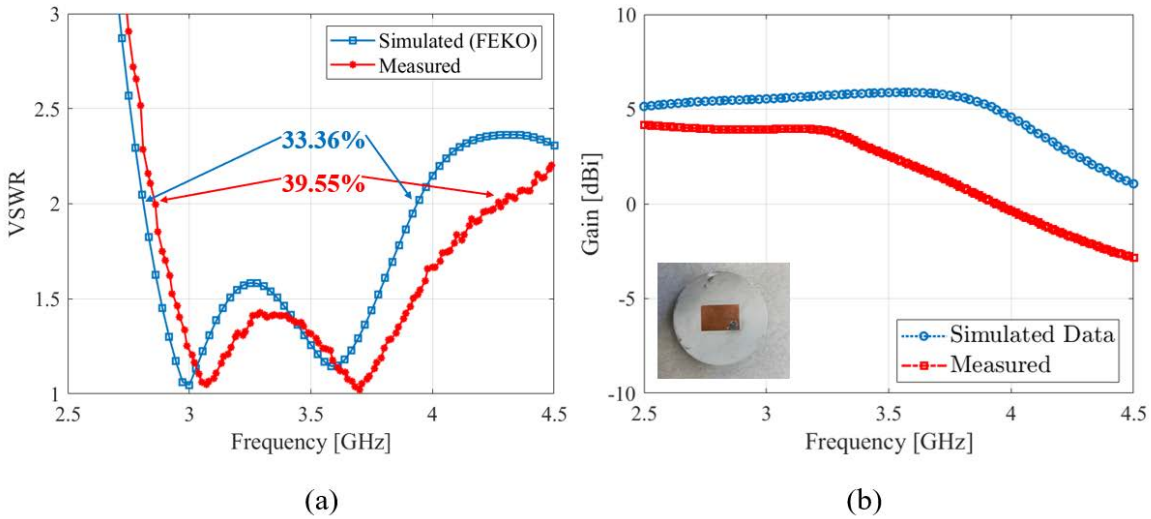


Fig. 5.1.4. Simulated and measured (a) VSWR and (b) gain of the coaxial probe-fed simple microstrip patch antenna on circular shaped TMM-6 substrate (Antenna #2).

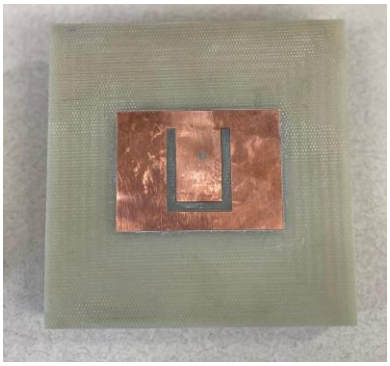


Fig. 5.1.5. Fabricated prototype – coaxial probe-fed U-slot microstrip patch antenna on square shaped G10/FR-4 substrate (Antenna #3).

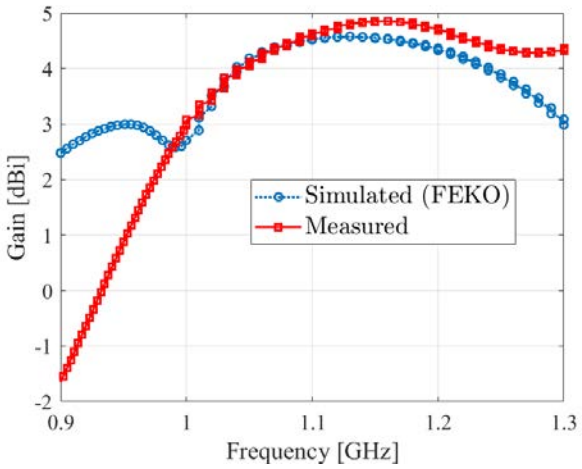


Fig. 5.1.6. Simulated and measured gain of the coaxial probe-fed U-slot patch antenna on square shaped G10/FR-4 substrate (Antenna #3).

Excellent agreement between the measured and the simulated VSWR results have been obtained for the simple patch antennas designed on TMM-10i (Antenna #1) and TMM-6 (Antenna #2) substrates.

Antenna gain testing was performed in the absence of a perfect anechoic chamber. Hence, the measured gain data, in both the cases, shows some discrepancies with the simulated data, owing to severe multi-path reflections from nearby metal objects.

Comparison between the measured and the simulated VSWR of Antenna #3, designed on G10/FR-4 substrate, will be provided in the next report after analysis.

(D) Time-domain analysis of the antennas:

Time-domain analysis of the coaxial probe-fed simple patch antenna, designed on TMM-10i substrate (Antenna #1), when subjected to input Gaussian pulse is investigated via CST simulations. The preliminary results are illustrated in Fig. 5.1.8.

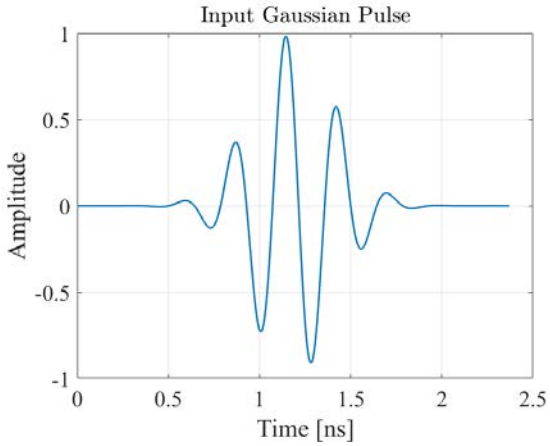


Fig. 5.1.7. Input Gaussian pulse.

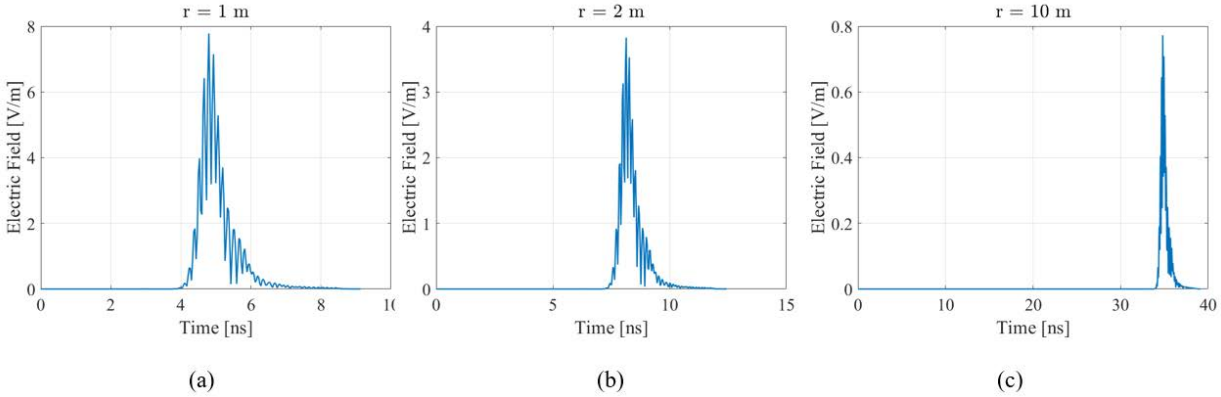


Fig. 5.1.8. Time-domain electric field of Antenna #1 (coaxial probe-fed simple rectangular microstrip patch antenna on TMM-10i substrate) when subjected to the input Gaussian pulse of Fig. 5.1.7 at a distance of (a) 1 m, (b) 2 m, and (c) 10 m from the antenna.

5.2 Tradespace Analysis of Other Ultra-Wide-Band (UWB) Single Elements

(Kalyan Durbhakula)

5.2.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining

performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelev antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem: The total surface currents on the Koshelev antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not clearly understood yet.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelev antenna that effectively reduce its physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelev antenna has been shown in the literature to withstand higher voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelev antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelev antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelev antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelev antenna.

(iii) The large electrical size (>5λ) of the Koshelev antenna at its highest operating frequency poses huge computational challenges. Efforts are underway to cleverly select important design parameters for the tradespace study.

5.2.2 Tasks and Milestones / Timeline / Status

(A) Complete literature search to identify and list antenna elements that satisfy UWB properties and HPM requirements, and down select accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelev antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB–MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design and show minimal to no variation in the bandwidth and gain with increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t,\phi,\theta)$) in receive or transmit mode.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelev antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size / Complete.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / MAR21/ Complete.

- Milestone: Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain over the desired bandwidth, and aperture efficiency / Complete.

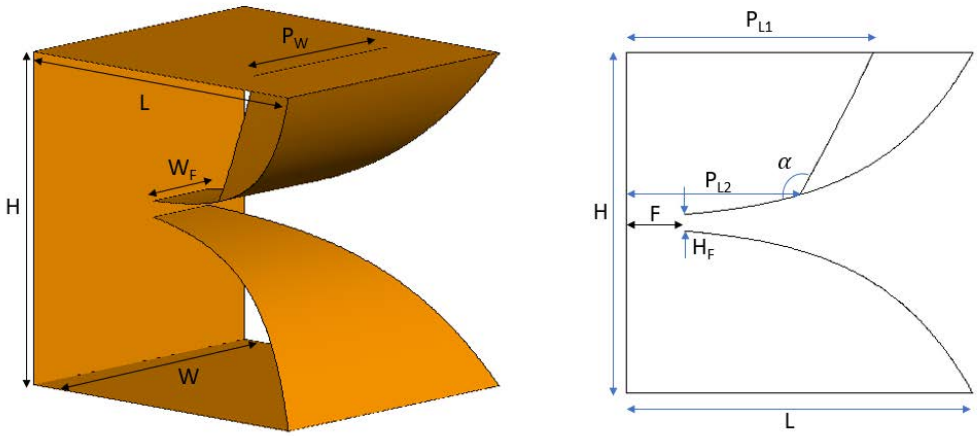
(F) Reduce Koshelev antenna aperture size (H×W) equal to or less than 90 mm × 90 mm for direct antenna metrics comparison against SOTA BAVA, which has an aperture size equal to 90 mm × 90 mm / MAR-APR21 **(NEW)** / Ongoing.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, and aperture efficiency equal to or greater than 130% at 900 MHz.
- Milestone: Build an array model using the optimized design parameters.

(G) Continue with the literature search and improving our understanding on special electromagnetic (EM) techniques to determine their applicability to the antennas under consideration. The special EM techniques include: inductive loading, dielectric embedding, dielectric loading, electromagnetic bandgap structure, resistive terminations, beveling and creating slots, defected ground structures, iterative projection method, dielectric/metamaterial lens, array lattice configuration (square vs rectangular vs triangular vs hexagonal vs sunflower, etc.), subarray overlapping, E-plane and H-plane array, and subarray placements. / JAN–APR21 / Ongoing.

5.2.3 Progress Made Since Last Report

(E) In the FEB 2021 MSR, an initial tradespace study on the width (*W*) design parameter was reported and we had shown a significant reduction in aperture area (by almost 50%) without losing significant bandwidth or gain. Over the last month, we continued with studying other design parameters of the Koshelev antenna. The other design parameters are length (*L*), feed position (*F*) and angle alpha (*α*), which are all shown in Fig. 5.2.1.



(a) (b)

Fig. 5.2.1. Koshelev antenna with design parameters. (a) 3D view, and (b) side view.

(F) We worked on a new task to reduce the aperture size from 208 mm × 190 mm (optimized aperture size reported in last MSR) towards a goal of 90 mm × 90 mm. Several parametric studies have been carried out to achieve the antenna metrics reported in the tasks and milestone section.

5.2.4 Significant Finding(s) and Mission Impact

5.2.4.1 Summary to Date

(A) An extensive literature search on various UWB antenna elements has resulted in finding three promising antenna elements. The down selected antenna elements are the Koshelev, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the single antenna element. Later, the single antenna element will be converted into a planar array.

(B) Initial validation of the Koshelev antenna simulated using CST software agreed well with the antenna metrics published in the open literature [1]. A UWB bandwidth response (10:1 bandwidth) and rE/V > 1 has been observed from our initial simulations of the Koshelev antenna. This validation ensured that the Koshelev antenna can be subjected to further tradespace studies to understand its performance followed by optimizing the design according to OSPRES grant requirements.

(C) The initial tradespace study and analysis of the Koshelev antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between the Koshelev antenna in [1] and aperture reduced Koshelev antenna are shown in Table 5.2.1. From Table 5.2.1, it is evident that the physical aperture area has been reduced by 50% (from 0.08 to 0.04 m^2) with a minimal and potentially acceptable tradeoff in bandwidth (200-MHz in 4.5-GHz) and peak gain (from 9.4 to 7.7 dBi). In addition, by reducing the physical aperture area (from 0.08 to 0.04 m^2), the aperture efficiency (80 to 100%) and rE/V (1.25 to 1.6) have improved. The 95% aperture area reduction milestone has been met successfully as demonstrated in Tale 5.2.1 i.e., 50% aperture area reduction can be seen from Koshelev [1] and Koshelev proposed 3.

Other antenna metrics such as peak and average power handling capability, electronic beam steering capability, effective radiated power (ERP), Q-factor, power spectral density, fidelity factor, and energy density will be added gradually in future MSRs.

Table 5.2.1. Antenna metrics (Green – Improvement, Red – Decline)

Antenna element type		Koshelev [1] & JAN MSR	Koshelev Proposed 1	Koshelev Proposed 2	Koshelev Proposed 3
Dimensions (mm) (L×H×W)		300 × 268 × 293	300 × 268 × 245	300 × 240 × 219	300 × 208 ×190
Physical Aperture area (m^2)		0.0785	0.0659	0.0527	0.0395
Bandwidth		10:1 f_L = 0.5 GHz, f_U = 5 GHz	8.33:1 f_L = 0.6 GHz, f_U = 5 GHz	7.69:1 f_L = 0.65 GHz, f_U = 5 GHz	7.14:1 f_L = 0.7 GHz, f_U = 5 GHz
Peak gain (dBi) (1 GHz)		9.4	9.06	8.41	7.69
Half-Power Beamwidth (HPBW) at 1 GHz	E-plane	51°	59°	66.7°	71.9°
	H-plane	53°	59°	64°	64.7°
Aperture Efficiency (1 GHz)		80%	87.40%	94.04%	100%
rE/V at 10 meters		1.25	1.35	1.49	1.6
FWHM (ps)		302	329	331	338
Ringing (ps) ($T_{ringing}$ = 0.1)		277	405	407	362

(D) An in-house code has been developed to calculate important UWB time domain antenna metrics such as full-width half maximum (FWHM) and ringing. FWHM and ringing antenna metrics have been calculated using in-house MATLAB code using the excitation voltage and radiated electric field information obtained from CST simulations. FWHM and ringing antenna metrics help with assessing or characterizing an antenna's UWB

response. In short, a FWHM and ringing values less than 200 ps is preferred for an UWB antenna to effectively and accurately radiate input short rise-time input pulse. The last two rows in Table 5.4.1 show the FWHM and ringing values obtained using in-house code for the original [1] and aperture area reduced Koshelev antenna.

5.2.4.2 Since Last Report

(E)

- A tradespace study has been performed on the length (*L*), feed position (*F*) and angle alpha (α) design parameters of the Koshelev antenna. Fig. 5.2.2 (a) shows the S11 response over a range of frequencies for different lengths of the antenna. The length of the Koshelev antenna corresponds to the propagation direction of the EM field and therefore plays a significant role in determining the bandwidth. Fig. 5.2.2. (a) shows the full frequency response and zoomed in frequency response of S11. The longer the Koshelev antenna's length, the higher the bandwidth. Moreover, the bandwidth improvement can be seen at the lower end of the frequency spectrum, which can be clearly seen from the zoomed in frequency response (0.1 GHz to 0.7 GHz) in Fig. 5.2.2 (a). Similar response from gain can be observed in Fig. 5.2.2 (b), which shows clear advantage of longer length Koshelev antenna.

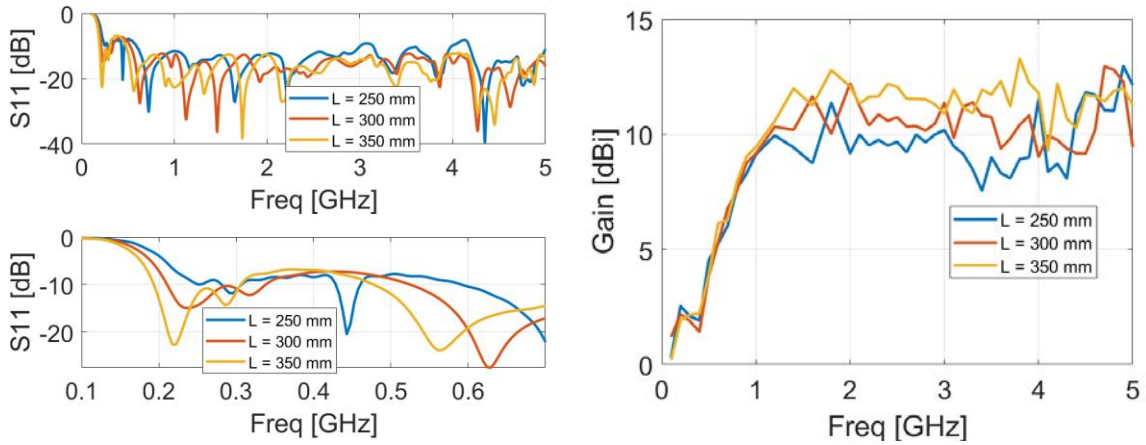
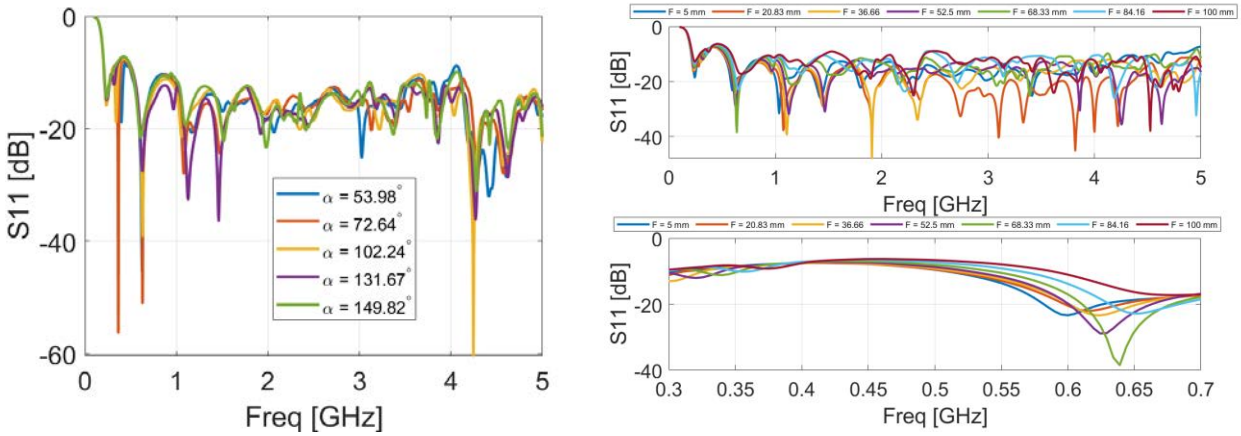


Fig. 5.2.2. (a) Reflection coefficient (S11) in dB and (b) Gain in dBi for four different width (W) values.

- Once an understanding of the length (*L*) design parameter of the Koshelev antenna has been established, we performed a tradespace study on angle alpha (α) and feed position (*F*). Fig. 5.2.3 (a) shows S11 over a range of frequencies for different alpha (α) values. An onset of $\alpha = 90°$ implies that the center adjusting plate is perpendicular to the top exponential profile. An $\alpha < 90°$ implies the center adjusting plate is leaning towards the reflector side of the antenna and $\alpha > 90°$ implies the center adjusting plate is leaning towards to the aperture side of the antenna. Fig.

5.2.3 (a) shows no significant difference with change in orientation of center adjusting plate with respect to top exponential profile. However, based on keen observation of S11 in Fig. 5.2.3 (a), it is helpful to choose an alpha (α) value greater than 90°, i.e., the center adjusting plate leaning towards the aperture side. In addition to angle alpha, the feed position (F) has also been studied. A change in feed position implies an effective reduction in the length of exponential profiles since the overall length (L) is kept constant for this case. Fig. 5.2.3 (b) also shows a full frequency range and zoomed in frequency range of S11 for different feed positions (F). A feed position closer to the back reflector is desired since that provides longer propagation path for the currents. However, a feed position too close to the back reflector could excite unintended or perturb intended currents on the back reflector. A feed position (F) between 5 mm and 20 mm (F = 1/20 < L < 1/10) can be chosen to achieve an optimum bandwidth.



(a) (b)

Fig. 5.2.3. Reflection coefficient (S11) in dB vs frequency for (a) different alpha (α) angles, and (b) different feed positions (F).

(F) A new effort has been undertaken in MAR21 to match the aperture size of the Koshelev antenna to 90 mm × 90 mm and to achieve a good S11 response (< –10 dB) at 900 MHz with a bandwidth of 200 MHz on both sides of 900 MHz. Based on the observations from the initial tradespace study of the Koshelev antenna, the antenna aperture size and other design parameters have been adjusted to come close to the required aperture size (90 mm × 90 mm). Based on the BAVA metrics information obtained from the source development team at UMKC and based on the adjusted aperture size of the Koshelev antenna, a comparison between the SOTA BAVA and the Koshelev antenna has been drawn and is shown in Table 5.2.2. The aperture size, aperture area and operating frequency range from Table 5.2.2 shows almost the same quantities from both antennas. The significant advantage of the Koshelev antenna over the SOTA BAVA can be noticed from the peak gain and aperture efficiency rows in Table 5.2.2. The Koshelev antenna outperforms the BAVA. Other metric comparison such as half-power beamwidth (HPBW), rE/V, side lobe levels, FWHM and ringing will be included in the next MSR once a BAVA CAD model is developed and simulated. More optimization

and adjustments can be made to the Koshelev antenna to further improve its performance.

Table 5.2.2. Antenna metrics comparison at 900 MHz between SOTA BAVA and Koshelev antenna.

Antenna element type		SOTA BAVA (single element)	Koshelov (single element)
Aperture size (H×W)		90 mm × 90 mm	93 mm × 85 mm
Physical Aperture area		0.0081 m^2	0.0076 m^2
Operating frequency range (fc±BW)		900 MHz ± 200 MHz	900 MHz ± 180 MHz
Peak gain (900 MHz)		3 dBi	4 dBi
HPBW at 900 MHz	E-plane	Unknown	83°
	H-plane	Unknown	83°
Aperture Efficiency (900 MHz)		217%	303%
Side lobe levels		Unknown	-2.5 dB
rE/V at 10 meters		Unknown	1.39
FWHM		Unknown	330 ps
Ringing ($T_{ringing}$ = 0.1)		Unknown	320 ps

5.2.5 References

[1] Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

5.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna

(Sadie Brasel and Kalyan Durbhakula)

5.3.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of Shark antenna elements whose miniaturization in two dimensions (height and width equal to $\lambda/4$ where λ corresponds to the lowest operating frequency) make it a good candidate for UWB HPM systems while having a reduced aperture area with respect to the current state-of-the-art. In the literature, the Shark antenna has already been shown to achieve a wide 20:1 impedance bandwidth, low dispersion, and a sectoral (also referred to as directional) radiation pattern.

Sub-Problem: The design parameter space of the Shark antenna has not been studied rigorously in the literature and therefore the effect of these parameters on the antenna metrics is not understood. In addition, the Shark antenna has been shown to be not very directive in the H-Plane. Preliminary studies have shown that aperture efficiencies at low frequencies are much better than at higher frequencies.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Explore the design parameter space for the Shark antenna element using computational electromagnetic (EM) wave solvers starting with the simulation and validation of a single element.

Relevance to OSPRES Grant Objective: The Shark antenna dimensions were established to be frequency dependent and can be readily modulated to fit the spectrum characteristics of an ultra-fast rise time input pulse.

Risks, Payoffs and Challenges:

(i) The Shark antenna is comprised of flare-angle-dependent bicones that are truncated in the azimuthal angle. This still yields considerably higher half power beam width (HPBW) than other antenna elements under investigation. The significant reduction of HPBW in the H-plane may be unattainable and can be considered a major risk.

(ii) Payoffs include the development of a library of antenna metrics data for various shapes and sizes of the bicones and reflector plates in the shark antenna.

(iii) Computational challenges remain present with respect to automation of design parameter space on our currently used supercomputer (LEWIS). Design challenges persist in obtaining lower operating frequencies while not increasing the height of the antenna and surpassing the 90 mm × 90 mm size requirement.

5.3.2 Tasks and Milestones / Timeline / Status

(A) Complete initial design, simulation, and validation of the Shark antenna / JAN21 / Complete.

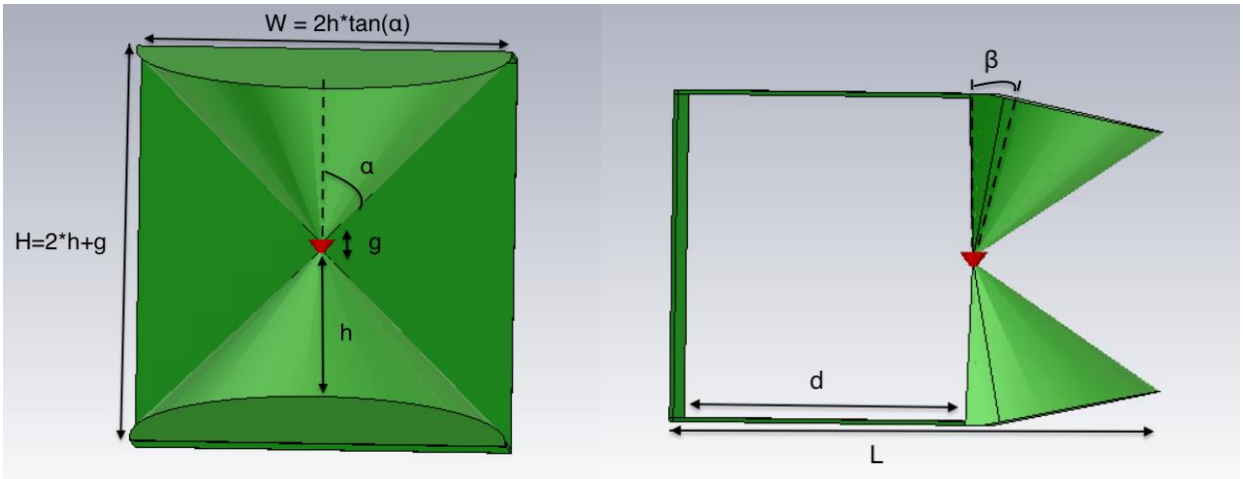
(B) Validate Shark antenna design using the LEWIS supercomputer over a wider range of frequency results (up to 20 GHz) / FEB–MAR21 / Complete.

(C) Identify Shark antenna design parameters which contribute significantly to bandwidth, gain, and physical aperture area. Determine which parameters contribute most to performance improvement/size reduction. Flare angle (α), cone height (h), and distance to backplane (d) are initial parameters of interest / FEB–MAR21 / Complete.

(D) Perform a preliminary tradespace study by simulating the Shark antenna with the extreme cases of flare angle, cone length, and distance to backplane. Gain a general understanding of how these parameters affect impedance bandwidth, rE/V, gain and HPBW / FEB21 / Complete.

(E) Perform a detailed tradespace study by simulating the Shark antenna with several cases of varying flare angle, cone length, and distance to backplane.

- Milestone: produce a detailed summary of change in impedance bandwidth, rE/V, HPBW in H-plane and E-plane as a function of flare angle (α), cone height (h), and distance to backplane (d) / FEB–APR21 / Ongoing.



(a) (b)

Figure 5.3.1. Shark antenna design parameters: *d, h, g*, α, β

5.3.3 Progress Made Since Last Report

(E) A detailed tradespace study for the Shark antenna is underway. To begin, we are focusing on the h = 40 mm and h = 45 mm cases. The goal is to obtain a lowest operating frequency of 700 MHz while staying within a 90 mm × 90 mm aperture area.

5.3.4 Significant Finding(s) and Mission Impact

5.3.4.1 Summary to Date

(A) The Shark antenna has been designed, simulated, and validated according to [1]. (Figure 5.3.1)

(B) Using the LEWIS supercomputer, the original Shark antenna design was simulated up to 20 GHz. The S11 result of this simulation was below –10 dB from the starting cutoff frequency up to 20 GHz as in [1].

(C) The Shark antenna design parameters which we have found to contribute significantly to bandwidth performance, directivity, and gain are the cone height (*h*) and distance to backplane (*d*).

(D) The preliminary Shark antenna study has been completed and has provided insight into the Shark antenna design space. Increasing the cone height *h* yields better impedance bandwidth at low frequencies and is more directive in the *e* and *h* planes. However, increasing *h* results in a larger aperture area.

5.3.4.2 Since Last Report

(E) To explore the tradeoff between height and low-frequency performance, which was discovered through the preliminary Shark antenna study in (D), the detailed parametric study this month focused on the *h* = 40 and 45 mm cases. These cases will be within the 90 × 90 mm requirement. Based on the results shown in Figure 5.3.2, the α = 40° and 50° cases do not perform as well at low frequencies and will therefore not be included in the parametric study moving forward. The goal of this work is to try and obtain a lowest –10 dB crossing frequency of 700 MHz. From Figure 5.3.3 it can be seen that increasing *d* from 75 to 100 mm does not help decrease the lowest –10 dB crossing frequency. The continuation of the parametric study will reveal if this relationship holds for several *h* values.

From Table 5.3.1 it can be seen that increasing *h* from 40 to 45 mm shifts the lowest –10 dB crossing frequency down. To further shift this frequency down to 700 MHz, other parameters will need to be changed and tested. From the previous study in (D), we expect increasing *d* and decreasing α should help obtain desired results. The cases which will be tested moving forward are listed in Table 5.3.3.

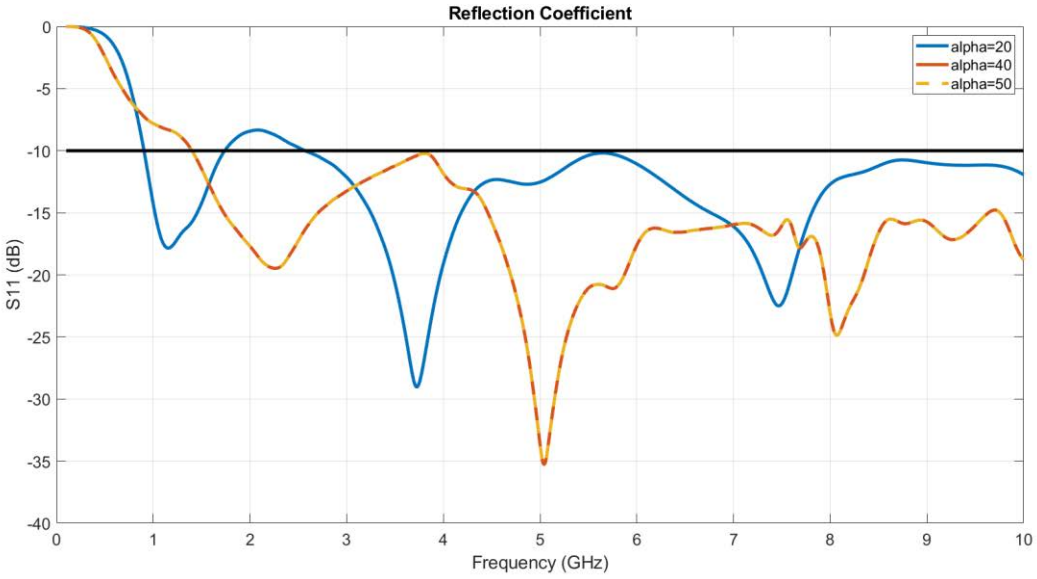


Figure 5.3.2. S11: *d* = 75 mm, *h* = 40 mm.

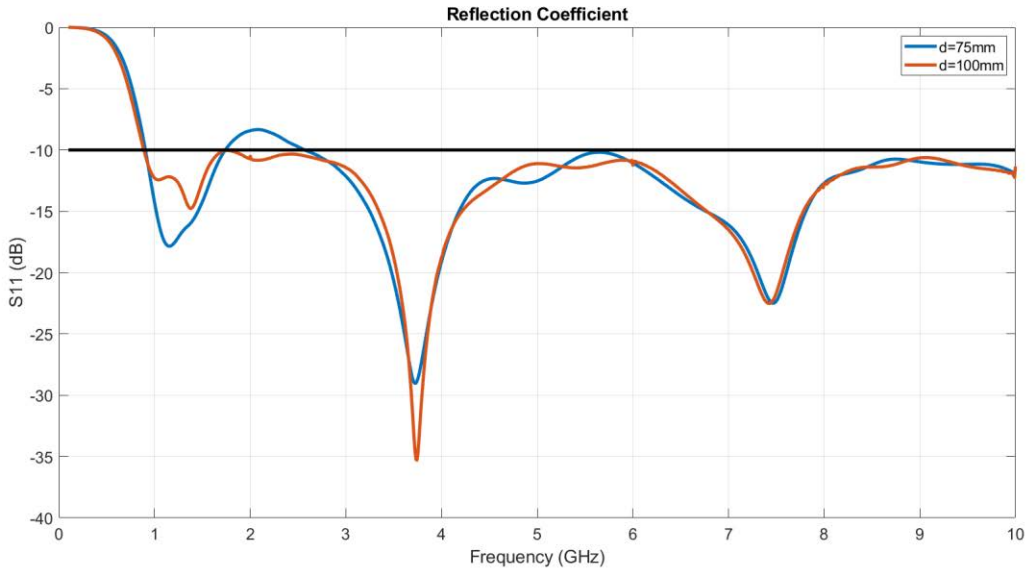


Figure 5.3.3. S11: $\alpha = 20°$, *h* = 40 mm.

Table 5.3.1. Shark antenna parametric study results

h *(mm)*	*d* *(mm)*	Flare Angle	Frequency Dependent Dimensions (W,H,L) $\lambda = \frac{c}{900e6}$	Physical Aperture Area $A_{phs} = W * H$	Bandwidth	Lowest –10 dB Crossing Frequency	Peak Gain (900 MHz)	HPBW (900 MHz)		Aperture Efficiency (%) (900 MHz)
								E-plane	H-plane	
40	75	20°	$\frac{\lambda}{4.1}, \frac{\lambda}{11.5}, \frac{\lambda}{3.4}$	30 mm X 82 mm	11:1	900 MHz	2.73 dBi	124.1°	312.6°	670%
45	75	20°	$\frac{\lambda}{3.6}, \frac{\lambda}{10.2}, \frac{\lambda}{3.3}$	32 mm X 92 mm	12.5:1	815 MHz	2.72 dBi	119.6°	331.2°	560%

Table 5.3.2. Detailed Shark antenna parametric study rE/V results

	rE/V	
h (mm)	r = 1 m	r = 2 m
40	0.73377447	0.36683953
45	0.93177559	0.45321458

Table 5.3.3. Detailed Shark antenna parametric cases to be run

h (mm)	Flare angle (α)		*d* (mm)	Feed gap (g) (mm)	β	Wire radius (mm)
40	20	15	75	2	12	0.3
45	20	15				
40	20	15	100			
45	20	15				

5.3.5 References:

[1] L. Desrumaux, A. Godard, M. Lalande, V. Bertrand, J. Andrieu and B. Jecko, "An Original Antenna for Transient High Power UWB Arrays: The Shark Antenna," in IEEE Transactions on Antennas and Propagation, vol. 58, no. 8, pp. 2515- 2522, Aug. 2010, doi: 10.1109/TAP.2010.2050418.

5.4 Tradespace Analysis of Ultra-Wide-Band (UWB) Fractal Antenna

(Sai Indharapu and Kalyan Durbhakula)

5.4.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. The fractal antenna packs multiple resonances closely spaced together to generate an UWB response, thereby effectively utilizing the 2D space (i.e., the radiating patch space). Its high degree of freedom provides an opportunity to develop systematically modified patch shapes which in turn leads to improved bandwidth while retaining high fidelity factor values.

Sub-Problem: Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

5.4.2 Tasks and Milestones / Timeline / Status

(A) Perform tradespace analysis of the fractal element radius *b* over the desired frequency range (4 GHz to 12 GHz) using the genetic algorithm (GA) optimization tool available in the commercial electromagnetic (EM) solver FEKO / FEB21 / Complete.

- Milestone: Provide a recommendation of an optimum value of *b* using OPTFEKO to minimize reflection coefficient or S11 (< –10 dB) / Complete.

(B) Perform tradespace study on different fractal shapes by changing the number of fractal segments to understand the number of segment effect on the impedance bandwidth / FEB21 / Complete.

- Milestone: Produce a detailed study of the antenna response such as S11, gain, and bandwidth by varying the number fractal segments / Complete.

(C) Apply the GA optimization tool on the fractal side length *b* over a wide frequency range (2 GHz to 12 GHz with 201 discrete frequency points) and number of fractal segments using OPTFEKO on the LEWIS cluster / MAR21 / Complete.

- Milestone: Reduce physical aperture area by 10% of its present design, reported in the FEB MSR, and demonstrate minimal or no change in S11, gain, and fidelity factor values / Complete.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a* / MAR21 / Complete.

- Milestone: Recommend a reduced value of *a* to reduce the physical aperture area and increase aperture efficiency (>50%) with no variation in other antenna metrics / Complete.

(E) Demonstrate correlation between transmitted and radiated signals, by calculating fidelity factor using (1) where $S(t)$ and $r(t)$ are the transmitted and radiated signals, respectively. The goal is to achieve and maintain fidelity factor values equal to or greater than 0.9 / MAR21 / Ongoing.

$$F = max \left| \frac{\int S(t) r(t-r)\, dt}{\int S(t)^2 . \int r(t)^2 dt} \right| \quad (1)$$

(F) Frequency scale current fractal antenna design such that the center frequency of the resulting antenna equals 1.3 GHz **(NEW)** / APR21 / Ongoing.

- Milestone: Modify antenna design with a center frequency equal to 1.3 GHz and achieve similar results (3:1 bandwidth at fc = 1.3 GHz, 3 dBi gain and >130% aperture efficiency at 900 MHz) to antenna design at center frequency ~7 GHz / Ongoing.

5.4.3 Progress Made Since Last Report

(C) Optimization using GA on OPTFEKO

(C1) The GA optimization search for the fractal side length *b* over a wider frequency range i.e. (201 discrete frequency points) returned the value of *b* to be 1.368 mm.

(C2) The antenna response after adjusting the value of fractal side length *b* with a new value (=1.368 mm) was not satisfactory.

(D) Parametric study of hexagonal patch

(D1) OPTFEKO has been employed for finding the optimum value for the hexagon patch radius *a*.

(D2) The antenna design with hexagon radius *a* = 8 mm yielded satisfactory results with decreased physical aperture area.

(F) Initiated efforts to frequency scale current antenna design to a center frequency of 1.3 GHz.

(F1) The current antenna design is modified such that resulting antenna yields a bandwidth of 3:1.

5.4.4 Significant Finding(s) and Mission Impact

5.4.4.1 Summary to Date

(A) The initial analysis of the simulation results with fractal radius *b* equal to 1.8 yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO has been used as an optimization tool with fractal radius *b* as the optimization variable. The optimum value for *b* is found to be 1.66 mm. The optimization is carried out over 51 discrete frequency points.

(B) The addition of fractal elements (*N*) to the simple hexagon improved antenna metrics such as S11. To further investigate and understand the fractal elements, the number of segments in the fractal geometry has been varied. The improvement in bandwidth is observed as the value of *N* is increased from 6 to 14.

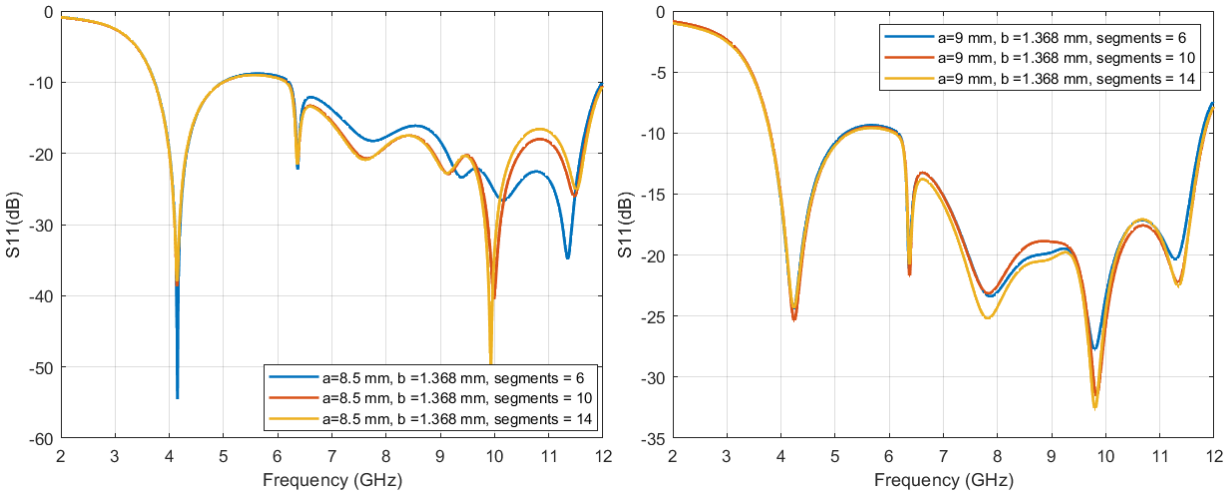
(C) The initial optimum value of *b* over 51 discrete frequency points is reported as 1.66 mm in task (A). To further increase the accuracy of the optimization algorithm and to find a more precise value for *b*, optimization is further performed over wider frequency points (201 discrete points between 2 GHz to 12 GHz).

(D) To further analyze *a*, OPTFEKO is employed to find the optimum value with the goal to decrease the physical aperture area, with the optimum value of *a* equals 8 mm antenna metrics such as S11, gain, and bandwidth are satisfactory as shown in the Table 5.4.1.

(F) The initial antenna design has been modified to achieve a center frequency of ~1.3 GHz. Antenna metrics such as gain and bandwidth have no variation to the initial design.

5.4.4.2 Since Last Report

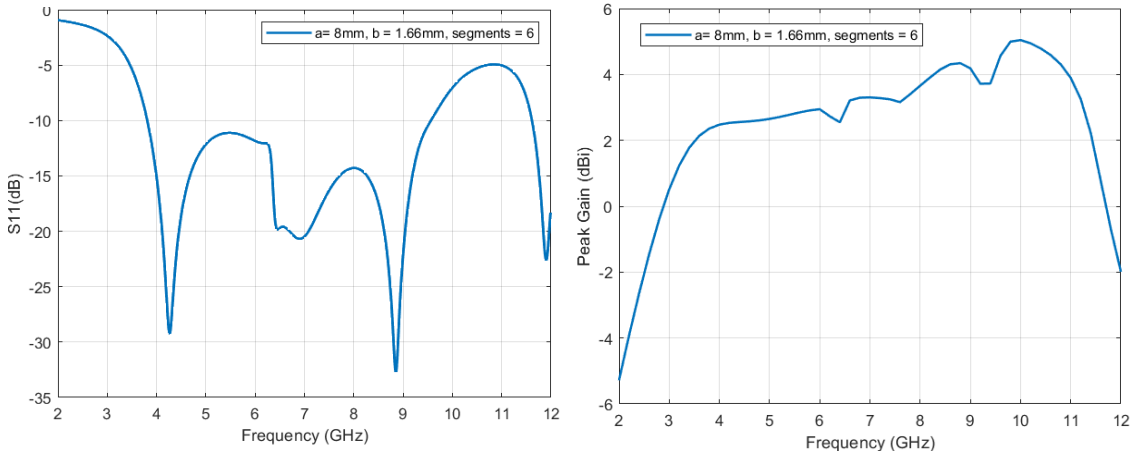
(C) The GA optimization of fractal side length *b* over a wider frequency range (2 GHz to 12 GHZ with 201 discrete frequency points) is found to be 1.368 mm. Upon changing the antenna design with the new *b* value, the antenna response was not satisfactory. The hexagon radius *a* and segments *N* have been varied to showcase the unsatisfactory performance from the new optimum *b* value and is displayed in Fig. 5.4.2. In Fig. 5.4.2, the unsatisfactory performance can be noticed between 5 GHz and 6 GHz where the S11 rises above –10 dB. Therefore, the actual value of *b* = 1.66 mm has been retained as the optimized value.



(a) (b)

Figure 5.4.2. Reflection coefficient of (a) antenna geometry with *a* = 8.5 mm and different *N* values, and (b) antenna geometry with *a* (=9 mm) and different *N* values.

(D) With the goal to decrease physical aperture area and to increase aperture efficiency, OPTFEKO has been employed to find the new optimum value for hexagon radius *a*. The antenna metrics such as S11 and gain are shown in Figure 5.4.3. The new value of *a* (= 8 mm) decreases the physical aperture area by 7% and increases the aperture efficiency by 29%. Other antenna metrics are shown in the third column of Table 5.4.1



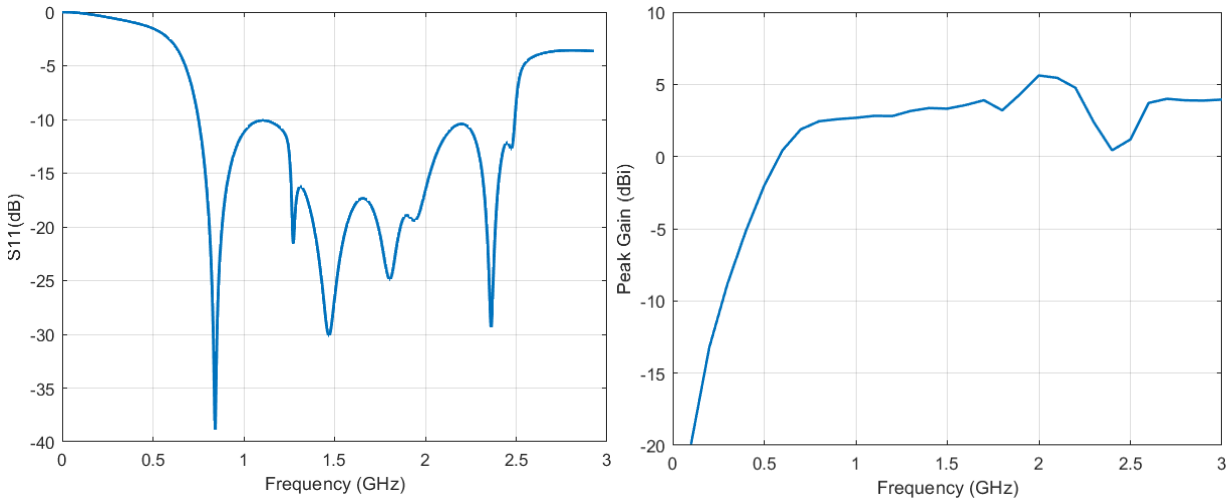
(a) (b)

Figure 5.4.3. (a) Reflection coefficient of antenna geometry with *a* = 8 mm, and (b) gain vs. frequency.

Table 5.4.1 Antenna metrics

Antenna element type		Original fractal antenna (a = 8.5 mm, *b* = 1.8 mm, N = 6 & fc = 6.65 GHz) [Reported in JAN MSR]	Optimized fractal antenna (a = 9 mm, *b* = 1.66 mm, N = 14 & fc = 7.8 GHz) [Reported in FEB MSR]	Optimized fractal antenna (a = 8 mm, *b* = 1.66 mm, N = 6 & fc = 7.8 GHz) [**NEW**]
Substrate Dimensions (mm)		25 × 25 × 1	25 × 25 × 1	25 × 25 × 1
Radiating Patch Dimensions (mm)		18.8 × 16.28	18.52 × 16.4	18.52 x 16
Physical Aperture area (mm^2)		0.306	0.303	0.296
Bandwidth		2.5:1 f_L = 3.8 GHz, f_U = 9.5 GHz	3:1 f_L = 4 GHz, f_U = 12 GHz	2.6:1 f_L = 3.8 GHz, f_U = 9.5 GHz
Peak gain (dBi) at f_C		3.56	3.98	3.24
Half-Power Beamwidth (HPBW)	E-plane (f_C)	69°	63.4°	71°
	H-plane (f_C)	71°	57.5°	80.4°
Aperture Efficiency (f_C)		120%	92%	115%
rE/V		0.6	0.6	0.7

(F) The current antenna design parameters are changed such that the resulting antenna metrics such as bandwidth and gain remain similar to those of the existing antenna model (third column of Table 5.4.1) . The antenna design is modified and the center frequency for the new antenna is ~1.3 GHz. The antenna response such as S11 and gain are shown in Figure 5.4.4, and other antenna metrics such as bandwidth, physical aperture area, and aperture efficiency are shown in the Table 5.4.2



(a) (b)

Figure 5.4.4. (a) Reflection coefficient of antenna geometry with *a* = 42.5 mm, *b* = 8.5 mm, *d* = 38 mm, and (b) gain vs. frequency.

Table 5.4.2. Antenna Metrics

Antenna element type	Aperture size (mm)	Physical Aperture area (m^2)	Bandwidth	Peak gain (dBi) at (900 MHz)	HPBW at 900 MHz		Aperture Efficiency (900 MHz)
					E-plane	H-plane	
SOTA BAVA	90 × 90	0.0081	10:1	3	Unknown	Unknown	217%
Fractal antenna	93 × 85	0.0079	3:1	2.58	83.2°	96.2°	208%

5.4.5 References

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

6.0 RF Coupling

6.1 Enclosure Effects on RF Coupling

(Mohamed Hamdalla and Ahmed Hassan)

6.1.1. Problem Statement, Approach, and Context

Primary Problem: UAVs are typically considered metallic/dielectric enclosures depending on their frame material. The shielding effectiveness of such enclosures might be compromised due to the slots and gaps on these enclosures, creating upset susceptibility to the enclosed electronics. The goal of this work is to quantify how the thresholds for upset susceptibility of enclosed wires and integrated circuits differ from those in free space.

Solution Space: Study enclosures with different shapes, material compositions, and slots to quantify their effect on RF coupling to the enclosed wires and electronics typically used in UAVs. The study will focus on the low-frequency range where the incident wavelength is comparable to the size of the enclosure or larger.

Sub-Problem: UAVs are manufactured with a wide variety of shapes and composites to accomplish an exponentially expanding list of missions. The configurations previously reported in the literature have simplistic assumptions regarding the shape and material composition of UAV enclosures that might overestimate or underestimate susceptibility.

State-of-the-Art (SOTA): Simple statistical analysis of specific enclosure configurations using either brute force simulations/measurements or pure statistical methods.

Deficiency in the SOTA: Brute force simulations/measurements of the voltages and currents induced in wires and integrated circuits contained in enclosures are computationally or experimentally complex and have several limitations. The computations are complicated by the multiscale nature of the simulations, and the experiments are complicated by the cost of the equipment and the extensive time needed to measure every variation to cover all possible scenarios. Statistical methods, such as the Random Coupling Model (RCM) for example [1], are only accurate for high frequencies where the wavelength is much smaller than the size of the enclosure. Another main deficiency of the RCM is that it can't predict the exact induced voltages and currents for a specific well-characterized system but it only provides the statistical properties of these induced currents and voltages.

Solution Proposed: Apply Characteristic Mode Analysis (CMA) to identify the fundamental modes of the enclosure, current distribution, and the field pattern of each mode. This will allow us to predict the worst-case RF coupling scenarios without the need for lengthy simulations and/or expensive experimental measurements. The proposed approach can predict measurements at a fraction of the cost/time.

Relevance to OSPRES Grant Objective: Provide general guidelines on how the environment, in this case, the enclosure, affects RF coupling and subsequent electromagnetic absorption to UAV wires and integrated circuits.

Risks, Payoffs, and Challenges: The modes depend mainly on the shape and material of the enclosure. Since UAVs have a wide variety of shapes and material compositions, a library of several UAVs needs to be studied before quantitative general conclusions can be drawn. Challenges can be mitigated by the use of the classification techniques of Machine Learning (ML). That is, different ML techniques will be evoked to detect hidden patterns on how the shape, material composition, and the shape/size location of slots correlate with the field enhancement inside the enclosure.

6.1.2 Tasks and Milestones / Timeline / Status

A. Complete the CMA implementation for studying the shielding effectiveness of metallic enclosures. Validate whether CMA can predict the worst-case shielding effectiveness of metallic enclosures as a function of their shapes. / JAN21 / Complete.

   A1. Prepare a manuscript for IEEE AWPL to document the progress done in A. / Ongoing.

B. Use CMA tool in (A) to predict the worst-case internal field magnitude of metallic and dielectric enclosures of ten COTS UAVs as a function of HPM waveform. / MAY21 / Ongoing.

C. Use the database in (B) to train a Machine Learning (ML) platform to predict RF coupling to enclosed wires and electronics. / OCT21 / Ongoing.

D. Progressively build an accurate representation of the UAV wiring system with all of the integrated circuit (ICs) and electronics to test assist the predictions of (c) and the experimental measurement of the actual UAV. / JUL21 / ongoing

6.1.3 Progress Made Since Last Report

D1. We have prepared a compact table, Table 6.1, that summarizes the basic components of the UAV circuitry and wiring system.

D2. We have created a full-wave model of a complete UAV with all of the wires and IC components to use as a numerical platform for studying effects and validating predictions. Figure. 6.1.1b shows the wiring diagram of the actual UAV with the different IC components. We have built an accurate replica of the UAV in Fig. 6.1.1a using the full-wave electromagnetic solver CST MWS/FEKO which is shown in Fig. 6.1.1c. The wires' length and diameters match the values in the actual UAV in Fig. 6.1.1a and match the values in Table 6.1. The CST/FEKO model has all the components modeled as a linear 50 Ω load, as a first approximation of the model. Thus, we were able to run exhaustive numerical frequency domain experiments to study the response to different incident electromagnetic waveforms.

D3. The full UAV model developed in B was compared to the simplified UAV model shown in Fig. 6.1.1d. The size of the rectangular patch of the simplified model is similar to the size of the metallic representation of the controller in the accurate model shown in

Fig.6.1.1a. The length of the wires of the simplified model is similar to the corresponding wires of the accurate model shown in Fig.6.1.1b.

D4. The electronic speed controller (ESC) is replaced by a 50 Ω load in both models in Fig. 6.1.1c and Fig. 6.1.1d and both models were excited by a plane wave excitation from multiple directions, $0^\circ<\theta<180^\circ$ with 22.5° increment and $0^\circ<\varphi<360^\circ$ with 22.5° increment. The average voltage over all the excitation angles across this load is plotted over the frequency range.

6.1.4 Significant Finding(s) and Mission Impact

6.1.4.1 Summary to Date

A1. A fast full-wave tool that facilitates studying the effect of a metallic enclosure on shielding effectiveness has been developed Using CMA.

6.1.4.2 Since Last Report

a. Figure. 6.2a illustrates that over the frequency range, the average induced voltage across the ESC on both UAV models exhibits the same response. That is, the load voltage, on average, peaks at 0.25 GHz. Moreover, the comparison between the voltage of both models shows a good agreement across the frequency range.

b. Figure.6.2b and Fig.6.2c show the probability of the induced voltage on the ESC to exceed –30 dB and –45 dB respectively. a good agreement between both models is achieved over the frequency range with slight deviation which proves the ability of the simplified model to detect all the possible coupling permutation and not only the average response.

c. Taking into consideration the computational time and the complexity of studying the actual wiring system of a specified UAV model, the simplified model of the geometry with the appropriate dimensions can give a good estimation of the coupling mechanism to the UAV loads. However, this might be applicable for the lower frequency range only where the wires bend and shape variation doesn't play a significant role.

6.1.5 Future Work

a. Based on our findings, for low-frequency analysis, we can study the effect of the enclosures on the coupling using the simplified UAV model rather than trying to model the actual wiring system.

b. The different electronics and components in Fig. 6.1.2c/Table 6.1, i.e. the motors, the ESCs, and the PX4 board, will be replaced by equivalent circuits obtained via direct experimental measurements or from the components' datasheets.

c. Compare the relatively high-frequency response of both UAV models.

Table 6.1. Quadcopter's main circuitry components and wires.

Part function	*Part #*	*specs.*	*length*
motor feed lines	1	18 AWG	
ESC out power lines	2	16 AWG	
ESC in power lines	3	16 AWG	~20 cm
esc in signal	4	22 awg	25 cm
battery out	5	14 AWG	
battery to controller	6	22 AWG	
main controller (autopilot)	7		carrier board 9.5 cm X4.5 cm
GP.1575.25.4.A.02 GPS/Galileo 25*25*4mm 1575.42MHz Patch Antenna2	8	22 AWG	~20 cm
Readytosky® 2212 920KV Brushless Motors	9		
SimonK 30A ESC Brushless Speed Controller	10		
Pixhawk Power Module 5.3V BEC XT60	11		

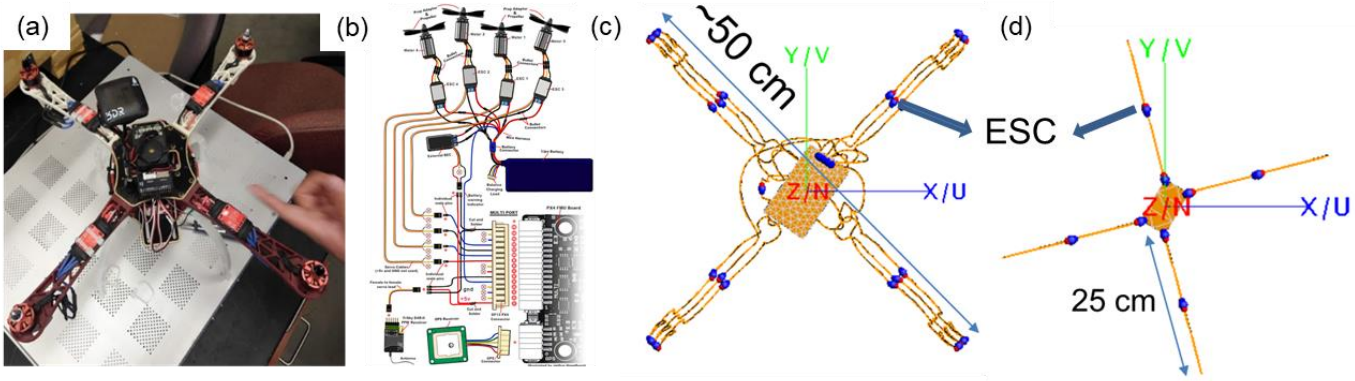


Fig. 6.1. (a) Model of the realistic UAV circuitry showing the wires, components, and frame, (b) the UAV wiring diagram showing all the wires and components, (c) the CST MWS model of the UAV in (a) and (b), (d) the simplified model of the UAV in (a) and (b).

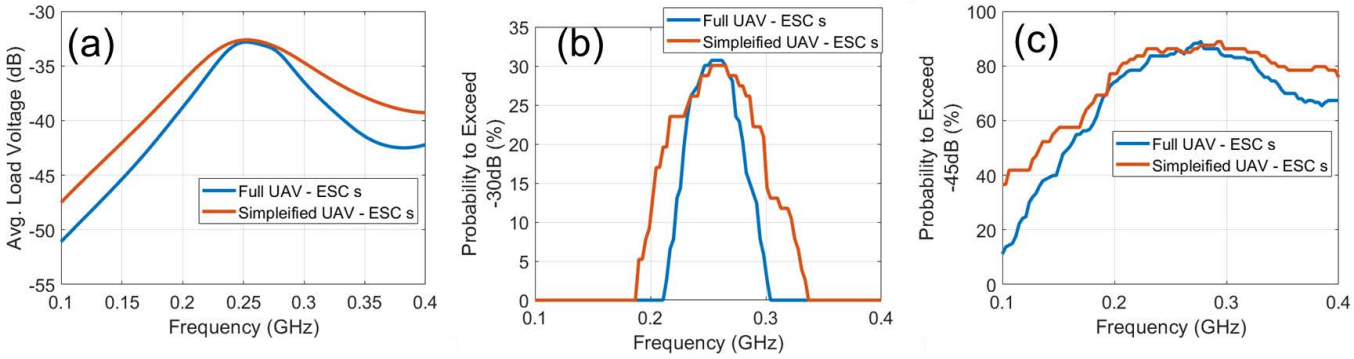


Fig. 6.2. (a) The average induced voltage on the ESC of both the complete UAV model and the simplified model shown in Fig.6.1c and Fig.6.1d respectively. And the probability of the induced voltage on the ESC of both UAV models to exceed, (b) –30 dB, (c) –45 dB.

7.0 Thermal Management

7.1 Micro-Jet Thermal Management System

(Jordan Berg, Roy Allen, and Sarvenaz Sobhansarbandi)

7.1.1 Problem Statement, Approach, and Context

After wrapping up our assessment on the initial jet impingement thermal management system (TMS) technology and concluding that this is not a viable option moving forward, we are currently evaluating the possibility of future work on alternative TMSs for HPM systems in support of the Naval afloat mission. This sub-section is being included as a placeholder.

7.2 Nanofluid Heat Transfer Fluid Development

(Jordan Berg, Roy Allen, and Sarvenaz Sobhansarbandi)

7.2.1 Problem Statement, Approach, and Context

Primary Problem: Dielectric fluids (non-conductive coolant) used in thermal management systems, while suitable for high-voltage HPM-based technologies, possess inherent thermophysical fluid properties (low thermal conductivity, high viscosity) that inhibit their ability to achieve >1 GW/m^3 cooling densities.

Solution Space: Develop a nanofluid by entraining ceramic nanoparticles and dispersants within the dielectric base-fluid, pure silicon fluid (PSF), to increase the nanofluid's thermophysical properties and cooling density capabilities with a similar form-factor.

Sub-Problem: While the dynamic viscosity of the dielectric fluid used, PSF-20cSt, is 'low' relative to other silicone-based fluids, it is ~15 times more viscous than water, and therefore requires increased pumping power within the TMS. Compounding this issue is the necessity to increase the flowrate of the fluid to achieve an equivalent heat removal rate compared to that of a water-based coolant.

State-of-the-Art (SOTA): Nanofluids, with optimal ratios of fluid-to-nanoparticles, have been shown to increase the thermal conductivity of dielectric fluids by 87% in comparison to the generic dielectric fluid alone; resulting in either greater cooling density, decreased pumping power, or reduced mass flow rate requirements.

Deficiency in the SOTA: The addition of nanoparticles within a base-fluid results in a tradeoff between one or more thermophysical properties. For example, adding nanoparticles may increase thermal conductivity of the nanofluid but may result in increased viscosity; i.e., heat removal rate may increase, but the required pumping power along with it. To the best of our knowledge, no one has attempted to create a nanofluid mixture with a goal of keeping the viscosity low. Therefore, the optimal nanoparticle-to-fluid ratio and specific nanoparticle type for the HPM thermal management systems needs to be identified and optimized with an attempt to maintain the viscosity of the mixture as low as possible.

Solution Proposed: Develop a nanofluid with both desirable thermal properties and a relatively low viscosity that can serve as a viable heat transfer fluid (HTF) for TMSs in HPM topologies and other high power density applications. Utilize systematic numerical and experimental strategies to evaluate a large sample set of various nanoparticles (with surfactants and dispersants).

Relevance to OSPRES Grant Objective: Increase cooling densities for HPM systems without requiring TMS design permutations, while decreasing pumping power requirements, in-line with the SWaP-C^2 objective.

Risks, Payoffs, and Challenges:

Risk: The pressures incurred by using a silicone-based fluid in a high-flow regime are not insignificant; large pump-chiller systems may still be necessary.

Challenges: Creating low volume-fraction samples of nanoparticles and surfactants is near equipment precision limit. Maintaining accuracy is critical to properly study modified fluids.

Payoff: A modified nanofluid dielectric fluid can be used to increase cooling capacity of any high power density system. An optimized nanofluid has the potential to extract 20% up to several factors more than the base fluid.

7.2.2 Tasks and Milestones / Timeline / Status

(A) Measure thermophysical properties of currently utilized PSF-20cSt / DEC20–JAN21 / Completed.

(B) Establish theoretical model of nanofluid compositions / DEC20–JAN21 / Completed.

(C) Create and test modified PSF-20cSt with nanoparticles and surfactants / JAN–MAR 21 / In progress.

(D) Select the nanofluid mixture with optimal thermal properties and re-evaluate the CFD modeling / MAR–APR21 / TBD.

7.2.3 Progress Made Since Last Report

(A) 18 nanofluids and the control have been prepared and tested in the differential scanning calorimeter (DSC) to determine the specific heat capacity of each sample.

(B) Several samples show desired specific heat capacity change relative to the base fluid.

7.2.3.1 Summary to Date

Based on literature, the creation of a dielectric nanofluid for use as a coolant in the HPM system could potentially improve cooling performance. The thermal dissipation requirements for HPM systems are not insignificant and could, therefore, benefit from performance enhancement from every aspect (geometric optimization, reduction of thermal resistances, coolant selection, material selection, etc.). A sample of the PSF-20cSt that was used in the experimental testing of the JI-TMS was tested with a Differential Scanning Calorimeter (DSC). The specific heat of the fluid was found to

significantly differ from that of the manufacturer's value. The vendor's reported value of the PSF-20cSt was 1.6 $\frac{J}{gC}$, while DSC measurements showed it to be closer to 1.4 $\frac{J}{gC}$. This difference hinders the accuracy of the CFD results of the TMS. Given the aforementioned error in specific heat capacity, coupled with the need for a high thermal performance coolant, nanoparticle-modified PSF-20cSt was determined to be a necessary and useful undertaking. Three different ceramic nanoparticles were chosen to be studied: alumina, silicon carbide, and iron (II,III) oxide. Ceramics were chosen to maintain HTF dielectric properties.

7.2.3.2 Since Last Report

Nineteen total nanofluid samples have been prepared. 9 Nanofluid samples were created by varying mass fractions (0.25, 0.5, and 0.75 wt. %) of various ceramic nanoparticles (Fe_2O_3, SiC, and Al_2O_3) in the PSF-20-cSt HTF mixed with two surfactants, as well as a set of 9 samples with no surfactants added. The purpose of surfactants in each of the mixtures is to help with the even dispersion of the nanoparticles in the HTF. Justification in testing samples with no surfactants comes from the realization that the surfactants chosen (based off of the literature) are much more viscous than the PSF. Though the volume fraction of the surfactant additives is on the order of 0.01 wt % of the sample, adding viscous fluids in the mixtures directly opposes the goal of creating a low-viscosity HTF. The addition of surfactants may be superfluous since the HTF with be in circulation. This circulation could agitate the mixture well enough so as to not need additional dispersants. DSC testing has be completed. These tests show the specific heat capacity (Cp) of each of the 19 samples. Each sample was tested in a range of 10–35 °C.

The following figures detail the DSC testing results of the nanoparticle-modified coolant. Figure 7.2.1 compares the Cp values received from the vendor, theoretical values, and the DSC values. The is a clear disparity in each of the values. However, we believe the measured data is correct for the following reasons. The vendor was contacted and when asked about the testing details on how the 1.6 J/gC value was determined, no answer was given, nor was a technical liaison available to reachable. The theoretical values rely on experimental data that is based off of temperature only and may vary from different manufactures and viscosities of silicone fluids. The DSC in the ART-E laboratory has

recently been calibrated and measures the actual fluid directly that was used in all 19 samples.

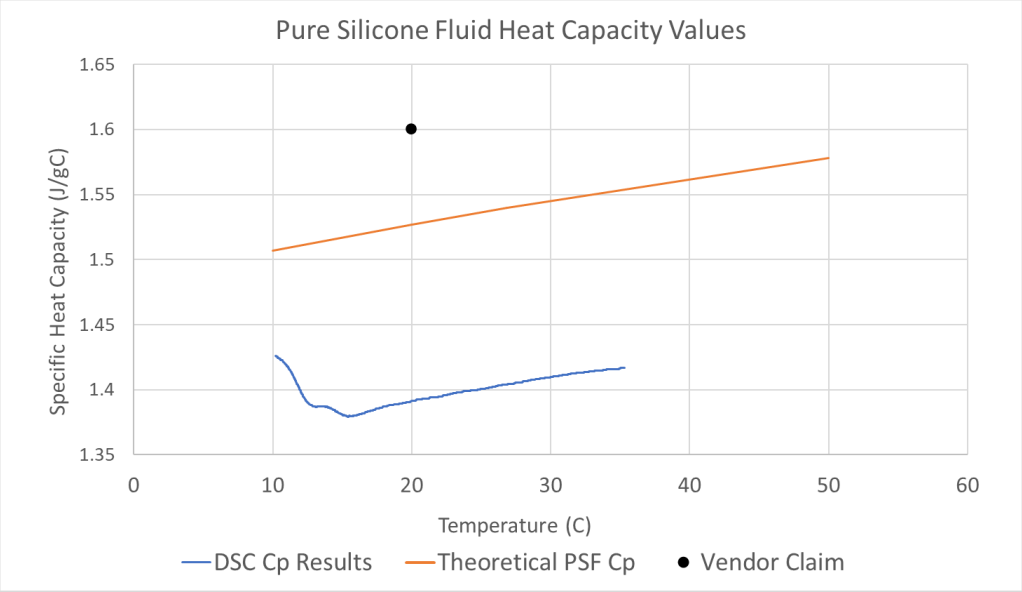


Figure 7.2.1. Comparison of vendor, theoretical, and measured PSF-20cSt Cp values.

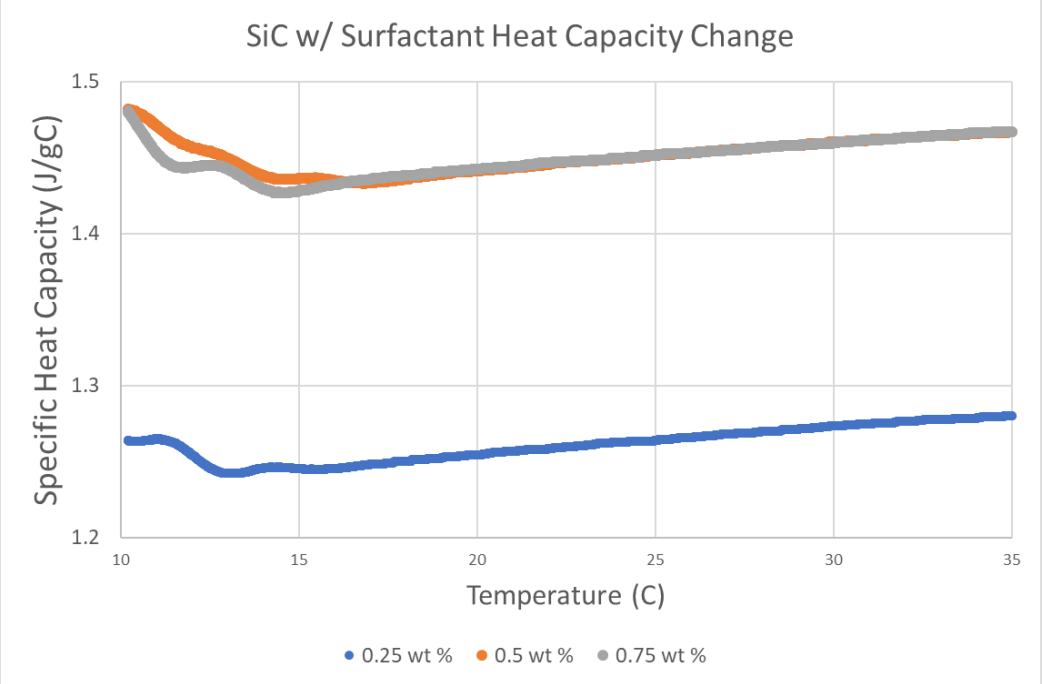


Figure 7.2.2. DSC measurements of SiC nanofluid samples.

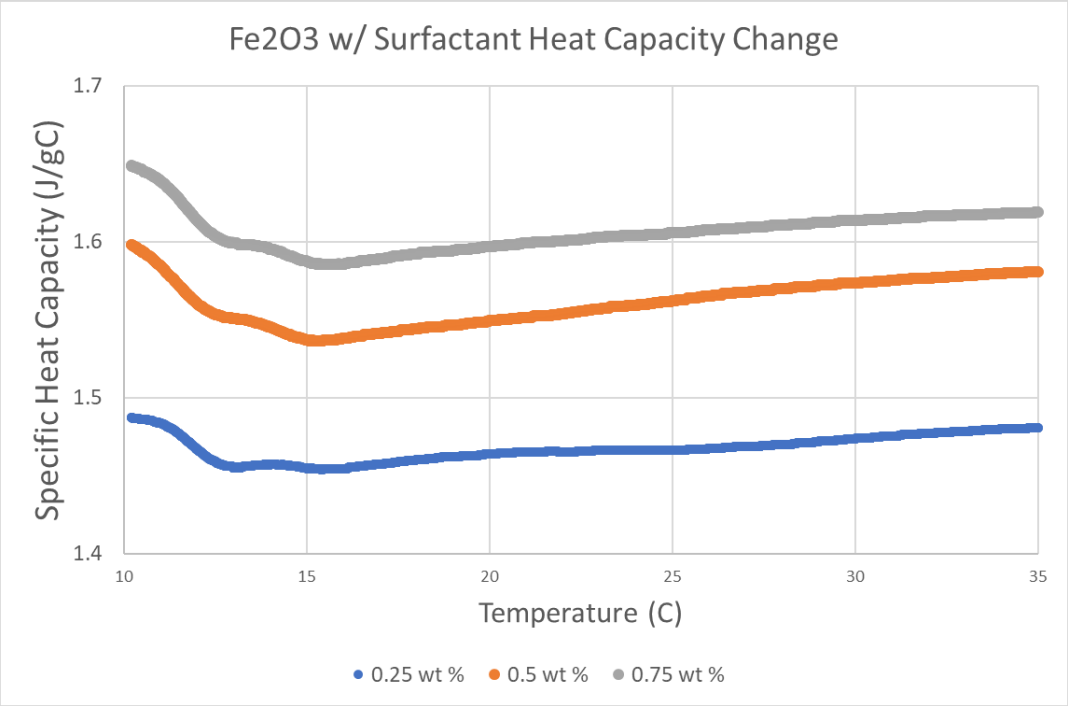


Figure 7.2.3. DSC measurements of Fe_2O_3 nanofluid samples.

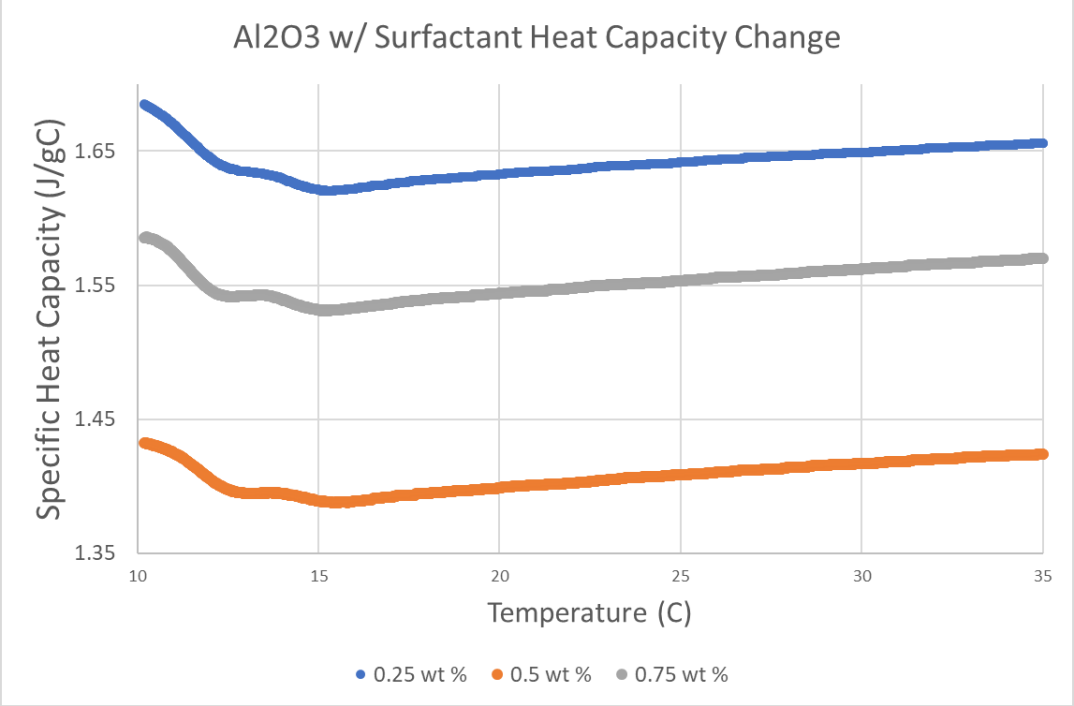


Figure 7.2.3. DSC measurements of Al_2O_3 nanofluid samples.

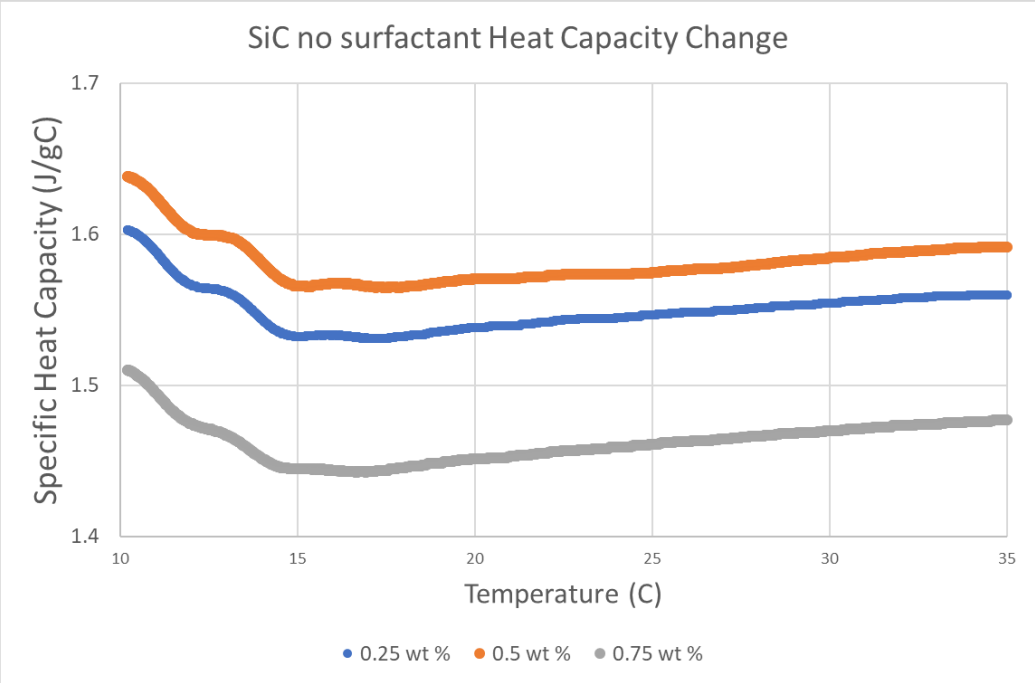


Figure 7.2.4. DSC measurements of SiC with no surfactant samples.

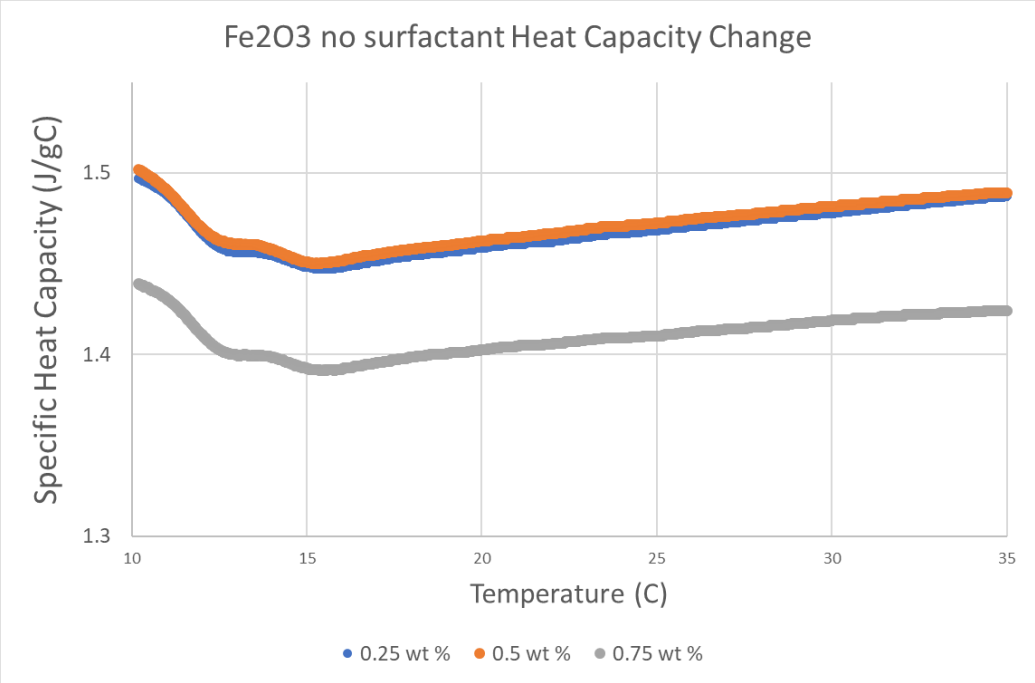


Figure 7.2.5. DSC measurements of Fe_2O_3 with no surfactant samples.

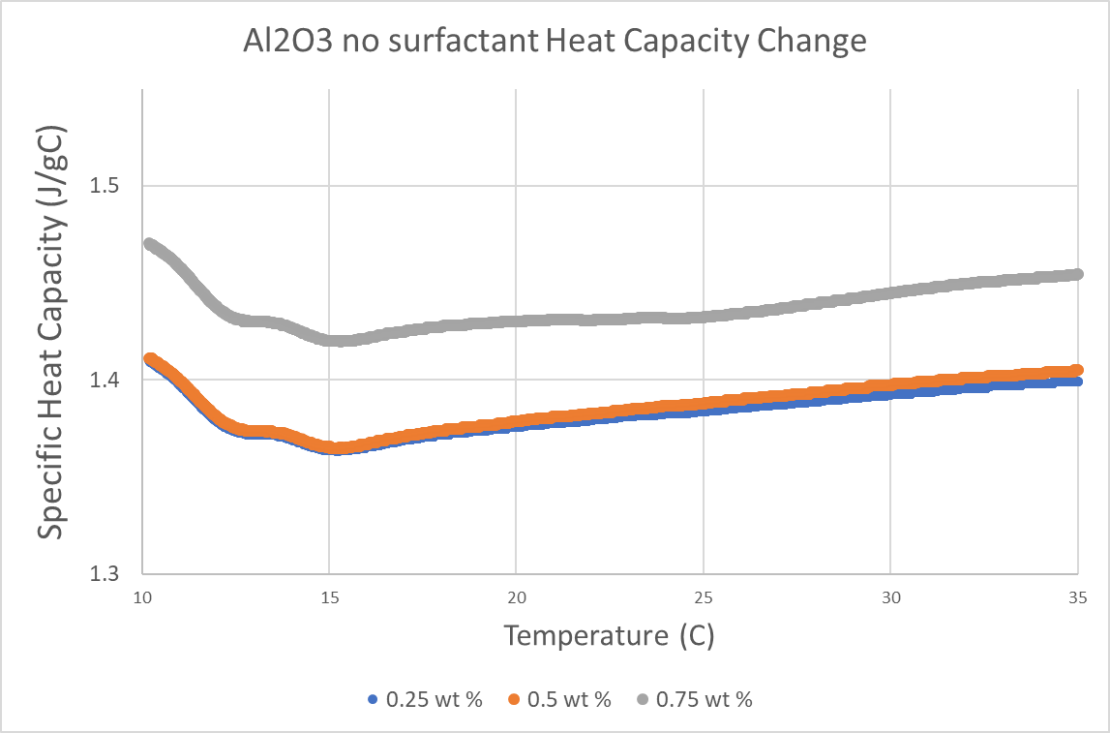


Figure 7.2.6. DSC measurements of Al_2O_3 with no surfactant samples.

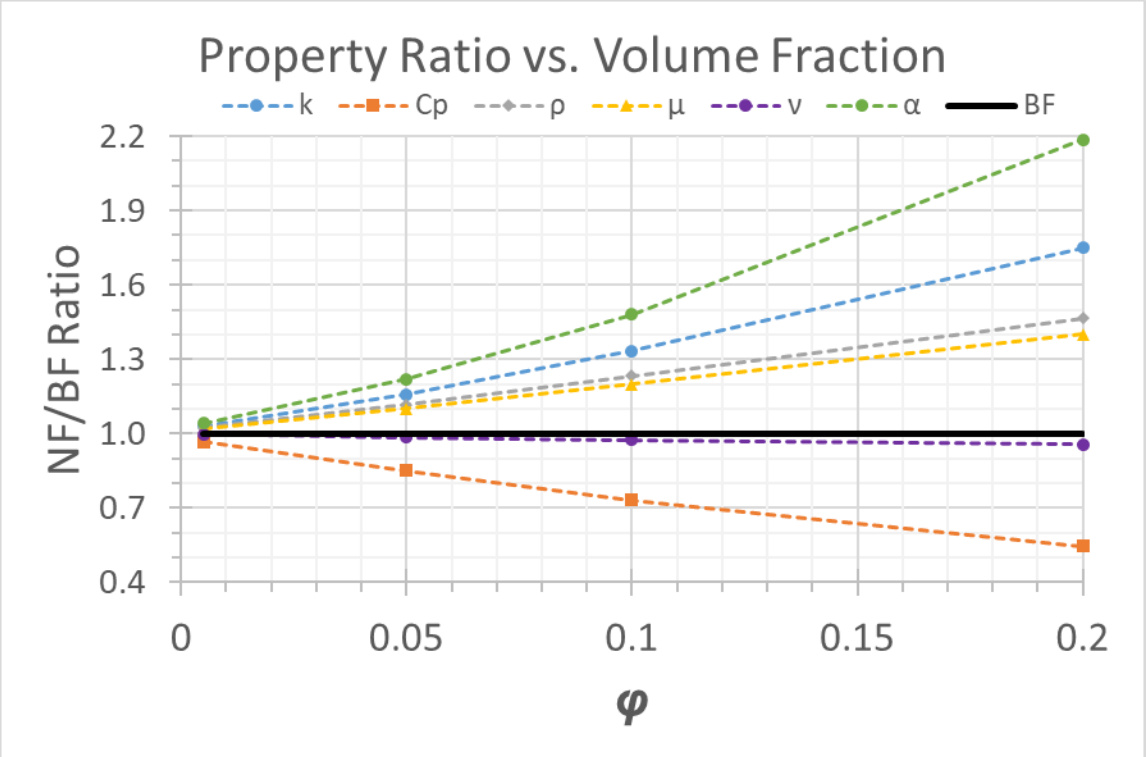


Figure 7.2.7. Theoretical fluid property changes vs volume fraction (φ) of nanoparticles.

Overall, the fluid Cp change is minimal. This is expected and due to the low mass fraction of nanoparticles that are being added to the base fluid in order to preserve the fluid's low viscosity. According to the theoretical values from Figure 7.2.7, as Cp decreases, the thermal conductivity increases. As increased thermal conductivity is the primary fluid property that is desirable to have increased, all the nanofluids with a decrease in Cp from the base fluid are expected to have increased thermal conductivity. The most promising sample thus far is 0.25 wt % SiC with surfactants. Thermal conductivity testing will determine if this hypothesis is accurate.

8.0 Program Management

8.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

8.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

8.3 Major Procurement Actions

i. Microsoft Office 365 GCC High (75 seats) - $45,000 (for OSPRES Contract CUI Compliance)

8.4 Travel

Destination	Purpose	Attendees	Estimated Costs

8.5 Pending or Upcoming Public Release Requests

9.0 Appendix B: Academic and IP Output

9.1 Students Graduated

Name	Degree	Currently
Al-Shaikhli, Waleed	MS	Kansas City National Security Campus, Honeywell
Bissen, Bear	MS	UMKC/MIDE (Staff)
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Hanif, Abu	PhD	
Harmon, Aaron	BS	Missouri University of Science & Technology
Harp, Joshua	MS	Small Business
Hauptman, Cash	BS	University of Nebraska-Lincoln
Labrada, Dario	BS	UMKC/MIDE (MS Student)
Lancaster, John	MS	Lawrence Livermore National Laboratory
Renzelman, Jeff	MS	Kansas City National Security Campus, Honeywell
Roy, Sourov	PhD	UMKC/MIDE (Postdoc)
Wagner, Adam	MS	Kansas City National Security Campus, Honeywell
Xia, Shengxuan	BS	Missouri University of Science & Technology

9.2 Conference Publications

[1] W. Azad, S. Roy, and F. Khan, "A Single Gate Driver-based Four-stage High-voltage SiC Switch Having Dynamic Voltage Balancing Capability," accepted in *2021 IEEE Applied Power Electronics Conference and Exposition* (APEC), Phoenix, AZ, USA, June 9-12, 2021.

[2] W. Azad, S. Roy, F. Khan and A. N. Caruso, "A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuits,"accepted in *2021 IEEE Kansas Power and Energy Conference* (KPEC), Manhattan, KS, USA, April 19-20, 2021.

[3] J. Hunter, S. Xia, A. Harmon, A. M. Hassan, V. Khilkevich, and D. Beetner, "Modeling and Statistical Characterization of Electromagnetic Coupling to Electronic Devices," *IEEE International Symposium on Antennas and Propagation and NSRM USNC-URSI National Radio Science Meeting*, Boulder, CO, January 4-9, 2021.

[4] W. Azad, S. Roy, and F. Khan, "A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver," accepted in *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, 2020.

[5] B. Barman, K. C. Durbhakula, B. Bissen, D. Chatterjee, and A. N. Caruso, "Performance Optimization of a Microstrip Patch Antenna using Characteristic Mode and D/Q Analysis," *2020 XXXIIIrd General Assembly and Scientific Symposium of the International Union of Radio Science*, Rome, Italy, Aug 29 - Sept 5, 2020, pp. 1-4 (online conference).

[6] J. Berg, and S. Sobhansarbandi. "CFD Modeling of Thermal Management Systems for a Silicon Semiconductor Switch." *ASME 2020 Heat Transfer Summer Conference collocated with the ASME 2020 Fluids Engineering Division Summer Meeting and the ASME 2020 18th International Conference on Nanochannels, Microchannels, and Minichannels*, Virtual, July 13–15, 2020, American Society of Mechanical Engineers Digital Collection [doi].

[7] B. Barman, D. Chatterjee, and A. N. Caruso, "Performance Optimization of Electrically Small Microstrip Patch Antennas on Finite Ground Planes," 2020 *IEEE International Symposium on Antennas and Propagation and North American Radio Science Meeting*, Montreal, Quebec, Canada, July 5-10, 2020, pp. 1–2 (online conference).

[8] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, "Scalable Characteristic Mode Analysis: Requirements and Challenges (White Paper)," *Large Scale Networking (LSN) Workshop on Huge Data: A Computing, Networking and Distributed Systems Perspective Sponsored by NSF*, Chicago, IL, April 13-14, 2020.

[9] M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Predicting Electromagnetic Interference to a Terminated Wire Using Characteristic Mode Analysis," *Proceedings of the Annual Review of Progress in Applied Computational Electromagnetics (ACES)*, Monterey, CA, March 22-26, 2020.

[10] W. Azad, F. Khan, and A. Caruso, "Self-sustaining High-power RF Signal Generation Using LDMOS Based Power Amplifier and Nonlinear Transmission Line," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 3567-3572 [doi].

[11] A. Hanif, W. Azad, and F. Khan, "Detection of Bond Wire Lift Off in IGBT Power Modules Using Ultrasound Resonators," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 345-350 [doi].

[12] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, "Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS," *Annual Directed Energy Science and Technology Symposium*, March 2020 (abstract appeared, but talk cancelled due to pandemic).

[13] B. Barman, D. Chatterjee, and A. N. Caruso, "Some Investigations into Mutual Coupling Analysis for Trade Space Studies of Linear Arrays," *2019 IEEE International Symposium on Phased Array Systems and Technology (PAST)* Waltham, MA, October 2019, pp. 1-8.

[14] B. Barman, D. Chatterjee, and A. N. Caruso, "Characteristic Mode Analysis of a straight and an L-probe fed Microstrip Patch," *2019 IEEE Indian Conference on Antennas and Propogation (InCAP)*, Ahmedabad, India, Dec 2019, pp. 1-3.

[15] M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of the Effect of the UAV Frame Material on Coupling and Interference," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019.

[16] M. Hamdalla, J. Hunter, Y. Liu, V. Khilkevich, D. Beetner, A. Caruso, and A. M. Hassan, "Electromagnetic Interference of Unmanned Aerial Vehicles: A Characteristic Mode Analysis Approach," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019.

[17] B. Barman, D. Chatterjee, and A. N. Caruso, "Analytical Models for L-Probe fed Microstrip Antennas," *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

[18] K. C. Durbhakula, J. Lancaster, J. Hunter, Y. Liu, D. Beetner, V. Khilkevich, D. Chatterjee, A. N. Caruso, and A. M. Hassan, "Electromagnetic Coupling Analysis of Printed Circuit Board Traces using Characteristic Mode Analysis," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (2 pages)*, Atlanta, Georgia, USA, July 7-12 2019.

[19] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "On the Location of Transverse Electric Surface Wave Poles for Electrically Thick Substrates," Proceedings of the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019.

[20] M. Hamdalla, B. Bissen, A. N. Caruso, and A. M. Hassan, "Experimental Validations of Characteristic Mode Analysis Predictions Using GTEM Measurements," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Montréal, *Québec, Canada, July 5-10, 2020*.

[21] W. Azad and F. Khan, "Sustaining High-power RF Signal Generation in a Positive Feedback Network," *2019 IEEE Pulsed Power and Plasma Science Conference (PPPS)*, Orlando, FL, USA, June 23-28 2019.

[22] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, "Scalable characteristic mode analysis using big data techniques," *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[23] M. Hamdalla, W. Al-Shaikhli, J. Lancaster, J. D. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of Electromagnetic Coupling to Wires with Realistic Shapes," *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[24] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "Location of Surface Wave Poles in Sommerfeld Integrals: A Mittag-Leffler Expansion Approach," *Proceedings of the URSI-B International Symposium on Electromagnetic Theory*, URSI Commission, San Diego, USA, May 2019.'

[25] D. Chatterjee, B. Barman. J. Kovarik, and A. N. Caruso, "Studies on Antenna Characterization and Propagation of High Power Pulsed Electromagnetic Waves with Minimal Spatial Dispersion," presented at the *Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium* Destin, Florida, USA, April 2019.

[26] J. Kovarik, B. Barman, D. Chatterjee and A. N. Caruso, "Some Investigations into Applications of Electrically Small Antennas as Phased Array Elements," presented

at the *Directed Energy Professional Society* (DEPS) *Annual Science and Technology Symposium*, Destin, Florida, USA, April 2019.

[27] K. C. Durbhakula, D. Chatterjee and A. M. Hassan, "Analytical Evaluation of Sommerfeld Integral Tails Present in Two-layered Media Green's Functions," *Proceedings of the Indian Conference on Antennas and Propagation* (InCAP), Hyderabad, India, December 2018.

[28] D. Beetner, V. Khilkevich, A. M. Hassan, J. Hunter, Y. Liu, and D. Floyd, "Characterization of the Electromagnetic Coupling to UAVs," *DE Systems Symposium*, September 24-27, 2018

[29] C. Hartshorn, K. Durbhakula, D. Welty, D. Chatterjee, J. Lancaster, A. M. Hassan, and A. N. Caruso, "Crosstalk and Coupling to Printed Circuit Board Metallic Traces with Arbitrary Shapes," *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[30] M. Hamdalla, J. Roacho-Valles, J. Hunter, D. Beetner, A. M. Hassan, and A. N. Caruso, "Electromagnetic Analysis of Unmanned Aerial Vehicles Using Characteristic Mode Analysis," *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[31] C. Hartshorn, M. Hamdalla, J. Lancaster, A. M. Hassan, and A. N. Caruso, "Electromagnetic Vulnerability of Wires with Arbitrary Shape," *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[32] K. C. Durbhakula, D. Chatterjee, A. M. Hassan, and M. S. Kluskens, "Studies on Numerical Evaluation of Sommerfeld Integrals for Multilayer Topologies," *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018.

[33] J. Lancaster, D. Chatterjee, and A. N. Caruso, "Some Investigations into the Dispersion Characteristics of Localized Bessel Beams," published in the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018 (1 page URSI Abstract).

[34] M. Hamdalla, A. M. Hassan, and A. N. Caruso "Characteristic Mode Analysis of Unmanned Aerial Vehicles with Realistic Shapes and Material Composition," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Boston, MA, July 8-13, 2018.

[35] W. Azad, S. Roy, A. S. Imtiaz, and F. Khan, "Microelectromechanical System (MEMS) Resonator: A New Element in Power Converter Circuits Featuring Reduced EMI," *2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, Niigata, May 20-24, 2018, pp. 2416-2420 [doi].

[36] J. Hunter, Y. Liu, D. Floyd, A. Hassan, V. Khilkevich, and D. Beetner, "Characterization of the Electromagnetic Coupling to UAVs," Annual Directed Energy Science and Technology Symposium, Feb 26-March 2, 2018.

9.3 Journal Publications

9.3.1 In Preparation

[1] W. Azad, F. Khan, and A. N. Caruso, “A Series-connected High-voltage SiC Switch Driven by a Compact High-voltage Isolated Gate Driver,” In preparation, **2021.**

[2] M. Z. M. Hamdalla, B. Bissen, J. D. Hunter , L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, “Experimental Evaluation of CMA Predictions and Control of Electromagnetic Interference to UAVs,” In Preparation, **2021**.

[3] S. Xia, J. Hunter, A. Harmon, M. Hamdalla, A. Hassan, V. Khilkevich, D. Beetner, “Simulation Driven Statistical Analysis of the Electro-magnetic Coupling to Microstriplines,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[4] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, “Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field Coupling to Randomly Shaped Wires,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[5] W. Azad, F. Khan, and A. N. Caruso, “A Medium Power, Self-Sustaining, Configurable RF Pulse Generation Circuit Using a Nonlinear Transmission Line and Power Amplifier in a Closed Loop Configuration, In Preparation, **2020**.

9.2.2 Submitted / Under Revision

[6] J. N. Berg, R. C. Allen, and S. Sobhansarbandi. “A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation.” *International Journal of Thermal Sciences*, Submitted, **2021**.

[7] W. Azad, F. Khan, and A. Caruso, "A Medium Power, Self-sustaining, Configurable RF Pulse Generation Circuit Using Nonlinear Transmission Line and a Power Amplifier in Closed Loop Configuration,” *IEEE Transaction on Plasma Science*, Submitted, **2021**.

[8] Khulud Alsultan, Mohamed Hamdalla, Sumitra Dey, A. N. Caruso, Praveen Rao, and A. M. Hassan, “Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform,” *IEEE Open Journal of Antennas and Propagation,* Submitted, **2020**.

[9] John Keerthi Paul Bhamidipati, Eliot R. Myers, Adam M. Conway, Lars F. Voss, and Anthony N. Caruso, “Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches,” *IEEE Transactions on Electronic Devices*, Under Revision, **2020**.

9.3.2 Published / In Press

[10] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems," *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364-373, **2019**.

[11] S. Roy, W. Azad, S. Baidya and F. Khan, "A Comprehensive Review on Rectifiers, Linear Regulators and Switched-mode Power Processing Techniques used for Powering Biomedical Sensors and Implants inside Human Body," *IEEE Transactions on Power Electronics*, Accepted, **2021**.

9.4 External Presentations/Briefings

DEPS Posters and Presentations 2020

[1] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[2] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

GOMAC 2019

[3] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[4] Eliot Myers, Picosecond High Power Switching Technologies

[5] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

DEPS Posters and Presentations 2019

[6] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[7] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[8] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[9] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[10] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[11] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[12] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[13] Deb Chatterjee, Studies On Antenna Characterization And Propogation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

DEPS Posters and Presentations 2018

[14] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[15] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[16] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

DEPS Posters and Presentations 2017

[17] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

9.5 IP Disclosures Filed

Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, 19UMK005, 28SEPT2018

Doynov, “Pulse Differential High-power Microwave Generation”, 19UMK007, 02JAN2019.

Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal”, 19UMK008, 28DEC2018.

Doynov, Caruso, “High-efficiency High-power Microwave Generation using Multipass Non-linear Network Topologies”, 19UMK017, 29AUG2020.

Doynov, “Scalable Modular System for High-power Microwaves Generation”, 20UMK010, 19APR2020.

Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna”, 20UMK011, 19APR2020.

Shepard, “A Novel Optical Fiber Amplifier”, 20UMK012, 02JUN2020.

Shepard, “A Low Noise Optical Amplifier”, 21UMK007, 14SEPT2020.

Bhamidipati, Myers, Caruso, “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources”, 21UMK009, 04NOV2020.

9.6 Provisional Patents Filed

Doynov, Caruso, “High-efficiency High-power Microwave Generation using Multipass Non-linear Network Topologies”, filed 26NOV2019.

9.7 Non-Provisional Patents Filed

None to date

ONR HPM Program - Monthly Status Report (MSR) – MAY 2021

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 JUNE 2021

Distribution Statement ~A: Distribution authorized to all OSPRES Grant and Contract performers, and any OSPRES uncompensated collaborators. Further dissemination per the Office of Naval Research, Ryan Hoffman (ryan.hoffman@navy.mil, 703-696-3873) or higher DoD Authority.

OSPRES Grant Goal: address and transition technologies and capabilities that enable the OSPRES Grant Objective using the OSPRES Grant Approach, while educating the next generation of pulsed power and defense minded, stewards and innovators.

OSPRES Grant Objective: to execute high-risk, high-payoff efforts that mitigate, fill or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable and electronically steerable high power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average power space, and includes the kill chain considerations including the target and its responsivity to radiofrequency stimuli.

OSPRES Metrics of Success: developed technologies and capabilities that are published in the peer review, protected as intellectual property, and/or, transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use, as enabling/integratable capability(ies).

OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

OSPRES Grant Security: All efforts should be fundamental and publically releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

1.0 Contents

2.0 Executive Summary 3
2.1 Progress, Significant Findings, and Impact 3
2.2 Completed, Ongoing, and Cancelled Sub-Efforts 5
2.3 Running Total of Academic and IP Program Output 6
3.0 Switch Evaluation and Innovation 7
3.1 Lasers and Optics 7
3.2 WBG-PCSS Enabled Laser Diode Array Driver 11
3.3 Diode-Based NLTLs 14
3.4 Si-PCSS Top Contact Modeling and Optimization for Cooling Requirements 19
3.5 GaN:C PCSS Direct RF Modulation 19
3.6 Drift-Step Recovery Diode and Pulse Shaping Device Optimization 22
3.7 SOS-based Pulsed Power Source Systematic Topological Optimization 28
4.0 Prime Power and Conditioning 37
4.1 HV Switch Pulsed Chargers 37
5.0 Tradespace Analysis of Ultra-Wide-Band Antenna Arrays 41
5.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs) 41
5.2 Tradespace Analysis of Other Ultra-Wide-Band (UWB) Single Elements 46
5.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna 53
5.4 Tradespace Analysis of Ultra-Wide-Band (UWB) Fractal Antenna 61
6.0 RF Coupling 69
6.1 Enclosure Effects on RF Coupling 69
7.0 Thermal Management 74
7.1 Micro-Jet Thermal Management System 74
7.2 Nanofluid Heat Transfer Fluid Development 74
8.0 UAS Engagement Wargaming & Modeling and Simulation (M&S) 78
8.1 Airborne Effector Weapon Task Assignment 78
9.0 Program Management 80
9.1 Issues 80
9.2 Interactions with Others 80
9.3 Major Procurement Actions 80
9.4 Travel 80
9.5 Pending or Upcoming Public Release Requests 80
10.0 Appendix B: Academic and IP Output 81
10.1 Students Graduated 81
10.2 Conference Publications 81
10.3 Journal Publications 85
10.4 Conference Presentations 86
10.5 IP Disclosures Filed 87
10.6 Provisional Patents Filed 88
10.7 Non-Provisional Patents Filed 88

2.0 Executive Summary

2.1 Progress, Significant Findings, and Impact

Fiber Lasers – Shepard
Simulations aimed at understanding self-focusing (SF) indicate that the SF of un-guided vs guided modes is dramatically different in its dependence on power. We discovered that, in the guided case, SF induced filamentation is not solely determined by beam power and that it can be controlled via the geometric factors within a waveguide.

Laser Diode Array Driver – Bhamidipati
Non-linear operation of lateral GaN-PCSS has not yet been verified experimentally. Working backwards from the final stage pulse trigger requirements, input pulse requirements for the LDA/LDS have been identified to tailor the switch parameters.

NLTLs – Gardner
In May a single and a double diode high voltage D-NLTL were tested and demonstrated nearly identical behavior. Results showed that with small enough sources of loss, higher voltages and frequencies can be achieved through stacking diodes.

Si-PCSS Top Contact – Eifler
An optimal laser windowing width was determined from TCAD simulations to be 350-μm wide with 10-μm metal widths producing a 30% laser energy reduction. Experimental verification, due to limited number of devices, only qualitatively showed a laser energy reduction and more device testing will be required for experimental confirmation. A summary report for sunset of this work will be included in the next monthly status report.

GaN:C PCSS Direct RF Modulation – Thompson
To better study the mode coupling from fiber into a GaN:C PCSS, single-mode operation was achieved via refinements in the COMSOL input boundary conditions and mesh scale.

DSRD – Eifler
DSRD avalanche models for device breakdown effects were shown to be accurate and were used in a device area and stacking parameter study showing the existence of an optimal die area for DSRD performance. From published work, it was determined that improved primary switch modeling, driver models and circuit parasitics will be required for accurate DSRD and DSRD-based pulser design and optimization.

DSRD – Roy (NEW SECTION)
A newly-constructed version of the SOS-IES pulse generator using DSRDs was tested and evaluated. The pulser developed leverages a topology containing two series-connected stages, each containing two parallel branches (i.e., a 2×2 permutation), exceeds similarly-sized and peak voltage output COTS systems through achieving nearly an order of magnitude increase in pulse repetition frequency (100-kHz) while generating 100% shot production within the 100-shot burst. All air cooled!

HV Switch – Azad
The arcing location in the gate driver at high-voltage has been identified. The gate driver PCB design has been revised to address the malfunctioning and sent out for fabrication.

ESAs – Barman
Performance optimization (in terms of bandwidth and gain) of the ESA element designs, which were reported earlier, have been initiated via stochastic and ML algorithms. Preliminary investigations show stochastic algorithms, such as Genetic Algorithm (GA), Particle Swarm Optimization (PSO), and Nelder-Mead Simplex method, are computationally intensive and do not significantly improve antenna performance.

UWB Antenna Elements (All sections combined) – Durbhakula
The array aperture area reduction tradespace study has been initiated for all the three antennas i.e., Koshelev, Shark and Fractal antennas. A comparison of various Koshelev array antenna topologies indicated that the diamond array topology is the optimum for improved center element S11, whereas the octagon array topology produced low side lobe levels with minimum reduction in gain. A tradeoff has been noticed between frequency domain gain and bandwidth of the Koshelev array antenna as the interelement spacing is varied. We also have added new machine learning algorithms to the study and prediction of antenna metrics of Fractal antenna.

RF Coupling – Hamdalla/Hassan
In the previous MSRs, we developed a CAD model of all the wires in a particular UAV to act as a platform for numerical RF coupling experiments. During the semi-annual review, we received several recommendations to study the effect of changing the UAV wire shapes. Therefore, we deformed the wires' shapes in the CAD UAV model to create multiple arbitrarily shaped yet realistic wire distributions. Our analysis shows that the UAV frame constraints the UAV wires leading to small variation in their shapes. These small variations caused the voltages coupled to the deformed wires to be very similar to that of the straight wires. This analysis shows the advantage of the numerical UAV platform in identifying which parameters significantly affect RF coupling.

Nanofluid – Berg/Sobhansarbandi
According to the DSC sample testing, the nanofluid that showed the most significant improvement in heat capacity was silicon carbide 0.25 wt%. This sample was used to determine the increase in thermal conductivity and showed a 32% increase over that of the base fluid. Using the new thermophysical in the CFD model, a 18.8% decrease in the maximum PCSS temperature was seen at 200-W average power.

Fields (NEW SECTION)
Recently, the M&S tradespace was expanded to include both fixed and airborne effector solutions. Efforts have been focused on generating realistic simulation environments while also investigating the complex space of weapon task assignment.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

2.2.1 Ongoing Sub-Efforts

	Start	End
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
HV Switch Pulsed Chargers	DEC 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Enclosure Effects on RF Coupling	OCT2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
Nanofluid Heat Transfer Fluid	NOV 2020	Present
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization	JAN 2021	Present
UAS Engagement M&S	MAR 2021	Present
SOS-Based Pulser	APR 2021	Present

2.2.2 Completed Sub-Efforts

Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020

2.2.3 Cancelled/Suspended Sub-Efforts

Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020
Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021
Bistable Operation of GaN	FEB 2021	MAR 2021

2.3 Running Total of Academic and IP Program Output

See Appendix A for authors, titles and inventors (this list is continuously being updated)

2.3.1	*Students Graduated*	5 BS, 8 MS, 2 PhD
2.3.2	*Conference Publications*	37 (4 submitted/accepted)
2.3.3	*Journal Publications*	3 (3 submitted/under revision)
2.3.4	*External Presentations/Briefings*	18
2.3.5	*IP Disclosures Filed*	9
2.3.6	*Provisional Patents Filed*	1
2.3.7	*Non-Provisional Patents Filed*	0

3.0 Switch Evaluation and Innovation

3.1 Lasers and Optics

(Scott Shepard and Heather Thompson)

3.1.1 Problem Statement, Approach, and Context

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$50K to \$5M.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution. This way of implementing an optical fiber laser (via an optical fiber amplifier) has SWaP advantages with respect to traditional (fiber and free-space) laser designs.

Sub-Problem (1): Optical pump power system costs are the dominant source of costs (in both normal/free-space lasers and in optical fiber lasers, of this class).

Sub-Problem (2): Amplified spontaneous emission (ASE) and fiber nonlinearities impede the optical amplifier performance.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive until reduced by a factor of two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping scheme which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments we are pursuing the use of gain saturation and a staged design of different fiber diameters.

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system needed to drive the PCSS will meet the modular and scalable volume and cost aim-points.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability.

3.1.2 Tasks and Milestones / Timeline / Status

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Ongoing.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Ongoing.

(E) Demonstrate a cost-reduced fiber laser. / Ongoing.

(E1) **March 2021** Finalize design. / Complete.
(E2) **April 2021** Assemble and test-check seed LD (laser diode)/driver. / Complete.
(E3) **April 2021** Measure power vs current transfer function of seed LD/driver. / Complete.
(E4) **May–June 2021** Measure ASE and jitter of 1064 nm seed LD/driver.
(E5) **May–June 2021** Measure ASE and jitter of 1030 nm seed LD/driver.
(E6) **May 2021** Assemble and test-check pump LDs/drivers.
/ (E6) – (E9) Delayed due to vendor issues (see below).
(E7) **May 2021** Measure power vs current transfer function of pump LDs/drivers.
(E8) **May 2021** Splice power combiners to Yb doped preamp fiber.
(E9) **May 2021** Connect seed and pumps to power combiners and test-check.
(E10) **June–July 2021** Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle.
(E11) **June–July 2021** Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle.
(E12) **July 2021** Splice power amplifier and its power combiner to best preamp.
(E13) **July–August 2021** Measure gain, ASE and jitter of entire amp assembly.
(E14) **July–August 2021** Analyze data and document.

(F) Design a new type of higher power, tubular core, fiber amplifier. / Ongoing.

3.1.3 Progress Made Since Last Report

(E3) We measured the power vs current transfer function of the 1064 nm seed LDs/driver as shown in Figure 3.1.1(a) after iterating with the vendor to get the proper software for assembly (E2) and initial testing. Results are as anticipated for these parameters.

(E4) We measured the timing jitter of the 1064 nm seed LD/driver to be within spec. as shown in Figure 3.1.1 (b). The quality of the DFB LD is demonstrably better than that of our Wedge laser.

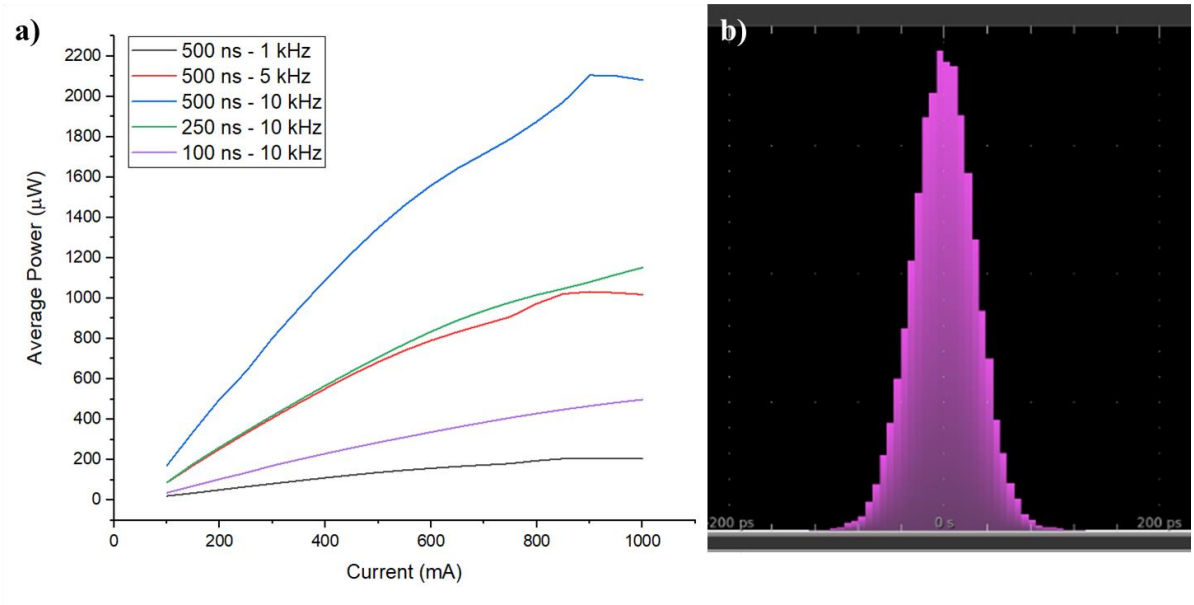


Figure 3.1.1. 1064 nm seed LD measured data. **(a)** power vs current; **(b)** timing jitter.

(E6) – (E9) Our pump LD vendor (based in France) incurred so many delays that we switched vendors (to one based in Virginia). The Yb-doped fiber has been shipped to our collaborator which is fabricating and splicing the power combiners. We decided that we can utilize some higher power connectors (for flexibility) by utilizing an index matching gel to minimize damage from any air present at the glass/air interfaces within a connector.

(F) The design of a new tubular core fiber amplifier requires an improved understanding of self-focusing (SF) and the similar thermal-lensing effects it hopes to mitigate. Thus, we began by studying SF in fiber via COMSOL simulation. Our multimode results have been submitted to the Optical Society of America conference, “Nonlinear Optics,” for review. Our single-mode study is underway now that we have achieved single-mode behavior (c.f., 3.5.4.2). Preliminary results indicate that the SF of un-guided vs guided modes is dramatically different in its dependence on power.

3.1.4 Significant Finding(s) and Mission Impact

3.1.4.1 Summary to Date

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with tolerable pre-burst ASE. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) The design of a proof-of-concept experiment demonstrating a cost-reduced optical pumping scheme was finalized MAR2021.

3.1.4.2 Since Last Report

(F) Self-focusing (SF) arises from the intensity-dependent index of refraction (a χ^3 nonlinear optical process) in Kerr media: $n = n_0 + n_2 I_0$, where I_0 is the optical intensity. In bulk media, propagation takes place in Gaussian beams with curved phase fronts that focus the laser beam to a minimal beam waist before diffraction takes over to spread it back out. Therein SF effects (which manifest primarily to reduce the minimal beam waist and move it to another location) are proportional to the beam power. A broader beam at the same power will reduce the local intensity, but we believe the SF effects are the same because this also forms a larger lens. A guided mode (as in fiber or any other waveguide) does not have a curved phase front (although it can have a Gaussian amplitude profile) and we conjecture that we can alter this lensing effect by altering the dimensions of the guide. Significantly we find this to be the case.

Figure 3.1.2 plots the z-component electric field (the polarization launched) in a fiber of core radius, r_0 = 5 microns, at increasing intensities in (a); (b); and (c) of I_a = 1E18 [W/m^2]; I_b = 4E18 [W/m^2] ; and I_c = 8E18 [W/m^2], respectively. The bottom row of Figure 3.1.2 plots the same for a fiber of half that core radius (1/4th the area) at four times those intensities in (d); (e); and (f) so that each column corresponds to the same power launched. These show that the mode patterns (hence the SF effects) clearly vary even for the same power launched (in contrast to the bulk media case). Moreover, in the top row we observe that the SF effect is to displace the field from the core into the cladding; and the bottom row shows a more rapid descent into catastrophic behavior as the intensity increases.

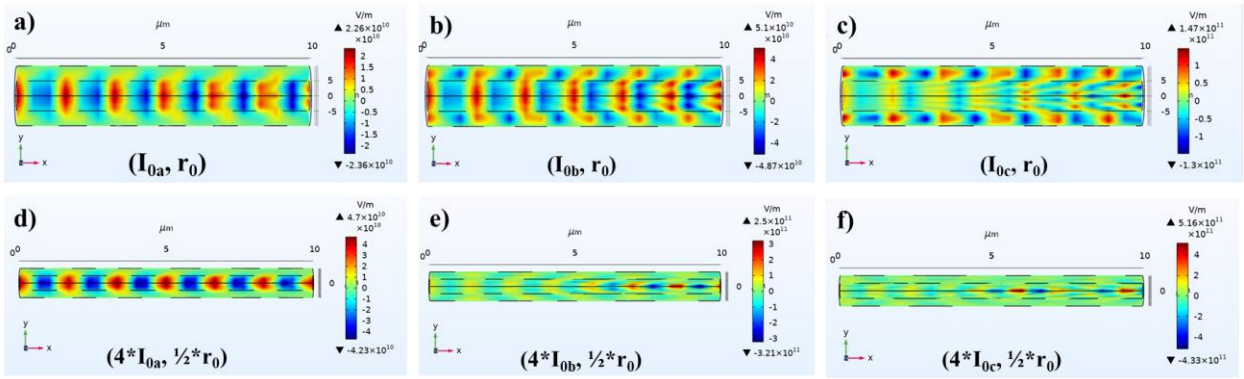


Figure 3.1.2. z-component electric field in a fiber of r_0 = 5 microns at increasing intensities in **(a)**; **(b)**; and **(c)** compared to that in a fiber of half that radius in **(d)**; **(e)**; and **(f)**.

In Figure 3.1.3 we plot the magnitude of the electric field vector for these same cases (a) – (f). These clearly show the mode confinement and the onset of filamentation. We significantly note the formation of a single filament in the case of the smaller core fiber (the bottom row) which remains near the center of the core.

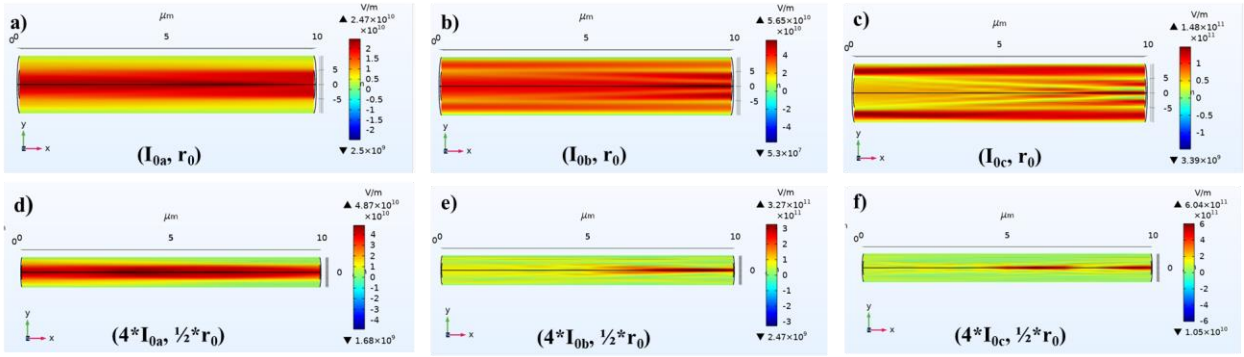


Figure 3.1.3. Electric field magnitude in a fiber of r_0 = 5 microns at increasing intensities in (a); (b); and (c) compared to that in a fiber of half that radius in (d); (e); and (f).

These results are significant in that, to our knowledge, this is the first observation of SF that is not characterized by beam power alone; and that instead it can indeed be controlled via the geometric factors within a waveguide. Filamentation is also a key issue in thermal lensing in the atmospheric propagation of high energy pulses as well as in fiber lasers (wherein the index of refraction is altered by thermal rather than nonlinear optical effects). Thus, this research has broader impacts as we begin to optimize over these parameter spaces.

3.2 WBG-PCSS Enabled Laser Diode Array Driver

(John Bhamidipati)

3.2.1 Problem Statement, Approach, and Context

Primary Problem: Need for heavy (~125 lbs.), bulky (~10 cu-ft), and expensive (~$120,000) conventional laser systems (1064 nm) in PCSS-based HPM applications, with an additional need for second and third harmonic generation (SHG/THG) optics to trigger wide bandgap (WBG) solids (GaN/SiC).

Solution Space: Design and implement a compact (~1.1 cu-ft), lightweight (10–15 lbs.), and inexpensive (<$15,000) alternative for conventional high average power optical trigger (laser) system to improve SWaP-C^2 index of HPM systems.

Sub-Problem: Unavailability of commercial-off-the-shelf (COTS) miniature optical sources with sub-nanosecond pulse widths and tens-of-μm beam width, delivering >1-Watt power to implement as a makeshift/turnkey solution for the laser system.

State-of-the-Art (SOTA): High average power picosecond pulsed lasers available up to 50 W output power with a gain factor up to 40 dB (~10,000x power) with laser amplifier.

Deficiency in the SOTA: High average power 1064-nm pulsed lasers are bulky and require auxiliary systems as well as additional optics for SHG/THG generation for WBG device triggering.

Solution Proposed: Multi-stage laser diode array/stack (LDA/LDS) driver powered by seed-laser-diode-driven avalanche WBG-PCSS as a compact, inexpensive laser replacement.

Relevance to OSPRES Grant Objective: Provides an enhanced SWaP-C^2 compliant solution for the laser (optical trigger) subsystem, with a subsequent impact on overall HPM system cost, volume, and power (optical and electrical) requirements.

Risks, Payoffs, and Challenges: Complex interconnect and thermal management system (TMS) design at high temperature (130–175°C) operation; unavailability of COTS high power pulsed laser diodes could potentially raise a need for research in laser diodes (arrays).

3.2.2 Tasks and Milestones / Timeline / Status

(A) Complete initial feasibility study for the cascaded multi-stage optical amplifier design and determine functional requirements for the laser diodes (arrays) and source driver [DEC–JAN 2020 / completed].

(B) Complete initial stage experimental implementation of the PCSS-based driver and demonstrate positive current gain using GaN-PCSS, triggered with a 404 nm laser diode. [MAY–JUN 2021 / in progress].

(C) Define performance metrics for PCSS-based driver and complete numerical calculations for required output current at each stage and corresponding PCSS (GaN/GaAs) operating voltages in light of electric fields required for lock-on/avalanche mode, establish real-time implementation timeline, cost estimates, jitter limitation, and explore ways to protect LDA from PCSS ringing. [MAR 2021 / partially complete / revisit after completing (B)].

(D) Study the feasibility of using mode-coupling in a slab geometry to bring the laser light into GaN/GaAs devices with reduced laser energy – modeled in COMSOL simulations [APR–MAY 2021 / effort transferred to subproject 3.5].

(E) Proof of concept test with a 50 Ω load at 1 kHz pulse repetition rate (PRR) [JUL–AUG 2021]

(F) Working prototype demonstration at ~MHz PRR with laser diode array/stack and ancillary optics based on HPM source driver needs including thermal management system (TMS). [SEP–OCT 2021]

3.2.3 Progress Made Since Last Report

(B) Pulse trigger requirements for the LDA/LDS have been identified based on Jenoptik's actively cooled quasi continuous wave (QCW) vertical diode laser stacks. These pulse requirements will be used to tailor device parameters for the enabling switch. COTS silicon optodiodes have been procured from Voltage Multipliers Inc. and testing is underway to verify their ability to switch >100 Amps over a high impedance strip line.

The first iteration of the SiC-MOSFET powered FWG prototype has been fabricated and testing is underway. This implements multiple 50 Ω coaxial cables with lengths between 20.8 cm and 41.6 cm to achieve a chirped propagation delay between 1–2 ns, a 7.5-cm x 6.5-cm two layered PCB with integrated Texas instruments ISO5852S gate driver and a 1.7 kV Cree/Wolfspeed SiC-MOSFET.

3.2.4 Significant Finding(s) and Mission Impact

3.2.4.1 Summary to Date

(A) The state-of-the-art COTS laser driver specifications and limitations have been comprehensively studied, and target performance metrics have been determined in terms of output current (>120 A), pulse repetition rate (>1 MHz), transient response (<200 ps risetime and <1 ns pulse width), and volume (<0.75 cu-ft). A preliminary feasibility study has signified the need for lock-on conduction mode with ~$10^{2.6}$ gain factor to drive at >1 MHz pulse repetition rate while limiting the amplification stages to 2. This reduces monetary costs to 10–12% of the conventional laser system, while achieving the expected goal of miniaturizing the optical subsystem by 90%.

(B) Pulse trigger requirements for the LDA/LDS have been identified based on Jenoptik's actively cooled (QCW) vertical diode laser stacks. These pulse requirements will be used to tailor device parameters for the enabling switch.

(C) Numerical calculations have been completed to estimate the electric fields and corresponding voltage bias required to induce lock-on operation while exploring ways to minimize the potential risks of high jitter at ~MHz order PRR switching, power reflections due to impedance mismatch and negative ringing currents during PCSS recovery. Expected on-state resistance and power dissipation for 50 μm and 100 μm devices in lock-on conduction mode have been calculated to estimate cooling system requirements while retaining the expected SWaP-C^2 factor.

(D) Kerr-induced self-focusing in silica fibers has been studied to understand laser beam characteristics and to deliver optimal light into the PCSS at reduced energy. Initial results were inconclusive due in part to difficulties in distinguishing multi-mode effects from nonlinear effects. Eliminating the nonlinear parameter, mode-coupling study was conducted on dielectric slabs separated by sub-μm order gap via COMSOL. Simulations have been performed for SiO_2-over-SiO_2 and SiO_2-over-GaN dielectric slabs with 0.1-μm air gap. Better mode coupling has been seen in SiO_2-over-GaN geometry at airgaps ≤0.1 μm. However the simulation results showed induction of higher order modes and phase shifts raising a need to quantify the phenomena mathematically.

3.2.4.2 Since Last Report:

(B) Initial testing of GaN-PCSS grown over SiC substrate has shown linear conduction with 355 nm optical trigger at 18 kV/cm. Non-linear operation has not yet been demonstrated experimentally. However, considering the device availability, cost, and long-term supply-chain sustainability factors, project scope has been expanded and switching technologies such as silicon avalanche switches (SASs), GaN-FETs, silicon

opto diodes, and topologies such as frozen wave generators (FWGs) are being considered alongside GaN-PCSS to drive the LDA/LDS. On the other hand, input pulse requirements for the COTS LDA/LDS have been identified based on Jenoptik's QCW laser diode stacks so that the switching device parameters can be tailored accordingly.

3.3 Diode-Based NLTLs

(Nicholas Gardner)

3.3.1 Problem Statement, Approach, and Context

Primary Problem: The size, weight, and cost of pulse forming/shaping networks (PFNs) need to be reduced and optimized for Navy afloat missions.

Solution Space: Develop a lumped-element nonlinear transmission line (LE-NLTL) as a pulse shaping network for the conversion of energy to the ultra-high frequency (UHF) band at single MW peak power.

Sub-Problem: Metrics used for component selection are designed for LE-NLTLs operating at sub 0.1 GHz frequencies. Using such metrics alone to design LE-NLTLs capable of single GHz frequency generation introduces a trial by error nature to the design process wherein frequency/power generation predictions and measurements can differ by a few hundred MHz or the design potentially fails to operate at all.

State-of-the-Art (SOTA): LE-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit. Simulations of LE-NLTLs indicate achievable frequencies in the single GHz range.

Deficiency in the SOTA: Simulation/measurement agreement becomes increasingly sensitive to parameters and factors outside of inductive and capacitive element choice alone at frequencies above ~100 MHz. Disparities between measurement and simulation above contribute to a trial by error design process for LE-NLTL networks.

Solution Proposed: Identify and characterize diode parameters affecting frequency generation in the context of a NLTL application and identify limits/desired ranges required for UHF generation. Such parameters include, but are not limited to: diode frequency response, diode reverse bias hold-off voltage, diode small signal capacitance, diode chip/package parasitics, and diode relaxation time. The improved understanding of the explored parameters will be used to design and fabricate a LE-NLTL capable of GHz center frequency generation at single MW peak powers.

Relevance to OSPRES Grant Objective: The SWaP-C^2 capabilities of LE-NLTLs (shown in Figure 3.3.1) represent a potential solution to the size, weight, and cost optimization issue for PFNs on Navy afloat missions.

Figure 3.3.1. 20 cell LE-NLTL of dimensions 1.1 x 23.45 cm constructed with COTS components.

Risks, Payoffs, and Challenges: There exists a potential tradeoff between power and frequency generation. Devices such as ceramic capacitors may be used in a LE-NLTL to generate high peak power due to their break down potentials in the 10s of kV, however, such devices become highly resistive at 0.1–0.2 GHz frequencies. Diodes have been shown to be operational at frequencies upwards of 0.4 GHz, however, possess low hold-off potentials limiting peak output power. The payoff to overcoming these challenges is significant reductions in PFN size and cost.

3.3.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Construct/demonstrate a prototype capable of UHF generation at low voltages (1–100 V excitation amplitude)

(A1) Break a low-voltage pulse into a sequence of solitons (SEP20)
(A2) Increase frequency generation past 200 MHz (NOV20)
(A3) Select diode candidate (junction capacitance <50 pF) and simulate expected results (Ongoing JUN21)
(A4) Design/fabricate/test line (Ongoing JUL21)

(B) Milestone – Demonstrate tuning of waveform at low voltages using electrical or mechanical means (**Completed with voltage biasing APR21**)

(B1) Simulate a topology capable of biasing the diodes using a DC voltage (Completed JAN21)
(B2) Perform Initial tests and refine prototype to reduce loss (Completed FEB21)
(B3) Show electrical tuning with a positive DC bias (Completed MAR21)
(B4) Show electrical tuning with a negative DC Bias (Completed APR21)

(C) Milestone – Construct/demonstrate a prototype capable of frequency generation above 1 GHz at single MW peak powers (Completed MW peak power but not GHz center frequency – Ongoing)

(C1) Identify diode candidates with a hold-off voltage of several kV and a low signal junction capacitance under 100 pF (Completed JAN21)
(C2) Design/fabricate single diode prototypes (Completed JAN21)
(C3) Perform initial tests using half-barrel pulse source (Completed FEB21)
(C4) Refine simulation using measurements (Completed FEB21)
(C5) Test a prototype using two diodes in series (Completed FEB–MAR21)
(C6) Test lines with pulses of varying characteristics to determine line behavior (**Ongoing JUN21)**
(C7) Test lines using Marx Generator as a source (**Ongoing JUN21**)
(C8) Test lines using PCSS based source (**Ongoing JUN21**)
(C9) Use simulations and tests to refine line for increased frequency generation (**Ongoing JUN-JULY21)**

(D) Milestone – Demonstrate power scalability using an array of LE-NLTLs (**Ongoing**)

(D1) Design a prototype capable of running two D-NLTLs simultaneously off of the same excitation pulse (**Ongoing JUN21**)
(D2) Build a circuit capable of measuring the CV curve of low voltage diodes and measure the CV curves of unused diodes and heavily used diodes (**Ongoing JUN21**)

3.3.3 Progress Made Since Last Report

(C) Tests were performed on the K50F HV D-NLTL line utilizing the Megaimpulse (MI) as a source with plans in place for tests using a PCSS-based source as well as a Marx Generator. Measurements and results are described in further detail in section 3.3.4.2 and figure 3.3.2.

(D) Initial designs for a line capable of running two D-NLTLs with the same pulsed source, and a CV curve measuring circuit were drawn up and simulated. The parallelization circuit is described in more detail in section 3.3.4.2 and figure 3.3.3. Both topologies are currently being drawn up in CAD to produce PCBs and will be utilized to observe the effect of variations on line behavior and determine if D-NLTLs can be effectively parallelized for an array-like set up.

3.3.4 Significant Finding(s) and Mission Impact

3.3.4.1 Summary to Date

(A) After a failure of the high-voltage diode-based nonlinear transmission lines (D-NLTLs) to reproduce simulated results, work refocused on low-voltage D-NLTLs to determine the source of the discrepancy. In NOV2020 a center frequency of ~250 MHz was achieved using a D-NLTL design based on the diode model SMV1702.

(B) Following the success of the SMV1702 D-NLTL, a circuit was designed capable of electrically tuning the center frequency utilizing DC biasing of the diodes. In FEB-APR2021 the circuit demonstrated a linear relationship between DC bias up to a limiting potential. Negative DC biases decreased center frequency while positive DC biases increased center frequency.

(C) In JAN2021 two diode candidates (models K100F and K50F) were identified for a HV D-NLTL design. FEB2021 saw successful tests of both D-NLTLs with each sharpening the rise time of a pulse produced by a DSRD based source down from ~1 ns to ~600 ps.

(D) During MAY2021 a line topology capable of feeding two identical D-NLTLs with the same pulsed source at the same time. Initial results were collected, and a prototype is currently being designed to test the ability to parallelized D-NLTLs.

3.3.4.2 Since Last Report

GHz MW D-NLTL prototype (C): Utilizing the MI as a source for the D-NLTL serves two purposes: first to display a characteristic of D-NLTLs, and second to show simulation–measurement agreement. Figures 3.3.2a and 3.3.2b display the waveform generated by the MI and D-NLTL respectively. The degradation of the pulse amplitude and rise time

caused by the D-NLTL is due to the low pass filter characteristic of the shunt capacitance and series inductance used to construct the D-NLTL. The MI source has a rise time of ~100 ps indicating the waveform has a much larger maximum frequency than the D-NLTL can pass through it. Any frequency above the ~1.67 GHz max frequency of the D-NLTL is filtered to ground as shown by the FFT in 3.3.2d. 3.3.2c shows the agreement between the measured and simulated waveform produced by the D-NLTL, further supporting the need to utilize the diode series inductance and parallel capacitance for proper simulation. Properly simulating the line behavior is critical for device selection and line design.

Power Scaling (D): Power scaling D-NLTLs in an array set up represents a possible method of increasing the peak power output of the networks. For such an array to function properly, each D-NLTL needs to produce an identical waveform and each waveform must reach the load at the same time. To determine the sensitivity of a D-NLTL waveform to network variations, a design was drawn up in SPICE capable of running two lines off the same input pulse. Figure 3.3.3a shows the behavior if both lines are identical, 3.3.3b shows the result if the lines have small variations, and 3.3.3c shows the result if the lines have large variations. The prototype will be designed to have two different termination set ups: one where each line terminates on separate loads, and one where both lines terminate on the same load. If D-NLTLs are able to be parallelized some of the peak power issues presented by the devices can be mitigated.

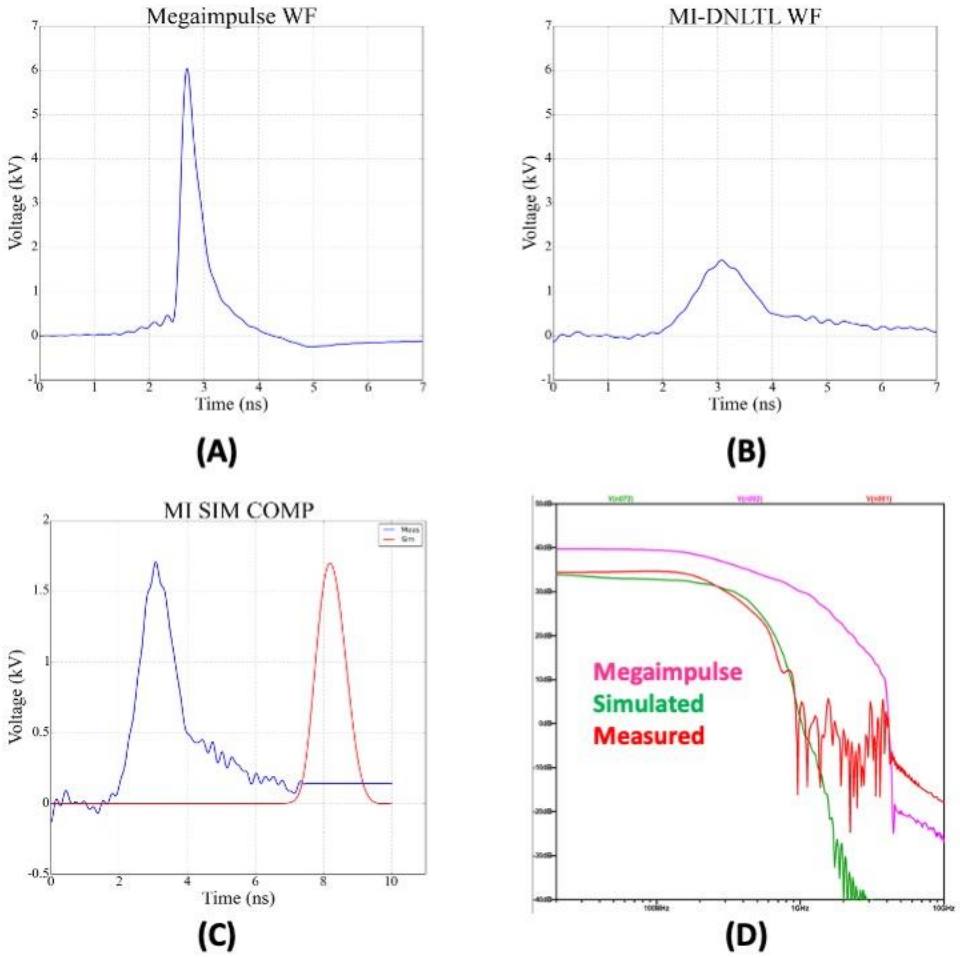


Figure 3.3.2. Results from a test of using the D-NLTL in conjunction with the MI source. (A) Waveform produced by MI. (B) Waveform produced by D-NLTL. (C) Comparison between measurement and simulation. (D) FFT of MI, measured D-NLTL, and simulated D-NLTL waveforms.

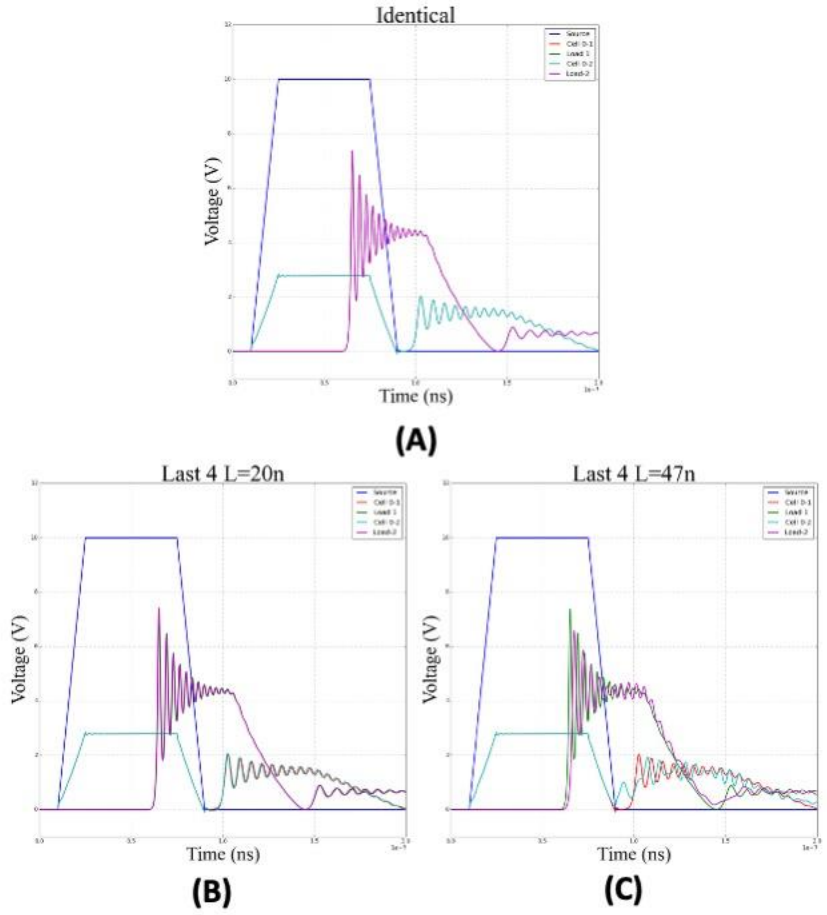


Figure 3.3.3. Simulated example waveforms for the parallelization tests. (A) Expected measurement results if lines behave identically. (B) Expected behavior if the lines have a slight variation. (C) Expected behavior if the lines have a large variation.

3.4 Si-PCSS Top Contact Modeling and Optimization for Cooling Requirements

(Jay Eifler)

A summary report is currently being prepared for this section.

3.5 GaN:C PCSS Direct RF Modulation

(Heather Thompson)

3.5.1 Problem Statement, Approach, and Context

Primary Problem: Need for a more compact, cost-effective RF pulse generation system for Navy afloat missions on smaller vessels and vehicles.

Solution Space: Improve efficiency and reduce necessary material, size, and thermal requirements by utilizing gallium nitride (GaN) in PCSSs through exploitation of its

theoretical material properties which allow for higher operating voltages, frequencies, and temperatures, while also eliminating the need for pulse-shaping transmission lines through direct RF modulation using the laser/photon source driving the PCSS.

Sub-Problem: Lack of maturity in compensated gallium nitride semiconductor (i.e., GaN:X with X=C,Fe) PCSS manufacturing, development, and optimization.

State-of-the-Art (SOTA): Si-based PCSS with >10 kV operational voltage, cooling system capacity of 500 W/cm^2, and theoretical breakdown of 1.3 MW/cm.

Deficiency in the SOTA: Si-based technologies requiring ~100 µJ optical pulses per 4 MW of RF output power, increasing the laser energy (per pulse) required for device triggering; long recovery time (ones-of-µs), limiting quick opening and high pulse-repetition-rate operation along with increased heating in the PCSS; critical electric field of 0.3 MV/cm, leading to devices that are ones-of-cm^2 in area for the target peak power; and operating temperature of <160°C, leading to increased cooling requirements.

Solution Proposed: Replace Si-PCSS device with GaN:C utilizing direct RF modulation — eliminating the need for a bulky pulse-forming transmission line (~3 ft long) — capable of handling >3 MW (peak power) with ~20 µJ of incident optical energy, device area <1 cm^2, and operating temperature ~500°C (theoretical temperature which will be limited by circuit components and solder).

Relevance to OSPRES Grant Objective: Reduction in size and cost for cooling system that prevents damage to the PCSS device and components along with eliminating need for a bulky pulse-shaping system, as well as decrease in material cost and needed incident laser energy, leading to enhanced SWaP-C^2 capability with greater modularity and scalability.

Risks, Payoffs, and Challenges: Due to manufacturing limitations, GaN PCSS devices tend to be limited to lateral geometries (both contacts on the top side of the device), limiting operating voltage due to current crowding and surface flashover. The recovery time (ones-to-tens-of-ns) may lead to device heating and increased DC, or zero-frequency, component when generating RF with a period on the same order as the recovery time.

3.5.2 Tasks and Milestones / Timeline / Status

(A) **Jan-April 2021** Demonstrate RF unipolar modulation in the 1–2 GHz regime and up to 2 kV operating voltage with current PCB setup and automated optical delay system. Achieving 2 kV operating voltage should allow for preliminary effects testing before (or in conjunction with) striving towards higher operating voltages. **Ongoing**

(B) **Start April 2021** Demonstrate RF bipolar modulation using an advanced test setup with two GaN:C PCSSs triggered using the same optical delay, but with the second device connected to a negative power supply.

(C) **Start April 2021** Achieve higher center frequency content in unipolar and bipolar modulation by using a faster (rise-time and pulse-width) laser to activate GaN:C PCSS.

(D) **Start May 2021** Complete study of recovery for differing gap lengths, incident energies, and operating voltages and find solutions to reduce the recovery time.

(E) **March-June 2021** Complete study on the feasibility of using mode-coupling to bring the laser light into GaN:C devices, allowing for a possible reduction of laser energy, and pulse shaping within the laser-coupler/GaN:C composite structure.

3.5.3 Progress Made Since Last Report

(E) Mode-coupling modeling continued using COMSOL, and single-mode waveguide operation was successfully demonstrated. This model will be built upon to observe how mode-coupling between fiber and GaN:C can be done to continue towards showing the feasibility of coupling optical fiber and GaN:C PCSS for direct RF modulation using the incident photon source to reduce the needed incident laser energy and overall system form factor.

3.5.4 Significant Finding(s) and Mission Impact

3.5.4.1 Summary to Date

(A) Towards showing direct RF modulation in the 1–2 GHz range, unipolar modulation has been demonstrated using an open-space time-optical delay using one GaN:C PCSS (lateral device with 500 μm gap length) of up to 1.2 kV charge voltage. The limiting factor to achieving higher charge voltage was flashover occurring in air-bubbles formed during curing of the Sylgard encapsulant. Previously, ~1.8 kV charge voltage was achieved using a 1 μm gap length GaN:C PCSS, so demonstration will continue using similar methods (corona-dope) to the Si-PCSS studies to achieve 2 kV+ charge voltage, with this being limited by the power supply being used to 2.5 kV.

(E) To continue towards a feasibility test of fiber coupling with GaN:C PCSS, single-mode waveguide modeling was initiated in COMSOL. This initial model will be modified to show optical fiber coupling to GaN:C PCSS.

3.5.4.2 Since Last Report

(E) To show the feasibility of using optical fiber coupling with GaN:C PCSS for the reduction of needed incident laser energy and direct RF modulation through incident pulse modulation, simulations were built using COMSOL. For an initial study, we wish to show how the coupling between two waveguides changes as a function of the distance between the two guides (separated by an air gap). Problems arose previously in our ability to achieve single-mode waveguide operation. We resolved these problems (mesh and input boundary condition issues) so that we now observe single-mode operation, as demonstrated in Fig. 3.1.1 for a circular-core optical fiber. In Fig.3.5.1 (a) we plot the magnitude of the electric field vector, which clearly shows confinement, and In Fig.3.5.1 (b) we plot the z-component of the electric field vector, which clearly shows the mode pattern.

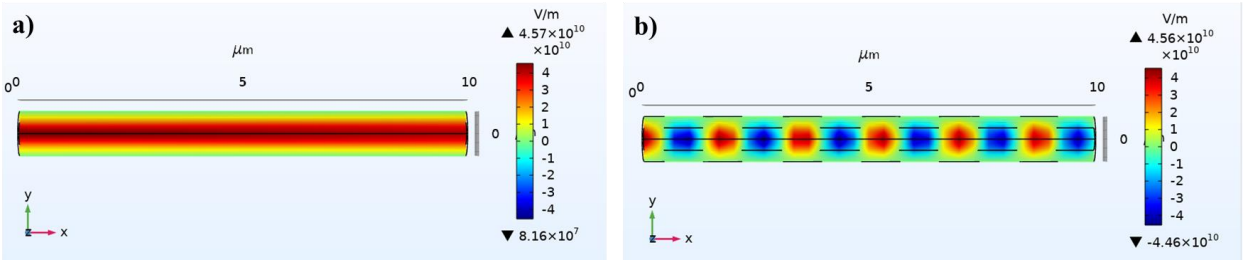


Figure 3.5.1: Demonstration using COMSOL of single-mode waveguide operation of a circular-core optical fiber with a) being the magnitude of the electric field, and b) the z-component of the electric field.

The mode pattern spacings closely match a simple dielectric slab approximation model, to which we fit a Gaussian approximation of the fundamental mode before launching it from the left boundary (at the input to the fiber). This model will be built upon to continue the study of mode coupling from fiber into a GaN:C PCSS.

3.6 Drift-Step Recovery Diode and Pulse Shaping Device Optimization

(Jay Eifler)

3.6.1 Problem Statement, Approach, and Context

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS but do not require a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times requires optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening device within the pulse shaping head circuit. Additional goals for pulse repetition frequency are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies. Also optimize the pulse sharpening device (PSD) within the pulse shaping head circuit.

Sub-Problem 1: TCAD and SPICE models of the DSRD are 40% accurate and must be improved. PSD models have not been developed.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetimes have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current. PSD have sharpened DSRD pulses to 100 ps-order.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or

sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power and minimum risetime, but also for low-jitter, reduced cooling, and compactness. Additionally, optimize pulser with PSD and pulse shaping head circuit.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2 cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities. DSRD and PSD must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD and PSD modeling.

3.6.2 Tasks and Milestones / Timeline / Status

(A) Develop accurate models for DSRD (TCAD and SPICE models are 40% accurate)

(A1) Develop accurate DSRD TCAD models / JAN–APR 2021 / Completed.

(A2) Develop accurate SPICE models / MAR–JUN 2021 / Discontinued.

(A3) Develop parasitic capacitance, inductance, and resistance models for single die and stacked DSRD and the DSRD-based pulser circuits. / MAR–JUN 2021 / Discontinued.

(B) Explore TCAD modeling to advance DSRD research using available DSRD models

(B1) Study carrier lifetime effect on risetime / FEB–APR 2021 / Completed.

(B2) Avalanche and device operation study / FEB-MAY 2021 / Avalanche models limit peak power and risetime but do not correspond to experiment and must not be included or included and improved and calibrated to experiment.

(B3) Study effect of the width of outer edge contact on current density and breakdown in device. / MAR–MAY 2021 / Discontinued.

(B4) Begin TCAD process modeling in Silvaco Athena and Victory Process of diffused and epitaxial processes for DSRD (and pulse sharpening device) fabrication and DSRD device modeling. / MAR–JUNE 2021 / Completed.

(B5) Determine optimal doping profile for Semiconductor Power Technologies (SPT) DSRD epitaxial designs. / MAY–JULY 2021 / Exponential doping profiles produced the best device performance. Ongoing effort.

(C) Pulse sharpening device (PSD) modeling

(C1) Begin TCAD modeling of PSD / DEC 2020 and APR–JUN 2020 / (a) Preliminary PSD research begun replicating published work but further work to continue. (b) More standard PSD device modeled in TCAD than as used in published work. (c) PSD simulated with DSRD 3-stack for more complete DSRD-based system modeling excluding only the primary switch model. Discontinued.

(C2) Determine current carrying capacity of PSD and stacks / MAR–JUN 2021 / PSD literature review begun. Discontinued,

(D) Receive and study DSRD-based pulser circuit topologies in SPICE with the DSRD and primary switch SPICE models. / MAR–APR / LTSPICE code and models received and understood. Completed.

3.6.3 Progress Made Since Last Report

(A1) An accurate DSRD TCAD model was developed by including both carrier–carrier scattering and Selberherr breakdown models. A 2D parameter study of varying DSRD areas and stacks of DSRD single dies has been carried out with the accurate DSRD model. The peak voltages obtained were shown to be much closer to experimental pulse data than earlier TCAD models. Subsequently, published work was found replicating the models and their accuracy when compared to experimental pulse data [1]. To better match experimental pulse data, improved primary switch models for TCAD simulation and inclusion of circuit parasitics will be necessary. This progress has been previously reported in the Spring 2021 UMKC OSPRES Grant Review and Technical Exchange.

(B5) Exponential doping profiles have been determined to have the best overall device performance for minimum doping of 5×10^{13}–1×10^{14} dopant atoms/cm^3. Device thickness of either 170 μm or 200 μm was found to have minimal effect on performance and moderately deeper junction placement as well had minimal effect. 200 μm thick devices were found to have 510 V higher breakdown as assessed in actual transient DSRD operation within a pulser circuit. In addition, leaving substantial amounts of highly doped substrate on the device was found to minimally effect performance, which confirms this manufacturing practice for increasing device ruggedness.

3.6.4 Significant Finding(s) and Mission Impact

3.6.4.1 Summary to Date

DSRD TCAD simulation started by replicating published TCAD DSRD results and then simulating devices similar with actual in-house DSRD. The variation of the sinewave pulse voltage input magnitude and period on DSRD charge storage were collected. Charge storage timing (when the diode empties charge stored from forward pulsing) of ~50% was achievable with sufficiently long voltage input period which is necessary for maximum reverse current cutoff.

DSRD stacks, as opposed to individual die DSRD, were simulated showing reduced risetime from single die to 5-stacked DSRDs consistent with published and earlier in-

house data. Series resistance to model metal resistance between DSRD in stacks and doping variability in stacks was also modeled in TCAD showing metal resistance must be large to have an impact on peak voltage and risetime and that doping variations proportionally effect risetime.

(A1) Accurate DSRD TCAD models have been developed that include both carrier-carrier scattering and Selberherr breakdown and are suitable for DSRD operation below the dynamic breakdown threshold. Peak voltage and risetime were limited by the breakdown model and more closely match experimental pulse data.

(A2) Work on DSRD SPICE models has been done for the primary switch model (MOSFET) with conversion of the code to TCAD SPICE being partly completed to allow for modeling the complete DSRD-based pulser system (except driver).

(B1) DSRD risetime performance was collected from TCAD simulations for variable carrier lifetime. Changes in lifetime had no significant effect on risetime other than the output pulse starting earlier.

(B2) DSRD peak voltage and risetime were simulated in TCAD to include avalanche modeling or not. TCAD avalanche models limited peak voltage and risetime at the load over a range of voltage input magnitudes. A TCAD parameter study for DSRD stack height and DSRD area for several doping profiles with and without avalanche modeling was performed (Spring 2021 UMKC OSPRES Grant Review and Technical Exchange). The avalanche model and model parameters were also modified to account for dynamic breakdown rather than static and then compared to the no avalanche case and experimental data. From the improved avalanche modeling and TCAD parameter study, the optimal area of the DSRD can be obtained. However, for the 500 V voltage input magnitude used, the DSRD output were all in breakdown and are not predictive of non-breakdown behavior. Future studies for optimal area will include a range of voltage magnitudes to study DSRD performance and breakdown.

(B4) TCAD process and device modeling for the development of process steps and their resultant doping profiles and device operation was begun. This modeling will enable a connection between the fabrication parameters and the device operation for DSRD (and PSD).

(B5) Exponential doping profiles were shown (via TCAD) to outperform Gaussian and error function profiles slightly. For exponential profiles had an optimal minimum doping of 5×10^{13}-$1x10^{14}$ dopant atoms/cm3, while Gaussian and error function profiles had an optimal minimum doping of 1×10^{13}-5×10^{13} dopant atoms/cm3.

(C1) Pulse sharpening has been verified for PSD devices for the standard design and another non-conventional design. The PSD was also modeled within a DSRD-based pulser circuit combining for the first time TCAD modeling of both DSRD and PSD together within the same circuit with only the primary switch model not included.

3.6.4.2 Since Last Report

(B5) To properly assess DSRD performance, three methods were compared. One method included adding a series resistance (~1–3 ohms) with the DSRD to lower the current and another method included adjusting the peak voltage to values seen in experiment (~4 kV). Adjusting the series resistance allowed the peak voltage to be calibrated but produced a long voltage prepulse tail not consistent with experiment. However, the addition of a series resistance shows that adding parasitics for the DSRD, circuit components, or representative of the PCB board and traces can change the DSRD output pulse from one dominated by IMPATT oscillations to the expected smooth peaked output pulse. The original method included a sinewave voltage input pulse with magnitude of 500 V and 200 ns in period but produced output pulses mostly dominated by IMPATT oscillations making use of the DSRD performances metrics (peak voltage, risetime, voltage riserate, maximum reverse current, pulse width, and prepulse height) ineffective. A third method of lowering the voltage input magnitude to lower than used in the experiments produced output pulses that allowed comparison of performance for different DSRD device models (varied doping profiles, thickness, area and stacking).

The use of the third method allows assessment of DSRD performance without avalanche effects interfering, but the use of varied voltage input magnitudes allows breakdown to be studied within the transient operation of the DSRD in an inductive pulser circuit design as well. Circuits including more realistic primary switch models have begun using a simple voltage-controlled switch within SPICE as well as SPICE and TCAD MOSFET models.

A variety of DSRD doping profiles have been simulated in TCAD for performance in the design of SPT epitaxial DSRD. Linear, Gaussian, error function, abrupt and exponential doping profile function types were examined. The peak voltage performance is shown in Figure 3.6.1. Exponential doping profiles proved to perform the best and are not possible with diffusion profiles (Gaussian and error function). The minimal doping at the PN-junction for best device performance with exponential doping was 5×10^{13}–1×10^{14} dopant atoms/cm^3. Both Gaussian and error function profiles performed nearly as well at minimum doping of 1×10^{13}–5×10^{13} dopant atoms/cm^3. The difference is due to the exponential doping profiles having a steeper gradient and wider region of lowering doping all producing a wider depletion zone. Linear and abrupt profiles performed less well. Further doping studies are being completed for variations in maximum doping of the p and n-sides, junction placement, and undoped base widths effect on device performance.

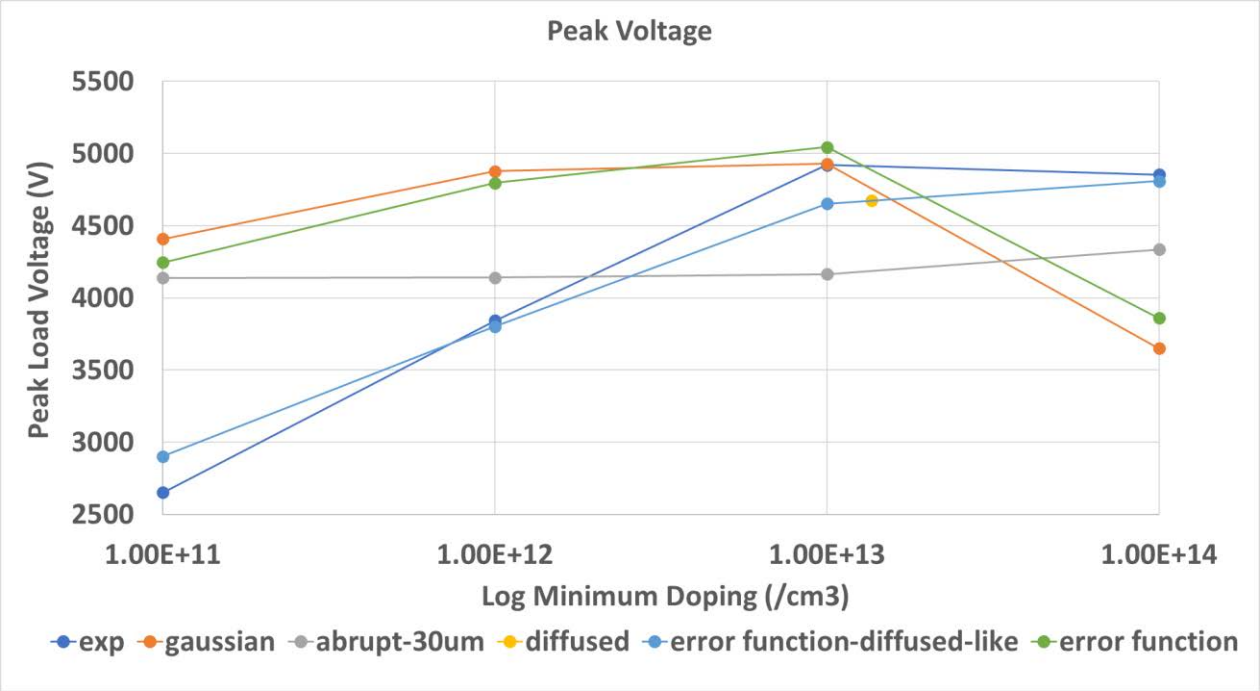


Figure 3.6.1. Peak voltage DSRD performance for a variety of doping profile types over a range of minimum PN-junction doping levels. Gaussian and error function profiles have similar curves, while exponential profiles and the profiles imitative of an earlier optimal diffusion profile have similar curves. The abrupt profile underperformed.

The thicknesses of 170 μm and 200 μm devices for device performance were compared in TCAD simulation due to the high cost of thicker epitaxial designs. It was found that this difference in device thickness had minimal effect within the optimal minimum doping range of exponential doping profiles. The use of 170 μm thick devices reduces cost of epitaxial designs and has been shown not to significantly reduce performance within the voltage input magnitude well below breakdown. In another TCAD study, 200 μm thick devices were shown to have a 510 V higher voltage breakdown than 170 μm thick devices. However, experimental lab testing of DSRD within pulser circuits has not shown breakdown effects for the voltages and input periods used to drive the circuits. Pushing the DSRD and pulser circuits designs to the limits of their capability for peak power and risetime would require understanding the breakdown limits.

Breakdown models including non-local models were performed in TCAD and showed, as expected, that local models over-estimate impact ionization. Adjustment of the impact parameters to 1.2 times the B_n impact parameter values were also performed and lowered the effect of impact ionization. However, neither of these models improved matching experimental and simulation results since they increase peak voltages in simulation to greater than that seen in experiment. Matching the results will require improved modeling of the primary switch and circuit parasitics, at which point, improved breakdown models may prove necessary.

The DSRD epitaxial devices are fabricated on highly doped Arsenic substrates which can be ground off after epitaxy. Leaving on some of the substrate helps to produce mechanical rigidity and prevents damage to the DSRD. TCAD simulations were used to assess the effect of additional substrate on the device performance. It was found that DSRD performance was minimally affected by the additional highly doped substrate. There are some suggestions for GaN devices that the additional substrate can lower the breakdown voltage and additional TCAD simulations will be performed to determine this, although initial simulations do not suggest much of an effect.

Published work [1] for including circuit parasitics to match experimental measurements to TCAD/SPICE simulation were replicated. A combination of accurate DSRD, primary MOSFET switch, and circuit component and PCB parasitics will be required to match experimental pulse measurements to TCAD simulations and to apply simulation results to design and optimization of DSRD and DSRD-based pulser systems.

3.6.5 References

[1] Lyublinsky, A. G., E. I. Belyakova, and I. V. Grekhov. "Numerical and Experimental Study of an Optimized p-SOS Diode." *Technical Physics* 64, no. 3 (2019): 373-379.

3.7 SOS-based Pulsed Power Source Systematic Topological Optimization

(Sourov Roy)

3.7.1 Problem Statement, Approach, and Context

Primary Problem: Semiconductor opening switch (SOS)-based pulse generators using inductive energy storage (IES) and release topologies able to produce ones of gigawatts in ones of nanoseconds are traditionally large and bulky, and suffer from low volumetric power densities rendering them impracticable for Navy afloat missions.

Solution Space: Through a combination of numerical and experimental efforts, systematically develop a modular architecture of SOE-IES pulser circuit—by determining the optimal permutation of series and parallel combination of stage(s) within the base SOS-IES pulser (and components utilized)—which maximizes the peak voltage, peak power, and volumetric power density achieved without sacrificing the desired nanosecond risetime of the pulses generated.

***Sub-Problem 1*:** Availability of viable SOS diodes, specifically p^+-p-n^+ silicon diode structure versions (i.e., Drift Step Recovery Diodes, or 'DSRDs' consistent with those discussed in Section 3.6), are in limited production, minimal supply, and are traditionally manufactured OCONUS; therefore, are difficult to procure. This leads to utilizing non-ideal diodes within the pulse generator circuit causing decreased performance.

Sub-Problem 2: A reciprocal relationship exists between the performance of the SOS-IES circuit (specifically, the components utilized), and the diodes performance characteristics. Hence physicomathematical modeling of this process requires

simultaneously solving the Kirchhoff equations for pulse generator's circuit containing the diodes, the continuity equation for the free carrier's recombination within the diode, and determining the electric field generated using the Poisson equation. Therefore, optimizing at the device level (e.g., doping profile & concentration) affects the impulse signal output. Conversely, an optimized circuit topology may require alterative components (e.g., differently valued inductors, and capacitors) which, in turn, affects the performance of the diodes themselves.

Sub-Problem 3: Another problem is finding the optimal permutation of the SOS-IES storage and release topology and its key component parameters which produces the highest peak power output, lowest rise time, and highest efficiency given theoretical and real-world constraints. Tradeoffs within the circuit component value's and topology permutation's tradespace exists which lead to competing optimal performance requirements. Compounding this issue, exploration of existing theoretical models which aid in simulation techniques to evaluate the performance tradeoffs is limited. Therefore, most of this work aims to determine the best-case configurations of SOS-IES topology by maturing a suitable predictive model for the SOS-IES modular architecture for a given performance matrix.

State-of-the-Art (SOTA): Large SOS-IES pulse generators ($\geq$ 1-m^3, $\geq$ 300-kg) which are comprised of sixteen parallel-branches, each containing four series-connected stacks (V_{max} = 130-kV, surface area ~20-mm^2), have demonstrated reverse pumping currents of 25-kA with an injection time of 400-ns to produce 400-kV pulse amplitudes with full-width half-maximum (FWHM) values of 60-ns produced across a 100-Ω load; a voltage gain factor of ~3 (i.e., power amplification level ~9.5-dB). Pulse repetition frequencies up to 4-MHz have also been produces across similar load values. Smaller versions (equivalent in size to the pulse generators developed for this effort, i.e., ~0.01-m^3, ~2-kg) are able to achieve 6-kV, 200-ps rise time, and < 500-ps FWHM across a 50-Ω load.

Deficiency in the SOTA: Large SOS pulse generators which can achieve the foregoing performance parameters are traditionally limited by mechanical design constraints (onboard itinerant vehicles) and power supply limitations, are large (case lengths < 1-m) and require transformer oil for cooling purposes with lead to undesirable system mass values up to 300-kg. The smaller air-cooled versions are limited to PRF < 15-kHz. Additionally, a comprehensive study on SOS generators aiming to achieve maximum gain and efficiency (reducing thermal load) through optimizing the number and ratio of parallel-branches and series-connected stages is missing in the SOTA.

Solution Proposed: Systematically determine topological configurations and values for the components thereof, that would seek a maximum in gain and efficiency, for that parameter space. Generate an optimization algorithm such as genetic algorithm or machine learning algorithm to build a suitable predictive model for this SOS-IES topology.

Relevance to OSPRES Grant Objective: SOS-IES pulse generators can remove the need for photo-triggered switches and their laser sub-systems. They are ideal for triggering sub-nanosecond rise-time sharpeners (SAS, D-NLTL, etc.), reducing overall cost, volume, and weight.

Risks, Payoffs, and Challenges:

Risks: SOS diodes — including their availability — which possess optimal doping profiles which facilitate the recombination of free carriers (electron/hole pairs) may limit the permissible injection time (pumping) of the switch, therefore time energy is accumulated within, thus limiting the reverse current amplitude during extraction time. This, in turn, may lead to devices with sub-optimal performance to be used in both, the genetic algorithms developed, and the experimental apparatuses generated, ultimately leading to spurious conclusions regarding ideal topological circuit configurations with 'N' number of series-connected stages, each containing 'M' parallel branches.

Payoffs: Leveraging cooperate partnerships with U.S.-based manufacturing of SOS diodes, the ability to refine and control the performance characteristics of the SOS devices themselves, along with the ability to simulate and manufacture the SOS pulsers in-house, enables a holistic soup-to-nuts capability to optimize, produce, and evaluate these nanosecond pulse generators.

Challenges: Determining the superlative ratio of design and development (through numerical analysis) to the effort put towards experimental construction and evaluation of the SOS pulser is challenging due to the novelty of the approach. The complexity of the theoretical model is extreme given the M×N number of stages within the pulse forming network. SPICE circuit simulation software algorithms possess computational convergence difficulties caused by abrupt changes in capacitance, inductance, and impedance. SOS diodes are non-autochthonal to SPICE software's databases thus are only approximated by equivalent combinations of circuit elements. Additionally, the variable time step imbedded in SPICE algorithms exacerbates this convergence issue. This summates to the existing discrepancy when comparing existing experimental data to that of simulated values.

3.7.2 Tasks and Milestones / Timeline / Status

To address the primary problem and meet the solution's objects proposed, two major parallel-path efforts for this work are distinguished as follows: (1) progressively and systematically iterate, through construction and experimental evaluation, permutations of the SOS pulse generator through increasing $M \times N$ stages towards increasing peak voltages, efficiencies, and gain without compromising risetime and pulse width; and (2) generate an optimization algorithm which produces a suitable predictive model for the SOS-IES topology permutations.

The first effort's milestones, and tasks to achieve them along with a timeline to do so, is as follows:

(A) Milestone – Construct/demonstrate a 2×2 SOS pulse generator prototype capable of producing $\geq$ 4-kV peak voltage, $\leq$ 1-ns risetime, $\leq$ 5-ns FWHM, $\geq$ 320-kW peak-power, $\geq$ 1-kHz PRF, $\geq$ 100 shots-per-burst, $\geq$ 5 number of bursts [*Estimated completion by JUL'21*].

1. Task – Perform literature review on SOS-IES generators and undergo training on in-house-developed DSRD-based generators developed to-date [*APR—MAY'21*];

2. Task – Develop and simulate (using LTSPICE software) circuit topology to include electrically-optimal (not mechanical) layout considerations and components within Altium [*Completed MAY'21*];
3. Task – Order and populate PCB [*Completed JUN'21*];
4. Task – Evaluate gate-drivers' performance and single-pulse performance output in terms of peak voltage amplitude, risetime, FWHM, and shot-to-shot variability [*Completed JUN'21*];
5. Task – Perform PRF, ranging from 100-Hz to 100-kHz, study to evaluate pulse generator's PRF handling capabilities and pulse outputs' standard deviation [*Completed JUN'21*];
6. Task – Process and analyze waveform data acquired, compare to LTSPICE simulations, provide results to TCAD simulation team, formulate strategy to integrate into machine learning algorithm [***Ongoing JUN'21***].

(B) Milestone – Construct/demonstrate a 4×2 SOS pulse generator prototype capable of producing $\geq$ 12-kV peak voltage, $\leq$ 1-ns risetime, $\leq$ 5-ns FWHM, $\geq$ 2-MW peak-power, $\geq$ 1-kHz PRF, $\geq$ 1,000 shots-per-burst, $\geq$ 500 number of bursts [*on hold until Milestone A is completed*].

1. Task – Work with TCAD simulation team (see Section 3.6) to compare-to, revise/update diode simulation model towards achieving refined and accurate diode performance and pulse generator circuit simulation output [*JUN–JUL'21*];
2. Task – Refine and simulate circuit topological permutation(s) to include increased number of parallel branches electrically-optimal layout considerations and components within Altium [*JUL–AUG'21*];

(C) Milestone – Construct/demonstrate a M×N SOS pulse generator prototype capable of producing $\geq$ 20-kV peak voltage, $\leq$ 1-ns risetime, $\leq$ 2-ns FWHM, $\geq$ 8-MW peak-power, $\geq$ 1-kHz PRF, $\geq 5\sigma_{Vpeak}$, which operates in continuous-burst mode as a viable candidate for OSPRES Contract source alternative [*on hold until Milestone B is completed*].

(D) Milestone – Construct/demonstrate a 8×2 SOS pulse generator prototype capable of producing $\geq$ 48-kV peak voltage, $\leq$ 1-ns risetime, $\leq$ 2-ns FWHM, $\geq$ 46-MW peak-power, $\geq$ 10-kHz PRF, $\geq 5\sigma_{Vpeak}$, $\geq$ 10,000 shots-per-burst, with a $\geq$ 50% duty cycle [*on hold until Milestone C is completed*].

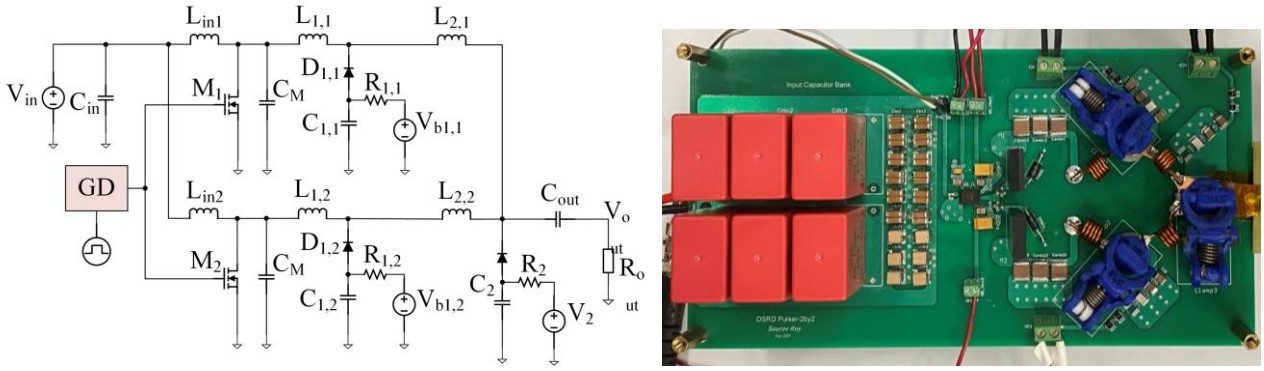
The second effort's milestones, and tasks to achieve them along with a timeline to do so, is as follows:

(E) Milestone – Through Boolean synthesis, generate a machine-learning algorithm, (which uses a decision-tree approach and iterative greedy algorithm) able to accurately predict the SOS-IES topology permutation's key performance metrics and produces the most efficient components and topologies in terms of pulser footprint [*Estimated completion by DEC'21*].

1. Task – Perform literature review on genetic and machine learning algorithms [*JUL—AUG'21*];
2. Task – Automate LTspice circuit simulation using Python scripting: auto generation of an input parameter card, autorun of that simulation space, and then the back-end processing of the output files [*JUN—AUG'21*];
3. Task – Build a suitable predictive model for the SOS-IES modular architecture for a given performance matrix based on sample data obtained in Task– 2 [*SEP—DEC'21*].

3.7.3 Progress Made Since Last Report

A 2×2 DSRD-based SOS-IES pulse generator has been designed, developed, and tested. The schematic and photograph of the pulse generator are shown in Fig. 3.7.1 (a) and Fig. 3.7.1 (b), respectively. The current design incorporated the following modifications/improvements in comparison to the previous design of the 2×2 DSRD-based SOS-IES pulse generator:



(a) (b)

Figure 3.7.1 (a) Circuit Schematic, (b) photograph of the 2×2 DSRD-based SOS-IES pulse generator.

i. A bulk input capacitor bank (C_{in}=265-uF) comprising of several parallel capacitors was designed to help support PRF operation of the pulser circuit.
ii. A single gate driver circuit (using UCC5390-Q1 driver IC from Texas Instruments) was designed to drive two parallel connected MOSFETs whereas the previous design of the pulser circuit includes individual gate driver circuit for driving each MOSFET. Driving multiple MOSFETs using a single gate driver minimizes differences in propagation delays of the MOSFET driving signals that ensures proper synchronization of the two parallel branches for low jitter operation and maximum output voltage.
iii. Some layout improvements and circuit design considerations were incorporated to reduce the parasitic oscillation, ringing and EMI pertaining to high voltage and high frequency operation.

Figure 3.7.2 shows the output waveform (a portion of one cycle) of the pulser circuit. As shown, the pulser circuit achieved peak output voltage of 5.59-kV with a peak power of 672-kW across a 50-Ω load, rise-time of 1.2-ns and a FWHM of 2-ns. It is

encouraging to compare this output with the 2×2 DSRD-based pulse generator proposed Kesar *et* al. that could generate up to 5-kV with a rise-time of 1.96 ns and a FWHM of 2.27-ns. Most importantly, the newly designed 2×2 SOS-IES pulse generator was able to run with multiple PRF in burst mode. Figure 3.7.3 shows the output waveforms (comb of pulses) each having 100-bursts for different PRFs demonstrating their excellent stability (minimum drop) in the peak amplitudes. The plots include the averages and standard deviations (σ) of the peak values of the respective output waveforms and it is apparent that the standard deviation decreases with the increasing PRF meaning the peak amplitudes are clustered close to their mean.

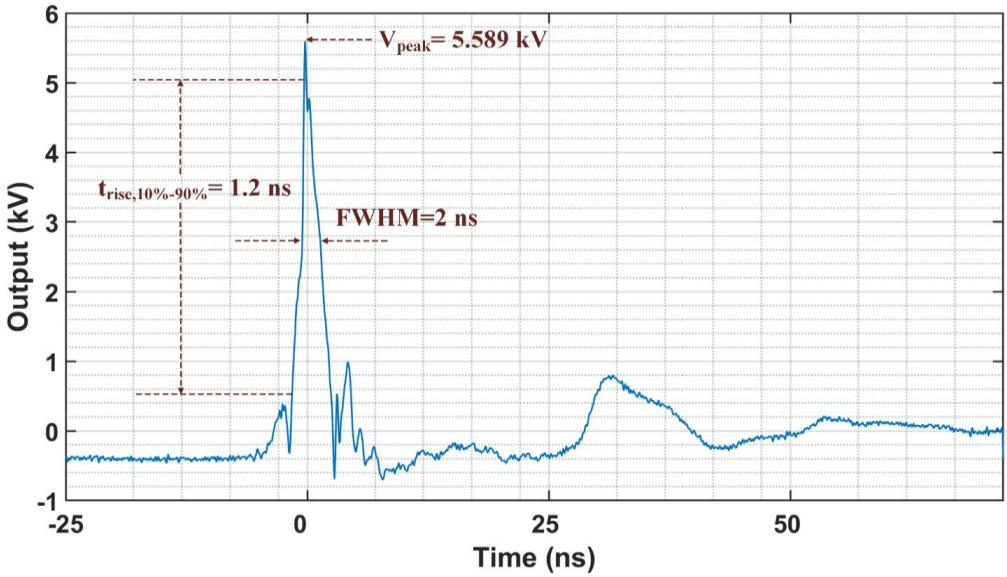
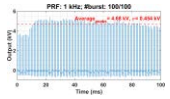
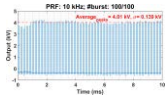


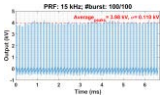
Figure 3.7.2 Output waveform (a portion of one cycle) of the pulser circuit.



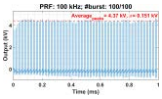
(a)



(b)



(c)



(d)

Figure 3.7.3 Comb of output pulses with different PRFs each having 100 bursts.

Interestingly, there exists a variation in the average peak amplitudes for different PRFs. For example, the average peak amplitude is 4.68 kV at 1kHz PRF whereas the average peak amplitude is 3.98-kV at 15-kHz PRF. Analysis of this result is still in its earliest stages, however one possibility of variation is attributed to the diodes achieving an ideal thermal state of operation (i.e., temperature). The second reason for variation is postulated as insufficient charging and discharging of the input capacitor at high PRFs with burst-mode operation. Greater in-depth analysis of these finding is thus required on understanding the thermal dissipation of the DSRDs, and the necessity of including a thermal management, as well as carefully design the input capacitor bank for the PRF of interest, and so on.

Finally, the output waveforms with multiple PRFs in 1ms time window are shown in Figure 3.7.4

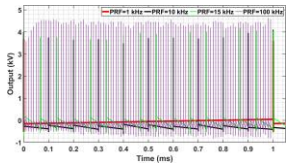


Figure 3.7.4 Output waveforms with multiple PRFs in 1ms time window.

3.7.4 Significant Finding(s) and Mission Impact

3.7.4.1 Summary to Date

(A.2–5) Constructed and demonstrated a 2×2 SOS pulse generator prototype capable of producing up to 5.59 kV peak voltage with 672 kW peak power, ~1.2 ns risetime, ~2-ns FWHM, 1-100 kHz PRF, 100 shots-per-burst for a minimum of 5 independent bursts. Most importantly, for the first time in the history of DSRD-based SOS-IES pulse generator research conducted by MIDE, the newly designed 2×2 DSRD-based pulse generator was able to be operated in burst mode at multiple PRFs such as 1 kHz, 10 kHz, 15 kHz and 100 kHz, each with 100 bursts. Moreover, comparing the performance of our newly designed prototype with the state-of-the-art 2×2 DSRD-based pulse generator, the newly

designed pulser circuit were able to achieve higher peak output voltage with lesser rise-time and FWHM.

4.0 Prime Power and Conditioning

4.1 HV Switch Pulsed Chargers

(Wasekul Azad and Faisal Khan)

4.1.1 Problem Statement, Approach, and Context

Primary Problem: Commercially available high-voltage solid-state switches made by BEHLKE are the best in SWaP-cooling, but are expensive, have long lead times (2–3 months), and are made outside of the US. For the Navy afloat mission to be successful, we need a sustainable supply of US-manufactured switches at a much lower cost.

Solution Space: Design and demonstrate modular high-voltage (~10 kV) and fast (repetition frequency = 100 kHz) solid-state switches using a combination of series- and parallel-connected commercially available inexpensive discrete MOSFETs and custom high-voltage (~10 kV) isolated gate drivers.

Sub-Problem: Voltage balancing among the series-connected MOSFETs, minimization of gate signal delays, cooling of the individual MOSFETs, balancing resistors, high-voltage isolation required for the power supplies, and the controlling pulse width modulated (PWM) signal as well as differential voltage feedback measurement across individual MOSFETs.

State-of-the-Art (SOTA): Direct liquid-cooled solid-state switch from BEHLKE (e.g., HTS-151-30).

Deficiency in the SOTA:

1. BEHLKE-made switches are expensive. For instance, a single HTS-151-30 switch costs around $5,000.
2. BEHLKE switches along with direct liquid cooling units occupy a considerable amount of space. For instance, an HTS-151-30 switch from BEHLKE has a footprint of approximately 225*85*75 mm without considering the liquid cooling system. Some key parameters of this switch are as follows.

   i) Maximum operating voltage = 15 kV

   ii) Maximum continuous load current = 2.52 A (without cooling), 30 A (with liquid cooling)

   iii) Maximum turn-ON peak current = 300 A (pulse width = 200 µs, duty cycle <1%)

   iv) Turn-ON resistance = 1.3 Ω
3. Once the switching frequency is greater than 10 kHz, a liquid cooling system is required to operate the BEHLKE switch.
4. Without liquid cooling, the maximum continuous power dissipation (P_{cont}) of the BEHLKE switch is limited (e.g., for HTS-151-30, P_{cont} is 10 W without liquid cooling).
5. At a higher switching frequency (>20 kHz), the BEHLKE switch requires multiple ancillary DC power supplies, i.e., 5, 15, and 60 V.

6. The switches made by BEHLKE cannot be reconfigured to withstand a higher voltage exceeding their recommended rating. BEHLKE offers separate products to operate them at higher voltage/currents.

Solution Proposed: Designing a modular high-voltage (~10 kV) switch using a single custom isolated gate driver for each module and having a construction cost lower than the BEHLKE switch with equivalent or better performance in all specification categories (Specifications for the BEHLKE switches can be found in the following link: http://www.behlke.com/separations/separation_c4.htm).

Relevance to OSPRES Grant Objective: The proposed modular high-voltage switch is expected to facilitate controlled hundreds-of-nanosecond charging of an array of transmission lines of pulse forming networks to drive an array of PCSSs, thereby producing controlled hundreds-of-picosecond scale high-voltage pulses.

Risks, Payoffs, and Challenges:

I. Lack of rigid control over voltage balancing can lead to a cascaded failure among the series-connected MOSFETs.

II. In the absence of an adequate mitigation scheme, voltage overshoot due to the fast switching speed can exceed the voltage rating of an individual MOSFET, thereby damaging the switch.

III. At high voltage (~10 kV) and high repetition rate (>100 kHz), mitigating EMI to safeguard the individual MOSFETs from false turn-ON is a major challenge.

4.1.2 Tasks and Milestones / Timeline / Status

(A) Design a surface-mount MOSFET-based four-stage switch (6.8 kV rated) and control it using the in-house gate driver, then test its voltage-withstanding ability with a DC supply voltage up to 4–5 kV and evaluate the effectiveness of the thermal management at its current state / DEC 2020 / Completed.

(B) Design and develop a modular HV switch (~10 kV rated) using the concept of the tested four-stage high-voltage switch module and an in-house modular gate driver to drive the modular switch /JAN–FEB 2021 / Completed.

(C)

(i) Test the voltage withstanding ability of the modular HV switch with a DC supply voltage up to 10 kV and switching frequency up to 50 kHz using a resistive load (5–10 kΩ) and evaluate the effectiveness of the thermal management at its current state / FEB–JUN 2021 / Ongoing.

(ii) Test the isolation capability and evaluate the synchronization accuracy of the gate drive signal generated from the modular in-house gate driver / FEB–JUN 2021 / Ongoing.

(iii) Encapsulate the gate driver board with potting material with a high (~15–20 kV) breakdown voltage rating to prevent possible flashover/arcing in between the HV switch and this board / MAR–JUN 2021 / Ongoing.

(D) Design and fabricate a compact power conditioner circuit based on a 12 kV rated SiC switch made by BEHLKE (HTS 121-15) / APR-MAY 2021 / Completed.

(E) Test this modular HV switch coupled with a Si PCSS device up to a DC supply voltage of 5–6 kV and a switching frequency of 50 kHz / On hold due to graduation in the Summer 21 semester.

(F)

(i) Design and develop a 20 kV rated modular (two modules, each with four MOSFETs) HV switch based on the design concept of the 10 kV rated modular switch using 3.3 kV rated SiC MOSFETs (new product made by GeneSiC Semi) / On hold due to graduation in the Summer 21 semester.

(ii) Design and develop a 20 kV rated modular gate driver based on a WPT based planar transformer topology to ensure adequate galvanic isolation (~30–40 kV) for the power supplies of the gate driver / On hold due to graduation in the Summer 21 semester.

4.1.3 Progress Made Since Last Report

(B)

(i) A conference paper written on the in-house modular HV switch has been accepted to the IEEE Kansas Power and Energy Conference 2021, and an oral presentation on the paper has been given.

(ii) A journal manuscript has been prepared on the modular HV switch and the custom gate driver circuit.

(C)

(ii) The gate driver is experiencing arcing at around 5.6 kV. We have pinpointed the location of the arcing in the gate driver circuit. We have designed a new gate driver PCB with increased clearance between traces with high potentials, and included slot cutouts underneath the gate driver IC for increased creepage allocation. We have revised the previous design to incorporate resistors with impedance in the range of megaohms across the control and power grounds of the gate driver IC.

4.1.4 Significant Finding(s) and Mission Impact

4.1.4.1 Summary to Date

(A) The 6.8 kV rated four-stage surface-mount MOSFET developed in-house was successfully tested up to a DC supply voltage of 4 kV and at a switching frequency up to 20 kHz with a 3.2 kΩ resistive load.

(B) A modular (two modules) 10 kV rated HV switch has been designed and a prototype has been developed using 1.7 kV rated SMD MOSFETs (C2M1000170J). An in-house 10 kV rated HV gate driver has been designed and incorporated with the HV switch to drive it. A manuscript has been prepared on the HV switch and the custom isolated gate driver for submitting in IEEE Transaction on Power Electronics.

(C) The HV switch coupled with the custom HV gate driver has been tested at a supply voltage up to 6 kV at a switching frequency up to 15 kHz. We have identified gate driver malfunctioning at around 6 kV, and are investigating the root cause of it.

4.1.4.2 Since Last Report

(C) Further testing of the HV switch couple with the custom gate driver has been accomplished to pinpoint the location of the arcing. The test has been video recorded to observe the arcing and we have identified that the arcing stems from the ground pin at the control side. We are planning to populate a new PCB board with new components and incorporate a high-valued (tens to hundreds of MΩ) resistor in between the grounds at the control side and the output side. Our assumption is that the floating ground at the control side is the root cause of this issue. We will apply a conformal coating all over the HV gate driver board to increase the voltage withstanding ability of the entire board.

We have prepared a manuscript on the multilevel modular HV switch architecture and will submit it to the IEEE Transactions on Power Electronics.

We have addressed the reviewers' comment related to a journal on NLTL works that was submitted to IEEE Transaction on Plasma Science. The revised journal article has been accepted for publication.

5.0 Tradespace Analysis of Ultra-Wide-Band Antenna Arrays

5.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

5.1.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wideband (UWB) antenna elements in a phased array for high-power microwave (HPM) transmissions.

Deficiency in SOTA: Large physical aperture size of the antennas.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters, followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area. Using stochastic and machine learning (ML) algorithms to optimize antenna element and array performance.

Relevance to OSPRES Grant Objective: Provides design and optimization guidelines for UWB ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN–MAY 2021 / Completed code.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN–MAY 2021 / Completed investigations of arrays on infinite ground plane.

(C) Build minimum viable validation prototypes of single ESA elements on substrates that have good power handling capabilities for HPM transmissions at UHF range (such as FR-4, TMM-10i, TMM-6) / JAN–AUG 2021 / Ongoing time-domain reflectometry (TDR) testing of the designed antenna elements.

(D) Optimization of ESA element performance using stochastic and ML algorithms / JUN–SEP 2021 **(NEW)** / Ongoing.

(E) Build minimum viable validation prototypes for arrays of ESA elements / JUN–SEP 2021 **(NEW)** / Ongoing.

5.1.3 Progress Made Since Last Report

(C) Build minimum viable validation prototypes of single ESA elements:

a. Modeled an UWB L-probe-fed U-slot-loaded rectangular microstrip patch antenna on FR-4 ($\varepsilon_r = 4.5$) substrate in the UHF range (0.52–1.17 GHz) via FEKO.

b. Two papers, on the design and characterization of single ESA elements, have been submitted to the 2021 AP-S/URSI conference.

c. Preparing manuscript for IEEE AP-S Magazine based on the tradespace analysis of microstrip patch ESA element design and optimization.

(D) Optimization of ESA (single element) performance using stochastic and ML algorithms:

a. Preliminary investigation into bandwidth enhancement of the designed microstrip patch antennas, by optimizing the feed-probe location using stochastic optimization tools (that are available in the EM-solver FEKO), such as Genetic Algorithm (GA), Particle Swarm Optimization (PSO) and Nelder-Mead Simplex methods, has been performed.

b. A paper has been submitted for the ACES 2021 conference, based on the results obtained from part D(a).

c. Initiated investigations into probe-location and ground plane size optimization, with the objective of bandwidth enhancement in a microstrip patch antenna element, using ML algorithms via Altair HyperStudy.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

a. Initiated modeling of a 25-element planar array of microstrip ESA elements, arranged in square and hexagonal lattices, in the UHF region (0.6–1 GHz).

5.1.4 Significant Finding(s) and Mission Impact

5.1.4.1 Summary to Date

(A) Developing Array Pattern Tool for large arrays calculations:

A MATLAB code has been developed for faster approximation of radiation pattern of a linear/planar array of any size and composed of any type of antenna elements. The code requires the center element pattern of a small array (say, 3×3) composed of same type of antenna elements, desired lattice arrangement, and total number of array elements, as user inputs. This work will be included in future publications.

(B) Investigate the effects of array aperture area reduction on different array parameters:

The effect of different array aperture area and lattice arrangements, on the array parameters (such as, array gain, beamwidth, electronic beam steerability, etc.), has been reported for arrays modeled on infinite ground planes. The array parameters for large arrays ($\geq 15 \times 15$) on finite ground planes could not be computed using the commercial EM solvers (FEKO and CST) due to excessive memory and time consumption. This work will be resumed after developing a method to estimate array performances on finite ground planes, either through ML or conventional approaches.

(C) Build minimum viable validation prototypes of single ESA elements:

Two bandwidth enhancement techniques applicable for single layer, coaxial probe-fed, microstrip ESAs, have been considered. First, a novel method to increase the bandwidth (≥30%) is proposed, by strategically placing the coaxial probe along 2/3rd the patch diagonal. Second, by introducing U-slots on rectangular microstrip patches. To validate the design approaches, two simple rectangular patch antennas (using the proposed bandwidth enhancement technique) on TMM-6 and TMM-10i substrates and a U-slot patch antenna on G10/FR-4 substrate have been manufactured and tested. Investigations into a U-slot-loaded rectangular microstrip ESA element, excited by L-probe-feed, has been initiated and shown to yield $\approx 77\%$ 2:1 VSWR bandwidth in the UHF region (0.52–1.17 GHz).

(D) Optimization of ESA (single element) performance using stochastic and ML algorithms:

Performance optimization of the antennas, in terms of bandwidth and gain, has been initiated using various stochastic and ML algorithms. Preliminary investigations have shown that stochastic algorithms, such as GA, PSO, and Simplex methods, are computationally intensive (in terms of time and memory consumption), and do not result in significant performance improvement of the designed microstrip ESA elements. Future work involves application of ML algorithms in performance optimization of designed single antenna elements.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

Initiated modeling of a 25-element planar array, composed of coaxial probe-fed microstrip patch ESA elements, in the UHF region (0.6–1 GHz).

5.1.4.2 Since Last Report

(C) Build minimum viable validation prototypes of single ESA elements:

An L-probe-fed U-slot-loaded rectangular microstrip patch antenna has been modeled via FEKO. The geometry of the design and its VSWR and gain response are illustrated in Fig. 5.1.1.

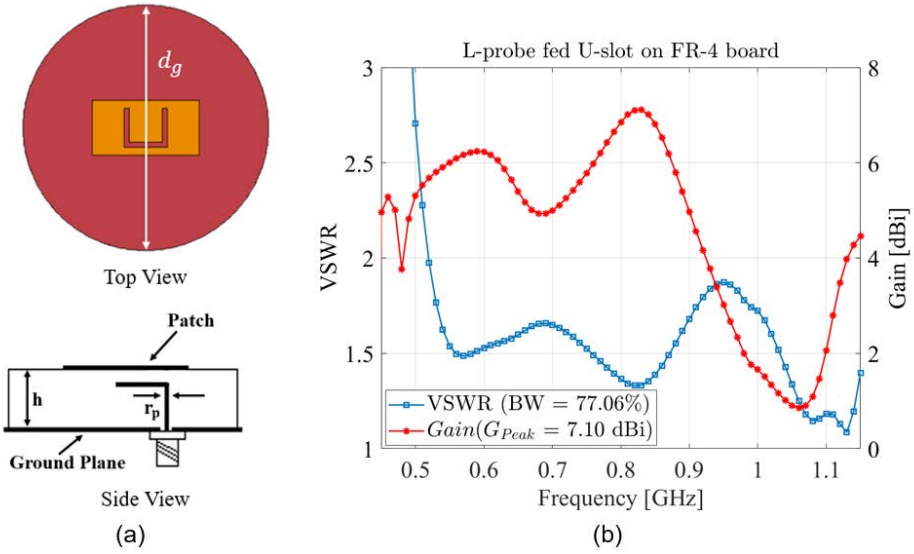


Fig. 5.1.1. (a) L-probe-fed U-slot patch antenna geometry; (b) VSWR and gain of the antenna.

Table 5.1.1. Antenna Dimensions

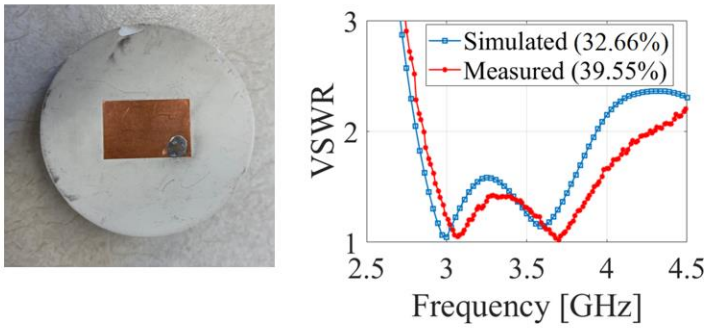
Parameters	Description	Values
L (mm)	Patch Length	87.855
W (mm)	Patch Width	171.7794
L_s (mm)	Slot Length	62.8862
W_s (mm)	Slot Width	70.3544
t (mm)	Slot Thickness	8.0106
L_h (mm)	Horizontal probe length	25
L_v (mm)	Vertical probe length	36.2562
r_p (mm)	Probe Radius	5.5
D (mm)	L-probe Location	-3.125
d_g (inch)	Ground Plane Radius	15.625

(D) Optimization of ESA (single element) performance using stochastic algorithms:

A comparison among three different stochastic optimization algorithms for seeking the best probe location in a wideband microstrip patch antenna designed on the TMM-6 substrate (at the center frequency of 3.75 GHz), with the objective of bandwidth enhancement, has been performed. The initial probe location of the design, which was earlier shown to yield 32.66% 2:1 VSWR bandwidth, is further optimized using the in-built GA, PSO and Nelder-Mead Simplex algorithms that are available in FEKO. The results are summarized in Table 5.1.2. While little to no change in bandwidth is obtained with GA and PSO, the Nelder-Mead Simplex algorithm resulted in 2% bandwidth improvement. In addition, the PSO-optimized probe location is shown to have improved the nature of the VSWR curve.

Table 5.1.2. Comparison of different optimization algorithms in seeking the best probe location (x_p, y_p) in the designed microstrip patch antenna.

Parameters	Optimization Algorithm		
	GA	PSO	Nelder-Mead
Optimization variables	x_p, y_p	x_p, y_p	x_p, y_p
Optimization Goal	VSWR < 2	VSWR < 2	VSWR < 2
Initial (x_p, y_p) (mm, mm)	(4.26, 6.38)	(4.26, 6.38)	(4.26, 6.38)
Optimized (x_p, y_p) (mm, mm)	(5.0001, 7.6471)	(4.5484, 7.4764)	(4.8863, 6.8211)
No. of iterations	10	50	100
No. of analysis	100	920	36
Runtime (dy-hr:min:sec)	00-04:03:06	01-19:53:54	00-01:45:24
% BW	32.99	32.34	34.73
Peak Gain (dBi)	5.65	5.59	5.62



(a) (b)

Fig. 5.1.2. (a) Manufactured prototype on a 6.35 mm thick TMM-6 substrate; (b) Simulated (FEKO) and measured VSWR of the prototype with the initial probe location. Note: The detailed design and characterization of the antenna has been reported in earlier MSRs.

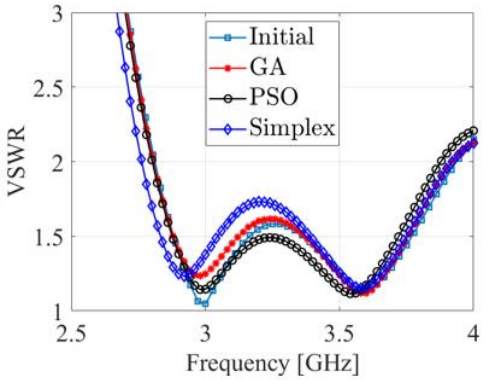


Fig. 5.1.3. Comparison of VSWR of the microstrip patch antenna with initial and optimized probe locations obtained via different stochastic algorithms.

5.2 Tradespace Analysis of Other Ultra-Wide-Band (UWB) Single Elements

(Kalyan Durbhakula)

5.2.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelev antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem: The total surface currents on the Koshelev antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not yet clearly understood.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelev antenna that effectively reduce its physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelev antenna has been shown in the literature to withstand higher voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelev antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelev antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelev antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelev antenna.

(iii) The large electrical size (>5λ) of the Koshelev antenna at its highest operating frequency poses huge computational challenges. Efforts are underway to cleverly select important design parameters for the tradespace study.

5.2.2 Tasks and Milestones / Timeline / Status

(A) Complete literature search to identify and list antenna elements that satisfy UWB properties and HPM requirements, and down select accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelev antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB–MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t, \phi, \theta)$) in receive or transmit mode.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelev antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size. / Complete.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / MAR21/ Complete.

- Milestone: Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain over the desired bandwidth, and aperture efficiency / Complete.

(F) Reduce Koshelev antenna aperture size (H×W) to equal to or less than 90 mm × 90 mm, equal to that of the SOTA BAVA, for direct antenna metrics comparison / MAR–APR21 / Complete.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, aperture efficiency equal to or greater than 130% at 900 MHz.

(G) Using the optimized model from (F), build various array simulation models/topologies to perform tradespace study and report tradeoffs between array antenna metrics such as

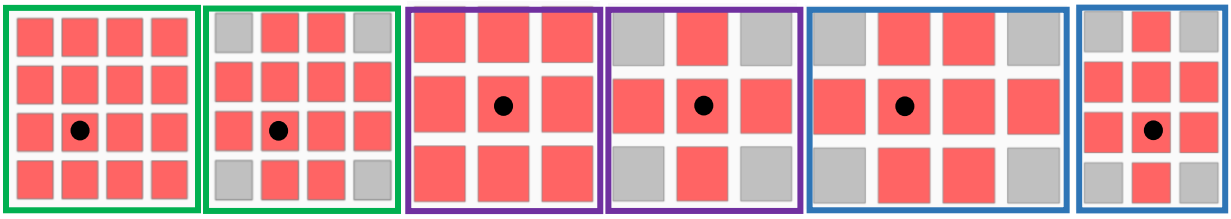
center element S11 value, gain vs theta at constant phi, physical aperture area, aperture efficiency and rE/V / MAY–JULY21 **(NEW)** / Ongoing.

- Milestone: Develop/showcase an optimized Koshelev array model that exceeds an aperture efficiency of 130% with a high rE/V.

(H) Continue with the literature search and improving our understanding on special electromagnetic (EM) techniques to determine their applicability to the antennas under consideration. / JAN–APR21 / Complete.

5.2.3 Progress Made Since Last Report

(G) An effort has been carried out over the last month to develop simulation models of various array topologies and execute the models for their array antenna metrics. Fig. 1 shows various array topologies considered for this study. Each colored square block In Fig. 5.2.1 represents the optimized Koshelev antenna. In Fig. 5.2.1, topologies (a) and (b) are compared against each other to draw an apples to apples comparison. Similarly, topologies (c) and (d) are compared against each other, and topologies (e) and (f) are compared against each other. The black dot represents the center most element of that topology which could have the worst-case S11 value due to maximum electromagnetic coupling (EMC). When comparing S11 value between the topologies, the center element's S11 value of each topology is considered. It is known that elements on the edge of the array tend to have a better S11 value when compared to elements located inside the array. Therefore, the S11 value of edge elements are avoided for brevity. Furthermore, Table 5.2.1 compares the area of all topologies under study. In addition, a simulation has also been carried out using the hexagon array (with 2 side elements) to show the variation in desired array antenna metrics as a function of interelement spacing.



(a) (b) (c) (d) (e) (f)

Fig. 5.2.1. Array topologies under study. (a) Square – 4×4, (b) Octagon – 2 side elements, (c) Square – 3×3, (d) Diamond – 2 side elements, (e) Hexagon – 2 side elements (4×3), and (f) Ellipse – 3×4.

Table 5.2.1. Area of Koshelev array topologies with $S_x = S_y$ = 50 mm

Array shape	Size of an array	Area
Square	4×4	0.2844 m^2
Octagon	2 side elements	0.2554 m^2

Square	3×3	0.1504 m^2
Diamond	2 side elements	0.074 m^2
Hexagon	2 side elements	0.1374 m^2
Ellipse	3×4	0.1598 m^2

5.2.4 Significant Finding(s) and Mission Impact

5.2.4.1 Summary to Date

(A) An extensive literature search on various UWB antenna elements has resulted in finding three promising options. The down-selected elements are the Koshelev, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the single antenna element. Later, the single antenna element will be converted into a planar array.

(B) Initial validation of the Koshelev antenna simulated using CST software agreed well with the antenna metrics published in the open literature [1]. A UWB bandwidth response (10:1 bandwidth) and rE/V > 1 has been observed from our initial simulations of the Koshelev antenna. This validation ensured that the Koshelev antenna can be subjected to further tradespace studies to understand its performance followed by optimizing the design according to OSPRES grant requirements.

(C) The initial tradespace study and analysis of the Koshelev antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between the Koshelev antenna in [1] and aperture reduced Koshelev antenna are shown in Table 5.2.1 of APR 21 MSR.

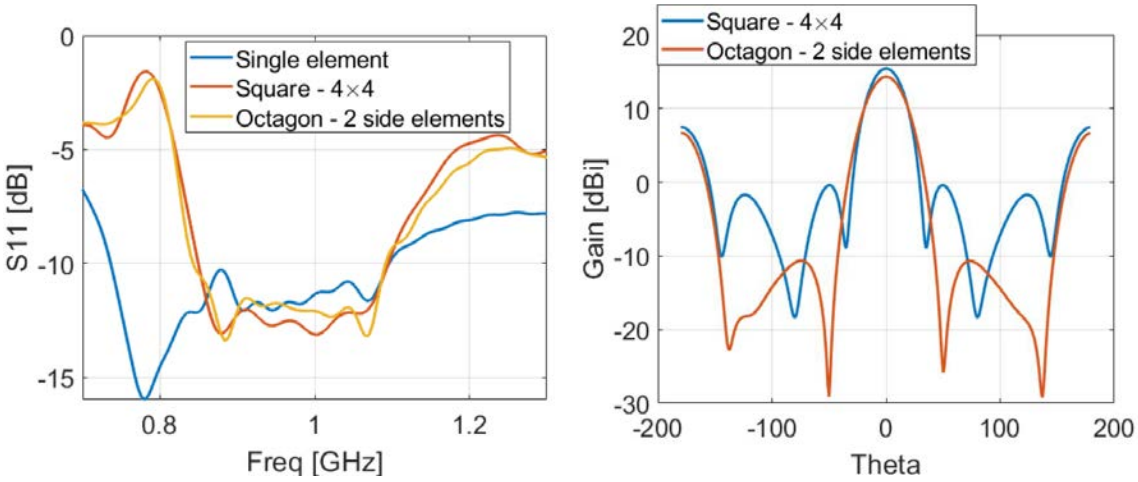
(D) An in-house code has been developed to calculate important UWB time domain antenna metrics such as full-width half maximum (FWHM) and ringing. These metrics have been calculated using in-house MATLAB code using the excitation voltage and radiated electric field information obtained from CST simulations. FWHM and ringing antenna metrics help with assessing or characterizing an antenna's UWB response.

5.2.4.2 Since Last Report

(G)

- The Koshelev array tradespace study has been initiated with the traditional method of exploring various array topologies. The topologies under study were shown in Fig. 5.2.1. Fig. 5.2.2a plots the S11 value of a single Koshelev antenna element and the S11 value of the center element of the square and octagon array topologies, shown in Fig. 5.2.1a and Fig. 5.2.1b, respectively. It is clear that the center element suffers

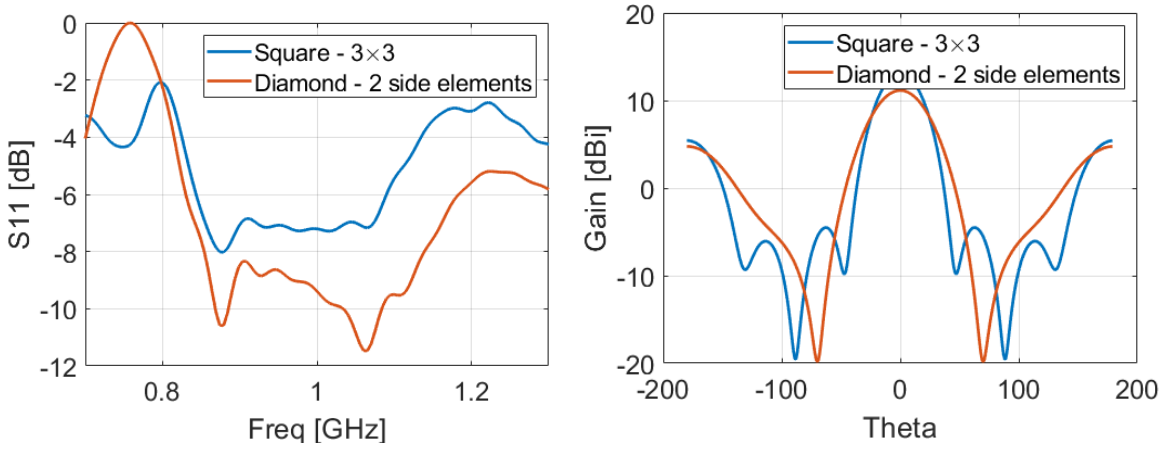
from maximum reflections due to EMC between elements located on all four sides. However, in terms of S11 value, the difference between square and octagon array topologies is negligible. Fig. 5.2.2b shows the gain as a function of theta (elevation) angle from –180° to 180° for the two array topologies. The difference in peak gain at θ = 0° between the two topologies is very small, however, the side lobes decreased by at least 10 dB, which is a significant improvement.



(a) (b)

Fig. 5.2.2. (a) S11 value of single element, center element S11 value of a 4×4 square Koshelev array and 2 side elements diamond Koshelev array, and (b) gain as a function of theta angle comparison between 4×4 square Koshelev array and 2 side elements diamond Koshelev array.

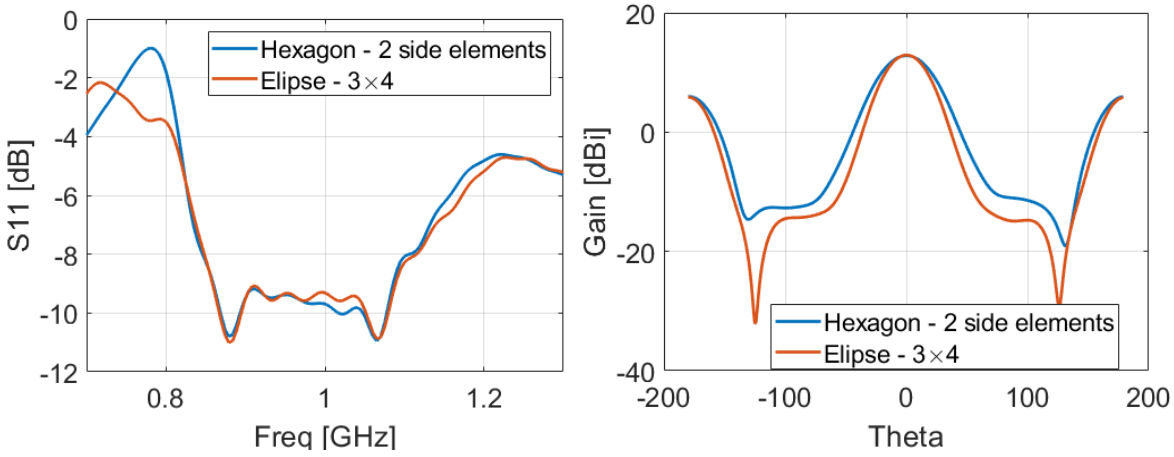
- A diamond array topology has also been utilized in some previous applications. Fig. 5.2.3a compares the S11 value of the center element of a square (3×3) and a diamond array, which are shown in Fig. 5.2.1c and Fig. 5.2.1d, respectively. From Fig. 5.2.3a, it is evident that a diamond array has better S11 value over the desired bandwidth than the square topology. A slight decrease in peak gain is expected due to the reduced number of elements in the case of the diamond array, however, an improvement in the side lobes can be noticed. By choosing a diamond topology, the aperture area can be significantly reduced while losing small value of gain. Moreover, the realized gain of a square array topology would be lower than the realized gain of a diamond array due to the poor S11 value of square array.



(a) (b)

Fig. 5.2.3. (a) Center element S11 value of a 3×3 square Koshelev array and 2 side diamond Koshelev array, and (b) gain as a function of theta angle comparison between 3×3 square Koshelev array and 2 side diamond Koshelev array.

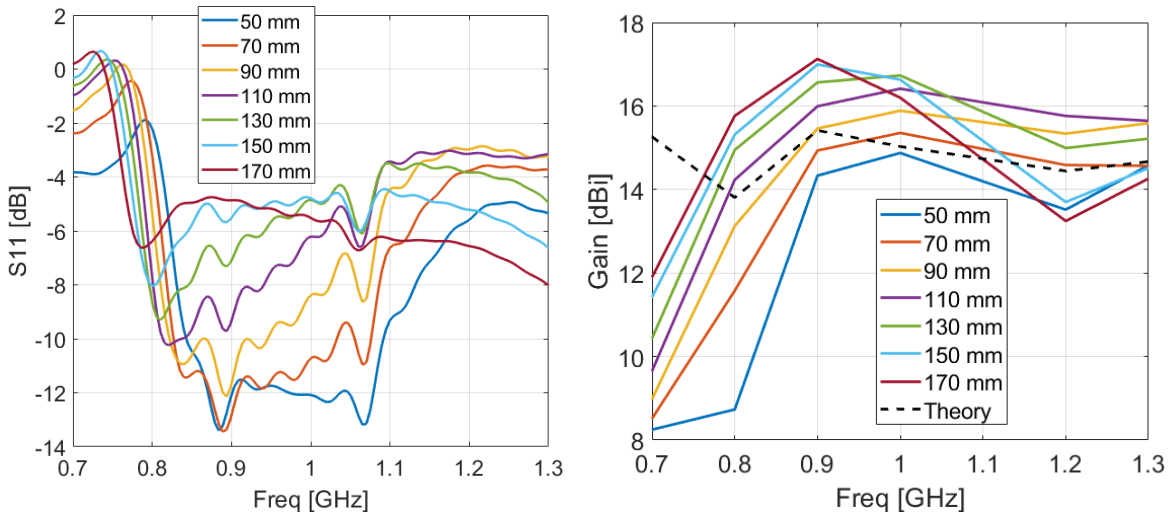
- The hexagon with 2 side elements yielded a 4×3 asymmetric array topology and an ellipse topology with reciprocal topology have been chosen to draw a comparison. The S11 value of the center element for both topologies in Fig. 5.2.4a depicts a similar response. Furthermore, the gain response from both topologies looks similar with a slight advantage to the ellipse topology. This is due to the addition of elements in the direction of the electric field rather than in the H-plane.



(a) (b)

Fig. 5.2.4. (a) Center element S11 value of a 2-side elements hexagon Koshelev array and a 3×4 ellipse Koshelev array, and (b) gain as a function of theta angle comparison between 2 side hexagon Koshelev array and a 3×4 ellipse Koshelev array.

- The inter-element spacing between the elements in both directions ($S_x = S_y$) has been varied to understand its effect on the S11 value and gain. It is well-known that as the spacing increases, the gain increases, which can be clearly seen in Fig. 5.2.5b. Fig. 5.2.5 shows the S11 value and gain evaluated over a range of different inter-element spacing values for the 2-side elements Octagon Koshelev array, shown in Fig. 5.2.1b. The dotted black line is the result obtained from the theoretical calculation of array gain ($= N_t G_{sinlge}$), where N_t is the total number of array elements and G_{sinlge} is the gain of a single Koshelev antenna. At 900 MHz, the dotted black line matches with the yellow line (90 mm), which is λ/2 around 1.67 GHz. However, Fig. 5.2.5a shows an opposite effect. As the inter-element spacing is increased, the S11 value shifted up i.e., deteriorated in its performance. Additional validations and detailed investigation are needed into the shift of S11 value. Preliminary analysis tells us that smaller inter-element spacings only affect higher frequencies and would not necessarily deteriorate performance at low frequencies. However, this needs to be confirmed with additional study. If this result holds, it would be wise to use smaller spacings for optimum realized gain even though it may result in decreased gain. In contrast, a poor S11 value with excellent gain will always result in unsatisfactory realized gain which can be seen with inter-element spacing equal to 170 mm in Fig. 5.2.5.



(a) (b)

Fig. 5.2.5. Variation of Koshelev array (a) center element S11 value, and (b) Gain over the desired frequency range for different interelement spacing values.

5.2.5 References

[1] Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

5.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna

(Sadie Brasel and Kalyan Durbhakula)

5.3.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of Shark antenna elements whose miniaturization in two dimensions (height and width equal to $\lambda/4$ where λ corresponds to the lowest operating frequency) make it a good candidate for UWB HPM systems while having a reduced aperture area with respect to the current state-of-the-art. In the literature, the Shark antenna has already been shown to achieve a wide 20:1 impedance bandwidth, low dispersion, and a sectoral (also referred to as directional) radiation pattern.

Sub-Problem: The design parameter space of the Shark antenna has not been studied rigorously in the literature and therefore the effect of these parameters on the antenna metrics is not understood. In addition, the Shark antenna has been shown to be not very directive in the H-Plane. Preliminary studies have shown that aperture efficiencies at low frequencies are much better than at higher frequencies.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Explore the design parameter space for the Shark antenna element using computational electromagnetic (EM) wave solvers starting with the simulation and validation of a single element.

Relevance to OSPRES Grant Objective: The Shark antenna dimensions were established to be frequency dependent and can be readily modulated to fit the spectrum characteristics of an ultra-fast rise time input pulse.

Risks, Payoffs and Challenges:

(i) The Shark antenna is comprised of flare-angle-dependent bicones that are truncated in the azimuthal angle. This still yields considerably higher half power beam width (HPBW) than other antenna elements under investigation. The significant reduction of HPBW in the H-plane may be unattainable and can be considered a major risk.

(ii) Payoffs include the development of a library of antenna metrics data for various shapes and sizes of the bicones and reflector plates in the shark antenna.

(iii) Computational challenges remain present with respect to automation of design parameter space on our currently used supercomputer (LEWIS). Design challenges

persist in obtaining lower operating frequencies while not increasing the height of the antenna and surpassing the 90 mm × 90 mm size requirement.

5.3.2 Tasks and Milestones / Timeline / Status

(A) Complete initial design, simulation, and validation of the Shark antenna / JAN21 / Complete.

(B) Validate Shark antenna design using the LEWIS supercomputer over a wider range of frequency results (up to 20 GHz) / FEB–MAR21 / Complete.

(C) Identify Shark antenna design parameters which contribute significantly to bandwidth, gain, and physical aperture area. Determine which parameters contribute most to performance improvement/size reduction/ FEB–MAR21 / Complete.

(D) Perform a tradespace study by simulating the Shark antenna with varying cases of flare angle, cone length, and distance to backplane. Gain a general understanding of how these parameters affect impedance bandwidth, rE/V, gain and HPBW / FEB-MAY / Complete.

- Milestone: produce a detailed summary of change in impedance bandwidth, rE/V, HPBW in H-plane and E-plane as a function of flare angle (α), cone height (h), and distance to backplane (d) / Complete.
- Milestone: Choose optimal Shark antenna design based on tradespace study / Complete.

(E) Using the optimal Shark antenna design in (D), simulate various array geometries including hexagonal, rectangular, and circular arrays. Determine which array geometries are optimal and analyze aperture fields and aperture efficiencies. / MAY–JUN21 / Ongoing.

- Milestone: produce a report which states the effects of array geometries for the Shark antenna. Consider the impedance bandwidth, max gain, directivity, and aperture efficiency of each array.

(F) Begin prototyping and validation of optimal Shark antenna single element. / JUN–JUL21 / Ongoing.

- Milestone: have a finished Shark antenna prototype. Compare S11 and radiation pattern with simulated Shark antenna.

(G) Apply dielectric loading techniques to reduce the lowest operating frequency of the Shark antenna to 700 MHz within the h = 45 mm height. / JUN–JUL21/ Ongoing.

- Milestone: demonstrate a reduction of 100 MHz to the lowest operating frequency with the inclusion of a dielectric loading technique with minimal effects to the maximum gain and aperture efficiency.

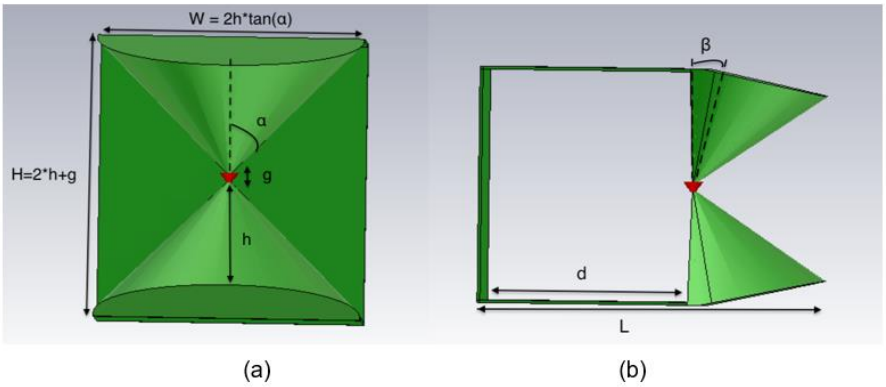


Figure 5.3.1. Shark antenna design parameters: *d, h, g,* α*,* β*.*

5.3.3 Progress Made Since Last Report

(D) The optimal Shark antenna design has been selected. This design has: *d* = 75 mm, *h* = 45 mm, *g* = 2 mm, α = 20°, β = 12°.

(E) Square and hexagonal Shark antenna arrays have been simulated. Their S parameters, gain patterns, rE/V, and aperture efficiencies have been noted.

(F) Efforts are underway to begin the prototyping of the single element Shark antenna. Initial ideas for fabrication include 3D printing using a metal extrusion and then electroplating the surface with copper. Alternatively, a cheaper method involves 3D printing and applying a copper paint.

5.3.4 Significant Finding(s) and Mission Impact

5.3.4.1 Summary to Date

(A-B) The Shark antenna has been designed, simulated, and validated according to [1]. (Figure 5.3.1)

(C) The Shark antenna design parameters that have been found to contribute significantly to bandwidth performance, directivity, and gain are the cone height (*h*) and distance to backplane (*d*).

(D) The Shark antenna tradespace study has been completed and has provided insight into the Shark antenna design space. Increasing the cone height *h* yields better impedance bandwidth at low frequencies and is more directive in the *e* and *h* planes. However, increasing *h* results in a larger aperture area. To remain within 90 x 90 mm, the maximum *h* value is 45 mm; with this a lowest operating frequency of 815 MHz is achievable.

5.3.4.2 Since Last Report

(E) First, a 3x3 square Shark array has been simulated in CST. When creating the array one can choose to connect the backplanes of the elements or not. Both methods have been attempted as shown in Figure 5.3.2.

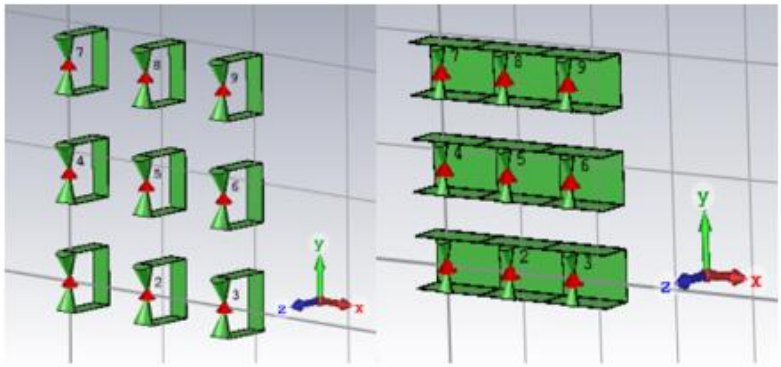
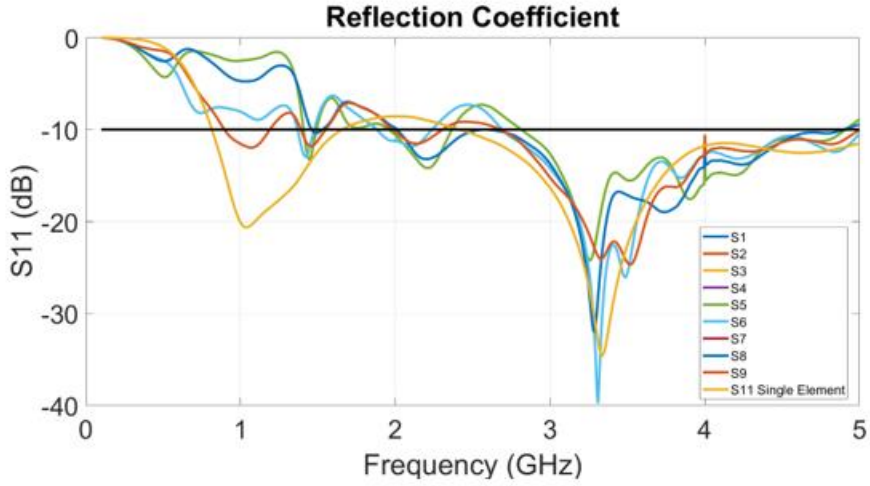
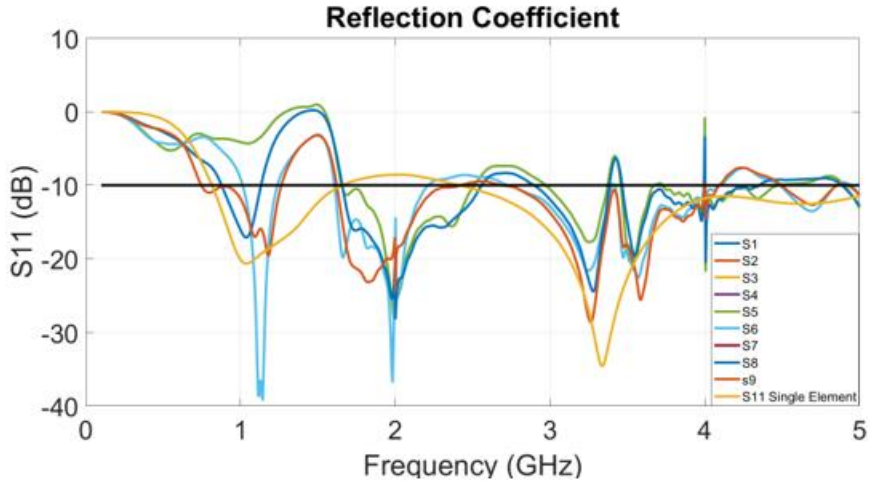


Figure 5.3.2. 3x3 Square Shark antenna array: (a) disconnected backplanes (b) connected backplanes.



(a)



(b)

Figure 5.3.3: Reflection coefficient of square arrays: (a) unconnected backplanes (b) connected backplanes.

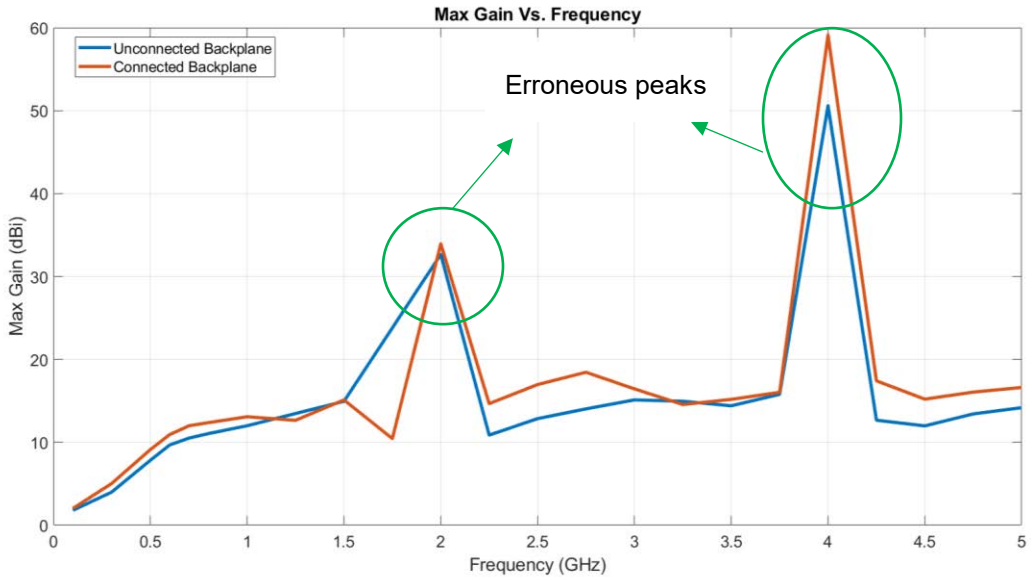
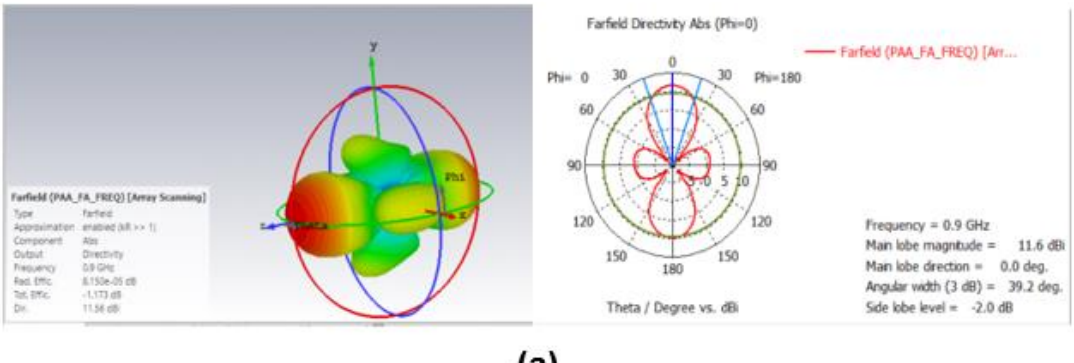
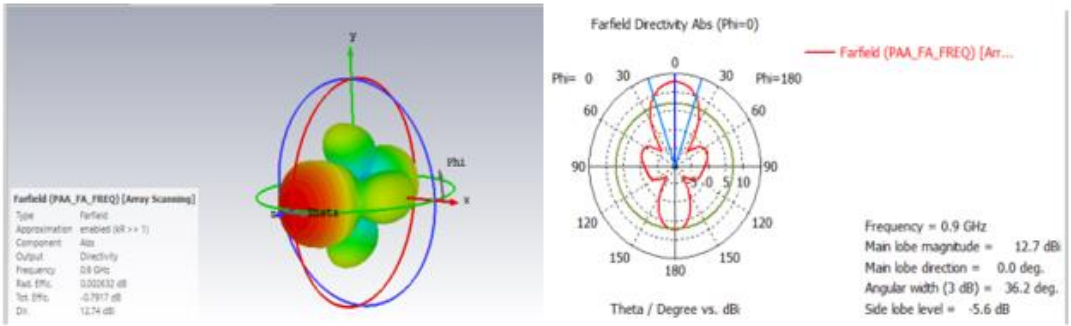


Figure 5.3.4: Max gain vs. frequency of the two square arrays.



(a)



(b)

Figure 5.3.5: 900 MHz radiation patterns of square arrays: (a) unconnected backplane (b) connected backplane.

(G) From the scattering parameter results and the max gain over frequency plots it can be seen that the inclusion of a backplane increases performance with the exception of some degradation between 1–2 GHz. However, at the low frequency and high frequency end the array with connected backplanes has a higher gain of about 1 dBi while having the same number of elements. It should be noted that the max gain vs. frequency plots are slightly incorrect due to the peaks at 2 and 4 GHz. This is due to the use of a 900 MHz pulse as the input excitation, the trend of a straight upward sloping line would be more accurate. Therefore, moving forward the connected backplane method will be used. An 8-element hexagonal Shark antenna array has also been simulated in CST.

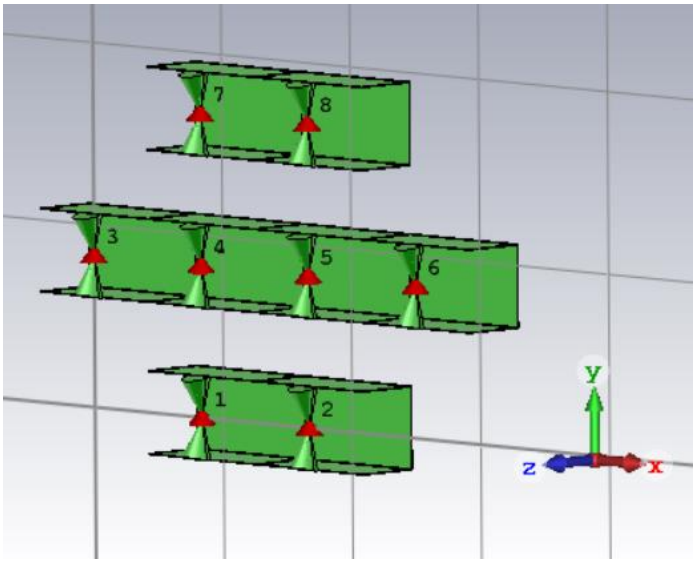


Figure 5.3.6: Hexagonal Shark antenna array.

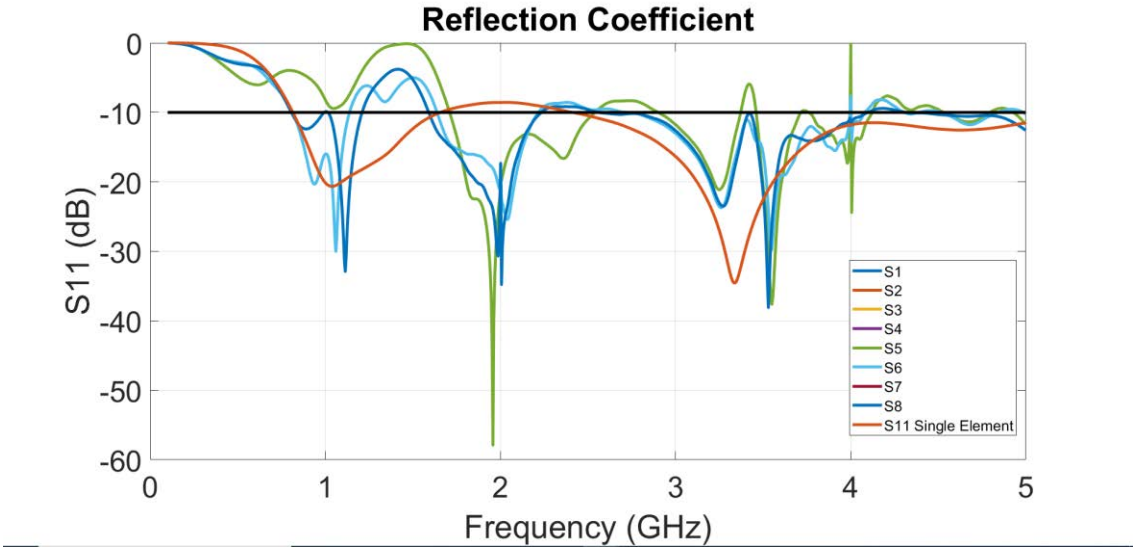


Figure 5.3.7: Hexagonal Shark antenna array reflection coefficient.

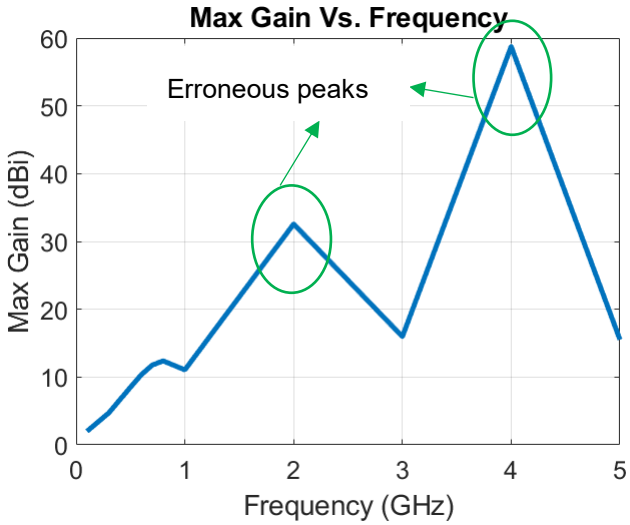


Figure 5.3.8: Hexagonal Shark antenna array max gain vs. frequency.

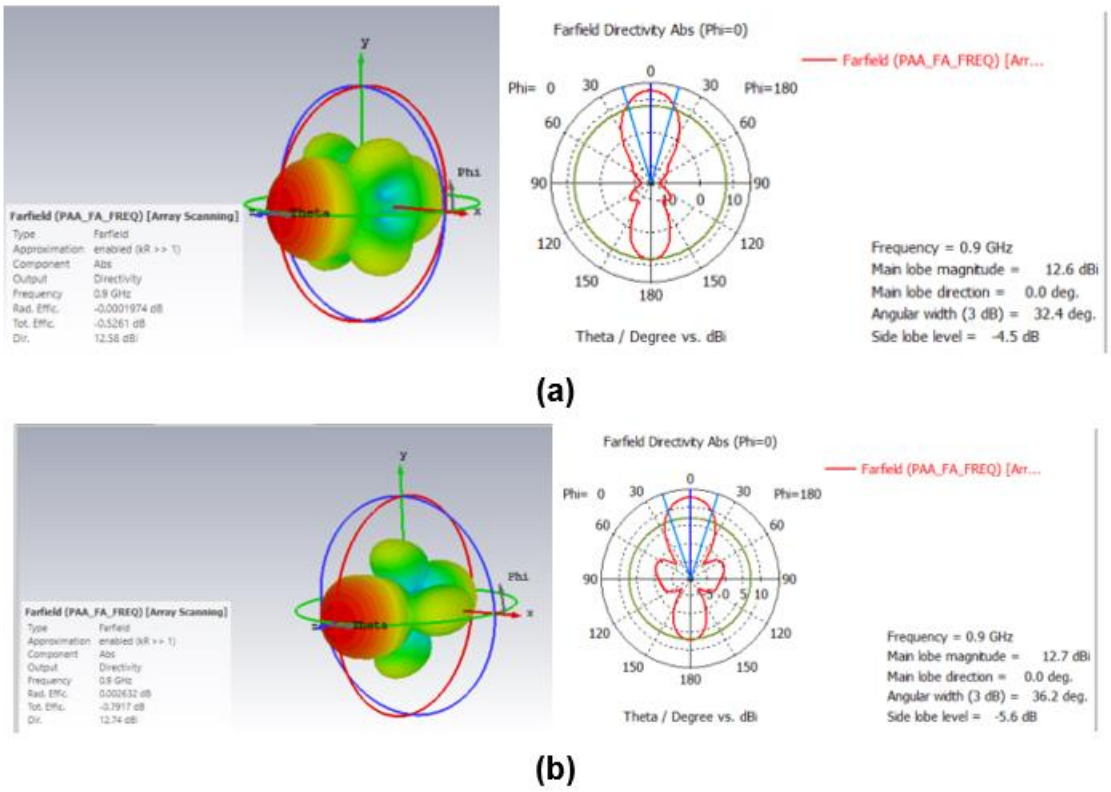


Figure 5.3.9: Shark array radiation patterns: (a) hexagonal array (b) square array.

(G) The hexagonal array has a max gain of about 12.58 dBi at 900 MHz while the square array has a max gain of 12.74 dBi. The hexagonal array has a small decrease in max gain for having one less element, therefore the hexagonal array is more efficient. The hexagonal array has the same degradation in the scattering parameters between 1-2 GHz. A single element Shark antenna provides 2.72 dBi of gain at 900 MHz. For 9 element array, the expected gain at 900 MHz is 12.26 dBi, whereas the gain from array simulation is 12.7 dBi. Similarly, for a 8 element array, the expected gain at 900 MHz is 11.75 dBi, whereas the simulation gain is 12.6 dBi. This comparison confirms the benefits of single element Shark antenna are being carried over to the array.

In summary, the new approach of connected ground plane for Shark array antenna is improving the gain by 1 dBi over unconnected ground plane. The 1 dBi improvement from 11.6 dBi to 12.7 dBi is a decent improvement. In addition, the benefits of single element Shark antenna are being carried over into the Shark array antenna with appropriate choice of interelement spacing.

5.3.5 References:

[1] L. Desrumaux, A. Godard, M. Lalande, V. Bertrand, J. Andrieu and B. Jecko, "An Original Antenna for Transient High Power UWB Arrays: The Shark Antenna," in IEEE

Transactions on Antennas and Propagation, vol. 58, no. 8, pp. 2515- 2522, Aug. 2010, doi: 10.1109/TAP.2010.2050418.

5.4 Tradespace Analysis of Ultra-Wide-Band (UWB) Fractal Antenna

(Sai Indharapu and Kalyan Durbhakula)

5.4.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. The fractal antenna packs multiple resonances closely spaced together to generate an UWB response, thereby effectively utilizing the 2D space (i.e., the radiating patch space). Its high degree of freedom provides an opportunity to develop systematically modified patch shapes, which in turn leads to improved bandwidth while retaining high fidelity factor values.

Sub-Problem: Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

5.4.2 Tasks and Milestones / Timeline / Status

(A) Perform tradespace analysis of the fractal element radius *b* over the desired frequency range (4 GHz to 12 GHz) using the genetic algorithm (GA) optimization tool available in the commercial electromagnetic (EM) solver FEKO / FEB21 / Complete.

- Milestone: Provide a recommendation of an optimum value of *b* using OPTFEKO to minimize reflection coefficient or S11 (< –10 dB) / Complete.

(B) Perform tradespace study on different fractal shapes by changing the number of fractal segments to understand the number of segment effect on the impedance bandwidth / FEB21 / Complete.

- Milestone: Produce a detailed study of the antenna response such as S11, gain, and bandwidth by varying the number fractal segments / Complete.

(C) Apply the GA optimization tool on the fractal side length *b* over a wide frequency range (2 GHz to 12 GHz with 201 discrete frequency points) and number of fractal segments using OPTFEKO on the LEWIS cluster / MAR21 / Complete.

- Milestone: Reduce physical aperture area by 10% of its present design, reported in the FEB MSR, and demonstrate minimal or no change in S11, gain, and fidelity factor values / Complete.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a* / MAR21 / Complete.

- Milestone: Recommend a value of *a* to reduce the physical aperture area and increase aperture efficiency (>50%) with no variation in other antenna metrics / Complete.

(E) Frequency scale current fractal antenna design such that the center frequency of the resulting antenna equals 1.3 GHz **(NEW)** / MAY–JUL21 / Ongoing.

- Milestone: Modify antenna design with a center frequency equal to 1.3 GHz and achieve similar results (3:1 bandwidth at fc = 1.3 GHz, 3 dBi gain and >130% aperture efficiency at 900 MHz) to antenna design at center frequency ~7 GHz / Ongoing.

(F) Design and simulate antenna array structures composed of fractal antennas to analyze the effect of each structure on antenna response metrics (i.e., gain, radiation pattern, rE/V)

- Milestone: Recommend a best possible structure with reduced aperture area and minimal loss in gain **(NEW)** / MAY–JUL21 / Ongoing.

(G) Apply existing machine learning (ML) models available in Altair Hyperstudy (2021) on fractal antenna design to analyze and understand the viability of ML models for fast and efficient antenna metrics (S11) prediction and optimization. ML models can replace convectional EM simulators for faster optimization.

- Milestone: Recommend most accurate and efficient ML model available in Altair Hyperstudy (2021). **(NEW)** / MAY–AUG21 / Ongoing.

5.4.3 Progress Made Since Last Report

(E) Designed fractal antenna has been fabricated and tested; reflection coefficient (S11) of the fabricated antenna has been measured using a vector network analyzer.

(F) Tradespace analysis of antenna array

(F1) The antenna array of square lattice structure composed of 9 antenna elements has been designed and simulated.

(F2) The antenna array of diamond lattice structure composed of 5 antenna elements has been designed and simulated.

(G) Implementation of ML models

(G1) Radial basis function (RBF), least square regression (LSR), and hyperkriging (HK) are three different ML models which are employed individually to predict the reflection coefficient (S11) of the fractal antenna design.

(G2) Prediction accuracy of each ML model is studied by comparing it with feko output, training data size for each algorithm is varied.

5.4.4 Significant Finding(s) and Mission Impact

5.4.4.1 Summary to Date

(A) The initial analysis of the simulation results with fractal radius *b* equal to 1.8 yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO has been used as an optimization tool with fractal radius *b* as the optimization variable. The optimum value for *b* is found to be 1.66 mm. The optimization is carried out over 51 discrete frequency points.

(B) The addition of fractal elements (*N*) to the simple hexagon improved antenna metrics such as S11. To further investigate and understand the fractal elements, the number of segments in the fractal geometry has been varied. The improvement in bandwidth is observed as the value of *N* is increased from 6 to 14.

(C) The initial optimum value of *b* over 51 discrete frequency points is reported as 1.66 mm in task (A). To further increase the accuracy of the optimization algorithm and to find a more precise value for *b*, optimization is further performed over wider frequency points (201 discrete points between 2 GHz to 12 GHz).

(D) To further analyze *a*, OPTFEKO is employed to find the optimum value with the goal to decrease the physical aperture area, with the optimum value of *a* equals 8 mm antenna metrics such as S11, gain, and bandwidth are satisfactory as shown in the Table 5.4.1.

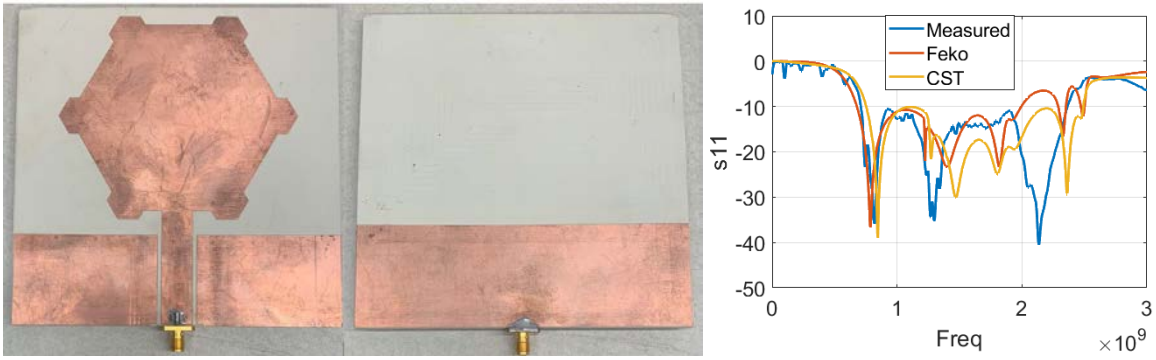
(E) The initial antenna design has been modified to achieve a center frequency of ~1.3 GHz. Antenna metrics such as gain, and bandwidth have no variation to the initial design. Designed antenna has been fabricated and tested, S11 response of the fabricated antenna has good agreement with Feko, CST.

(F) The tradespace analysis of two different array lattices has been studied, aperture area of two array's (i.e diamond lattice = 135.6 mm^2, square lattice = 366mm^2). Diamond lattice structure has 5 antenna elements, whereas square lattice structure has 9 elements. The inter element spacing between each element is set to be 240 mm (lambda/2).

(G) The initial prediction of reflection coefficient (S11) of the three ML models were satisfactory and have a good agreement with FEKO output for the same antenna design. In addition, RBF and LSR are down selected from the initial three ML models. To further analyze each ML model is trained with 4 different sizes of training data (i.e. 5, 10,15 and 20).

5.4.4.2 Since Last Report

(E) Fabricated antenna has been tested using a vector network analyzer (VNA). The measure S11 response of the fabricated antenna has a good agreement with S11 response of simulated antenna. The comparison of S11 response is illustrated in the figure 5.4.1

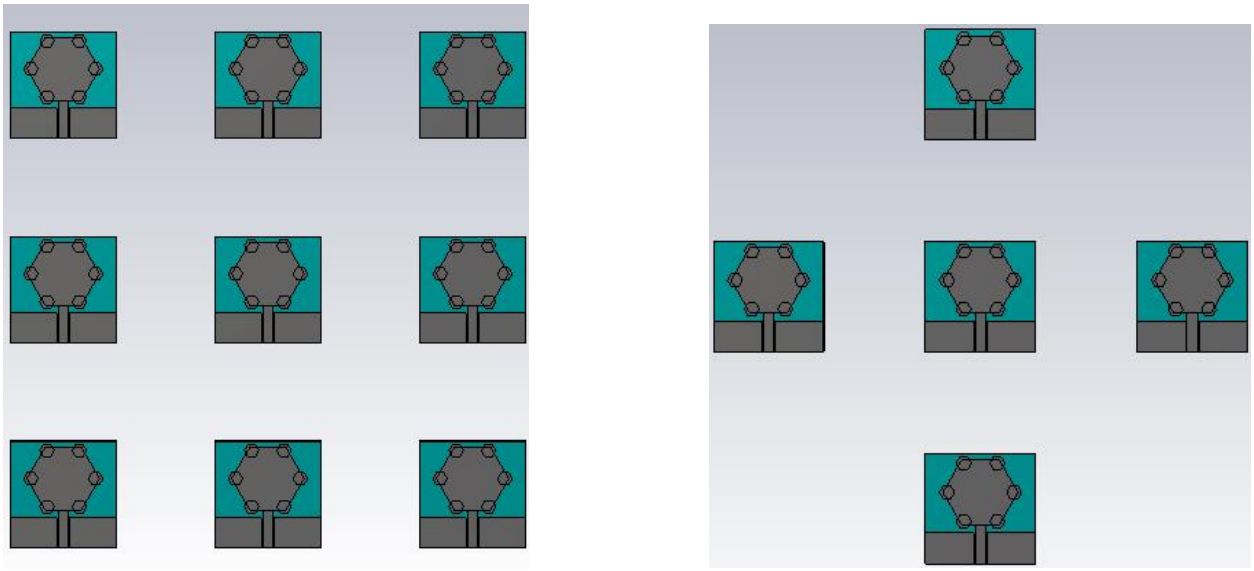


(a) (b)

Figure 5.4.1 (a) Fabricated antenna; (b) reflection coefficient (S11) comparison between Feko, CST, andmeasurement.

(F) The antenna array of diamond and square lattices composed of fractal antennas are simulated. Gain for both structures is observed at the center frequency (i.e. 900 MHz)

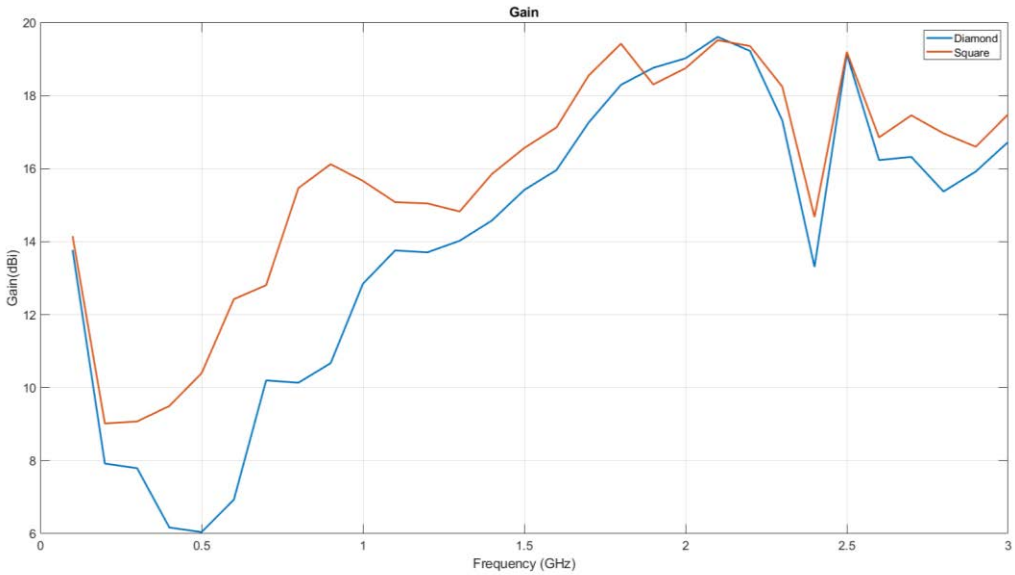
which can be observed from the table 5.4.1. The square lattice has extra elements than diamond lattice as shown in figure 5.4.2.



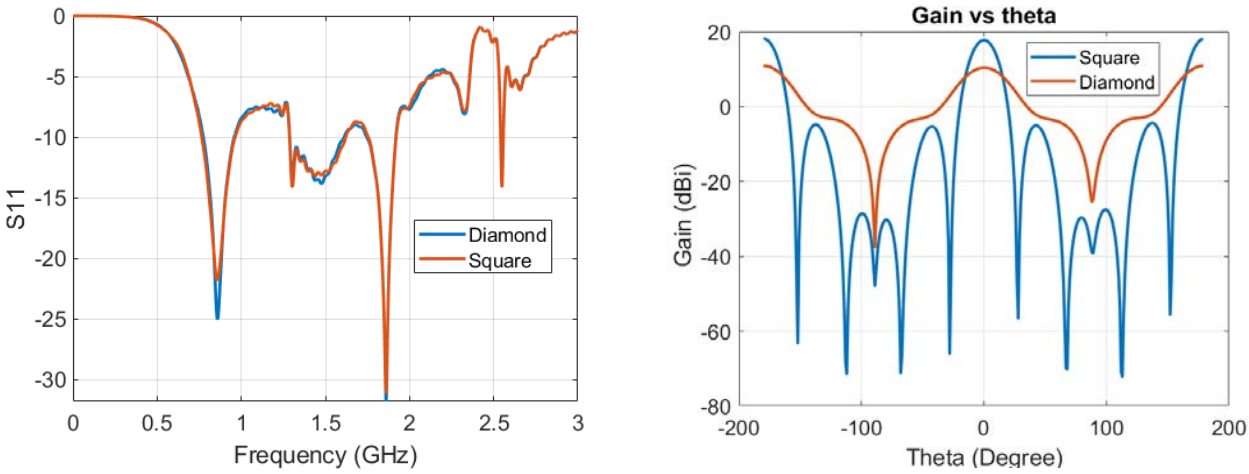
(a) (b)

Figure 5.4.2 (a) Square lattice, (b) diamond lattice.

The difference in gain value at 900 MHz between square and diamond lattice is significant, which can be seen in figure 5.4.3a. However, the center element S11 of both lattices cannot be separated by much due to λ/2 interelement spacing at 900 MHz. Although the gain from a diamond lattice shows a signficant decrease, the number of side lobes from a diamond lattice is minimal compared to square lattice. The near-future studies of fractal array antenna in diamond lattice will be focused at achieving gain values closer to that of square lattice without increasing the aperture area.



(a)



(b) (c)

Figure 5.4.3 (a) Gain in dBi; (b) S11 for center element; (c) gain vs theta for two different antenna array lattices.

Table 5.4.1 Fractal array antenna metrics comparision

Antenna array type	Physical Aperture area (m^2)	Peak gain (dBi) at (900 MHz)	HPBW at 900 MHz		Aperture Efficiency (900 MHz)
			E-plane	H-plane	
Square lattice	0.366	17.7409	17.5°	12.9°	143%
Diamond lattice	0.1356	10.3707	33.7°	21.4°	70%

(G) The predicted output (S11) from each ML model is plotted against the output response of EM simulator (i.e. FEKO) which is illustrated in Figure 5.4.4. Each model used for prediction is trained with 5 sets of input and output (training data) prior evaluation. Input for the ML model contains 5 different pairs of *'a'* and *'b'* whereas output has S11 results for 30 different frequency points over a range of 100MHz to 3GHz.

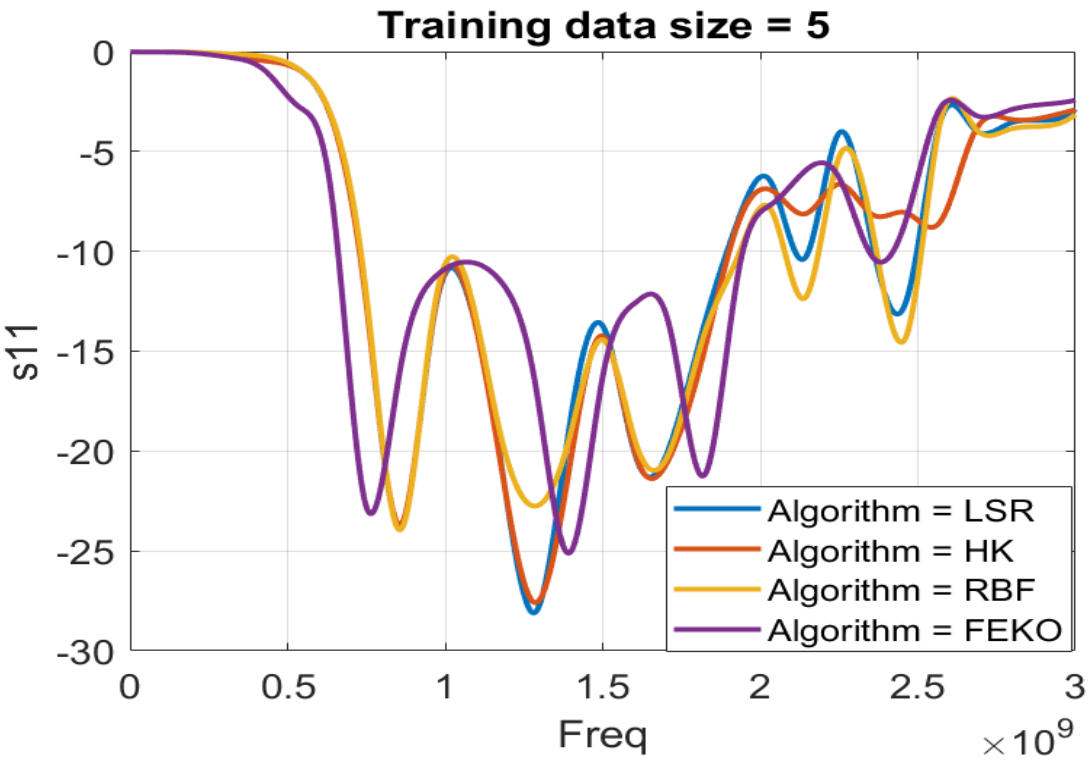


Figure 5.4.4. Reflection coefficient (S11) comparison of least square regression (LSR), hyperkriging (HK), and radial basis function (RBF) with FEKO.

From our initial studies, we have found the HK ML algorithm to display poor accuracy as the training dataset size is increased. Training dataset size used for each algorithm is increased to see if the prediction output accuracy increases. Four different training datasets sizes 5, 10, 15, and 20 respectively are considered. Each of this training dataset contains *'a'* and *'b'* as inputs and corresponding output (S11 response) for 30 different discrete frequency points over a range of 100 MHz to 3 GHz. The results of the above study are illustrated below in figure 5.4.5.

Except for training data size equal to 10, other three data size results from LSR and RBF are in agreement with FEKO as shown in figure 5.4.5a, 5.4.5b, and 5.4.5c, respectively. While the LSR and RBF agree with each other and with FEKO, the RBF is in better agreement with FEKO in terms of S11 values as well as the S11 bandwidth. These results indicate that RBF ML algorithm can be applied to predict S11 performance of a fractal antenna. The next study set will include determination and prediction of gain as a function of frequency and electric field as a function of time.

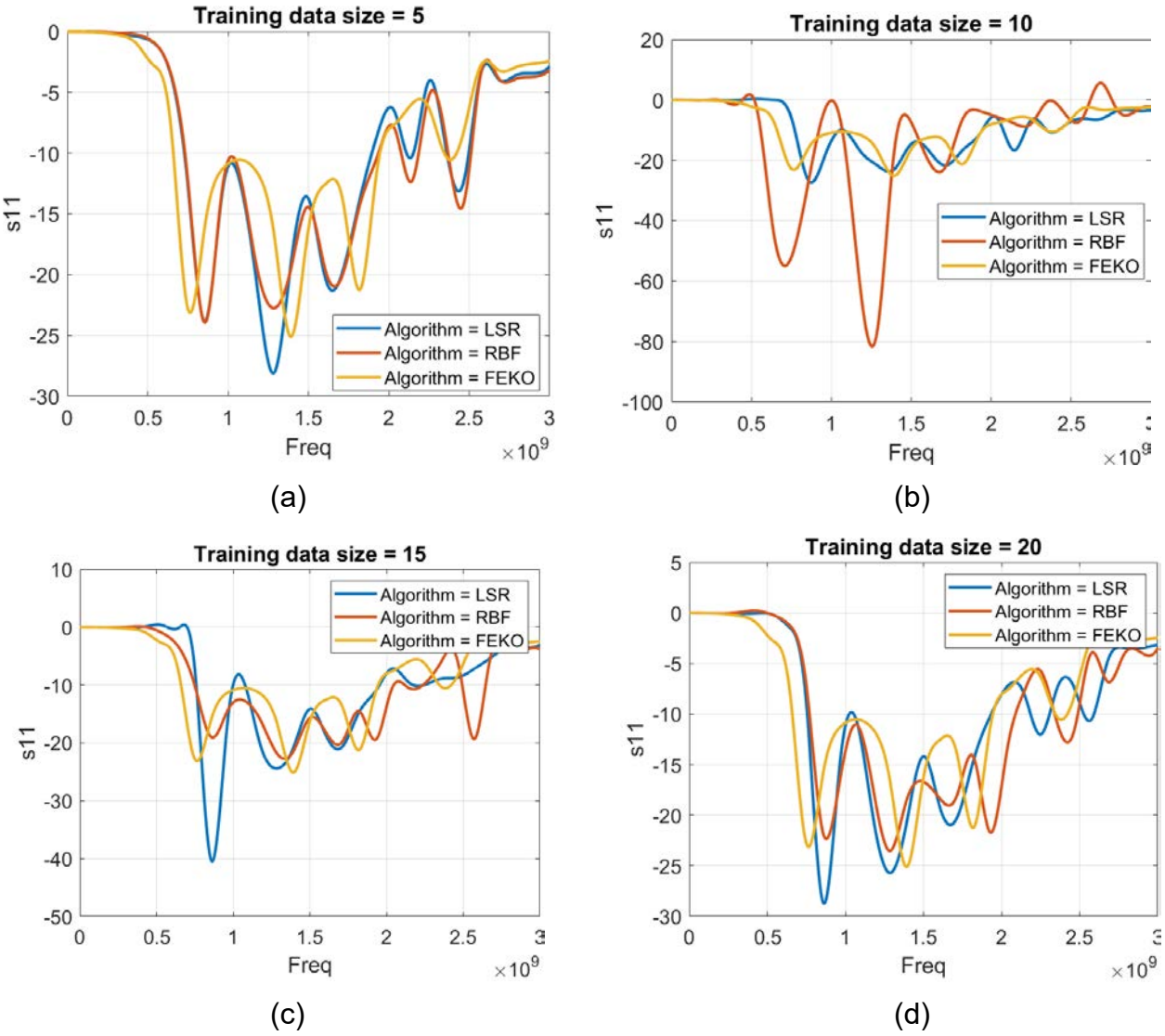


Figure 5.4.5 (a) Reflection coefficient (S11) comparison of LSR, RBF and FEKO for (a) training dataset size = 5, (b) training dataset size = 10, (c) training dataset size = 15, (d) training dataset size = 20.

5.4.5 References

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

6.0 RF Coupling

6.1 Enclosure Effects on RF Coupling

(Mohamed Hamdalla and Ahmed Hassan)

6.1.1. Problem Statement, Approach, and Context

Primary Problem: UAVs are typically considered metallic/dielectric enclosures depending on their frame material. The shielding effectiveness of such enclosures might be compromised due to the slots and gaps on these enclosures, creating upset susceptibility to the enclosed electronics. The goal of this work is to quantify how the thresholds for upset susceptibility of enclosed wires and integrated circuits differ from those in free space.

Solution Space: Study enclosures with different shapes, material compositions, and slots to quantify their effect on RF coupling to the enclosed wires and electronics typically used in UAVs. The study will focus on the low-frequency range where the incident wavelength is comparable to the size of the enclosure or larger.

Sub-Problem: UAVs are manufactured with a wide variety of shapes and composites to accomplish an exponentially expanding list of missions. The configurations previously reported in the literature have simplistic assumptions regarding the shape and material composition of UAV enclosures that might overestimate or underestimate susceptibility.

State-of-the-Art (SOTA): Simple statistical analysis of specific enclosure configurations using either brute force simulations/measurements or pure statistical methods. Also, simplified UAV wire distributions are assumed.

Deficiency in the SOTA: Brute force simulations/measurements of the voltages and currents induced in wires and integrated circuits contained in enclosures are computationally or experimentally complex and have several limitations. The computations are complicated by the multiscale nature of the simulations, and the experiments are complicated by the cost of the equipment and the extensive time needed to measure every variation to cover all possible scenarios. Statistical methods, such as the Random Coupling Model (RCM) for example [1], are only accurate for high frequencies where the wavelength is much smaller than the size of the enclosure. Another main deficiency of the RCM is that it can't predict the exact induced voltages and currents for a specific well-characterized system but it only provides the statistical properties of these induced currents and voltages.

Solution Proposed: Apply Characteristic Mode Analysis (CMA) to identify the fundamental modes of the enclosure, current distribution, and the field pattern of each mode. This will allow us to predict the worst-case RF coupling scenarios without the need for lengthy simulations and/or expensive experimental measurements. The proposed approach can predict measurements at a fraction of the cost/time. Moreover, we propose to study RF coupling to realistic UAV wire distributions, experimentally reconstructed, when they are placed inside metallic/dielectric UAV enclosures.

Relevance to OSPRES Grant Objective: Provide general guidelines on how the environment, in this case, the enclosure, affects RF coupling and subsequent electromagnetic absorption to UAV wires and integrated circuits.

Risks, Payoffs, and Challenges: The modes depend mainly on the shape and material of the enclosure. Since UAVs have a wide variety of shapes and material compositions, a library of several UAVs needs to be studied before general quantitative conclusions can be drawn. Challenges can be mitigated by the use of the classification techniques of Machine Learning (ML). That is, different ML techniques will be evoked to detect hidden patterns on how the shape, material composition, and the shape/size location of slots correlate with the field enhancement inside the enclosure.

6.1.2 Tasks and Milestones / Timeline / Status

A. Complete the CMA implementation for studying the shielding effectiveness of metallic enclosures. Validate whether CMA can predict the worst-case shielding effectiveness of metallic enclosures as a function of their shapes. / JAN21 / Complete.

   A1. Prepare a manuscript for IEEE AWPL to document the progress done in A. / Ongoing.

B. Use CMA tool in (A) to predict the worst-case internal field magnitude of metallic and dielectric enclosures of ten COTS UAVs as a function of HPM waveform. / MAY21 / Ongoing.

C. Use the database in (B) to train a Machine Learning (ML) platform to predict RF coupling to enclosed wires and electronics. / OCT21 / Ongoing.

D. Progressively build an accurate representation of the UAV wiring system with all of the integrated circuit (ICs) and electronics to test assist the predictions of (c) and the experimental measurement of the actual UAV. / JUL21 / ongoing.

E. Address the 2021 UAV's semi-annual review recommendations to study arbitrarily shaped UAV wire distribution. / JUNE21 / Complete.

6.1.3 Progress Made Since Last Report

E1. The effect of the shape of the UAV wiring system is studied.

   E1.1. Previously, we created a full-wave model of a complete UAV with all of the wires and IC components to use as a numerical platform for studying effects and validating predictions. Figure. 6.1b shows the wiring diagram of the actual UAV with the different IC components. We built an accurate replica of the UAV in Fig. 6.1a using the full-wave electromagnetic solvers CST MWS and FEKO as shown in Fig. 6.1c. The wires' length and diameters match the values in the actual UAV in Fig. 6.1a and Table 6.1. As a first approximation, the CST/FEKO model has all the components modeled as linear 50 Ω loads. Thus, we were able to run

exhaustive numerical experiments to study the response to different electromagnetic excitations.

E1.2. The full UAV model developed in E1.1 was compared to the simplified UAV model shown in Fig. 6.1d. The rectangular patch of the simplified model is the same size as the controller in the accurate model shown in Fig. 6.1a. The lengths of the wires of the simplified model in Fig. 6.1d are similar in size to the corresponding wires of the accurate model in Fig. 6.1b.

E1.3. Each of the 4 wire of the simplified model in Fig. 6.1d are divided into 5 segments, and each segment is rotated with a random angle to create a random wire configuration. The rotation angles of the segments were chosen to maintain a practical representation of the wires above the quadcopter's frame. The rotation angles are in the plane of the UAV, thus, no variations in the wire's heights were studied since we assume that these wires are mounted on top of the frame with minimal height variations. One hundred different wire shapes were studied in this analysis. The sketch of the proposed arbitrary wired UAV representation is illustrated in Fig.6.2a. Each wire configuration is excited by 325 incident angles with 2 different polarizations. Therefore, a total of 650 different incident excitations were studied: 2 polarizations, $0^\circ<\theta<180^\circ$ with 15° increment, and $0^\circ<\varphi<360^\circ$ with 15° increment.

E1.4 Shape variations are also introduced to the accurate UAV wire model in Fig.1c. In this model, the shape of the wires in only one arm shape was varied, and 10 different shapes are studied. The number of shapes studied for the accurate model is significantly less than that of the simplified model due to the computational time requirements. More shapes will be studied in future MSRs.

6.1.4 Significant Finding(s) and Mission Impact

6.1.4.1 Summary to Date

A1. A fast full-wave tool that facilitates studying the effect of a metallic enclosure on shielding effectiveness has been developed Using CMA.

6.1.4.2 Since Last Report

a. For the simplified M=model, 100 different wire shapes were simulated. The coupled voltage to the load of interest was averaged over the 100 different shapes and 650 different angles of incidence and plotted in dashed red in Fig. 6.2b. The blue curve in Fig. 6.2b shows the voltage calculated at the load of interest using the UAV model in Fig. 6.1d with no shape variations. Fig. 6.2b shows that for a maximum frequency of 1 GHz, the shape variations cause, on average, small deviations in the coupled voltage in comparison to the reference UAV model in Fig. 6.1d. The reference UAV model, with no shape variations, shows a maximum difference of ~20% in the coupled voltage in comparison to the UAV models with deformed wire shapes shown

in Fig. 6.2a. Thus, at most frequencies in Fig. 6.2b, the reference UAV model is sufficient for predicting the worst-case coupled voltage.

b. The wire shapes of the accurate UAV wire model in Fig. 6.1c were also varied. However, the shapes of the wires in only one arm shape are varied, as shown in Fig. 6.3a. In this month, 10 different shapes were studied. Fig. 6.3a illustrates two cases of the randomly shaped representation of the UAV accurate model. Similar to the simplified model, the shape variations was limited to the vicinity of the frame. Each configuration was illuminated by the 650 different incident excitations previously described. The reference case in Fig. 6.3b represents the load voltage of the straight wire model over all angles of incidence, whereas the red dashed curve represents the load voltage averaged over all the incident angles and over the 10 different wire configurations. Again, Figure 6.3b shows that shape of the wires has a minimal effect on the coupled voltage to the load of interest. In future MSRs, we will increase the number of wire configurations studied to confirm the previous conclusion.

6.1.5 Future Work

a. Vary the shape of the wires in the four arms of the UAV and increase the number of configurations. Moreover, we will study different parameters such as pulsed excitations with variable center frequencies, pulse width, pulse repetition frequency, etc.

Table 6.1. Quadcopter's main circuitry components and wires.

Part function	***Part #***	***specs.***	***length***
motor feed lines	1	18 AWG	
ESC out power lines	2	16 AWG	
ESC in power lines	3	16 AWG	~20 cm
esc in signal	4	22 awg	25 cm
battery out	5	14 AWG	
battery to controller	6	22 AWG	
main controller (autopilot)	7		carrier board 9.5 cm X4.5 cm
GP.1575.25.4.A.02 GPS/Galileo 25*25*4mm 1575.42MHz Patch Antenna2	8	22 AWG	~20 cm
Readytosky® 2212 920KV Brushless Motors	9		
SimonK 30A ESC Brushless Speed Controller	10		
Pixhawk Power Module 5.3V BEC XT60	11		

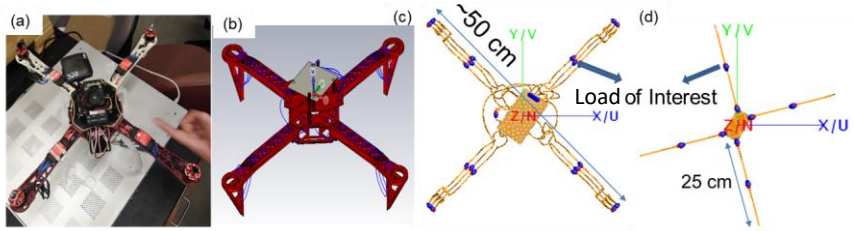


Fig. 6.1. (a) Model of the realistic UAV circuitry showing the wires, components, and frame, (b) the UAV wiring diagram showing all the wires and components, (c) the CST MWS model of the UAV in (a) and (b), (d) the simplified model of the UAV in (a) and (b).

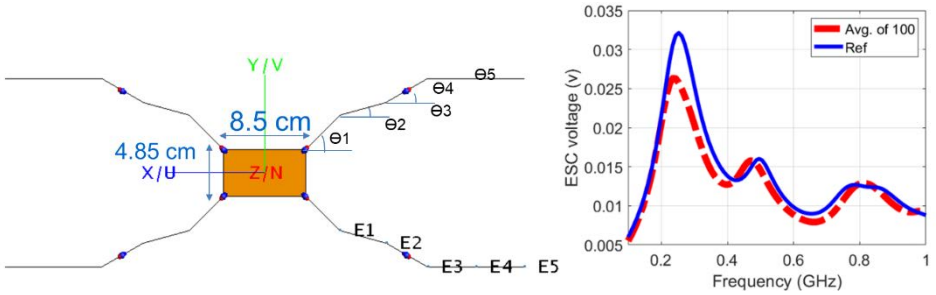


Fig. 6.2. (a) Sketch of the proposed arbitrary wired UAV representation when Θ1=45˚, Θ2=15˚, Θ3=30˚, Θ4=0˚, and Θ5=0˚ (b) the coupled voltage to the load of interest averaged over 100 different wire configurations of the model in (a).

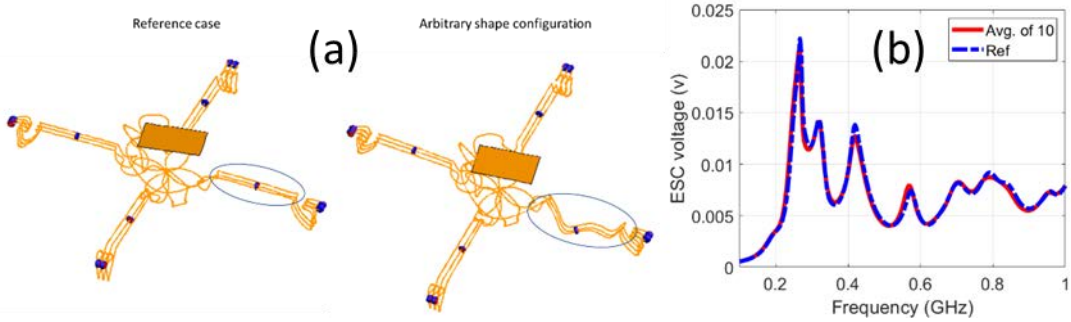


Fig. 6.3. (a) Sketch of the proposed arbitrary wired UAV representation showing two cases, one with straight wires and another with arbitrarily shaped wires on one of its arms (b) the coupled voltage to the load of interest averaged over 10 different wire configurations of the model in (a).

7.0 Thermal Management

7.1 Micro-Jet Thermal Management System

(Jordan Berg, Roy Allen, and Sarvenaz Sobhansarbandi)

7.1.1 Problem Statement, Approach, and Context

After wrapping up our assessment on the initial jet impingement thermal management system (TMS) technology and concluding that this is not a viable option moving forward, we are currently evaluating the possibility of future work on alternative TMSs for HPM systems in support of the Naval afloat mission. This sub-section is being included as a placeholder.

7.2 Nanofluid Heat Transfer Fluid Development

(Jordan Berg, Roy Allen, and Sarvenaz Sobhansarbandi)

7.2.1 Problem Statement, Approach, and Context

Primary Problem: Dielectric fluids (non-conductive coolant) used in thermal management systems, while suitable for high-voltage HPM-based technologies, possess inherent thermophysical fluid properties (low thermal conductivity, high viscosity) that inhibit their ability to achieve >1 GW/m^3 cooling densities.

Solution Space: Develop a nanofluid by entraining ceramic nanoparticles and dispersants within the dielectric base-fluid, pure silicon fluid (PSF), to increase the nanofluid's thermophysical properties and cooling density capabilities with a similar form-factor.

Sub-Problem: While the dynamic viscosity of the dielectric fluid used, PSF-20cSt, is 'low' relative to other silicone-based fluids, it is ~15 times more viscous than water, and therefore requires increased pumping power within the TMS. Compounding this issue is the necessity to increase the flowrate of the fluid to achieve an equivalent heat removal rate compared to that of a water-based coolant.

State-of-the-Art (SOTA): Nanofluids, with optimal ratios of fluid-to-nanoparticles, have been shown to increase the thermal conductivity of dielectric fluids by 87% in comparison to the generic dielectric fluid alone; resulting in either greater cooling density, decreased pumping power, or reduced mass flow rate requirements.

Deficiency in the SOTA: The addition of nanoparticles within a base-fluid results in a tradeoff between one or more thermophysical properties. For example, adding nanoparticles may increase thermal conductivity of the nanofluid but may result in increased viscosity; i.e., heat removal rate may increase, but the required pumping power along with it. To the best of our knowledge, no one has attempted to create a nanofluid mixture with a goal of keeping the viscosity low. Therefore, the optimal nanoparticle-to-fluid ratio and specific nanoparticle type for the HPM thermal management systems needs to be identified and optimized with an attempt to maintain the viscosity of the mixture as low as possible.

Solution Proposed: Develop a nanofluid with both desirable thermal properties and a relatively low viscosity that can serve as a viable heat transfer fluid (HTF) for TMSs in HPM topologies and other high power density applications. Utilize systematic numerical and experimental strategies to evaluate a large sample set of various nanoparticles (with surfactants and dispersants).

Relevance to OSPRES Grant Objective: Increase cooling densities for HPM systems without requiring TMS design permutations, while decreasing pumping power requirements, in-line with the SWaP-C^2 objective.

Risks, Payoffs, and Challenges:

Risk: The pressures incurred by using a silicone-based fluid in a high-flow regime are not insignificant; large pump-chiller systems may still be necessary.

Challenges: Creating low volume-fraction samples of nanoparticles and surfactants is near equipment precision limit. Maintaining accuracy is critical to properly study modified fluids.

Payoff: A modified nanofluid dielectric fluid can be used to increase cooling capacity of any high power density system. An optimized nanofluid has the potential to extract 20% up to several factors more than the base fluid.

7.2.2 Tasks and Milestones / Timeline / Status

(A) Measure thermophysical properties of currently utilized PSF-20cSt / DEC20–JAN21 / Completed.

(B) Establish theoretical model of nanofluid compositions / DEC20–JAN21 / Completed.

(C) Create and test modified PSF-20cSt with nanoparticles and surfactants / JAN–MAR21 / Completed.

(D) Select the nanofluid mixture with optimal thermal properties and re-evaluate the CFD modeling / MAR–APR21 / Completed.

7.2.3 Progress Made Since Last Report

(A) 18 nanofluids and the control have been prepared and tested in the differential scanning calorimeter (DSC) to determine the specific heat capacity of each sample.

(B) Several samples show desired specific heat capacity change relative to the base fluid.

7.2.3.1 Summary to Date

Based on literature, the creation of a dielectric nanofluid for use as a coolant in the HPM system could potentially improve cooling performance. The thermal dissipation requirements for HPM systems are not insignificant and could, therefore, benefit from performance enhancement from every aspect (geometric optimization, reduction of thermal resistances, coolant selection, material selection, etc.). A sample of the PSF-20cSt that was used in the experimental testing of the JI-TMS was tested with a Differential Scanning Calorimeter (DSC). The specific heat of the fluid was found to

significantly differ from that of the manufacturer's value. The vendor's reported value of the PSF-20cSt was 1.6 $\frac{J}{gC}$, while DSC measurements showed it to be closer to 1.4 $\frac{J}{gC}$. This difference hinders the accuracy of the CFD results of the TMS. Given the aforementioned error in specific heat capacity, coupled with the need for a high thermal performance coolant, nanoparticle-modified PSF-20cSt was determined to be a necessary and useful undertaking. Three different ceramic nanoparticles were chosen to be studied: alumina, silicon carbide, and iron (II,III) oxide. Ceramics were chosen to maintain HTF dielectric properties. 18 nanofluid samples were tested for heat capacity enhancement. Of the 18 samples tested, the sample that showed the greatest heat capacity decrease was chosen, as theoretically, the largest heat capacity decrease correlates with the largest thermal conductivity increase. The sample that achieved the great heat capacity drop was the 0.25 wt.% silicon carbide with surfactants, achieving a value of 1.254 $\frac{J}{gC}$.

7.2.3.2 Since Last Report

Using the heat capacity data that was recorded one month prior that is summarized in Table 7.2.1, the sample that showed the greatest heat capacity decrease (sample 1 in Table 7.2.1) was estimated using a modified Maxwell equation. As thermal conductivity increases with the largest heat capacity drop, only sample 1 was studied further. Sample 1 was sent to a third party to have the thermal conductivity determined. In the interim, the theoretical thermal conductivity of sample 1 was determined to be 0.147 W/mK. This compares to the vendor reported value of the pure silicone fluid of 0.142 W/mK. The thermal conductivity increase for sample 1 showed a 3.5% increase over the base fluid. The CFD model was then updated with the new theoretical thermal conductivity value achieved with sample 1. Shortly after the CFD model was updated with the theoretical thermal conductivity, the measured thermal conductivity was received. The measured value was determined to be 0.197 W/mK. This value was a major improvement over the vendor's claimed 0.142 W/mK value, representing a 32.4 % increase. Again, the CFD model was updated with the measured thermal conductivity value. Table 7.2.2 summarizes the results from each average power test (100 W and 200 W dissipated by the PCSS) for the base fluid CFD, theoretical CFD, measure CFD and experimental results with the base fluid.

Table 7.2.1. DSC heat capacity values of nanofluid samples

Sample #	Sample	C_p (J/gC)	Std Dev (%)
1	Silicon Carbide 0.25 wt %	1.254	0.04
2	Silicon Carbide 0.5 wt %	1.441	0.38
3	Silicon Carbide 0.75 wt %	1.442	0.39
4	Silicon Carbide 0.25 wt %*	1.538	2.33
5	Silicon Carbide 0.5 wt %*	1.570	1.14
6	Silicon Carbide 0.75 wt %*	1.451	0.10
7	Iron Oxide 0.25 wt %	1.464	0.26
8	Iron Oxide 0.5 wt %	1.549	0.50
9	Iron Oxide 0.75 wt %	1.59	0.86
10	Iron Oxide 0.25 wt %*	1.458	0.23
11	Iron Oxide 0.5 wt %*	1.462	0.13
12	Iron Oxide 0.75 wt %*	1.402	0.69
13	Aluminum Oxide 0.25 wt %	1.632	1.21
14	Aluminum Oxide 0.5 wt %	1.399	0.79
15	Aluminum Oxide 0.75 wt %	1.544	0.18
16	Aluminum Oxide 0.25 wt %*	1.376	0.25
17	Aluminum Oxide 0.5 wt %*	1.378	0.54
18	Aluminum Oxide 0.75 wt %*	1.430	1.17
19	PSF-20cSt	1.391	0.58

* No surfactant sample

Table 7.2.1. DSC heat capacity values of nanofluid samples

Max Semiconductor Temperature					
Test	**PSF k CFD**	**Theoretical k CFD**	**Measured k CFD**	**Experimental**	**% Improvement**
100 W	54.7	54.36˚C	46.67˚C	57.5˚C	18.8
200 W	99.0	90.18˚C	83.49˚C	98.2˚C	14.9

The goal of this project is to maintain the PCSS under 80˚C while the PCSS dissipates a certain amount of power is dissipated as heat. The results from Table 7.2.2 show that in every case, the 100 W average power dissipated by the PCSS was kept well below 80˚C. For the 200 W average power case, the 80˚C threshold was always exceeded. However, with the utilization of nanofluids as a coolant, the maximum PCSS temperature was dropped significantly. The measured thermal conductivity CFD model shows a 18.8% and 14.9% drop in maximum PCSS temperature seen by the PCSS. The results show that a significant heat transfer performance for the thermal management system is achievable using a small mass fraction of nanoparticles in the heat transfer fluid. For this reason, a heat transfer nanofluid will likely be implemented in future thermal management systems for the PCSS and similar high-power density electronics.

8.0 UAS Engagement Wargaming & Modeling and Simulation (M&S)

8.1 Airborne Effector Weapon Task Assignment

(Cody Smith and Travis Fields)

8.1.1 Problem Statement, Approach, and Context

Primary Problem: Over the past decade, due to rapidly evolving technology, the threat of autonomous small unmanned aircraft systems has greatly increased in both civilian and military environments. Their low cost, ease of use, low risk, and versatility have military commanders and civilian security managers racing to develop effective countermeasures. Technological development trends suggest the potential for the application of both coordinated and cooperative hostile sUAS attacks in the near future. Defense strategies are currently under development which primarily utilize aerial- or ground-based defense systems or a layered combination of the two. An engagement with multiple blue (friendly) vehicles against many red (hostile) vehicles presents an interesting challenge in assigning which blue engages which red(s). The problem complexity grows factorially with the number of hostile vehicles, which can easily be unrealizable on modern computer or embedded systems.

Solution Space: We propose to combine the Moving Traveling Salesman Problem with Genetic Algorithms with constraints in order to produce computationally efficient sub-optimal task assignment allocations to the blue forces.

State-of-the-Art (SOTA): Many current techniques consider stationary targets and/or holonomic vehicles, which within the proposed scenario is not applicable. Considering the task assignment problem with constrained (or realistic flight-like) motion with many potential targets that must be intercepted with several friendly assets is a unique (at least in the literature) problem.

Relevance to OSPRES Grant Objective: The concepts for weapon task assignment (WTA) are applicable to both fixed and airborne weapon systems. Developing the strategies for assigning assets is critically important for considering layered defense scenarios, as the battlefield is now heterogenous with a diverse array of capabilities, performance, and cost.

8.1.2 Tasks and Milestones / Timeline / Status

(A) Literature review on task assignment-related studies/research activities / MAR21–MAY21 / Completed.

(B) Implementation and evaluation of engagement-level WTA (one vs. few) in simulated environment / MAY21–JUN21 / In Progress.

(C) Implementation and evaluation of mission-level WTA (few vs. many) in simulated environment / JUN21–JUL21 / Upcoming.

(D) Identification and dissemination of WTA paradigm for airborne effector program / AUG21–SEP21 / Upcoming.

8.1.2.1 Summary to Date

The current study aims to develop a framework comprised of the necessary algorithms required for effective weapons target assignment (WTA) optimization for both aerial- and ground-based weapons during hostile unmanned aerial threat engagements. Historically, path-planning algorithms like the Traveling Salesman Problem and the Vehicle Routing Problem have been utilized for WTA. The development of an effective WTA framework will require a combination of features from several of these common path planning algorithms: for example, the Traveling Salesman Problem with Neighborhoods to manage conditions where direct interception is not required, the Moving Traveling Salesman Problem where incoming hostile targets are known to be moving, and the Dynamic Traveling Salesman Problem where assigned paths are updated with the emergence of previously unknown threats. Because this framework is being developing using NP-combinatorial optimization algorithms, increasing the number of targets rapidly causes the WTA problem to become computationally intractable. Various heuristics are to be studied and a comparative analysis is to be performed against several other popular path planning algorithms (i.e. auction and genetic algorithms) to gain insight and develop situational strategies for potential aerial threats.

9.0 Program Management

9.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

9.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

9.3 Major Procurement Actions

i. Microsoft Office 365 GCC High (75 seats) - $45,000 (for OSPRES Contract CUI Compliance)

9.4 Travel

Destination	Purpose	Attendees	Estimated Costs

9.5 Pending or Upcoming Public Release Requests

10.0 Appendix B: Academic and IP Output

10.1 Students Graduated

Name	Degree	Currently
Al-Shaikhli, Waleed Berg, Jordan	MS Spring 19 MS Spring 21	Kansas City National Security Campus, Honeywell
Bissen, Bear	MS Spring 19	UMKC/MIDE (Staff)
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Hanif, Abu	PhD May 21	
Harmon, Aaron	BS	Missouri University of Science & Technology
Harp, Joshua	MS	Small Business
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Klappa, Paul	MS Spring 21	
Labrada, Dario	BS Spring 20	UMKC/MIDE (MS Student)
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory
Renzelman, Jeff	MS Spring 18	Kansas City National Security Campus, Honeywell
Roy, Sourov	PhD Spring21	UMKC/MIDE (Staff)
Wagner, Adam	MS Fall 20	Kansas City National Security Campus, Honeywell
Xia, Shengxuan	BS	Missouri University of Science & Technology

10.2 Conference Publications

[1] B. Barman, D. Chatterjee, and A. N. Caruso, “Effect of Ground Plane Shape and Size on the Input Impedance of a Monopole embedded in a Grounded Dielectric Substrate,” submitted to the *2021 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*, Marina Bay Sands, Singapore, December 4-10, 2021.

[2] B. Barman, D. Chatterjee, and A. N. Caruso, “Comparison of Q-Factor Calculation Methods for Wideband Microstrip Patch Antennas,” submitted to the *2021 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*, Marina Bay Sands, Singapore, December 4-10, 2021.

[3] S. R. Shepard and H. A. Thompson, “Self-focusing in Guided and Un-guided Media,” submitted to the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, 2021.

[4] B. Barman, D. Chatterjee, and A. N. Caruso, “Probe-location Optimization in a Wideband Microstrip Patch Antenna using Genetic Algorithm, Particle Swarm and Nelder-Mead Optimization Methods,” accepted in *2021 International Applied Computational Electromagnetics Society (ACES) Symposium*, USA, August 1-5, 2021.

[5] W. Azad, S. Roy, and F. Khan, "A Single Gate Driver-based Four-stage High-voltage SiC Switch Having Dynamic Voltage Balancing Capability," *2021 IEEE Applied*

Power Electronics Conference and Exposition (APEC), Phoenix, AZ, USA, June 9-12, 2021.

[6] W. Azad, S. Roy, F. Khan and A. N. Caruso, "A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuits," *2021 IEEE Kansas Power and Energy Conference* (KPEC), Manhattan, KS, USA, April 19-20, 2021 [doi].

[7] T. Layman, T. D. Fields, and O. A. Yakimenko, "Evaluation of Proportional Navigation for Multirotor Pursuit," AIAA SciTech Forum, Virtual Event, January 11-21, 2021 [doi].

[8] P. J. Klappa, and T. D. Fields, "Assessment of Fixed-Wing UAV System Identification Models during Actuator and Payload Drop Failures," AIAA Atmospheric Flight Mechanics Conference, Virtual Event, January 11-21, 2021 [doi].

[9] J. Hunter, S. Xia, A. Harmon, A. M. Hassan, V. Khilkevich, and D. Beetner, "Modeling and Statistical Characterization of Electromagnetic Coupling to Electronic Devices," *IEEE International Symposium on Antennas and Propagation and NSRM USNC-URSI National Radio Science Meeting*, Boulder, CO, January 4-9, 2021 [doi].

[10] B. Barman, K. C. Durbhakula, B. Bissen, D. Chatterjee, and A. N. Caruso, "Performance Optimization of a Microstrip Patch Antenna using Characteristic Mode and D/Q Analysis," *2020 XXXIIIrd General Assembly and Scientific Symposium of the International Union of Radio Science*, Rome, Italy (online conference), Aug 29-Sept 5, 2020, pp. 1-4 [doi].

[11] J. Berg, and S. Sobhansarbandi. "CFD Modeling of Thermal Management Systems for a Silicon Semiconductor Switch." *ASME 2020 Heat Transfer Summer Conference collocated with the ASME 2020 Fluids Engineering Division Summer Meeting and the ASME 2020 18th International Conference on Nanochannels, Microchannels, and Minichannels*, Virtual, July 13–15, 2020, American Society of Mechanical Engineers Digital Collection [doi].

[12] B. Barman, D. Chatterjee, and A. N. Caruso, "Performance Optimization of Electrically Small Microstrip Patch Antennas on Finite Ground Planes," 2020 *IEEE International Symposium on Antennas and Propagation and North American Radio Science Meeting*, Montreal, Quebec, Canada, July 5-10, 2020, pp. 1–2 (online conference) [doi].

[13] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, "Scalable Characteristic Mode Analysis: Requirements and Challenges (White Paper)," *Large Scale Networking (LSN) Workshop on Huge Data: A Computing, Networking and Distributed Systems Perspective Sponsored by NSF*, Chicago, IL, April 13-14, 2020.

[14] M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Predicting Electromagnetic Interference to a Terminated Wire Using Characteristic Mode Analysis," *Proceedings of the Annual Review of Progress in Applied Computational Electromagnetics (ACES)*, Monterey, CA, March 22-26, 2020.

[15] W. Azad, F. Khan, and A. Caruso, "Self-sustaining High-power RF Signal Generation Using LDMOS Based Power Amplifier and Nonlinear Transmission Line," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 3567-3572 [doi].

[16] A. Hanif, W. Azad, and F. Khan, "Detection of Bond Wire Lift Off in IGBT Power Modules Using Ultrasound Resonators," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 345-350 [doi].

[17] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, "Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS," *Annual Directed Energy Science and Technology Symposium*, March 2020 (abstract appeared, but talk cancelled due to pandemic).

[18] B. Barman, D. Chatterjee, and A. N. Caruso, "Some Investigations into Mutual Coupling Analysis for Trade Space Studies of Linear Arrays," *2019 IEEE International Symposium on Phased Array Systems and Technology (PAST)*, Waltham, MA, October 2019, pp. 1-8.

[19] B. Barman, D. Chatterjee, and A. N. Caruso, "Characteristic Mode Analysis of a straight and an L-probe fed Microstrip Patch," *2019 IEEE Indian Conference on Antennas and Propogation (InCAP)*, Ahmedabad, India, Dec 2019, pp. 1-3.

[20] M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of the Effect of the UAV Frame Material on Coupling and Interference," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019.

[21] M. Hamdalla, J. Hunter, Y. Liu, V. Khilkevich, D. Beetner, A. Caruso, and A. M. Hassan, "Electromagnetic Interference of Unmanned Aerial Vehicles: A Characteristic Mode Analysis Approach," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019.

[22] B. Barman, D. Chatterjee, and A. N. Caruso, "Analytical Models for L-Probe fed Microstrip Antennas," *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

[23] K. C. Durbhakula, J. Lancaster, J. Hunter, Y. Liu, D. Beetner, V. Khilkevich, D. Chatterjee, A. N. Caruso, and A. M. Hassan, "Electromagnetic Coupling Analysis of Printed Circuit Board Traces using Characteristic Mode Analysis," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (2 pages)*, Atlanta, Georgia, USA, July 7-12 2019.

[24] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "On the Location of Transverse Electric Surface Wave Poles for Electrically Thick Substrates," Proceedings of the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019.

[25] M. Hamdalla, B. Bissen, A. N. Caruso, and A. M. Hassan, "Experimental Validations of Characteristic Mode Analysis Predictions Using GTEM Measurements," *IEEE*

International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting, Montréal, *Québec, Canada, July 5-10, 2020*.

[26] W. Azad and F. Khan, “Sustaining High-power RF Signal Generation in a Positive Feedback Network," *2019 IEEE Pulsed Power and Plasma Science Conference (PPPS)*, Orlando, FL, USA, June 23-28 2019.

[27] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, “Scalable characteristic mode analysis using big data techniques,” *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[28] M. Hamdalla, W. Al-Shaikhli, J. Lancaster, J. D. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, “Characteristic Mode Analysis of Electromagnetic Coupling to Wires with Realistic Shapes,” *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[29] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “Location of Surface Wave Poles in Sommerfeld Integrals: A Mittag-Leffler Expansion Approach,” *Proceedings of the URSI-B International Symposium on Electromagnetic Theory*, URSI Commission, San Diego, USA, May 2019.

[30] D. Chatterjee, B. Barman. J. Kovarik, and A. N. Caruso, “Studies on Antenna Characterization and Propagation of High Power Pulsed Electromagnetic Waves with Minimal Spatial Dispersion,” presented at the *Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium*, Destin, Florida, USA, April 2019.

[31] J. Kovarik, B. Barman, D. Chatterjee and A. N. Caruso, “Some Investigations into Applications of Electrically Small Antennas as Phased Array Elements,” presented at the *Directed Energy Professional Society* (DEPS) *Annual Science and Technology Symposium*, Destin, Florida, USA, April 2019.

[32] K. C. Durbhakula, D. Chatterjee and A. M. Hassan, “Analytical Evaluation of Sommerfeld Integral Tails Present in Two-layered Media Green’s Functions,” *Proceedings of the Indian Conference on Antennas and Propagation* (InCAP), Hyderabad, India, December 2018.

[33] D. Beetner, V. Khilkevich, A. M. Hassan, J. Hunter, Y. Liu, and D. Floyd, *“*Characterization of the Electromagnetic Coupling to UAVs,*”* *DE Systems Symposium*, September 24-27, 2018

[34] C. Hartshorn, K. Durbhakula, D. Welty, D. Chatterjee, J. Lancaster, A. M. Hassan, and A. N. Caruso, “Crosstalk and Coupling to Printed Circuit Board Metallic Traces with Arbitrary Shapes,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[35] M. Hamdalla, J. Roacho-Valles, J. Hunter, D. Beetner, A. M. Hassan, and A. N. Caruso, “Electromagnetic Analysis of Unmanned Aerial Vehicles Using Characteristic Mode Analysis,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[36] C. Hartshorn, M. Hamdalla, J. Lancaster, A. M. Hassan, and A. N. Caruso, “Electromagnetic Vulnerability of Wires with Arbitrary Shape,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[37] K. C. Durbhakula, D. Chatterjee, A. M. Hassan, and M. S. Kluskens, “Studies on Numerical Evaluation of Sommerfeld Integrals for Multilayer Topologies,” *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018.

[38] J. Lancaster, D. Chatterjee, and A. N. Caruso, “Some Investigations into the Dispersion Characteristics of Localized Bessel Beams,” published in the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018 (1 page URSI Abstract).

[39] M. Hamdalla, A. M. Hassan, and A. N. Caruso “Characteristic Mode Analysis of Unmanned Aerial Vehicles with Realistic Shapes and Material Composition,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Boston, MA, July 8-13, 2018.

[40] W. Azad, S. Roy, A. S. Imtiaz, and F. Khan, "Microelectromechanical System (MEMS) Resonator: A New Element in Power Converter Circuits Featuring Reduced EMI," *2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, Niigata, May 20-24, 2018, pp. 2416-2420 [doi].

[41] J. Hunter, Y. Liu, D. Floyd, A. Hassan, V. Khilkevich, and D. Beetner, “Characterization of the Electromagnetic Coupling to UAVs,” Annual Directed Energy Science and Technology Symposium, Feb 26-March 2, 2018.

10.3 Journal Publications

10.3.1 In Preparation

[1] B. Barman, D. Chatterjee, and A. N. Caruso, “Tradespace analysis of wideband coaxial probe-fed microstrip patch electrically small antenna elements,” In preparation, **2021**.

[2] W. Azad, F. Khan, and A. N. Caruso, “A Custom High-Voltage Isolated Gate Driver Circuit Combined With Coupling, and Snubber Circuits for a Scalable Multilevel – Modular 10 kV Silicon Carbide MOSFET Module,” In preparation for IEEE Transactions on Power Electronics, **2021.**

[3] M. Z. M. Hamdalla, B. Bissen, J. D. Hunter , L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, “Experimental Evaluation of CMA Predictions and Control of Electromagnetic Interference to UAVs,” In Preparation, **2021**.

[4] S. Xia, J. Hunter, A. Harmon, M. Hamdalla, A. Hassan, V. Khilkevich, D. Beetner, “Simulation Driven Statistical Analysis of the Electro-magnetic Coupling to Microstriplines,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[5] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, "Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field Coupling to Randomly Shaped Wires," *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

9.2.2 Submitted / Under Revision

[6] J. N. Berg, R. C. Allen, and S. Sobhansarbandi. "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation." *International Journal of Thermal Sciences*, Submitted, **2021**.

[7] Khulud Alsultan, Mohamed Hamdalla, Sumitra Dey, A. N. Caruso, Praveen Rao, and A. M. Hassan, "Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform," *IEEE Open Journal of Antennas and Propagation,* Submitted, **2020**.

[8] John Keerthi Paul Bhamidipati, Eliot R. Myers, Adam M. Conway, Lars F. Voss, and Anthony N. Caruso, "Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches," *IEEE Transactions on Electronic Devices*, Under Revision, **2020**.

10.3.2 Published / In Press

[9] W. Azad, F. Khan, and A. N. Caruso, "A Medium Power, Self-Sustaining, Configurable RF Pulse Generation Circuit Using a Nonlinear Transmission Line and Power Amplifier in a Closed Loop Configuration, *IEEE Transactions on Plasma Science*, Accepted, **2021**.

[10] S. Roy, W. Azad, S. Baidya and F. Khan, "A Comprehensive Review on Rectifiers, Linear Regulators and Switched-mode Power Processing Techniques used for Powering Biomedical Sensors and Implants utilizing In-body Energy Harvesting and External Power Delivery," *IEEE Transactions on Power Electronics*, Early Access, **2021** [doi].

[11] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems," *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364-373, **2019** [doi].

10.4 Conference Presentations

[1] W. Azad, S. Roy, and F. Khan, "A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver," *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, 2020 (oral).

DEPS Posters and Presentations 2020

[1] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[2] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

GOMAC 2019

[3] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[4] Eliot Myers, Picosecond High Power Switching Technologies

[5] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

DEPS Posters and Presentations 2019

[6] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[7] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[8] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[9] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[10] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[11] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[12] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[13] Deb Chatterjee, Studies On Antenna Characterization And Propogation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

DEPS Posters and Presentations 2018

[14] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[15] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[16] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

DEPS Posters and Presentations 2017

[17] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

10.5 IP Disclosures Filed

Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, 19UMK005, 28SEPT2018

Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal”, 19UMK008, 28DEC2018.

Doynov, “Pulse Differential High-power Microwave Generation”, 19UMK007, 02JAN2019.

Doynov, “Scalable Modular System for High-power Microwaves Generation”, 20UMK010, 19APR2020.

Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna”, 20UMK011, 19APR2020.

Shepard, “A Novel Optical Fiber Amplifier”, 20UMK012, 02JUN2020.

Doynov, Caruso, “High-efficiency High-power Microwave Generation using Multipass Non-linear Network Topologies”, 19UMK017, 29AUG2020.

Shepard, “A Low Noise Optical Amplifier”, 21UMK007, 14SEPT2020.

Bhamidipati, Myers, Caruso, “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources”, 21UMK009, 04NOV2020.

10.6 Provisional Patents Filed

Doynov, Caruso, “High-efficiency High-power Microwave Generation using Multipass Non-linear Network Topologies”, filed 26NOV2019.

10.7 Non-Provisional Patents Filed

None to date

ONR HPM Program - Monthly Status Report (MSR) – JUNE 2021

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 JULY 2021

Distribution Statement ~A: Distribution authorized to all OSPRES Grant and Contract performers, and any OSPRES uncompensated collaborators. Further dissemination per the Office of Naval Research, Ryan Hoffman (ryan.hoffman@navy.mil, 703-696-3873) or higher DoD Authority.

OSPRES Grant Goal: address and transition technologies and capabilities that enable the OSPRES Grant Objective using the OSPRES Grant Approach, while educating the next generation of pulsed power and defense minded, stewards and innovators.

OSPRES Grant Objective: to execute high-risk, high-payoff efforts that mitigate, fill or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable and electronically steerable high power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average power space, and includes the kill chain considerations including the target and its responsivity to radiofrequency stimuli.

OSPRES Metrics of Success: developed technologies and capabilities that are published in the peer review, protected as intellectual property, and/or, transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use, as enabling/integratable capability(ies).

OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

OSPRES Grant Security: All efforts should be fundamental and publically releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

1.0 Contents

2.0 Executive Summary 4
2.1 Progress, Significant Findings, and Impact 4
2.2 Completed, Ongoing, and Cancelled Sub-Efforts 6
2.3 Running Total of Academic and IP Program Output 7
3.0 Prime Power and Conditioning 8
3.1 HV Switch Pulsed Chargers 8
4.0 Switch Evaluation and Innovation 12
4.1 GaN:C PCSS Direct RF Modulation 12
4.2 Drift-Step Recovery Diode and Pulse Shaping Device Optimization 15
4.3 Pioneering Drift-Step Recovery Diode Processing and Manufacturing 27
4.4 Characterization of SOS Diode Performance through DOE Augmentation 27
4.5 SOS-Based Pulsed Power Source Systematic Topological Optimization 27
4.6 Optimizing SOS-IES Pulse Generator Performance with Machine Learning 37
4.7 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners 37
5.0 Pulse Forming Networks 43
5.1 Diode-Based NLTLs 43
6.0 Tradespace Analysis of Ultra-Wide-Band Antenna Arrays 48
6.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs) 48
6.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna 54
6.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna 61
6.4 Tradespace Analysis of Ultra-Wide-Band (UWB) Fractal Antenna 67
7.0 RF Coupling 74
7.1 Enclosure Effects on RF Coupling 74
8.0 Laser Development 78
8.1 Fiber Lasers and Optical Amplifiers 78
8.2 WBG-PCSS Enabled Laser Diode Array Driver 81
9.0 Thermal Management 85
9.1 Nanofluid Heat Transfer Fluid Development 85
10.0 UAS Engagement Wargaming & Modeling and Simulation (M&S) 87
10.1 Fixed-Effector Wargaming Simulation Toolkit Development 87
10.2 Airborne Effector Weapon Task Assignment 88
11.0 Program Management 91
11.1 Issues 91
11.2 Interactions with Others 91
11.3 Major Procurement Actions 91
11.4 Travel 91
11.5 Pending or Upcoming Public Release Requests 91
12.0 Appendix: Academic and IP Output 92
12.1 Students Graduated 92
12.2 Journal Publications 92
12.3 Conference Publications 93

12.4 Conference Presentations....97
12.5 IP Disclosures Filed....98
12.6 Provisional Patents Filed....99
12.7 Non-Provisional Patents Filed....99

2.0 Executive Summary

2.1 Progress, Significant Findings, and Impact

HV Switch. The redesigned gate driver board experienced arcing at a DC supply voltage level of 6.5 kV. A completely modular architecture has been adopted for a redesigned gate driver board featuring a new galvanic isolation link which will be tested in tandem with the HV switch.

GaN:C PCSS Direct RF Modulation. As proof of concept, demonstration of bipolar modulation was completed using two GaN:C PCSS devices with the free-space optical delay setup at 50 V charge voltage. On-state resistance was high due to limited laser energy available, but future testing will be performed with different laser options that allow for higher laser energies leading to lower on-state resistance.

SOS Pulsed Power Source. From device-level simulations to machine learning algorithm development towards optimization of the SOS-IES pulsed-power generator, the SOS team has transformed and grown to rapidly develop a non-laser-based Si-PCSS alternative which meets or exceeds the required key performance metrics necessary to be a viable alternative. Extensive TCAD simulations have resulted in pinpointing the optimal doping profile and thus the ability to produce higher peak voltage at shorter risetimes in comparison to the current SOTA; experimental apparatuses are being constructed to evaluate the next generation of epitaxial devices being manufactured by the collaborative effort of MIDE and SPT; the DSRD-based 2×2 SOS pulse generator prototype is able to produce over a megawatt of peak power with a near 1-ns risetime while maintaining a 6σ peak voltage pulse output variation at a PRF of 100-kHz; systematic topology optimization of the pulser layout and components leveraging machine learning is underway; and alternatives to DSRDs, or additions to the existing circuits topology, using thyristors, dynistors, and other technologies, are being investigated and evaluated which will further increase the peak voltage output, shorten the risetime, and shape the pulse.

Diode-Based Nonlinear Transmission Line. The K50F model D-NLTL was tested using the PCSS as a source and waveforms with a center frequency of 700–800 MHz, and Bragg cutoff frequencies of 1.25 GHz were produced. The SMV1702 tunable board was successfully used with bipolar excitations, demonstrating better diode saturation and higher frequency generation than with a monopolar excitation of a similar geometry and amplitude.

Antennas. A single coaxial probe-fed microstrip ESA element, on a G10/FR-4 substrate was modeled and characterized using FEKO, at the UHF range (0.756–1.121 GHz), for future manufacturing. Machine learning based stochastic search algorithms, used for bandwidth optimization in a single microstrip ESA element, have been found to be almost as accurate as the regular stochastic algorithms, while having ~39% faster convergence. For the Koshelev array antenna tradespace study, we introduced two independent

variables: pulse duration and a constant factor. The study yielded an optimum pulse duration and a constant factor to determine an optimum interelement spacing. Furthermore, we performed different active-passive configurations with the diamond Koshelev array antenna topology to identify a specific configuration that gives an opportunity to reduce array aperture area. With the Shark antenna, we have been able to identify an array topology that gives minimum side lobe compared to the traditional square topology. Finally, we learned that machine learning models in Altair hyperstudy fail to directly train on negative values.

RF Coupling. In the previous MSRs, we developed a CAD model of all of the wires in a particular UAV to act as a platform for numerical RF coupling experiments. During the semi-annual review, we received several recommendations to study the effect of changing the UAV wire shapes. Therefore, we deformed the wires' shapes in the CAD UAV model to create multiple arbitrarily shaped yet realistic wire distributions. Our analysis shows that the UAV frame constrains the UAV wires, leading to small variations in their shapes. These small variations caused the voltages coupled to the deformed wires to be very similar to those of the straight wires at the low-frequency range and significantly different at higher frequencies. This analysis shows the advantage of the numerical UAV platform in identifying which parameters do or do not significantly affect RF coupling.

Fiber Laser. We found that our tubular core geometry can exhibit and maintain fundamental mode propagation in either the glass wall or the hollow interior of the tube (in air). The existence of the mode in air is significant for the application of power delivery: very high power can be transferred in this very inexpensive embodiment. Moreover, we can couple the mode in glass to the mode in air in order to increase the operating power of optical amplifiers.

Laser Diode Array Driver. COTS silicon optodiodes are being evaluated as a potential alternative for GaN-PCSS. The initial results showed <500-ps rise-time and <10-ns pulse-width for 200-μJ optical excitation at 200V charge voltage. The test needs to be repeated at low optical energies (<20-μJ) to determine their viability. The first iteration of an 8-segment frozen wave generator (FWG) capable of chirped pulse-width has been designed, fabricated, and tested. While the initial test results show the expected chirped pulse widths, pulse deformation due to the reflections resulting from impedance mismatch needs to be addressed.

UAS Engagement Modeling and Simulation. During June, the fixed-effector wargaming simulation was created in the Unity environment as a transition away from the former software package Modern Air Power. This new simulation tool represents a shift to having full control over the simulation environment to truly realize the UMKC expertise for identifying and quantifying sUAS engagements.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

2.2.1 Ongoing Sub-Efforts

	Start	End
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
HV Switch Pulsed Chargers	DEC 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Enclosure Effects on RF Coupling	OCT2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
Nanofluid Heat Transfer Fluid	NOV 2020	Present
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization	JAN 2021	Present
UAS Engagement M&S	MAR 2021	Present
SOS-Based Pulser	APR 2021	Present
SOS Diode Manufacturing	MAY 2021	Present
SOS Diode Characterization	MAY 2021	Present
SOS Pulser Machine Learning Optimization	MAY 2021	Present
Sub-Nanosecond Megawatt Pulse Shaper Alternatives	MAY 2021	Present

2.2.2 Completed Sub-Efforts

Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020

2.2.3 Cancelled/Suspended Sub-Efforts

Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020
Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021
Bistable Operation of GaN	FEB 2021	MAR 2021

2.3 Running Total of Academic and IP Program Output

See Appendix for authors, titles and inventors (this list is continuously being updated)

Students Graduated	5 BS, 8 MS, 2 PhD
Conference Publications	35 (5 submitted/accepted)
Journal Publications	3 (4 submitted/under revision)
External Presentations/Briefings	18
IP Disclosures Filed	9
Provisional Patents Filed	1
Non-Provisional Patents Filed	0

3.0 Prime Power and Conditioning

3.1 HV Switch Pulsed Chargers

(Wasekul Azad and Faisal Khan)

3.1.1 Problem Statement, Approach, and Context

Primary Problem: Commercially available high-voltage solid-state switches made by BEHLKE are the best in SWaP-cooling, but are expensive, have long lead times (2–3 months), and are made outside of the US. For the Navy afloat mission to be successful, we need a sustainable supply of US-manufactured switches at a much lower cost.

Solution Space: Design and demonstrate modular high-voltage (~10 kV) and fast (repetition frequency = 100 kHz) solid-state switches using a combination of series- and parallel-connected commercially available inexpensive discrete MOSFETs and custom high-voltage (~10 kV) isolated gate drivers.

Sub-Problem: Voltage balancing among the series-connected MOSFETs, minimization of gate signal delays, cooling of the individual MOSFETs, balancing resistors, high-voltage isolation required for the power supplies, and the controlling pulse width modulated (PWM) signal as well as differential voltage feedback measurement across individual MOSFETs.

State-of-the-Art (SOTA): Direct liquid-cooled solid-state switch from BEHLKE (e.g., HTS-151-30).

Deficiency in the SOTA:

1. BEHLKE-made switches are expensive. For instance, a single HTS-151-30 switch costs around $5,000.
2. BEHLKE switches along with direct liquid cooling units occupy a considerable amount of space. For instance, an HTS-151-30 switch from BEHLKE has a footprint of approximately 225*85*75 mm without considering the liquid cooling system. Some key parameters of this switch are as follows.

   i) Maximum operating voltage = 15 kV

   ii) Maximum continuous load current = 2.52 A (without cooling), 30 A (with liquid cooling)

   iii) Maximum turn-ON peak current = 300 A (pulse width = 200 µs, duty cycle <1%)

   iv) Turn-ON resistance = 1.3 Ω
3. Once the switching frequency is greater than 10 kHz, a liquid cooling system is required to operate the BEHLKE switch.
4. Without liquid cooling, the maximum continuous power dissipation (P_{cont}) of the BEHLKE switch is limited (e.g., for HTS-151-30, P_{cont} is 10 W without liquid cooling).
5. At a higher switching frequency (>20 kHz), the BEHLKE switch requires multiple ancillary DC power supplies, i.e., 5, 15, and 60 V.

6. The switches made by BEHLKE cannot be reconfigured to withstand a higher voltage exceeding their recommended rating. BEHLKE offers separate products to operate them at higher voltage/currents.

Solution Proposed: Designing a modular high-voltage (~10 kV) switch using a single custom isolated gate driver for each module and having a construction cost lower than the BEHLKE switch with equivalent or better performance in all specification categories (Specifications for the BEHLKE switches can be found in the following link: http://www.behlke.com/separations/separation_c4.htm).

Relevance to OSPRES Grant Objective: The proposed modular high-voltage switch is expected to facilitate controlled hundreds-of-nanosecond charging of an array of transmission lines of pulse forming networks to drive an array of PCSSs, thereby producing controlled hundreds-of-picosecond scale high-voltage pulses.

Risks, Payoffs, and Challenges:

I. Lack of rigid control over voltage balancing can lead to a cascaded failure among the series-connected MOSFETs.

II. In the absence of an adequate mitigation scheme, voltage overshoot due to the fast switching speed can exceed the voltage rating of an individual MOSFET, thereby damaging the switch.

III. At high voltage (~10 kV) and high repetition rate (>100 kHz), mitigating EMI to safeguard the individual MOSFETs from false turn-ON is a major challenge.

3.1.2 Tasks and Milestones / Timeline / Status

(A) Design a surface-mount MOSFET-based four-stage switch (6.8 kV rated) and control it using the in-house gate driver, then test its voltage-withstanding ability with a DC supply voltage up to 4–5 kV and evaluate the effectiveness of the thermal management at its current state / DEC 2020 / Completed.

(B) Design and develop a modular HV switch (~10 kV rated) using the concept of the tested four-stage high-voltage switch module and an in-house modular gate driver to drive the modular switch /JAN–FEB 2021 / Completed.

(C)

(i) Test the voltage withstanding ability of the modular HV switch with a DC supply voltage up to 10 kV and switching frequency up to 50 kHz using a resistive load (5–10 kΩ) and evaluate the effectiveness of the thermal management at its current state / FEB–JULY 2021 / Ongoing.

(ii) Test the isolation capability and evaluate the synchronization accuracy of the gate drive signal generated from the modular in-house gate driver / FEB–JULY 2021 / Ongoing.

(iii) Encapsulate the gate driver board with potting material with a high (~15–20 kV) breakdown voltage rating to prevent possible flashover/arcing in between the HV switch and this board / MAR–JULY 2021 / Ongoing.

(D) Design and fabricate a compact power conditioner circuit based on a 12 kV rated SiC switch made by BEHLKE (HTS 121-15) / APR–MAY 2021 / Completed.

(E) Test this modular HV switch coupled with a Si PCSS device up to a DC supply voltage of 5–6 kV and a switching frequency of 50 kHz / On hold due to graduation in the Summer 21 semester.

(F)

(i) Design and develop a 20 kV rated modular (two modules, each with four MOSFETs) HV switch based on the design concept of the 10 kV rated modular switch using 3.3 kV rated SiC MOSFETs (new product made by GeneSiC Semi) / On hold due to graduation in the Summer 21 semester.

(ii) Design and develop a 20 kV rated modular gate driver based on a WPT based planar transformer topology to ensure adequate galvanic isolation (~30–40 kV) for the power supplies of the gate driver / On hold due to graduation in the Summer 21 semester.

3.1.3 Progress Made Since Last Report

(B)

(i) A conference paper written on the in-house modular HV switch has been accepted to the IEEE Kansas Power and Energy Conference 2021 and published.

(ii) A journal manuscript has been prepared on the modular HV switch and the custom gate driver circuit and submitted in IEEE Transactions on Power Electronics.

(C)

(ii) A new gate driver has been designed and fabricated with slot cutouts under the gate driver IC to increase the creepage to further increase the isolation. In addition, the high-voltage traces are further spaced out to prevent any potential arcing between high-voltage traces. The gate driver IC has been coated with conformal coating material with high dielectric breakdown. The gate driver has been tested at a supply voltage up to 6.5 kV. At 6.5 kV we have observed arcing at the primary side of the gate driver IC. Based on the observation, we have designed a gate driver which is entirely modular in nature. Each switch module will be driven by an identical gate driver board. A new optical fiber link (AFBR-395075RZ) capable of providing isolation up to 40-kV peak transient voltage and 13-kV peak working voltage has been incorporated in the revised design.

3.1.4 Significant Finding(s) and Mission Impact

3.1.4.1 Summary to Date

(A) The 6.8 kV rated four-stage surface-mount MOSFET developed in-house was successfully tested up to a DC supply voltage of 4 kV and at a switching frequency up to 20 kHz with a 3.2 kΩ resistive load.

(B) A modular (two modules) 10 kV rated HV switch has been designed and a prototype has been developed using 1.7 kV rated SMD MOSFETs (C2M1000170J). An in-house 10 kV rated HV gate driver has been designed and incorporated with the HV switch to

drive it. A manuscript on the HV switch and the custom isolated gate driver has been submitted in IEEE Transaction on Power Electronics.

(C) The HV switch coupled with the custom HV gate driver has been tested at a supply voltage up to 6.5 kV at a switching frequency up to 15 kHz. We have observed gate driver malfunctioning at around 6.5 kV and have designed a revised modular gate driver with an alternative optical fiber link.

3.1.4.2 Since Last Report

(C) The redesigned gate driver has been coupled with the modular HV switch and tested up to a DC supply voltage of 6.5 kV. We have observed arcing at the primary side of the gate driver board and the video footage helped us to locate the source of the arcing. A buffer IC (SN75451) required to drive the optical fiber link was damaged during arcing. The buffer IC is common to both the gate driver modules housed in a single board. To mitigate the problem, we have adopted an alternate galvanic isolation link (AFBR-395075RZ series) for control signal transmission. Separate gate driver boards with identical configuration will be connected to each switch module of the HV switch in the latest approach. The 3D model of the redesigned gate driver module is shown in Figure 3.1.1.

A manuscript on the multilevel modular HV switch architecture has been submitted to the IEEE Transactions on Power Electronics.

The journal article on the nonlinear transmission line work that was accepted in IEEE Transactions on Plasma Science has been published.

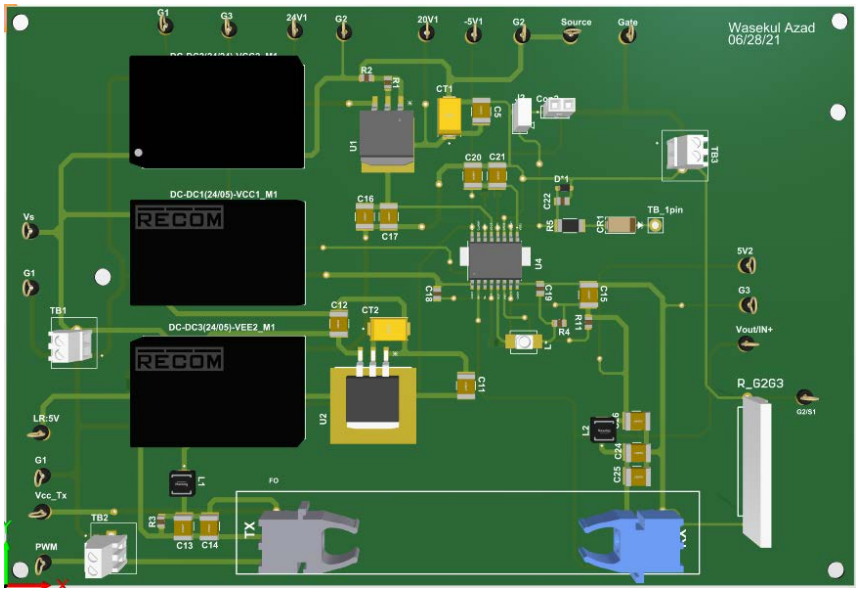


Figure 3.1.1: 3D view of the redesigned modular gate driver board with alternative optical fiber link.

4.0 Switch Evaluation and Innovation

4.1 GaN:C PCSS Direct RF Modulation

(Heather Thompson and Scott Shepard)

4.1.1 Problem Statement, Approach, and Context

Primary Problem: Need for a more compact, cost-effective RF pulse generation system for Navy afloat missions on smaller vessels and vehicles.

Solution Space: Improve efficiency and reduce necessary material, size, and thermal requirements by utilizing gallium nitride (GaN) in PCSSs through exploitation of its theoretical material properties which allow for higher operating voltages, frequencies, and temperatures, while also eliminating the need for pulse-shaping transmission lines through direct RF modulation using the laser/photon source driving the PCSS.

Sub-Problem: Lack of maturity in compensated gallium nitride semiconductor (i.e., GaN:X with X=C,Fe) PCSS manufacturing, development, and optimization.

State-of-the-Art (SOTA): Si-based PCSS with >10 kV operational voltage, cooling system capacity of 500 W/cm^2, and theoretical breakdown of 1.3 MW/cm.

Deficiency in the SOTA: Si-based technologies requiring ~100 µJ optical pulses per 4 MW of RF output power, increasing the laser energy (per pulse) required for device triggering; long recovery time (ones-of-µs), limiting quick opening and high pulse-repetition-rate operation along with increased heating in the PCSS; critical electric field of 0.3 MV/cm, leading to devices that are ones-of-cm^2 in area for the target peak power; and operating temperature of <160°C, leading to increased cooling requirements.

Solution Proposed: Replace Si-PCSS device with GaN:C utilizing direct RF modulation — eliminating the need for a bulky pulse-forming transmission line (~3 ft long) — capable of handling >3 MW (peak power) with ~20 µJ of incident optical energy, device area <1 cm^2, and operating temperature ~500°C (theoretical temperature which will be limited by circuit components and solder).

Relevance to OSPRES Grant Objective: Reduction in size and cost for cooling system that prevents damage to the PCSS device and components along with eliminating need for a bulky pulse-shaping system, as well as decrease in material cost and needed incident laser energy, leading to enhanced SWaP-C^2 capability with greater modularity and scalability.

Risks, Payoffs, and Challenges: Due to manufacturing limitations, GaN PCSS devices tend to be limited to lateral geometries (both contacts on the top side of the device), limiting operating voltage due to current crowding and surface flashover. The recovery time (ones-to-tens-of-ns) may lead to device heating and increased DC, or zero-frequency, component when generating RF with a period on the same order as the recovery time.

4.1.2 Tasks and Milestones / Timeline / Status

(A) **Start Jan 2021** Demonstrate RF unipolar modulation in the 1–2 GHz regime and up to 2 kV operating voltage with current PCB setup and automated optical delay system. Achieving 2 kV operating voltage should allow for preliminary effects testing before (or in conjunction with) striving towards higher operating voltages. **Ongoing**

(B) **Start June 2021** Demonstrate RF bipolar modulation using an advanced test setup with two GaN:C PCSSs triggered using the same optical delay, but with the second device connected to a negative power supply. **Ongoing**

(C) **Start June 2021** Achieve higher center frequency content in unipolar and bipolar modulation by using a faster (rise-time and pulse-width) laser to activate GaN:C PCSS. **Ongoing**

(D) **Start May 2021** Complete study of recovery for differing gap lengths, incident energies, and operating voltages and find solutions to reduce the recovery time.

(E) **March-August 2021** Complete study on the feasibility of using mode-coupling to bring the laser light into GaN:C devices, allowing for a possible reduction of laser energy, and pulse shaping within the laser-coupler/GaN:C composite structure.

4.1.3 Progress Made Since Last Report

(B) Direct bipolar modulation was demonstrated at 50 V (charge voltage).

4.1.4 Significant Finding(s) and Mission Impact

4.1.4.1 Summary to Date

(A) Towards showing direct RF modulation in the 1–2 GHz range, unipolar modulation has been demonstrated using an open-space time-optical delay using one GaN:C PCSS (lateral device with 500 μm gap length) of up to 1.2 kV charge voltage. The limiting factor to achieving higher charge voltage was flashover occurring in air-bubbles formed during curing of the Sylgard encapsulant. Previously, ~1.8 kV charge voltage was achieved using a 1 μm gap length GaN:C PCSS, so demonstration will continue using similar methods (corona-dope) to the Si-PCSS studies to achieve 2 kV+ charge voltage, with this being limited by the power supply being used to 2.5 kV.

(B) Demonstration of direct RF generation began with low-voltage (50 V charge voltage) testing to determine the feasibility of the bipolar setup and modulation. A bipolar pulse was achieved, but with high on-state resistance due to limitations in the available laser energy when using the neoLASE system. After conversion from 1064 nm to 355 nm, 6 μJ of energy was available to split into two beams for free-space optical delay. Future testing will commence using the laser sent to UMKC from BAE once that is setup.

(E) To continue towards a feasibility test of fiber coupling with GaN:C PCSS, single-mode waveguide modeling was initiated in COMSOL. This initial model will be modified to show optical fiber coupling to GaN:C PCSS.

4.1.4.2 Since Last Report

(B) To demonstrate the ability to use the incident laser on GaN:C PCSS for direct bipolar modulation (Figure 4.1.1), testing was done at 50 V (charge voltage). An ideal on-state resistance (<1 Ω) was not achieved due to the limited available laser energy, but as expected the rise time was ~70 ps (characteristic of the neoLASE). After conversion, there was 6 µJ of 355 nm wavelength to split using a 50:50 beam splitter for the free-space optical delay setup. Normally, to get to a minimum on-state resistance, tens-of-µJ of energy are needed (depending on the gap length of the device). Future testing will be done using the higher peak power laser built by BAE and/or the wedge laser. These options will offer the ability to reach minimal on-state resistance, maximizing power output and allowing us to measure the range of RF that can be generated using this setup with GaN:C PCSS.

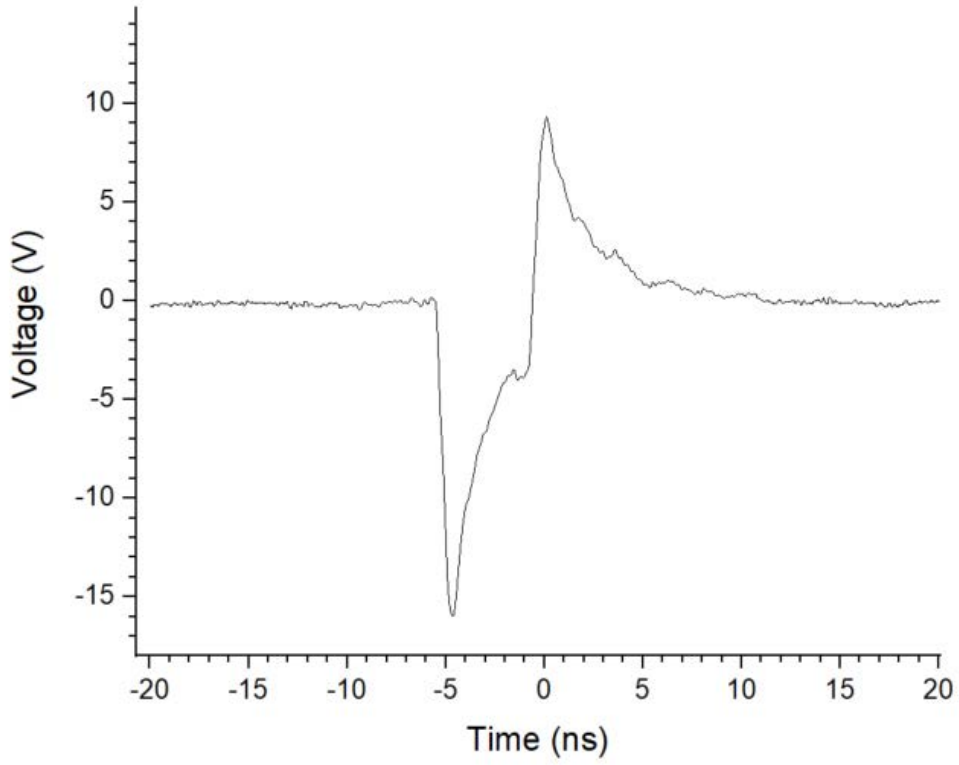


Figure 4.1.1: Bipolar output from GaN:C PCSS using a free-space optical delay setup.

4.2 Drift-Step Recovery Diode and Pulse Shaping Device Optimization

(Jay Eifler)

4.2.1 Problem Statement, Approach, and Context

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS but do not require a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times requires optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening device within the pulse shaping head circuit. Additional goals for pulse repetition frequency are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies. Also optimize the pulse sharpening device (PSD) within the pulse shaping head circuit.

Sub-Problem 1: TCAD and SPICE models of the DSRD are 40% accurate and must be improved. PSD models have not been developed.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetimes have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current. PSD have sharpened DSRD pulses to 100 ps-order.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power and minimum risetime, but also for low-jitter, reduced cooling, and compactness. Additionally, optimize pulser with PSD and pulse shaping head circuit.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2 cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities. DSRD and

PSD must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD and PSD modeling.

4.2.2 Tasks and Milestones / Timeline / Status

(A) Develop accurate models for DSRD (TCAD and SPICE models are 40% accurate)

(A1) Develop accurate DSRD TCAD models / JAN–APR 2021 / Completed.

(A2) Develop accurate SPICE models / MAR–JUN 2021 / Discontinued.

(A3) Develop parasitic capacitance, inductance, and resistance models for single die and stacked DSRD and the DSRD-based pulser circuits. / MAR–JUN 2021 / Discontinued.

(B) Explore TCAD modeling to advance DSRD research using available DSRD models

(B1) Study carrier lifetime effect on risetime / FEB–APR 2021 / Completed.

(B2) Avalanche and device operation study / FEB-MAY 2021 / Avalanche models limit peak power and risetime but do not correspond to experiment and must not be included or included and improved and calibrated to experiment.

(B3) Study effect of the width of outer edge contact on current density and breakdown in device. / MAR–MAY 2021 / Discontinued.

(B4) Begin TCAD process modeling in Silvaco Athena and Victory Process of diffused and epitaxial processes for DSRD (and pulse sharpening device) fabrication and DSRD device modeling. / MAR–JUNE 2021 / Completed.

(B5) Determine optimal doping profile for Semiconductor Power Technologies (SPT) DSRD epitaxial designs. / MAY–JULY 2021 / Exponential doping profiles produced the best device performance with a minimum doping of 5×10^{13}, no basewidth and a junction depth of 95 μm on a 170 μm thick device in two different DSRD circuit topologies (see circuits A and B).

(C) Pulse sharpening device (PSD) modeling

(C1) Begin TCAD modeling of PSD / DEC 2020 and APR–JUN 2020 / (a) Preliminary PSD research begun replicating published work but further work to continue. (b) More standard PSD device modeled in TCAD than as used in published work. (c) PSD simulated with DSRD 3-stack for more complete DSRD-based system modeling excluding only the primary switch model. Discontinued.

(C2) Determine current carrying capacity of PSD and stacks / MAR–JUN 2021 / PSD literature review begun. Discontinued,

(D) Receive and study DSRD-based pulser circuit topologies in SPICE with the DSRD and primary switch SPICE models. / MAR–APR 2021/ LTSPICE code and models received and understood. Completed.

(E) Perform TCAD simulations in DSRD-based pulser circuit topologies, including the single-bar (circuit B) and 2x2 (circuit C) DSRD pulser circuit topology and compare to experiment / JUL-AUG 2021 / Single-bar and 2x2 DSRD pulsers were successfully simulated but variability or inaccuracy remains due to the MOSFET models used.

4.2.3 Progress Made Since Last Report

(B5) Larger DSRD doping parameter studies were completed in TCAD for the better performing exponential doping profiles. The results show that a minimum doping of 5×10^{13} dopant atoms/cm^3 , no basewidth and 95 μm junction depth is an optimal doping profile for DSRD performance based on peak load voltage, risetime, voltage riserate, maximum reverse current, FWHM pulsewidth and prepulse. The better peak voltage and risetime devices invariability had better voltage riserate and prepulse. The pulsewidth for better performing profiles tended toward the middle of possible values, since prepulse vs pulsewidth shows increasing pulsewidth does not further decrease prepulse past the average pulsewidth results. High peak voltages also corresponded to higher maximum reverse currents as expected. Further doping parameter studies can pinpoint the best minimum doping, peak doping pair, junction placement and basewidths over a range of voltage input magnitudes for any of circuits A, B or C and determine (over the voltage input magnitudes used) if a single overall best performance doping profile exists. The doping parameter suggest that higher peak voltages are possible but at reduced risetimes and for doping profiles with larger basewidths and higher minimum dopings than the optimal doping profile determined by the doping parameter study (see black outline in Figure 4.2.2).

(E) The DSRD 2x2 pulser circuit topology (see Figure 4.2.1, circuit C) has been simulated within TCAD using a TCAD MOSFET model. The results show the ability to match the experiment by adjusting the MOSFET model width for increasing the drain current with all other circuit parameters set to experimental values (no parasitics). Both MOSFET and DSRD models introduce inaccuracy in matching experiment to TCAD. As the MOSFET model is refined (whether a TCAD or SPICE model), the accuracy of the TCAD simulation will be better estimated. Already, the 2x2 DSRD pulser TCAD results are a large improvement over the available DSRD SPICE model (level 1 diode model with a few measured diode parameters), see Figure 4.2.6. In addition, the peak voltages in TCAD simulation reduce after the first pulse likely due to the initial, well-equilibrated steady-state circuit condition and pulse repetition studies must be done to match experiment.

4.2.4 Significant Finding(s) and Mission Impact

4.2.4.1 Summary to Date

DSRD TCAD simulation started by replicating published TCAD DSRD results and then simulating devices similar with actual in-house DSRD. The variation of the sinewave pulse voltage input magnitude and period on DSRD charge storage were collected. Charge storage timing (when the diode empties charge stored from forward pulsing) of ~50% was achievable with sufficiently long voltage input period which is necessary for maximum reverse current cutoff.

DSRD stacks, as opposed to individual die DSRD, were simulated showing reduced risetime from single die to 5-stacked DSRDs consistent with published and earlier in-house data. Series resistance to model metal resistance between DSRD in stacks and doping variability in stacks was also modeled in TCAD showing metal resistance must be large to have an impact on peak voltage and risetime and that doping variations proportionally effect risetime.

(A1) Accurate DSRD TCAD models have been developed that include both carrier-carrier scattering and Selberherr breakdown and are suitable for DSRD operation below the dynamic breakdown threshold. Peak voltage and risetime were limited by the breakdown model and more closely match experimental pulse data.

(A2) Work on DSRD SPICE models has been done for the primary switch model (MOSFET) with conversion of the code to TCAD SPICE being partly completed to allow for modeling the complete DSRD-based pulser system (except driver).

(B1) DSRD risetime performance was collected from TCAD simulations for variable carrier lifetime. Changes in lifetime had no significant effect on risetime other than the output pulse starting earlier.

(B2) DSRD peak voltage and risetime were simulated in TCAD to include avalanche modeling or not. TCAD avalanche models limited peak voltage and risetime at the load over a range of voltage input magnitudes. A TCAD parameter study for DSRD stack height and DSRD area for several doping profiles with and without avalanche modeling was performed (Spring 2021 UMKC OSPRES Grant Review and Technical Exchange). The avalanche model and model parameters were also modified to account for dynamic breakdown rather than static and then compared to the no avalanche case and experimental data. From the improved avalanche modeling and TCAD parameter study, the optimal area of the DSRD can be obtained. However, for the 500 V voltage input magnitude used, the DSRD output were all in breakdown and are not predictive of non-breakdown behavior. Future studies for optimal area will include a range of voltage magnitudes to study DSRD performance and breakdown.

(B4) TCAD process and device modeling for the development of process steps and their resultant doping profiles and device operation was begun. This modeling will enable a connection between the fabrication parameters and the device operation for DSRD (and PSD).

(B5) Exponential doping profiles were shown (via TCAD) to outperform Gaussian and error function profiles slightly. Exponential profiles have an optimal minimum doping of 5×10^{13}-$1\text{x}10^{14}$ dopant atoms/cm^3, while Gaussian and error function profiles have an optimal minimum doping of 1×10^{13}-5×10^{13} dopant atoms/cm^3. Further exponential doping parameter studies were carried out in circuits A and B of Figure 4.2.1 which included a broader doping parameter space for minimum doping, junction placement, basewidth and peak doping over a wider range of voltage input magnitudes (for breakdown limitations). The results are similar to before and show the optimally performing doping profile has a minimum doping of 5×10^{13}, no basewidth, junction placement of 95 µm, as well as, peak doping of 1×10^{18} (p-side) and 1×10^{19} (n-side) dopant atoms/cm^3.

(C1) Pulse sharpening has been verified for PSD devices for the standard design and another non-conventional design. The PSD was also modeled within a DSRD-based pulser circuit combining for the first time TCAD modeling of both DSRD and PSD together within the same circuit with only the primary switch model not included.

(E) DSRD pulser circuits for the single-bar (Circuit B of Figure 4.2.1) and 2x2 (circuit C of Figure 4.2.1) have been simulated within TCAD allowing the use of a TCAD DSRD model, whereas in SPICE no accurate DSRD SPICE model is available. Currently, the primary switch MOSFET is modeled in TCAD, as well, but SPICE models can also be developed for the SPICE within TCAD as and will allow for better use of computational resources within TCAD. The MOSFET model and pulse repetition are being studied in detail to more closely match experiment and TCAD.

4.2.4.2 Since Last Report

(B5) To prepare for an epitaxial DSRD fabrication on 25 wafers, a doping parameter and DSRD performance TCAD study was performed to identify what doping profiles had better overall performance. Earlier, exponential doping profiles were discovered to be the overall best doping profile. Exponential doping profiles are not possible with diffusion and epitaxial designs may be more suitable. To build on this, exponential doping profiles for a 170 μm device were generated over a range of doping parameters and over a wide range of each doping parameter (smaller thicknesses are in planning and allow for a wider range of thicknesses to be studied). The wide doping parameter ranges necessitated a coarse sampling of the parameter space, so a few data points were selected for each doping parameter. The following two doping parameter studies are performed in circuit A of Figure 4.2.1. An additional doping parameter study was performed in circuit B. And circuit C has been simulated and MOSFET and DSRD parameters are being refined to match closely to experiment.

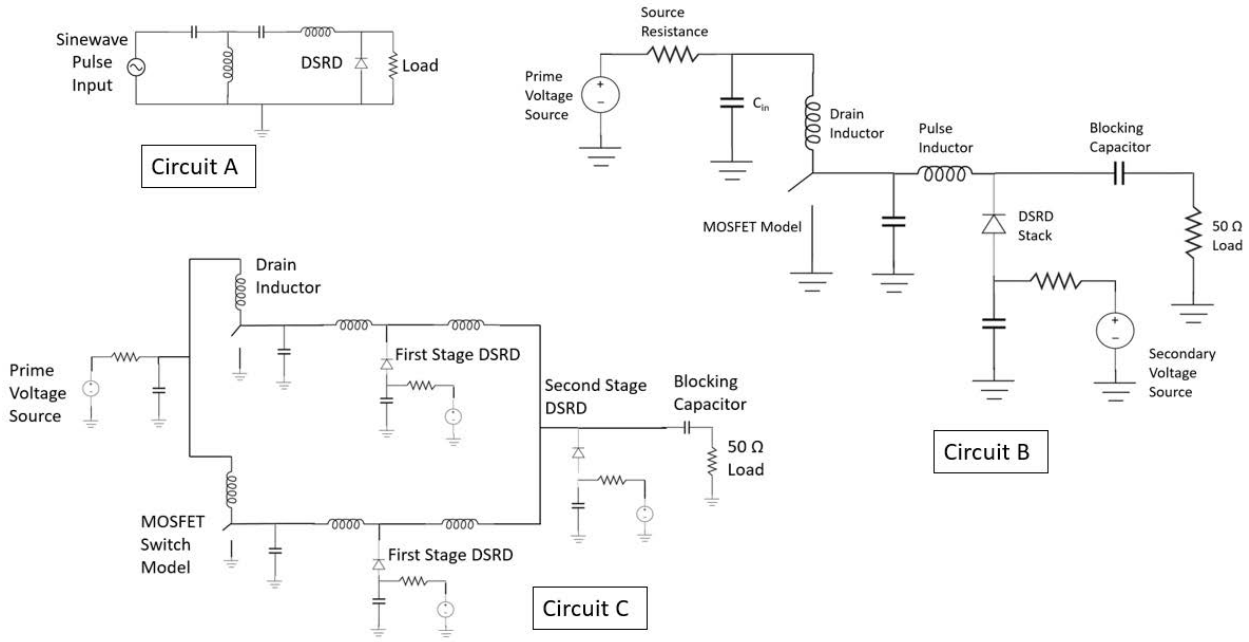


Figure 4.2.1. Three circuits used for TCAD simulations.

Circuit A Simulations

The first doping parameter study was a high resolution sampling of junction placement or depth to since it is thought that the placement is sensitive. Also, in the literature [1] it is known that a slightly deeper from the center p-side doping is optimal for diffused doping profiles. The higher resolution study in junction placement included three doping profile variants (in minimum doping and basewidth) and showed that junction placement was not as important as previous thought, at least for exponential profiles within the pulser circuit A, meaning performance metrics did not decrease until the junction placement was near the edges of either side of the device (for 5-15 μm wide p or n depths). This shows the possibility of larger displacements of the junction from the middle having good performance and positioning in the middle of the device is not very sensitive. Since it is not possible to study a large parameter space in high resolution only lower resolution parameter studies were later performed.

The first lower resolution doping study (for circuit A) was over a range of junction placements, minimum doping levels, and basewidths. The voltage input magnitude (for the sinewave pulse input) included 100, 200, 300 and 400 V for a 200 ns sinewave pulse period. The junction placements were selected to range over the width of the device and varied from 5 μm to 165 μm with 5 or 6 samples with actual values varying depending on basewidth used. The basewidths or regions of constant p base doping were 0, 5, 25 and 45 μm. The minimum dopings (basewidth doping or lowest doping of the p-n junction for no basewidth) were 1×10^{12},1×10^{13}, 5×10^{13}, 1×10^{14} and 5×10^{14} dopant atoms/cm^3. A total of 415 simulations were performed in this parameter space study. The simulations were

analyzed for the performance metrics: peak load voltage, risetime, voltage riserate, maximum reverse current, FWHM pulsewidth and prepulse (determined by knee point). In Figure 4.2.2 is a summary of the simulations as a scatter plot. First, only junction placements near the middle (70-100 μm junction depths) are shown and only output pulses showing no signs of breakdown for 42 out of 415 simulations. The plot is peak load voltage against risetime since there is generally a tradeoff. A tradeoff area has been suggested by circling a region for the maximum possible peak voltage at a risetime.

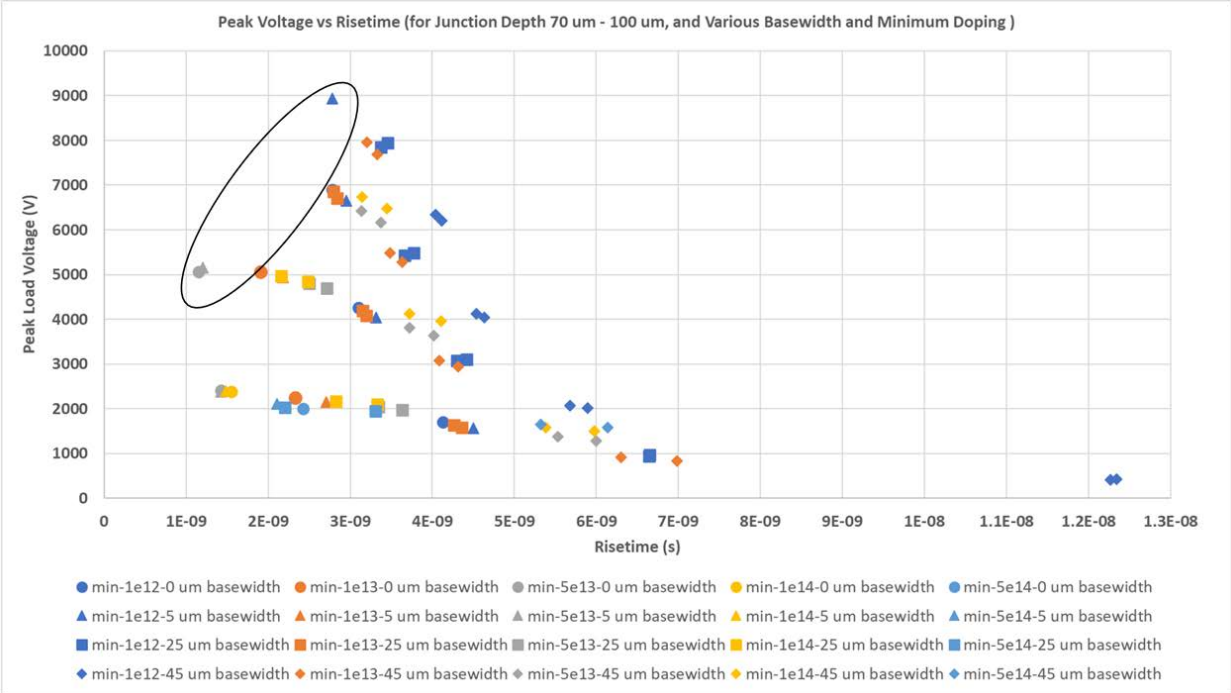


Figure 4.2.2. Peak load voltage vs risetime for colored minimum doping and symbolled basewidths of exponential doping profiles. Not shown are variable junction placement (closer duplicate colored symbols are different, approximately center junction placements) and voltage magnitude input used (same colored symbol at higher peak voltage and lower risetimes correspond to different voltage input used). The black outline suggests the doping parameter space region of maximum peak voltage at a risetime and the well-known peak voltage-risetime performance tradeoff.

Sampling of the doping parameter space for the circled region will serve for determining what doping profile variations have maximum peak power at a risetime and over a range of good DSRD risetimes likely between 1-2 ns. What doping profile has the best performance over a range of voltage input magnitudes can also be determined. The higher voltages used result in higher peak voltages and lower risetimes for a particular doping profile (color and symbol) and can be seen as a lining up of data points in the figure. The best doping profile used a voltage input magnitude of 200 V and had a minimum doping of 5×10^{13} dopant atoms/cm^3, junction placement was 95 μm, either a 0 μm or 5 μm basewidth served about as well, and can be seen as a grey triangle and grey circle within the black outline. There are also 7000, 8000 and 9000 V cases but none are

close to 2 ns in risetime. Cases may exist where different values of the minimum doping, basewidth and voltage input magnitude have lower risetime and the higher 7000-9000 V peak load voltage within the tradeoff suggested by the black outline (probably a 7000 V, 2 ns limit). Rather than continue searching this doping profile-performance parameter space, new TCAD simulations were conducted for a more restricted set of doping profiles suggested by the epitaxial manufacturer. Also, the simulations used circuit B which serves as a modular unit for circuit C used for obtaining higher peak powers and for which experimental measurements are being carried out (see Section 4.3).

Circuit B Simulations

The epitaxial manufacturer suggested that the depth of doping could not be more than 85 μm on either side and that the doping should not change more than 5-6 orders of magnitude. For thicker devices, such as 170 μm, his limited the possible basewidths and junction placements (the n side must be doped to 85 μm and the p-side to either 65, 75 or 85 μm with corresponding basewidths of 20, 10 and 0 μm since the base is p-doped). For these three junction placement-basewidth pairs, three minimum doping were chosen 1×10^{13}, 5×10^{13}, and 1×10^{14} dopant atoms/cm^3. Also, peak doping pairs for the p and n side were chosen as: $1\times10^{19}/1\times10^{19}$, $1\times10^{19}/1\times10^{18}$, $1\times10^{18}/1\times10^{19}$. $1\times10^{18}/1\times10^{18}$ dopant atoms/cm^3. The voltage sources in circuit B were varied with the prime voltage as: 50, 100, 150 and 200 V and the secondary voltage sources half that. Varying the voltage sources allows for determination of breakdown and exploring higher peak voltages. In Figures 4.2.3-5 are shown a similar scatter plot as for circuit A study but for circuit B. The prime voltages used are given symbols this time and the colors correspond in the different figures to different doping parameters: minimum doping, junction-basewidth pair, and peak doping pair. The breakdown cases are not shown in the figures.

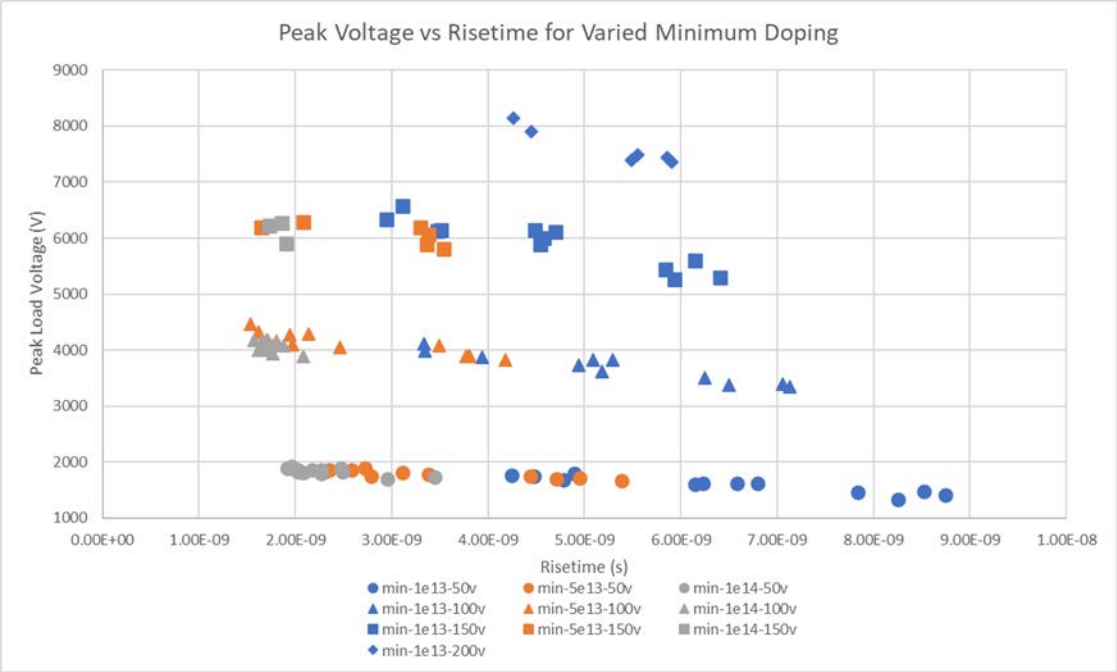


Figure 4.2.3. Scatter plot of peak voltage vs risetime for various minimum doping levels (colors) and prime voltage source voltages (symbols). The DSRD performance of interest have risetimes 2 ns are lower.

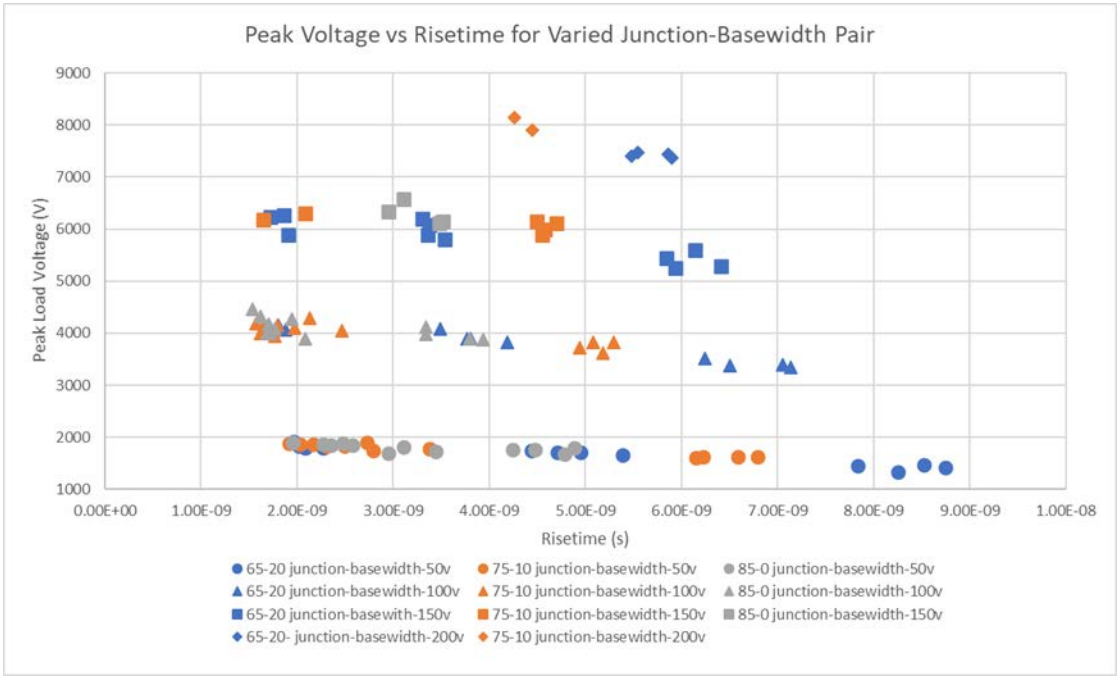


Figure 4.2.4. Scatter plot of peak voltage vs risetime for various junction placement-basewidth pairings (colors) and prime voltage source voltages (symbols). The DSRD performance of interest have risetimes 2 ns and lower.

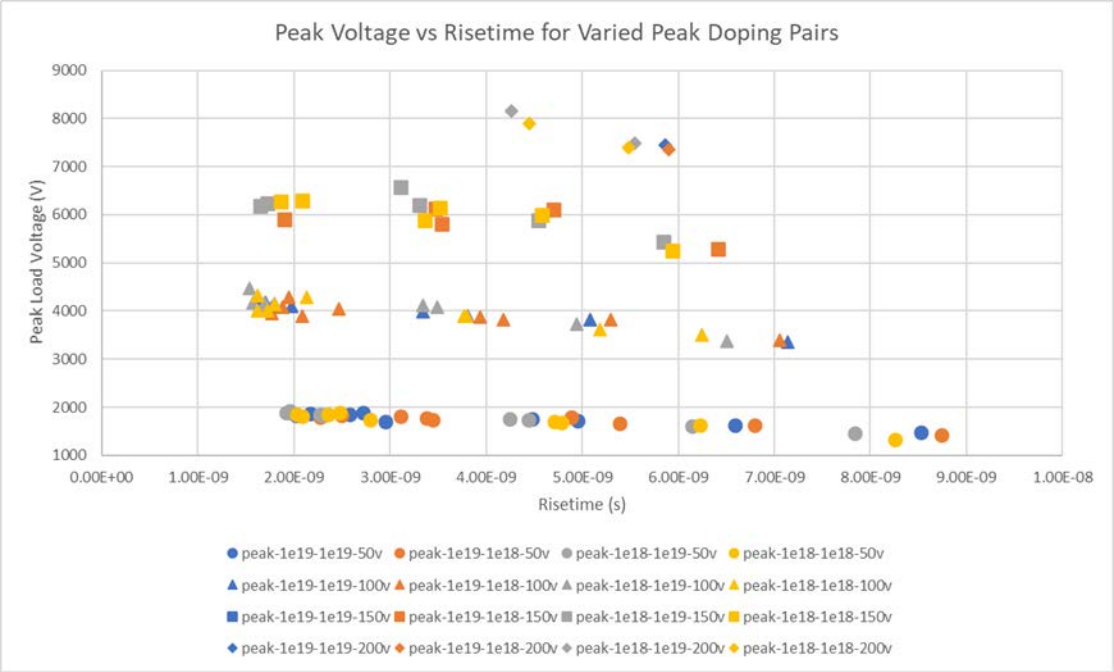


Figure 4.2.5. Scatter plot of peak voltage vs risetime for various peak doping pairs for the p-side and n-side (colors) and prime voltage source voltages (symbols). The DSRD performance of interest have risetimes 2 ns and lower.

The lines of different voltages are flatter in this figure (likely due to restricted doping profiles and voltage resolution used as well as a different circuit) and the black outline (not shown) likely occurs in the same peak voltage-risetime region. The best doping profiles are located at ~6000 V and ~ 1.5 ns using a 150 V prime voltage source. The minimum doping for risetime less than 2 ns can be seen to be either 5×10^{13} or 1×10^{14} with 5×10^{13} dopant atoms/cm^3 for the best cases. For the minimum dopings a blue, orange, grey ordering can be seen from right to left. For the junction-basewidth pair, less basewidth is better at ~4000 V but more basewidth at ~6000 V as expected. For junction-basewidth pairs, an ordering of blue, orange, grey can be seen in the smaller clusters from right to left but is obscured at the lower risetimes. For the peak doping pairs, $1\times10^{18}/1\times10^{19}$ and $1\times10^{18}/1\times10^{18}$ dopant atoms/cm^3 can be seen to be among the best cases. Also, in an individual small cluster there is a right to left ordering of orange, blue, yellow, grey.

The junction placement, basewidth and minimum doping results yield the same result that a 5×10^{13} minimum doping, 0 µm basewidth (near center junction only studied) are optimal. The peak doping results are new and show that $1\times10^{18}/1\text{x}10^{19}$ was best overall and $1\times10^{18}/1\times10^{18}$ was preferable over $1\times10^{19}/1\times10^{19}$ as used in the circuit A studies. 1×10^{18} dopant atoms/cm^3 doping is then preferable, as long as, it does not interfere with ohmicity at the contacts.

Additional plots of different performance metric pairs, such as: prepulse/peak voltage vs pulsewidth, can be made with the colored doping parameter and symbolled voltage levels. Also, the trigger duration for the voltage controlled resistor switch or time-dependent resistor used (simple MOSFET models) can be varied and can cause breakdown alone at sufficient prime/secondary voltages and can be included in the DSRD circuit topology input parameter space but has not been done here. Other linearly interpolated plots, showing performance as a function of doping parameters, have been made and similar conclusions can be reached but have not been shown due to their complexity and/or large number of plots. A larger collection of simulations using different thicknesses has been put on hold to compare experimental results to TCAD simulations for circuit C. Variations in stack height, device area and trigger duration along with variations in circuit components and parasitics can also be added to the parameter space but care must be taken in the size of the space and feasible computations.

Circuit C Simulations

(E) Since current experimental measurements are being performed on the 2x2 DSRD pulser (circuit C) and a good DSRD SPICE model is not available, TCAD simulations were developed to compare to experiment and SPICE with the idea of supplanting SPICE simulations for the design of the smaller 2x2 DSRD pulser and performing doping parameter-performance studies for the determination of the doping profile. Essentially, this provides a connection between DSRD design and fabrication parameters and DSRD pulser design and pulse performance.

A large number of simulations were performed to build confidence in the simulation method resulting in using a ramping of voltage biases over 1 ms and a subsequent 39 ms (depending on the capacitor C_{in}) charging of the energy storage elements (capacitors and inductors) and stabilization of the circuit behavior into steady-state. From here, the simple MOSFET model as a voltage-controlled resistor or time-dependent resistor was seen to be a poor MOSFET model and the circuit behavior was not limited to the primary MOSFET switch driving capabilities. Using a TCAD silicon power MOSFET model of a single MOSFET power cell (actually half cell) the width can be scaled to scale the current and set the load output (peak voltage) to within experiment. Along with DSRD variability, matching the MOSFET model to the vendor datasheet is necessary to determine the accuracy of the TCAD simulations when compared to experiment.

An experimental voltage measurement of circuit C at the load, an LTSPICE simulation, and a TCAD simulation of the load voltage output is shown in Figure 4.2.6. Table 4.2.1 gives a percent difference comparison of the experimental and simulation data in the figure. The LTSPICE simulation over-estimates the peak voltage and especially the risetime when compared to either experiment or TCAD. However, better DSRD SPICE are likely possible. The TCAD result matches the experiment as closely as possible except for the MOSFET model which has not been set to match the peak load voltage of the experiment.

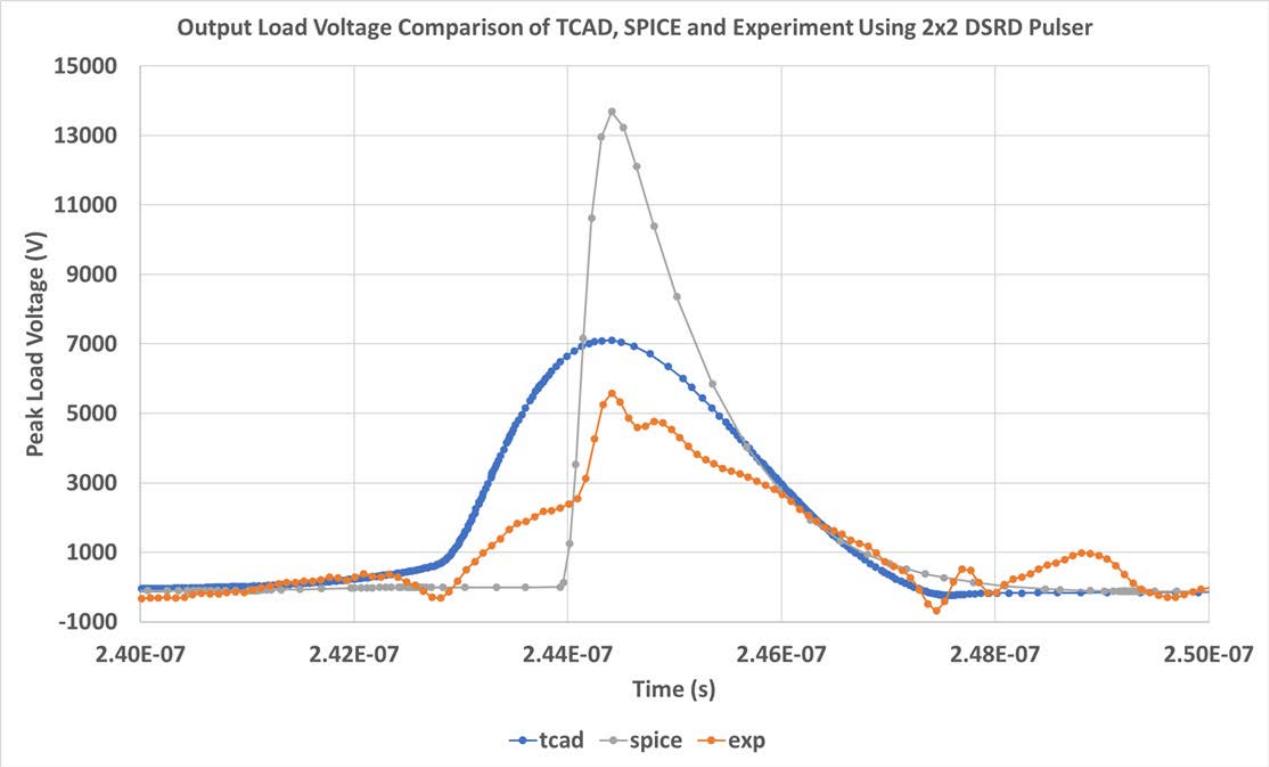


Figure 4.2.6. Aligned peaks of TCAD, SPICE and experiment for load output voltage of the 2x2 DSRD pulser (circuit C). The TCAD and experiment are much closer in pulse characteristics (peak voltage, risetime and pulsewidth). The TCAD result has not been intentionally fit to the experiment by adjusting the MOSFET model width.

Table 4.2.1. Percent differences between experiment and TCAD or LTSPICE

	Experiment	SPICE Simulation	TCAD Simulation	SPICE Percent difference	TCAD Percent Difference
Peak Load Voltage (V)	5271	13688	7098	160	35
Risetime (ns)	1.21	0.267	1.08	78	11
Voltage Riserate (kV/ns)	3.48	40.94	5.28	1078	52
FWHM Pulsewidth (ns)	1.93	1.09	2.49	44	29

The datasheets of the TCAD MOSFET model can be produced with TCAD to some extent and compared and the TCAD MOSFET model adjusted accordingly. This TCAD MOSFET model is the quickest and best MOSFET model available within TCAD and its integrated SPICE simulation. There is also the level 1 Schichman-Hodges MOSFET SPICE model available in TCAD and has yielded promising results but may not be as

easily matched to the datasheets. Other custom built MOSFET SPICE models may be possible within TCAD that can be accurate and require less computational resources than the TCAD MOSFET model. Whichever MOSFET model is used once it is accurate the TCAD results can be better calibrated to the experiment for predictive simulation.

4.2.5 References

[1] Lyublinsky, A. G., E. I. Belyakova, and I. V. Grekhov. "Numerical and Experimental Study of an Optimized p-SOS Diode." *Technical Physics* 64, no. 3 (2019): 373-379.

4.3 Pioneering Drift-Step Recovery Diode Processing and Manufacturing

This section is scheduled to be included in next month's MSR. Section 4.3 aims to brief on the DSRD manufacturing effort that MIDE is executing along with its collaborators at SPT. Leveraging the simulation work and results provided in **Section 4.2**, information on both loose compression stacks produced using deep-diffusion techniques as well as epitaxial growth methods to produce optimized DSRDs will be provided. The ability to manufacture DSRD/SOS devices is necessary to not only overcome Sub-problem 1 outlined in **Section 4.5** but doing so within the continental United States is imperative to the success of OSPRES Grant's objective to support of the Naval afloat mission.

4.4 Characterization of SOS Diode Performance through DOE Augmentation

This section is scheduled to be included in next month's MSR. Section 4.4 aims to provide information on the experimental evaluation of the DSRDs manufactured as briefed on in **Section 4.3**. Generating holistic and rapid assessment apparatuses to evaluate diode performance metrics is essential to experimentally verify the TCAD simulations results portrayed in **Section 4.2**, ensure they are met by the manufacturing methods described in **Section 4.3**, and enable selection of optimal diodes utilized in the pulsers developed as described in **Section 4.5**.

4.5 SOS-Based Pulsed Power Source Systematic Topological Optimization

(Sourov Roy)

4.5.1 Problem Statement, Approach, and Context

Primary Problem: Semiconductor opening switch (SOS)-based pulse generators using inductive energy storage (IES) and release topologies able to produce ones of gigawatts in ones of nanoseconds are traditionally large and bulky, and suffer from low volumetric power densities, rendering them impracticable for Navy afloat missions.

Solution Space: Through a combination of numerical and experimental efforts, systematically develop a modular architecture of an SOS-IES pulser circuit—by determining the optimal permutation of series and parallel combinations of stages within the base SOS-IES pulser (and components utilized)—which maximizes the peak voltage, peak power, and volumetric power density achieved without sacrificing the desired nanosecond risetime of the pulses generated.

***Sub-Problem 1*:** Viable SOS diodes, specifically p^+-p-n^+ silicon diode structure versions (i.e., drift-step recovery diodes, or 'DSRDs' consistent with those discussed in Section 4.2) are in limited production, minimal supply, and are traditionally manufactured OCONUS, therefore are difficult to procure. This leads to using non-ideal diodes within the pulse generator circuit, causing decreased performance.

Sub-Problem 2: A reciprocal relationship exists between the performance of the SOS-IES circuit (specifically, the auxiliary components utilized), and diode's performance characteristics. Hence physicomathematical modeling of this process requires simultaneously solving, (1) the Kirchhoff equations for the pulse generator circuit containing the diodes, (2) the continuity equation for the free carrier recombination within the diode itself, and (3) determining the electric field generated within the diode using the Poisson equation. Therefore, optimizing at the diode level (e.g., doping profile and concentration) affects the impulse signal output. Conversely, an optimized circuit topology may require alternative components (e.g., differently valued inductors and capacitors) different than those used when simulating/optimizing the diode's performance which, in turn, affects the performance of the diodes.

Sub-Problem 3: Another problem is finding the optimal parallel-series permutation of the SOS-IES storage and release topology and its key component parameters which produces the highest peak power output, lowest rise time, and highest efficiency given theoretical and real-world constraints. That is to say, the optimal diode performance and ancillary components used in a 1×1 topology cannot simply be scaled to a 2×2, a 4×2, etc. as the pulse combining and compression occurring within each stage requires different considerations. Compounding this issue, exploration of existing theoretical models which aid in simulation techniques to evaluate the performance tradeoffs is limited. Therefore, most of this work aims to determine the best-case configurations of SOS-IES topology by maturing a suitable predictive model for the SOS-IES modular architecture for a given performance matrix.

State-of-the-Art (SOTA): Large SOS-IES pulse generators ($\geq$1-m^3, $\geq$300-kg) which are comprised of sixteen parallel-branches, each containing four series-connected stacks (V_{max} = 130-kV, surface area ~20-mm^2), have demonstrated reverse pumping currents of 25-kA with an injection time of 400-ns to produce 400-kV pulse amplitudes with full-width half-maximum (FWHM) values of 60-ns produced across a 100-Ω load; a voltage gain factor of ~3 (i.e., power amplification level ~9.5-dB). Pulse repetition frequencies up to 4-MHz have also been produced across similar load values. Smaller versions (equivalent in size to the pulse generators developed for this effort, i.e., ~0.01-m^3, ~2-kg) are able to achieve 6-kV, 200-ps rise time, and < 500-ps FWHM across a 50-Ω load.

Deficiency in the SOTA: Large SOS pulse generators which can achieve the foregoing performance parameters are traditionally limited by mechanical design constraints (onboard itinerant vehicles) and power supply limitations, are large (case lengths <1-m), and require transformer oil for cooling purposes, which lead to undesirable system mass values up to 300-kg. The smaller air-cooled versions are limited to PRF < 15-kHz. Additionally, a comprehensive study on SOS generators aiming to achieve maximum gain and efficiency (reducing thermal load) through optimizing the number and ratio of parallel-branches and series-connected stages is missing in the SOTA.

Solution Proposed: Systematically determine topological SOS-IES circuit configurations and the necessary components therein that maximize voltage gain and efficiency achieved by the pulser. Generate an optimization algorithm (i.e., machine learning algorithm) to build a suitable predictive model for the SOS-IES topology.

Relevance to OSPRES Grant Objective: SOS-IES pulse generators can remove the need for photo-triggered switches and their laser sub-systems. They are ideal for triggering sub-nanosecond rise-time sharpeners (SAS, D-NLTL, etc.), reducing overall cost, volume, and weight.

Risks, Payoffs, and Challenges:

Risks: SOS diodes which possess sub-optimal doping profiles may limit the permissible injection time (pumping) of the switch. This leads to a decreased amount of time energy is accumulated and ultimately limits the reverse current amplitude during extraction time. Development of sub-optimal diodes may lead to sub-optimal circuits with sub-optimal performance. The data gathered from these circuits would then be used to train the genetic algorithms developed and the redesign future topologies constructed; ultimately leading to spurious conclusions regarding ideal topological circuit configurations with 'N' number of series-connected stages, each containing 'M' parallel branches.

Payoffs: Leveraging collaborative partnerships with U.S.-based manufacturers of SOS diodes, the ability to refine and control the performance characteristics of the SOS devices themselves, along with the ability to simulate and manufacture the SOS pulsers in-house, enables a holistic soup-to-nuts capability to optimize, produce, and evaluate these nanosecond pulse generators.

Challenges: Determining the superlative ratio of design/development (through numerical analysis) to the effort put towards experimental testing/evaluation of the SOS pulser is challenging due to the novelty of the approach. The complexity of the theoretical model is extreme given the M×N number of stages within the pulse forming network. SPICE circuit simulation software algorithms possess computational convergence difficulties caused by abrupt changes in capacitance, inductance, and impedance. SOS diodes are non-autochthonal to SPICE software's databases thus are only approximated by equivalent combinations of circuit elements. Additionally, the variable time step imbedded in SPICE algorithms exacerbates this convergence issue. This summates to the existing discrepancy when comparing existing experimental data to that of simulated values.

4.5.2 Tasks and Milestones / Timeline / Status

To address the primary problem and achieve the solution proposed, two major parallel-path efforts for this work are distinguished: (1) progressively and systematically iterate, through construction and experimental evaluation, permutations of the SOS pulse generator through increasing M×N stages towards increasing peak voltages, efficiencies, and gain without compromising risetime and pulse width; and (2) generate an optimization algorithm which produces a suitable predictive model for the SOS-IES topology permutations.

Milestones for the first effort, and tasks to achieve them along with a timeline to do so, are as follows:

(A) Milestone – Construct/demonstrate a 2×2 SOS pulse generator prototype capable of producing ≥4-kV peak voltage, ≤1-ns risetime, ≤5-ns FWHM, ≥320-kW peak-power, ≥1-kHz PRF, ≥100 shots-per-burst, ≥5 number of bursts [***Completed JUL21***].

1. Task – Perform literature review on SOS-IES generators and undergo training on in-house-developed DSRD-based generators developed to-date [*APR—MAY21*];
2. Task – Develop and simulate (using LTSPICE software) circuit topology to include electrically optimal (not mechanical) layout considerations and components within Altium [*Completed MAY21*];
3. Task – Order and populate PCB [*Completed JUN21*];
4. Task – Evaluate gate-driver performance and single-pulse performance output in terms of peak voltage amplitude, risetime, FWHM, and shot-to-shot variability [*Completed JUN21*];
5. Task – Perform PRF study, ranging from 100-Hz to 100-kHz, to evaluate the PRF handling capabilities of the pulse generator and standard deviation of the pulse output [*Completed JUN21*];
6. Task – Process and analyze waveform data acquired, compare to LTSPICE simulations, provide results to TCAD simulation team, formulate strategy to integrate into machine learning algorithm [*Completed JUN21*].

(B) Milestone – Construct/demonstrate a 4×2 SOS pulse generator prototype capable of producing ≥12-kV peak voltage, ≤1-ns risetime, ≤5-ns FWHM, ≥2-MW peak-power, ≥1-kHz PRF, ≥1,000 shots-per-burst, ≥500 number of bursts [*Ongoing, estimated completion by AUG21*].

1. Task – Work with TCAD simulation team (see Section 3.6) to compare-to, revise/update diode simulation model towards achieving refined and accurate diode performance and pulse generator circuit simulation output [*Ongoing–JUL21*];
2. Task – Refine and simulate circuit topological permutation(s) to include an increased number of parallel branches within an electrically optimal layout using Altium [*JUL–AUG21*];

(C) Milestone – Construct/demonstrate a M×N SOS pulse generator prototype capable of producing ≥20-kV peak voltage, ≤1-ns risetime, ≤2-ns FWHM, ≥8-MW peak-power, ≥1-kHz PRF, and $\geq 2\sigma_{V_{peak}}$, which operates in continuous-burst mode as a viable candidate for OSPRES Contract source alternative [*on hold until Milestone B is completed*].

(D) Milestone – Construct/demonstrate a 8×2 SOS pulse generator prototype capable of producing ≥48-kV peak voltage, ≤1-ns risetime, ≤2-ns FWHM, ≥46-MW peak-power, ≥10-kHz PRF, $\geq 2\sigma_{V_{peak}}$, ≥10,000 shots-per-burst, with a ≥50% duty cycle [*on hold until Milestone C is completed*].

Milestones for the second effort, and tasks to achieve them along with a timeline to do so, are as follows:

(E) Milestone – Through Boolean synthesis, generate a machine-learning algorithm, (which uses a decision-tree approach and iterative greedy algorithm) able to accurately predict the SOS-IES topology permutation's key performance metrics and produces the most efficient components and topologies in terms of pulser footprint [*Estimated completion by DEC21*].

1. Task – Perform literature review on genetic and machine learning algorithms [*JUL–AUG21*];
2. Task – Automate LTspice circuit simulation using Python scripting: auto generation of an input parameter card, autorun of that simulation space, and then the back-end processing of the output files [*JUN–AUG21*];
3. Task – Build a suitable predictive model for the SOS-IES modular architecture for a given performance matrix based on sample data obtained in Task 2 [*SEP–DEC21*].

4.5.3 Progress Made Since Last Report

Milestone A – The 2×2 DSRD-based SOS-IES pulse generator has been further tested to perform a parametric study varying the ON time of the trigger signal (T_{ON}) and the main supply voltage (V_{supply}). Keeping the V_{supply} consistent with the previous experimental results presented in last month's report (i.e., 225-V), the resulting peak voltage ($V_{out,peak}$) and risetime (t_{rise}; 20%-90%) was recorded while increasing T_{ON} from 100–400-ns where the results are presented in Fig. 4.5.1.

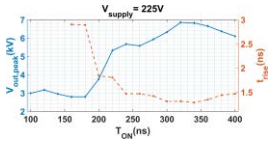


Figure 4.5.1. Resulting peak voltage and risetime achieved as a function of trigger length (T_{ON}) utilized in the 2×2 DSRD-based SOS-IES pulse generator.

As shown in Fig. 4.5.1, $V_{out,peak}$ increases and t_{rise} decreases with the increasing T_{ON} until it reaches 340-ns. Interestingly, once T_{ON} exceeds 340-ns, $V_{out,peak}$ decreases and t_{rise} increases. Analysis of this result is still in its earliest stages, however this result may be explained by the fact that DSRD accumulates an optimum concentration of charge carriers (i.e., saturation limit) when T_{ON} reaches 340-ns due to the optimum forward pumping current governed by LC oscillation and the ongoing recombination of the free carriers. This optimum accumulated of charge leads to shortest interruption time and highest peak value of the reverse current leading to highest $L(dI/dt)$, i.e. peak output voltage and fastest risetime when V_{supply} is not varied.

After selecting the optimum T_{ON} for this specific circuit, we varied the V_{supply} from 100-V to 200-V and plotted the observed $V_{out,peak}$ and t_{rise} as provided in Fig. 4.5.2.

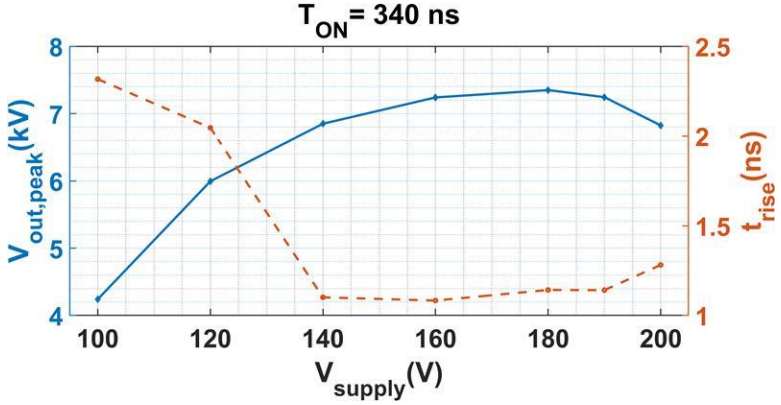


Figure 4.5.2. Resulting peak voltage and risetime achieved as a function of supply voltage utilized in the 2×2 DSRD-based SOS-IES pulse generator.

We found that there exists an optimum V_{supply} equal to 180-V that results in highest $V_{out,peak}$ and fastest t_{rise}. Additional experiment for higher T_{ON} and V_{supply} is needed to validate the trends in the obtained results. We had to limit both T_{ON} and V_{supply} up to 400-ns and 200-V, respectively because of the presently utilized SiC MOSFET's current rating limitation. The next iteration of the SOS-IES pulse generator will include SiC MOSFETs with the highest possible current rating available.

To ensure the pulser still achieved the required PRF of 1-kHz at the newly record peak voltage without compromise to the voltage output's standard deviation, the pulser was operated in burst mode (100 shot-burst) at a pulse repetition frequency (PRF) of 1-kHz, with T_{ON} = 340-ns and V_{supply} = 180-V. Fig 4.5.3 shows the output waveform (comb of pulses) demonstrating its excellent stability in the peak amplitudes where it maintains 97.8% peak voltage (i.e., $SD_{Vpeak} = 6\sigma$).

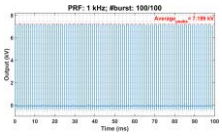


Figure 4.5.3. Comb of pulse outputs (100/100 pulses acquired) at a PRF of 1-kHz, with T_{ON} = 340-ns, and V_{supply} = 180-V.

Another interesting observation was that the output voltage waveform initially consists of three sequential pulses at short trigger lengths (< 200-ns). The reason for this is not clear but it may indicate a mismatch in timing of the current interruption of the first two diode stacks in parallel stages, resulting in a deviation in the final output pulse from its expected single pulse shape. As we increased the T_{ON}, the shape of the output pulse tends to get closer to the ideal singular output pulse shape. This phenomenon, depicted in Fig. 4.5.4, may be attributed to the fact that there exists a mismatch in the circuit parameters between the two parallel stages, ultimately resulting in the reverse current interruption of the DSRDs in these parallel branches occurring out of synchronization.

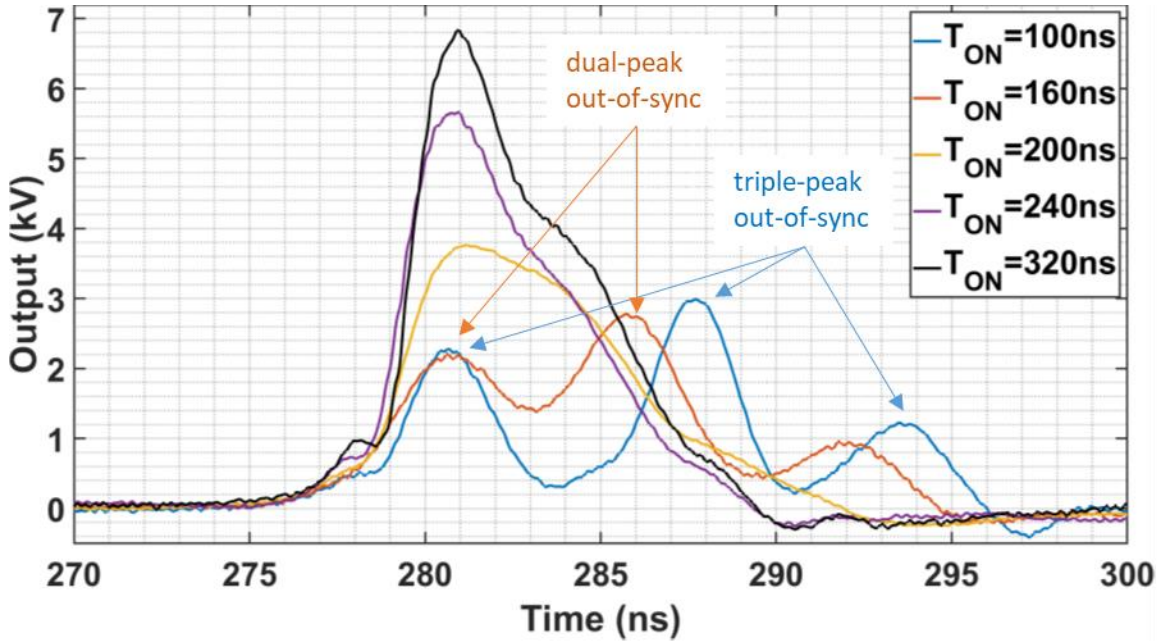


Figure 4.5.4. Waveform outputs as function of trigger signal duration (T_{ON})

The resultant pulses from the two parallel branches tend to become more synchronized with the increasing T_{ON}. We also observed large variations in the characteristics of the output voltage for different DSRD samples. For example, we achieved peak output voltage greater than 5-kV with one set of DSRD samples whereas another set of DSRD samples resulted in peak output voltage of ~3.3-kV provided that the operating conditions were the same such as T_{ON}=100-ns and V_{supply}=200-V.

Another modified version of the PCB layout of the previous 2×2 DSRD-based pulse generator circuit has been designed and sent out for fabrication. The modifications and improvements, in comparison to the previous design, include correction of gate-driver IC's footprint, larger total capacitance values of bulk input capacitor bank to help support PRF operation > 100-kHz while operating at an output voltage greater than 7-kV, and increased strategies within the layout to minimize and mitigate parasitic oscillations, ringing, and EMI pertaining to high-voltage and high-frequency operation. The 3D view of this modified version of the PCB layout is shown in Fig. 4.5.5 (a).

(a) (b) (c)

Fig. 4.5.5. 3D view of **(a)** modified PCB layout of 2×2 DSRD-based pulse generator circuit, **(b)** 1×1 DSRD-based pulse generator (base-unit), and **(c)** cylindrical DSRD clamp/housing.

In support of the research effort briefed in **Section 4.4** to evaluate the devices manufactured as described in **Section 4.3**, a 1×1 DSRD-based pulse generator (base-unit) has been designed and its PCB layout has been sent out for fabrication. This design includes a custom-designed cylindrical DSRD clamp/housing to help measuring characteristics of multiple press-pack DSRD packages. Fig. 4.5.5 (b) and (c) show the 3D-view of this base-unit of the DSRD-based pulse generator and a photograph of the cylindrical DSRD clamp/housing.

The waveform data acquired in the previous experimental setup (see ONR HPM MSR from MAY'21) has been compared to LTSPICE simulations and the results have been provided to the TCAD simulation team for comparison.

Milestone E – A Python script has been developed to automate LTspice circuit simulation of a 1×1 DSRD-based pulse generator (base-unit). This effort will be transitioned to **Section 4.6** during the remainder of this month.

4.5.4 Significant Finding(s) and Mission Impact

4.5.4.1 Summary to Date

Milestone A – Successful construction and operation of a 2×2 SOS-IES pulse generator prototype has been completed which meets or exceeds the milestone's required key

performance metrics. Shown in Table 4.5.1 are the previous and current pulse generator's performance specifications in comparison to a similar 2×2 pulser developed by Kesar *et al.* [1] using DSRDs, and to that of a commercial off-the-shelf (COTS) DSRD pulser of similar space and weight developed by Megaimpulse (i.e., PPM-0731) which also uses DSRDs with silicon avalanche shapers (SAS) [2]. Although the Megaimpulse pulser utilizes a SAS with a <500-ps risetime (a threshold we do not intend to go below due to Commerce Controlled List limitations), it is interesting to compare the results of linear voltage gain and peak power of this system, to that of one that utilizes a SAS.

Table 4.5.1

KPM	**Units**	**MIDE - V1** Previous	**MIDE - V2** Current	**Kesar *et al.*** SOTA	**MI-PPM0731** COTS
V_{supply}	V	225	180	300	160
T_{ON}	ns	100	340	?	200
V_{peak}	kV	5.59	**7.35**	5	6.3
Gain	V/V	24.8	**40.8**	16.7	39.4
$\tau_{rise,20\text{-}90\%}$	ns	1.2	1.142	1.96	0.12
dV/dτ	kV/ns	4.66	6.44	2.55	**52.50**
FWHM	ns	2	5.48	2.27	0.35
PW	ns	5	7	3.5	2.5
Z_{LOAD}	Ω	50	50	50	50
P_{peak}	MW	0.625	**1.080**	0.500	0.794
E_{pp}	mJ	0.125	0.154	0.143	0.318
PRF_{max}	kHz	100	100	100	15
Burst	shots	100	100	*N/A*	100
	%	100	100	*N/A*	100
SD_{Vpeak}	σ	> 2	**> 2**	*N/A*	*N/A*
	%	96.5	**97.8**	*N/A*	*N/A*

The current permutation of the 2×2 SOS-IES pulser developed by MIDE under the ONR OSPRES Grant is able to achieve a higher peak voltage and shorter risetime than DSRD-based pulsers reported in literature of comparable space and weight as well as those commercially available. The ability to generate a linear voltage gain of 40.8 to produce over a Megawatt of peak power into a 50-Ω load while achieving a peak voltage output standard deviation of 6σ when operating at a PRF of at least 100-kHz, brings this technology to the forefront of viable options to potentially support the Naval afloat mission.

4.5.4.2 Since Last Report

Milestone A – Further investigation of the optimal performance parameters through the systematic parametric study pinpointed the optimal trigger length and charge voltage for the 2×2 pulse generator developed for this effort. It is encouraging to compare this output with the 2×2 DSRD-based pulse generator proposed by Kesar *et al.* that could generate

up to 5-kV with a rise-time of 1.96-ns; of which the compression stage topology of this circuit is based on [1]. Additional experimental investigations for higher T_{ON} and V_{supply} is needed to verify the trends presented in this month's results, and to finalize the optimal performance parameters before moving onto the tasks set forth towards achieving Milestone B.

Milestone E – A Python script has been developed to automate LTspice circuit simulation of a 1×1 DSRD-based pulse generator (base-unit). This script can perform auto generation of an input parameter card, autorun of that simulation space, and then the back-end processing of the output files.

4.5.5 References:

[1] L. M. Merensky, M. Ogranovich, D. Shmilovitz, A. S. Kesar, and A. F. Kardo-Sysoev, '6-kV, 130-ps rise-time pulsed-power circuit featuring cascaded compression by fast recovery and avalanche diodes', Electronics Letters, vol. 49, no. 24, pp. 1539–1540, Nov. 2013, doi: 10.1049/el.2013.2129.

[2] http://www.megaimpulse.com/info/PPM0731.pdf

4.6 Optimizing SOS-IES Pulse Generator Performance with Machine Learning

This section is scheduled to be included in next month's MSR. Section 4.6 aims to provide information on the machine learning effort being developed to support the systematic topology optimization of the SOS-IES pulse generator being developed throughout the tasks within Milestones A–D in **Section 4.5**. This month kicks off this effort towards developing the automation tools to run large batches of parametric studies on the DSRD-based M×N in LTspice towards training the machine learning algorithm being developed. **Section 4.5**'s milestone E will be shifted to this section moving forward where results and expansion of the topic will be provided in next month's MSR.

4.7 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners

(Gyanendra Bhattarai)

4.7.1 Problem Statement, Approach, and Context

Primary Problem: High-voltage gas-based spark-gap switches (e.g., hydrogen switches) utilized in high-power microwave sources are limited in maximum pulse repetition frequency (PRF) (<1-kHz) and overall shot lifetime (<10^4 shots) due to their inherent gas breakdown recovery time and electrode erosion rate characteristics. To compound this issue, generating a hermetically sealed hydrogen switch is very difficult from both a design and manufacturing perspective, due to the atomic volume of hydrogen. Mitigation strategies to overcome this issue have included continuous gas supply designs which can increase the PRF by an order of magnitude (~10-kHz); however, at the pressures required for these gas switches to operate (>500-psi), this adds additional complexity, maintenance, and safety issues within these spark-gap systems, in comparison to their

hermetically-sealed counterparts, otherwise rendering them ill-suited for Naval afloat missions.

Solution Space: Utilize viable pulse shaping/compression technologies with key performance metrics comparable to those of hydrogen spark-gap switches (HSG) (i.e., a peak voltage >10-kV, peak power >1-MW, and a risetime $\leq$1-ns) within solid-state pulse generators to increase peak power, gain, and efficiency of the pulse generation system. The main categories and sub-categories of the technologies considered consist of the following:

- Semiconductor opening switches (SOS)
  - *Drift-step recovery diodes (DSRD)*
  - *Semiconductor opening switches (i.e., different doping profiles than DSRDs)*
- Semiconductor closing switches (SCS)
  - *Silicon avalanche sharpeners (SAS)*
  - *Delayed impact ionization diodes (DBD)*
  - *Reverse switching dynistors (RSD)*
  - *Deep level dynistors (DLD)*
  - *Fast ionizing dynistors (FID)*
- Thyristors

As viable alternatives, the aforementioned solid-state switches have significantly longer lifetime (>10^{11} shots) than spark gap switches and their PRF can be increased by implementing thermal mitigation strategies, unlike in gas switches which are limited by their long recovery time regardless of leveraging cooling technologies. Optimizing the solid-state switch's geometry and intrinsic properties to increase current handling capabilities through ideal doping profiles containing optimum carrier concentration, while minimizing the resulting joule heating effect, yields device arrangements (in series and parallel configurations) which enables switching 10's of GW of power. Performance metrics of viable all-solid-state alternatives to spark-gap gas-switches currently being evaluated are provided in Table 4.7.1.

Sub-Problem 1: Semiconductor closing switches, (e.g., silicon avalanche sharpeners (SAS), fast ionization dynistors (FID), deep level dynistors (DLD), and reverse switched on dynistors (RSD)), are not commonly available within the United States where fabrication and/or procurement of these devices requires long lead-times.

Sub-Problem 2: Silicon diodes generally break down below 3-kV. Thus, achieving >100-kV peak voltage and >100-kA peak current requires a combination of series and parallel stacks of diodes as discussed in Section 4.5. Stacking diodes in this type of configuration leads to increased pulse risetime. Optimization of diode stacks based on theory, simulation, and experiment is necessary to enhance switching performances. Additionally, exploring alternative wide bandgap (WBG) materials based on their known properties and theoretical simulations may lead to more robust switches, but would require significant time in developing device models and fabrication techniques.

Table 4.7.1. Comparison of SWaP-C key performance metrics for different pulsed power supplies and switches.

Semiconductor Pulsers & Shapers			SWaP-C Key Performance Metrics					
Product	Classification	Manufacturer	Peak Voltage kV	Peak Power MW	Risetime ps	Pulse Width ps	PRF kHz	I^2t J/Ohm
JOLT[1]	HSG	AFRL	1,000	12,000	80	100	0.6	0.014
H-3[2]	HSG	AFRL	1,000	25,000	130	300	2	0.187
SNIPER[3]	HSG		250	1,250	200	3,000	5	0.075
GP-81B	HSG	Excelitas	120					
PPG-7/10	DSRD/SAS	Megaimpulse	7	0.98	100	300	10	5.9E-6
PPG-2/1000	DSRD/SAS	Megaimpulse	2	0.08	600	1,500	1,000	
S-500[4]	SOS	RAS	900	13,000	3,000	7,000	1	1.451
FPG 200-p	FID/DRD	FID Technology	200	800	200	1,000	1	
FPG 1000-n	FID/DRD	FID Technology	1,000	10,000	1,000	1,000	1	
BNL[5]	FID		50	50	10,000	50,000	0.1	0.050
Ioffe[6]	Si-diodes	Ioffe	117	280	40			
Ioffe[6]	Si-Dynistors	Ioffe	515	5,500	450			
T343-500	Si-Thyristor		5		220			

Sub-Problem 3: Driving a single 100-μm thick silicon switch in the impact ionization mode requires input pulses >2-kV with voltage rise rate >0.5-kV/ns. For a stack of several switches in series, the peak voltage requirement increases proportionately. Semiconductor opening switch (SOS) based pulsed-power generators, which are also limited in availability as COTS products, are required for driving impact ionization-based switches.

Sub-Problem 4 (Fundamental Physics): The phenomenon behind the origin of free carriers that trigger the impact-ionization at higher-than-breakdown fields when applying a sharply increasing voltage pulse is not completely known. A University of New Mexico study[7] has concluded that the operation of a SAS is inconsistent with the theory described by Russian scientists. Further, it is not clear whether the switching (generation of electron–hole plasma) is uniform across the device area nor is localized (filamentary). Such different mechanisms are believed to be dependent on device geometry and doping concentration based on experimental evidence. It is crucial to understand those mechanisms to devise even faster and more powerful switches.

State-of-the-Art (SOTA): Hydrogen-based spark gap switches provide the highest peak-voltage output and are accompanied by the shortest risetimes of the technologies evaluated. Large (>1-m^3) SOS-based pulsers which utilize hundreds of diodes stacked in series, as well as FIDs, can produce equivalent peak voltages (~ 1-MV), and peak power outputs (~ 1-GW).

Deficiency in the SOTA: Closed-loop hydrogen spark-gap switches (HGS) are limited in their PRF capabilities (< 1-kHz) deeming them unable to achieve the performance requirements for DSRD/SOS-based pulse generators. FID-based pulsers are limited by their long risetime and long pulse width, deeming them ill-suited options which produce the necessary frequency spectra and high pulse energy, comparable to the DSRD pulser, as direct SWaP replacements which improve the SOTA. DSRDs and SOS diodes alone, while able to achieve the PRF and pulse performance metrics necessary, are limited in their ability to achieve increased peak voltage/power requirements without compromise to the ultracompact form-factor of the system (<0.1-m^3).

Solution Proposed: Downselect viable replacement(s)/additional(s) technologies which meet or exceed the performance parameters set forth in Section 4.5's Milestone's A-D. Optimize SAS diode, dynistor, and/or thyristor structure (material, topology, geometry, doping concentration, packaging) to increase peak reverse current while enhancing thermal dissipation by combining semiconductor and thermodynamic simulation tools, such as TCAD and COMSOL Multiphysics. Utilize the data produced from these simulations in correlation with the results obtained from experiments of available semiconductor closing switches. Systematically optimize the circuit, numbers of diodes/dynistors in series/parallel, and use transmission line topology packaging of diode-stacks to achieve >100 kV output pulses with subnanosecond risetime.

Relevance to OSPRES Grant Objective: The alternative all-solid-state technologies presented in Table 4.7.1 could individually, or in combination, provide the means to produce order(s) of magnitude greater peak power, without severe limitation to PRF, as SWaP-centric means to increase the capability and extent of protecting naval assets.

Risks, Payoffs, and Challenges:

Risks: The performance tradespace regarding these different technologies is both diverse and extensive due to their unique mechanisms of operation being very different. Where one technology might produce the greatest peak power, it is normally accompanied by worst-in-class PRF performance. Down-selecting one technology based on peak power output alone presents risk to other secondary or tertiary performance metrics such as PRF and pulse energy, which risks developing ill-suited technologies to support the float mission.

Simulating a fast ionizing dynistors (FID) within a pulsed-power generator, requires different models, setups, and understanding, even in comparison to their closely-related reverse switching dynistors (RSD), let alone SOS or thyristor-based models. This leads to risk of not meeting down-select gates within reasonable time frames. Additionally, as new technology emerges via research, scope creep to numerically and experimentally evaluate new technologies may delay transitioning these technologies into viable systems.

With the high levels of peak (and average) power associated with these systems, thermal management necessities may prove inevitable and more extensive than their photoconductive semiconductor switch (PCSS) or DSRD-based counterparts.

Payoffs: The SWaP-C tradeoff of generating a non-laser-based system with any number of these systems can yield a higher fidelity pulsed-power waveform output. Determining

which technology is viable and feasible in terms of the key performance metrics should yield a more ultracompact form factor pulse generator with order(s) of magnitude greater power density without compromise to overall size and weight to the system.

Challenges: Determining the true performance metrics of interest based on these highly different devices is challenging. Without a more robust and deep understanding of their operation, and how to utilize them within a pulse generator topology, in a swappable configuration or otherwise, requires additional time and consideration. Managing the tradeoff between the academic understanding of the technologies of interest presented in the foregoing table, and the transition to prototype effort/mentality, will require both a delicate balance and leveraging the pulsed-power team's combined effort.

4.7.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Downselect viable technology as replacement to currently utilized DSRD which increases at least one of the key performance metrics by an order of magnitude without compromise to the overall volume of the system [*Estimated completion by AUG21*].

1. Task – Finalize literature study of different technologies and topologies and compare SWaP tradeoff evaluation to PCSS and DSRD-based pulse generators [*JUN–JUL21*];
2. Task – Determine which DSRD alternatives are commercially available that could be used to either replace DSRD, or be used as pulse shaper/sharpening devices to improve pulse generator performance [*JUN–JUL21*];
3. Task – Select appropriate devices among commercially available DSRD alternatives for further experimental verification of their performance metrics. [*JUL–AUG'21*];

(B) Milestone – Model and numerically verify the performance of the downselected technology as a direct replacement, or additional component in tandem with DSRDs utilized within a SOS-IES pulse generator, which meet or exceed the necessary performance requirements. [*on hold until Milestone A is complete*].

1. Task – Design experimental circuit with one selected SAS/dynistor and obtain theoretical performance metrics using standard electronic simulation tools such as LT-Spice. [*JUL–AUG21*];
2. Task – Experimentally verify whether the selected device topology can be an HSG alternative in terms of peak power produced and the pulse risetime. [*JUL–SEP21*];

(C) Milestone – Model diode/dynistor topologies using silicon or alternative WBG materials and fabrication process. [*on hole until Milestones A and B are completed*].

1. Task – Model silicon and/or alternative diode, and dynistors with optimized device cross section (size, geometry) based on theory and simulations to increase current and thermal dissipation. [*JUL–SEP21*];
2. Task – Model/design fabrication process with optimum device topology and doping concentration. [*SEP–OCT21*]

4.7.3 Progress Made Since Last Report

Milestone A – A segment of the scientific literature on HSG, DSRD/SOS-IES based switches and semiconductor alternatives (SAS, FID) for pulse sharpening have been reviewed. A complete comparison of SWaP-C performance metrics of these devices is in preparation.

4.7.4 Significant Finding(s) and Mission Impact

4.7.4.1 Summary to Date

Milestone A – No single technology appears to meet or exceed the key performance metric requirements across the board. Where HGS lead in peak voltage and peak power, in comparison to the other technologies of interest, they lack in their ability to meet the required PRF, device lifetime, and SWaP-C metrics.

4.7.4.2 Since Last Report

As this is first time, this section will be updated in the next report.

4.7.5 References

1. Baum, C. E. *et al.* JOLT: A highly directive, very intensive, impulse-like radiator. *Proc. IEEE* **92**, 1096–1107 (2004).
2. Agée, F. J. *et al.* Ultra-wideband transmitter research. *IEEE Trans. Plasma Sci.* **26**, 860–873 (1998).
3. L. F, R. & Buttram, M. T. Sandia National Laboratories' High Power Electromagnetic Impulse Sources.
4. Rukin, S. N. Pulsed power technology based on semiconductor opening switches: A review. *Rev. Sci. Instrum.* **91**, (2020).
5. Zhang, W. *et al.* Accelerator fast kicker R&D with ultra compact 50MVA nano-second FID pulse generator. *Dig. Tech. Pap. Int. Pulsed Power Conf.* (2013) doi:10.1109/PPC.2013.6627620.
6. Gusev, A. I., Pedos, M. S., Rukin, S. N., Timoshenkov, S. P. & Tsyranov, S. N. Semiconductor sharpeners providing a subnanosecond voltage rise time of GW-range pulses. *Rev. Sci. Instrum.* **88**, (2017).
7. Schamiloglu, E., Fleddermann, C. B., Focia, R. & Gaudet, J. A STUDY OF ADVANCED SEMICONDUCTOR SWITCH PHYSICS AND TECHNOLOGY PHILLIPS LABORATORY Advanced Weapons and Survivability Directorate AIR FORCE MATERIEL COMMAND KIRTLAND AIR FORCE BASE, NM 87117-5776. (1997).

5.0 Pulse Forming Networks

5.1 Diode-Based NLTLs

(Nicholas Gardner)

5.1.1 Problem Statement, Approach, and Context

Primary Problem: The size, weight, and cost of pulse forming/shaping networks (PFNs) need to be reduced and optimized for Navy afloat missions.

Solution Space: Develop a diode-based nonlinear transmission line (D-NLTL) as a pulse shaping network for the conversion of energy to the ultra-high frequency (UHF) band at single MW peak power.

Sub-Problem: Metrics used for component selection are designed for D-NLTLs operating at sub 0.1 GHz frequencies. Using such metrics alone to design D-NLTLs capable of single GHz frequency generation introduces a trial by error nature to the design process wherein frequency/power generation predictions and measurements can differ by a few hundred MHz or the design potentially fails to operate at all.

State-of-the-Art (SOTA): D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit. Simulations of LE-NLTLs indicate achievable frequencies in the single GHz range.

Deficiency in the SOTA: Simulation/measurement agreement becomes increasingly sensitive to parameters and factors outside of inductive and capacitive element choice alone at frequencies above ~100 MHz. Disparities between measurement and simulation above contribute to a trial by error design process for D-NLTL networks.

Solution Proposed: Identify and characterize diode parameters affecting frequency generation in the context of a NLTL application and identify limits/desired ranges required for UHF generation. Such parameters include, but are not limited to: diode frequency response, diode reverse bias hold-off voltage, diode small signal capacitance, diode chip/package parasitics, and diode relaxation time. The improved understanding of the explored parameters will be used to design and fabricate a D-NLTL capable of GHz center frequency generation at single MW peak powers.

Relevance to OSPRES Grant Objective: The SWaP-C^2 capabilities of D-NLTLs (shown in Figure 3.3.1) represent a potential solution to the size, weight, and cost optimization issue for PFNs on Navy afloat missions.

Figure 5.1.1. 20 cell LE-NLTL of dimensions 1.1 x 23.45 cm constructed with COTS components.

Risks, Payoffs, and Challenges: There exists a potential tradeoff between power and frequency generation. Devices such as ceramic capacitors may be used in a D-NLTL to generate high peak power due to their break down potentials in the 10s of kV, however,

such devices become highly resistive at 0.1–0.2 GHz frequencies. Diodes have been shown to be operational at frequencies upwards of 0.4 GHz, however, possess low hold-off potentials limiting peak output power. The payoff to overcoming these challenges is significant reductions in PFN size and cost.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Construct/demonstrate a prototype capable of UHF generation at low voltages (1–100 V excitation amplitude)

(A1) Break a low-voltage pulse into a sequence of solitons (SEP20)
(A2) Increase frequency generation past 200 MHz (NOV20)
(A3) Select diode candidate (junction capacitance <50 pF) and simulate expected results (Ongoing)
(A4) Design/fabricate/test line (Ongoing)

(B) Milestone – Demonstrate tuning of waveform at low voltages using electrical or mechanical means (**Completed with voltage biasing APR21**)

(B1) Simulate a topology capable of biasing the diodes using a DC voltage (Completed JAN21)
(B2) Perform Initial tests and refine prototype to reduce loss (Completed FEB21)
(B3) Show electrical tuning with a positive DC bias (Completed MAR21)
(B4) Show electrical tuning with a negative DC bias (Completed APR21)
(B5) Demonstrate the use of bipolar excitations with a voltage-biased line (**Completed JUN21**)

(C) Milestone – Construct/demonstrate a prototype capable of frequency generation above 1 GHz at single MW peak powers (Completed MW peak power but not GHz center frequency – Ongoing)

(C1) Identify diode candidates with a hold-off voltage of several kV and a low signal junction capacitance under 100 pF (Completed JAN21)
(C2) Design/fabricate single diode prototypes (Completed JAN21)
(C3) Perform initial tests using half-barrel pulse source (Completed FEB21)
(C4) Refine simulation using measurements (Completed FEB21)
(C5) Test a prototype using two diodes in series (Completed FEB–MAR21)
(C6) Test lines using Mega Impulse source (Completed MAY21**)**
(C7) Test K50F D-NLTL using PCSS as a source (**Completed JUN21**)
(C8) Use simulations and tests to refine line for increased frequency generation (**Ongoing JULY21)**
(C9) Rebuild lines for negative polarity pulses (**Ongoing JULY21**)
(C10) Test lines using PCSS as a source with various cell inductances **(Ongoing JULY21)**
(C11) Test lines using Marx Generator as a source (**Ongoing JULY21**)

(D) Milestone – Demonstrate power scalability using an array of D-NLTLs (**Ongoing**)

(D1) Design a prototype capable of running two D-NLTLs simultaneously off of the same excitation pulse (**Completed JUN21**)

(D2) Build a circuit capable of measuring the CV curve of low-voltage diodes and measure the CV curves of unused diodes and heavily used diodes (**Completed JUN21**)

5.1.3 Progress Made Since Last Report

(B) The voltage tunable line was successfully used with bipolar excitation pulses. Bipolar pulses can be used if the line is biased to the amplitude of the bipolar pulse and has the advantage of being able to saturate the diodes more than a monopolar pulse due to the source-line impedance mismatch.

(C) The K50F D-NLTL was tested with the PCSS source. The resultant waveform had a center frequency of 700–800 MHz and a Bragg cutoff frequency of 1.25 GHz.

5.1.4 Significant Finding(s) and Mission Impact

5.1.4.1 Summary to Date

(A) After a failure of the high-voltage diode-based nonlinear transmission lines (D-NLTLs) to reproduce simulated results, work refocused on low-voltage D-NLTLs to determine the source of the discrepancy. In NOV2020 a center frequency of ~250 MHz was achieved using a D-NLTL design based on the diode model SMV1702.

(B) Following the success of the SMV1702 D-NLTL, a circuit was designed capable of electrically tuning the center frequency utilizing DC biasing of the diodes. In FEB–APR2021 the circuit demonstrated a linear relationship between DC bias up to a limiting potential. Negative DC biases decreased center frequency while positive DC biases increased center frequency.

(C) In JAN2021 two diode candidates (models K100F and K50F) were identified for a HV D-NLTL design. FEB2021 saw successful tests of both D-NLTLs with each sharpening the rise time of a pulse produced by a DSRD based source down from ~1 ns to ~600 ps.

(D) During MAY2021 a line topology capable of feeding two identical D-NLTLs with the same pulsed source at the same time. Initial results were collected, and a prototype is currently being designed to test the ability to parallelized D-NLTLs.

5.1.4.2 Since Last Report

Voltage Tunable Prototype (B): The same voltage tunable circuitry that allows for electrical control over the produced waveform center frequency can also enable the use of bipolar excitation pulses with the network. To utilize a bipolar excitation, the line must be biased to the amplitude of the excitation pulse. With bias the negative polarity portion of the excitation pulse will drop the potential across the leads to zero instead of causing the diodes to conduct. The advantage of utilizing bipolar excitations is shown in the right panel of Figure 5.1.2, where the 10 V peak-to-peak square results in a 8 V excitation after the source-line interface. The 8 V excitation results in greater diode saturation and an increased center frequency of 263 MHz. For comparison, a 10 V monopolar pulse was

utilized with the same line model and resulted in a 3 V amplitude after the source-line interface and a center frequency of 250 MHz.

GHz MW D-NLTL Prototype (C): The HV lines based on diode models K50F and K100F continue to be characterized with different HV sources. Most recently the K50F line was utilized with the PCSS set up. Results showed the network breaking the square PCSS pulse into two solitons with center frequencies ranging from 700–800 MHz across the tested range of charges and a Bragg frequency of 1.25 GHz. However, to get the test to work, the positive and negative connections of the N-type RF connections had to be flipped to allow for the negative polarity pulse to be accepted and used by the D-NLTL. As such it is believed that the functionality of the D-NLTL can be improved by rebuilding the lines to properly accept negative polarity pulses by flipping all of the diodes. The K50F line has since been re-built with the K100F line to follow. Post-rebuild, the lines will be tested once again with the PCSS using cell inductances of 12 nH, 6.6 nH, and 3.3 nH.

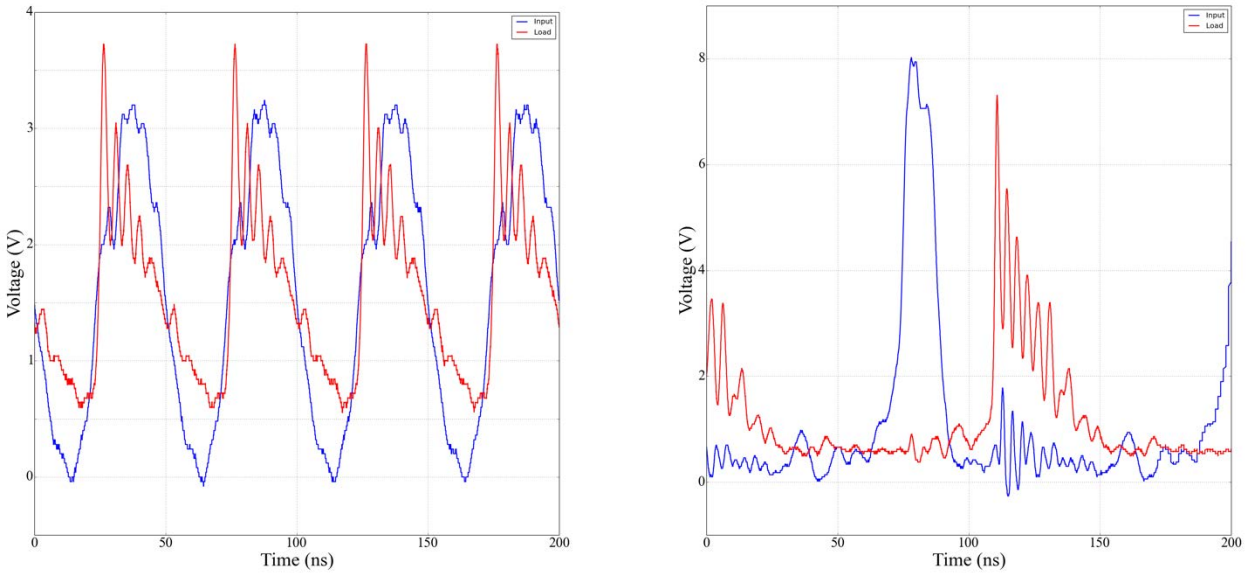


Figure 5.1.2. Two bipolar excitation pulses used with the voltage-tunable D-NLTL based on the SMV1702 model diode. (Left) A 20 MHz sine wave with a peak-to-peak amplitude of 10 V. (Right) An 8 MHz square wave with a 20% duty cycle and a peak-to-peak amplitude of 10 V. In both images blue gives the excitation waveform after the source-line interface and red gives the waveform at the load.

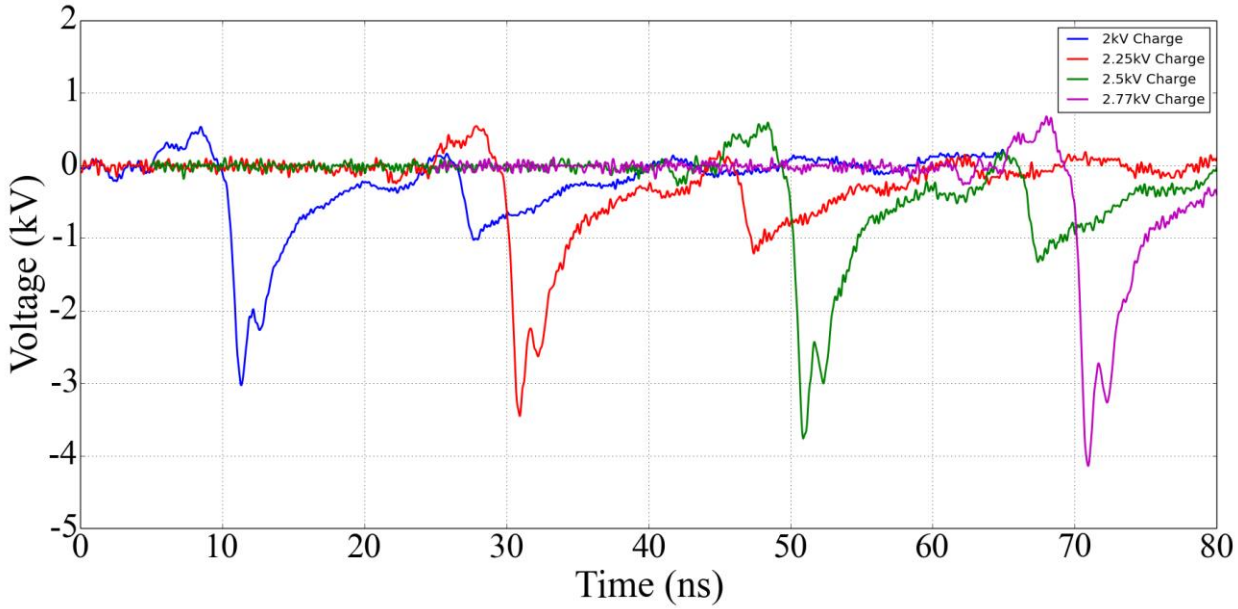


Figure 5.1.3. Waveforms produces for 4 charges of the PCSS. Waveforms are superimposed and separated for viewing ease. In all cases the network successfully broke the excitation into solitons with a center frequency range of 700–800 MHz and a Bragg frequency of 1.25 GHz.

6.0 Tradespace Analysis of Ultra-Wide-Band Antenna Arrays

6.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

6.1.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wideband (UWB) antenna elements in a phased array for high-power microwave (HPM) transmissions.

Deficiency in SOTA: Large physical aperture size of the antennas.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters, followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area. Using stochastic and machine learning (ML) algorithms to optimize antenna element and array performance.

Relevance to OSPRES Grant Objective: Provides design and optimization guidelines for UWB ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

6.1.2 Tasks and Milestones / Timeline / Status

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN–MAY 2021 / Completed code.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN–MAY 2021 / Completed investigations of arrays on infinite ground planes.

(C) Build minimum viable validation prototypes of single ESA elements on substrates that have good power handling capabilities for HPM transmissions at UHF range (such as FR-4, TMM-10i, TMM-6) / JAN–AUG 2021 / Ongoing time-domain reflectometry (TDR) testing of the designed antenna elements.

(D) Optimization of ESA (single element) performance using regular and ML based stochastic search algorithms / JUN–SEP 2021 / Ongoing.

(E) Build minimum viable validation prototypes for arrays of ESA elements / JUN–SEP 2021/ Ongoing.

6.1.3 Progress Made Since Last Report

(C) Build minimum viable validation prototypes of single ESA elements:

a. Modeled a coaxial probe-fed rectangular microstrip patch antenna on G10/FR-4 ($\varepsilon_r = 5.2$) substrate in the UHF range (0.756–1.121 GHz) via FEKO.

b. The antenna yields $\geq 30\%$ 2:1 VSWR bandwidth with a peak gain of ~ 5 dBi.

(D) Optimization of ESA (single element) performance using regular and ML based stochastic search algorithms:

a. Investigated into the bandwidth enhancement of a microstrip patch antenna, by optimizing the feed-probe location, using regular and ML based genetic algorithms (GAs).

b. Implemented ML algorithms to estimate the S_{11}-parameter and/or VSWR and directivity of a microstrip ESA element on different ground plane shapes and sizes.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

a. Completed initial modeling of a 3×3 array of ESAs, on a 1.25” thick G10/FR-4 board, at the UHF range (0.756–1.121 GHz).

6.1.4 Significant Finding(s) and Mission Impact

6.1.4.1 Summary to Date

(A) Developing Array Pattern Tool for large arrays calculations:

A MATLAB code has been developed for faster approximation of radiation pattern of a linear/planar array of any size and composed of any type of antenna elements. The code requires the center element pattern of a small array (say, 3×3) composed of same type of antenna elements, desired lattice arrangement, and total number of array elements, as user inputs. This work will be included in future publications.

(B) Investigate the effects of array aperture area reduction on different array parameters:

The effect of different array aperture area and lattice arrangements, on the array parameters (such as, array gain, beamwidth, electronic beam steerability, etc.), has been reported for arrays modeled on infinite ground planes (DEC 2020 ONR-OSPRES-Grant MSR). The results show that with 30% reduction in the aperture area (≈50% reduction in # of elements), the gain drops by < 3.5 dBi without any scan blindness spotted as the main beam is steered from boresight to $\pm 60^\circ$ in the range 640–990 MHz.

The array parameters for large arrays ($\geq 15 \times 15$) on finite ground planes could not be computed using the commercial EM solvers (FEKO and CST) due to excessive memory

and time consumption. This work will be resumed after developing a method to estimate array performances on finite ground planes, either through ML or conventional approaches.

(C) Build minimum viable validation prototypes of single ESA elements:

Investigated different bandwidth enhancement techniques applicable to single layer microstrip patch ESAs:

a. Method I: Bandwidth enhancement by strategically placing the coaxial probe along 2/3rd the patch diagonal – This method is proposed and experimentally validated using prototypes manufactured on TMM-6 and TMM-10i substrates at 2.5–5 GHz. An antenna has been modeled on a G10/FR-4 substrate, at the UHF range (0.6–1 GHz) and is being considered for manufacturing.
b. Method II: Coaxial probe-fed U-slot loaded rectangular microstrip ESAs – A prototype is manufactured on a G10/FR-4 substrate (0.9–1.3 GHz) and tested.
c. Method III: L-probe-fed U-slot-loaded rectangular microstrip ESAs – An antenna has been modeled on a TMM-4 substrate that operates in the 0.52–1.17 GHz range ($\approx 77\%$ 2:1 VSWR bandwidth). Due to the complexity in fabrication of the L-probe-feed, this antenna is not being manufactured.

(D) Optimization of ESA (single element) performance using regular and ML based stochastic search algorithms:

Investigated the bandwidth enhancement of the coaxial probe-fed microstrip patch antennas, using regular and ML based stochastic search algorithms (GA, PSO, and Simplex methods), by optimizing the feed-probe location and ground plane shape and size. Compared to regular search algorithms, ML algorithms are found to be less computationally intensive (in terms of time and memory consumption).

(E) Build minimum viable validation prototypes for arrays of ESA elements:

A 3×3 array of microstrip ESA elements, on a TMM-10i board, has been manufactured and tested at the 2.5–5 GHz range. Initiated modeling of a 3×3 array of microstrip ESAs on a 1.25” thick G10/FR-4 substrate for operation in the UHF range (0.6–1 GHz).

6.1.4.2 Since Last Report

(C) Build minimum viable validation prototypes of single ESA elements:

A coaxial probe-fed microstrip patch antenna has been modeled, in FEKO, at the UHF range (0.6–1 GHz) on a G10/FR-4 ($\varepsilon_r = 5.2$) substrate, with the probe placed along 2/3rd the patch diagonal. A 38.89% 2:1 VSWR bandwidth has been obtained using the model (0.756–1.121 GHz) with a peak gain of 4.97 dBi. The antenna geometry and its VSWR and gain characteristics are illustrated in Fig. 6.1.1.

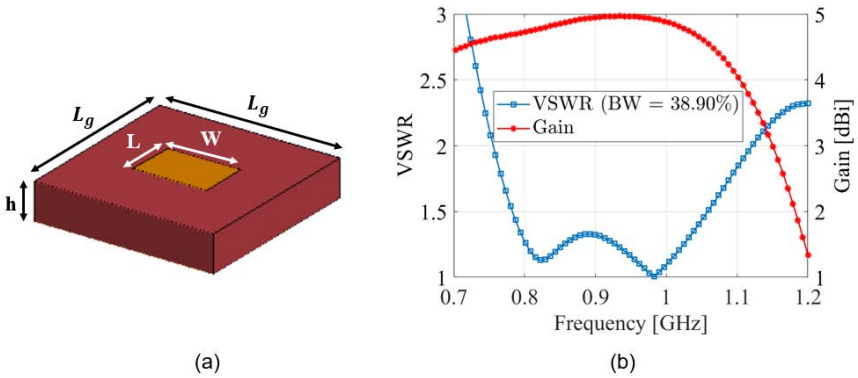


Fig. 6.1.1. (a) CAD model of the coaxial probe-fed microstrip patch antenna on G10/FR-4 substrate ($\mathrm{h} = 1.25, \mathrm{L_g}$=5", $\mathrm{L} = 50.42\ \mathrm{mm}, \mathrm{W} = 75.63\ \mathrm{mm}$); (b) VSWR and gain of the antenna.

(D) Optimization of ESA (single element) performance using regular and ML based stochastic algorithms:

(a) Task 1:

Objective: Seeking the best feed-probe location in a microstrip patch antenna element with the objective of bandwidth enhancement.

Procedure followed: A coaxial probe-fed microstrip patch antenna is modeled, using FEKO, on a 0.25" TMM-6 ($\varepsilon_r = 6$) substrate, at the center frequency of 3.75 GHz. The antenna dimensions are calculated using the standard equations given in [1]. Using the FEKO Method-of-Moment (MoM) solver, the VSWR of the antenna is obtained, for the feed-probe located exactly at the center of the patch, (x_p, y_p) = (0 mm, 0 mm). This input–output (probe location–VSWR) pair is used as the training data for ML (in the Altair HyperStudy platform). Next, using both regular (available in FEKO) and ML (HyperStudy) based GAs, the probe location is obtained which provides the best 2:1 VSWR bandwidth. The results are summarized in Table 6.1.1.

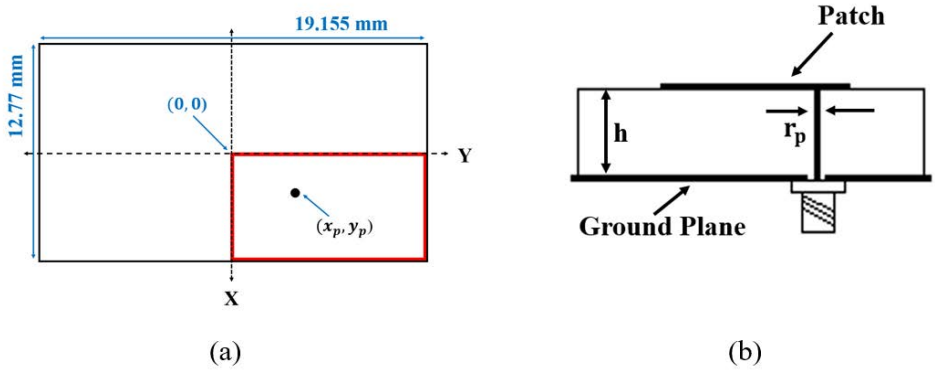


Fig. 6.1.2. (a) Top view of the patch showing probe location (x_p, y_p) and search region (in red); (b) Side view of the antenna.

Table 6.1.1. Comparison of the regular and ML based GA optimizer in finding the best probe location (x_p, y_p) in the microstrip ESA, designed on a TMM-6 substrate.

Parameters	Regular GA	ML based GA
Optimization variables	(x_p, y_p)	
Optimization goal	VSWR < 2	
Initial (x_p, y_p) (mm, mm)	(0,0)	
Search area	Shown in red in Fig. 5.1.2 (a).	
Optimized (x_p, y_p) (mm, mm)	(5.0001, 7.6471)	(5.4251, 8.3141)
No. of iterations	10	10
Runtime (hr:min:sec)	04:03:06	Data Collection: 00:10:00 Training Model: 01:25:00 Optimization using Trained Model: 00:00:10 Total: 01:35:10
% BW	32.9866	31.8418

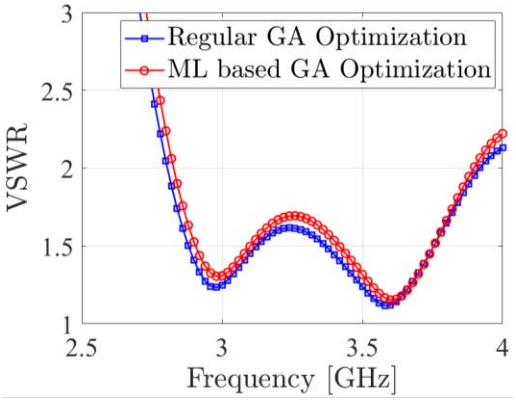


Fig. 6.1.3. Comparison of the VSWR response for the optimum probe locations obtained from regular and ML based GA optimization tools.

Remark: The optimum probe-location predicted by the ML based and the regular GAs are found to be close and with almost equal impedance BWs (32.99% and 31.84% from regular and ML resp.). In addition, the ML based GA was found to be $\sim 39\%$ faster.

(b) Task 2:

Objective: To estimate S_{11}-parameter and directivity of a coaxial probe-fed microstrip patch antenna on grounded substrates of varying shapes (circular and elliptical).

Procedure followed: A rectangular microstrip patch antenna is modeled on an elliptical TMM-10i $(\varepsilon_r = 9.8,\ \tan\delta = 0.002,\ \mathrm{h} = 6.35\ \mathrm{mm})$ substrate with $r_u = 30$ mm (See Fig. 6.1.4). S_{11}-parameter and directivity vs. frequency, for 51 frequency points, over 2.5–5 GHz, are obtained via FEKO MoM solver and is used as the training data for ML. The

Radial Basis Function (RBF) based ML algorithm is now used to estimate the S_{11}-parameter and directivity of the antenna for any r_u value between 10 mm to 50 mm (keeping area of cross-section of the ground plane backed TMM-10i substrate constant at 17.35 cm^2). The accuracy of the estimated S_{11} and directivity vs. frequency is compared with the full wave simulated (FEKO) data for $r_u = 15$ mm and 23.49 mm (shown in Fig. 6.1.5).

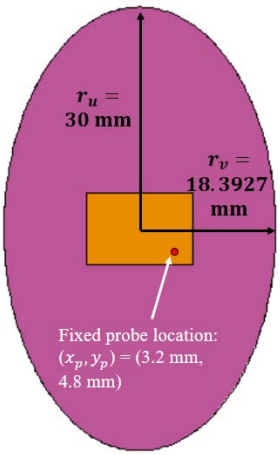


Fig. 6.1.4. CAD model of the initial microstrip patch antenna model.

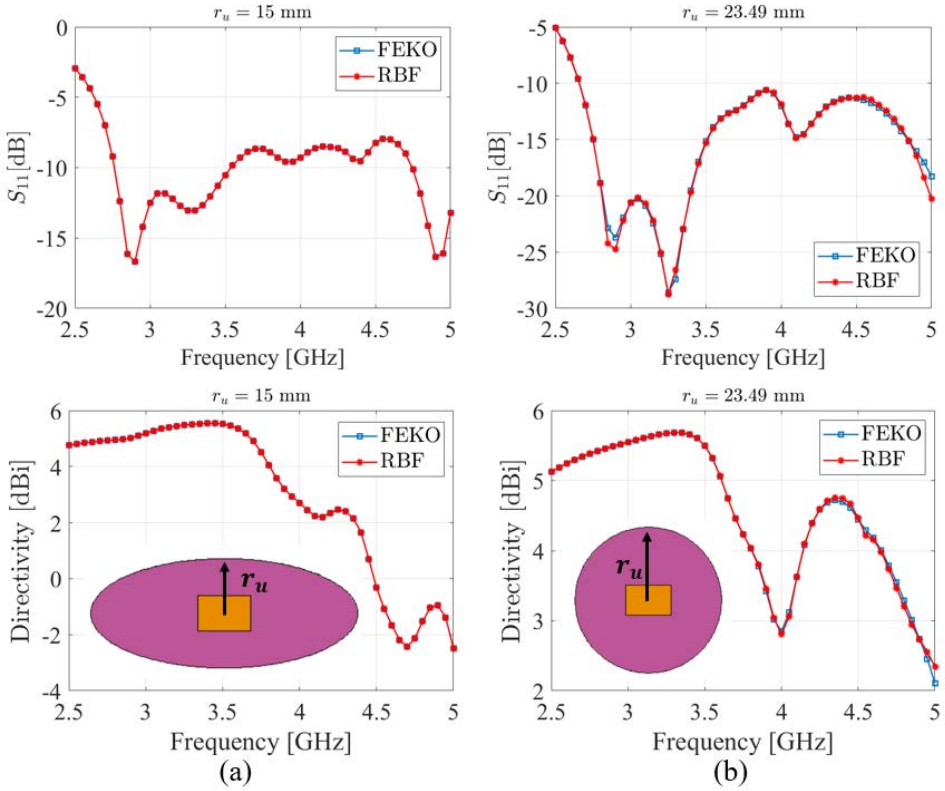


Fig. 6.1.5. Comparison of the ML estimated S_{11} and directivity of the antenna with FEKO MoM data for (a) $r_u = 15$ mm and (b) $r_u = 23.5$ mm.

Remark: The RBF based ML algorithm is shown to predict the antenna response very accurately. The accuracy of estimation can be further improved by increasing the number of training data points.

6.1.5 References

[1] D. R. Jackson, *Introduction to Microstrip Patches,* IEEE International Symposium on Antennas and Propagation and USNC-URSI National Radio Science Meeting. Jul. 2013.

6.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna

(Kalyan Durbhakula)

6.2.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelev antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem: The total surface currents on the Koshelev antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not yet clearly understood.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelev antenna that effectively reduce its physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelev antenna has been shown in the literature to withstand higher voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelev antenna can handle high input voltages (and therefore high power with 50 Ω

input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelev antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelev antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelev antenna.

(iii) The large electrical size (>5λ) of the Koshelev antenna at its highest operating frequency poses huge computational challenges. Efforts are underway to cleverly select important design parameters for the tradespace study.

6.2.2 Tasks and Milestones / Timeline / Status

(A) Complete literature search to identify and list antenna elements that satisfy UWB properties and HPM requirements, and down select accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelev antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB–MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t, \phi, \theta)$) in receive or transmit mode / MAR–APR21 / Complete.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelev antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / MAR21/ Complete.

- Milestone: Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain over the desired bandwidth, and aperture efficiency.

(F) Reduce Koshelev antenna aperture size (H×W) to equal to or less than 90 mm × 90 mm, equal to that of the SOTA BAVA, for direct antenna metrics comparison / MAR–APR21 / Complete.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, aperture efficiency equal to or greater than 130% at 900 MHz.

(G) Using the optimized model from (F), build various array simulation models/topologies to perform a tradespace study and report tradeoffs between array antenna metrics such as center element S11 value, gain vs theta at constant phi, physical aperture area, aperture efficiency and rE/V / MAY–JULY21/ Ongoing.

- Milestone: Develop/showcase an optimized Koshelev array model that exceeds an aperture efficiency of 130% with a high rE/V.

(H) Perform literature search to investigate, understand and determine the applicability of special electromagnetic (EM) techniques to the antennas under consideration. / JAN–APR21 / Complete.

6.2.3 Progress Made Since Last Report

(G) The May21 MSR provided some insight into how different Koshelev array topologies radiate and the variation in gain as a function of elevation angle. From different Koshelev array topologies, the diamond array topology has been selected for its compact size while retaining the same characteristics as the square array. To further improve our understanding of the Koshelev array antenna radiation in the time domain, we considered varying the pulse duration of the input pulse. In addition, a series of simulation studies were carried out to identify the contribution of each Koshelev element to the gain with respect to their relative positioning in a diamond array topology. We did this by periodically switching off (passive) one Koshelev element while exciting all other Koshelev elements in the diamond array. The four cases can be found in Fig. 6.2.1.

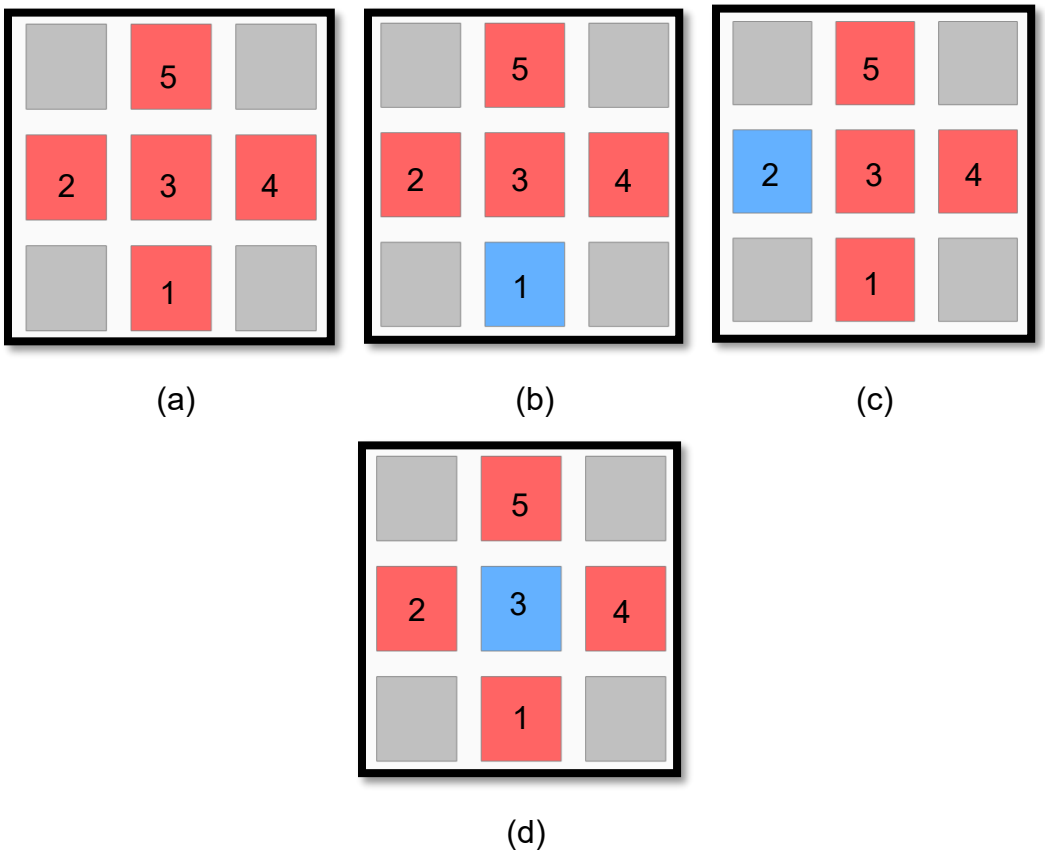


Fig. 6.2.1. (a) All elements active, (b) Element#1 – passive, (c) Element#2 – passive, and (d) Element#3 – passive.

6.2.4 Significant Finding(s) and Mission Impact

6.2.4.1 Summary to Date

(A) An extensive literature search on various UWB antenna elements has resulted in finding three promising options. The down-selected elements are the Koshelev, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the single antenna element. Later, the single antenna element will be converted into a planar array.

(B) Initial validation of the Koshelev antenna simulated using CST software agreed well with the antenna metrics published in the open literature [1]. A UWB bandwidth response (10:1 bandwidth) and rE/V > 1 has been observed from our initial simulations of the Koshelev antenna. This validation ensured that the Koshelev antenna can be subjected to further tradespace studies to understand its performance followed by optimizing the design according to OSPRES grant requirements.

(C) The initial tradespace study and analysis of the Koshelev antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between the Koshelev antenna in [1] and aperture reduced Koshelev antenna are shown in Table 5.2.1 of the APR 21 MSR.

(D) An in-house code has been developed to calculate important UWB time domain antenna metrics such as full-width half maximum (FWHM) and ringing. These metrics have been calculated using in-house MATLAB code using the excitation voltage and radiated electric field information obtained from CST simulations. FWHM and ringing antenna metrics help with assessing or characterizing an antenna's UWB response.

(E) The tradespace study of feed position provided a deeper understanding of how its position impacts the S11 bandwidth. An optimum value for feed position i.e., $F = 1/20 < L < 1/10$ is recommended to achieve maximum bandwidth. The tradespace study of the antenna length (L) is straightforward. A longer antenna length will radiate better at lower frequencies. However, physical size restrictions/requirements must be kept in mind in determining the antenna length. Finally, a larger α value (>120°) is recommended to avoid unnecessary reflections from the electric monopole.

(F) From a thorough tradespace study, the aperture size of the Koshelev antenna (single element) is determined to be 90 mm × 100 mm in order to achieve desired antenna metrics performance proposed in the milestone.

(G) The physical aperture area of the Koshelev array antenna largely depends on the interelement spacing and the shape of the array. We were able to determine that the diamond topology is the optimum shape for the Koshelev array antenna. From the initial tradespace study of interelement spacing, we were able to observe that a particular value of pulse duration is optimal to feed into the diamond Koshelev array for maximum radiation. Pulse duration slightly shorter or longer would be inefficient. Moreover, with the diamond Koshelev array, by making only element#3 passive we were able to obtain similar gain characteristics as a function of elevation angle as the all elements active.

6.2.4.2 Since Last Report

(G)

- The element spacing in the time domain is determined by the pulse duration, which is given by the following equation:

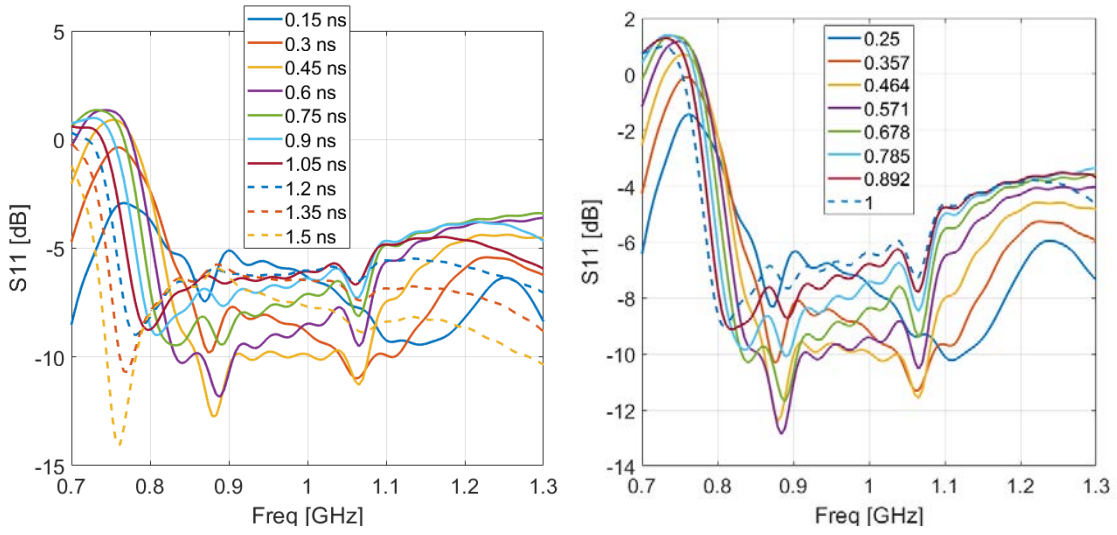
$$S_x = S_y = K\tau_p c_0 \quad (1)$$

where S_x & S_y are the interelement spacing variables in the x-axis and y-axis. In (1), K is a numeric constant, τ_p is the pulse duration, and c_0 is the speed of light in m/s. For the first study, we chose the value of K=0.5 and varied τ_p from 0.15 ns to 1.5 ns. For the second study, we picked the optimum τ_p value from the first test and varied the value of K from 0.25 to 1. An optimum K has also been identified. The criteria for optimum output is set when the reflection coefficient (S11) output metric stays around or below the –10 dB line over as wide a bandwidth as possible centered around 900 MHz.

  We performed the active-passive combination study on the diamond Koshelev array topology with the optimum τ_p and K values. Four cases were chosen to execute this study and they can be found in Fig. 6.2.1. In Fig. 6.2.1, the elements are numbered

from 1 to 5, where pink indicates the element is active and blue indicates the element is passive.

- As mentioned, the first study focused on varying the pulse duration by keeping other parameters constant. Fig. 6.2.2(a) shows the reflection coefficient or S11 (scattering parameter at input port of the Koshelev antenna) in dB over the desired frequency range for a range of pulse duration values from 0.15 ns to 1.5 ns. By closely observing the results in Fig. 6.2.2(a), we can say that for this particular aperture area of the Koshelev antenna element, a pulse duration of around 0.45 ns would be the optimum. A shorter or longer pulse duration would be inefficient. A longer pulse duration signal might radiate effectively at much lower frequencies and not at the desired frequency range. Similarly, a shorter pulse duration signal could produce a higher bandwidth, which is achieved by increasing the aperture area of the Koshelev antenan. By using this optimum pulse duration, the numeric constant variable, K has been varied over the range 0.25 to 1. Theory suggests that a value around 0.5 is the optimum, however this can change depending on the antenna element. Fig. 6.2.2(b) shows that a value of 0.464 is the optimum with extreme end values of the range performing worse.

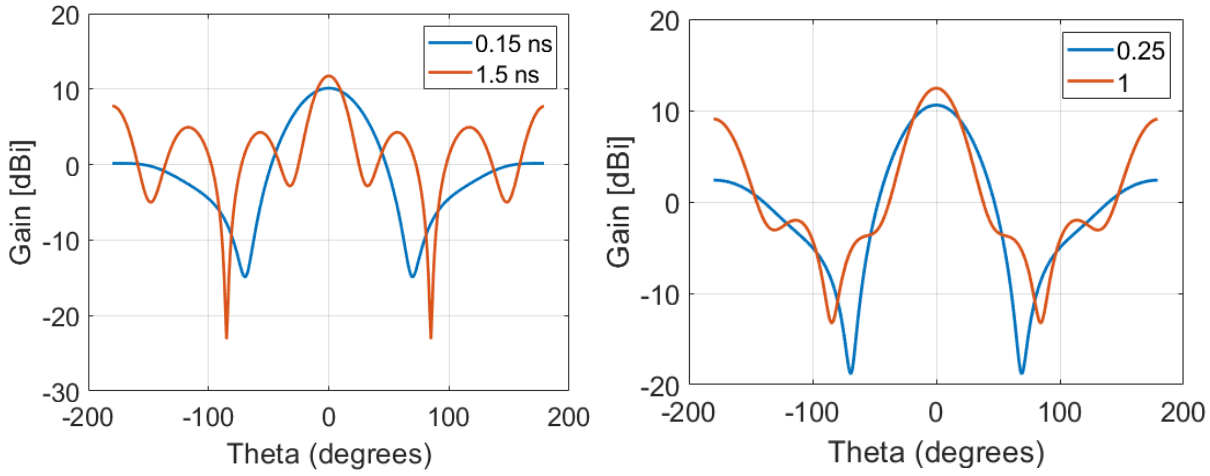


(a) (b)

Fig. 6.2.2. (a) S11 of center element (#3) of diamond Koshelev array over the desired frequency range for different pulse duration values, and (b) S11 of center element (#3) of diamond Koshelev array over the desired frequency range for different K values.

- Moving forward, the gain as a function of elevation angle (θ) has been plotted in Fig. 6.2.3(a) for two values of pulse duration. A pulse with shorter duration than desired yields lower gain at 900 MHz, while a pulse with longer duration than desired yields higher gain at 900 MHz. However, the longer duration pulses have shown worse S11 performance therefore an optimum must be looked for a certain aperture area to radiate effectively with highest gain possible at 900 MHz. Similarly, Fig. 6.2.3(b) carries the same analysis i.e., an intermediate value of K just below 0.5 would be the optimum value. This optimum value of K will be verified and confirmed by extending

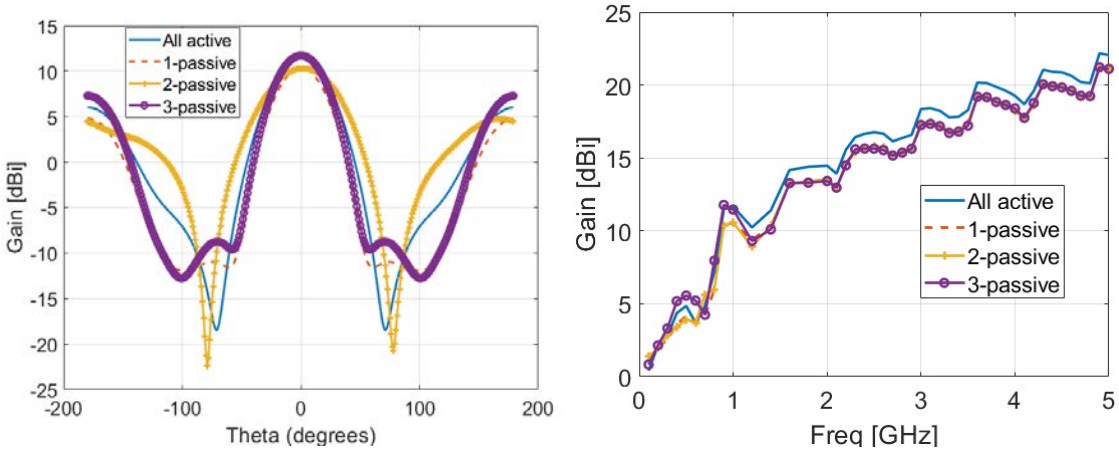
the study to other Koshelev array antenna topologies such as hexagon, octagon, and ellipse which are reported in May 21 MSR.



(a) (b)

Fig. 6.2.3. (a) Gain as a function of elevation angle (θ) for diamond Koshelev array antenna for two pulse duration values at 900 MHz, and (b) Gain as a function of elevation angle (θ) for diamond Koshelev array antenna for two K values at 900 MHz.

- Based on the optimal values obtained from the above studies, four different combinations of active and passive elements have been considered, which are shown in Fig. 6.2.1. In Fig. 6.2.4, the solid blue curve is the case when all elements are excited. Similarly, in Fig. 6.2.4, the dotted red curve indicates element#1 is passive, pointed yellow curve indicates element#2 is passive and pointed purple curve indicates element#3 is passive, while other elements remain active. Several observations can be made from reviewing Fig. 6.2.4(a). First, all elements active, element#1 passive and element#3 passive produced same peak gain value (around 11.73 dBi) at boresight with similar half-power beamwidth value (around 40°). Second, the element#2 passive acted as a unique case which produced lower gain value. This indicates that by carefully switching off input power to a certain element and redirecting it to other elements, the peak gain and beamwidth can be controlled or adjusted. Third, the first null from all elements active and element#2 passive are similar whereas the first null from element#1 passive and element#3 passive appeared at much higher dBi value.
- To understand the impact of switching elements to active and passive at different frequencies, the peak gain is plotted as a function of frequency in Fig. 6.2.4(b). At higher frequencies (> 1.5 GHz), all elements active clearly shows higher gain than other three cases. However, at lower frequencies (< 1.5 GHz), element#3 passive produced slightly higher gain than other three cases, especially at 900 MHz. It is important to understand why this particular case (element#3 passive) has produced higher peak gain than all elements active. More in-depth investigations will be carried out to find answers pertaining to previous statement.



(a) (b)

Fig. 6.2.4. (a) Gain as a function of elevation angle (θ), and (b) Gain as a function of frequency.

6.2.5 References

[1] Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

6.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna

(Sadie Brasel and Kalyan Durbhakula)

6.3.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of Shark antenna elements whose miniaturization in two dimensions (height and width equal to $\lambda/4$ where λ corresponds to the lowest operating frequency) make it a good candidate for UWB HPM systems while having a reduced aperture area with respect to the current state-of-the-art. In the literature, the Shark antenna has already been shown to achieve a wide 20:1 impedance bandwidth, low dispersion, and a sectoral (also referred to as directional) radiation pattern.

Sub-Problem: The design parameter space of the Shark antenna has not been studied rigorously in the literature and therefore the effect of these parameters on the antenna metrics is not understood. In addition, the Shark antenna has been shown to be not very directive in the H-Plane. Preliminary studies have shown that aperture efficiencies at low frequencies are much better than at higher frequencies.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Explore the design parameter space for the Shark antenna element using computational electromagnetic (EM) wave solvers starting with the simulation and validation of a single element.

Relevance to OSPRES Grant Objective: The Shark antenna dimensions were established to be frequency dependent and can be readily modulated to fit the spectrum characteristics of an ultra-fast rise time input pulse.

Risks, Payoffs and Challenges:

(i) The Shark antenna is comprised of flare-angle-dependent bicones that are truncated in the azimuthal angle. This still yields considerably higher half power beam width (HPBW) than other antenna elements under investigation. The significant reduction of HPBW in the H-plane may be unattainable and can be considered a major risk.

(ii) Payoffs include the development of a library of antenna metrics data for various shapes and sizes of the bicones and reflector plates in the shark antenna.

(iii) Computational challenges remain present with respect to automation of design parameter space on our currently used supercomputer (LEWIS). Design challenges persist in obtaining lower operating frequencies while not increasing the height of the antenna and surpassing the 90 mm × 90 mm size requirement.

6.3.2 Tasks and Milestones / Timeline / Status

(A) Complete initial design, simulation, and validation of the Shark antenna / JAN21 / Complete.

(B) Validate Shark antenna design using the LEWIS supercomputer over a wider range of frequency results (up to 20 GHz) / FEB–MAR21 / Complete.

(C) Identify Shark antenna design parameters which contribute significantly to bandwidth, gain, and physical aperture area. Determine which parameters contribute most to performance improvement/size reduction/ FEB–MAR21 / Complete.

(D) Perform a tradespace study by simulating the Shark antenna with varying cases of flare angle, cone length, and distance to backplane. Gain a general understanding of how these parameters affect impedance bandwidth, rE/V, gain and HPBW / FEB–MAY21 / Complete.

- Milestone: produce a detailed summary of change in impedance bandwidth, rE/V, HPBW in H-plane and E-plane as a function of flare angle (α), cone height (*h*), and distance to backplane (*d*) / Complete.

- Milestone: Choose optimal Shark antenna design based on tradespace study / Complete.

(E) Using the optimal Shark antenna design in (D), simulate various array geometries including hexagonal, rectangular, and circular arrays. Determine which array geometries are optimal and analyze aperture fields and aperture efficiencies. / MAY–JULY21 / Ongoing.

- Milestone: produce a report which states the effects of array geometries for the Shark antenna. Consider the impedance bandwidth, max gain, directivity, and aperture efficiency of each array.

(F) Begin prototyping and validation of optimal Shark antenna single element. / JUN–JUL21 / Ongoing.

- Milestone: have a finished Shark antenna prototype. Compare S11 and radiation pattern with simulated Shark antenna.

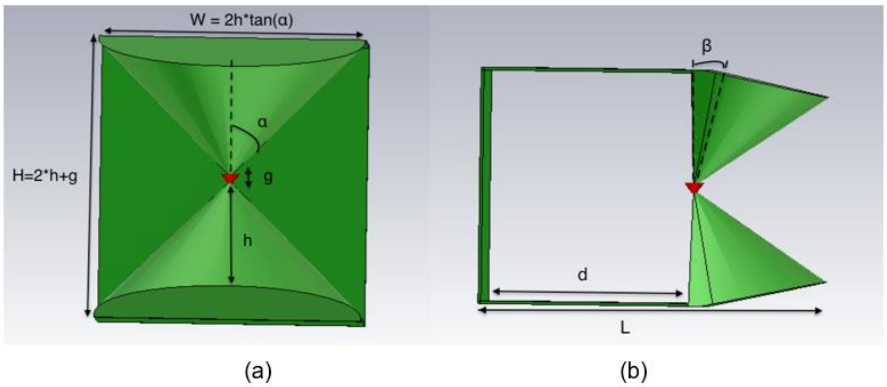


Figure 6.3.1. Shark antenna design parameters: *d, h, g,* α*,* β*.*

6.3.3 Progress Made Since Last Report

(E) An elliptical Shark antenna array has been simulated. Additional metrics have been noted for all of the array geometries, including aperture efficiency and rE/V.

(F) A finalized Shark antenna design has been selected for fabrication so that it is compatible with 50 Ω cables and connectors. A fabrication method has been selected and is underway.

6.3.4 Significant Finding(s) and Mission Impact

6.3.4.1 Summary to Date

(A-B) The Shark antenna has been designed, simulated, and validated according to [1]. (Figure 6.3.1)

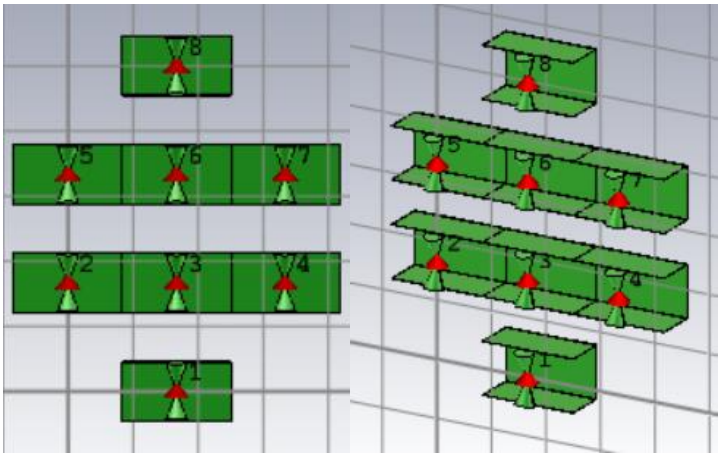
(C) The Shark antenna design parameters that have been found to contribute significantly to bandwidth performance, directivity, and gain are the cone height (*h*) and distance to backplane (*d*).

(D) The Shark antenna tradespace study has been completed and has provided insight into the Shark antenna design space. Increasing the cone height *h* yields better impedance bandwidth at low frequencies and is more directive in the *e* and *h* planes. However, increasing *h* results in a larger aperture area. To remain within 90 x 90 mm, the maximum *h* value is 45 mm; with this a lowest operating frequency of 815 MHz is achievable.

(E) Square and hexagon Shark arrays have been simulated in CST. The square array was simulated with and without connected ground planes to study how this affects performance. The approach of connected ground plane for the square Shark array improves the gain by 1 dBi over unconnected ground plane. The 1 dBi improvement from 11.6 dBi to 12.7 dBi is a decent improvement, therefore connected ground plane arrays are used moving forward.

6.3.4.2 Since Last Report

(E) An 8 element elliptical Shark antenna array has been simulated in CST as shown in Figure 6.3.2. Figure 6.3.3 shows the reflection coefficients of each element compared to that of a single element. Elements 8 and 1 are fairly well matched to the single element reflection coefficient, elements 2 – 7 however have worse reflection coefficients as they are in the center of the array and experience more interference from adjacent Shark antennas. Figure 6.3.4 shows the max gain over frequency for each array geometry. The square array has a 1dBi increase of gain over the entire frequency range as it has one more antenna element compared to the elliptical and hexagonal arrays.



(a) (b)

Figure 6.3.2. 8 element elliptical Shark antenna array (a) front view (b) orthographic view.

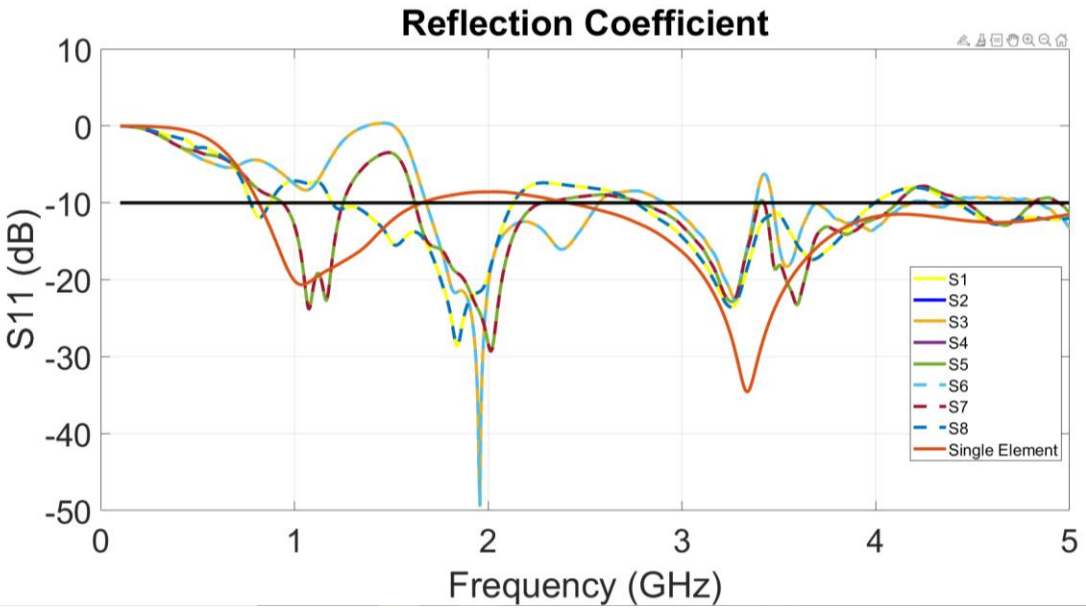


Figure 6.3.3: Reflection coefficient of elliptical array.

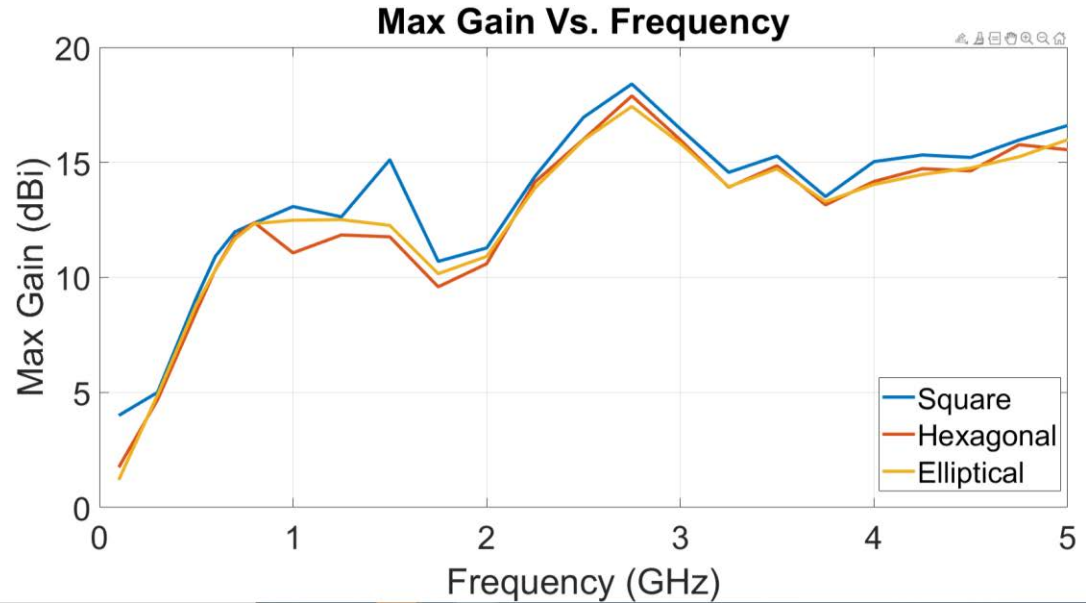


Figure 6.3.4: Max gain vs. frequency.

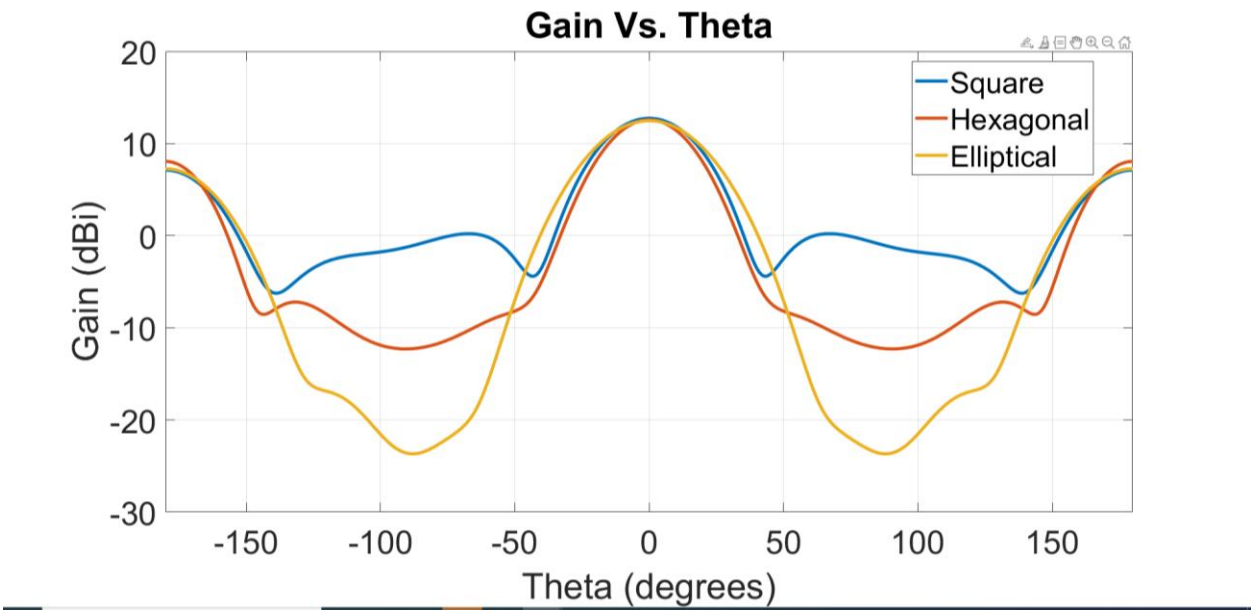


Figure 6.3.5: 900 MHz radiation patterns (phi = 0°).

Table 6.3.1: Performance comparison of Shark array geometries.

Geometry	# of Elements	Max Gain (900MHz) (dBi)	Aperture Efficiency (%)	rE/V (1m)	rE/V (2m)	Beamwidth (°)	Sidelobes (dB)
square	9	12.719	53.13	8.91	9.25	36.2	-5.6
hexagon	8	11.728	52.38	7.98	8.21	32.4	-4.5
ellipse	8	12.408	52.3	7.86	8.13	40.4	-5.2

(E) The elliptical Shark antenna array has a similar shape and size as the hexagonal array but performs slightly worse in terms of the beamwidth and rE/V according to Table 6.3.1. The hexagonal array has the most directive radiation pattern with the smallest beamwidth and sidelobe level. The sidelobe metric shown in Table 6.3.1 is actually a measurement of the back lobe levels due to the way CST calculates this metric. A better illustration of sidelobe levels can be seen in Figure 6.3.5 around theta = 90°. Figure 6.3.5 shows that the elliptical array has the lowest sidelobe levels while maintaining the same peak gain.

Overall, the three array configurations have worse aperture efficiency compared to that of the single Shark antenna element which was shown to have aperture efficiencies exceeding 100% in previous MSRs. The 50% decrease in aperture efficiency in the transition from single element to array is due to destructive interference between adjacent elements in the antenna array. To accommodate for this moving forward more novel array geometries will be implemented.

(F) The shark prototype design has been adjusted such that it is compatible with a 50 Ω measurement device and cabling. To do this the flare angle (α) and cone height (h) were increased to 70° and 75 mm respectively. To fabricate the Shark antenna, the top and bottom cone will be 3D printed separately, the backplane of the antenna will be constructed by folding sheet metal and will then be attached to the cones. A 50 Ω coaxial

cable will then be fed through the bottom cone where the outer conductor will be attached, the inner conductor will then be attached to the top cone.

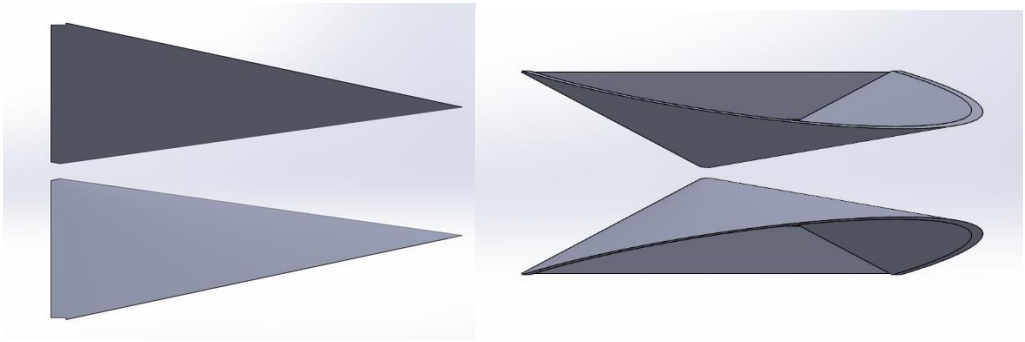


Figure 5.3.6: Shark antenna cone Solidworks model (a) side view (b) orthographic view.

6.3.5 References:

[1] L. Desrumaux, A. Godard, M. Lalande, V. Bertrand, J. Andrieu and B. Jecko, "An Original Antenna for Transient High Power UWB Arrays: The Shark Antenna," in IEEE Transactions on Antennas and Propagation, vol. 58, no. 8, pp. 2515- 2522, Aug. 2010, doi: 10.1109/TAP.2010.2050418.

6.4 Tradespace Analysis of Ultra-Wide-Band (UWB) Fractal Antenna

(Sai Indharapu and Kalyan Durbhakula)

6.4.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. The fractal antenna packs multiple resonances closely spaced together to generate an UWB response, thereby effectively utilizing the 2D space (i.e., the radiating patch space). Its high degree of freedom provides an opportunity to develop systematically modified patch shapes, which in turn leads to improved bandwidth while retaining high fidelity factor values.

Sub-Problem: Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

6.4.2 Tasks and Milestones / Timeline / Status

(A) Perform tradespace analysis of the fractal element radius *b* over the desired frequency range (4 GHz to 12 GHz) using the genetic algorithm (GA) optimization tool available in the commercial electromagnetic (EM) solver FEKO / FEB21 / Complete.

- Milestone: Provide a recommendation of an optimum value of *b* using OPTFEKO to minimize reflection coefficient or S11 (< –10 dB).

(B) Perform tradespace study on different fractal shapes by changing the number of fractal segments to understand the number of segment effect on the impedance bandwidth / FEB21 / Complete.

- Milestone: Produce a detailed study of the antenna response such as S11, gain, and bandwidth by varying the number fractal segments.

(C) Apply the GA optimization tool on the fractal side length *b* over a wide frequency range (2 GHz to 12 GHz with 201 discrete frequency points) and number of fractal segments using OPTFEKO on the LEWIS cluster / MAR21 / Complete.

- Milestone: Reduce physical aperture area by 10% of its present design, reported in the FEB MSR, and demonstrate minimal or no change in S11, gain, and fidelity factor values.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a* / MAR–APR21 / Complete.

- Milestone: Recommend a value of *a* to reduce the physical aperture area and increase aperture efficiency (>50%) with no variation in other antenna metrics.

(E) Frequency scale fractal antenna design such that the center frequency of the resulting antenna equals 1.3 GHz / MAY21 / Complete.

- Milestone: Modify antenna design with a center frequency equal to 1.3 GHz and achieve similar results (3:1 bandwidth at fc = 1.3 GHz, 3 dBi gain and >130% aperture efficiency at 900 MHz) to antenna design at center frequency ~7 GHz.

(F) Design and simulate various array antenna geometries composed of optimized fractal antenna elements (obtained from (E)) to analyze the effect of overall array antenna geometry on the desired array antenna response metrics (i.e., gain vs. frequency, gain vs. elevation angle at constant phi, rE/V, half-power beamwidth and side-lobe level.) / MAY–JUL21 / Ongoing

- Milestone: Recommend a best possible structure with reduced aperture area and minimal loss in gain.

(G) Apply machine learning (ML) models available in Altair Hyperstudy (2021) on fractal antenna element to try and understand the possibilities and limitations of ML models for fast and efficient antenna metrics (S11) prediction and optimization. Through successful testing, a ML model can replace conventional EM simulators for faster optimization and easy prediction. / MAY–OCT21 / Ongoing.

- Milestone: Recommend most accurate and efficient ML model available in Altair Hyperstudy (2021) for array antenna metrics prediction.

6.4.3 Progress Made Since Last Report

(F) Tradespace analysis of the fractal antenna array has been carried out over the range 75 mm to 145 mm for both square (3x3) and diamond (2x2) lattices. The interelement spacing for each of the array topologies has been modified to investigate changes in antenna response, such as gain as a function of theta and gain as a function of frequency.

(G) ML models have shown promising results in predicting S11 response for the fractal antenna. Therefore, we extended the application of ML models on fractal antenna for prediction of gain as a function of frequency.

(G1) Specific ML algorithms such as radial basis function (RBF) and least square regression (LSR) models were selected to extend the prediction capability to the antenna gain metric.

(G2) The gain response from the EM simulator (FEKO) was plotted against the output response from the two aforementioned ML algorithms to test the accuracy of the ML models.

6.4.4 Significant Finding(s) and Mission Impact

6.4.4.1 Summary to Date

(A) The initial analysis of the simulation results with fractal radius *b* equal to 1.8 mm yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO has been used as an optimization tool with fractal radius *b* as the optimization variable. The optimum value for *b* is found to be 1.66 mm. A comparison between reflection coefficient for initial *b* (= 1.8 mm) value and the optimized *b* (= 1.66 mm) can be found in Figure. 6.4.1. The optimization is carried out over 51 discrete frequency points.

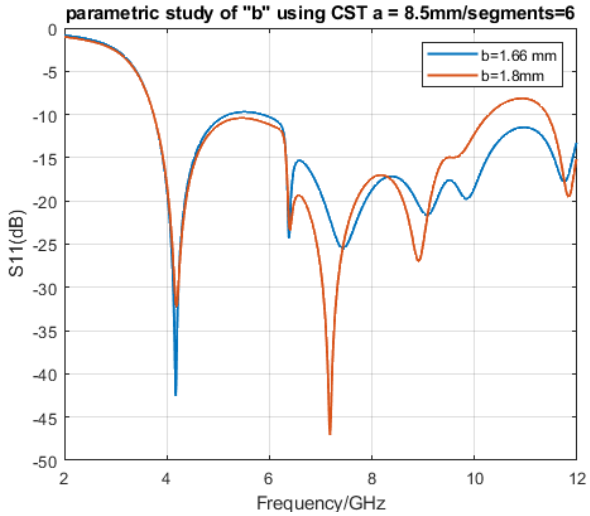


Figure 6.4.1 Reflection coefficient of fractal antenna for initial and optimized *b* value.

(B) The addition of fractal elements (*N*) to the simple hexagon improved antenna metrics such as S11. To further investigate and understand the fractal elements, the number of segments in the fractal geometry has been varied. The improvement in bandwidth is observed as the value of *N* is increased from 6 to 14.

(C) The initial optimum value of *b* over 51 discrete frequency points is reported as 1.66 mm in task (A). To further increase the accuracy of the optimization algorithm and to find a more precise value for *b*, optimization is further performed over wider frequency points (201 discrete points between 2 GHz to 12 GHz).

(D) The hexagonal patch radius *a* has a significant effect on the physical aperture area of the antenna. Therefore, Altair OPTFEKO has been utilized to find an optimum *a* value, which was found to be 8 mm over the range 7.2 mm to 9 mm. Antenna metrics such as S11, gain, and bandwidth have shown desired performance with the optimized *a* value.

(E) The initial antenna design has been modified to achieve a center frequency of ~1.3 GHz. The gain value at 900 MHz is 3.5 dBi and were able to achieve an impedance

bandwidth ratio of 3.3:1.The designed antenna has been fabricated and tested, and the S11 response of the fabricated antenna agrees well when compared against FEKO, CST.

(F) The tradespace analysis of two different array lattices has been carried out. The aperture area of antenna array with diamond lattice is 135.6 mm^2. The aperture area of antenna array with square lattice is 366 mm2. Diamond lattice has 5 antenna elements, whereas square lattice has 9 elements. The interelement spacing between each antenna element has been varied from 75 mm to 115 mm with a step size of 10 mm.

(G) The initial prediction of reflection coefficient (S11) from the three ML models were satisfactory and have shown a good agreement against FEKO output for the same antenna design. In addition, radial basis function (RBF) and least square regression (LSR) were down selected from the initial three ML models. To further analyze, each ML model has been trained with 4 different sizes of training data (i.e. 5, 10,15 and 20).

6.4.4.2 Since Last Report

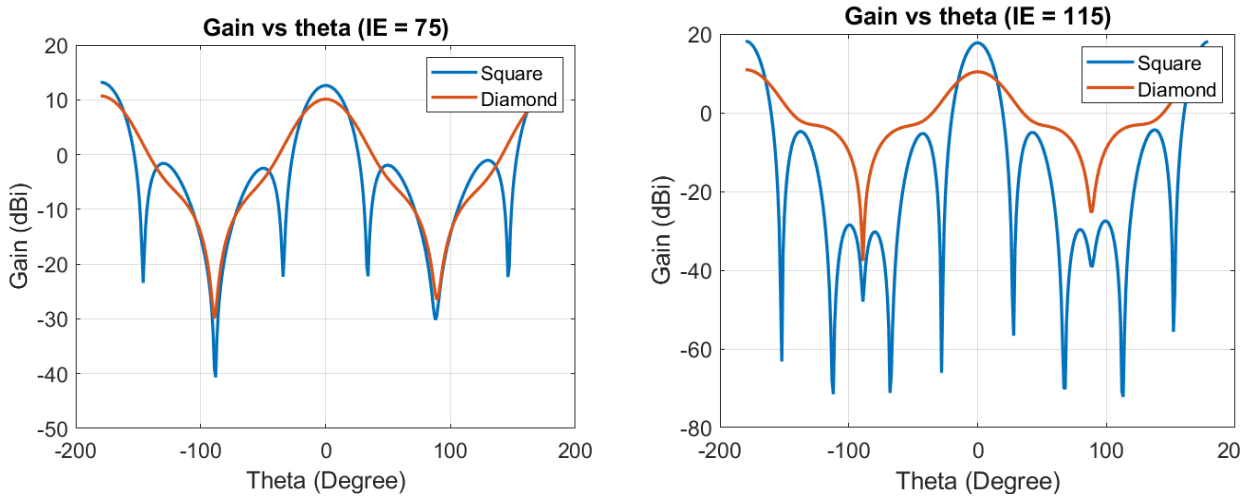
(F) The interelement spacing between antenna elements in an array has shown a significant impact on antenna response metrics such as gain and HPBW. The diamond lattice simulations of gain at 900 MHz for different interelement spacing values have shown no significant change. Table 6.4.1 shows a comparison of peak gain at 900 MHz between square lattice and diamond lattice for different interelement spacing values.

Table 6.4.1 Gain Comparison of different antenna array lattices with different interelement spacing values.

Interelement spacing (mm)	Peak Gain in dBi at 900 MHz	
	Square lattice	Diamond lattice
75	13.2026	10.7189
85	13.6177	10.8343
95	14.0174	10.9108
105	14.3750	10.9441
115	14.6578	10.9337
125	14.8261	10.8784
135	14.8441	10.7792
145	14.6933	10.6373

Figure 6.4.2 illustrates the comparison gain as a function of theta (in degrees) over a range of –180 to 180° of both antenna arrays (i.e., square lattice and diamond lattice).

Gain at θ = 0 is close to 20 dBi when interelement spacing is 115 mm for square lattice with no major decrease in sidelobes levels. Diamond lattice have no significant change in gain with change in interelement spacing. The interelement spacing is set to be 115 mm for further studies.



(a) (b)

Figure 6.4.2: Gain vs Theta for two square and diamond antenna array lattices (a) Interelement spacing = 75 mm (b) Interelement spacing = 115 mm.

(G) RBF and LSR which were previously used for predicting S11 response are also being utilized to predict antenna gain. The fractal antenna hexagon patch radius *a* and fractal side length *b* are used for generating the training data set. In this case, the output is the antenna gain, which has been simulated at 30 discrete frequency points over the frequency range from 100 MHz to 3 GHz. The gain values are collected from the *.out (FEKO) file as shown in figure 6.4.3. The highlighted value in Figure 6.4.3 is the directivity in dB, which is 0.29 dB higher than the gain value.

LOCATION		ETHETA		EPHI		directivity in dB			POLARISATION	
THETA	PHI	magn.	phase	magn.	phase	vert.	horiz.	total	axial r.	angle direction
0.00	0.00	1.075E-06	-75.01	6.273E-03	0.97	-73.5918	1.7308	1.7308	0.0002	90.00 LINEAR

Figure 6.4.3: Snapshot from *.out file

The gain values obtained from the RBF and LSR ML models are plotted against the output from FEKO as shown in Figure 6.4.4. The agreement between ML model and FEKO is not satisfactory at higher frequencies, which can be observed from Figure 6.4.4. Training data for these models have gain (dBi) values in the output data which include both positive and negative values. With our current setup, the Altair hyperstudy is failing to recognize negative values from the .out file. As a result, ML models in Altair hyperstudy partly failed to predict negative values of gain (in dBi). which is illustrated in Figure 6.4.4. , . We are working on modifying our current setup to ensure that the training data from .out file contain negative values of gain (in dBi). Alternatively, we also plan to train all ML models using training data whose values are in linear scale.

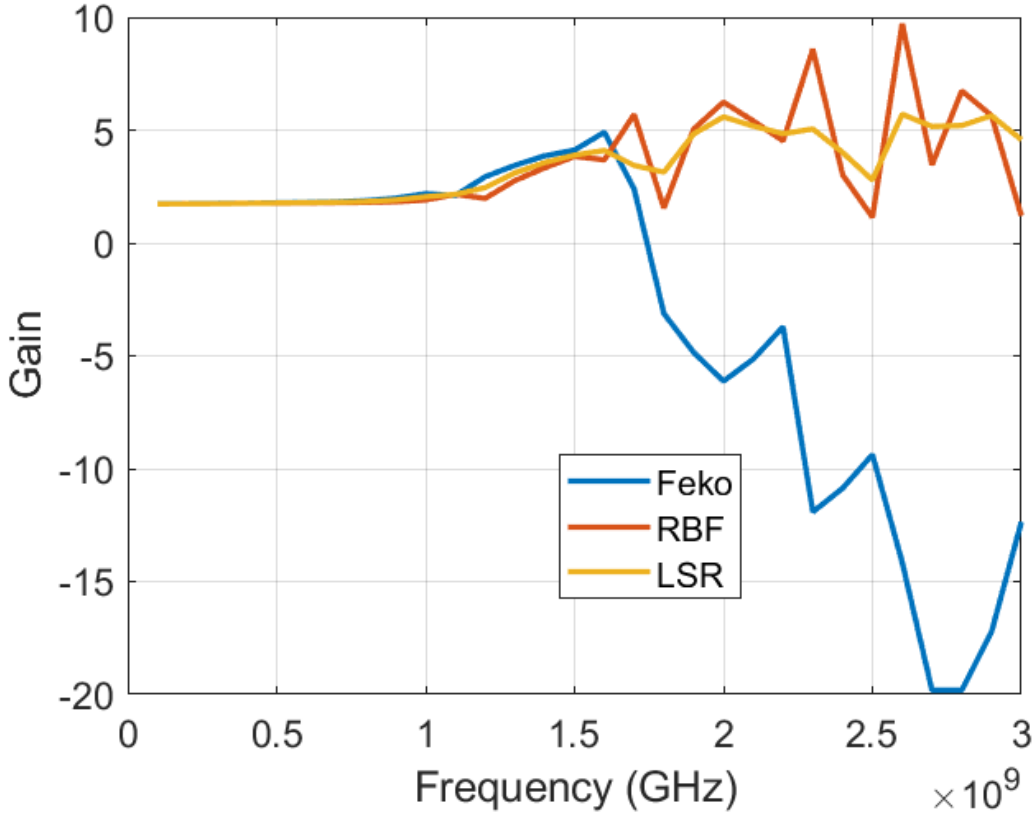


Figure 6.4.4: Gain (dBi) comparison of FEKO with radial basis function (RBF), least square regression (LSR).

6.4.5 References

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

7.0 RF Coupling

7.1 Enclosure Effects on RF Coupling

(Mohamed Hamdalla and Ahmed Hassan)

7.1.1 Problem Statement, Approach, and Context

Primary Problem: UAVs are typically considered metallic/dielectric enclosures depending on their frame material. The shielding effectiveness of such enclosures might be compromised due to the slots and gaps on these enclosures, creating upset susceptibility to the enclosed electronics. The goal of this work is to quantify how the thresholds for upset susceptibility of enclosed wires and integrated circuits differ from those in free space.

Solution Space: Study enclosures with different shapes, material compositions, and slots to quantify their effect on RF coupling to the enclosed wires and electronics typically used in UAVs. The study will focus on the low-frequency range where the incident wavelength is comparable to the size of the enclosure or larger.

Sub-Problem: UAVs are manufactured with a wide variety of shapes and composites to accomplish an exponentially expanding list of missions. The configurations previously reported in the literature have simplistic assumptions regarding the shape and material composition of UAV enclosures that might overestimate or underestimate susceptibility.

State-of-the-Art (SOTA): Simple statistical analysis of specific enclosure configurations using either brute force simulations/measurements or pure statistical methods. Also, simplified UAV wire distributions are assumed.

Deficiency in the SOTA: Brute force simulations/measurements of the voltages and currents induced in wires and integrated circuits contained in enclosures are computationally or experimentally complex and have several limitations. The computations are complicated by the multiscale nature of the simulations, and the experiments are complicated by the cost of the equipment and the extensive time needed to measure every variation to cover all possible scenarios. Statistical methods, such as the Random Coupling Model (RCM) for example [1], are only accurate for high frequencies where the wavelength is much smaller than the size of the enclosure. Another main deficiency of the RCM is that it can't predict the exact induced voltages and currents for a specific well-characterized system but it only provides the statistical properties of these induced currents and voltages.

Solution Proposed: Apply Characteristic Mode Analysis (CMA) to identify the fundamental modes of the enclosure, current distribution, and the field pattern of each mode. This will allow us to predict the worst-case RF coupling scenarios without the need for lengthy simulations and/or expensive experimental measurements. The proposed approach can predict measurements at a fraction of the cost/time. Moreover, we propose to study RF coupling to realistic UAV wire distributions, experimentally reconstructed, when they are placed inside metallic/dielectric UAV enclosures.

Relevance to OSPRES Grant Objective: Provide general guidelines on how the environment, in this case, the enclosure, affects RF coupling and subsequent electromagnetic absorption to UAV wires and integrated circuits.

Risks, Payoffs, and Challenges: The modes depend mainly on the shape and material of the enclosure. Since UAVs have a wide variety of shapes and material compositions, a library of several UAVs needs to be studied before general quantitative conclusions can be drawn. Challenges can be mitigated by the use of the classification techniques of Machine Learning (ML). That is, different ML techniques will be evoked to detect hidden patterns on how the shape, material composition, and the shape/size location of slots correlate with the field enhancement inside the enclosure.

7.1.2 Tasks and Milestones / Timeline / Status

A. Complete the CMA implementation for studying the shielding effectiveness of metallic enclosures. Validate whether CMA can predict the worst-case shielding effectiveness of metallic enclosures as a function of their shapes. / JAN21 / Complete.

   A1. Prepare a manuscript for IEEE AWPL to document the progress done in A. / Ongoing.

B. Use CMA tool in (A) to predict the worst-case internal field magnitude of metallic and dielectric enclosures of ten COTS UAVs as a function of HPM waveform. / MAY21 / Ongoing.

C. Use the database in (B) to train a Machine Learning (ML) platform to predict RF coupling to enclosed wires and electronics. / OCT21 / Ongoing.

D. Progressively build an accurate representation of the UAV wiring system with all of the integrated circuit (ICs) and electronics to test assist the predictions of (c) and the experimental measurement of the actual UAV. / JUL21 / ongoing.

E. Address the 2021 UAV's semi-annual review recommendations to study arbitrarily shaped UAV wire distribution. / JUNE21 / Complete.

7.1.3 Progress Made Since Last Report

E1. The effect of the shape of the UAV wiring system is studied.

   E1.1. Each of the 12 wires of the UAV model in Fig. 7.1c is divided into 5 segments, and each segment is rotated with a random angle to create a random wire configuration. The rotation angles of the segments were chosen to maintain a practical representation of the wires above the quadcopter's frame. The rotation angles are in the plane of the UAV, thus, no variations in the wire's heights were studied since we assume that these wires are mounted on top of the frame with minimal height variations. Ten different wire configurations were studied in this analysis. Two of these wire configurations are illustrated in Fig. 7.2a. Each wire configuration is excited by 325 incident angles with 2 different polarizations.

Therefore, a total of 650 different incident excitations were studied: 2 polarizations, $0^\circ<\theta<180^\circ$ with 15° increment, and $0^\circ<\varphi<360^\circ$ with 15° increment.

7.1.4 Significant Finding(s) and Mission Impact

7.1.4.1 Summary to Date

A1. A fast full-wave tool that facilitates studying the effect of a metallic enclosure on shielding effectiveness has been developed Using CMA.

7.1.4.2 Since Last Report

a. Figure 7.2a illustrates two configurations, out of ten, of the UAV wires. The coupled voltage to the load of interest was averaged over the ten different configurations and the 650 different angles of incidence and plotted in dashed red in Fig. 7.2b. The blue curve in Fig. 7.2b shows the voltage calculated at the load of interest using the UAV model in Fig. 7.1c with no shape variations. Fig. 7.2c shows the percentage difference between the reference coupled voltage and the average coupled voltage calculated from the ten different wiring configurations. Fig. 7.2 shows that for low frequencies, up to 1 GHz, the shape variations in the wires have a small effect on the coupled voltage (less than 50%). For frequencies higher than 1 GHz, the shape variations in the UAV wires start to significantly affect the coupled voltage, leading to significant deviations from the reference coupled voltage as shown in Fig. 7.2c. The analysis in Fig. 7.2, identifies for an sUAV wire system, with realistic dimensions and distributions, the frequency range where the variations in wire shapes have a negligible effect on coupling and the frequency range where they must be taken into consideration.

Table 7.1. Quadcopter's main circuitry components and wires.

Part function	***Part #***	***Specs.***	***Length***
motor feed lines	1	18 AWG	
ESC out power lines	2	16 AWG	
ESC in power lines	3	16 AWG	~20 cm
esc in signal	4	22 AWG	25 cm
battery out	5	14 AWG	
battery to controller	6	22 AWG	
main controller (autopilot)	7		carrier board 9.5 cm x 4.5 cm
GP.1575.25.4.A.02 GPS/Galileo 25*25*4mm 1575.42MHz Patch Antenna2	8	22 AWG	~20 cm
Readytosky® 2212 920KV Brushless Motors	9		
SimonK 30A ESC Brushless Speed Controller	10		
Pixhawk Power Module 5.3V BEC XT60	11		

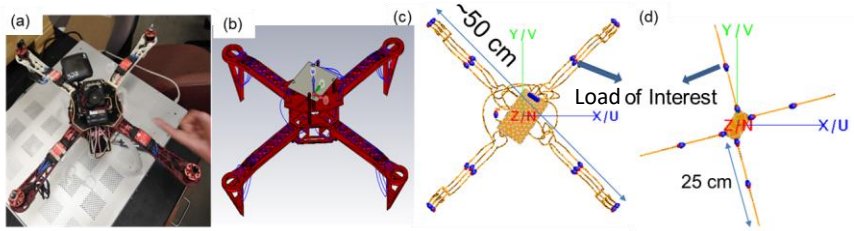


Fig. 7.1. (a) Model of the realistic UAV circuitry showing the wires, components, and frame, (b) the UAV wiring diagram showing all the wires and components, (c) the CST MWS model of the UAV in (a) and (b), (d) the simplified model of the UAV in (a) and (b).

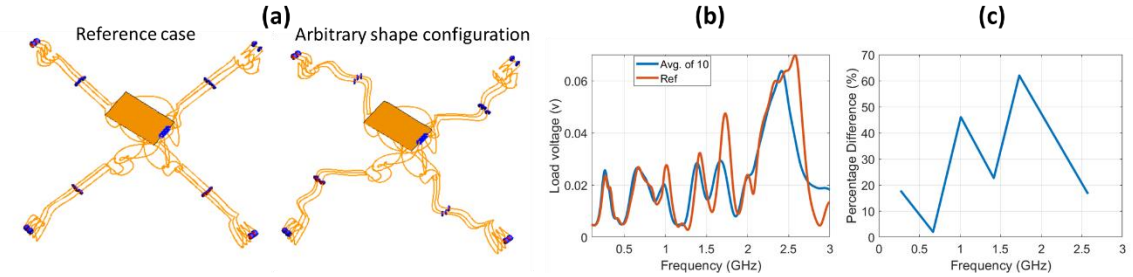


Fig. 7.2. (a) Sketch of the proposed arbitrary wired UAV representation showing two cases, one with straight wires and another with arbitrarily shaped wires on one of its arms (b) the coupled voltage to a load of interest averaged over 10 different wire configurations of the model in (a). (c) percentage difference of the peak's magnitudes.

8.0 Laser Development

8.1 Fiber Lasers and Optical Amplifiers

(Heather Thompson and Scott Shepard)

8.1.1 Problem Statement, Approach, and Context

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$50K to \$5M.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution. This way of implementing an optical fiber laser (via an optical fiber amplifier) has SWaP advantages with respect to traditional (fiber and free-space) laser designs.

Sub-Problem (1): Optical pump power system costs are the dominant source of costs (in both normal/free-space lasers and in optical fiber lasers, of this class).

Sub-Problem (2): Amplified spontaneous emission (ASE) and fiber nonlinearities impede the optical amplifier performance.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive until reduced by a factor of two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping scheme which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments we are pursuing the use of gain saturation and a staged design of different fiber diameters.

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system needed to drive the PCSS will meet the modular and scalable volume and cost aim-points.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability.

8.1.2 Tasks and Milestones / Timeline / Status

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Ongoing.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Ongoing.

(E) Demonstrate a cost-reduced fiber laser. / Ongoing.

(E1) **March 2021** Finalize design. / Complete.
(E2) **April 2021** Assemble and test-check seed LD (laser diode)/driver. / Complete.
(E3) **April 2021** Measure power vs current transfer function of seed LD/driver. / Complete.
(E4) **May–July 2021** Measure ASE and jitter of 1064 nm seed LD/driver. / Ongoing.
(E5) **May–July 2021** Measure ASE and jitter of 1030 nm seed LD/driver. / Ongoing.
(E6) **June-July 2021** Assemble and test-check pump LDs/drivers. / Ongoing.
(E7) **June-July 2021** Measure power vs current transfer function of pump LDs/drivers. / Ongoing.
/ (E8) – (E14) Delayed due to vendor issues (see MAY MSR).
(E8) **September 2021** Splice power combiners to Yb doped preamp fiber.
(E9) **September 2021** Connect seed and pumps to power combiners and test-check.
(E10) **September-October 2021** Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle.
(E11) **September-October 2021** Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle.
(E12) **November 2021** Splice power amplifier and its power combiner to best preamp.
(E13) **November-December 2021** Measure gain, ASE and jitter of entire amp assembly.
(E14) **December 2021** Analyze data and document.

(F) Design a new type of higher power, tubular core, fiber amplifier. / Ongoing.

8.1.3 Progress Made Since Last Report

(F) We submitted an abstract to DEPS 2021: “A Tubular Core Optical Power Amplifier,” highlighting that that the self-focusing of un-guided vs guided modes is dramatically different in its dependence on power; and introducing the advantages of a tubular core. Simulations on the tubular core geometry indicate that we can excite and maintain fundamental mode propagation in either the glass wall or the hollow interior of the tube.

8.1.4 Significant Finding(s) and Mission Impact

8.1.4.1 Summary to Date

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with tolerable pre-burst ASE. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) The design of a proof-of-concept experiment demonstrating a cost-reduced optical pumping scheme was finalized MAR2021.

(F) We made (to our knowledge) the first observation of self-focusing effects that are not determined by beam power alone; which instead can also be controlled via the geometric factors within a waveguide (such as fiber core diameter) MAY2021.

8.1.4.2 Since Last Report

(F) We were surprised to find that we can excite, propagate and maintain a fundamental mode in the hollow interior of the tube, as shown in plots of the z-component electric field and total electric field strength in Figures 8.1.1 (a) and (b) respectively. Hollow-core propagation in photonic crystal fiber is commonplace, but therein the hollow-core is surrounded by complex structures of glass and air which create the photonic bandgap mechanism for wave guidance. In our case we only have a hollow glass tube, hence only two reflecting glass/air interfaces in the transverse dimension. We refer to this as the “air mode” and its existence is significant for the application of power delivery. Very high power can be transferred in this very inexpensive embodiment.

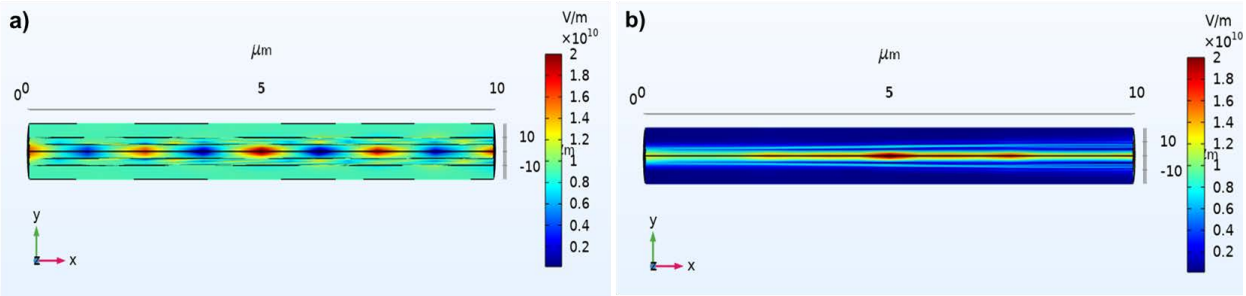


Figure 8.1.1. (a) z-component and **(b)** total E field of air mode in a simple glass tube.

Of course we cannot make an amplifier out of air but if we could get a mode in the glass wall (which has been doped and pumped to form an amplifier) to couple to the air mode then we ought to be able to increase the amplifier’s ability to operate at higher powers. Figure 8.1.2 (a) shows excitation of the glass mode, launched into the wall of the tube; and Figure 8.1.2 (b) shows evidence of the coupling of energy from the glass mode into the air mode (near the center of the tube).

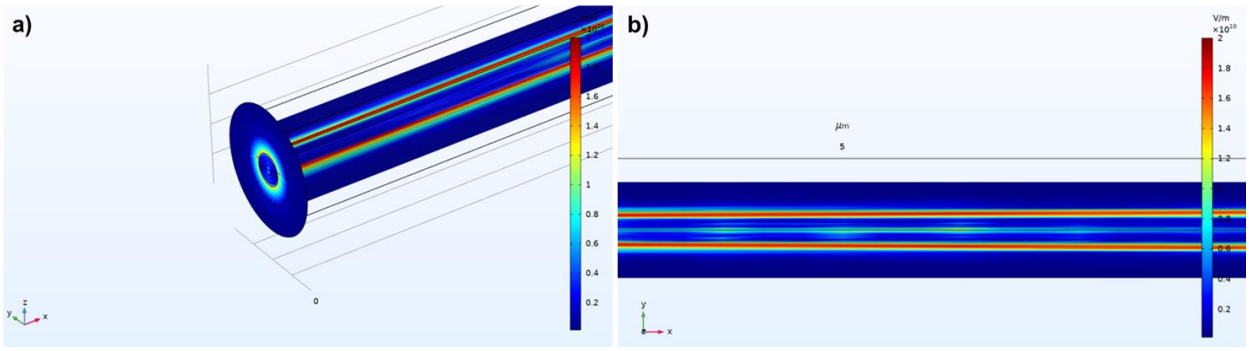


Figure 8.1.2. (a) glass mode launched and **(b)** the growth of an air mode from coupling.

Both the existence of an air mode and our ability to couple energy into it are fortuitous results. Further study is certainly merited due to the significant impacts anticipated for power transfer and optical amplification.

8.2 WBG-PCSS Enabled Laser Diode Array Driver

(John Bhamidipati)

8.2.1 Problem Statement, Approach, and Context

Primary Problem: Need for heavy (~125 lbs.), bulky (~10 cu-ft), and expensive (~$120,000) conventional laser systems (1064 nm) in PCSS-based HPM applications, with an additional need for second and third harmonic generation (SHG/THG) optics to trigger wide bandgap (WBG) solids (GaN/SiC).

Solution Space: Design and implement a compact (~1.1 cu-ft), lightweight (10–15 lbs.), and inexpensive (<$15,000) alternative for conventional high average power optical trigger (laser) system to improve SWaP-C^2 index of HPM systems.

Sub-Problem: Unavailability of commercial-off-the-shelf (COTS) miniature optical sources with sub-nanosecond pulse widths and tens-of-μm beam width, delivering >1-Watt power to implement as a makeshift/turnkey solution for the laser system.

State-of-the-Art (SOTA): High average power picosecond pulsed lasers available up to 50 W output power with a gain factor up to 40 dB (~10,000x power) with laser amplifier.

Deficiency in the SOTA: High average power 1064-nm pulsed lasers are bulky and require auxiliary systems as well as additional optics for SHG/THG generation for WBG device triggering.

Solution Proposed: Multi-stage laser diode array/stack (LDA/LDS) driver powered by seed-laser-diode-driven avalanche WBG-PCSS as a compact, inexpensive laser replacement.

Relevance to OSPRES Grant Objective: Provides an enhanced SWaP-C^2 compliant solution for the laser (optical trigger) subsystem, with a subsequent impact on overall HPM system cost, volume, and power (optical and electrical) requirements.

Risks, Payoffs, and Challenges: Complex interconnect and thermal management system (TMS) design at high temperature (130–175°C) operation; unavailability of COTS high power pulsed laser diodes could potentially raise a need for research in laser diodes (arrays).

8.2.2 Tasks and Milestones / Timeline / Status

(A) Complete initial feasibility study for the cascaded multi-stage optical amplifier design and determine functional requirements for the laser diodes (arrays) and source driver [DEC–JAN 2020 / completed].

(B) Complete initial stage experimental implementation of the PCSS-based driver and demonstrate positive current gain using GaN-PCSS, triggered with a 404 nm laser diode. [JUN-JUL 2021 / in progress]

(C) In addition to (B), investigate potential alternatives to GaN-PCSS in both PCSS and non-PCSS domains. [JUN–JUL 2021 / in progress].

(D) Define performance metrics for PCSS-based driver and complete numerical calculations for required output current at each stage and corresponding PCSS (GaN/GaAs) operating voltages in light of electric fields required for lock-on/avalanche mode, establish real-time implementation timeline, cost estimates, jitter limitation, and explore ways to protect LDA from PCSS ringing. [MAR 2021 / partially complete / revisit after completing (B)].

(E) Demonstrate a tunable 1.7kV SiC-MOSFET powered frozen wave generator (FWG) prototype on a custom-built PCB with Cree/Wolfspeed MOSFET(s), 16-segments of 50 Ω coaxial cables and/or microstrip transmission lines capable of generating chirped pulse widths. [JUL–AUG 2021]

(F) Proof of concept testing of the two-stage PCSS-enabled driver system with a 50 Ω load at 1 kHz pulse repetition rate (PRR) [AUG–SEP 2021]

(G) Working prototype demonstration at ~MHz PRR with laser diode array/stack and ancillary optics based on HPM source driver needs including thermal management system (TMS). [OCT–NOV 2021]

8.2.3 Progress Made Since Last Report

(C) The commercial off-the-shelf silicon optodiodes procured from Voltage Multipliers Inc. have been tested to evaluate their performance in terms of rise-time, fall-time, pulse-widths and on-state resistance in order to be considered as a potential alternative to GaN-PCSS. The testing was performed on a 4.4-Ω microstrip with a 200-μJ laser pulse illumination. The device response at low energy optical illumination (~20-μJ) will be studied in the next reporting period to finalize evaluating its implementability as an alternative to GaN-PCSS.

(E) The first iteration of design, fabrication and testing of an 8-segment SiC-MOSFET powered FWG has been completed. A functioning FWG with chirped pulse-widths has been demonstrated, but predominant reflection-induced ringing was noticed, which will be mitigated in the next iteration.

8.2.4 Significant Finding(s) and Mission Impact

8.2.4.1 Summary to Date

(A) The state-of-the-art COTS laser driver specifications and limitations have been comprehensively studied, and target performance metrics have been determined in terms of output current (>120-A), pulse repetition rate (>1-MHz), transient response (<200-ps risetime and <1-ns pulse width), and volume (<0.75 cu-ft). A preliminary feasibility study has signified the need for lock-on conduction mode with ~$10^{2.6}$ gain factor to drive at >1-MHz pulse repetition rate while limiting the amplification stages to 2. This reduces monetary costs to 10–12% of the conventional laser system, while achieving the expected goal of miniaturizing the optical subsystem by 90%.

(B) Pulse trigger requirements for the LDA/LDS have been identified based on Jenoptik's actively cooled quasi continuous wave vertical diode laser stacks to tailor the device parameters of the enabling switch accordingly.

(C) Silicon optodiodes are being evaluated against the identified performance metrics for the enabling switch. The first iteration of testing was performed at 200 V charge voltage with 200-µJ laser illumination. The device response needs to be evaluated for the optical energies ~20-µJ/pulse which will be carried out in the next reporting cycle.

(D) Numerical calculations have been completed to estimate the electric fields and corresponding voltage bias required to induce lock-on operation while exploring ways to minimize the potential risks of high jitter at ~MHz order PRR switching, power reflections due to impedance mismatch, and negative ringing currents during PCSS recovery. Expected on-state resistance and power dissipation for 50 µm and 100 µm devices in lock-on conduction mode have been calculated to estimate cooling system requirements while retaining the expected SWaP-C^2 factor.

(E) A MOSFET-enabled FWG prototype has been fabricated and tested. The goal of this effort is to demonstrate a 1.7-kV MOSFET-switched compact tunable pulse generator capable of generating chirped pulse-widths. Primary operation of an FWG has been demonstrated at 150-V, but the impedance mismatch induced reflections in the circuit have resulted in ringing across the transmission lines which needs to be mitigated.

3.2.4.2 Since Last Report:

(C) In an effort to evaluate switching technologies as potential alternatives for GaN-PCSS, commercial off-the-shelf silicon optodiodes rated for 15-kV procured from Voltage Multipliers Inc. (SKU: OZ150SG) have been tested on a 4.4-Ω microstrip with 2.5-ns and 5-ns propagation delays on the charge-and discharge-sides, respectively, to verify the device's ability to demonstrate <300-ps rise-time and ~1-ns pulse width while pushing >100-A current when excited with a 70-ps FWHM ~200-µJ laser pulse. These devices typically come with >2-mm thick epoxy encapsulation. Optical absorption parameters for the epoxy were not reported by the manufacturer. The tests have been performed with and without the encapsulation to study the device response in both cases. The results from the test are reported below:

	Pulse energy (µJ)	Charge voltage (V)	Output voltage (V)	Rise time (ps)	Fall time (ns)	On-state resistance (Ω)
With 2.5-mm encapsulation	200	200	60	620	8.532	2.93
With <0.5-mm encapsulation	200	200	96.4	398	6.606	0.143

Table 8.2.1. Results from Si optodiode pulse testing performed at 200-V charge voltage with a 70-ps FWHM 200-µJ optical pulse illumination.

A significant reduction in on-state resistance (~2.787-Ω) and rise- and fall-times (~222-ps and 1.926-ns, respectively) has been observed when tested with <0.5-mm encapsulation. While the device performance at 200-µJ optical pulse energy is on the order of the target metrics in terms of on-state resistance (0.143-Ω observed vs. 0.072-Ω target) and pulse width (6.6-ns observed vs. 1-ns target), the device response at low energy optical illumination (~20-µJ) needs to be studied to evaluate its implementability as an alternative to GaN-PCSS.

(E) The first iteration of an 8-segment SiC-MOSFET powered pulse-width chirp-capable FWG has been fabricated and tested. The design implements a 1.7-kV Cree/Wolfspeed SiC-MOSFET (C2M045170P) rated for 13-ns rise-time driven using a Texas Instruments UCC5390 driver. Theoretically, the FWG output pulse-width is dependent on the propagation delay induced by the implemented transmission line segments. For the transmission line segments, 4 pairs of coaxial cables with 0.66 velocity factor were used, each pair with lengths 5-, 4-, 3- and 1-meters inducing propagation delays of 25-ns, 20.23-ns, 15.17-ns, and 5.05-ns, respectively. The testing was performed at 150 V charge voltage and 1 MHz repetition rates with 30% gate trigger duty cycle. The anticipated pulsewidth chirp along the lines of the propagation delay times induced by the coaxial cables was observed; however, the reflection-induced ringing resulting in pulse deformation has been observed, which needs to be mitigated in the next iteration.

9.0 Thermal Management

9.1 Nanofluid Heat Transfer Fluid Development

(Jordan Berg, Roy Allen, and Sarvenaz Sobhansarbandi)

9.1.1 Problem Statement, Approach, and Context

Primary Problem: Dielectric fluids (non-conductive coolant) used in thermal management systems, while suitable for high-voltage HPM-based technologies, possess inherent thermophysical fluid properties (low thermal conductivity, high viscosity) that inhibit their ability to achieve >1 GW/m^3 cooling densities.

Solution Space: Develop a nanofluid by entraining ceramic nanoparticles and dispersants within the dielectric base-fluid, pure silicon fluid (PSF), to increase the nanofluid's thermophysical properties and cooling density capabilities with a similar form-factor.

Sub-Problem: While the dynamic viscosity of the dielectric fluid used, PSF-20cSt, is 'low' relative to other silicone-based fluids, it is ~15 times more viscous than water, and therefore requires increased pumping power within the TMS. Compounding this issue is the necessity to increase the flowrate of the fluid to achieve an equivalent heat removal rate compared to that of a water-based coolant.

State-of-the-Art (SOTA): Nanofluids, with optimal ratios of fluid-to-nanoparticles, have been shown to increase the thermal conductivity of dielectric fluids by 87% in comparison to the generic dielectric fluid alone; resulting in either greater cooling density, decreased pumping power, or reduced mass flow rate requirements.

Deficiency in the SOTA: The addition of nanoparticles within a base-fluid results in a tradeoff between one or more thermophysical properties. For example, adding nanoparticles may increase thermal conductivity of the nanofluid but may result in increased viscosity; i.e., heat removal rate may increase, but the required pumping power along with it. To the best of our knowledge, no one has attempted to create a nanofluid mixture with a goal of keeping the viscosity low. Therefore, the optimal nanoparticle-to-fluid ratio and specific nanoparticle type for the HPM thermal management systems needs to be identified and optimized with an attempt to maintain the viscosity of the mixture as low as possible.

Solution Proposed: Develop a nanofluid with both desirable thermal properties and a relatively low viscosity that can serve as a viable heat transfer fluid (HTF) for TMSs in HPM topologies and other high power density applications. Utilize systematic numerical and experimental strategies to evaluate a large sample set of various nanoparticles (with surfactants and dispersants).

Relevance to OSPRES Grant Objective: Increase cooling densities for HPM systems without requiring TMS design permutations, while decreasing pumping power requirements, in-line with the SWaP-C^2 objective.

Risks, Payoffs, and Challenges:

Risk: The pressures incurred by using a silicone-based fluid in a high-flow regime are not insignificant; large pump-chiller systems may still be necessary.

Challenges: Creating low volume-fraction samples of nanoparticles and surfactants is near equipment precision limit. Maintaining accuracy is critical to properly study modified fluids.

Payoff: A modified nanofluid dielectric fluid can be used to increase cooling capacity of any high power density system. An optimized nanofluid has the potential to extract 20% up to several factors more than the base fluid.

9.1.2 Tasks and Milestones / Timeline / Status

(A) Measure thermophysical properties of currently utilized PSF-20cSt / DEC20–JAN21 / Completed.

(B) Establish theoretical model of nanofluid compositions / DEC20–JAN21 / Completed.

(C) Create and test modified PSF-20cSt with nanoparticles and surfactants / JAN–MAR21 / Completed.

(D) Select the nanofluid mixture with optimal thermal properties and re-evaluate the CFD modeling / MAR–APR21 / Completed.

9.1.3 Progress Made Since Last Report

This effort is currently on hold.

10.0 UAS Engagement Wargaming & Modeling and Simulation (M&S)

10.1 Fixed-Effector Wargaming Simulation Toolkit Development

(Nolan Petersen and Travis Fields)

10.1.1 Problem Statement, Approach, and Context

Primary Problem: Wargaming simulations enable rapid evaluation of different weapon systems and strategies. However, the lack of easy to use, high-fidelity software tools makes producing and studying different engagement scenarios (i.e., one friendly system versus five hostile agents) difficult and time-consuming.

Solution Space: We propose developing a simulation environment using the Unity real-time development platform to offer an easy to use, medium-fidelity environment for the purpose of studying different blue vs. red engagement scenarios. Unity is a well-established game development software, with a strong community base for tutorials, training, and software assistance. This makes Unity an ideal solution for a medium-fidelity simulation environment to narrow down optimal fixed effector configurations, which could then be studied further in a higher fidelity environment.

State-of-the-Art (SOTA): Current software tools for this purpose are tedious to adapt and/or modify for running different scenarios due to a lack of support as well as documentation.

Relevance to OSPRES Grant Objective: The ability to simulate and benchmark performance of different scenarios, such as different fixed-effector positions, types, and targeting strategies to provide insight into the ideal utilization of HPM-related systems.

10.1.2 Tasks and Milestones / Timeline / Status

(A) Reproduction of previous results obtained from the previously used wargame software Modern Air Power by John Tiller Software, which is no longer in development, using the Unity environment / MAY21 – JUN21 / Completed.

(B) Implementation of radar uncertainty into simulation environment enabling increased realism to better simulate current targeting capabilities / JUN21 – JUL21 / In Progress.

(C) Trade-space study of microwave, tracking, and hostile agent performance to identify key limitations and low-risk, low-cost improvements enabling increased weapon efficacy / JUL21 – SEP21 / Not Yet Started.

10.1.3 Significant Finding(s) and Mission Impact

(A) The current objective is to develop a realistic simulation environment capable of easily being modified by the user without compromising the results and realism of the simulation. This has primarily involved reproducing results obtained from the previously mentioned wargame software Modern Air Power by John Tiller Software. The results produced came from a simple scenario in which a ground-based effector was surrounded by 32 equally spaced UAVs that are simultaneously converging on

the effector. The effector had a range-dependent probability of neutralization in accordance with the inverse square law. Without access to the original code, from which these results were produced, the main challenge was in accurately reproducing the previous results and allowing the user to speed up and slow down the simulation without affecting said results.

10.2 Airborne Effector Weapon Task Assignment

(Cody Smith and Travis Fields)

10.2.1 Problem Statement, Approach, and Context

Primary Problem: Unmanned aircraft technological development trends suggest the potential for the application of both coordinated and cooperative hostile sUAS attacks in the near future. Defense strategies are currently under development which primarily utilize aerial- or ground-based defense systems or a layered combination of the two. An engagement with multiple blue (friendly) vehicles against many red (hostile) vehicles presents an interesting challenge in assigning which blue engages which red(s) as the computational burden grows factorially.

Solution Space: We propose to combine the Moving Traveling Salesman Problem with Genetic Algorithms with constraints in order to produce computationally efficient task assignment allocations to the blue forces.

State-of-the-Art (SOTA): Many current techniques consider stationary targets and/or holonomic vehicles, which within the proposed scenario is not applicable. Considering the task assignment problem with constrained (or realistic flight-like) motion with many potential targets that must be intercepted with several friendly assets is a unique (at least in the literature) problem.

Relevance to OSPRES Grant Objective: The concepts for weapon task assignment (WTA) are applicable to both fixed and airborne weapon systems. Developing the strategies for assigning assets is critically important for considering layered defense scenarios, as the battlefield is now heterogeneous with a diverse array of capabilities, performance, and cost.

10.2.2 Tasks and Milestones / Timeline / Status

(A) Literature review on task-assignment-related studies/research activities / MAR21–MAY21 / Completed.

(B) Implementation and evaluation of engagement-level WTA (one vs. few) in simulated environment / MAY21–JUN21 / In Progress.

(C) Implementation and evaluation of mission-level WTA (few vs. many) in simulated environment / JUN21–JUL21 / Upcoming.

(D) Dissemination of Genetic and Auction-based algorithm performance for realistic mission and engagement-level scenarios / AUG21–SEP21 / Upcoming.

10.2.3 Progress Made Since Last Report

(B) A brute force engagement algorithm was developed and has been undergoing initial verification. The brute force algorithm looks at every permutation for pursuing few red targets (i.e., intercepting red A, then C, then B, then D) and identifying the path with the shortest time to complete the mission.

10.2.4 Significant Finding(s) and Mission Impact

10.2.4.1 Summary to Date

(A) A review of the task assignment literature was completed and two key strategies were identified: Genetic Algorithm and Auction Algorithm.

10.2.4.2 Since Last Report

The current study aims to develop a framework comprised of the necessary algorithms required for effective path-planning optimization and weapons target assignment (WTA) for both aerial- and ground-based weapons during hostile unmanned aerial threat engagements. Historically, various types of algorithms such as the auction, genetic, and brute force algorithms have been used for path planning and WTA. The development of an effective WTA framework will require an algorithm that is capable of handling a combination of features from several of the common path planning problems: for example, the Traveling Salesman Problem with Neighborhoods to manage conditions where direct interception is not required, the Moving Traveling Salesman Problem where incoming hostile targets are known to be moving, and the Dynamic Traveling Salesman Problem where assigned paths are updated with the emergence of previously unknown threats. Various heuristics are to be studied and a comparative analysis is to be performed against several other popular path planning algorithms (i.e. Auction and Genetic algorithms) to gain insight and develop situational strategies for potential aerial threats. Currently, an analysis tool has been developed using brute force that is capable of outputting the optimal path, path length, and time of completion for a friendly system to intercept a small number of incoming hostile threats ($n < 9$). An example 1 vs. 4 brute force engagement solution is provided in Figure 10.2.1. Customizable parameters include blue starting position, red starting positions, red starting speeds, minimum protection radius, and number of reds. This tool will be used as a method for comparative analysis with non-brute-force approaches like the Genetic and Auction algorithms. Additionally, various aspects like patrol and detection radius will be evaluated. Immediate future work includes an expansion of the brute force analysis tool to include multiple friendly systems for ‘few vs. few’ path planning scenarios.

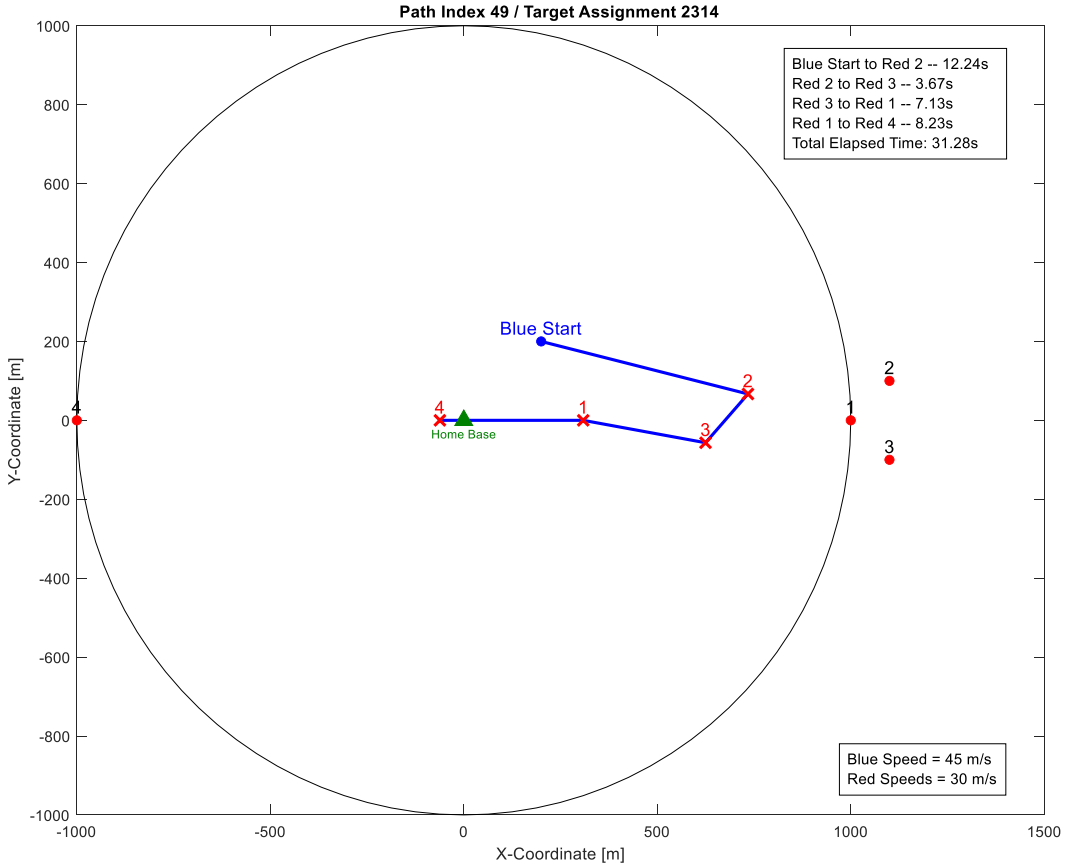


Figure 10.2.1. One versus four brute force-derived optimal trajectory.

11.0 Program Management

11.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

11.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

11.3 Major Procurement Actions

11.4 Travel

Destination	Purpose	Attendees	Estimated Costs

11.5 Pending or Upcoming Public Release Requests

12.0 Appendix: Academic and IP Output

12.1 Students Graduated

Name	Degree	Currently
Al-Shaikhli, Waleed Berg, Jordan	MS Spring 19 MS Spring 21	Kansas City National Security Campus, Honeywell
Bissen, Bear	MS Spring 19	UMKC/MIDE (Staff)
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Hanif, Abu	PhD May 21	
Harmon, Aaron	BS	Missouri University of Science & Technology
Harp, Joshua	MS	Small Business
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Klappa, Paul	MS Spring 21	
Labrada, Dario	BS Spring 20	UMKC/MIDE (MS Student)
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory
Renzelman, Jeff	MS Spring 18	Kansas City National Security Campus, Honeywell
Roy, Sourov	PhD Spring21	UMKC/MIDE (Staff)
Wagner, Adam	MS Fall 20	Kansas City National Security Campus, Honeywell
Xia, Shengxuan	BS	Missouri University of Science & Technology

12.2 Journal Publications

12.2.1 In Preparation

[1] N. Gardner, A. N. Caruso, and P. Doynov, “Diode-Based Non-Linear Transmission Line: A Bandwidth and Center Frequency Tuning Study,” *Transactions on Microwave Theory and Technique*, In Preparation, **2021**.

[2] B. Barman, D. Chatterjee, and A. N. Caruso, “Tradespace analysis of wideband coaxial probe-fed microstrip patch electrically small antenna elements,” In preparation, **2021**.

[3] M. Z. M. Hamdalla, B. Bissen, J. D. Hunter , L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, “Experimental Evaluation of CMA Predictions and Control of Electromagnetic Interference to UAVs,” In Preparation, **2021**.

[4] S. Xia, J. Hunter, A. Harmon, M. Hamdalla, A. Hassan, V. Khilkevich, D. Beetner, “Simulation Driven Statistical Analysis of the Electro-magnetic Coupling to Microstriplines,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[5] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, “Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field Coupling to Randomly Shaped Wires,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

12.2.2 Submitted / Under Revision

[6] W. Azad, F. Khan, and A. N. Caruso, "A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Featuring Custom Isolated Gate Driver Circuit Combined With Coupling and Snubber Circuits," *IEEE Transactions on Power Electronics*, Submitted, **2021.**

[7] J. N. Berg, R. C. Allen, and S. Sobhansarbandi. "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation." *International Journal of Thermal Sciences*, Submitted, **2021**.

[8] Khulud Alsultan, Mohamed Hamdalla, Sumitra Dey, A. N. Caruso, Praveen Rao, and A. M. Hassan, "Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform," *IEEE Open Journal of Antennas and Propagation,* Submitted, **2020**.

[9] John Keerthi Paul Bhamidipati, Eliot R. Myers, Adam M. Conway, Lars F. Voss, and Anthony N. Caruso, "Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches," *IEEE Transactions on Electronic Devices*, Under Revision, **2020**.

12.2.3 Published / In Press

[10] W. Azad, F. Khan, and A. N. Caruso, "A Medium Power, Self-Sustaining, Configurable RF Pulse Generation Circuit Using a Nonlinear Transmission Line and Power Amplifier in a Closed Loop Configuration, *IEEE Transactions on Plasma Science*, **2021** [doi].

[11] S. Roy, W. Azad, S. Baidya and F. Khan, "A Comprehensive Review on Rectifiers, Linear Regulators and Switched-mode Power Processing Techniques used for Powering Biomedical Sensors and Implants utilizing In-body Energy Harvesting and External Power Delivery," *IEEE Transactions on Power Electronics*, Early Access, **2021** [doi].

[12] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems," *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364-373, **2019** [doi].

12.3 Conference Publications

12.3.1 Submitted / Accepted

[1] H. Thompson, S. Shepard, A. N. Caruso, "A Tubular Core Optical Power Amplifier," submitted to the *2021 DEPS Advanced High-Power Laser and Beam Control Conference*, Virtual Event, August 3-5, 2021 (Submitted).

[2] B. Barman, D. Chatterjee, and A. N. Caruso, "Effect of Ground Plane Shape and Size on the Input Impedance of a Monopole embedded in a Grounded Dielectric

Substrate," submitted to the *2021 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*, Marina Bay Sands, Singapore, December 4-10, 2021.

[3] B. Barman, D. Chatterjee, and A. N. Caruso, "Comparison of Q-Factor Calculation Methods for Wideband Microstrip Patch Antennas," submitted to the *2021 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*, Marina Bay Sands, Singapore, December 4-10, 2021.

[4] S. R. Shepard and H. A. Thompson, "Self-focusing in Guided and Un-guided Media," submitted to the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, 2021.

[5] B. Barman, D. Chatterjee, and A. N. Caruso, "Probe-location Optimization in a Wideband Microstrip Patch Antenna using Genetic Algorithm, Particle Swarm and Nelder-Mead Optimization Methods," accepted in *2021 International Applied Computational Electromagnetics Society (ACES) Symposium*, USA, August 1-5, 2021.

12.3.2 Presented

[6] W. Azad, S. Roy, and F. Khan, "A Single Gate Driver-based Four-stage High-voltage SiC Switch Having Dynamic Voltage Balancing Capability," *2021 IEEE Applied Power Electronics Conference and Exposition* (APEC), Phoenix, AZ, USA, June 9-12, 2021.

[7] W. Azad, S. Roy, F. Khan and A. N. Caruso, "A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuits," *2021 IEEE Kansas Power and Energy Conference* (KPEC), Manhattan, KS, USA, April 19-20, 2021 [doi].

[8] T. Layman, T. D. Fields, and O. A. Yakimenko, "Evaluation of Proportional Navigation for Multirotor Pursuit," AIAA SciTech Forum, Virtual Event, January 11-21, 2021 [doi].

[9] P. J. Klappa, and T. D. Fields, "Assessment of Fixed-Wing UAV System Identification Models during Actuator and Payload Drop Failures," AIAA Atmospheric Flight Mechanics Conference, Virtual Event, January 11-21, 2021 [doi].

[10] J. Hunter, S. Xia, A. Harmon, A. M. Hassan, V. Khilkevich, and D. Beetner, "Modeling and Statistical Characterization of Electromagnetic Coupling to Electronic Devices," *IEEE International Symposium on Antennas and Propagation and NSRM USNC-URSI National Radio Science Meeting*, Boulder, CO, January 4-9, 2021 [doi].

[11] B. Barman, K. C. Durbhakula, B. Bissen, D. Chatterjee, and A. N. Caruso, "Performance Optimization of a Microstrip Patch Antenna using Characteristic Mode and D/Q Analysis," *2020 XXXIIIrd General Assembly and Scientific Symposium of the International Union of Radio Science*, Rome, Italy (online conference), Aug 29-Sept 5, 2020, pp. 1-4 [doi].

[12] J. Berg, and S. Sobhansarbandi. “CFD Modeling of Thermal Management Systems for a Silicon Semiconductor Switch.” *ASME 2020 Heat Transfer Summer Conference collocated with the ASME 2020 Fluids Engineering Division Summer Meeting and the ASME 2020 18th International Conference on Nanochannels, Microchannels, and Minichannels*, Virtual, July 13–15, 2020, American Society of Mechanical Engineers Digital Collection [doi].

[13] B. Barman, D. Chatterjee, and A. N. Caruso, “Performance Optimization of Electrically Small Microstrip Patch Antennas on Finite Ground Planes,” 2020 *IEEE International Symposium on Antennas and Propagation and North American Radio Science Meeting*, Montreal, Quebec, Canada, July 5-10, 2020, pp. 1–2 (online conference) [doi].

[14] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, “Scalable Characteristic Mode Analysis: Requirements and Challenges (White Paper),” *Large Scale Networking (LSN) Workshop on Huge Data: A Computing, Networking and Distributed Systems Perspective Sponsored by NSF*, Chicago, IL, April 13-14, 2020.

[15] M. Hamdalla, A. N. Caruso, and A. M. Hassan, “Predicting Electromagnetic Interference to a Terminated Wire Using Characteristic Mode Analysis,” *Proceedings of the Annual Review of Progress in Applied Computational Electromagnetics (ACES)*, Monterey, CA, March 22-26, 2020. [doi]

[16] W. Azad, F. Khan, and A. Caruso, "Self-sustaining High-power RF Signal Generation Using LDMOS Based Power Amplifier and Nonlinear Transmission Line," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 3567-3572 [doi].

[17] A. Hanif, W. Azad, and F. Khan, "Detection of Bond Wire Lift Off in IGBT Power Modules Using Ultrasound Resonators," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 345-350 [doi].

[18] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, “Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS,” *Annual Directed Energy Science and Technology Symposium*, March 2020 (abstract appeared, but talk cancelled due to pandemic).

[19] B. Barman, D. Chatterjee, and A. N. Caruso, “Some Investigations into Mutual Coupling Analysis for Trade Space Studies of Linear Arrays,” *2019 IEEE International Symposium on Phased Array Systems and Technology (PAST)*, Waltham, MA, October 2019, pp. 1-8 [doi].

[20] B. Barman, D. Chatterjee, and A. N. Caruso, “Characteristic Mode Analysis of a straight and an L-probe fed Microstrip Patch,” *2019 IEEE Indian Conference on Antennas and Propogation (InCAP)*, Ahmedabad, India, Dec 2019, pp. 1-3 [doi].

[21] M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of the Effect of the UAV Frame Material on Coupling and Interference," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019 [doi].

[22] M. Hamdalla, J. Hunter, Y. Liu, V. Khilkevich, D. Beetner, A. Caruso, and A. M. Hassan, "Electromagnetic Interference of Unmanned Aerial Vehicles: A Characteristic Mode Analysis Approach," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019 [doi].

[23] B. Barman, D. Chatterjee, and A. N. Caruso, "Analytical Models for L-Probe fed Microstrip Antennas," *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

[24] K. C. Durbhakula, J. Lancaster, A. M. Hassan, D. Chatterjee, A. N. Caruso, J. D. Hunter, Y. Liu, D. Beetner, and V. Khilkevich, "Electromagnetic Coupling Analysis of Printed Circuit Board Traces using Characteristic Mode Analysis," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (2 pages)*, Atlanta, Georgia, USA, July 7-12 2019 [doi].

[25] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "On the Location of Transverse Electric Surface Wave Poles for Electrically Thick Substrates," Proceedings of the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 [doi].

[26] M. Hamdalla, B. Bissen, A. N. Caruso, and A. M. Hassan, "Experimental Validations of Characteristic Mode Analysis Predictions Using GTEM Measurements," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Montréal, Québec, Canada, July 5-10, 2020 [doi].

[27] W. Azad and F. Khan, "Sustaining High-power RF Signal Generation in a Positive Feedback Network," *2019 IEEE Pulsed Power and Plasma Science Conference (PPPS)*, Orlando, FL, USA, June 23-28 2019.

[28] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, "Scalable characteristic mode analysis using big data techniques," *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[29] M. Hamdalla, W. Al-Shaikhli, J. Lancaster, J. D. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of Electromagnetic Coupling to Wires with Realistic Shapes," *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[30] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "Location of Surface Wave Poles in Sommerfeld Integrals: A Mittag-Leffler Expansion Approach," *Proceedings of the URSI-B International Symposium on Electromagnetic Theory*, URSI Commission, San Diego, USA, May 2019 [doi].

[31] K. C. Durbhakula, D. Chatterjee and A. M. Hassan, "Analytical Evaluation of Sommerfeld Integral Tails Present in Two-layered Media Green's Functions," *Proceedings of the Indian Conference on Antennas and Propagation* (InCAP), Hyderabad, India, December 2018 [doi].

[32] D. Beetner, V. Khilkevich, A. M. Hassan, J. Hunter, Y. Liu, and D. Floyd, "Characterization of the Electromagnetic Coupling to UAVs," *DE Systems Symposium*, September 24-27, 2018

[33] C. Hartshorn, K. Durbhakula, D. Welty, D. Chatterjee, J. Lancaster, A. M. Hassan, and A. N. Caruso, “Crosstalk and Coupling to Printed Circuit Board Metallic Traces with Arbitrary Shapes,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[34] M. Hamdalla, J. Roacho-Valles, J. Hunter, D. Beetner, A. M. Hassan, and A. N. Caruso, “Electromagnetic Analysis of Unmanned Aerial Vehicles Using Characteristic Mode Analysis,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[35] C. Hartshorn, M. Hamdalla, J. Lancaster, A. M. Hassan, and A. N. Caruso, “Electromagnetic Vulnerability of Wires with Arbitrary Shape,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[36] K. C. Durbhakula, D. Chatterjee, A. M. Hassan, and M. S. Kluskens, “Studies on Numerical Evaluation of Sommerfeld Integrals for Multilayer Topologies,” *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018.

[37] J. Lancaster, D. Chatterjee, and A. N. Caruso, “Some Investigations into the Dispersion Characteristics of Localized Bessel Beams,” published in the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018 (1 page URSI Abstract).

[38] M. Hamdalla, A. M. Hassan, and A. N. Caruso “Characteristic Mode Analysis of Unmanned Aerial Vehicles with Realistic Shapes and Material Composition,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Boston, MA, July 8-13, 2018.

[39] W. Azad, S. Roy, A. S. Imtiaz, and F. Khan, "Microelectromechanical System (MEMS) Resonator: A New Element in Power Converter Circuits Featuring Reduced EMI," *2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, Niigata, May 20-24, 2018, pp. 2416-2420 [doi].

[40] J. Hunter, Y. Liu, D. Floyd, A. Hassan, V. Khilkevich, and D. Beetner, “Characterization of the Electromagnetic Coupling to UAVs,” Annual Directed Energy Science and Technology Symposium, Feb 26-March 2, 2018.

12.4 Conference Presentations

[1] W. Azad, S. Roy, and F. Khan, “A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver,” *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, 2020 (oral).

DEPS Posters and Presentations 2020

[2] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[3] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

GOMAC 2019

[4] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[5] Eliot Myers, Picosecond High Power Switching Technologies

[6] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium, Destin, Florida, USA, April 2019:

[7] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[8] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[9] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[10] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[11] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[12] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[13] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[14] Deb Chatterjee, Studies On Antenna Characterization And Propogation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

DEPS Posters and Presentations 2018

[15] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[16] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[17] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

DEPS Posters and Presentations 2017

[18] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

12.5 IP Disclosures Filed

Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, 19UMK005, 28SEPT2018

Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal”, 19UMK008, 28DEC2018.

Doynov, “Pulse Differential High-power Microwave Generation”, 19UMK007, 02JAN2019.

Doynov, “Scalable Modular System for High-power Microwaves Generation”, 20UMK010, 19APR2020.

Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna”, 20UMK011, 19APR2020.

Shepard, “A Novel Optical Fiber Amplifier”, 20UMK012, 02JUN2020.

Doynov, Caruso, “High-efficiency High-power Microwave Generation using Multipass Non-linear Network Topologies”, 19UMK017, 29AUG2020.

Shepard, “A Low Noise Optical Amplifier”, 21UMK007, 14SEPT2020.

Bhamidipati, Myers, Caruso, “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources”, 21UMK009, 04NOV2020.

12.6 Provisional Patents Filed

Doynov, Caruso, “High-efficiency High-power Microwave Generation using Multipass Non-linear Network Topologies”, filed 26NOV2019.

12.7 Non-Provisional Patents Filed

None to date

ONR HPM Program - Monthly Status Report (MSR) – JULY 2021

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 AUGUST 2021

Distribution Statement ~A: Distribution authorized to all OSPRES Grant and Contract performers, and any OSPRES uncompensated collaborators. Further dissemination per the Office of Naval Research, Ryan Hoffman (ryan.hoffman@navy.mil, 703-696-3873) or higher DoD Authority.

OSPRES Grant Goal: address and transition technologies and capabilities that enable the OSPRES Grant Objective using the OSPRES Grant Approach, while educating the next generation of pulsed power and defense minded, stewards and innovators.

OSPRES Grant Objective: to execute high-risk, high-payoff efforts that mitigate, fill or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable and electronically steerable high power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average power space, and includes the kill chain considerations including the target and its responsivity to radiofrequency stimuli.

OSPRES Metrics of Success: developed technologies and capabilities that are published in the peer review, protected as intellectual property, and/or, transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use, as enabling/integratable capability(ies).

OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

OSPRES Grant Security: All efforts should be fundamental and publically releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

1.0 Contents

2.0 Executive Summary 4
2.1 Progress, Significant Findings, and Impact 4
2.2 Completed, Ongoing, and Cancelled Sub-Efforts 6
2.3 Running Total of Academic and IP Program Output 7
3.0 Prime Power and Conditioning 8
3.1 HV Switch Pulsed Chargers 8
4.0 Switch Evaluation and Innovation 11
4.1 GaN:C PCSS Direct RF Modulation 11
4.2 Drift-Step Recovery Diode and Pulse Shaping Device Optimization 14
4.3 Pioneering Drift-Step Recovery Diode Processing and Manufacturing 26
4.4 Characterization of SOS Diode Performance through DOE Augmentation 35
4.5 DSRD-Based Pulsed Power Source Systematic Topological Optimization 39
4.6 Optimizing SOS-IES Pulse Generator Performance with Machine Learning 45
4.7 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners 51
5.0 Pulse Forming Networks 57
5.1 Diode-Based NLTLs 57
6.0 Tradespace Analysis of Ultra-Wide-Band Antenna Arrays 63
6.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs) 63
6.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna 68
6.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna 76
6.4 Tradespace Analysis of Ultra-Wide-Band (UWB) Fractal Antenna 83
7.0 RF Coupling 92
7.1 Enclosure Effects on RF Coupling 92
8.0 Laser Development 97
8.1 Fiber Lasers and Optical Amplifiers 97
8.2 WBG-PCSS Enabled Laser Diode Array Driver 101
9.0 Thermal Management 105
9.1 Nanofluid Heat Transfer Fluid Development 105
9.2 Ultra-Compact Integrated Cooling System Development 108
10.0 UAS Engagement Wargaming & Modeling and Simulation (M&S) 111
10.1 Fixed-Effector Wargaming Simulation Toolkit Development 111
10.2 Airborne Effector Weapons Target Assignment 113
11.0 Program Management 118
11.1 Issues 118
11.2 Interactions with Others 118
11.3 Major Procurement Actions 118
11.4 Travel 118
11.5 Pending or Upcoming Public Release Requests 118
12.0 Appendix A: Academic and IP Output 119
12.1 Students Graduated 119
12.2 Journal Publications 119

12.3 Conference Publications 120
12.4 Conference Presentations 124
12.5 IP Disclosures Filed 125
12.6 Provisional Patents Filed 126
12.7 Non-Provisional Patents Filed 126
13.0 Appendix B: Jet Impingement Thermal Management System 127
13.1 Executive Summary 127
13.2 Technical Background 127
13.3 Methods 129
13.4 Results and Discussion 131
13.5 Significant Findings 133
13.6 Publications 134
13.7 References 134

2.0 Executive Summary

2.1 Progress, Significant Findings, and Impact

GaN:C PCSS Direct RF Modulation. To model the optical coupler approach to illuminating the PCSS, we circumvented COMSOL delays via a time domain simulation in Mathematica. Pulse broadening due to the saturable absorbing in GaN restricts the switch times to over 2 ns in devices of 3 cm in length (in an initial, not yet optimized, coupler design).

IES Pulsed Power Source Technology Leveraging DSRDs. Epitaxially grown DSRDs are being manufactured with industry partners to experimentally compare their performance to the results achieved through TCAD simulations. The diodes will be evaluated using the newly developed design of experiment (DOE) and compared to the numerical results produced. The latest iteration of the DSRD-based 2×2 pulse generator circuit aimed to increase the peak voltage and risetime produced, which match the LTspice simulation output's optimal values realized through machine learning, did not achieve significant inceases as anticipated. Further investigation of these results is underway to pinpoint whether the diode is the limiting factor, or the circuits new components selected.

Diode-Based Nonlinear Transmission Line. Further testing was performed using a PCSS-based pulsed source to excite the K50F and K100F D-NLTLs. The generated PCSS pulse had a FWHM 1/3 of the PCSS pulse used in the June PCSS-D-NLTL tests, resulting in the lines operating with a low pass filter characteristic instead of a soliton generation characteristic.

Antennas. Time-domain analysis of an UWB microstrip ESA element at the UHF range (638–990.6 MHz) has been performed, in terms of Fidelity Factor calculation, via CST Microwave Studio. A single ESA element, modeled on a polyethylene substrate ($f_{\text{operating}}$ ≈ 940 MHz), and a 2×2 array of ESA elements, modeled on a TMM-10i substrate ($f_{\text{operating}}$ ≈ 930 MHz), have been finalized and forwarded for manufacturing.

A study on the non-symmetric arrangement of antenna elements in the diamond Koshelev array antenna has shown that the interelement spacing variable in the H-plane axis (S_x) has a higher effect on the array antenna metrics than the interelement spacing variable in the E-plane axis (S_y). In other words, a smaller S_y value can be used with an optimum S_x value without any negative effect on the output. This meets the objective of reducing the physical aperture area of the Koshelev array antenna without degrading its performance. A study on different array topologies for the Shark array antenna has revealed that an ellipse shaped Shark array antenna would yield optimum array antenna metrics with minimum physical aperture area. The machine learning models introduced in 6.4 have been successfully trained with fractal antenna element data and tested for antenna metrics such as gain as a function of frequency, and time domain radiated electric field.

RF Coupling. We propose to use the equivalent circuit approach (ECA) as an effective tool to test several linear/nonlinear loads of the UAV wires using Spice models in a computationally efficient manner. The ECA involves two full-wave simulations to calculate V_{oc} and Z_{in} at the port where the desired load will be located. This month, we have studied different RLC circuits to accurately represent Z_{in} of the UAV wiring system. Two Second series equivalent circuits/resonance is found to be the best circuit to represent Z_{in}.

Fiber Laser. Our tubular optical amplifier can handle power levels that are 2 orders of magnitude above the power limits of the SOTA standard dual-core fiber amplifiers. We quantified the coupling of the tubular glass mode to that of the hollow-core air mode and demonstrate how self-focusing can be used to move roughly half of the power out of glass and into the hollow-core of the tube (with less than 10% being lost into the air outside the tube). This effect means we can roughly double the operating power of our tubular optical amplifiers.

Laser Diode Array Driver. COTS silicon optodiodes have been evaluated as a potential alternative to GaN-PCSS. The device performance at 20-uJ optical illumination showed >100× the required on-state resistance (R_{on}) and ~2× the rise-time (t_{rise}) metrics determined by the feasibility study, making the optodiodes an unviable substitute for GaN-PCSS. Alternative switching technologies including avalanche transistors and silicon avalanche shapers will be evaluated in the near future. A second iteration frozen wave generator (FWG) has been designed, fabricated, and tested for 2-, 4- and 8-segment configurations. Pulse overlap and pulse deformation still exist in the 8-segment unbalanced load configuration, which will be addressed in the next iteration using a tunable component-based transmission medium.

Thermal Management. A full summary report for the jet impingement thermal management system sub-project (MAY 2018–FEB 2021) has been provided in Appendix B. A short summary report has additionally been provided for the nanofluid heat transfer fluid project (NOV 2020–JUL 2021) in Section 9.1. A new sub-project describing the development of an ultra-compact integrated cooling system is introduced this month in Section 9.2.

UAS Engagement Modeling and Simulation. The Unity-based wargaming framework realism was improved through incorporation of reasonable radar/tracking models. Additionally, the challenges associated with brute force planning for multiple friendly assets engaging many hostile assets were quantified, and ongoing efforts are evaluating machine learning techniques to overcome the computational challenges.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

	Start	End
2.2.1 Ongoing Sub-Efforts		
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
HV Switch Pulsed Chargers	DEC 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Enclosure Effects on RF Coupling	OCT2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization	JAN 2021	Present
UAS Engagement M&S	MAR 2021	Present
DSRD-Based IES Pulse Generator Development	APR 2021	Present
Drift-Step Recovery Diode Manufacturing	MAY 2021	Present
IES Diode Characterization	MAY 2021	Present
IES Pulser Machine Learning Optimization	MAY 2021	Present
Sub-Nanosecond Megawatt Pulse Shaper Alternatives	MAY 2021	Present
Ultra-Compact Integrated Cooling System Development	MAY 2021	Present
2.2.2 Completed Sub-Efforts		
Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
Nanofluid Heat Transfer Fluid	NOV 2020	JUL 2021
2.2.3 Cancelled/Suspended Sub-Efforts		
Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020
Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021
Bistable Operation of GaN	FEB 2021	MAR 2021

2.3 Running Total of Academic and IP Program Output

See Appendix for authors, titles and inventors (this list is continuously being updated)

Students Graduated	5 BS, 8 MS, 2 PhD
Conference Publications	35 (5 submitted/accepted)
Journal Publications	3 (4 submitted/under revision)
External Presentations/Briefings	18
IP Disclosures Filed	9
Provisional Patents Filed	1
Non-Provisional Patents Filed	0

3.0 Prime Power and Conditioning

3.1 HV Switch Pulsed Chargers

(Wasekul Azad and Faisal Khan)

3.1.1 Problem Statement, Approach, and Context

Primary Problem: Commercially available high-voltage solid-state switches made by BEHLKE are the best in SWaP-cooling, but are expensive, have long lead times (2–3 months), and are made outside of the US. For the Navy afloat mission to be successful, we need a sustainable supply of US-manufactured switches at a much lower cost.

Solution Space: Design and demonstrate modular high-voltage (~10 kV) and fast (repetition frequency = 100 kHz) solid-state switches using a combination of series- and parallel-connected commercially available inexpensive discrete MOSFETs and custom high-voltage (~10 kV) isolated gate drivers.

Sub-Problem: Voltage balancing among the series-connected MOSFETs, minimization of gate signal delays, cooling of the individual MOSFETs, balancing resistors, high-voltage isolation required for the power supplies, and the controlling pulse width modulated (PWM) signal as well as differential voltage feedback measurement across individual MOSFETs.

State-of-the-Art (SOTA): Direct liquid-cooled solid-state switch from BEHLKE (e.g., HTS-151-30).

Deficiency in the SOTA:

1. BEHLKE-made switches are expensive. For instance, a single HTS-151-30 switch costs around $5,000.
2. BEHLKE switches along with direct liquid cooling units occupy a considerable amount of space. For instance, an HTS-151-30 switch from BEHLKE has a footprint of approximately 225*85*75 mm without considering the liquid cooling system. Some key parameters of this switch are as follows.

   i) Maximum operating voltage = 15 kV

   ii) Maximum continuous load current = 2.52 A (without cooling), 30 A (with liquid cooling)

   iii) Maximum turn-ON peak current = 300 A (pulse width = 200 µs, duty cycle <1%)

   iv) Turn-ON resistance = 1.3 Ω
3. Once the switching frequency is greater than 10 kHz, a liquid cooling system is required to operate the BEHLKE switch.
4. Without liquid cooling, the maximum continuous power dissipation (P_{cont}) of the BEHLKE switch is limited (e.g., for HTS-151-30, P_{cont} is 10 W without liquid cooling).
5. At a higher switching frequency (>20 kHz), the BEHLKE switch requires multiple ancillary DC power supplies, i.e., 5, 15, and 60 V.

6. The switches made by BEHLKE cannot be reconfigured to withstand a higher voltage exceeding their recommended rating. BEHLKE offers separate products to operate them at higher voltage/currents.

Solution Proposed: Designing a modular high-voltage (~10 kV) switch using a single custom isolated gate driver for each module and having a construction cost lower than the BEHLKE switch with equivalent or better performance in all specification categories (Specifications for the BEHLKE switches can be found in the following link: http://www.behlke.com/separations/separation_c4.htm).

Relevance to OSPRES Grant Objective: The proposed modular high-voltage switch is expected to facilitate controlled hundreds-of-nanosecond charging of an array of transmission lines of pulse forming networks to drive an array of PCSSs, thereby producing controlled hundreds-of-picosecond scale high-voltage pulses.

Risks, Payoffs, and Challenges:

I. Lack of rigid control over voltage balancing can lead to a cascaded failure among the series-connected MOSFETs.

II. In the absence of an adequate mitigation scheme, voltage overshoot due to the fast switching speed can exceed the voltage rating of an individual MOSFET, thereby damaging the switch.

III. At high voltage (~10 kV) and high repetition rate (>100 kHz), mitigating EMI to safeguard the individual MOSFETs from false turn-ON is a major challenge.

3.1.2 Tasks and Milestones / Timeline / Status

(A) Design a surface-mount MOSFET-based four-stage switch (6.8 kV rated) and control it using the in-house gate driver, then test its voltage-withstanding ability with a DC supply voltage up to 4–5 kV and evaluate the effectiveness of the thermal management at its current state / DEC 2020 / Completed.

(B) Design and develop a modular HV switch (~10 kV rated) using the concept of the tested four-stage high-voltage switch module and an in-house modular gate driver to drive the modular switch /JAN–FEB 2021 / Completed.

(C)

(i) Test the voltage withstanding ability of the modular HV switch with a DC supply voltage up to 10 kV and switching frequency up to 50 kHz using a resistive load (5–10 kΩ) and evaluate the effectiveness of the thermal management at its current state / FEB–JULY 2021 / Ongoing.

(ii) Test the isolation capability and evaluate the synchronization accuracy of the gate drive signal generated from the modular in-house gate driver / FEB–JULY 2021 / Ongoing.

(iii) Encapsulate the gate driver board with potting material with a high (~15–20 kV) breakdown voltage rating to prevent possible flashover/arcing in between the HV switch and this board / MAR–JULY 2021 / Ongoing.

(D) Design and fabricate a compact power conditioner circuit based on a 12 kV rated SiC switch made by BEHLKE (HTS 121-15) / APR–MAY 2021 / Completed.

(E) Test this modular HV switch coupled with a Si PCSS device up to a DC supply voltage of 5–6 kV and a switching frequency of 50 kHz / On hold.

(F)

(i) Design and develop a 20 kV rated modular (two modules, each with four MOSFETs) HV switch based on the design concept of the 10 kV rated modular switch using 3.3 kV rated SiC MOSFETs (new product made by GeneSiC Semi) / On hold.

(ii) Design and develop a 20 kV rated modular gate driver based on a WPT based planar transformer topology to ensure adequate galvanic isolation (~30–40 kV) for the power supplies of the gate driver / On hold.

3.1.3 Progress Made Since Last Report

This sub-project is currently on hold due to a transition in personnel (student graduation and replacement). We expect work to resume in the next 1–2 months.

3.1.4 Summary of Significant Findings and Mission Impact

(A) The 6.8 kV rated four-stage surface-mount MOSFET developed in-house was successfully tested up to a DC supply voltage of 4 kV and at a switching frequency up to 20 kHz with a 3.2 kΩ resistive load.

(B) A modular (two modules) 10 kV rated HV switch has been designed and a prototype has been developed using 1.7 kV rated SMD MOSFETs (C2M1000170J). An in-house 10 kV rated HV gate driver has been designed and incorporated with the HV switch to drive it. A manuscript on the HV switch and the custom isolated gate driver has been submitted in IEEE Transaction on Power Electronics.

(C) The HV switch coupled with the custom HV gate driver has been tested at a supply voltage up to 6.5 kV at a switching frequency up to 15 kHz. We have observed gate driver malfunctioning at around 6.5 kV and have designed a revised modular gate driver with an alternative optical fiber link.

4.0 Switch Evaluation and Innovation

4.1 GaN:C PCSS Direct RF Modulation

(Heather Thompson and Scott Shepard)

4.1.1 Problem Statement, Approach, and Context

Primary Problem: Need for a more compact, cost-effective RF pulse generation system for Navy afloat missions on smaller vessels and vehicles.

Solution Space: Improve efficiency and reduce necessary material, size, and thermal requirements by utilizing gallium nitride (GaN) in PCSSs through exploitation of its theoretical material properties which allow for higher operating voltages, frequencies, and temperatures, while also eliminating the need for pulse-shaping transmission lines through direct RF modulation using the laser/photon source driving the PCSS.

Sub-Problem: Lack of maturity in compensated gallium nitride semiconductor (i.e., GaN:X with X=C,Fe) PCSS manufacturing, development, and optimization.

State-of-the-Art (SOTA): Si-based PCSS with >10 kV operational voltage, cooling system capacity of 500 W/cm^2, and theoretical breakdown of 1.3 MW/cm.

Deficiency in the SOTA: Si-based technologies requiring ~100 µJ optical pulses per 4 MW of RF output power, increasing the laser energy (per pulse) required for device triggering; long recovery time (ones-of-µs), limiting quick opening and high pulse-repetition-rate operation along with increased heating in the PCSS; critical electric field of 0.3 MV/cm, leading to devices that are ones-of-cm^2 in area for the target peak power; and operating temperature of <160°C, leading to increased cooling requirements.

Solution Proposed: Replace Si-PCSS device with GaN:C utilizing direct RF modulation — eliminating the need for a bulky pulse-forming transmission line (~3 ft long) — capable of handling >3 MW (peak power) with ~20 µJ of incident optical energy, device area <1 cm^2, and operating temperature ~500°C (theoretical temperature which will be limited by circuit components and solder).

Relevance to OSPRES Grant Objective: Reduction in size and cost for cooling system that prevents damage to the PCSS device and components along with eliminating need for a bulky pulse-shaping system, as well as decrease in material cost and needed incident laser energy, leading to enhanced SWaP-C^2 capability with greater modularity and scalability.

Risks, Payoffs, and Challenges: Due to manufacturing limitations, GaN PCSS devices tend to be limited to lateral geometries (both contacts on the top side of the device), limiting operating voltage due to current crowding and surface flashover. The recovery time (ones-to-tens-of-ns) may lead to device heating and increased DC, or zero-frequency, component when generating RF with a period on the same order as the recovery time.

4.1.2 Tasks and Milestones / Timeline / Status

(A) **Start Jan 2021** Demonstrate RF unipolar modulation in the 1–2 GHz regime and up to 2 kV operating voltage with current PCB setup and automated optical delay system. Achieving 2 kV operating voltage should allow for preliminary effects testing before (or in conjunction with) striving towards higher operating voltages. **Ongoing**

(B) **Start June 2021** Demonstrate RF bipolar modulation using an advanced test setup with two GaN:C PCSSs triggered using the same optical delay, but with the second device connected to a negative power supply. **Ongoing**

(C) **Start June 2021** Achieve higher center frequency content in unipolar and bipolar modulation by using a faster (rise-time and pulse-width) laser to activate GaN:C PCSS. **Ongoing**

(D) **Start May 2021** Complete study of recovery for differing gap lengths, incident energies, and operating voltages and find solutions to reduce the recovery time. **Ongoing**

(E) **March-August 2021** Complete study on the feasibility of using mode-coupling to bring the laser light into GaN:C devices, allowing for a possible reduction of laser energy, and pulse shaping within the laser-coupler/GaN:C composite structure. **Ongoing**

4.1.3 Progress Made Since Last Report

(E) We circumvented COMSOL delays via a time domain simulation in Mathematica. Pulse broadening due to the saturable absorbing in GaN restricts the switch times to over 2 ns in devices of 3 cm in length (in an initial, not optimized, coupler design).

4.1.4 Technical Results

(B) To demonstrate the ability to use the incident laser on GaN:C PCSS for direct bipolar modulation (Figure 4.1.1), testing was done at 50 V (charge voltage). An ideal on-state resistance (<1 Ω) was not achieved due to the limited available laser energy, but as expected the rise time was ~70 ps (characteristic of the neoLASE). After conversion, there was 6 μJ of 355 nm wavelength to split using a 50:50 beam splitter for the free-space optical delay setup. Normally, to get to a minimum on-state resistance, tens-of-μJ of energy are needed (depending on the gap length of the device). Future testing will be done using the higher peak power laser built by BAE and/or the wedge laser. These options will offer the ability to reach minimal on-state resistance, maximizing power output and allowing us to measure the range of RF that can be generated using this setup with GaN:C PCSS.

(E) In parallel with the COMSOL simulations of the optical mode coupler approach to excitation of the GaN:C PCSS, we constructed a model in Mathematica. At 355 nm we would have challenges interpreting the multimode response of the coupler in the frequency domain, so we chose to simplify the problem by solving the nonlinear equations in the time domain. In terms of the optics: the GaN is considered to be a saturable absorber. We normalize the pulse amplitude to the square root of the saturation power of

GaN (P_S = 255 [mW] is typical at room temp); and the time coordinate to GaN's relaxation time (T_1 = 1 [ns] is typical at room temp).

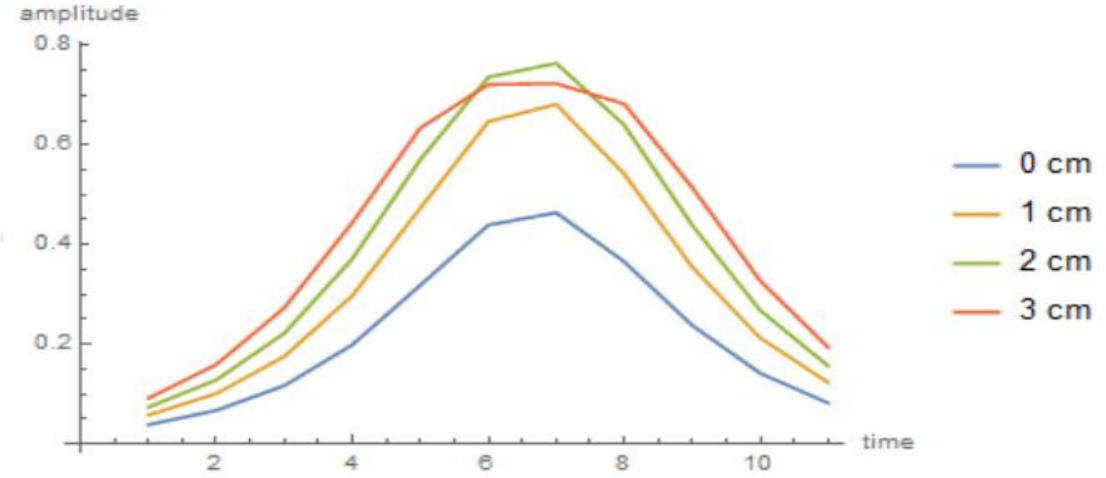


Figure 4.1.1 Evolution of an optical pulse coupled into GaN demonstrating considerable pulse flattening at a length of 3 cm.

For a particular coupler (silica glass slab at an air gap of 1 mm) we observe, in Figure 4.1.1, considerable pulse broadening and flattening at a switch length of 3 cm. We find that (without further optimization and development) this technique is not fast enough in response time to be used for switching times less than 2 ns.

4.1.5 Summary of Significant Findings and Mission Impact

(A) Towards showing direct RF modulation in the 1–2 GHz range, unipolar modulation has been demonstrated using an open-space time-optical delay using one GaN:C PCSS (lateral device with 500 μm gap length) of up to 1.2 kV charge voltage. The limiting factor to achieving higher charge voltage was flashover occurring in air-bubbles formed during curing of the Sylgard encapsulant. Previously, ~1.8 kV charge voltage was achieved using a 1 μm gap length GaN:C PCSS, so demonstration will continue using similar methods (corona-dope) to the Si-PCSS studies to achieve 2 kV+ charge voltage, with this being limited by the power supply being used to 2.5 kV.

(B) Demonstration of direct RF generation began with low-voltage (50 V charge voltage) testing to determine the feasibility of the bipolar setup and modulation. A bipolar pulse was achieved, but with high on-state resistance due to limitations in the available laser energy when using the neoLASE system. After conversion from 1064 nm to 355 nm, 6 μJ of energy was available to split into two beams for free-space optical delay. Future testing will commence using the laser sent to UMKC from BAE once that is setup.

(E) To continue towards a feasibility test of fiber coupling with GaN:C PCSS, single-mode waveguide modeling was initiated in COMSOL. This initial model will be modified to show optical fiber coupling to GaN:C PCSS.

4.2 Drift-Step Recovery Diode and Pulse Shaping Device Optimization

(Jay Eifler)

4.2.1 Problem Statement, Approach, and Context

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS but do not require a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times requires optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening device within the pulse shaping head circuit. Additional goals for pulse repetition frequency are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies. Also optimize the pulse sharpening device (PSD) within the pulse shaping head circuit.

Sub-Problem 1: TCAD and SPICE models of the DSRD are 40% accurate and must be improved. PSD models have not been developed.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetimes have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current. PSD have sharpened DSRD pulses to 100 ps-order.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power and minimum risetime, but also for low-jitter, reduced cooling, and compactness. Additionally, optimize pulser with PSD and pulse shaping head circuit.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2 cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities. DSRD and

PSD must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD and PSD modeling.

4.2.2 Tasks and Milestones / Timeline / Status

(A) Milestone – TCAD and SPICE models of the DSRD and MOSFET developed which match experimental values of both the diode and circuit within 5% accuracy [*Estimated completion by AUG21*].

1. Task – Develop baseline DSRD model in TCAD [*completed JAN–APR21*];
2. Task – Develop SPICE model of DSRD within Silvaco [*completed MAR–JUN21*];
3. Task – Develop SPICE model of MOSFET within Silvaco [*JUL–AUG21*];
4. Task – Compare results of SPICE models developed in TCAD to the simulation values achieved using LTspice and experimentally (see Section 4.5) [*JUL–AUG21*];
5. Task – Incorporate parasitic capacitance, inductance, and resistance models for both single die and DSRD diode stacks (multiple dies in series) as well as for the DSRD-based pulser circuits [*discontinued after MAR–JUN21*];

(B) Milestone – Optimal characteristics of epitaxially-grown DSRD pinpointed from parametric study which produce the maximum waveform fidelity characteristics (e.g., maximum peak voltage, shortest risetime, highest dV/dt) [*Estimated completion by AUG21*].

1. Task – Determine carrier lifetime effect on risetime [*completed FEB–APR21*];
2. Task – Determine effect of including avalanche modeling on DSRD performance [*completed FEB–MAY21*];
3. Task – Determine effect of the width of outer edge contact on current density and breakdown in device [*discontinued after MAR–MAY21*];
4. Task – Model TCAD process in Silvaco Athena and Victory Process for DSRD diffused and epitaxial processes (and pulse sharpening devices) used for DSRD fabrication and DSRD device modeling [*discontinued after MAR–JUN21*];
5. Task – Determine optimal doping profile for Semiconductor Power Technologies (SPT) DSRD epitaxial designs [*completed MAY–JUL21*];
6. Task – Determine best doping profile from fabricated and optimal conceptual designs by comparing performance in the 2x2 DSRD pulser [***completed JUL21***];
7. Task – Complete DSRD performance study on epitaxial doping profile (n-side) variation manufactured by SPT in conjunction with LSRL [***completed JUL21***];
8. Task – Complete gain study for DSRD stack height and gain staging design [***completed JUL21***];

9. Task – Verify accuracy of TCAD simulations by comparing to experiment for DSRD-based pulser circuit topologies [*JUL–AUG21*];

(C) Milestone – Pulse sharpening devices developed within TCAD which improve the risetime and peak voltage of the IES pulse generator developed in Section 4.5 [***transitioned to Section 4.7 JUL21***].

1. Task – Develop preliminary pulse sharpening devices (PSD) models within TCAD [*discontinued after DEC20*];
2. Task – Develop standard PSD models within TCAD to reproduce results from published work [*discontinued APR–JUN20*];
3. Task – PSD simulated with DSRD 3-stack for more complete DSRD-based system modeling excluding only the primary switch model [*APR–JUN20*];
4. Task – Determine current carrying capacity of PSD and DSRD stacks [*discontinued MAR–JUN21*];

4.2.3 Progress Made Since Last Report

(A.3) A MOSFET SPICE model usable in TCAD has been developed. While the tuning of the parameters to the datasheet can be further refined, current models already show an improvement over the earlier used TCAD MOSFET model, in that, the output pulses are all relatively of the same height rather than having a higher peak voltage for the first output pulse as when using the TCAD MOSFET model. Use of a SPICE MOSFET reduces the computational cost and enables simulation of DSRD 2x2 pulsers with higher stack heights. In addition, the SPICE MOSFET models can be tuned to fit the datasheet, while TCAD MOSFET models can also be tuned to fit a datasheet the method to do so is not clear or already published.

(B.6) A doping profile performance comparison has been made for the existing designs of SPT and LLNL and conceptual doping designs using exponential and error function profiles. Exponential profiles had the best overall performance as shown in earlier studies where the comparison was not as direct.

(B.7) Epitaxial doping profiles for DSRD are currently being fabricated and SRP data for the n-side has arrived. An assessment of the performance of the real SRP with its deviations from the ideal exponential profile was made using TCAD. This study showed that the deviations in epitaxy did not alter the performance significantly.

(B.8) A TCAD study of the stack height effect on gain was made where variations in prime voltage supply and stack height had not been made in earlier studies. 7- and 13- stacks of DSRD showed the highest gain with the 7-stack having slightly higher gain. However, the peak voltage obtained was higher for 13-stacks and is important when this is the main concern. Gain per single dies within a DSRD stack was also assessed and showed 1-stacks or single DSRD have the best gain per singles used in a stack, which shows as DSRD stack height increases, the gain drops (with 1-, 7-, 13- and 26-stacks studied). Future studies can include DSRD area and thickness, along with variations in the secondary voltage supplies

and trigger duration, to assess gain and its impact on the design of pulser systems using gain staging. We want to answer the question of what stack heights should be manufactured for designing optimal DSRD pulser systems, here advantages have been shown for all the stack heights.

4.2.4 Technical Results

(A.3) The original MOSFET primary switch model used was a voltage-controlled resistor, which serves as a reasonable approximation of a MOSFET but does not accurately reproduce the correct voltage and current relationship of a MOSFET. As an improved MOSFET model available in TCAD, a TCAD MOSFET model was used which better modeled MOSFET action than the voltage-controlled resistor model. Initial study showed the TCAD MOSFET model did not match the datasheet [1] of the MOSFET used in DSRD pulser experiments. A SPICE MOSFET model in TCAD is desirable both for matching the datasheet and reducing the TCAD mesh points required enabling larger DSRD stacks to be simulated. It may be possible to adjust the TCAD MOSFET model as well to match the datasheet but no prior work in the literature has been found to act as a guide. Therefore, a SPICE MOSFET model in TCAD was developed for DSRD pulser simulation.

The SPICE MOSFET model used was based on the Shichman–Hodges level 1 MOSFET model widely used [2]. But with the addition and modification of source and drain resistances and a non-linear capacitance model for the drain-source capacitance taken from [3-6]. This model did not use behavioral models, which are not available in the SPICE within TCAD, but could be developed for TCAD.

First the zero-bias voltage threshold parameter and transconductance parameter [3,4,7,8] are extracted from the transfer curve. Since the goal is to replace the CREE manufacturer LTSPICE MOSFET model with one usable in TCAD, the transfer and other curves are taken from the CREE SPICE model rather than the CREE datasheet. Note, we can compare to the datasheet and eventually extract parameters from the datasheet for modeling and comparison as well. The drain-source on-state resistance (taken at the operating point defined by the rated current) and channel length modulation parameter (λ) are also extracted according to [3,4,9]. However, λ did not match well with the values tabulated in [4] and zero is usually taken as an acceptable value since the SiC power MOSFETs are not operating in the saturation region. In addition, the length and width of the MOSFET channel are also varied to fit the MOSFET transfer and output characteristic curves. These adjustments are done in the order specified in [3,4] and iterated until a close fit between datasheet (CREE SPICE model) and developed model are obtained. In Figure 4.2.1 and Figure 4.2.2, a few iterations for a rougher match have been made for the transfer and output characteristic curves and comprise the DC portion of the model.

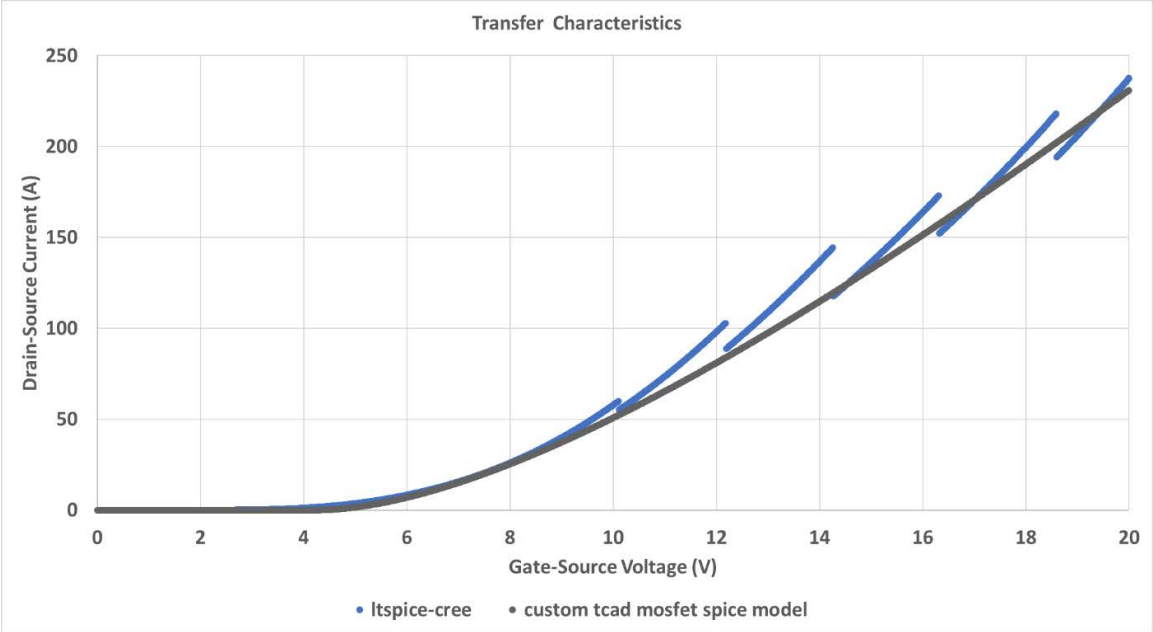


Figure 4.2.1 Transfer curve comparison for the LTSPICE-CREE (blue) and TCAD (dark gray) MOSFET SPICE models. There are discontinuities in the CREE model for gate-source voltages after about 10 V.

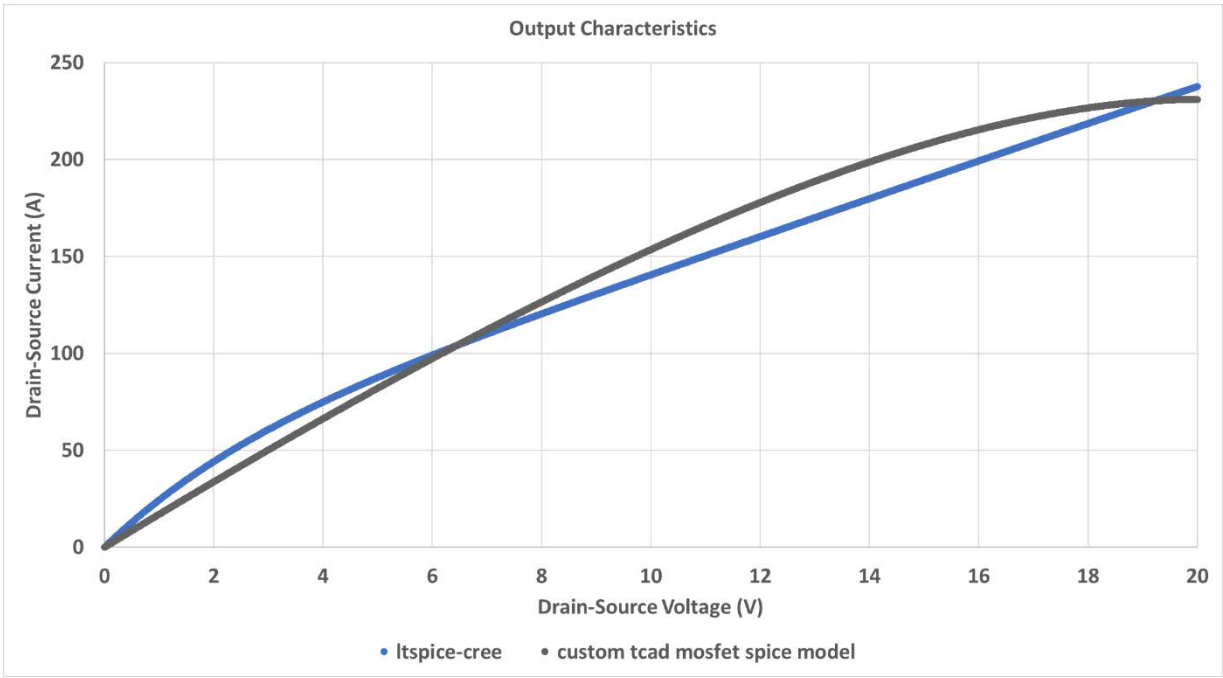


Figure 4.2.2 Output Characteristic curve comparison between CREE (blue) and TCAD (dark gray) MOSFET SPICE models.

The body diode characteristic has not been as well calibrated yet. The body diode DC part of the TCAD level 1 MOSFET model could not be turned off and had to be used which complicates the model development. In Figure 4.2.3 the comparison between the CREE and TCAD MOSFET SPICE models is shown.

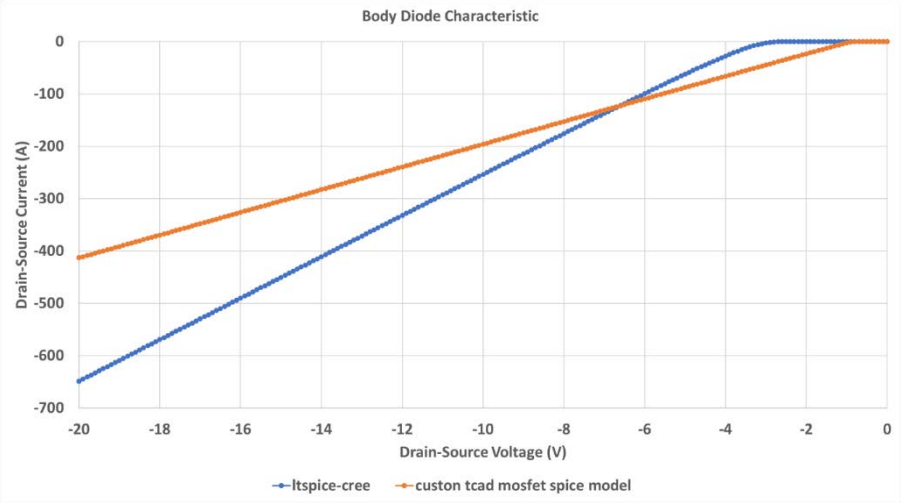


Figure 4.2.3 Body diode characteristic curve for CREE (blue) and TCAD (orange) MOSFET SPICE models. *No calibration has been performed.*

The dynamic operation of the MOSFET is modeled by the MOSFET capacitances as experimentally measured: the input capacitance (C_{iss}), the output capacitance (C_{oss}) and the reverse transfer capacitance (C_{rss}). These are decomposed into the gate-source, gate-drain, and drain-source capacitances which are not usually measured directly. For example, the gate-source capacitance is taken as constant and can be calculated from the datasheet (or CREE SPICE model output) as the average value of (C_{iss} - C_{rss}). The details of calculating the capacitances can be found in [5]. In Figure 4.2.4 is shown the MOSFET capacitances compared between the CREE and TCAD MOFET SPICE models.

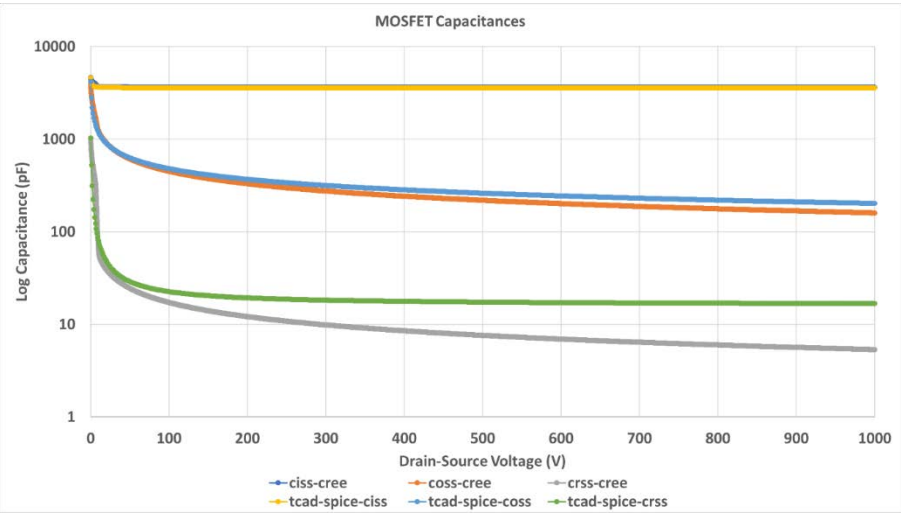
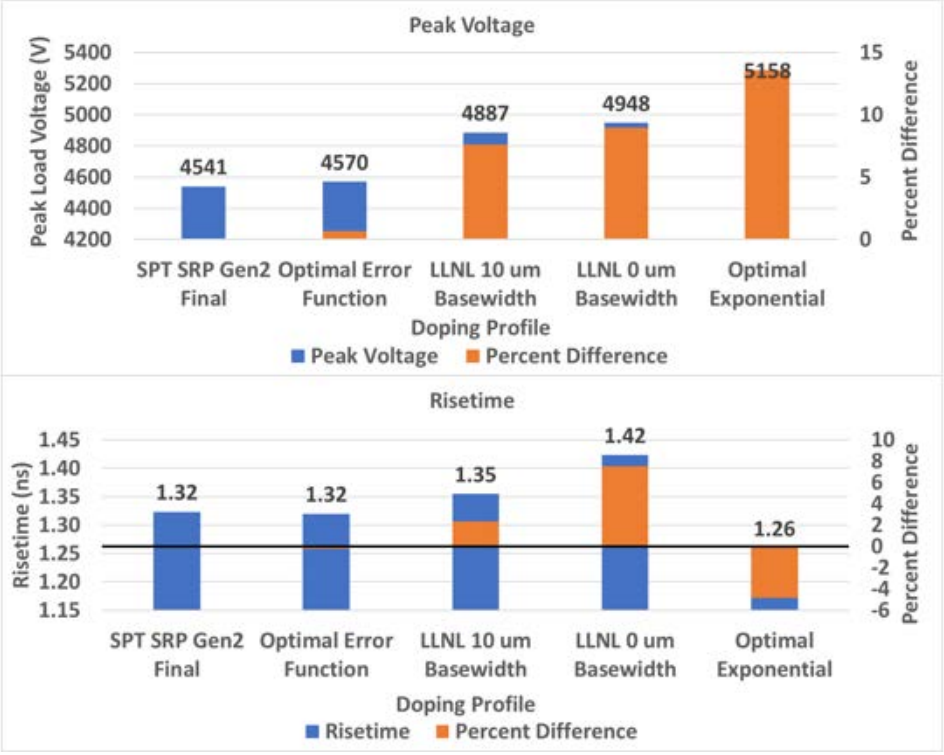


Figure 4.2.4 Comparison of MOSFET capacitances between the CREE and TCAD MOSFET SPICE models.

The new TCAD MOSFET SPICE model was used in the single and 2x2 DSRD pulsers and showed that there was no initially larger peak voltage on the first output pulse as with the TCAD MOSFET model (first larger peak voltage did not occur using the voltage-controlled resistor MOSFET model either). The simulations also run faster due to less mesh points used when SPICE modeling the MOSFET (as opposed to TCAD modeling) and the single output pulse required to characterize the pulser operation. However, modeling the gate charge and switching waveforms, switching timing and switching energy losses have not been completed and compared to the datasheets. An external gate resistor has not been added as used in experiment and can affect the gate charge and switching curves. Further model development and refinement for matching curves closely will soon be completed and tested in the DSRD pulser circuits for predictive design of the DSRD and the DSRD pulser. Initial results show as close a match as was obtained using the TCAD MOSFET of earlier. Where the TCAD MOSFET model was adjusted in width to fit results, the TCAD SPICE MOSFET model was not fit to pulser experiments but still matches reasonably well (within 10%).

(B.6) The existing doping profiles of DSRD devices from Semiconductor Power Technologies and Lawrence Livermore National Laboratory (LLNL) and exponential and error function concept doping profiles were compared for performance in TCAD simulation within the 2x2 DSRD pulser. In Figure 4.5.5 is shown the peak voltage, risetime, voltage rise-rate and gain for the doping profiles (blue) and the percent difference from the SPT SRP Gen2 Final doping profile (orange).



continued below

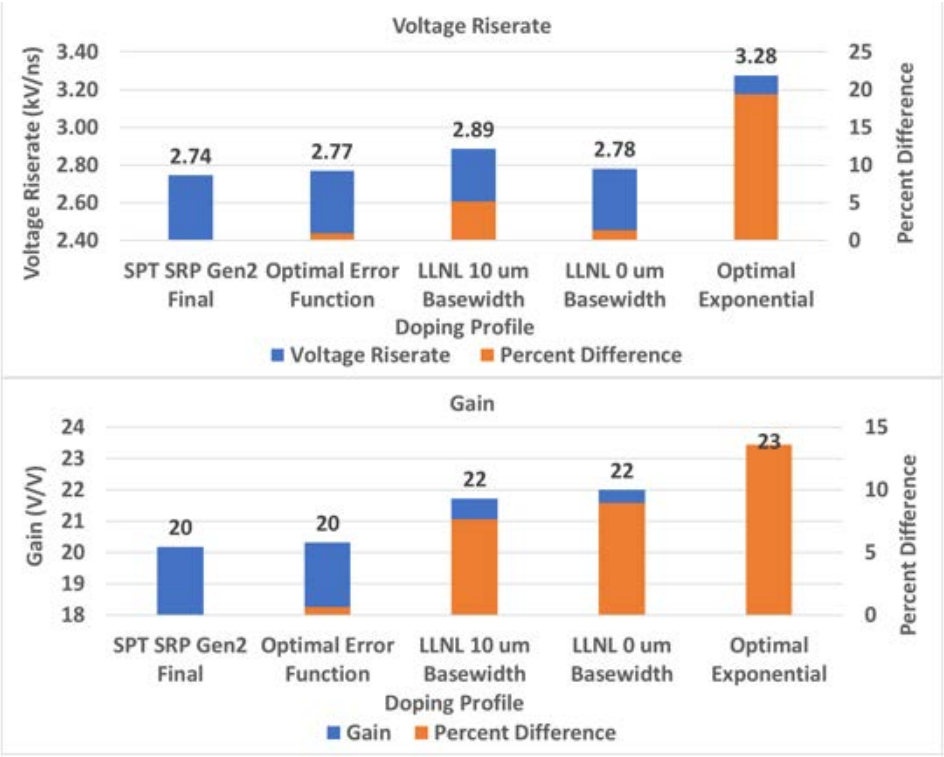


Figure 4.2.5 Doping profile performance compared in 2x2 DSRD pulser between SPT, LLNL and exponential and error function concept doping profiles with percent difference.

The optimal doping profile for the exponential doping profile performed the best overall as has been indicated by a variety of earlier simulation tests. SPT is currently overseeing the production of 25 wafers of a variety of exponential doping profiles which will be tested after fabrication of the final DSRD devices has been completed.

(B.7) SPT sent information on the n-side exponential doping profile for the DSRD epitaxial designs that showed some fluctuations from the ideal exponential curve. TCAD simulation was performed to determine the change in performance that can be expected from deviations in the exponential profile that occur in the epitaxial process. Simulations showed little difference in performance for the deviations that occur in epitaxy for the DSRD.

(B.8) A series of TCAD simulations were carried out for studying gain or peak voltage divided by the prime voltage input (in the single bar and 2x2 DSRD pulsers, see JUN 2021 Grant Report). The simulations are essentially a study of varying device geometry (stack height) and circuit inputs (prime voltage) for performance (gain). Understanding the relationship of stack height and gain is useful for gain staging design in the DSRD pulsers. Gain is a relationship between circuit input and output voltages (and is not the efficiency). In Figures 4.2.6 and 4.2.7 are shown the gain and peak voltage vs prime input voltage. In Figure 4.5.8 is shown the gain per number of dies in a stacked DSRD vs prime voltage per number of dies in a stacked DSRD.

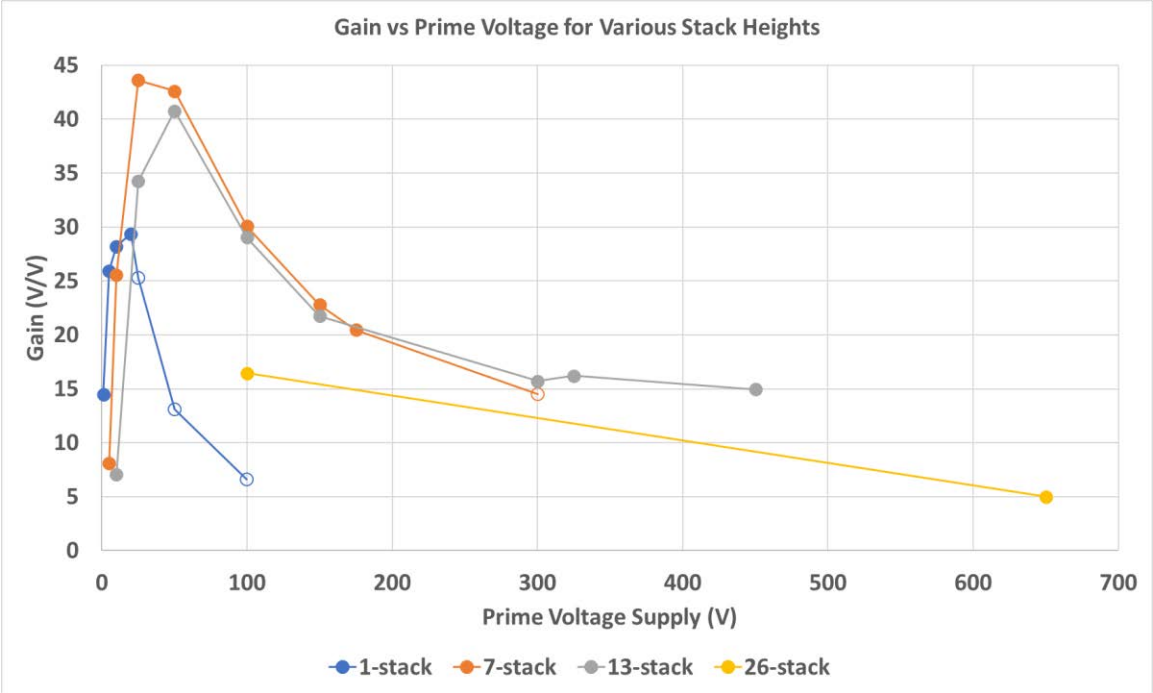


Figure 4.2.6 Gain vs prime voltage for various DSRD stack heights. Open circles indicate breakdown in the output pulse shape.

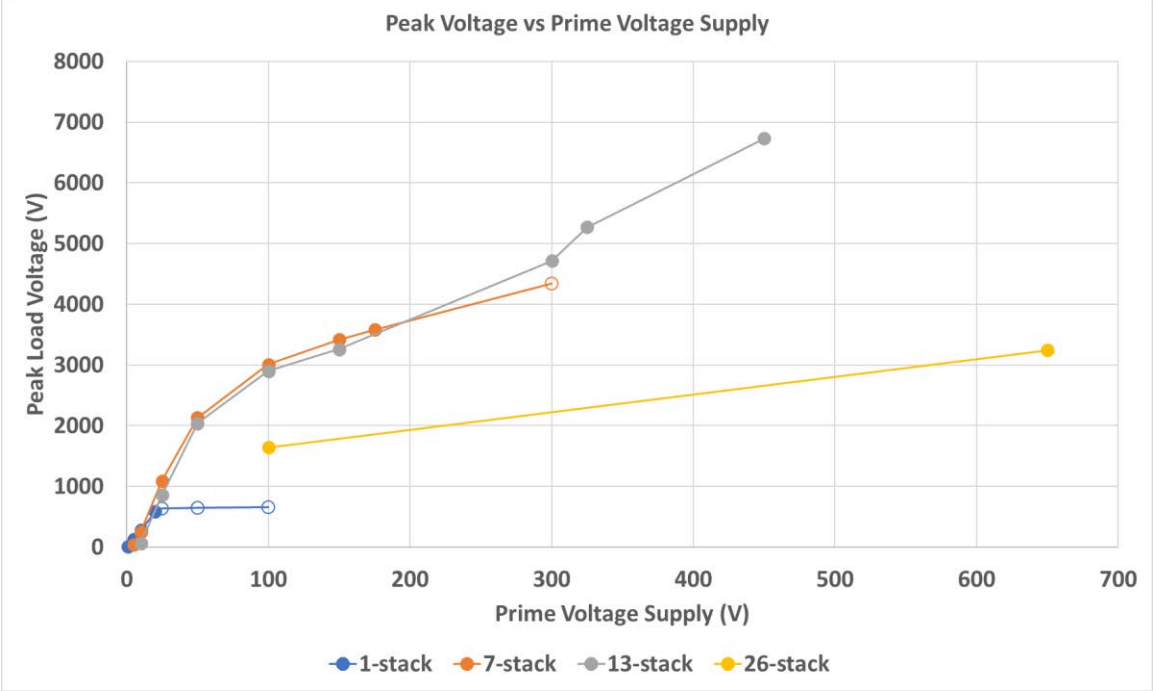


Figure 4.2.7 Peak voltage at load vs prime voltage input for various DSRD stack heights. Open circles indicate breakdown in the output pulse shape.

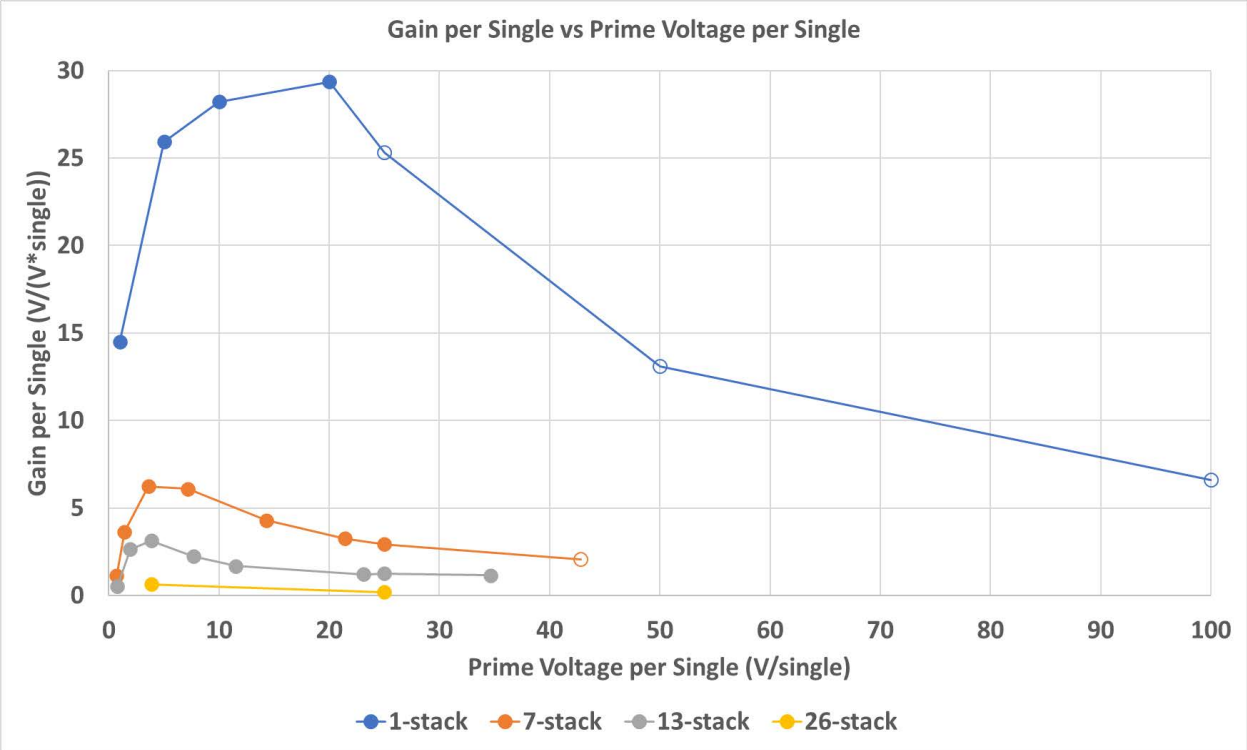


Figure 4.2.8 Gain per single vs prime voltage input per single for various DSRD stack heights. Open circles indicate breakdown in output pulse shape.

In Figure 4.2.6, the 7- and 13-stack DSRD achieve the highest gain with 7-stack having the highest. However, in Figure 4.2.7, 13-stack DSRD achieve the highest peak voltage. The 26-stack have not been simulated at a high enough prime voltage to see breakdown limiting or maximum achievable gain or peak voltage. One concern is the MOSFET drain-source peak current exceeds the rated maximum (160 A) for prime voltages about ~200V. Two MOSFETS can in theory be used to excite these higher stacks without exceeding the MOSFET maximum rated current or through the use of gain staging in DSRD pulser systems. In Figure 4.2.8, the 1-stack is shown having the highest gain per single die in the DSRD stack. Together these results are themselves not conclusive and will depend on the optimization sought for the DSRD and DSRD pulser systems.

4.2.5 Summary of Significant Findings and Mission Impact

DSRD TCAD simulation started by replicating published TCAD DSRD results and then simulating devices similar with actual in-house DSRD. The variation of the sinewave pulse voltage input magnitude and period on DSRD charge storage were collected. Charge storage timing (when the diode empties charge stored from forward pulsing) of ~50% was achievable with sufficiently long voltage input period which is necessary for maximum reverse current cutoff.

DSRD stacks, as opposed to individual die DSRD, were simulated showing reduced risetime from single die to 5-stacked DSRDs consistent with published and earlier in-house data. Series resistance to model metal resistance between DSRD in stacks and doping variability in stacks was also modeled in TCAD showing metal resistance must be

large to have an impact on peak voltage and risetime and that doping variations proportionally effect risetime.

A.1 – Accurate DSRD TCAD models have been developed that include both carrier-carrier scattering and Selberherr breakdown and are suitable for DSRD operation below the dynamic breakdown threshold. Peak voltage and risetime were limited by the breakdown model and more closely match experimental pulse data.

A.2 – Work on DSRD SPICE models has been done for the primary switch model (MOSFET) with conversion of the code to TCAD SPICE being partly completed to allow for modeling the complete DSRD-based pulser system (except driver). However, the conversion to TCAD of the MOSFET primary switch model, developed by CREE, to TCAD SPICE is complicated by having to develop custom behavioral models in TCAD SPICE which would be high-risk. Instead, a published model usable in TCAD SPICE was implemented and fit to the datasheet and then tested in a DSRD pulser simulation. The new MOSFET SPICE model usable in TCAD showed improvement in not having a first output pulse peak that was higher. This higher pulse had occurred in the TCAD MOSFET model (not SPICE model) and had not occurred in the voltage-controlled resistor MOSFET model (inaccurate). Further refinement and testing of the new MOSFET SPICE model for use in TCAD will more closely fit the published datasheet and the model can be adapted to new SiC power MOSFETS as needed.

B.1 – DSRD risetime performance was collected from TCAD simulations for variable carrier lifetime. Changes in lifetime had no significant effect on risetime other than the output pulse starting earlier.

B.2 – DSRD peak voltage and risetime were simulated in TCAD to include avalanche modeling or not. TCAD avalanche models limited peak voltage and risetime at the load over a range of voltage input magnitudes. A TCAD parameter study for DSRD stack height and DSRD area for several doping profiles with and without avalanche modeling was performed (Spring 2021 UMKC OSPRES Grant Review and Technical Exchange). The avalanche model and model parameters were also modified to account for dynamic breakdown rather than static and then compared to the no avalanche case and experimental data. From the improved avalanche modeling and TCAD parameter study, the optimal area of the DSRD can be obtained. However, for the 500 V voltage input magnitude used, the DSRD output were all in breakdown and are not predictive of non-breakdown behavior. Future studies for optimal area will include a range of voltage magnitudes to study DSRD performance and breakdown.

B.4 – TCAD process and device modeling for the development of process steps and their resultant doping profiles and device operation was begun. This modeling will enable a connection between the fabrication parameters and the device operation for DSRD (and PSD).

B.5 – Exponential doping profiles were shown (via TCAD) to outperform Gaussian and error function profiles slightly. Exponential profiles have an optimal minimum doping of 5×10^{13}–$1x10^{14}$ dopant atoms/cm^3, while Gaussian and error function profiles have an optimal minimum doping of 1×10^{13}-5×10^{13} dopant atoms/cm^3. Further exponential doping parameter studies were carried out in circuits A and B of Figure 4.2.1 (see JUN 2021

Grant Report) which included a broader doping parameter space for minimum doping, junction placement, basewidth and peak doping over a wider range of voltage input magnitudes (for breakdown limitations). The results are similar to before and show the optimally performing doping profile has a minimum doping of 5×10^{13}, no basewidth, junction placement of 95 µm, and peak doping of 1×10^{18} (p-side) and 1×10^{19} (n-side) dopant atoms/cm^3. A comparison was made for the optimal exponential doping profiles to optimal error function, LLNL and SPT DSRD designs within the 2x2 DSRD pulser system. The TCAD study showed the exponential doping profile performs the best overall when considering peak voltage, risetime, voltage riserate, maximum reverse current, FWHM pulsewidth, prepulse and gain. Epitaxy designs with realistic deviations from the ideal exponential profile from the SRP data were shown in TCAD to not significantly affect the performance.

B.7 – A more complete gain study for varying prime voltage input and stack height was completed. The results show a variety of considerations must be made for determining the better stack heights to use in DSRD pulsers. The design of the pulsers can be improved when considering the gain staging in multi-staged DSRD pulsers as caused by the DSRD stack heights used. The 7- and 13-stacks showed the best gain. However, the peak voltages were best for the 13-stack while the 26-stack required unrealistic MOSFET currents to achieve its maximal peak voltage (or gain). For gain per die within a DSRD stack, 1-stacks showed the best gain per single and showed that gain 'efficiency' drops with stack height. Still, higher 7- and 13-stacks had the highest gain. How best to use this new data for DSRD pulsers is under discussion.

C.1 – Pulse sharpening has been verified for PSD devices for the standard design and another non-conventional design. The PSD was also modeled within a DSRD-based pulser circuit combining for the first time TCAD modeling of both DSRD and PSD together within the same circuit with only the primary switch model not included.

E – DSRD pulser circuits for the single-bar (Circuit B of Figure 4.2.1) and 2x2 (circuit C of Figure 4.2.1) have been simulated within TCAD allowing the use of a TCAD DSRD model, whereas in SPICE no accurate DSRD SPICE model is available. Currently, the primary switch MOSFET is modeled in TCAD, as well, but SPICE models can also be developed for the SPICE within TCAD as and will allow for better use of computational resources within TCAD. The MOSFET model and pulse repetition are being studied in detail to more closely match experiment and TCAD.

4.2.6 References

[1] CREE C2M0045170P Silicon Carbide Power MOSFET C2M MOSFET Technology N-Channel Enhancement Mode, Datasheet Rev. 04-2018, 2018.

[2] Shichman, Harold, and David A. Hodges. "Modeling and simulation of insulated-gate field-effect transistor switching circuits." IEEE Journal of Solid-State Circuits 3, no. 3 (1968): 285-289.

[3] Arribas, Alejandro Pozo, Fei Shang, Mahesh Krishnamurthy, and Krishna Shenai. "Simple and accurate circuit simulation model for SiC power MOSFETs." IEEE Transactions on Electron Devices 62, no. 2 (2015): 449-457.

[4] Arribas, Alejandro Pozo, Mahesh Krishnamurthy, and Krishna Shenai. "A simple and accurate circuit simulation model for high-voltage SiC power MOSFETs." ECS Transactions 64, no. 7 (2014): 99.

[5] Hendrik Jan Zwerver, 'LTspice built in VDMOS model', 04 Dec 2006. http://www.magma.ca/~legg/SR5/LTspice_built_in_VDMOS_model.pdf

[6] Hegglun, Ian, 'VDMOS parameter extraction', 20 Aug 2020, version 3.

[7] Ortiz-Conde, Adelmo, FJ Garcıa Sánchez, Juin J. Liou, Antonio Cerdeira, Magali Estrada, and Y. Yue. "A review of recent MOSFET threshold voltage extraction methods." Microelectronics reliability 42, no. 4-5 (2002): 583-596.

[8] Ortiz-Conde, Adelmo, Francisco J. García-Sánchez, Juan Muci, Alberto Terán Barrios, Juin J. Liou, and Ching-Sung Ho. "Revisiting MOSFET threshold voltage extraction methods." Microelectronics Reliability 53, no. 1 (2013): 90-104.

[9] Alhalabi, Marah, Abdelrahman Rashed, Nusrat Binte Iqbal, and Anas Al Tarabsheh. "Modelling of SiC Power MOSFET in Matlab, Simulink, and LTSpice." In 2018 IEEE International Conference on Environment and Electrical Engineering and 2018 IEEE Industrial and Commercial Power Systems Europe (EEEIC/I&CPS Europe), pp. 1-6. IEEE, 2018.

4.3 Pioneering Drift-Step Recovery Diode Processing and Manufacturing

(Alex Usenko)

4.3.1 Problem Statement, Approach, and Context

Primary Problem: Since Boff, Moll, and Shen's discovery of the high-speed switching effect inherent in initially forward-biased solid-state diodes that are suddenly reverse-biased in 1960 [1]; DSRD's (as termed by Grekhov and Kardo-Syseov in 1985 [2]) performance has not increased as their deep-diffusion manufacturing process remains the same as it was over 60 years ago. Albeit new pulse generator topologies which utilize IES diodes like DSRDs, i.e., SOS diodes (termed by Rukin in 1992 [3]) have shown improvement at circuit level given they operate under a higher direct-current density compared to that of DSRD-based pulsers – the voltage-to-risetime, dV/dt, of these silicon-based solid-state IES diodes remain on the order of 10^{12} V/s. Furthermore, all possible ways to improve pulse performance of DSRD made by deep diffusion have been extensively investigated and exhausted. To achieve the 10^{13} V/s (10 kV/ns) voltage-to-risetime required by an all-solid-state HPM pulse generation utilized to support of the Naval afloat mission, improving DSRD manufacturing techniques must ensue.

Solution Space: Leverage applicable concepts from mainstream silicon wafer industry and apply new/novel manufacturing methods to DSRD processing. Viable options which have improved the performance of silicon wafers include the following:

1. Anisotropic etch (borrowed from MEMS industry) – to mitigate the problem of side-wall passivation/insulation of DSRD dies.
2. 3D wafer level packaging: SLID wafer bonding (from more-than-Moore) – during process for stacking DSRD dies. For the first time, stacking is on wafer level, not on die level.
3. Porous silicon growth (from MEMS sensor industry) – to passivate side walls of DSRD at room temperature.
4. Fluorinated Silicon dioxide deposition from liquid at room temperature – towards passivating silicon surfaces in already metallized DSRD dies.

5. Replacing starting wafers. Small FZ (float zone) silicon wafers, traditionally used in power devices industry, will be replaced with 200 mm mainstream Cz (Czochralski) wafers. This would enable a highly automated 200 mm silicon production lines, SPC (statistical process control) use, etc., resulting in a higher yield and tight distribution in DSRD specs.
6. Wafer bonding using newest EVG Gmbh bonder – ComBond. This allows to replace drive-in diffusion by out-diffusion thus allowing use of slip resistant Cz wafers with high oxygen content instead of FZ wafers.
7. Minimize parasitics by press-pack. Replace home-made packaging by inserting silicon diode stacked die into SOTA press-pack kit used in power semiconductor industry.

The necessity driving each of these seven solution space concepts is briefed in the following four sub-problems discussed hereafter.

Sub-Problem 1 – Diode stack sidewall insulation/passivation: The present SOTA is represented in Figure 4.3.1 where a 26-stack DSRD die is shown. The diode possesses a polymer coating which was initially applied manually onto the sidewall of the diode.

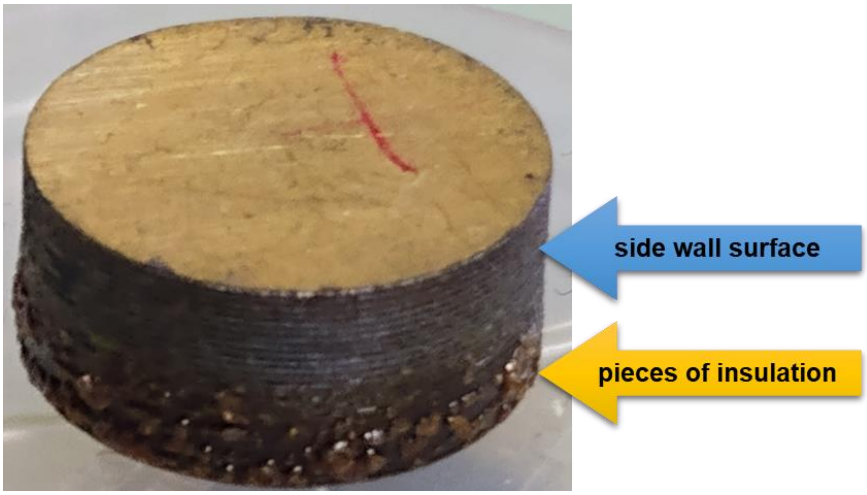


Figure 4.3.1. Image of 26-stack DSRD die produced by LLNL.

During diode operation, heating causes degrading of the coating, and only pieces of the original passivant coating remain intact on the sidewall's surface. Diode breakdown voltage is unstable and drops during diode operation in pulser circuit. Moreover, even the freshly applied coating is not an ideal passivation. The best passivation for silicon surface known is thermal oxide grown on the surface. However, the diode already has metallization layers on top and bottom of the stack as is evident in Figure 4.3.1. Therefore, it cannot be thermally processed at oxidation temperatures > 800°C. Therefore, the side wall passivation issue must be solved to achieve higher hold-off voltages which are closer to theoretical breakdown voltage limit.

The breakdown voltage is controlled by depletion depth of the diode. The minimum depletion depth is determined by electrical breakdown field. For silicon it is 3x10E5 V/cm, i.e., every micron can holdoff 30 Volts. Mathematically, to withstand 1000 V this dictates

a minimum of 33 microns is needed. However, in the applied power semiconductor industry a 3X margin is added. Therefore, to make 1000 V rated diode, it must have 100-micron wide depletion region. Justification to add this factor of three margin is that the manufacturing processing is not ideal, and there are always weak points where the surfaces are typically the weakest areas and points of failure. Should this process be perfected a 33-micron thick diode will then become be at least 3X faster in switching speed. Solving the side passivation problem will allow to approach silicon theoretical limit 3x10E5 V/cm and thus triple the pulse rise-rate performance.

Sub-Problem 2 – Deep diffusion technology restricts optimization of doping profile: Consistent with the diode shown in Figure 4.3.1, present SOTA DSRDs are manufactured using deep diffusion technology exclusively; a technology which is extremely limited in its ability to produce an optimal doping profile. This limitation stems from allows only one doping profile, the erfc function, which gives rise to diffusion tails being present on the p-type and n-type sides of the diode. To visualize the doping profile and the diffusion tails present, Figure 4.3.2 (A) from [3] and Figure 4.3.2 (B–C) from [6] are provided.

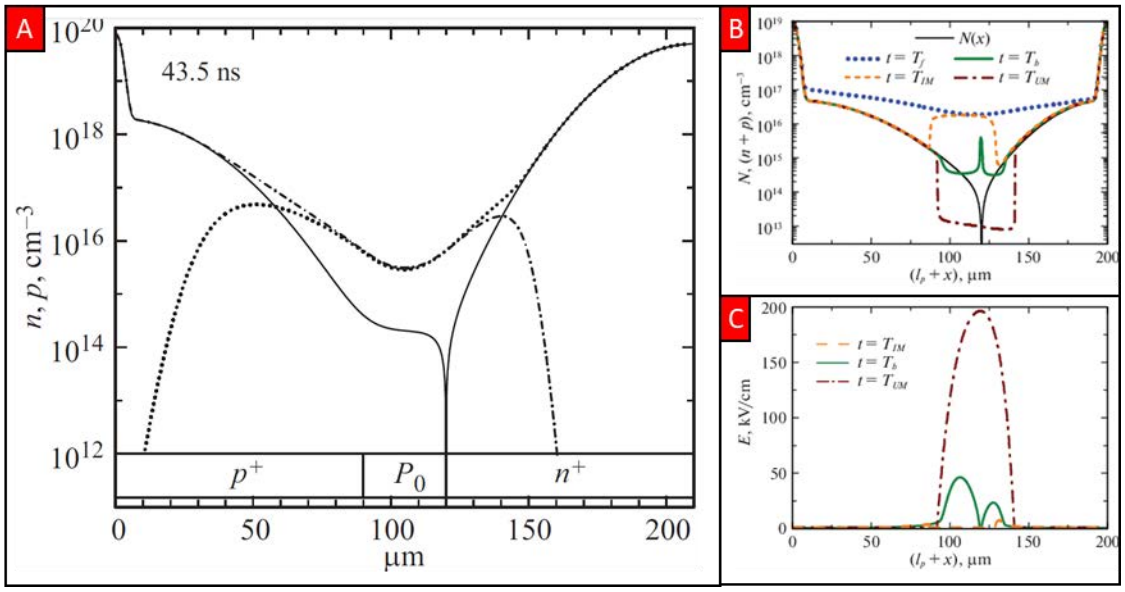


Figure 4.3.2. (A) SOTA doping profile used for deep diffusion obtained from [3]; (B) SOTA doping profile obtained from [6]; (C) Resulting electric field distribution within diode produced from [6].

Between the diffusion tails there is a flat doping region where the doping concentration level is equal to the starting wafer's base carrier concertation. Notice, if we assume an intrinsic (totally non-doped) starting wafer, and extrapolate towards the diffusion tails, the tail ends will meet at the p-n junction location (i.e., the optimum point). Should the deep diffusion process remain the SOTA manufacturing process, nothing else can be modified/optimized.

Somehow over the last 60 years the SOTA has remained as deep diffusion technology. Literature has shown that an Israeli group published papers using epitaxy to form doping profile [4]. Though, the group uses the simplest flat doping concentration 25-micron thick

epi film, i.e., abrupt junction. Simulations show that the abrupt junction is not the optimal profile for the DSRD (described in detail in Section 4.2). Even though the epitaxial process is not restricted in the profile optimization and allows the manufactures complete freedom in designing the profile, optimization of the doping profile remained amiss prior to Section 4.2's findings presented. It should be noted that there are also publications/patents where DSRDs are manufactured from materials other than silicon. However, this project is directed toward silicon-based DSRD, thus optimization of the diodes performances is not compared to SiC-, GaAs-, or GaN-based DSRDs.

Sub-Problem 3 – Stacking of DSRD dies: Typically, peak voltage requirements for a DSRD pulser is on the order of ones to tens of kilovolts. However, the breakdown voltage of single diode is limited to about 1 kV; a property intrinsic of silicon. Thus, to achieve the required pulser voltage the individual diodes must be connected in serial. This can be done by connecting the dies by wires, however doing so results in the generation of very high parasitics added to the circuit. The addition of parasitic inductance and capacitance would result in the pulse front to lose its sharpness. Pulse fronts must be as sharp as possible. For example, 1 ns long pulse rise time is about equal to 1st harmonic frequency 1 GHz. As is the case with any high frequency device, every piece of open wire act as an antenna emitting radiofrequency power. In terms of parasitic elements of a circuit, this is equal to adding inductive, capacitive, and resistive elements to an equivalent circuit; a result which further complicates the already complex TCAD and LTspice simulations and would otherwise render diode and pulser evaluation and optimization problematic.

To minimize parasitic elements connecting wires must be excluded. Even coaxial cable (absent of the antenna effect) brings excess parasitics into the circuit. The conclusion is made that the individual diodes must be stacked. In the present SOTA, stacking is performer by soldering, eutectic bonding, "loose stack" (kept by mechanical pressure), gluing by conductive polymer, even fusion bonding [5].

No one of these approaches is efficient nor sufficient to solve the problem. For soldering, gluing, and eutectic approaches, say, solder is pushed out from space between silicon dies and causes shorts at side edge surfaces. Fusion bonding suffer from cross autodoping p- an n-dopants, thus adding parasitic resistance.

Still, the monolith design is attractive for potential minimum parasitics.

Sub-Problem 4 – Packaging of stacked dies: Also present in the SOTA is the use of press-pack (called also tablet, flat package, etc.). The press-pack package is well developed and can be found in IXYS, Infineon, Toshiba, and many other power semiconductor manufacturers. The fastest switching diodes, thyristors, IGBTs for silicon and SiC devices are also packaged this way. This type of package is widely considered in power semiconductor industry as a solution optimized for both fast switching and thermal dissipation. Examples of a press-pack package in both the disassembled and assembled form is provided in Figure 4.3.3.

The 'home-made' press-pack packaging solution will unlikely approach the SOTA's quality as millions of man-hours have been spent at power electronics device companies to develop the processing method. A more efficient approach would be to find a vendor

that manufactures all parts of the press pack, buy COTS kits, and then assemble the diode stacks into the press-pack kits to complete the packaging process in-house.

Figure 4.3.3 (A) Disassembled press-pack of diode manufactured by Westcode; (B) Isometric top view of press-pack assembled; (C) Isometric bottom view of press-pack assembled.

State-of-the-Art (SOTA): In a recently published paper (2019) from the Russian St. Petersburg team at the Ioffe institute [3] reported achieving a peak current density of 5 kA/cm^2 with a rise time of the output pulse front being ~ 2.3 ns, and the peak voltage across the load is 900 V (i.e., the peak switching power is 4.5×10^6 W/cm^2). The St. Petersburg team utilized deep diffusion technology. The team at NPO Energomodule, Moscow, Russia [6] who also use the deep diffusion method to report simulation results where a 1.35 ns rise time was achieved for ~ 1000 V peak voltage impulse. In a paper published by the team at Ekaterinburg, Russia, a voltage pulse amplitude of 540 kV with a 20%–90% rise time of ~1.2 ns corresponding to a voltage rise rate of ~0.3 MV/ns was reported. To achieve these higher performance metrics however, a deep diffusion SOS diode was used with additional dynistor pulse sharpener. Neither dynistor design nor the fabrication process described within [8].

As one can see, without additional pulse compression methods like those used in [8] which compensate for the DSRDs produced using deep diffusion, there has not been any significant improvement in DRSR pulse performance compared to pioneering work done in 1960 [1].

Deficiency in the SOTA: First, no DSRDs have been manufactured using epitaxy technology with doping profile optimization. Second, no DSRD processing method exists which integrates side passivation with silicon dioxide. Finally, an acceptable DSRD stacking process has yet to be developed.

Solution Proposed: Manufacture DSRDs within the continental United States (CONUS) using epitaxy growth process leveraging the optimal characteristics (e.g., doping profile, carrier concentration) determined through the work performed in Section 4.2 through working with industry partners at Semiconductor Power Technologies (SPT) and Livermore Semiconductor Research Laboratories (LSRL).

Relevance to OSPRES Grant Objective: DSRD manufacturing technology is a major building block of short-pulse high-peak power defense systems. Our new disruptive process flow for DSRDs enables not only manufacturing of DSRDs at scale, but within the continental United States (CONUS). In doing so we will redefine the SOTA by producing optimal DSRDs which are used within best-in-class HPM pulse generators which become part of more advanced defense systems within the Navy's arsenal of protecting the warfighter and its high-value assets.

Risks, Payoffs, and Challenges:

Risks: As the process of producing DSRDs using Epitaxial growth is both novel and uncharted territory, there is inherent risk to its success. Additionally, post-processing methods based on the discussions provided in the ***Sub-Problems*** section have yet to be matured.

Payoffs: Deep diffusion technology allows to make DSRD that use about 1/3 of theoretical silicon capabilities. Our epi DSRD expected to approach theoretical limit of silicon. 3X improvements in pulse time performance, and 3X improvement in pulse voltage magnitude are expected.

Challenges:

1. Develop process for much thicker ~ 200-micron epitaxial layers; previously 100 microns was considered as a limit for growing defect free silicon epitaxial layer.
2. Discover an optimal doping profile for DSRD and develop epitaxial recipes resulting in this profile.
3. Develop new die stacking technology that allow to achieve pulse performance close to theoretical limit.
4. Develop new silicon surface passivation technology for vertical side surface of diodes that allow to achieve pulse performance close to theoretical limit.
5. Find process integration solution (make compatible) for steps of forming p-n junction, die stacking, and side passivation.
6. Solve packaging issues to make packaged DSRD with lower than SOTA parasitics
7. Solve packaging issues limiting diode lifetime
8. Solve packaging issues related to thermal management.

4.3.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Epitaxial DSRDs produced which contain optimal exponential doping profile and carrier concentrations [*Estimated completion by AUG21*].

1. Task – Obtain quotes from potential vendors for epitaxy [*MAR—APR21*];
2. Task – Plan epitaxy split on 25 wafers through negotiations with vendors [*MAY–JUL21*];
3. Task – DSRD stack epitaxy on 25 wafers, split on all… [*JUN–AUG21*];

(B) Milestone – Processing techniques able to manufacture loose-stack press-pack DSRDs from epitaxial wafers [*on hold until Milestone A is completed*].

4.3.3 Progress Made Since Last Report

(A.1) Lawrence Semiconductor Research Laboratory selected as epitaxy vendor to produce 25 wafers with 10 sets of 7-stack diodes per wafer.

(A.2) New approach to sidewall passivation investigated.

4.3.4 Technical Results

(A.1) 2nd and 3rd generation DSRD lots have been started. Both based on epitaxy (1st generation was based on old deep diffusion technology.

2nd and 3rd epitaxy 'runs' (i.e., manufacturing processes) ongoing. Both are at the final stage and near completing epitaxy step. 2nd run uses epi vendor SVM (Silicon Valley Microelectronics, Inc.) where doping profile used are similar to those of deep diffusion. 3rd run uses epi vendor LSRL (Lawrence Semiconductor Research Laboratory) and doping profile is best-predicted-by-simulation (exponential).

Upon receiving wafer lots from epi vendors, diode fabrication will continue for metallization, cutting into individual dies, stacking of dies, and side wall passivation. Finished DSRD stacks will be tested on static and pulse performances.

Some wafers from 2nd and 3rd generation lots will be processed using new techniques that were recently suggested: (1) side wall passivation by fluorinated SiO2 deposited at room temperature; (2) side wall passivation by staining in HF/HNO3 1:1000 mixture; (3) stacking on wafer level using SLID wafer bonding process; (4) side insulation of individual diodes by etched V-grooves and thermal oxidation.

IP disclosure and provisional patent application [10] have been filed on one of 4 new techniques. Rest 3 will be filed in next reporting period.

4.3.5 Summary of Significant Findings and Mission Impact

(A) Technical feasibility analyzed: can we switch from 60-years old deep diffusion DSRD process to epitaxy-based process? Rigorously analyzed with analytical and simulation approaches. Decision made to concentrate on the new epitaxy process.

Vendors successfully found to outsource epitaxy process. Doping profiles of p-n junctions negotiated with the vendors. Quotes for processing obtained. Orders for epitaxy placed. SRP (spreading resistance profiles) on test wafers analyzed. Working with vendors, epitaxy processing recipes developed. All wafers processed, waiting for shipment.

New process integration scheme suggested. It combines side diode insulation by anisotropic V-groove etch Figure. 4.3.4 and thermal SiO2 and stacking on wafer level instead of die level Figure 4.3.5. This scheme will be implemented on ongoing 3rd generation DSRD run.

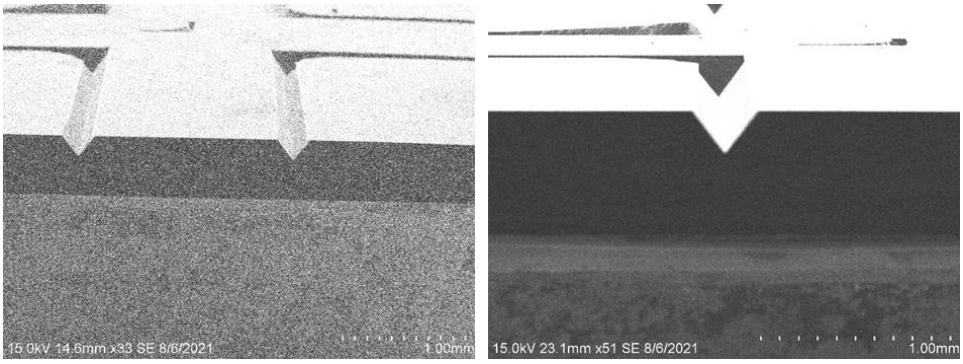


Figure 4.3.4. Side insulation by anisotropic groove etch. Technical feasibility ran on blanket wafer.

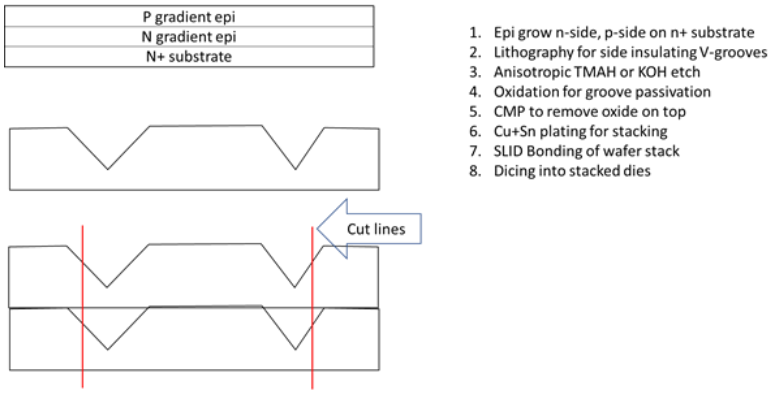


Figure 4.3.5. Process integration scheme.

2 new processes suggested for diode side wall passivation – staining, and liquid phase SiO2 deposition, both room temperature. Experimental setups for both processes have been built. Short loop runs on blanket wafers to prove technical feasibility planned. Experiment on staining in HF/HNO3 finished. Results show that near 1-micron thick SiO2 film is successfully grown. Experiment on SiO2 deposition from liquid phase is ongoing.

New DSRD fabrication process based on out-diffusion of dopants and wafer bonding is suggested. Experiment planned and ongoing. Vendors for out-diffusion – THAT Corp. and SVM Inc., and vendor for wafer bonding – EV Group chosen.

Quotes requested. IP disclosure filed. Provisional patent application filed with USPTO. Abstract [9] describing the process flow submitted to upcoming Pulsed Power Conference.

4.3.6 References

[1] Boff, A., J. Moll, and R. Shen. "A new high-speed effect in solid-state diodes." in 1960 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, vol. 3, pp. 50-51. IEEE, 1960

[2] Grekhov, I. V., V. M. Efanov, A. F. Kardo-Sysoev, and S. V. Shenderey. "Power drift step recovery diodes (DSRD)." Solid-State Electronics 28, no. 6 (1985): 597-599.

[3] Lyublinsky, A. G., E. I. Belyakova, and I. V. Grekhov. "Numerical and Experimental Study of an Optimized p-SOS Diode." Technical Physics 64, no. 3 (2019): 373-379.

[4] Люблинский, А. Г., Е. И. Белякова, and И. В. Грехов. "Численное и экспериментальное исследования оптимизированного p-SOS-диода." Журнал технической физики 89, no. 3 (2019): 409-415.

[5] Kesar, Amit S., Yaakov Sharabani, Inbar Shafir, Shoval Zoran, and Ariel Sher. "Characterization of a drift-step-recovery diode based on all epi-Si growth." IEEE Transactions on Plasma Science 44, no. 10 (2016): 2424-2428.

[6] Voss, Lars F., and Adam M. Conway. "Tunnel drift step recovery diode." U.S. Patent Application 17/081,902, filed April 29, 2021.

[7] Kyuregyan, A. S. "High-Voltage Diffused Step Recovery Diodes: I. Numerical Simulation." Semiconductors 53, no. 7 (2019): 962-968.

[8] Rukin, S. N. "Pulsed power technology based on semiconductor opening switches: A review." Review of Scientific Instruments 91, no. 1 (2020): 011501.

[9] S. V. Korotkov, Yu. V. Aristov, V. B. Voronkov, and D. A. Korotkov, “Studying dynistor switches with nanosecond switching times,” Instrum. Exp. Tech. 57, 437–442 (2014).

[10] Alex Usenko, Anthony Caruso, Steven Bellinger “New Paradigm on Making Semiconductor Opening Switches for Pulsed Power” abstract #456, 23th IEEE Pulsed Power Conference 12-16 December, 2021, Denver, CO

[11] A.Usenko, DIODE AND METHOD OF MAKING THE SAME, US Provisional Patent Application 63/216550 filed 06/30/2021.

4.4 Characterization of SOS Diode Performance through DOE Augmentation

(Megan Hyde)

4.4.1 Problem Statement, Approach, and Context

Primary Problem: Disagreements exist between simulation and experimental data produced by the IES pulse generator utilizing DSRDs. Diodes, which are manufactured like those from Section 4.3, may contain less-than-ideal characteristics, e.g., deviations from the ideal doping profile and carrier concentration, as described in Section 4.2. This problem is magnified by non-existent experimental assessment and optimization at the diode level by means of a holistic evaluation network which ties the diode’s performance back to both the simulated models and to the pulser’s performance.

Solution Space: Developing a holistic evaluating network through augmenting the design of experiment (DOE) and predictive analytics to assess the shot-to-lifespan performance of DSRDs, beginning from diode modeling/simulation and ending with pulser generation, entails pinpointing the causal relationship of each 'tunable' parameter to achieve optimal peak voltage and rise times. Understanding these causal relationships requires, (1) establishing a standardized characteristic testing procedure, (2) experimental evaluation of various/varying diodes, and (3) using statistical analysis methodologies to establish key performance indicators (KPI). Investigating these three intertwined relationships enables soup-to-nuts correlation of diode characteristics to the pulser's performance.

***Sub-Problem 1*:** It is not yet understood how altering, or deviation from the ideal, diode parameters influence performance of the diodes due to unstandardized testing procedures.

Sub-Problem 2: A cohesive, standardized method for correlating the diode's KPIs to both the DSRD-based IES pulser generator's performance and to the simulation models does not exist.

Sub-Problem 3: The non-linear separable data generated from the DOE is too complex to leverage traditional data analytics.

State-of-the-Art (SOTA): IES diodes are characterized by their reverse recovery time (RRT), forward and reverse IV, and zero bias capacitance (CV) curve tracing. These measurements are standard for diode testing and can all be characterized using a Keysight B1500A Semiconductor Device Parameter Analyzer.

Deficiency in the SOTA: Standalone performance metrics for IES diodes (e.g., DSRDs) are non-existent – which are available for more common COTS diodes (e.g., Zener, Schottky, FERD) from manufacturer's datasheets – that contain all testing and performance specifications relevant to a specific component. This leads to a difficulty in correlating the performance of a diode, or stack of diodes, to be utilized within a pulse generating circuit.

Solution Proposed: Develop a holistic evaluation network to characterize the KPIs of IES diodes. This network will include augmentation of a DOE to improve analytical correlation capabilities towards uncovering causal relationships between the diodes, the pulser's performance, and simulated results achieved. Machine learning will be used as the primary decision-making tool for augmenting the DOE. Once the network is established, it will be used to outline the optimal parameters for stacks of DSRDs within an IES pulse generator.

Relevance to OSPRES Grant Objective: Bridging the gap between the theoretical and the physical performance of these IES diodes enables closing the gap between a low fidelity TRL3 breadboard pulse generation system, to one which is at high fidelity TRL4 prototype level. At the TRL4 level, the DSRD-IES pulse generator system would be sufficient to replace the costly laser-based Si-PCSS HPM generator without compromise to scalability and the KPI required to support the Naval afloat mission.

Risks, Payoffs, and Challenges:

Risks: The results of the simulation models from Section 4.2 and the IES pulser results from Section 4.6 may not produce corresponding results (*post hoc* augmentation) leaving unknown KPIs to remain amiss; KPIs which are necessary to correlate the statistically significant experimental results to those of the of the model(s) simulated.

Payoffs: A holistic evaluation network of the diode's KPIs will be developed which links the entire modeling/simulation, fabrication process, and IES pulser's outputs; a robust assessment policy which has not yet been published within the literature.

Challenges: Traditional predictive analytics will be difficult to correlate with the augmented DOE due to the large volume of data. Machine learning is expected to assist with decision making processes for the DOE, but only if the proper KPIs have been established and good data has been used to train the machine learning model.

4.4.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Preliminary DOE and SOP for identifying KPIs of IES diodes established [*estimated completion by DEC21*].

4. Task – Ascertain current KPIs used to optimize diodes simulated, manufactured, and utilized (from Sections 4.2–6) [*JUN–AUG21*];
5. Task – Construct preliminary experimental evaluation network (DOE) using Minitab to acquire data on all KPIs based on Task 1 [*AUG–SEP21*];
1. Task – Leverage existing Python script to process legacy diodes' KPI data [*AUG—SEP21*];
2. Task – Develop/review new/existing SOPs for experimental testing apparatuses used to evaluate individual KPIs and assess their aptness [*AUG–OCT21*];
3. Task – Identify gaps/deficiencies in legacy KPI data, evaluate existing theoretical relationships to bridge gap and minimize DOE if possible [*SEP–OCT21*];
4. Task – Using SOPs developed in Task 4, acquire experimental data from legacy DSRDs, refine SOP(s) *pro re nata* [*SEP–OCT21*];
5. Task – Assess the repeatability and reproducibility of legacy data acquired following the SOPs [*AUG–OCT21*];
6. Task – Begin training machine learning model with legacy data to determine statistical correlations and significance of KPIs, and their interdependent relationships [*OCT–DEC21*];

(B) Milestone – DOE facilitates preliminary evaluation of IES diode's performance governed by the SOPs developed [*on hold until Milestone A is completed*].

1. Task – Report findings to SOS-IES sub-team members, augment DOE to include previously unidentified yet relevant KPIs based on new findings [*Est. Spring22*];
2. Task – Acquire data on newly manufactured Epitaxial DSRDs from Section 4.3 using refined SOPs from Milestone A [*Est. Spring22*];

3. Task – Correlate KPIs to TCAD simulation model, manufactured diode characteristics, and 'M×N' IES pulser's performance to aid in simulation model development, fabrication procedures, and circuit topology development [*Est. Spring22*];

(C) Milestone – SOS diode network evaluation [*on hold until Milestone B is completed*].

1. Task – Refine Python script to incorporate new correlations based on findings from Milestone's A&B [*Est. Fall22*];
2. Task – Amend ML training model with data acquired on new DSRDs (as characterized by Sections 4.2-3) to investigate statistical correlation of diode performance [*Est. Summer22*];
3. Task – Work with TCAD simulation team to address discrepancies between the DSRD's performance obtained experimentally, and that achieved within simulations [*Est. Summer22*];
4. Task – Collaborate with DSRD manufacturing team to address discrepancies between the DSRD's characteristics evaluated experimentally, and that desired by manufacturing process [*Est. Summer22*];
5. Task – Investigate relationships between statistical significance of individual diode KPIs to the peak performance of the IES pulser with the pulse generator team. [*Est. Summer22*];
6. Task – Incorporate findings from Tasks 1-5 into ML model, pinpoint KPI correlations of interest, and provide recommendations to IES sub-teams accordingly [*Est. Summer22*];

(D) Milestone – SOS diode network evaluation [*on hold until Milestone C is completed*].

1. Task – Augment DOE network to streamline diode evaluation and identify checkpoints/gates within simulation, manufacturing, and circuit development process to ensure optimal diodes are selected and utilized to produced robust high-fidelity IES pulse generator prototypes [*Est. Fall22*];

4.4.3 Progress Made Since Last Report

(A.1) Identification of key performance indicators (i.e., relevant performance metrics) from those obtained from simulation models, used in manufacturing of the diodes, those used in circuit simulations and experimental evaluations, have been established in a KPI Matrix.

(A.2) Awaiting Minitab installation to begin preliminary KPI evaluation of legacy data.

(A.3) Familiarization with Python data processing script in progress.

(A.4) Reviewed existing SOPs developed for diode characterization measurements. Determined possible points of variation within testing procedure.

4.4.4 Technical Results

(A.1) Figure 4.4.1 shows the proposed roadmap to evaluate the reliability and repeatability of the current measurement processes. This initial evaluation will be important to determine the precision and bias of the legacy data and, therefore, will be a key metric to measure the reproducibility of any new or revised SOPs.

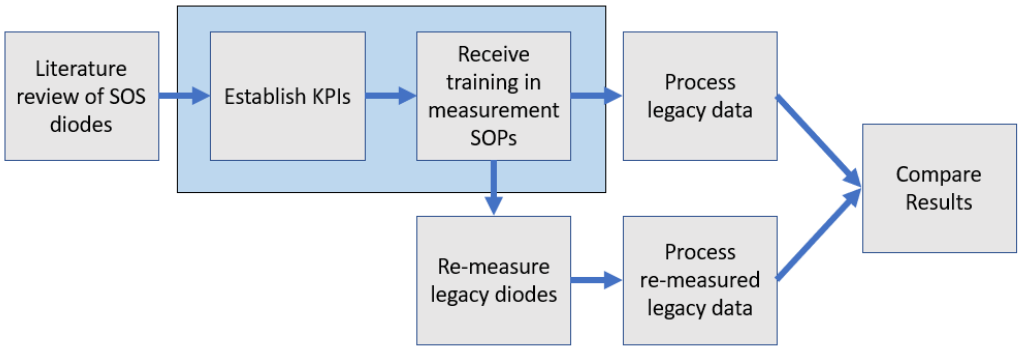


Figure 4.4.1 Projected path forward for assessing current state of measurement testing and data processing. The current tasks in progress are highlighted in blue.

(A.2) Figure 4.4.2 shows the proof-of-concept of the KPIs for the preliminary DOE design. Preliminary results, as they are found, will be shared with all team members. The findings -on a continual basis- will be used to further refine the augmentation process until the final evaluation network is fully established.

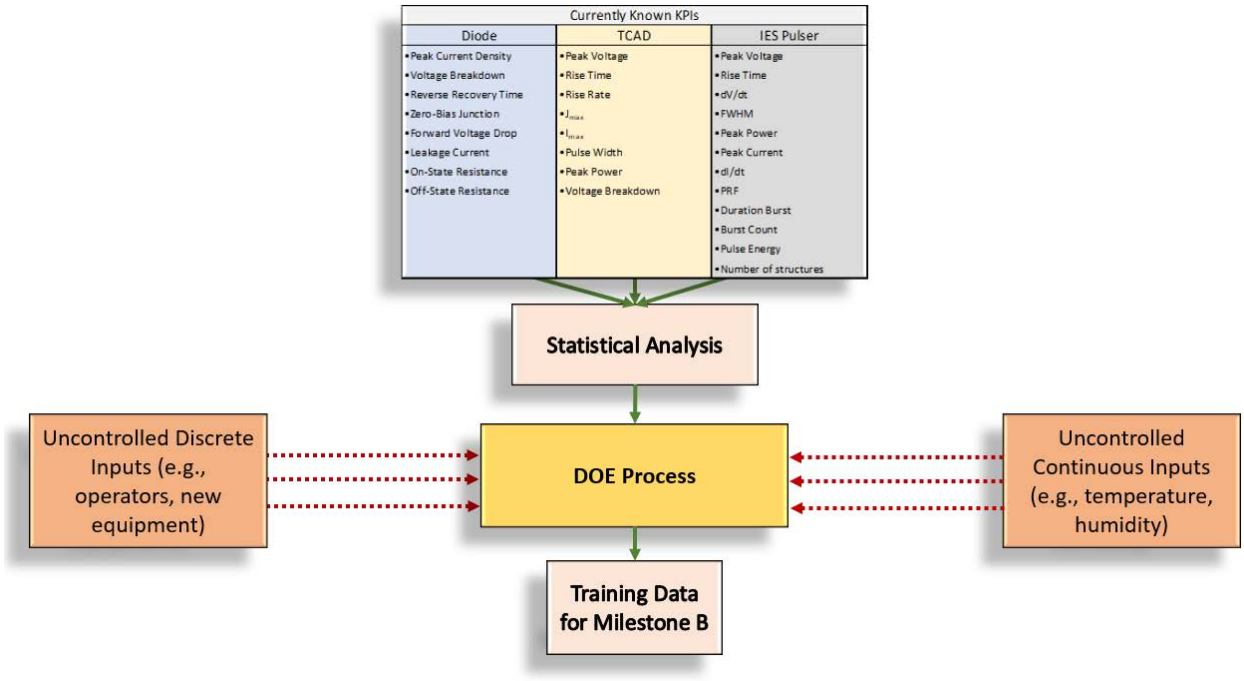


Figure 4.4.2 Preliminary DOE strategy to evaluate KPIs from legacy diodes without knowing complete fabrication recipes.

4.4.5 Summary of Significant Findings and Mission Impact

(A) Figure 4.4.2 shows the extensive number of KPIs required to bridge the gap between diode simulation, diode performance, and pulser performance. Therefore, careful consideration shall be given to the initial measurement process since it is a prime source of measurement bias. In addition, the quantity of information necessary to sift through will require leveraging ML to reduce the number of inputs for the final analytic model. Thus, this model will provide the basis for a holistic DOE evaluation network from simulation modeling to pulser performance.

4.5 DSRD-Based Pulsed Power Source Systematic Topological Optimization

(Sourov Roy)

4.5.1 Problem Statement, Approach, and Context

Primary Problem: Semiconductor opening switch (SOS)-based pulse generators using inductive energy storage (IES) and release topologies able to produce ones of gigawatts in ones of nanoseconds are traditionally large and bulky, and suffer from low volumetric power densities, rendering them impracticable for Navy afloat missions.

Solution Space: Through a combination of numerical and experimental efforts, systematically develop a modular architecture of an SOS-IES pulser circuit—by determining the optimal permutation of series and parallel combinations of stages within the base SOS-IES pulser (and components utilized)—which maximizes the peak voltage, peak power, and volumetric power density achieved without sacrificing the desired nanosecond risetime of the pulses generated.

***Sub-Problem 1*:** Viable SOS diodes, specifically p^+-p-n^+ silicon diode structure versions (i.e., drift-step recovery diodes, or 'DSRDs' consistent with those discussed in Section 4.2) are in limited production, minimal supply, and are traditionally manufactured OCONUS, therefore are difficult to procure. This leads to using non-ideal diodes within the pulse generator circuit, causing decreased performance.

Sub-Problem 2: A reciprocal relationship exists between the performance of the SOS-IES circuit (specifically, the auxiliary components utilized), and diode's performance characteristics. Optimizing at the diode level (e.g., doping profile and concentration) affects the impulse signal output. Conversely, an optimized circuit topology may require alternative components (e.g., differently valued inductors and capacitors) different than those used when simulating/optimizing the diode's performance which, in turn, affects the performance of the diodes.

Sub-Problem 3: Another problem is finding the optimal parallel-series permutation of the IES storage and release topology and its key component parameters which produces the highest peak power output, lowest rise time, and highest efficiency given theoretical and real-world constraints. That is to say, the optimal diode performance and ancillary components used in a 1×1 topology cannot simply be scaled to a 2×2, a 4×2, etc. as the pulse combining and compression occurring within each stage requires different considerations. Compounding this issue, exploration of existing theoretical models which

aid in simulation techniques to evaluate the performance tradeoffs is limited. Therefore, most of this work aims to determine the best-case configurations of IES topology by maturing a suitable predictive model for the IES modular architecture for a given performance matrix.

State-of-the-Art (SOTA): Large IES pulse generators ($\geq$1-m^3, $\geq$300-kg) – comprised of SOS- and DSRD-based pulsers – which are comprised of sixteen parallel-branches, each containing four series-connected stacks (V_{max} = 130 kV, surface area ~20 mm^2), have demonstrated reverse pumping currents of 25 kA with an injection time of 400 ns to produce 400 kV pulse amplitudes with full-width half-maximum (FWHM) values of 60 ns produced across a 100 Ω load; a voltage gain factor of ~3 (i.e., power amplification level ~9.5 dB). Pulse repetition frequencies up to 4 MHz have also been produced across similar load values. Smaller versions (equivalent in size to the pulse generators developed for this effort, i.e., ~0.01-m^3, ~2-kg) are able to achieve 6-kV, 200-ps risetime, and <500 ps FWHM across a 50 Ω load.

Deficiency in the SOTA: Large IES pulse generators which can achieve the foregoing performance parameters are traditionally limited by mechanical design constraints (onboard itinerant vehicles) and power supply limitations, are large (case lengths <1 m), and require transformer oil for cooling purposes, which lead to undesirable system mass values up to 300 kg. The smaller air-cooled versions are limited to PRF < 15 kHz. Additionally, a comprehensive study on SOS/DSRD generators aiming to achieve maximum gain and efficiency (reducing thermal load) through optimizing the number and ratio of parallel-branches and series-connected stages is missing in the SOTA.

Solution Proposed: Systematically determine topological IES circuit configurations, (focusing solely on DSRD-based systems) and the necessary components therein that maximize voltage gain and efficiency achieved by the pulser.

Relevance to OSPRES Grant Objective: IES pulse generators using DSRDs can remove the need for photo-triggered switches and their laser sub-systems. They are ideal for triggering sub-nanosecond rise-time sharpeners (SAS, D-NLTL, etc.), reducing overall cost, volume, and weight.

Risks, Payoffs, and Challenges:

Risks: DSRDs which possess sub-optimal doping profiles may limit the permissible injection time (pumping) of the switch. This leads to a decreased amount of time energy is accumulated and ultimately limits the reverse current amplitude during extraction time. Development of sub-optimal diodes may lead to sub-optimal circuits with sub-optimal performance. The data gathered from these circuits would then be used to train the genetic algorithms developed and the redesign future topologies constructed; ultimately leading to spurious conclusions regarding ideal topological circuit configurations with ‘N’ number of series-connected stages, each containing ‘M’ parallel branches.

Payoffs: Leveraging collaborative partnerships with U.S.-based manufacturers of DSRDs, the ability to refine and control the performance characteristics of the IES devices themselves, along with the ability to simulate and manufacture the IES pulsers in-house, enables a holistic soup-to-nuts capability to optimize, produce, and evaluate these nanosecond pulse generators.

Challenges: Determining the superlative ratio of design/development (through numerical analysis) to the effort put towards experimental testing/evaluation of the DSRD pulser is challenging due to the novelty of the approach. The complexity of the theoretical model is extreme given the M×N number of stages within the pulse forming network. SPICE circuit simulation software algorithms possess computational convergence difficulties caused by abrupt changes in capacitance, inductance, and impedance. DSRDs are non-autochthonal to SPICE software's databases thus are only approximated by equivalent combinations of circuit elements. Additionally, the variable time step imbedded in SPICE algorithms exacerbates this convergence issue. This summates to the existing discrepancy when comparing existing experimental data to that of simulated values.

4.5.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Construct/demonstrate a DSRD-based 2×2 IES pulse generator prototype capable of producing ≥4 kV peak voltage, ≤1 ns risetime, ≤5 ns FWHM, ≥320 kW peak-power, ≥1 kHz PRF, ≥100 shots-per-burst, ≥5 number of bursts [***Completed JUL21***].

(B) Milestone – Construct/demonstrate a DSRD-based 4×2 IES pulse generator prototype capable of producing ≥12 kV peak voltage, ≤1 ns risetime, ≤5 ns FWHM, ≥2 MW peak-power, ≥1 kHz PRF, ≥1,000 shots-per-burst, ≥500 number of bursts [*Ongoing, estimated completion by AUG21*].

1. Task – Work with TCAD simulation team (see Section 3.6) to compare-to, revise/update diode simulation model towards achieving refined and accurate diode performance and pulse generator circuit simulation output [***Ongoing–JUL21***];

2. Task – Refine and simulate circuit topological permutation(s) to include an increased number of parallel branches within an electrically optimal layout using Altium [*JUL–AUG21*];

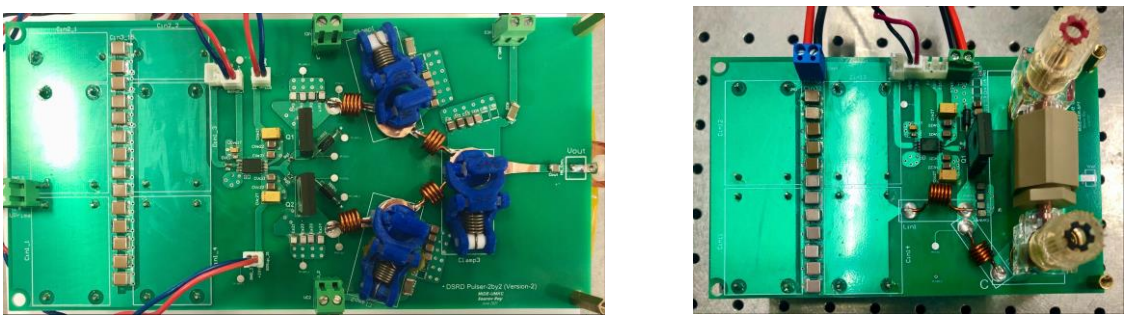
(C) Milestone – Construct/demonstrate a M×N pulse generator prototype capable of producing ≥20 kV peak voltage, ≤1 ns risetime, ≤2 ns FWHM, ≥8 MW peak-power, ≥1 kHz PRF, and $\geq 2\sigma_{V_{peak}}$, which operates in continuous-burst mode as a viable candidate for OSPRES Contract source alternative [*on hold until Milestone B is completed*].

(D) Milestone – Construct/demonstrate a 8×2 pulse generator prototype capable of producing ≥48 kV peak voltage, ≤1 ns risetime, ≤2 ns FWHM, ≥46 MW peak-power, ≥10 kHz PRF, $\geq 2\sigma_{V_{peak}}$, ≥10,000 shots-per-burst, with a ≥50% duty cycle [*on hold until Milestone C is completed*].

4.5.3 Progress Made Since Last Report

(A) Both modified versions of the 2×2 DSRD-based pulse generator and 1×1 DSRD-based pulse generator (base-unit) with a custom-designed cylindrical DSRD clamp/housing have been populated with required components. The base-unit was developed to evaluate the performance of the epitaxially grown DSRDs outlined in Section 4.2-3, as prescribed by the methods portrayed in Section 4.4.

Moreover, the modified version of the 2×2 pulse generator has been tested in the laboratory. Photographs of these boards are shown in Figure 4.5.1 (a, b).



(a) **(b)**

Figure 4.5.1. Photograph of the **(a)** modified version of the 2×2 DSRD-based pulse generator circuit, and **(b)** 1×1 DSRD-based pulse generator (base-unit)

4.5.4 Technical Results

(A) For the modified 2×2 DSRD-based pulse generator and 1×1 DSRD-based pulse generator (base-unit) circuit designs, we selected snubber capacitors (for the power MOSFETs) with lower voltage ratings (630 V) compared to the ones (rated at 3 kV) used in the previous version of the pulser circuit to minimize their footprint. Moreover, the SiC MOSFETs with lower voltage rating (1.2 kV) were chosen to achieve the highest possible current rating (ID=102-A, IDM=408-A) whereas the previous design used 1.7 kV MOSFET (ID=72-A, IDM=160-A) [1,2]. High current MOSFETs are advantageous to use since they will allow us to run the pulse generator with MOSFET trigger length (T_{ON}) beyond 400 ns.

Unfortunately, due to the interaction with the parasitic inductances and capacitances, the switching node experienced ringing and oscillations with an amplitude above the absolute maximum rated voltage of both the SiC switch and the snubber capacitors which resulted in their destruction on multiple occasions. To overcome this issue, we replaced the snubber capacitor with a higher voltage rating (3 kV). Moreover, we can still select the 1.2-kV, 102-A SiC MOSFET by using higher valued snubber capacitors to further suppress the voltage overshoot and ringing below 1.2 kV.

In a separate study, we performed an automated LTspice simulation of a 1×1 IES pulse generator (base-unit) using Python scripting and KNN machine learning algorithm where we found that the effect of snubber capacitor on the circuit performance is negligible. Therefore, increasing snubber capacitance allowing the use of 1.2-kV, 102-A SiC MOSFET is a viable option and further testing of the pulser circuit with the increased snubber capacitance will be performed during the remainder of this month. Alternatively, we may use a higher valued input inductor (L_{in}) to limit the peak current for large T_{ON} and this will allow us to incorporate 1.7 kV MOSFET with a limited current rating. Further simulation and experimental validation of such pulser circuit using higher valued L_{in} will be performed during the remainder of this month to investigate the effect of its parameter space in the circuit performance. More details on this study are presented in Section 4.6.

After each pulse generator failure event, many components in the circuit suffered cascading failure such as gate-source TVSS diodes, gate-driver circuits, MOSFETs, and the snubber capacitors and we had to debug, troubleshoot, and replace them. While further testing the circuit with MOSFETs and snubber capacitors with higher voltage ratings, 630-V and 1.7-kV, respectively, we found that the resultant output was compromised meaning the peak amplitude, rise-time and FWHM were far less than they were obtained with the testing of the previous version using the similar components and with similar operating condition (T_{ON}= 340-ns and V_{supply} = 180-V). Furthermore, the output waveforms exhibit inconsistent pre/post-pulses with poor repeatability/stability meaning large shot-to-shot variability as is evident in Figure 4.5.2. We suspect that one or more diodes in the diode stacks might have been damaged due to excessive current flow through them during the destruction of either MOSFET or snubber capacitor that resulted from transient voltage overshoot at the switching node. Further characterization of these diodes is needed before using them in the circuit, otherwise, the circuit will require to be tested with new diode stacks.

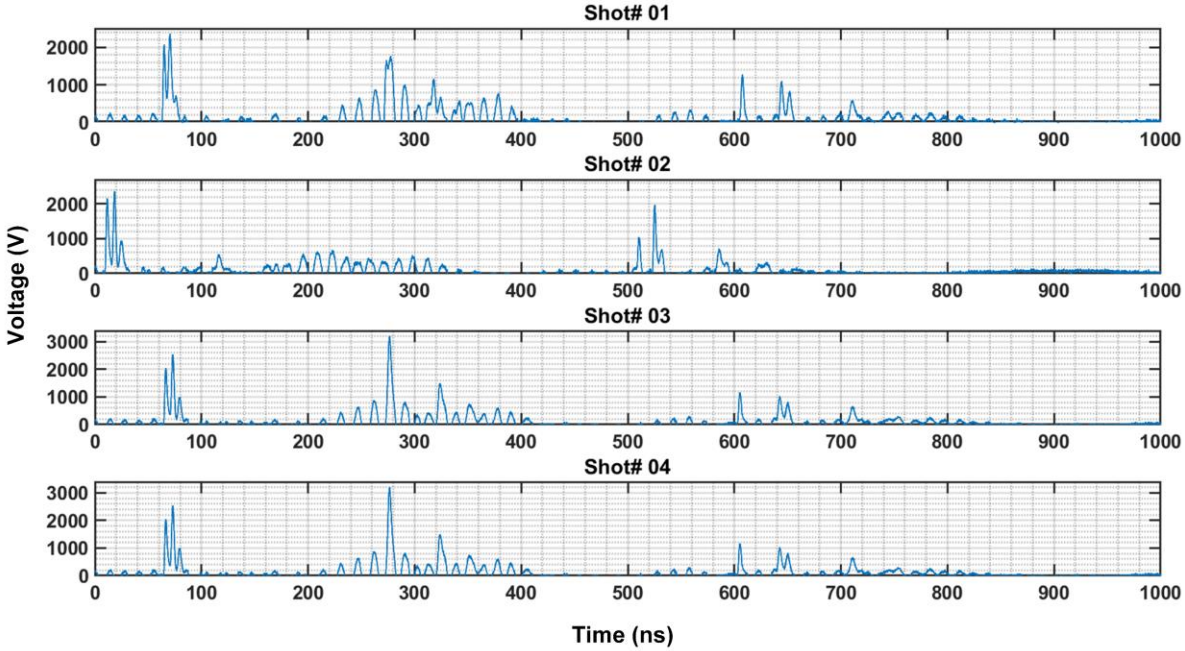


Figure 4.5.2. Output waveform for multiple number of shots.

4.5.5 Summary of Significant Findings and Mission Impact

(A) Successful construction and operation of a 2×2 DSRD-based IES pulse generator prototype has been completed which meets or exceeds the milestone's required key performance metrics. Shown in Table 4.5.1 are the previous and current pulse generator's performance specifications in comparison to a similar 2×2 pulser developed by Kesar et al. [1] using DSRDs, and to that of a commercial off-the-shelf (COTS) DSRD pulser of similar space and weight developed by Megaimpulse (i.e., PPM-0731) which also uses DSRDs with silicon avalanche shapers (SAS) [2]. Although the Megaimpulse pulser

utilizes a SAS with a <500 ps risetime (a threshold we do not intend to go below due to Commerce Controlled List limitations), it is interesting to compare the results of linear voltage gain and peak power of this system, to that of one that utilizes a SAS.

Table 4.5.1 Comparison of DSRD-based IES Pulse Generator Performance

KPM	Units	MIDE - V1 Previous	MIDE - V2 Current	Kesar *et al.* SOTA	MI-PPM0731 COTS
V_{supply}	V	225	180	300	160
T_{ON}	ns	100	340	?	200
V_{peak}	kV	5.59	**7.35**	5	6.3
Gain	V/V	24.8	**40.8**	16.7	39.4
$\tau_{rise,20\text{-}90\%}$	ns	1.2	1.142	1.96	0.12
dV/dτ	kV/ns	4.66	6.44	2.55	**52.50**
FWHM	ns	2	5.48	2.27	0.35
PW	ns	5	7	3.5	2.5
Z_{LOAD}	Ω	50	50	50	50
P_{peak}	MW	0.625	**1.080**	0.500	0.794
E_{pp}	mJ	0.125	0.154	0.143	0.318
PRF_{max}	kHz	100	100	100	15
Burst	shots	100	100	*N/A*	100
	%	100	100	*N/A*	100
SD_{Vpeak}	σ	> 2	**> 2**	*N/A*	*N/A*
	%	96.5	**97.8**	*N/A*	*N/A*

The current permutation of the 2×2 SOS-IES pulser developed by MIDE under the ONR OSPRES Grant is able to achieve a higher peak voltage and shorter risetime than DSRD-based pulsers reported in the literature of comparable space and weight as well as those commercially available. The ability to generate a linear voltage gain of 40.8 to produce over a Megawatt of peak power into a 50Ω load while achieving a peak voltage output standard deviation of 2σ when operating at a PRF of at least 100 kHz, brings this technology to the forefront of viable options to potentially support the Naval afloat mission.

4.5.6 References

[1] https://www.onsemi.com/pdf/datasheet/nvh4l020n120sc1-d.pdf

[2] https://cms.wolfspeed.com/app/uploads/2020/12/C2M0045170P.pdf

4.6 Optimizing SOS-IES Pulse Generator Performance with Machine Learning

(Dewan Noor and Sourov Roy)

4.6.1 Problem Statement, Approach, and Context

Primary Problem: Multiple components exist within each M×N stage of the pulse generator's circuit. Statistical correlations between the non-linear separable data of the component's characteristics and the pulser's performance is ill-suited for traditional linear regression methods.

Solution Space: Explore machine learning, deep learning, and artificial intelligence methodologies to generate training data and determine the shape of the underlying statistical model with minimal error.

***Sub-Problem 1*:** Using machine learning would require a lot of data to train the model to optimize the parameters for desired design. But data generation takes a lot of time and space in the storage. These lead to both time and space complexity.

Sub-Problem 2: Each dataset has its own patterns. Hence, each one will behave differently while training for a certain machine learning algorithm. The training model might act complete different while using a testing dataset with different conditions. So, testing with the experimental model data may act differently from result in the training using simulation model.

Sub-Problem 3: Choosing correct machine learning algorithm for a certain solution can be tricky if the dataset changes pattern with increasing number of variable parameters as we increase the values of M and N for higher stages. A supervised learning might not work well with the variations in the pattern of the existing variables.

State-of-the-Art (SOTA): To characterize the relation among the multiple components of each M-parallel and N-series connected stage of the pulse generator's circuit, genetic algorithm and polynomial regression are mostly usually applied to optimize the parameters if they are not linearly correlated. Polynomial regression with higher degree often generates a relation among the variables. Hence, they also take less time and space complexity.

Deficiency in the SOTA: Genetic algorithm and polynomial regression often fail if the variables are not mutually exclusive. Their interdependency usually overfit the data within their certain range. So, when we want to establish the relationship for higher number of M and N (multiple stages), the more the interdependency among the variables, the less effective the algorithm would be. Hence, the model is bound to fail in the end.

Solution Proposed: In order to train the model with certain parameters, we need to find out the top (i.e., most relevant, and statistically significant) parameters/features contributing most towards the circuits output. A machine learning algorithm e.g., random forest (RF), K-nearest neighbor (KNN), etc., can be used or the feature selection method using the dataset with variable sweeping of the input parameters (Input voltage, biasing voltage, capacitance, inductance etc.) for the output parameters (Peak voltage, rise time etc.). Once the top features are selected, those selected parameters can be trained

against a machine learning algorithm for a certain desired output. Hence, we can find the optimized value of the parameters for out desired output parameters.

Relevance to OSPRES Grant Objective: SOS-IES pulse generators with desired output with a design modeled by a machine learning algorithm can remove the need for photo-triggered switches and their laser sub-systems. They are ideal for triggering sub-nanosecond rise-time sharpeners (SAS, D-NLTL, etc.), reducing overall cost, volume, and weight.

Risks, Payoffs, and Challenges:

Risks: The model generated from machine learning algorithm using the simulated training dataset might have high bias if the generated sample size is of low volume. On the other hand, the variance may be high if we try to generate high volume data using data augmentation algorithm like bootstrapping or k-fold cross validation. The trade off between bias and variance are somewhat a risky assignment to take care of while applying the machine learning algorithm.

Payoffs: If the loss ratio between training and testing dataset is kept minimal with maintaining a certain volumetric unbiased and low-variance data, the input parameters can be optimized for the desired output.

Challenges: The main challenge would be to maintain the trained model stable all he way from the training dataset to the testing dataset as the testing dataset is basically the data generated from the experimental setup with circuit components having variations in manufacturing and having different models than the simulated components. Hence, the algorithm should be able to forecast the trend of behavioral patterns among the components.

4.6.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Automated script generating thousands of LTSpice simulations in Python in the batch mode to accumulate large volume of data for model training developed [***Completed JUL21***].

1. Task – Accommodate the Python package to run the LTSpice to the script [*JUL–AUG21*];
2. Task – Generate the script to run ~1000 LTSpice simulation in Python for 2X2 stage of the pulse generator [*JUL—AUG21*];
3. Task – Sweep charge voltage and trigger time parameter to establish the trend of peak voltage and rise time against the trigger time for the 2x2 stage and compare the trend with the experimental data [*JUL–AUG21*];

(B) Milestone – Machine learning model utilizes feature selection method to determine the statistically significant input parameters and their optimal/maximum values peak voltage/rise time [***Completed JUL21***].

1. Task – Choose 1x1 cell to first find of the top features and assume similar features contributing towards the 2x2 stage [*JUL–AU21*];

2. Task – Apply random forest feature selection algorithm to compute the top features [*JUL–AUG21*];
3. Task – Apply k-nearest neighbor feature selection algorithm to compute the top feature [*JUL–AUG21*];
4. Task – Apply Pearson coefficient correlation feature selection algorithm to compute the top features [*JUL–AUG21*];

(C) Milestone – Sweep the top features/input parameters contributing most towards peak voltage/rise time and find out the trend. [*estimated completion by SEP21*].

1. Task – Select the top features to sweep after being computed from the feature selection method and prepare the script [*JUL–AUG21]*
2. Task – Generate the trend of the top peak voltage/rise time varying the top selected features. [*AUG–SEP21]*

4.6.3 Progress Made Since Last Report

(A) Milestones A has been completed. Automated scripts were ran to simulate the LTspice DSRD pulse generator in the batch mode with infinite number of iterations/simulations given the capability of the computer.

(B) Milestone B was also completed; features were computed using the machine learning algorithms, random forest and KNN feature selection method. The features were varied according to their importance to generate desired output towards achieving the desired output of Milestone C.

4.6.4 Technical Results

(A) An automated Python script was written to perform LTspice simulations in batch mode with the capability of running infinite number of simulations given the capability of the computer/machine. The script modifies a template netlist for a certain design (with the different variations of the input parameters) in each iteration and generates output data and finally stores the data in a matrix.

First, the ON time of the trigger signal was varied and peak voltage and rise time are observed. The simulated result is compared with the experimented result provided in Section 4.5's June 2021 MSR for a fixed supply voltage. The experimental results are reproduced in Figure 4.6.1 for comparison to the automated LTspice simulation results produced which are provided in Figure 4.6.2.

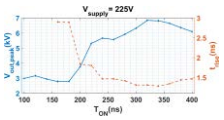


Figure 4.6.1. Resulting peak voltage and risetime achieved as a function of trigger length (T_{ON}) utilized in the 2×2 DSRD-based IES pulse generator *Experimented result from JUL21 OSPRES Grant MSR, Section 4.5*.

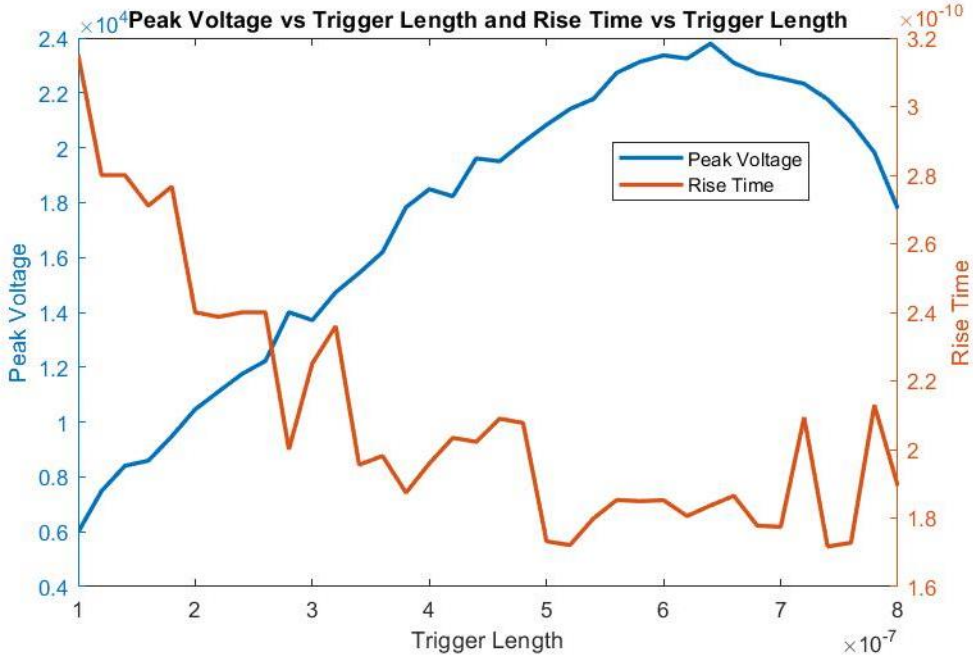


Figure 4.6.2. Resulting peak voltage and risetime achieved as a function of trigger length (T_{ON}) generated from the automated python script running LTspice in batch mode.

From Figure 4.6.2, the trend of both the peak voltage and the rise time against the ON time of the trigger signal are behaving similar way in both the experimented and the simulated plot. Although the difference is observed in the value of peak voltage. The maximum value obtained in the simulated result (~23 kV) is lot higher than the experimented result(~7 kV). The downward slope of the peak voltage also starts from 630ns in the simulated result while it follows the same trend from 340 ns in the experimented result. The variation is due to the fact that the model properties are different in the simulated LTspice circuit and in the experimental setup.

(B) Top feature/input parameters are investigated from the 1x1 stage of the pulse generator. From the simulation circuit, Supply Voltage (V_{in}) , ON time of the trigger signal (Trg), Snubber Capacitance (C_s), bias capacitance (C_1), series inductance(L_1) and bias voltage (V_1) are chosen as the features. We applied random forest feature selection method, K-nearest neighbors and Pearson correlation coefficient method to find out the top features contributing towards the output parameters peak voltage and rise time. In the analysis, a feature index value (0,1,2,3,4,5) is given for each feature which are Trg:0, L_1:1, C_1:2, V_1:3, C_s:4, V_{in}:5.

Figure 4.6.3. Feature selection using Random Forest method. Feature index values are given as Trg:0, L_1:1, C_1:2, V_1:3, C_s:4, V_{in}:5.

Fig 4.6.3 is showing the bar plot of feature score values. From the plot it is clear then feature Trg:0 is having the highest score value, hence being the most important feature. The next 2 important features are V_5 (Supply voltage) and V_1 (Bias voltage). From the random forest method, the importance of other 3 features are negligible as their score values are 0. The bar chart on the left-hand side of Fig 4.6.4 shows the same analysis using K-nearest neighbor (KNN) feature selection method. Here, the rank of importance is as follows :Trg>V_1>V_{in}>C_1>L_1>C_s . As KNN is robust to noisy training data and is effective in case of large number of training examples, the score values are more prominent using KNN method. The random forest works better in less noisy and more categorial data. But, both of the feature selection method still shows the importance of Trg, V_1 and V_{in}. We also analyzed the features using the statistical method of Pearson correlation coefficient shown on the right in Fig 4.6.4. Hence, the correlation scores of Trg, V_1 and V_{in} are higher with output parameters peak voltage and rise time.

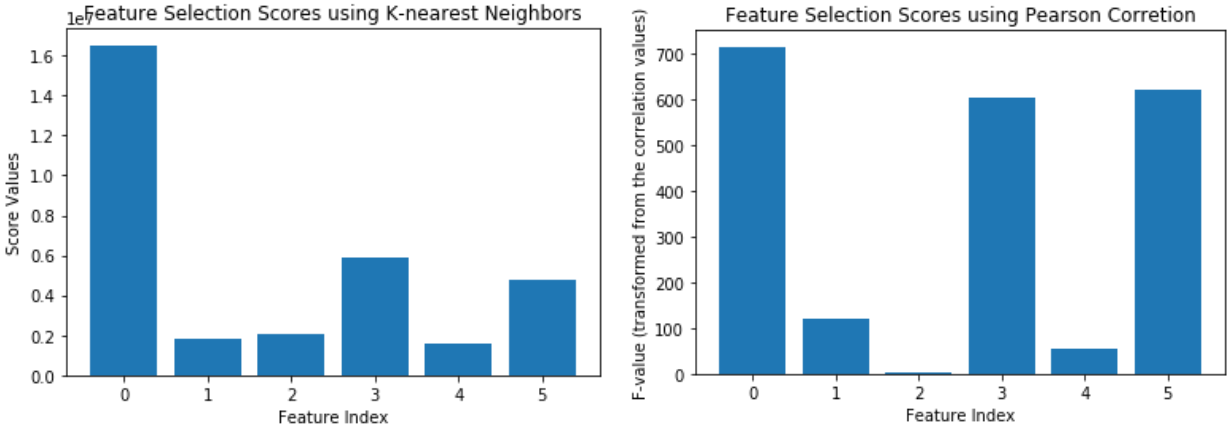


Figure 4.6.4. ***(Left)*** Feature selection using K-nearest neighbor (KNN). Feature index values are given as Trg:0, L_1:1, C_1:2, V_1:3, C_s:4, V_{in}:5. ***(Right)*** Feature selection using Pearson Correlation Coefficient. Feature index values are given as Trg:0, L_1:1, C_1:2, V_1:3, C_s:4, V_{in}:5.

4.6.5 Summary of Significant Findings and Mission Impact

(A-B) The Python automated script generation is completed marking the completion of milestone A. Feature selection method is applied to find out the top features contributing towards the output marking the completion of milestone B. Milestone C is in progress with the completion of task-1 to vary the important features and modify the script accordingly.

4.7 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners

(Gyanendra Bhattarai)

4.7.1 Problem Statement, Approach, and Context

Primary Problem: Producing a megawatt sub-nanosecond waveform from pulse generators containing DSRDs alone requires multiple diodes stacked in series which results in rise-times > 1 ns and thus make them ill-suited to achieve the SWaP metrics necessary for HPM pulse generators for the Navy afloat mission.

Solution Space: Utilize viable pulse shaping/compression technologies (e.g., semiconductor opening switches, silicon avalanche shapers, dynistors, thyristors) with SWaP metrics within solid-state pulse generators to increase peak power, gain, and efficiency of the pulse generation system. *Please refer to OSPRES Grant's July MSR for full problem and solution space brief and explanation.*

Sub-Problem 1 Exploring viable alternatives to non-commercially available silicon-based semiconductor devices such as alternative wide bandgap (WBG) materials (e.g., GaN, SiC) based on their known properties and theoretical simulations may lead to more robust and improved performance switches; however, doing so would require significant time in developing device models and fabrication techniques.

Sub-Problem 2 (Fundamental Physics): The phenomenon behind the origin of free carriers that trigger the impact-ionization at higher-than-breakdown fields when applying a sharply increasing voltage pulse is not completely known. A University of New Mexico study [1] has concluded that the operation of a silicon avalanche shaper (SAS) is inconsistent with the theory described by Russian scientists. Further, it is not clear whether the switching (generation of electron–hole plasma) is uniform across the device area nor is localized (filamentary). Such different mechanisms are believed to be dependent on device geometry and doping concentration based on experimental evidence. It is crucial to understand those mechanisms to devise even faster and more powerful switches.

State-of-the-Art (SOTA): Hydrogen-based spark gap switches (HGS) provide the highest peak-voltage output and are accompanied by the shortest risetimes of the technologies evaluated. Large (>1 m^3) SOS-based pulsers which utilize hundreds of diodes stacked in series, as well as fast ionizing dynistors (FID)s, can produce equivalent peak voltages (~1 MV), and peak power outputs (~1 GW).

Deficiency in the SOTA: Closed loop HGS are limited in their PRF capabilities (<1 kHz). FID-based pulser generators are unable to generate the frequency spectra and high pulse energy due to their long risetime and long pulse width. DSRDs and SOS diodes alone, while able to achieve the necessary PRF and peak voltage/power requirements, are unable to achieve sub-nanosecond risetimes without compromise to the ultracompact form-factor of the system (<0.1 m^3).

Solution Proposed: Downselect viable replacement(s)/additional technologies which meet or exceed the performance parameters set forth in Section 4.5's Milestones A-D. Improve SOTA through optimizing: SAS diode, dynistor, and/or thyristor structure (material, topology, geometry, doping concentration, packaging) to increase inductive energy storage and peak reverse current capabilities while mitigating increased thermal dissipation requirements. Leverage simulation results in correlation with the experimental results obtained from Section 4.5 to produce an all-solid-state megawatt sub-nanosecond pulse generator with semiconductor sharpener.

Relevance to OSPRES Grant Objective: The alternative all-solid-state technologies discussed could individually, or in combination, provide the means to produce order(s) of magnitude greater peak power, without severe limitation to PRF, as SWaP-centric means to increase the capability and extent of protecting naval assets.

Risks, Payoffs, and Challenges:

Risks: Undergoing time-intensive and complex simulations to then down-select one technology based on peak power output alone presents risk to other secondary or tertiary performance metrics such as PRF and pulse energy, which risks developing ill-suited technologies to support the float mission. Additionally, as new technology emerges via research, scope creep to numerically and experimentally evaluate new technologies may delay transitioning these technologies into viable systems.

Payoffs: The SWaP tradeoff of generating a non-laser-based system with any number of these systems can yield a higher fidelity pulsed-power waveform output. Determining which technology is viable and feasible in terms of the key performance metrics should

yield a more ultracompact form factor pulse generator with order(s) of magnitude greater power density without compromise to overall size and weight to the system.

Challenges: Determining the true performance metrics of interest based on these highly different devices is challenging. Without a more robust and deep understanding of their operation, and how to utilize them within a pulse generator topology, in a swappable configuration or otherwise, requires additional time and consideration. Managing the tradeoff between the academic understanding of the technologies of interest presented in the foregoing table, and the transition to prototype effort/mentality, will require both a delicate balance and leveraging the pulsed-power team's combined effort.

4.7.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Downselect viable technology as replacement to currently utilized DSRD, which increases at least one of the key performance metrics by an order of magnitude without compromise to the overall volume of the system [*Estimated completion by AUG21*].

1. Task – Finalize literature study of different technologies and topologies and compare SWaP tradeoff evaluation to PCSS and DSRD-based pulse generators [*JUN–JUL21*];
2. Task – Determine which DSRD alternatives are commercially available that could be used to either replace DSRD, or be used as pulse shaper/sharpening devices to improve pulse generator performance [*JUN–JUL21*];
3. Task – Select appropriate devices among commercially available DSRD alternatives for further experimental verification of their performance metrics. [*JUL–AUG21*];

(B) Milestone – Model and numerically verify the performance of the downselected technology as a direct replacement to, or additional component in tandem with, DSRDs utilized within a SOS-IES pulse generator, which meet or exceed the necessary performance requirements. [*on hold until Milestone A is complete*].

1. Task – Design experimental circuit with one selected SAS/dynistor and obtain theoretical performance metrics using standard electronic simulation tools such as LT-Spice. [*JUL–AUG21*];
2. Task – Experimentally verify whether the selected device topology can be an HSG alternative in terms of peak power produced and the pulse risetime. [*JUL–SEP21*];

(C) Milestone – Model diode/dynistor topologies using silicon or alternative WBG materials and fabrication process. [*on hold until Milestones A and B are completed*].

1. Task – Model silicon and/or alternative diode, and dynistors, with optimized device cross section (size, geometry) based on theory and simulations to increase current and thermal dissipation. [*JUL–SEP21*];
2. Task – Model/design fabrication process with optimum device topology and doping concentration. [*SEP–OCT21*]

4.7.3 *Progress Made Since Last Report*

(A.1) Scientific literature on HSG, DSRD/SOS-IES based switches and semiconductor alternatives (SAS, DBD, FID, and DLD) for pulse sharpening has been reviewed, and a detailed comparison of SWaP-C metrics is made based on these review materials.

(A.2) Sharpening the output pulses from DSRD/SOS based switches using the silicon avalanche sharpeners (SAS), delayed breakdown diodes (DBD), and fast ionization dynistors (FID) or deep level dynistors (DLD) are identified as the best alternatives to hydrogen spark gaps, which can produce comparable pulsed power, with shorter pulse risetime and higher PRF. SAS, DBD, FID/DLD are available for purchase, however, from Russia.

4.7.4 *Technical Results*

(A) Based on the review materials [2], [3], [12]–[18], [4]–[11], the ranges of peak power and risetime of different switches is presented in Figure 4.7.1.

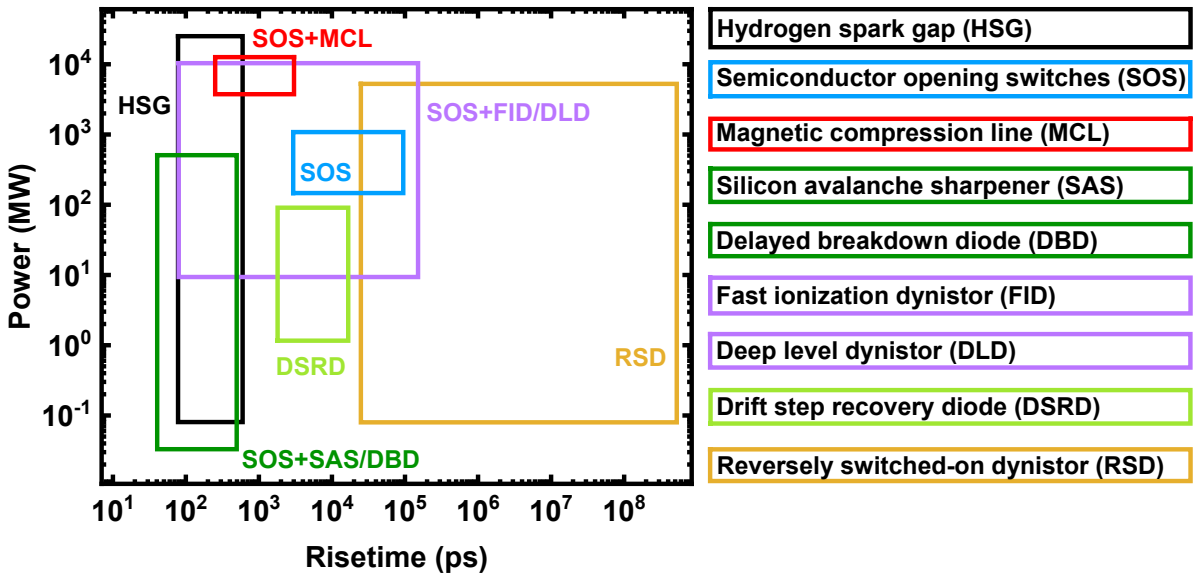


Figure 4.7.1 Ranges of peak power and pulse risetime of different types of high-power switches.

DSRD (p^+–n–n^+) and SOS (p^+–p–n–n^+) are [ideally] similar to the SAS and DBD respectively. The only difference between them is the way they work. DSRD and SOS pulsers need a forward pumping current and their switching is based on extracting the injected charge, while SAS and DBD work completely on reverse bias by switching these devices due to the delayed impact ionization by a steep reverse voltage rise rate of ~10 kV/ns. In presence of certain process-induced (PI) defect states in silicon, they are switched by voltage pulses with rise rate of ~1–2 kV/ns. Therefore, we can at least try DSRD or SOS in SAS and DBD configuration to test their performance if we have power switches producing about 3 kV with 10kV/ns rise rate.

4.7.5 Summary of Significant Findings and Mission Impact

(A) No single technology appears to meet or exceed the key performance metric requirements across the board. Where HSG lead in peak voltage and peak power, in comparison to the other technologies of interest, they lack in their ability to meet the required PRF, device lifetime, and SWaP-C metrics. All solid-state switching power supplies utilizing SOS and semiconductor sharpeners seem viable technology to compete against HSG with comparable or better SWaP-C metrics.

4.7.6 References

[1] E. Schamiloglu, C. B. Fleddermann, R. Focia, and J. Gaudet, “A STUDY OF ADVANCED SEMICONDUCTOR SWITCH PHYSICS AND TECHNOLOGY PHILLIPS LABORATORY Advanced Weapons and Survivability Directorate AIR FORCE MATERIEL COMMAND KIRTLAND AIR FORCE BASE, NM 87117-5776,” 1997.

[2] S. Schneider and T. F. Podlesak, “Reverse switching dynistor pulsers,” *IEEE Trans. Plasma Sci.*, vol. 28, no. 5, pp. 1512–1519, 2000, doi: 10.1109/27.901224.

[3] V. I. Brylevskiy, I. A. Smirnova, A. V. Rozhkov, P. N. Brunkov, P. B. Rodin, and I. V. Grekhov, “Picosecond-Range Avalanche Switching of High-Voltage Diodes: Si Versus GaAs Structures,” *IEEE Trans. Plasma Sci.*, vol. 44, no. 10, pp. 1941–1946, 2016, doi: 10.1109/TPS.2016.2561404.

[4] V. M. Efanov, V. V. Karavaev, A. F. Kardo-Sysoev, and I. G. Tchashnikov, “Fast ionization dynistor (FID)-a new semiconductor superpower closing switch,” in *Digest of Technical Papers. 11th IEEE International Pulsed Power Conference (Cat. No.97CH36127)*, 1997, vol. 2, pp. 988–991, doi: 10.1109/PPC.1997.674523.

[5] I. V. Grekhov and P. B. Rodin, “Triggering of superfast ionization fronts in silicon diode structures by field-enhanced thermionic electron emission from deep centers,” *Tech. Phys. Lett.*, vol. 37, no. 9, pp. 849–853, 2011, doi: 10.1134/S1063785011090203.

[6] V. I. Brylevskii, I. A. Smirnova, P. B. Rodin, and I. V. Grekhov, “Subnanosecond avalanche switching in high-voltage silicon diodes with abrupt and graded p-n junctions,” *Tech. Phys. Lett.*, vol. 40, no. 4, pp. 357–360, 2014, doi: 10.1134/S1063785014040166.

[7] C. A. Frost, R. J. Focia, T. C. Stockebrand, and M. J. Walker, “Multi-kilovolt solid-state picosecond switch studies,” *IEEE Int. Conf. Plasma Sci.*, p. O1H7, 2001, doi: 10.1109/PPPS.2001.960861.

[8] S. K. Lyubutin, S. N. Rukin, B. G. Slovikovsky, and S. N. Tsyranov, “High-power ultrafast current switching by a silicon sharpener operating at an electric field close to the threshold of the Zener breakdown,” *IEEE Trans. Plasma Sci.*, vol. 38, no. 10 PART 1, pp. 2627–2632, 2010, doi: 10.1109/TPS.2010.2045396.

[9] A. I. Bushlyakov *et al.*, “Solid-state SOS-based generator providing a peak power of 4 GW,” *IEEE Trans. Plasma Sci.*, vol. 34, no. 5 I, pp. 1873–1878, 2006, doi: 10.1109/TPS.2006.881300.

[10] I. V. Grekhov, A. G. Lyublinskiy, and S. A. Yusupova, “High-power subnanosecond silicon avalanche shaper,” *Tech. Phys.*, vol. 62, no. 5, pp. 812–815, 2017, doi: 10.1134/S1063784217050115.

[11] I. V. Grekhov, A. K. Kozlov, S. V. Korotkov, I. A. Rol’nik, and A. L. Stepanyantz, “A High-Voltage Reverse Switch-on Dynistor Switch with a Transistor Control Circuit,” *Instruments Exp. Tech.*, vol. 45, no. 5, pp. 679–681, 2002, doi: 10.1023/A:1020466420755.

[12] P. Rodin, A. Minarsky, and I. Grekhov, “Impact ionization fronts in semiconductors: Numerical evidence of superfast propagation due to nonlocalized preionization,” *J. Appl. Phys.*, vol. 108, no. 3, pp. 9–11, 2010, doi: 10.1063/1.3465302.

[13] A. I. Gusev, S. K. Lyubutin, S. N. Rukin, B. G. Slovikovsky, and S. N. Tsyranov, “On the picosecond switching of a high-density current (60 kA/cm2) via a Si closing switch based on a superfast ionization front,” *Semiconductors*, vol. 48, no. 8, pp. 1067–1078, 2014, doi: 10.1134/S1063782614080132.

[14] V. I. Brylevskiy, I. A. Smirnova, N. I. Podolska, Y. A. Zharova, P. B. Rodin, and I. V. Grekhov, “Picosecond-range avalanche switching of bulk semiconductors triggered by steep high-voltage pulses,” *IEEE Trans. Plasma Sci.*, vol. 47, no. 1, pp. 994–999, 2019, doi: 10.1109/TPS.2018.2875423.

[15] V. Brylevskiy, N. Podolska, I. Smirnova, P. Rodin, and I. Grekhov, “Picosecond-Range Avalanche Switching Initiated by a Steep High-Voltage Pulse: Si Bulk Samples Versus Layered pn Junction Structures,” *Phys. Status Solidi Basic Res.*, vol. 256, no. 6, pp. 1–6, 2019, doi: 10.1002/pssb.201800520.

[16] V. Brylevskiy, I. Smirnova, A. Gutkin, P. Brunkov, P. Rodin, and I. Grekhov, “Delayed avalanche breakdown of high-voltage silicon diodes: Various structures exhibit different picosecond-range switching behavior,” *J. Appl. Phys.*, vol. 122, no. 18, 2017, doi: 10.1063/1.5004524.

[17] C. E. Baum *et al.*, “JOLT: A highly directive, very intensive, impulse-like radiator,” *Proc. IEEE*, vol. 92, no. 7, pp. 1096–1107, 2004, doi: 10.1109/JPROC.2004.829011.

[18] S. N. Rukin, “Pulsed power technology based on semiconductor opening switches: A review,” *Rev. Sci. Instrum.*, vol. 91, no. 1, 2020, doi: 10.1063/1.5128297.

5.0 Pulse Forming Networks

5.1 Diode-Based NLTLs

(Nicholas Gardner)

5.1.1 Problem Statement, Approach, and Context

Primary Problem: The size, weight, and cost of pulse forming/shaping networks (PFNs) need to be reduced and optimized for Navy afloat missions.

Solution Space: Develop a diode-based nonlinear transmission line (D-NLTL) as a pulse shaping network for the conversion of energy to the ultra-high frequency (UHF) band at single MW peak power.

Sub-Problem: Metrics used for component selection are designed for D-NLTLs operating at sub 0.1 GHz frequencies. Using such metrics alone to design D-NLTLs capable of single GHz frequency generation introduces a trial by error nature to the design process wherein frequency/power generation predictions and measurements can differ by a few hundred MHz or the design potentially fails to operate at all.

State-of-the-Art (SOTA): D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit. Simulations of LE-NLTLs indicate achievable frequencies in the single GHz range.

Deficiency in the SOTA: Simulation/measurement agreement becomes increasingly sensitive to parameters and factors outside of inductive and capacitive element choice alone at frequencies above ~100 MHz. Disparities between measurement and simulation above contribute to a trial by error design process for D-NLTL networks.

Solution Proposed: Identify and characterize diode parameters affecting frequency generation in the context of a NLTL application and identify limits/desired ranges required for UHF generation. Such parameters include, but are not limited to: diode frequency response, diode reverse bias hold-off voltage, diode small signal capacitance, diode chip/package parasitics, and diode relaxation time. The improved understanding of the explored parameters will be used to design and fabricate a D-NLTL capable of GHz center frequency generation at single MW peak powers.

Relevance to OSPRES Grant Objective: The SWaP-C^2 capabilities of D-NLTLs (shown in Figure 3.3.1) represent a potential solution to the size, weight, and cost optimization issue for PFNs on Navy afloat missions.

Figure 5.1.1 20 cell LE-NLTL of dimensions 1.1 x 23.45 cm constructed with COTS components.

Risks, Payoffs, and Challenges: There exists a potential tradeoff between power and frequency generation. Devices such as ceramic capacitors may be used in a D-NLTL to generate high peak power due to their break down potentials in the 10s of kV, however,

such devices become highly resistive at 0.1–0.2 GHz frequencies. Diodes have been shown to be operational at frequencies upwards of 0.4 GHz, however, possess low hold-off potentials limiting peak output power. The payoff to overcoming these challenges is significant reductions in PFN size and cost.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Construct/demonstrate a prototype capable of UHF generation at low voltages (1–100 V excitation amplitude)

(A1) Break a low-voltage pulse into a sequence of solitons (SEP20)
(A2) Increase frequency generation past 200 MHz (NOV20)
(A3) Select diode candidate (junction capacitance <50 pF) and simulate expected results (Ongoing)
(A4) Design/fabricate/test line (Ongoing)

(B) Milestone – Demonstrate tuning of waveform at low voltages using electrical or mechanical means (**Completed with voltage biasing APR21**)

(C) Milestone – Construct/demonstrate a prototype capable of frequency generation above 1 GHz at single MW peak powers (Completed MW peak power but not GHz center frequency – Ongoing)

(C1) Identify diode candidates with a hold-off voltage of several kV and a low signal junction capacitance under 100 pF (Completed JAN21)
(C2) Design/fabricate single diode prototypes (Completed JAN21)
(C3) Perform initial tests using half-barrel pulse source (Completed FEB21)
(C4) Refine simulation using measurements (Completed FEB21)
(C5) Test a prototype using two diodes in series (Completed FEB–MAR21)
(C6) Test lines using Mega Impulse source (Completed MAY21**)**
(C7) Test K50F D-NLTL using PCSS as a source (Completed JUN21)
(C8) Use simulations and tests to refine line for increased frequency generation (**Completed JULY21)**
(C9) Rebuild lines for negative polarity pulses (**Completed JULY21**)
(C10) Test lines using PCSS as a source with various cell inductances **(Completed JULY)**
(C11) Test lines using Marx Generator as a source (**Ongoing AUG21**)
(C12) Reconstruct PCSS strip line to produce a pulse similar to 5.1.2 (left) and retest (**Ongoing AUG21)**

(D) Milestone – Demonstrate power scalability using an array of D-NLTLs (**On Hold – Prioritizing Milestone C**)

(D1) Design a prototype capable of running two D-NLTLs simultaneously off of the same excitation pulse (Completed JUN21)
(D2) Build a circuit capable of measuring the CV curve of low-voltage diodes and measure the CV curves of unused diodes and heavily used diodes (Completed JUN21)

5.1.3 Progress Made Since Last Report

(C) Both the K50F and K100F D-NLTLs were tested using a photoconductive semiconductor switch (PCSS) based source and cell inductances of 12 nH and 3.7 nH. Results are discussed fully in section 5.1.4 and shown in figure 5.1.3. In all cases the K50F and K100F lines demonstrate similar behaviors, with the K50F variant producing larger peak amplitudes and the K100F variant producing greater max frequencies throughout all tests. Due to the PCSS pulse geometry, the lines primarily functioned with a low pass filter (LPF) characteristic. Next steps for the GHz MW prototype will be described at the end of section 5.1.4.

5.1.4 Technical Results

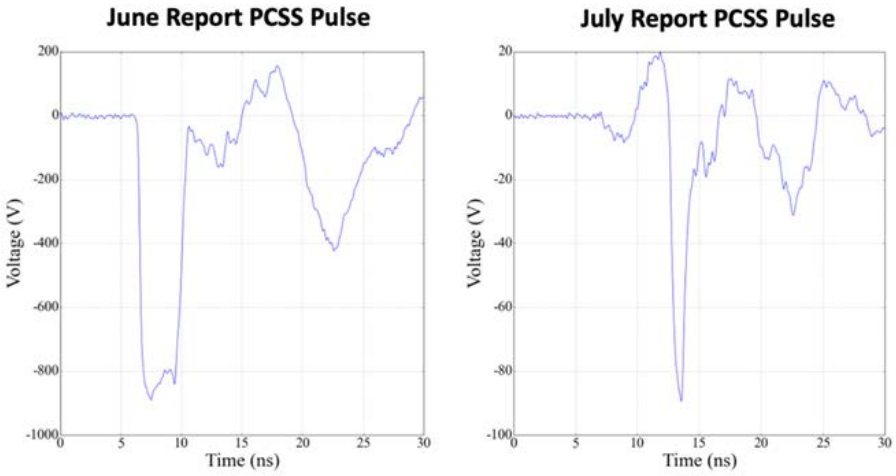
GHz MW D-NLTL Prototype (C):

PCSS-DNLTL simulations indicated that a cell inductance of 3-4 nH would be capable of generating a center frequency greater than 1 GHz when using a PCSS excitation similar to the geometry shown in the left panel of Figure 5.1.2. The PCSS source had several issues, including: arcing at the switch, arcing at the transformer, and inconsistent pulse geometry. It was initially concluded that the impedance transformer on the PCSS transmission line had sustained damage, and the line was rebuilt. The new PCSS transmission line produced an excitation with a full width at half max (FWHM) equal to 1/3 of the July excitation pulse; a comparison of the two pulses is shown in Figure 5.1.2. Arcing was still present at the switch as well resulting in a maximum charge voltage of 1.5 kV. Less charge voltage and a smaller FWHM caused the D-NLTLs to operate with a low pass filter (LPF) characteristic. Comparison of the July results (shown in Figure 5.1.3) and June results (shown in Figure 5.1.4) demonstrate the effect the excitation pulse has on D-NLTL behavior with the June excitation inducing soliton formation and the July excitation causing the LPF characteristic.

There are 2 frequency trends that can be observed in Figure 5.1.3: first, the decrease in inductance caused an increase in Bragg frequency for both lines at all charge voltages; second, in all cases the K100F line produced a larger Bragg frequency than the K50F line. The difference in Bragg frequency between the two lines indicates the presence of frequency losses from the added lead inductance and parasitic capacitance when stacking diodes. Figure 5.1.3 also shows a difference in amplitude between the two lines with the K50F line producing a larger amplitude than the K100F line in all cases. When initially observed with the DSRD-DNLTL tests in the spring it was concluded that an impedance mismatch was causing the difference in amplitude. While that could still be the case as all connections are hand soldered, it is more likely that the staking of diodes is causing either a better line-source impedance match or distributing the pulse amplitude across multiple diodes allows for greater peak amplitudes to be produced.

Next steps for the K50F and K100F based D-NLTLs include a test with the Marx generator pulsed source, as well as a retest with the PCSS based pulsed source. The last observation needed to complete milestone C is a center frequency >1 GHz as measured by the inverse between successive solitons. Simulations indicate that a pulse of dimensions similar to that of Figure 5.1.2 (left) combined with the 3.7 nH inductance

used in this month's tests is capable of pushing the center frequency into the single GHz range as shown in Figure 5.1.5.



	June Pulse	July Pulse
Rise Time	0.44 ns	0.56 ns
FWHM	3.5 ns	1.2 ns

Figure 5.1.2 Comparison of the June and July PCSS test pulses. Each pulse has a similar risetime, however the June pulse has a FWHM nearly 3 times× that of the July pulse.

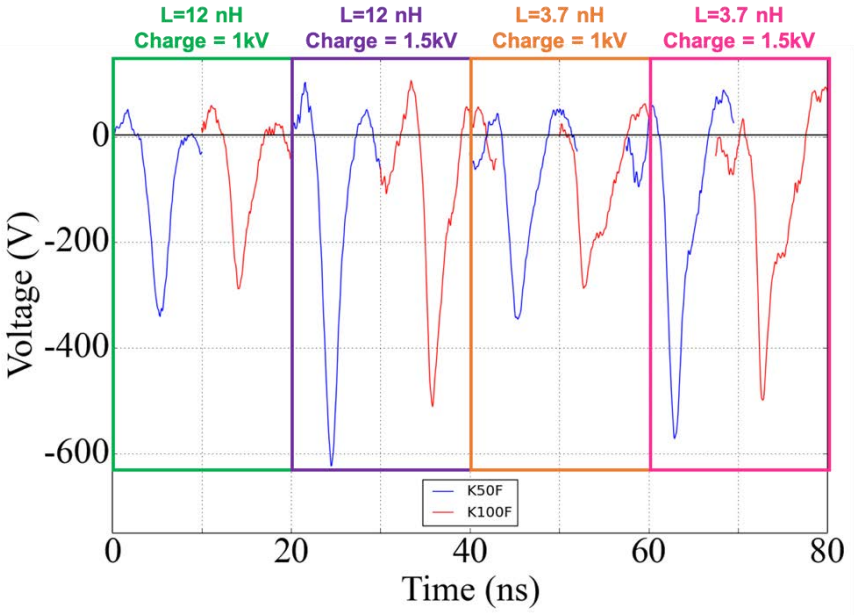


Figure 5.1.3 Waveforms produces for 4 charges of the PCSS from the July PCSS-D-NLTL test. Waveforms are superimposed and separated for viewing ease. Blue represents results for the K50F line, red represents results for the K100F line. Results are paired by the line inductance and charge voltage used to produce each waveform.

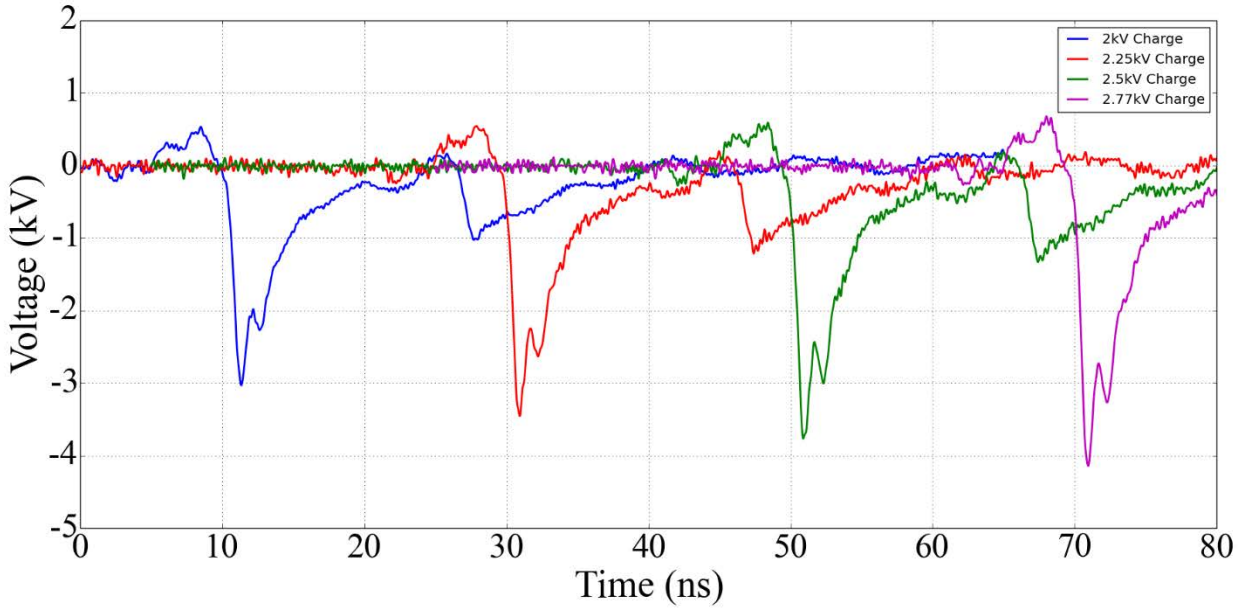


Figure 5.1.4. Waveforms produces for 4 charges of the PCSS from the June PCSS-D-NLTL test. Waveforms are superimposed and separated for viewing ease. In all cases, the network successfully broke the excitation into solitons with a center frequency range of 700–800 MHz and a Bragg frequency of 1.25 GHz.

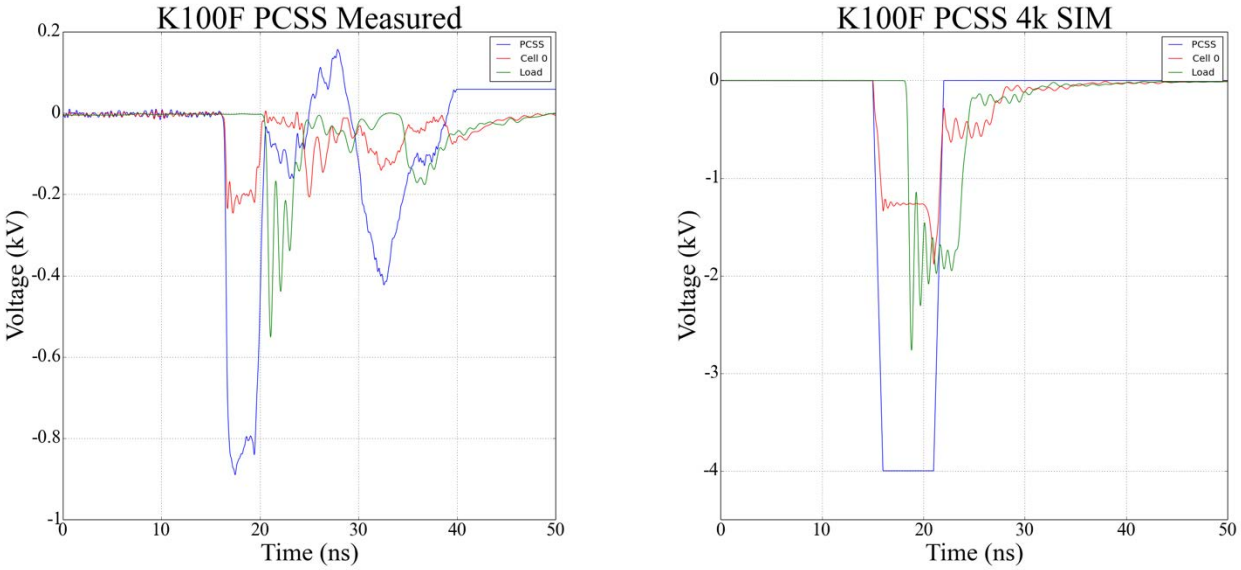


Figure 5.1.5 Measured and simulated waveforms from the 3.7 nH K100F line. In both images blue is the waveform produced by the PCSS, red is the waveform that makes it onto the line, and green is the produced waveform. The left image has a center frequency of 920 MHz, the right image has a center frequency of 1.1 GHz.

5.1.5 Summary of Significant Findings and Mission Impact

(A) After a failure of the high-voltage diode-based nonlinear transmission lines (D-NLTLs) to reproduce simulated results, work refocused on low-voltage D-NLTLs to determine the source of the discrepancy. In NOV2020 a center frequency of ~250 MHz was achieved using a D-NLTL design based on the diode model SMV1702.

(B) Following the success of the SMV1702 D-NLTL, a circuit was designed capable of electrically tuning the center frequency utilizing DC biasing of the diodes. In FEB–APR2021 the circuit demonstrated a linear relationship between DC bias up to a limiting potential. Negative DC biases decreased center frequency while positive DC biases increased center frequency.

(C) In JAN2021 two diode candidates (models K100F and K50F) were identified for a HV D-NLTL design. FEB2021 saw successful tests of both D-NLTLs with each sharpening the rise time of a pulse produced by a DSRD based source down from ~1 ns to ~600 ps.

(D) During MAY2021 a line topology capable of feeding two identical D-NLTLs with the same pulsed source at the same time. Initial results were collected, and a prototype is currently being designed to test the ability to parallelize D-NLTLs.

6.0 Tradespace Analysis of Ultra-Wide-Band Antenna Arrays

6.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

6.1.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wideband (UWB) antenna elements in a phased array for high-power microwave (HPM) transmissions.

Deficiency in SOTA: Large physical aperture size of the antennas.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters, followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area. Using stochastic and machine learning (ML) algorithms to optimize antenna element and array performance.

Relevance to OSPRES Grant Objective: Provides design and optimization guidelines for UWB ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

6.1.2 Tasks and Milestones / Timeline / Status

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN–MAY 2021 / Completed code.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN–MAY 2021 / Completed investigations of arrays on infinite ground planes.

(C) Build minimum viable validation prototypes of single ESA elements on substrates that have good power handling capabilities for HPM transmissions at UHF range (such as FR-4, TMM-10i, TMM-6) / JAN–SEP 2021 / Ongoing time-domain analysis of the designed antenna elements.

(D) Optimization of ESA (single element) performance using regular, and ML based stochastic search algorithms / JUN–SEP 2021 / Ongoing.

(E) Build minimum viable validation prototypes for arrays of ESA elements / JUN–SEP 2021/ Ongoing.

6.1.3 Progress Made Since Last Report

(C) Build minimum viable validation prototypes of single ESA elements:

a. Performed time-domain analysis of the microstrip patch antennas, designed at the UHF range (0.6-1 GHz), via CST Microwave Studio.

b. Modeled a coaxial probe-fed rectangular microstrip patch antenna, via FEKO, on a 0.65-inch-thick polyethylene ($\varepsilon_r = 2.3$) substrate in the UHF range (912.3–969.5 MHz); prototype is being manufactured currently.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

Modeled a 2×2 array of single resonant microstrip patch antennas on a 0.25-inch-thick TMM-10i substrate ($\varepsilon_r = 9.8$), at the center frequency of ≈ 930 MHz; Ongoing manufacturing of the prototype.

6.1.4 Technical Results

(C) Build minimum viable validation prototypes of single ESA elements:

<u>Part 1: Time-domain analysis of the designed UWB microstrip ESAs at the UHF range:</u>

Earlier we have reported (FEB-DEC 2020 ONR-OSPRES-Grant MSR) the modeling and frequency-domain characterization of a single and a 15×15 array of wideband, coaxial probe-fed, microstrip ESA elements, on a 1.05-inch-thick TMM-10i substrate, at the UHF range ($638 - 990.6$ MHz). The single ESA element was shown to have a 43.27% 2:1 VSWR bandwidth with a peak gain of 5.67 dBi.

Time-domain analysis of the single ESA element has been initiated via CST Microwave Studio. A parameter, which can be used to quantify the time-domain performance of an antenna, is the Fidelity Factor (FF), which is defined as the cross-correlation between the transmitted $T_s(t)$ and the received pulse $R_s(t)$, which is represented as:

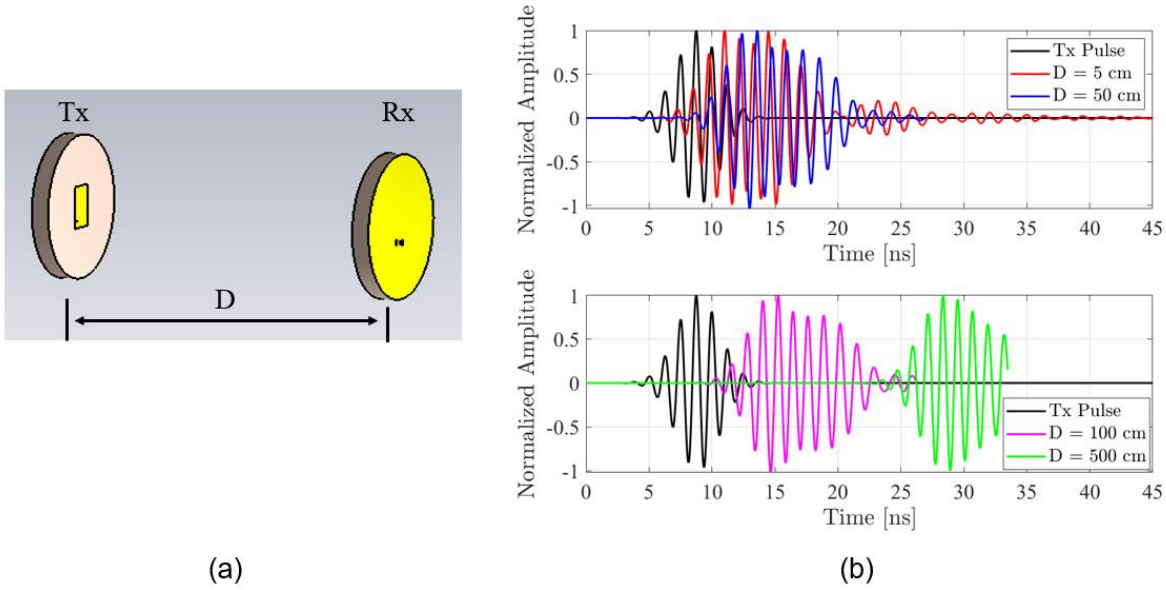
$$FF = \max_{\tau} \left(\left| \frac{\int_{-\infty}^{\infty} T_s(t) R_s(t+\tau) dt}{\sqrt{\int_{-\infty}^{\infty} |T_s(t)|^2 dt} \sqrt{\int_{-\infty}^{\infty} |R_s(t)|^2 dt}} \right| \right). \quad (1)$$

Eq. (1) suggests that, if $FF = 1$, then the received and the transmitted pulses have the exact same shapes.

In this study, we used the default Gaussian pulse that is available in CST as input to the designed antenna. The received pulses were obtained at different distances from the Tx antenna (using an Rx antenna of the same type), and the corresponding FF values were

computed using Eq. (1), via MATLAB. The FF's at different distances are enlisted in Table 6.1.1.

To facilitate comparison, the amplitudes of the transmitted and the received pulses have been normalized. It can be observed from Figure 6.1.1 (b) that the received pulse at $D = 500$ cm has maximum resemblance with the shape of the transmitted pulse. This is also confirmed from the FF value (0.8663), which is found to be maximum at $D = 500$ cm.



(a) (b)

Figure 6.1.1 (a) CST simulation setup of the Tx-Rx antennas (b) transmitted and received pulses.

TABLE 6.1.1: Fidelity Factor (FF) of the UWB microstrip ESA modeled on a circular shaped 1.05-inch-thick TMM-10i substrate in the UHF region ($638 - 990.6$ MHz).

Distance D (cm)	FF
5	0.7563
10	0.8069
50	0.7139
100	0.8130
500	0.8663

Part 2: Building single microstrip ESA prototypes:

It has been shown, in earlier reports, that a simple coaxial probe-fed, microstrip patch ESA element can yield $\geq 30\%$ 2:1 VSWR bandwidth, by strategically placing the feed-probe along $2/3rd$ the patch diagonal. One of the major requirements of such designs is that the feed-probe must have a radius, $r_p \gtrsim 0.005\lambda$ (where λ is calculated at the center frequency f_c of the antenna's operating band). Therefore, at the desired UHF range

(0.6–1.0 GHz) the probe radius must be: $r_p \gtrsim 2$ mm. The commercially available SMA connectors are not suitable to feed the wideband, single layer, microstrip patch ESA designs at the UHF range, as they have $r_p \approx 0.635 - 0.65$ mm.

A plausible solution to this problem is the use of 3D printed customized connectors (with $r_p \gtrsim 2$ mm). However, before using the customized connectors, it was decided to validate the design approach, at the UHF range, using a standard, commercially available, SMA connector ($r_p = 0.635$ mm). For the purpose, a simple coaxial probe-fed microstrip patch antenna element is designed on a 0.65-inch-thick polyethylene ($\varepsilon_r = 2.3$) substrate, at the upper UHF range ($912.3 - 969.5$ MHz). The antenna shows narrowband (6.08% 2:1 VSWR bandwidth) characteristics as $r_p = 0.635\ \text{mm} \approx 0.002\lambda$ (λ being calculated at $f_c = 940.9$ MHz). The antenna geometry and its S_{11} and gain parameters are illustrated in Figure 6.1.2. The prototype is currently being manufactured and a comparison between the simulated and the experimental data will be provided in subsequent MSRs.

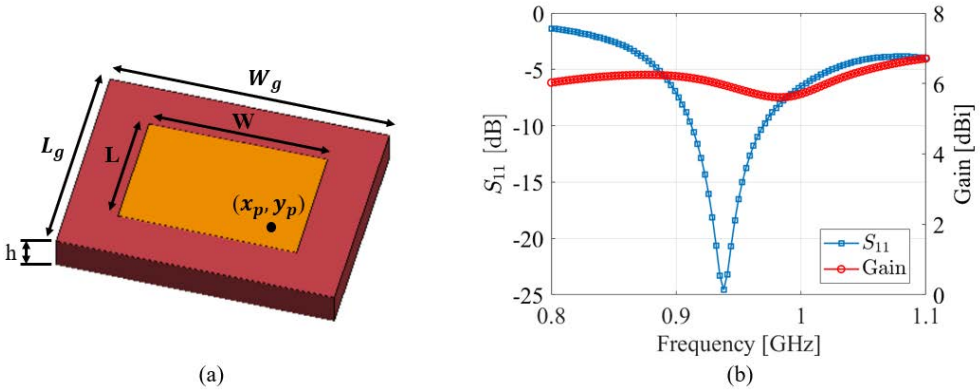
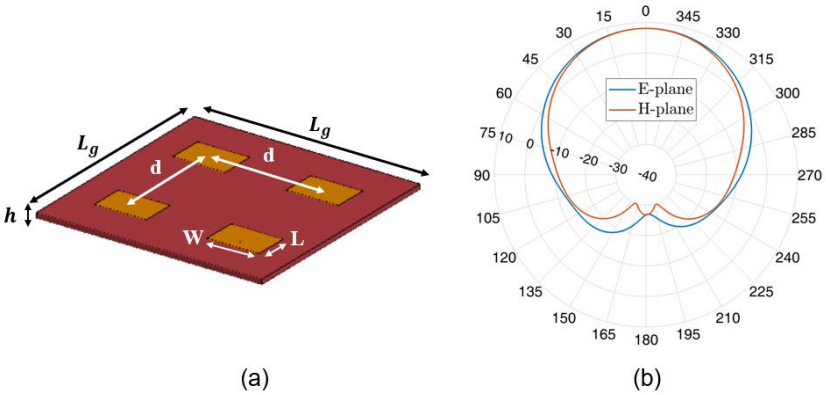


Figure 6.1.2 (a) FEKO simulation model of the coaxial probe-fed microstrip patch antenna on polyethylene substrate ($\text{h} = 0.65", \text{L}_\text{g} = 5", \text{W}_\text{g} = 6", \text{L} = 65.86\ \text{mm}, \text{W} = 98.79\ \text{mm}, (x_p, y_p) = (21.95\ \text{mm}, 32.93\ \text{mm}), r_p = 0.635\ \text{mm}$); (b) Reflection coefficient and gain of the antenna.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

To experimentally validate the array design approach at the UHF range ($0.6 - 1$ GHz), a 2×2 array of single resonant microstrip patch antennas has been modeled to operate at ≈ 930 MHz, on a 0.25-inch-thick TMM-10i substrate ($\varepsilon_r = 9.8$). Like the single element validation approach, followed in (C), standard SMA connectors ($r_p = 0.635\ \text{mm}$) have been used to feed the patches. The CAD model of the array is shown in Figure 6.1.3 (a). At the center frequency, $f_C = 930.71$ MHz, the boresight gain is 8.08 dBi. Manufacturing of the prototype is ongoing.



(a) (b)

Figure 6.1.3 (a) CAD model of the 2×2 array of coaxial probe-fed microstrip patch antennas on a square-shaped TMM-10i substrate $(\mathrm{h} = 0.25", \mathrm{L_g} = 10", \mathrm{L} = 1.84", \mathrm{W} = 2.77", \mathrm{d} = 5", r_p = 0.635\ \mathrm{mm})$; (b) E- $(\phi = 0°)$ and H- $(\phi = 90°)$ plane radiation patterns of the array at 930.71 MHz.

6.1.5 Summary of Significant Findings and Mission Impact

(A) Developing Array Pattern Tool for large arrays calculations:

A MATLAB code has been developed for faster approximation of radiation pattern of a linear/planar array of any size and composed of any type of antenna elements. The code requires the center element pattern of a small array (say, 3×3) composed of the same type of antenna elements, desired lattice arrangement, and total number of array elements, as user inputs. This work will be included in future publications.

(B) Investigate the effects of array aperture area reduction on different array parameters:

The effect of different array aperture area and lattice arrangements on the array parameters (such as array gain, beamwidth, electronic beam steerability, etc.) have been reported for arrays modeled on infinite ground planes (DEC 2020 ONR-OSPRES-Grant MSR). The results show that, with 30% reduction in the aperture area ($\approx 50\%$ reduction in # of elements), the gain drops by < 3.5 dBi without any scan blindness spotted as the main beam is steered from boresight to $\pm 60°$ in the $640 - 990$ MHz range.

The array parameters for large arrays ($\geq 15 \times 15$) on finite ground planes could not be computed using the commercial EM solvers (FEKO and CST) due to excessive memory and time consumption. This work will be resumed after developing a method to estimate array performances on finite ground planes, either through ML or conventional approaches.

(C) Build minimum viable validation prototypes of single ESA elements:

Investigated different bandwidth enhancement techniques applicable to single layer microstrip patch ESAs:

a. Method I: Bandwidth enhancement by strategically placing the coaxial probe along 2/3rd of the patch diagonal – This method is proposed and experimentally validated using prototypes manufactured on TMM-6 and TMM-10i substrates at $2.5 - 5$ GHz.

An antenna has been modeled on a G10/FR-4 substrate, at the UHF range ($0.6-1$ GHz), and is being considered for manufacturing.

b. Method II: Coaxial probe-fed U-slot loaded rectangular microstrip ESAs – A prototype is manufactured on a G10/FR-4 substrate ($0.9-1.3$ GHz) and tested.

c. Method III: L-probe-fed U-slot-loaded rectangular microstrip ESAs – An antenna has been modeled on a TMM-4 substrate that operates in the $0.52-1.17$ GHz range ($\approx 77\%$ 2:1 VSWR bandwidth). Due to fabrication complexity of the L-probe proximity coupled feed, this antenna will not be manufactured.

(D) Optimization of ESA (single element) performance using regular, and ML based stochastic search algorithms:

Investigated the bandwidth enhancement of the coaxial probe-fed microstrip patch antennas, using regular and ML based stochastic search algorithms (GA, PSO, and Simplex methods), by optimizing the feed-probe location and ground plane shape and size. Compared to regular search algorithms, ML algorithms are found to be less computationally intensive (in terms of time and memory consumption).

(E) Build minimum viable validation prototypes for arrays of ESA elements:

A 3×3 array of microstrip ESA elements, on a TMM-10i substrate, has been manufactured and tested at the $2.5-5$ GHz range. We have modeled and submitted a work order for manufacturing a 2×2 array of narrowband microstrip ESAs, on a 0.25" TMM-10i substrate, for operation at the UHF range ($0.9-1$ GHz).

6.1.6 References

[1] D. R. Jackson, *Introduction to Microstrip Patches,* IEEE International Symposium on Antennas and Propagation and USNC-URSI National Radio Science Meeting. Jul. 2013.

6.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna

(Kalyan Durbhakula)

6.2.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelev antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem: The total surface currents on the Koshelev antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not yet clearly understood.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelev antenna that effectively reduce its physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelev antenna has been shown in the literature to withstand higher voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelev antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelev antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelev antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelev antenna.

(iii) The large electrical size (>5λ) of the Koshelev antenna at its highest operating frequency poses huge computational challenges. Efforts are underway to cleverly select important design parameters for the tradespace study.

6.2.2 Tasks and Milestones / Timeline / Status

(A) Complete literature search to identify and list antenna elements that satisfy UWB properties and HPM requirements, and down select accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelev antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB–MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design

and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t, \phi, \theta)$) in receive or transmit mode / MAR–APR21 / Complete.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelev antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / MAR21/ Complete.

- Milestone: Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain over the desired bandwidth, and aperture efficiency.

(F) Reduce Koshelev antenna aperture size (H×W) to equal to or less than 90 mm × 90 mm, equal to that of the SOTA BAVA, for direct antenna metrics comparison / MAR–APR21 / Complete.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, aperture efficiency equal to or greater than 130% at 900 MHz.

(G) Using the optimized model from (F), build various array simulation models/topologies to perform a tradespace study and report tradeoffs between array antenna metrics such as center element reflection coefficient (S11) value, gain vs theta at constant phi, physical aperture area, aperture efficiency, and rE/V / MAY–JULY21 / Ongoing.

- Milestone: Develop/showcase an optimized Koshelev array model that exceeds an aperture efficiency of 130% with a high rE/V.

(H) Perform literature search to investigate, understand, and determine the applicability of special electromagnetic (EM) techniques to the antennas under consideration. / JAN–APR21 / Complete.

(I) Explore different impedance taper (microstrip based and coax based) designs that can interface well (both mechanically and electrically) to transition the signal from a coax cable to the input of the Koshelev antenna element **(NEW)** / JULY21–AUG21 / Ongoing.

- Milestone: Recommend the optimum impedance taper design (with minimum reflections and maximum power transfer) with the optimum dimensions to successfully convert the high-voltage, short-rise time input signal from a coax cable to the feed of the Koshelev array.

6.2.3 Progress Made Since Last Report

(G) In the last month, the interelement spacing variables in both axes (S_x and S_y) for the diamond Koshelev array have been varied to study and understand their effect on S11

value, gain as a function of elevation angle (θ), and time domain electric field at 10 meters. If the S_x is varied along a range, the S_y is kept constant and vice-versa. Figure 6.2.1 shows the diamond Koshelev array with non-symmetric interelement spacing variables.

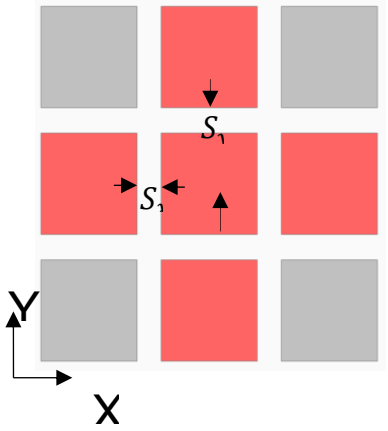
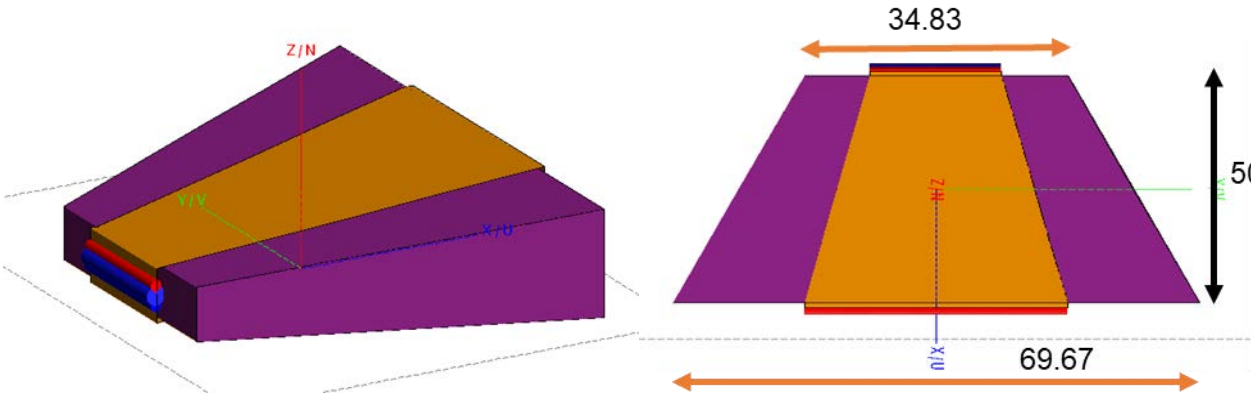


Figure 6.2.1 Diamond Koshelev array antenna with non-symmetric interelement spacing values.

(I) A linear microstrip based impedance taper has been designed and simulated for its S11 value using Altair FEKO. The impedance taper is designed to take coax input on one end and will be connected to exponential flares of the Koshelev antenna element on the other end. Both ends of the impedance taper are designed to have 50 ohms impedance. Fig. 6.2.2 shows the FEKO model of the microstrip based impedance taper with its dimensions. As it can be seen the width of the microstrip and height of the substrate are linearly increased to maintain 50 ohms impedance from start to end.



(a) (b)

Figure 6.2.2 Linear microstrip based impedance taper design (a) Isometric view, and (b) Top view.

6.2.4 Technical Results

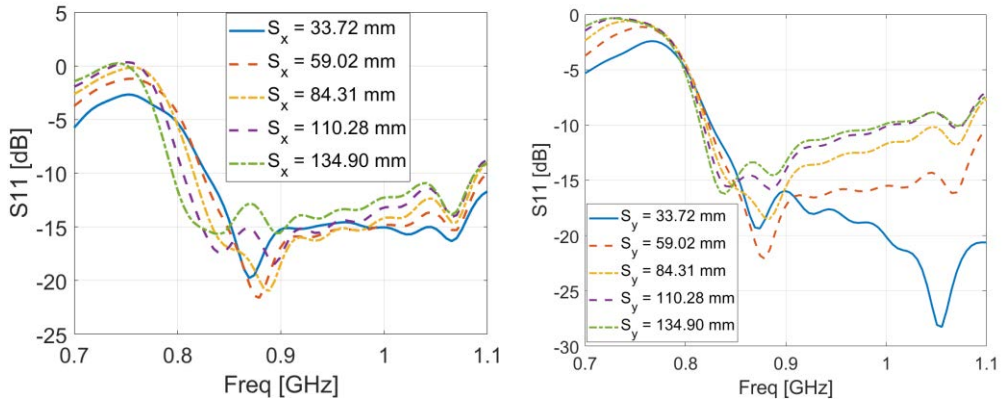
(G) The element spacing in the time domain is determined by the pulse duration, which is given by the following equation:

$$S_x = K_x \tau_p c_0$$

$$S_y = K_y \tau_p c_0$$

where S_x & S_y are the interelement spacing variables in the x-axis and y-axis. In (1), K is a numeric constant, τ_p is the pulse duration, and c_0 is the speed of light in m/s. For the first study, we kept the value of K_y= 0.464 and varied $K_x$from 0.25 ns to 1. For the second study, we kept the value of K_x= 0.464 and varied K_y from 0.25 ns to 1. An optimum K_x & K_y value have been identified. The criterion for optimum output is set when the S11 value stays below the –10 dB line over as wide a bandwidth as possible centered around 900 MHz. In conjunction with the S11 value, the gain pattern with minimum side lobe can also be considered as the optimum variable.

The first array antenna metric that must be taken into analysis is the reflection coefficient as a function of frequency. The range of frequency is concentrated only from 700 MHz to 1100 MHz. In Figure 6.2.3, the S11 value of the center most element of the diamond Koshelev array has been plotted for the two studies mentioned above. Figure 6.2.3 (a) shows the S11 value for constant S_y and variable S_x, while Figure 6.2.3 (b) shows the S11 value for constant S_x and variable S_y.



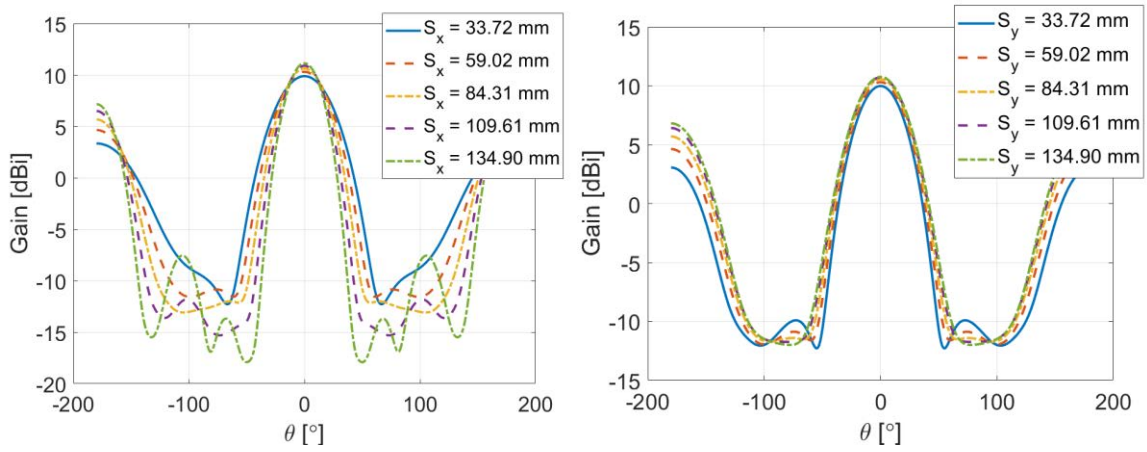
(a) (b)

Figure 6.2.3 (a) S11 value of center element of diamond Koshelev array over the desired frequency range for different S_x values with a constant S_y (= 62.59 mm) value, and (b) S11 value of center element (#3) of diamond Koshelev array over the desired frequency range for different S_y values with a constant S_x (= 62.59 mm) value.

In Figure 6.2.3 (a), the bandwidth calculated at a center frequency of 900 MHz shifted left as the value of S_x increased. The shift is significant at the lower frequency end of the spectrum than at the higher frequency end of the spectrum. Therefore, an intermediate value between 84.31 mm and 110.26 mm can be chosen as the optimum value of S_x. On

the other hand, Figure 6.2.3 (b) showed a significant change in the S11 value as the value of S_y is varied while keeping S_x constant. It is evident that the maximum bandwidth in Fig. 6.2.3(b) is obtained by the smallest S_y value. However, as mentioned in the previous MSRs, the gain as a function of frequency increases with spacing, which also cannot be neglected in determining an optimum interelement spacing value. Therefore, an optimum S_y value around 84.31 mm can be chosen.

The next important array antenna metric is the gain as a function of elevation angle. This is otherwise known as the radiation pattern, which can be plotted as a 3D radiation pattern or as a 1D cartesian plot. Figure 6.2.4 (a) shows the 1D radiation pattern for a range of S_x values, whereas Fig. 6.2.4(b) shows the 1D radiation pattern for a range of S_y values. In Figure 6.2.4 (a), as the value of S_x is increased, the peak gain at θ = 0° increased as expected and the side lobes (region of gain between –100° to –50° and between 50° to 100°) were minimum for the largest value of S_x. The change in half-power beamwidth (HPBW) in Figure 6.2.4 (a) is also significant and noticeable. In Figure 6.2.4 (b), the change in S_y did not affect the gain value unlike in Figure 6.2.4 (a). Furthermore, the side lobes, and the HPBW did not vary much when the value of S_y is varied.

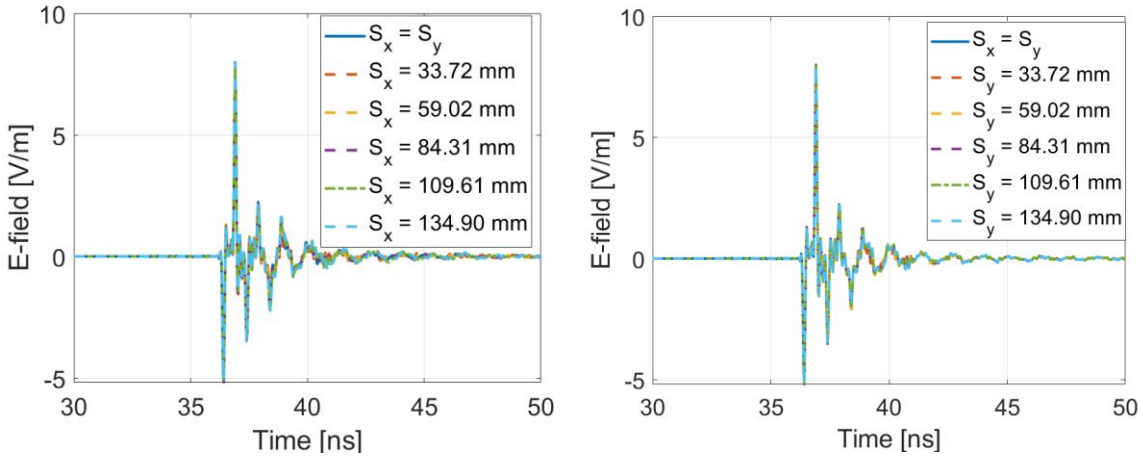


(a) (b)

Figure 6.2.4 (a) Gain as a function of elevation angle (θ) for diamond Koshelev array antenna for different S_x values with a constant S_y (= 62.59 mm) value at 900 MHz, and (b) Gain as a function of elevation angle (θ) for diamond Koshelev array antenna for different S_y values with a constant S_x (= 62.59 mm) value at 900 MHz.

Finally, we excited the diamond Koshelev array antenna with a 900 MHz time domain input signal (resembles a damped rectangular wave) and obtained the time domain radiated electric field at a distance of 10 meters. Figure 6.2.5 shows the time domain radiated electric field at this distance as the values of S_x and S_y are varied. No big improvements or deviations were identified in the overall radiated electric field or peak-to-peak radiated electric field. However, on a miniscule scale of comparison of these results, we found the interelement spacing value of 84.31 mm (for both S_x and S_y) to be

the optimum value. The signal shape and the frequency content of the input pulse has been retained by the diamond Koshelev array.



(a) (b)

Figure 6.2.5 (a) Time domain radiated electric field for different S_x values with a constant S_y (= 62.59 mm) value at 10 meters and (b) Time domain radiated electric field for different S_y values with a constant S_x (= 62.59 mm) value at 10 meters.

(I) A linear microstrip based impedance taper has been designed and simulated. Figure 6.2.6 shows the S11 value at the coax end of the impedance taper. The coax end is the end with the 17.41 mm trace width and the other end is connected to the feed of the Koshelev antenna element. The S11 value over the frequency range of interest in Figure 6.2.6 shows good response i.e., S11 < –10 dB between 600 MHz and 3 GHz.

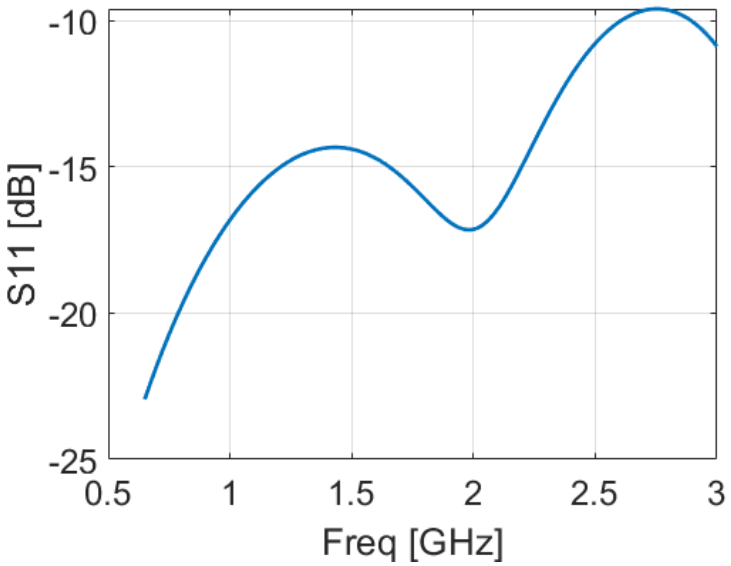


Figure 6.2.6 S11 value of the linear microstrip based impedance taper.

6.2.5 Summary of Significant Findings and Mission Impact

(A) An extensive literature search on various UWB antenna elements has resulted in finding three promising options. The down-selected elements are the Koshelev, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the single antenna element. Later, the single antenna element will be converted into a planar array.

(B) Initial validation of the Koshelev antenna simulated using CST software agreed well with the antenna metrics published in the open literature [1]. A UWB bandwidth response (10:1 bandwidth) and rE/V > 1 has been observed from our initial simulations of the Koshelev antenna. This validation ensured that the Koshelev antenna can be subjected to further tradespace studies to understand its performance followed by optimizing the design according to OSPRES grant requirements.

(C) The initial tradespace study and analysis of the Koshelev antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between the Koshelev antenna in [1] and aperture reduced Koshelev antenna are shown in Table 5.2.1 of the APR 21 MSR.

(D) An in-house code has been developed to calculate important UWB time domain antenna metrics such as full-width half maximum (FWHM) and ringing. These metrics have been calculated using in-house MATLAB code using the excitation voltage and radiated electric field information obtained from CST simulations. FWHM and ringing antenna metrics help with assessing or characterizing an antenna's UWB response.

(E) The tradespace study of feed position provided a deeper understanding of how its position impacts the S11 value bandwidth. An optimum value for feed position i.e., $F = 1/20 < L < 1/10$ is recommended to achieve maximum bandwidth. The tradespace study of the antenna length (L) is straightforward. A longer antenna length will radiate better at lower frequencies. However, physical size restrictions/requirements must be kept in mind in determining the antenna length. Finally, a larger α value (>120°) is recommended to avoid unnecessary reflections from the electric monopole.

(F) From a thorough tradespace study, the aperture size of the Koshelev antenna (single element) is determined to be 90 mm × 100 mm in order to achieve desired antenna metrics performance proposed in the milestone.

(G) The physical aperture area of the Koshelev array antenna largely depends on the interelement spacing and the shape of the array. We were able to determine that the diamond topology is the optimum shape for the Koshelev array antenna. From the initial tradespace study of interelement spacing, we were able to observe that a particular value of pulse duration is optimal to feed into the diamond Koshelev array for maximum radiation. Pulse duration slightly shorter or longer would be inefficient. Moreover, with the diamond Koshelev array, by making only element#3 passive we were able to obtain similar gain characteristics as a function of elevation angle as the all elements active. A study on non-symmetric interelement spacing values for the diamond Koshelev array yielded that the array antenna metrics are more sensitive to the value of S_x than to the value of S_y. Therefore, when designing the Koshelev array, the focus must be laid on the S_x interelement spacing value which has a greater control on the gain and bandwidth. We

expect the same response from other Koshelev array antenna shapes such as the square, hexagon, octagon, and ellipse. Therefore, a smaller S_y value and an optimum S_x value must be chosen to reduce the physical aperture area of the Koshelev array.

(H) The literature search on the special EM techniques expanded our knowledge and opened door of opportunities to apply some of those techniques to antennas under study. EM techniques such as non-symmetric and non-square array topologies have been applied to the development and study of Koshelev array antenna.

(I) The first impedance taper design under consideration has shown good S11 value over the frequency range of interest and is currently being fabricated and integrated with the Koshelev single element prototype.

6.2.6 References

[1] Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

6.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna

(Sadie Brasel and Kalyan Durbhakula)

6.3.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of Shark antenna elements whose miniaturization in two dimensions (height and width equal to $\lambda/4$ where λ corresponds to the lowest operating frequency) make it a good candidate for UWB HPM systems while having a reduced aperture area with respect to the current state-of-the-art. In the literature, the Shark antenna has already been shown to achieve a wide 20:1 impedance bandwidth, low dispersion, and a sectoral (also referred to as directional) radiation pattern.

Sub-Problem: The design parameter space of the Shark antenna has not been studied rigorously in the literature and therefore the effect of these parameters on the antenna metrics is not understood. In addition, the Shark antenna has been shown to be not very directive in the H-Plane. Preliminary studies have shown that aperture efficiencies at low frequencies are much better than at higher frequencies.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Explore the design parameter space for the Shark antenna element using computational electromagnetic (EM) wave solvers starting with the simulation and validation of a single element.

Relevance to OSPRES Grant Objective: The Shark antenna dimensions were established to be frequency dependent and can be readily modulated to fit the spectrum characteristics of an ultra-fast rise time input pulse.

Risks, Payoffs and Challenges:

(i) The Shark antenna is comprised of flare-angle-dependent bicones that are truncated in the azimuthal angle. This still yields considerably higher half power beam width (HPBW) than other antenna elements under investigation. The significant reduction of HPBW in the H-plane may be unattainable and can be considered a major risk.

(ii) Payoffs include the development of a library of antenna metrics data for various shapes and sizes of the bicones and reflector plates in the shark antenna.

(iii) Computational challenges remain present with respect to automation of design parameter space on our currently used supercomputer (LEWIS). Design challenges persist in obtaining lower operating frequencies while not increasing the height of the antenna and surpassing the 90 mm × 90 mm size requirement.

6.3.2 Tasks and Milestones / Timeline / Status

(A) Complete initial design, simulation, and validation of the Shark antenna / JAN21 / Complete.

(B) Validate Shark antenna design using the LEWIS supercomputer over a wider range of frequency results (up to 20 GHz) / FEB–MAR21 / Complete.

(C) Identify Shark antenna design parameters which contribute significantly to bandwidth, gain, and physical aperture area. Determine which parameters contribute most to performance improvement/size reduction/ FEB–MAR21 / Complete.

(D) Perform a tradespace study by simulating the Shark antenna with varying cases of flare angle, cone length, and distance to backplane. Gain a general understanding of how these parameters affect impedance bandwidth, rE/V, gain and HPBW / FEB–MAY21 / Complete.

- Milestone: produce a detailed summary of change in impedance bandwidth, rE/V, HPBW in H-plane and E-plane as a function of flare angle (α), cone height (*h*), and distance to backplane (*d*) / Complete.
- Milestone: Choose optimal Shark antenna design that has the lowest operating frequency within size requirements based on tradespace study / Complete.

(E) Using the optimal Shark antenna design in (D), simulate various array geometries including hexagonal, rectangular, and circular arrays. Determine which array geometries are optimal and analyze aperture fields and aperture efficiencies. / MAY–JULY21 / Ongoing.

- Milestone: Produce a report which states the effects of various array geometries for the Shark antenna. The optimal array geometry chosen should have the least interference between elements, therefore yielding higher impedance bandwidth and higher aperture efficiency. Overall, the optimal Shark array geometry should have at least 20% impedance bandwidth at 900 MHz center frequency for the center most element with 130% array aperture efficiency, ± 60 degrees beam steering capability, and rE/V equal to or greater than 4.

(F) Begin prototyping and validation of optimal Shark antenna single element. / JUN–AUG21 / Ongoing.

- Milestone: have a finished Shark antenna prototype. Compare S11 and radiation pattern with simulated Shark antenna.

6.3.3 Progress Made Since Last Report

(E) A 13 element diamond Shark antenna array has been simulated. An elliptical array has also been simulated with 12 elements to be compared with the diamond array.

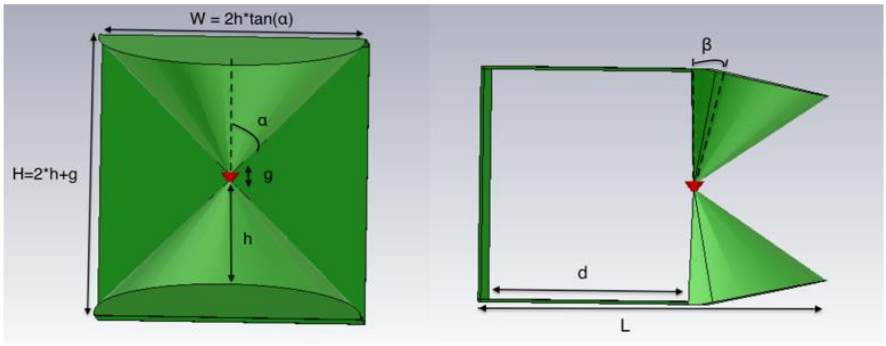
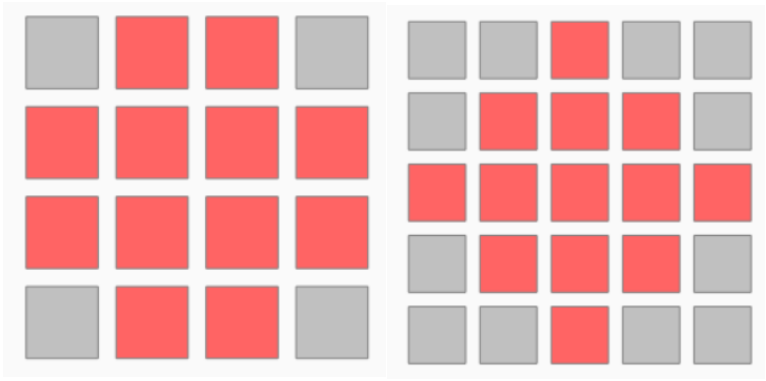


Figure 6.3.1 Shark antenna design parameters: *d, h, g,* α*,* β.

(F) The 50 Ω Shark antenna design was too large for 3D printing. Therefore, an impedance taper has been designed to transform 50 Ω to 150 Ω and the original optimal design from (D) is utilized.

6.3.4 Technical Results

(E) Two additional Shark antenna arrays have been simulated. Both have a larger number of elements as compared to those presented in last month's MSR, with 12–13 antenna elements. Figure 6.3.2 shows the geometries of the two new Shark arrays.



(a) (b)

Figure 6.3.2 (a) 12 element elliptical Shark antenna array (b) 13 element diamond Shark antenna array.

Figure 6.3.3 shows the reflection coefficient of the first elements of the Shark antenna arrays. The diamond array has a slightly better S11 as the top and bottom elements are more isolated than those of the 12 element elliptical array shown in Figure 6.3.2.

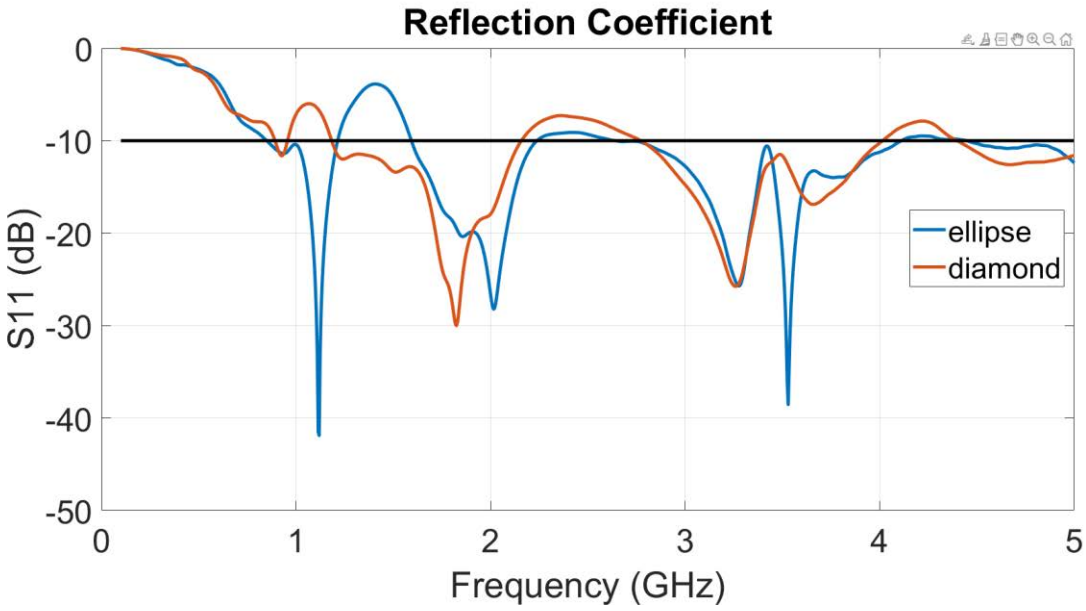


Figure 6.3.3 Reflection coefficient of elliptical and diamond arrays.

Figure 6.3.4 shows the gain vs. frequency plots for both the elliptical and diamond arrays. The diamond array has one more antenna element than the elliptical array, so it follows that it has a slightly higher gain over the entire frequency range.

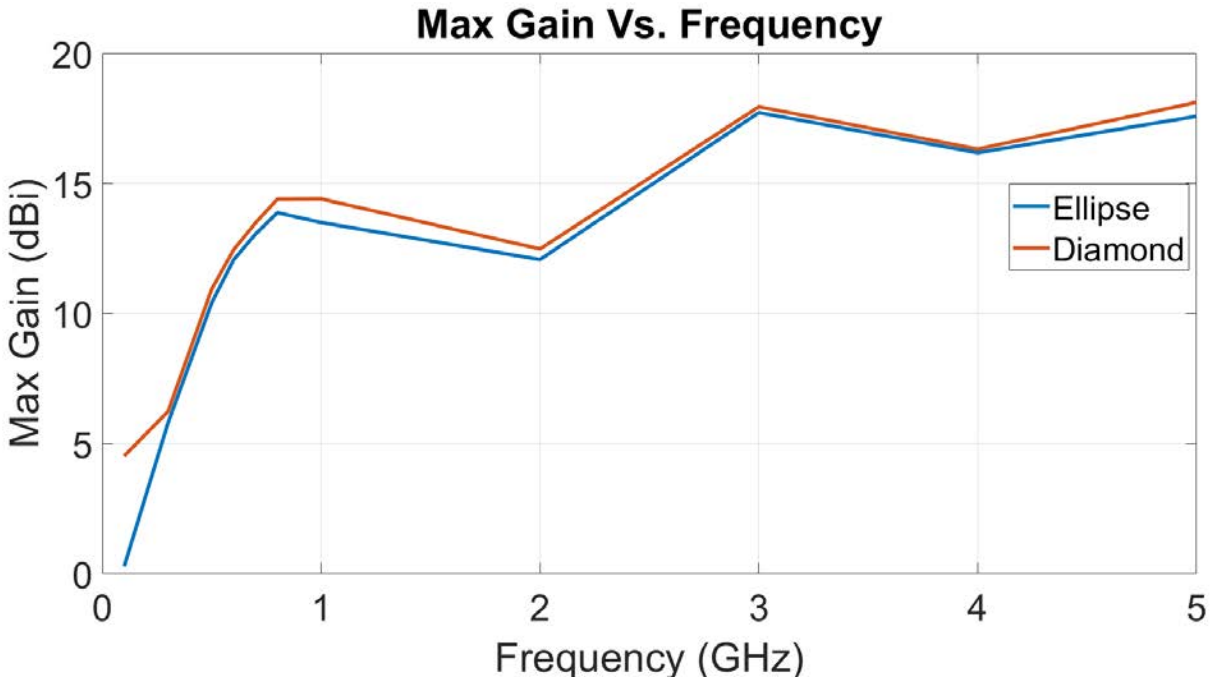


Figure 6.3.4 Max gain vs. frequency.

Figure 6.3.5 shows the radiation pattern of the arrays in the H-plane. It can be seen that the diamond geometry is more directive as it has lower side lobe levels in the 50–150° range.

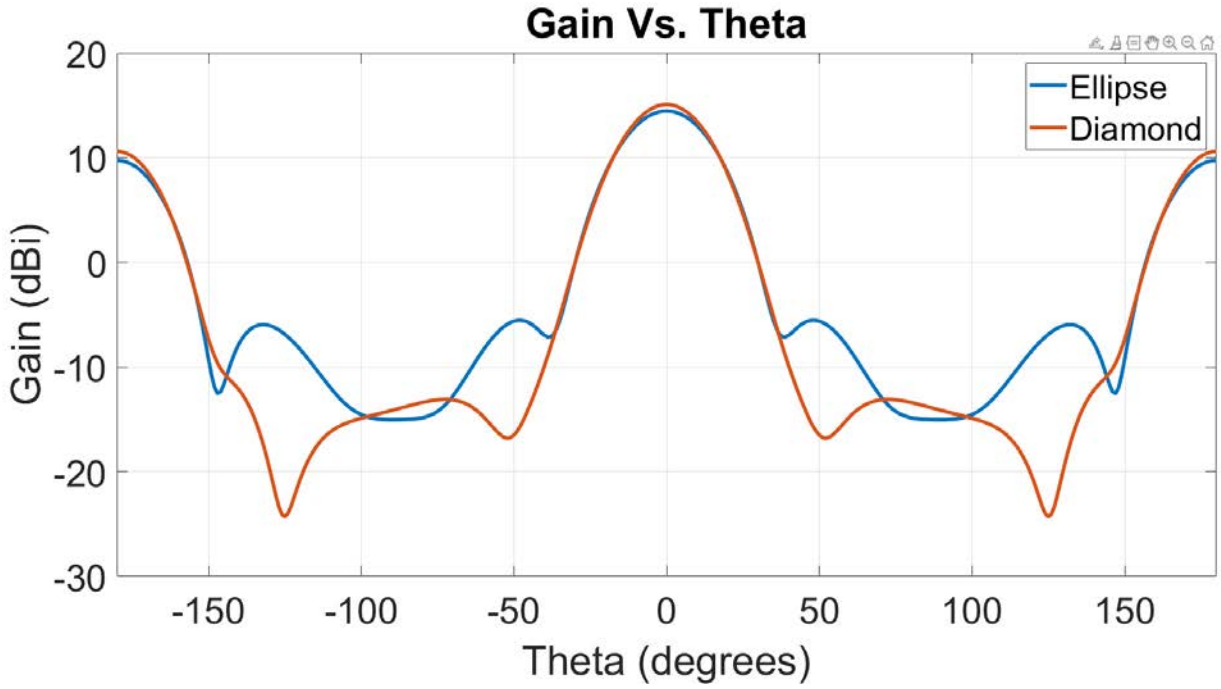


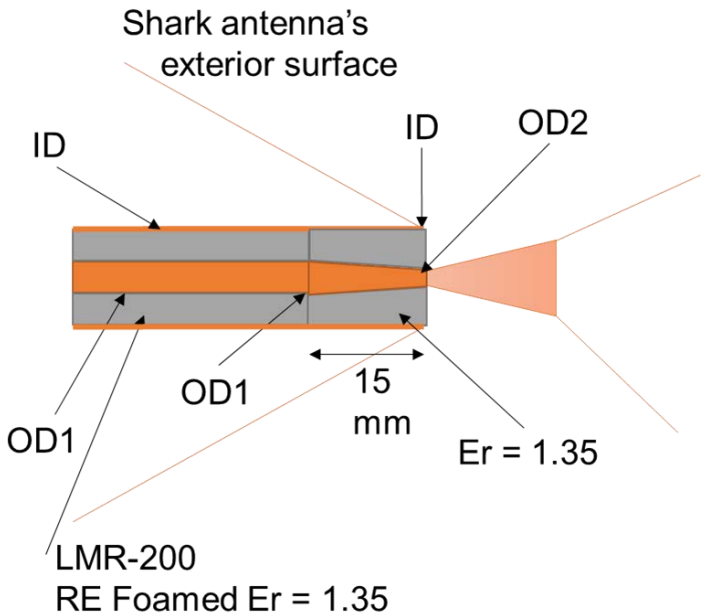
Figure 6.3.5 H-field 900 MHz radiation patterns (phi = 0°).

Table 6.3.1: Performance comparison of Shark array geometries.

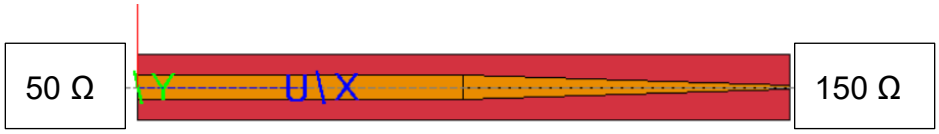
Geometry	# of Elements	Apperture Area	max gain (900MHz)	Effective Aperture	Aperture Efficiency	rE/V (10m)	HPBW (E-field)	HPBW (H-field)
square	9	0.211665	12.719	0.11246065	53.1314	9.15	40.2	36.2
hexagon	8	0.19798	11.728	0.10369829	52.3782	8.122	22	32.4
ellipse	8	0.20978	12.408	0.10971081	52.298	8.05	24	40
diamond	13	0.3491737	14.4	0.12732395	36.4644	13.12	24	27
ellipse	12	0.308	13.7	0.1211346	39.3294	12.14	22.4	29

The 13-element diamond array only has a slight increase in gain as compared to the 12-element elliptical array. Therefore, the elliptical array has a 4% better aperture efficiency than the diamond array. The diamond array however has a more directive pattern in the H-plane.

(F) As the 50 Ω input impedance Shark antenna design was too large for the 3D printer. The original 150 Ω input impedance Shark antenna design will be used with a coaxial linear impedance transformer. Figure 6.3.6 shows the designed geometry in FEKO. Table 6.3.1 outlines all of the design parameters for the proposed impedance transformer. The dielectric inner diameter is kept constant along the length of the cable while the inner conductor outer diameter is varied along the length of the cable to vary the impedance smoothly from 50 Ω to 150 Ω. Validation of the design is underway.



(a)



(b)

Figure 6.3.6. Impedance taper (a) design schematic (b) sliced FEKO model side view.

Table 6.3.2: Summary of impedance taper design variables.

Metric	Value (mm)
ID	2.95
OD1	1.12
OD2	0.161
Substrate Permittivity	1.35

6.3.5 Summary of Significant Findings and Mission Impact

(A-B) The Shark antenna has been designed, simulated, and validated according to [1]. (Figure 6.3.1)

(C) The Shark antenna design parameters that have been found to contribute significantly to bandwidth performance, directivity, and gain are the cone height (*h*) and distance to backplane (*d*).

(D) The Shark antenna tradespace study has been completed and has provided insight into the Shark antenna design space. Increasing the cone height *h* yields better impedance bandwidth at low frequencies and is more directive in the *e* and *h* planes. However, increasing *h* results in a larger aperture area. To remain within 90 x 90 mm, the maximum *h* value is 45 mm; with this a lowest operating frequency of 815 MHz is achievable.

(E) Square and hexagon Shark arrays have been simulated in CST. The square array was simulated with and without connected ground planes to study how this affects performance. The approach of connected ground plane for the square Shark array improves the gain by 1 dBi over unconnected ground plane. The 1 dBi improvement from 11.6 dBi to 12.7 dBi is a decent improvement, therefore connected ground plane arrays are used moving forward.

The study of array geometries has also confirmed that aperture efficiency decreases as more elements, and therefore more aperture area, is added to the array. The aperture efficiency metric is best used to compare arrays with the same or similar number of antenna elements. The square antenna array can also be ruled out as it has been shown

to be much less directive in the E and H planes compared to the other geometries listed in Table 6.3.1.

6.3.6 References:

[1] L. Desrumaux, A. Godard, M. Lalande, V. Bertrand, J. Andrieu and B. Jecko, "An Original Antenna for Transient High Power UWB Arrays: The Shark Antenna," in IEEE Transactions on Antennas and Propagation, vol. 58, no. 8, pp. 2515- 2522, Aug. 2010, doi: 10.1109/TAP.2010.2050418.

6.4 Tradespace Analysis of Ultra-Wide-Band (UWB) Fractal Antenna

(Sai Indharapu and Kalyan Durbhakula)

6.4.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. The fractal antenna packs multiple resonances closely spaced together to generate an UWB response, thereby effectively utilizing the 2D space (i.e., the radiating patch space). Its high degree of freedom provides an opportunity to develop systematically modified patch shapes, which in turn leads to improved bandwidth while retaining high fidelity factor values.

Sub-Problem: Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same

board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

6.4.2 Tasks and Milestones / Timeline / Status

(A) Perform tradespace analysis of the fractal element radius *b* over the desired frequency range (4 to 12 GHz) using the genetic algorithm (GA) optimization tool available in the commercial electromagnetic (EM) solver FEKO / FEB21 / Complete.

- Milestone: Provide a recommendation of an optimum value of *b* using OPTFEKO to minimize reflection coefficient or S11 (< –10 dB).

(B) Perform tradespace study on different fractal shapes by changing the number of fractal segments to understand the effect of this change on the impedance bandwidth / FEB21 / Complete.

- Milestone: Produce a detailed study of the antenna response such as S11, gain, and bandwidth by varying the number fractal segments.

(C) Apply the GA optimization tool on the fractal side length *b* over a wide frequency range (2 to 12 GHz with 201 discrete frequency points) and number of fractal segments using OPTFEKO on the LEWIS cluster / MAR21 / Complete.

- Milestone: Reduce physical aperture area by 10% of its present design, reported in the FEB MSR, and demonstrate minimal or no change in S11, gain, and fidelity factor values.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a* / MAR–APR21 / Complete.

- Milestone: Recommend a value of *a* to reduce the physical aperture area and increase aperture efficiency (>50%) with no variation in other antenna metrics.

(E) Frequency scale fractal antenna design such that the center frequency of the resulting antenna equals 1.3 GHz / MAY21 / Complete.

- Milestone: Modify antenna design with a center frequency equal to 1.3 GHz and achieve similar results (3:1 bandwidth at fc = 1.3 GHz, 3 dBi gain and >130% aperture efficiency at 900 MHz) to antenna design at center frequency ~7 GHz.

(F) Design and simulate various array antenna geometries composed of optimized fractal antenna elements (obtained from (E)) to analyze the effect of overall array antenna geometry on the desired array antenna response metrics (i.e., gain vs. frequency, gain vs. elevation angle at constant phi, rE/V, half-power beamwidth and side-lobe level.) / MAY–JUL21 / Ongoing

- Milestone: Recommend a best possible structure with reduced aperture area and minimal loss in gain.

(G) Apply machine learning (ML) models available in Altair Hyperstudy (2021) on the fractal antenna to try and understand the possibilities and limitations of ML models for fast and efficient antenna metrics prediction and optimization. Through successful testing, a ML model can replace conventional EM simulators for faster optimization and prediction. / MAY–OCT21 / Ongoing.

- Milestone: Recommend most accurate and efficient ML model available in Altair Hyperstudy (2021) for array antenna metrics prediction.

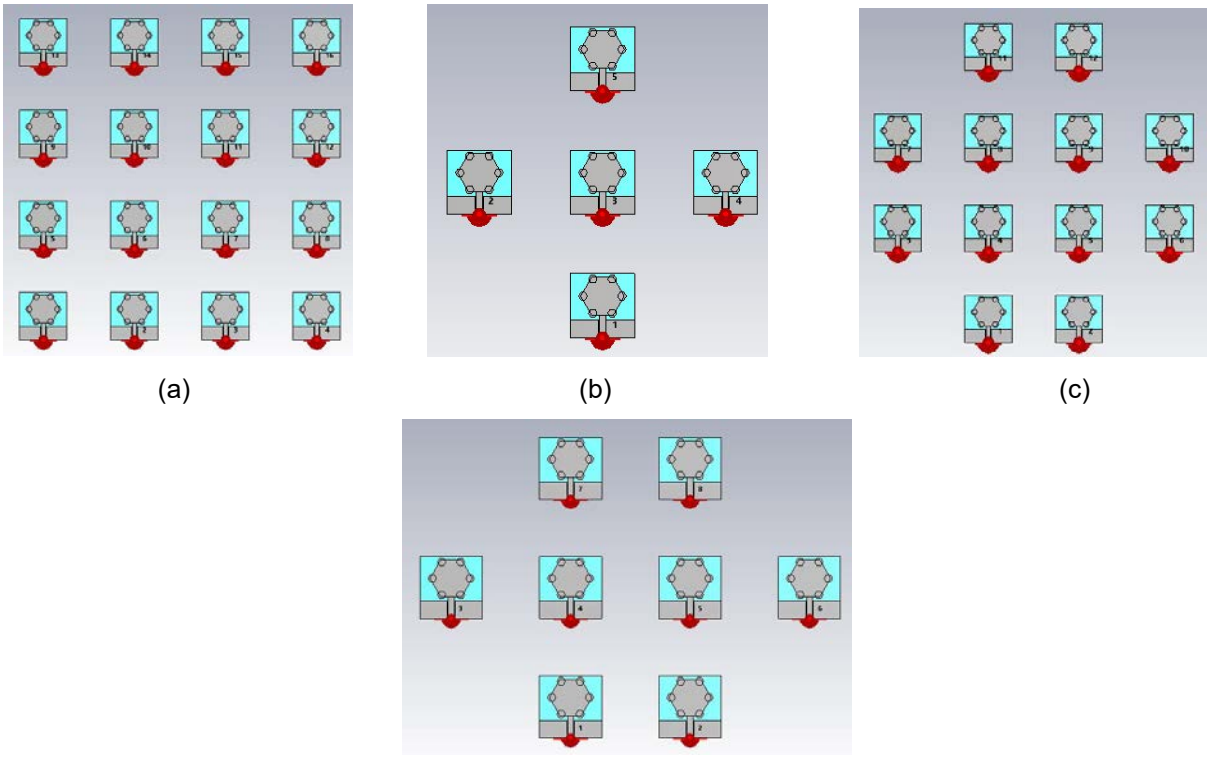
6.4.3 Progress Made Since Last Report

(F) Tradespace analysis of the fractal antenna array geometries has been carried out to analyze and compare the antenna metrics. In this process, a square shaped array geometry with 16 elements, a diamond shaped array geometry with 5 elements, an octagon shaped array geometry with 12 elements, and a hexagon shaped array geometry with 8 elements are designed and simulated using commercial electromagnetic (EM) software.

(G) ML models such as radial basis function (RBF) and least square regression (LSR) models have shown promising results in predicting S11 response for the fractal antenna. Therefore, we extended the application of ML models on fractal antenna to the prediction of gain as a function of frequency and electric field strength in the far field.

6.4.4 Technical Results

(F) Four different array geometries (i.e., a square shaped array geometry with 16 elements, a diamond shaped array geometry with 5 elements, an octagon shaped array geometry with 12 elements, and a hexagon shaped array geometry with 8 elements) are designed and simulated to understand and compare the effect of each geometry on the antenna metrics. Figure 6.4.1 illustrates the designed array geometries.



(a) (b) (c)

(d)

Figure 6.4.1: Fractal antenna array geometries: (a) square array geometry, (b) diamond array geometry, (c) hexagon array geometry, and (d) octagon array geometry.

Figure 6.4.2(a) shows the gain as a function of theta; the antenna array with octagonal geometry has lower sidelobe levels while maintaining equivalent gain at 0 degrees. The S11 response of the center element is shown in Figure 6.4.2(b); the antenna arrays with hexagonal geometry and octagonal geometry yielded maximum bandwidth. Table 6.4.1 summarizes physical aperture area, aperture efficiency, and gain at 900 MHz for all the above-mentioned antenna array geometries. The octagonal geometry has a higher bandwidth, higher gain with minimal sidelobe levels, and lower physical aperture area.

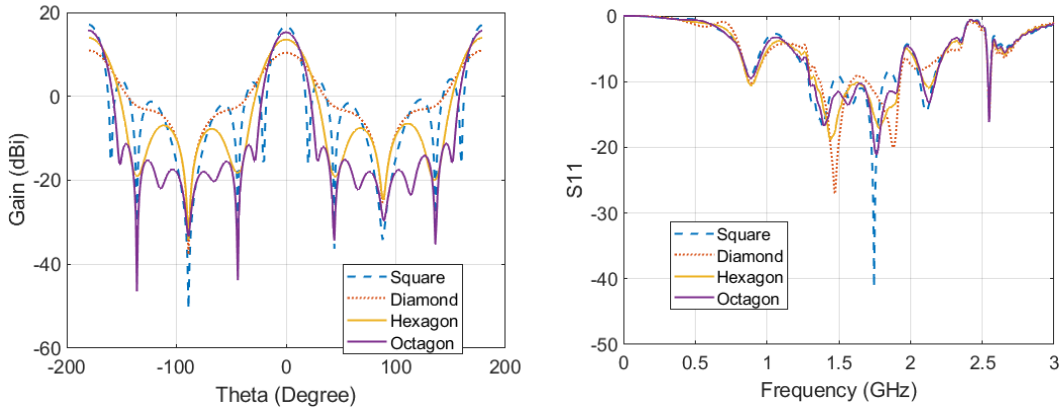


Figure 6.4.2: (a) Gain as a function of theta for different geometries at 900 MHz (b) S11 response of center element of array geometries.

Table 6.4.1. Array antenna metrics

Antenna array geometry	Physical aperture area (m^2)	Peak gain (dBi) (900 MHz)	Aperture efficiency (900 MHz)
Diamond	135.625	10.9337	80.8%
Hexagon	280.825	13.96155	78.4%
Octagon	483.625	15.71514	68.1%
Square	714.025	17.07985	63.2%

(G1) The inability of RBF and LSR to predict gain response with negative values is due to the failure of Altair Hyperstudy to retrieve negative gain values from the *.out file. This issue has been resolved by specifying the setup to retrieve values with additional decimal points as shown in Figure 6.4.3.

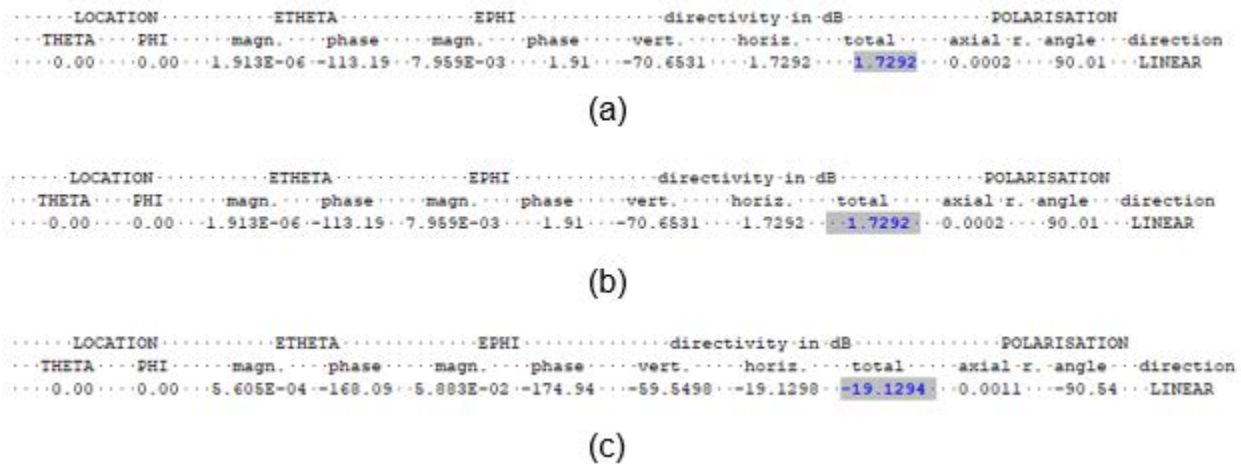


Figure 6.4.3: Snapshot from *.out file (a) previous setup (b) present (resolved) setup (c) successful retrieval of negative values.

With this new setup, RBF and LSR are trained with *a* and *b* values in the input of training data while the output of training data has values of gain for the respective *a* and *b* values. The training data is generated for 30 discrete frequency points over a range of 100 MHz to 3 GHz with a step size of 100 MHz. This step is taken in order to eliminate interpolated data in training. From Figure 6.4.4, it is evident that steps taken to resolve the issue were successful.

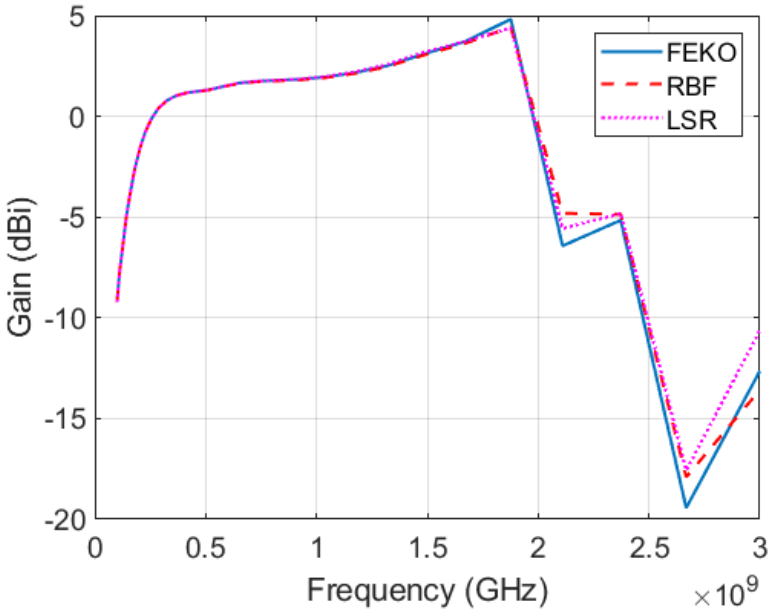


Figure 6.4.4: Gain (dBi) comparison of FEKO with radial basis function (RBF), least square regression (LSR).

(G2) The ML models, RBF and LSR, are employed to predict the electric field strength radiated by the fractal antenna in the far field region. On using discrete frequency points for generating training data was proved to be helpful for accurate prediction. So, in the process of generating training data, the hexagonal patch radius *a* and fractal side length *b* values are used in the training input, and the corresponding electric field strength at 30 discrete frequency points over a range of 100 MHz to 3 GHz with a step size of 100 MHz is used in the output of the training data. Figure 6.4.5 illustrates the electric field strength of a fractal antenna at 3 far field points (i.e., 100, 200, and 300 mm) predicted by the ML models and calculated using, FEKO. Generalization capability of LSR at lower and higher frequencies can be improved by increasing the training data size (current training data size = 10). The prediction of ML model (RBF) has very close agreement to that of FEKO response.

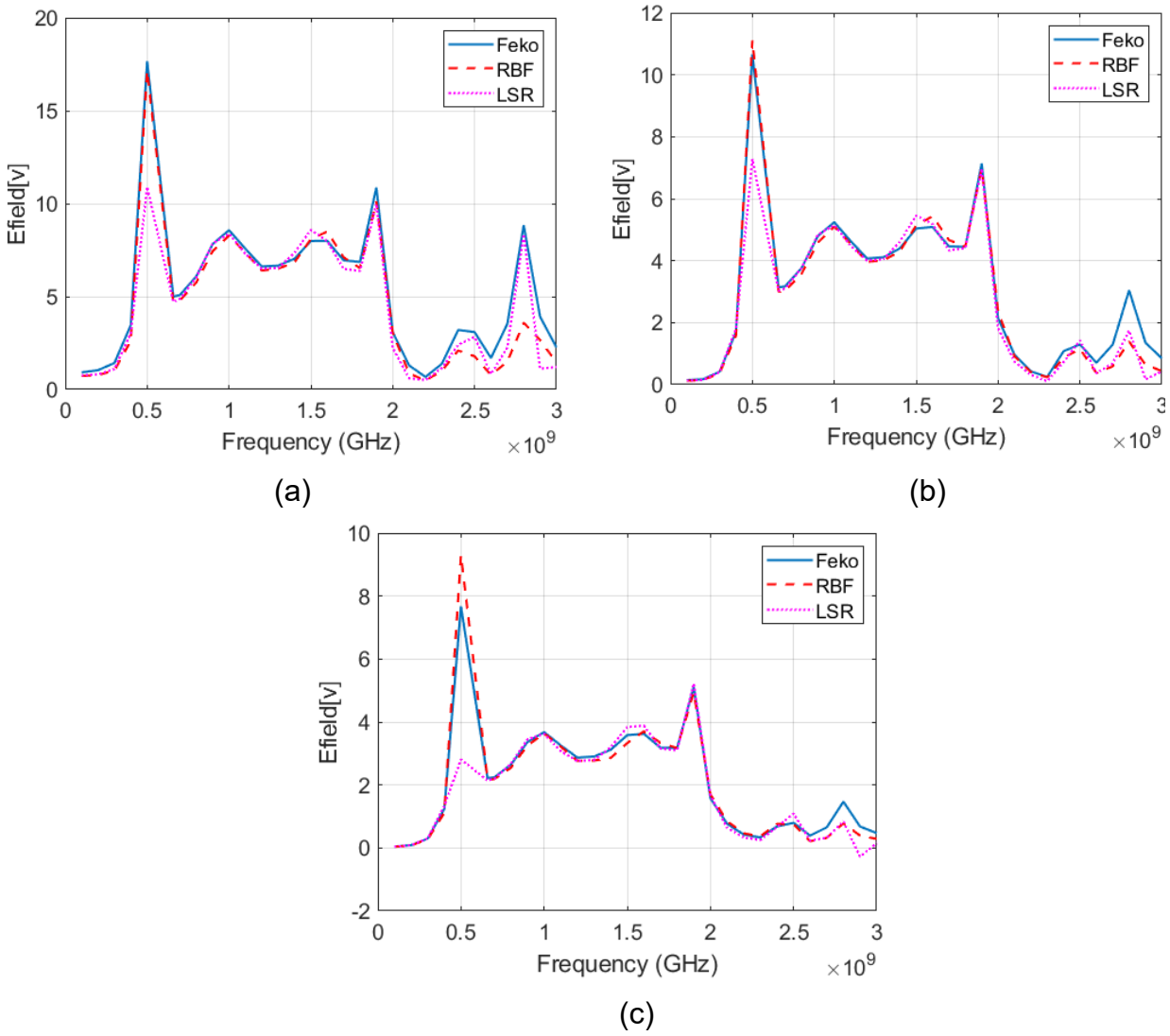


Figure 6.4.5: The electric field strength in a far field region at a distance (a) 100 mm, (b) 200 mm, and (c) 300 mm from a fractal antenna.

6.4.5 Summary of Significant Findings and Mission Impact

(A) The initial analysis of the simulation results with fractal radius *b* equal to 1.8 mm yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO has been used as an optimization tool with fractal radius *b* as the optimization variable. The optimum value for *b* is found to be 1.66 mm. A comparison between reflection coefficient for initial *b* (= 1.8 mm) value and the optimized *b* (= 1.66 mm) can be found in Figure. 6.4.6. The optimization is carried out over 51 discrete frequency points.

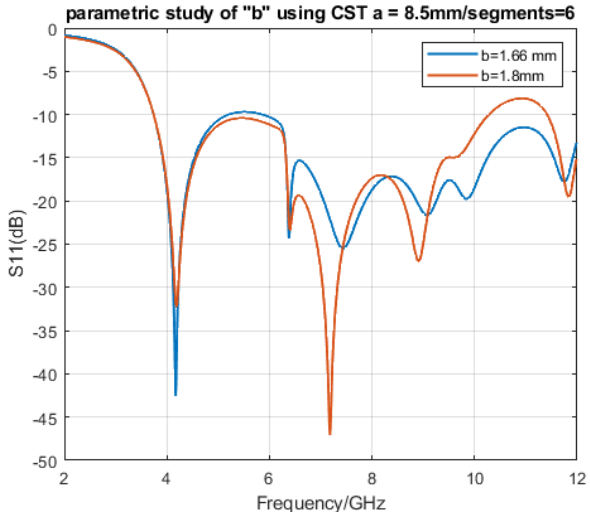


Figure 6.4.6 Reflection coefficient of fractal antenna for initial and optimized *b* value.

(B) The addition of fractal elements (*N*) to the simple hexagon improved antenna metrics such as S11. To further investigate and understand the fractal elements, the number of segments in the fractal geometry has been varied. The improvement in bandwidth is observed as the value of *N* is increased from 6 to 14.

(C) The initial optimum value of *b* over 51 discrete frequency points is reported as 1.66 mm in task (A). To further increase the accuracy of the optimization algorithm and to find a more precise value for *b*, optimization is further performed over wider frequency points (201 discrete points between 2 GHz to 12 GHz) which yielded the optimum value of b as 1.368 mm. The S11 response of antenna design with newly found *b* (i.e., 1.368 mm) hasn't produced any better bandwidth with respect to *b* (= 1.66 mm). Thus, *b* is set to be 1.66 mm for further research.

(D) The hexagonal patch radius *a* has a significant effect on the physical aperture area of the antenna. Therefore, Altair OPTFEKO has been utilized to find an optimum *a* value, which was found to be 8 mm over the range 7.2 to 9 mm. Antenna metrics such as S11, gain, and bandwidth have shown desired performance with the optimized *a* value.

(E) The initial antenna design has been modified to achieve a center frequency of ~1.3 GHz. The gain value at 900 MHz is 3.5 dBi and, with the modified antenna design, we were able to achieve an impedance bandwidth ratio of 3.3:1. The designed antenna has been fabricated and tested, and the S11 response of the fabricated antenna agrees well when compared against FEKO, CST.

(F) To summarize, four different fractal antenna array geometries (i.e., square, diamond, hexagon, and octagon) have been designed and simulated. The antenna array with square geometry has the largest physical aperture area (714.025 m^2) and the highest gain at 900 MHz (17.07 dBi). However, from the gain as a function of theta plot, square array geometry has very high sidelobe levels. Antenna array geometry with octagonal shape minimal sidelobe levels with gain (15.715 dBi) at 900 MHz close to that of square geometry with 32.27% lower physical aperture area than that of square geometry.

(G) The initial prediction of reflection coefficient (S11) from the three ML models was satisfactory and has shown a good agreement against the FEKO response. In addition, radial basis function (RBF) and least square regression (LSR) were down selected from the initial three ML models basing upon the generalization capability. Further analysis of increasing training data set size has shown no improvement in prediction accuracy. As a result, the training data set is fixed to 10 for further studies. Moving forward, the above-mentioned ML models are trained and tested to predict the gain as a function of frequency, the electric field strength in the far field. Thus, ML models (RBF, LSR) trained to predict S11, gain, electric field have shown very accurate agreement with FEKO response.

6.4.6 References

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

7.0 RF Coupling

7.1 Enclosure Effects on RF Coupling

(Mohamed Hamdalla and Ahmed Hassan)

7.1.1 Problem Statement, Approach, and Context

Primary Problem: UAVs are typically considered metallic/dielectric enclosures depending on their frame material. The shielding effectiveness of such enclosures might be compromised due to the slots and gaps on these enclosures, creating upset susceptibility to the enclosed electronics. The goal of this work is to quantify how the thresholds for upset susceptibility of enclosed wires and integrated circuits differ from those in free space.

Solution Space: Study enclosures with different shapes, material compositions, and slots to quantify their effect on RF coupling to the enclosed wires and electronics typically used in UAVs. The study will focus on the low-frequency range where the incident wavelength is comparable to the size of the enclosure or larger.

Sub-Problem: UAVs are manufactured with a wide variety of shapes and composites to accomplish an exponentially expanding list of missions. The configurations previously reported in the literature have simplistic assumptions regarding the shape and material composition of UAV enclosures that might overestimate or underestimate susceptibility.

State-of-the-Art (SOTA): Simple statistical analysis of specific enclosure configurations using either brute force simulations/measurements or pure statistical methods. Also, simplified UAV wire distributions are assumed.

Deficiency in the SOTA: Brute force simulations/measurements of the voltages and currents induced in wires and integrated circuits contained in enclosures are computationally or experimentally complex and have several limitations. The computations are complicated by the multiscale nature of the simulations, and the experiments are complicated by the cost of the equipment and the extensive time needed to measure every variation to cover all possible scenarios. Statistical methods, such as the Random Coupling Model (RCM) for example [1], are only accurate for high frequencies where the wavelength is much smaller than the size of the enclosure. Another main deficiency of the RCM is that it can't predict the exact induced voltages and currents for a specific well-characterized system but it only provides the statistical properties of these induced currents and voltages.

Solution Proposed: Apply Characteristic Mode Analysis (CMA) to identify the fundamental modes of the enclosure, current distribution, and the field pattern of each mode. This will allow us to predict the worst-case RF coupling scenarios without the need for lengthy simulations and/or expensive experimental measurements. The proposed approach can predict measurements at a fraction of the cost/time. Moreover, we propose to study RF coupling to realistic UAV wire distributions, experimentally reconstructed, when they are placed inside metallic/dielectric UAV enclosures.

Relevance to OSPRES Grant Objective: Provide general guidelines on how the environment, in this case, the enclosure, affects RF coupling and subsequent electromagnetic absorption to UAV wires and integrated circuits.

Risks, Payoffs, and Challenges: The modes depend mainly on the shape and material of the enclosure. Since UAVs have a wide variety of shapes and material compositions, a library of several UAVs needs to be studied before general quantitative conclusions can be drawn. Challenges can be mitigated by the use of the classification techniques of Machine Learning (ML). That is, different ML techniques will be evoked to detect hidden patterns on how the shape, material composition, and the shape/size location of slots correlate with the field enhancement inside the enclosure.

7.1.2 Tasks and Milestones / Timeline / Status

A. Complete the CMA implementation for studying the shielding effectiveness of metallic enclosures. Validate whether CMA can predict the worst-case shielding effectiveness of metallic enclosures as a function of their shapes. / JAN21 / Complete.

   A1. Prepare a manuscript for IEEE AWPL to document the progress done in A. / Ongoing.

B. Use CMA tool in (A) to predict the worst-case internal field magnitude of metallic and dielectric enclosures of ten COTS UAVs as a function of HPM waveform. / MAY21 / Ongoing.

C. Use the database in (B) to train a Machine Learning (ML) platform to predict RF coupling to enclosed wires and electronics. / OCT21 / Ongoing.

D. Progressively build an accurate representation of the UAV wiring system with all of the integrated circuit (ICs) and electronics to test assist the predictions of (c) and the experimental measurement of the actual UAV. / JUL21 / Ongoing.

E. Address the 2021 UAV's semi-annual review recommendations to study arbitrarily shaped UAV wire distribution. / JUNE21 / Complete.

7.1.3 Progress Made Since Last Report

D1. An accurate representation of the UAV wiring system.

D1.1. In a previous MSR We have created a full-wave model of a complete UAV with all the wires and all the IC components to use as a numerical platform for studying effects and validating predictions. Figure. 7.1.1b shows the wiring diagram of the actual UAV with the different IC components. We have built an accurate replica of the UAV in Fig. 7.1.1a using the full-wave electromagnetic solver FEKO which is shown in Fig. 7.1.1c. The wires' length and diameters match the values in the actual UAV in Fig. 7.1.1a and match the values in Table 7.1. The FEKO model had all the components modeled as a linear 50 Ω load, as a first approximation of the model.

As an effective tool to test different linear/nonlinear loads as the load of interest instead of the 50 Ω, we propose to use the Equivalent circuit approach (ECA). The approach had been discussed in detail in contract reports for N00014-18-C-1017. Briefly, the ECA involves performing two full-wave simulations to calculate the Voc and Zin of the

wiring/trace system at the port of interest. After that, much faster circuit simulations can be used to simulate RF coupling to hundreds of possible nonlinear loads that can be connected to the wiring system. These simulations will be much faster when performed using a circuits solver such as LTSPICE than if they were performed using a full-wave electromagnetic solver. Also, this will allow us to simulate, in a feasible computational time, practical electronics with tens of components.

The input impedance Zin can be represented by a series of RLC circuits where one RLC circuit is needed for each resonance in the frequency band of interest. During this month we have studied two different RLC circuit representations to study the most accurate representation of Zin. The two representations are (1) Parallel RLC [1], (2) Second series equivalent circuits for a complex pole pair [2]. The two RLC circuits are shown in Fig. 7.2. Each RLC branch in Fig. 7.2 represents a resonance frequency of Yin. Thus, to represent Yin over the frequency range of interest, N – RLC circuits need to be stacked in parallel where N is the number of resonances of Yin.

7.1.4 Technical Results

Figure 7.3 illustrates the comparison between Yin, at the port of interest, calculated using the Full-wave solver FEKO and Yin calculated using the two different equivalent RLC circuits. In Fig. 7.3b 8 Second series equivalent circuits, similar to the circuit in Fig. 7.2b, are connected in parallel where each circuit represents a resonance of Yin. While in In Fig. 7.3c,16 Second series equivalent circuits similar to the circuit in Fig. 7.2b, are connected in parallel where each pair of circuits represent a resonance of Yin. Clearly, the Second series equivalent circuit is a much better representation to be used in our future analysis to represent Yin of the system. This will ensure better accuracy in calculating the voltage across the linear/nonlinear loads at the port of interest.

In the next report, the circuit representation will be used to calculate the voltage across different loads using LtSpice.

Table 7.1. Quadcopter's main circuitry components and wires.

Part function	***Part #***	***Specs.***	***Length***
motor feed lines	1	18 AWG	
ESC out power lines	2	16 AWG	
ESC in power lines	3	16 AWG	~20 cm
esc in signal	4	22 AWG	25 cm
battery out	5	14 AWG	
battery to controller	6	22 AWG	
main controller (autopilot)	7		carrier board 9.5 cm x 4.5 cm
GP.1575.25.4.A.02 GPS/Galileo 25*25*4mm 1575.42MHz Patch Antenna2	8	22 AWG	~20 cm
Readytosky® 2212 920KV Brushless Motors	9		
SimonK 30A ESC Brushless Speed Controller	10		
Pixhawk Power Module 5.3V BEC XT60	11		

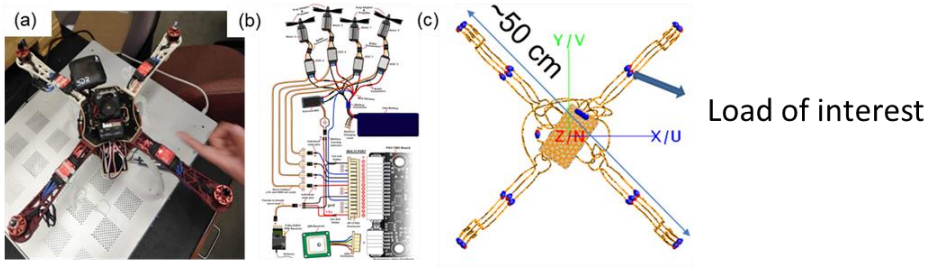


Fig. 7.1. (a) Model of the realistic UAV circuitry showing the wires, components, and frame, (b) the UAV wiring diagram showing all the wires and components, (c) the FEKO model of the UAV in (a) and (b).

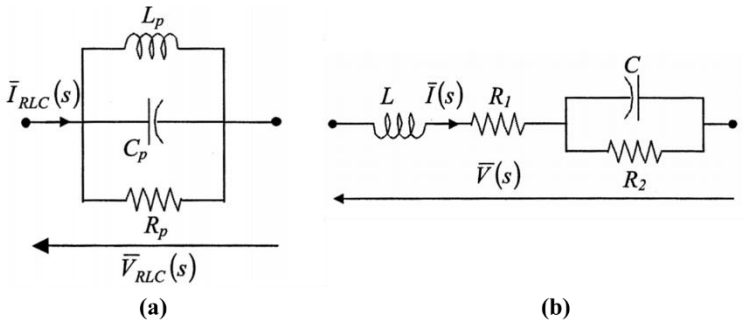


Fig. 7.2. RLC circuit for each resonance frequency of Yin at a load of interest (a) Parallel RLC circuit (b) Second series equivalent circuit [2].

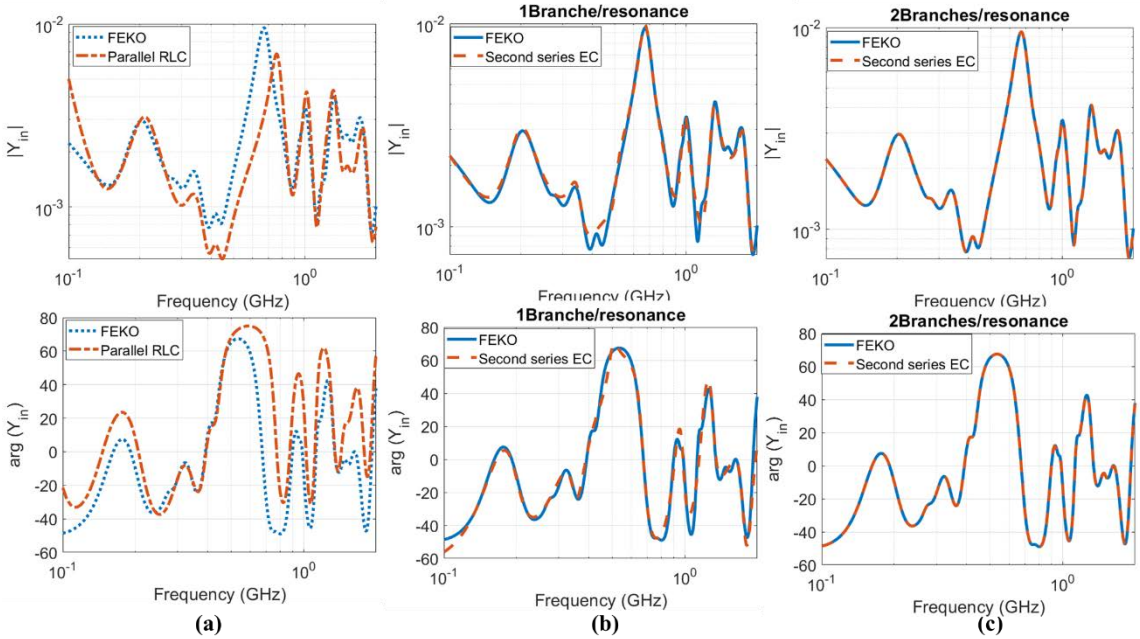


Fig. 7.2. Comparison between the magnitude and phase of Yin calculated using (a) FEKO and circuit representation using parallel RLC circuit/resonance (b) FEKO and circuit representation using Second series equivalent circuit/resonance (c) FEKO and circuit representation using two Second series equivalent circuit/resonance.

7.1.5 Summary of Significant Findings and Mission Impact

A1. A fast full-wave tool that facilitates studying the effect of a metallic enclosure on shielding effectiveness has been developed using CMA.

D1. Two Second series equivalent circuit branches/resonance is the best combination for the RLC circuit to accurately represent Zin of the system.

Reference:

[1] R. Michels, M. Willenbockel and F. Gronwald, "A Parametric Study of an Energy Storage Effect due to Nonlinear Components and HPEM-Excitation," 2019 International Symposium on Electromagnetic Compatibility - EMC EUROPE, Barcelona, Spain, 2019, pp. 59-64.
[2] G. Antonini, "SPICE equivalent circuits of frequency-domain responses," in IEEE Transactions on Electromagnetic Compatibility, vol. 45, no. 3, pp. 502-512, Aug. 2003, doi: 10.1109/TEMC.2003.815528.

8.0 Laser Development

8.1 Fiber Lasers and Optical Amplifiers

(Heather Thompson and Scott Shepard)

8.1.1 Problem Statement, Approach, and Context

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$50K to \$5M.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution. This way of implementing an optical fiber laser (via an optical fiber amplifier) has SWaP advantages with respect to traditional (fiber and free-space) laser designs.

Sub-Problem (1): Optical pump power system costs are the dominant source of costs (in both normal/free-space lasers and in optical fiber lasers, of this class).

Sub-Problem (2): Amplified spontaneous emission (ASE) and fiber nonlinearities impede the optical amplifier performance.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive until reduced by a factor of two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping scheme which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments we are pursuing the use of gain saturation and a staged design of different fiber diameters.

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system needed to drive the PCSS will meet the modular and scalable volume and cost aim-points.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability.

8.1.2 Tasks and Milestones / Timeline / Status

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Ongoing.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Ongoing.

(E) Demonstrate a cost-reduced fiber laser. / Ongoing.

(E1) **March 2021** Finalize design. / Complete.
(E2) **April 2021** Assemble and test-check seed LD (laser diode)/driver. / Complete.
(E3) **April 2021** Measure power vs current transfer function of seed LD/driver. / Complete.
(E4) **May–July 2021** Measure ASE and jitter of 1064 nm seed LD/driver. / Ongoing.
(E5) **May–July 2021** Measure ASE and jitter of 1030 nm seed LD/driver. / Ongoing.
(E6) **June–July 2021** Assemble and test-check pump LDs/drivers. / Ongoing.
(E7) **June–July 2021** Measure power vs current transfer function of pump LDs/drivers. / Ongoing.
/ (E8) – (E14) Delayed due to vendor issues (see MAY MSR).
(E8) **September 2021** Splice power combiners to Yb doped preamp fiber.
(E9) **September 2021** Connect seed and pumps to power combiners and test-check.
(E10) **September–October 2021** Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle.
(E11) **September–October 2021** Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle.
(E12) **November 2021** Splice power amplifier and its power combiner to best preamp.
(E13) **November–December 2021** Measure gain, ASE and jitter of entire amp assembly.
(E14) **December 2021** Analyze data and document.

(F) Design a new type of higher power, tubular core, fiber amplifier. / Ongoing.

8.1.3 Progress Made Since Last Report

(F) We quantified the coupling of the tubular glass mode to that of the hollow-core air mode and demonstrated how self-focusing can be used to move roughly half of the power out of glass and into the hollow-core of the tube (with less than 10% being lost into the air outside the tube). This effect means we can roughly double the operating power of our tubular optical amplifiers.

8.1.4 Technical Results

(F) The coupling of the mode in the glass tube (referred to as a “cladding” due to its location) to that of the mode in hollow-core air (referred to as a “core” due to its location) is quantified in Figure 8.1.1(a). Note that the power which remains in the cladding/glass (where it’s launched) is reduced when gamma is not equal to zero. Gamma is the nonlinear refractive index and its presence (at the number in the figure appropriate for glass at a 1064 nm wavelength) acts to throw energy out of the glass waveguide. Fortunately, most of the dispelled energy gets trapped in the core (rather than radiating out of the sides of the tube. This is shown in Figure 8.1.1(b) where we note that the power

coupled from cladding/glass (where it's launched) into the core/air goes up dramatically when gamma is not equal to zero.

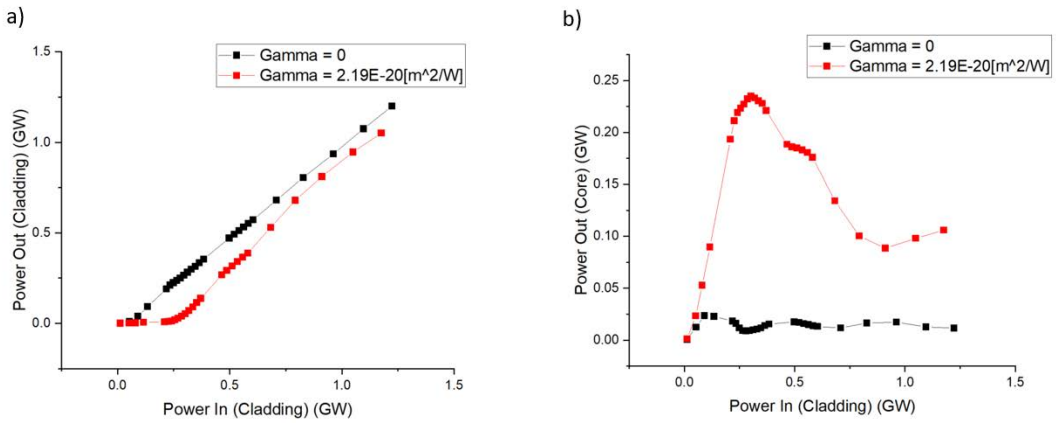


Figure 8.1.1. Self-focusing **(a)** reduces the power transferred in the glass/cladding and **(b)** increases the power coupled into the air/core.

For example, when $P_{in\ cladding}$ = 0.497 [GW] and gamma = 0 (so self-focusing is "off") most of that power comes out the end of that waveguide as $P_{out\ cladding}$ = 0.47 [GW] but when gamma is "on," that power drops by almost half to $P_{out\ cladding}$ = 0.267 [GW]. Moreover, for that same input power we find that the power coming out of the core jumps from a "leakage" amount of 0.017 [GW] (at gamma = 0) to a $P_{out\ core}$ = 0.189 [GW] when gamma is not zero. The cladding power dropped by 0.203 [GW] while the core power increased by 0.172 [GW] so only 6% of the input energy was lost into the air around the tube. Thus, the self-focusing helps to couple energy into the confined mode in air without incurring substantial loss into the surrounding air.

A graphical representation of this effect is demonstrated in the electric field magnitude plots of the end-view of the waveguide in figure 8.1.2. Therein we see that self-focusing has altered the uniform excitation of the glass tube at the input (a) into a distribution which includes the hollow air core of the tubular waveguide. Both the existence of an air mode and our ability to couple energy into it are fortuitous results. Further study is certainly merited due to the significant impacts already demonstrated in this factor of two (on top of two orders of magnitude over the SOTA) for power transfer and optical amplification.

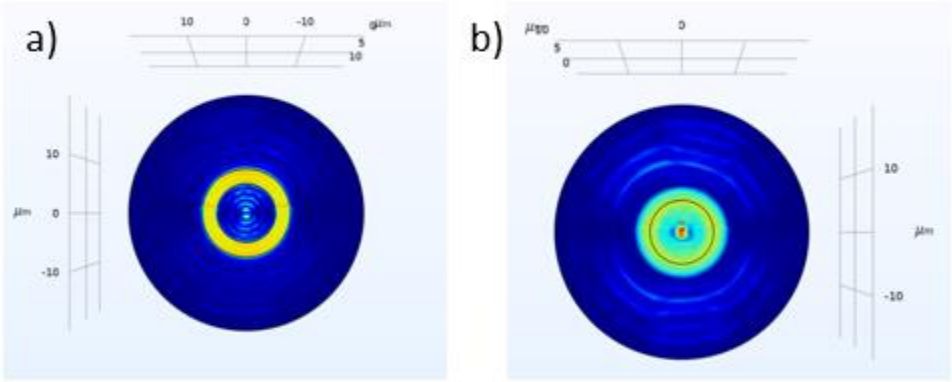


Figure 8.1.2: Tubular waveguide electric field magnitudes at the **(a)** input plane and the **(b)** output plane, revealing the growth of the hollow-core mode.

8.1.5 Summary of Significant Findings and Mission Impact

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with tolerable pre-burst ASE. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) The design of a proof-of-concept experiment demonstrating a cost-reduced optical pumping scheme was finalized MAR2021.

(F) We made (to our knowledge) the first observation of self-focusing effects that are not determined by beam power alone. We found instead that these can also be controlled via the geometric factors within a waveguide (such as fiber core diameter) MAY2021.

(F) We made (to our knowledge) the first observation that a mode exists in the air within a simple glass tube into which we can couple energy from the mode in the glass. Thus, an amplifier (in the doped and pumped glass) can operate at higher powers JUNE2021.

8.2 WBG-PCSS Enabled Laser Diode Array Driver

(John Bhamidipati)

8.2.1 Problem Statement, Approach, and Context

Primary Problem: Need for heavy (~125 lbs.), bulky (~10 cu-ft), and expensive (~$120,000) conventional laser systems (1064 nm) in PCSS-based HPM applications, with an additional need for second and third harmonic generation (SHG/THG) optics to trigger wide bandgap (WBG) solids (GaN/SiC).

Solution Space: Design and implement a compact (~1.1 cu-ft), lightweight (10–15 lbs.), and inexpensive (<$15,000) alternative for conventional high average power optical trigger (laser) system to improve SWaP-C^2 index of HPM systems.

Sub-Problem: Unavailability of commercial-off-the-shelf (COTS) miniature optical sources with sub-nanosecond pulse widths and tens-of-μm beam width, delivering >1-Watt power to implement as a makeshift/turnkey solution for the laser system.

State-of-the-Art (SOTA): High average power picosecond pulsed lasers available up to 50 W output power with a gain factor up to 40 dB (~10,000x power) with laser amplifier.

Deficiency in the SOTA: High average power 1064-nm pulsed lasers are bulky and require auxiliary systems as well as additional optics for SHG/THG generation for WBG device triggering.

Solution Proposed: Multi-stage laser diode array/stack (LDA/LDS) driver powered by seed-laser-diode-driven avalanche WBG-PCSS as a compact, inexpensive laser replacement.

Relevance to OSPRES Grant Objective: Provides an enhanced SWaP-C^2 compliant solution for the laser (optical trigger) subsystem, with a subsequent impact on overall HPM system cost, volume, and power (optical and electrical) requirements.

Risks, Payoffs, and Challenges: Complex interconnect and thermal management system (TMS) design at high temperature (130–175°C) operation; unavailability of COTS high power pulsed laser diodes could potentially raise a need for research in laser diodes (arrays).

8.2.2 Tasks and Milestones / Timeline / Status

(A) Complete initial feasibility study for the cascaded multi-stage optical amplifier design and determine functional requirements for the laser diodes (arrays) and source driver [DEC–JAN 2020 / completed].

(B) Complete initial stage experimental implementation of the PCSS-based driver and demonstrate positive current gain using GaN-PCSS, triggered with a 404 nm laser diode. [JUL–AUG 2021 / in progress].

(C) In addition to (B), investigate potential alternatives to GaN-PCSS in both PCSS and non-PCSS domains. [JUL–AUG 2021 / in progress].

(D) Define performance metrics for PCSS-based driver and complete numerical calculations for required output current at each stage and corresponding PCSS (GaN/GaAs) operating voltages in light of electric fields required for lock-on/avalanche mode, establish real-time implementation timeline, cost estimates, jitter limitation, and explore ways to protect LDA from PCSS ringing. [MAR 2021 / partially complete / revisit after completing (B)].

(E) Demonstrate a tunable 1.7kV SiC-MOSFET-powered frozen wave generator (FWG) prototype on a custom-built PCB with Cree/Wolfspeed MOSFET(s), 16-segments of 50 Ω coaxial cables and/or microstrip transmission lines capable of generating chirped pulse widths. [JUL–AUG 2021]

(F) Proof of concept testing of the two-stage PCSS-enabled driver system with a 50 Ω load at 1 kHz pulse repetition rate (PRR) [SEP–OCT 2021]

(G) Working prototype demonstration at ~MHz PRR with laser diode array/stack and ancillary optics based on HPM source driver needs including thermal management system (TMS). [NOV–DEC 2021]

8.2.3 Progress Made Since Last Report

(C) Photo-illuminated pulse testing has been completed for the commercial off-the-shelf silicon optodiodes procured from Voltage Multipliers Inc. Testing was performed at 200-V charge voltage on a 4.4-Ω microstrip with laser pulse energies ranging between 20-μJ and 200-μJ, and results were evaluated against the required performance metrics determined in (A) in order to be considered as a potential alternative to GaN-PCSS. The optodiode performance failed to meet the expected rise-time (t_{rise}) (<200-ps) and on-state resistance (R_{on}) (~72-mΩ) metrics at low voltages (<200-V) and are no longer considered a viable alternative to GaN-PCSS.

(E) The second iteration of design, fabrication, and testing of the SiC-MOSFET-powered FWG has been completed. A pulse-width chirp capable FWG has been demonstrated with balanced and unbalanced load configurations. The reflection-induced ringing issues reported in the previous report have been mitigated in the balanced load configuration, but still need to be addressed for unbalanced loads. To further optimize the FWG, a discrete element-based transmission media that uses tunable inductors and capacitors will be implemented in the next iteration.

8.2.4 Technical Results

(C) In an effort to evaluate switching technologies as potential alternatives for GaN-PCSS, commercial off-the-shelf Si optodiodes rated for 15-kV procured from Voltage Multipliers Inc. (SKU: OZ150SG) have been tested on a 4.4-Ω microstrip to verify the device ability to demonstrate <200-ps t_{rise} and <75-mΩ R_{on} while pushing >100-A current when excited with a 70-ps FWHM laser pulse at <50-μJ illumination. The device under test had a <0.5-mm epoxy encapsulation. Optical absorption parameters for the epoxy were not reported by the manufacturer and were ignored. The results from the test are reported below:

Pulse energy (µJ)	Charge/bias voltage (V)	Output voltage (V)	Rise time (ps)	Fall time (ns)	On-state resistance (Ω)
200	200	96	428	4.845	0.143
103	200	66	368.56	4.652	2.266
47	200	55	360.65	4.3	3.6
21	200	42	329.46	3.9	6.076

Table 8.2.1. Results from Si optodiode pulse testing performed at 200-V charge voltage with a 70-ps FWHM optical pulse illumination and varied optical pulse energies.

An optical energy sweep test was performed, keeping the charge voltage and laser spaciotemporal profile the same. The best result in terms of on-state resistance (0.143-Ω) was observed at 200-µJ illumination while t_{rise} (329.4-ps) was observed when illuminated with 21-µJ optical energy. Nonetheless, the obtained results failed to satisfy the metrics (R_{on} = 0.072-Ω and t_{rise} < 200-ps) determined by the feasibility study. Hence, the VMI optodiodes are considered infeasible for implementation as an alternative to GaN-PCSS. Avalanche transistors and silicon avalanche shapers will be evaluated in the next reporting cycle.

(E) The second iteration of a SiC-MOSFET powered pulse-width chirp-capable FWG has been fabricated and tested. The design implements a 1.7-kV Cree/Wolfspeed SiC-MOSFET (C2M1000170D) rated for 10.5-ns rise-time driven using a Texas Instruments UCC5390 driver. 2-,4- and 8-segment transmission line versions of the FWG, each with balanced and unbalanced load configurations, have been tested. For the transmission line segments, 4 pairs of coaxial cables with 0.66 velocity factor were used, each pair with lengths 5-, 4-, 3- and 1-meters inducing propagation delays of 25-ns, 20.23-ns, 15.17-ns, and 5.05-ns, respectively. The testing was performed at 150 V charge voltage and 100 kHz repetition rates with 30% gate trigger duty cycle.

The highest power transfer with no pulse deformation has been noticed in the 2-segment (2 x 5 m coax cables) configuration. However, with an increase in number of transmission line segments, an increase in reflections, pulse overlap, and pulse deformation due to deconstructive interference was noticed. Also, the expected chirp was not distinguishable in the 8-segment configuration. It is assumed that using the same transmission line configuration for balanced and unbalanced load configurations could be a potential reason for the noticed issues as the signal path changes (due to reflections) in the unbalanced load configuration when compared with balanced load, which could potentially lead to deconstructive interference along the propagation path. Testing for unbalanced load configuration will be repeated with a different transmission line configuration to overcome the aforementioned issues. Also, in the next iteration, a waveform-tunable FWG will be implemented using a discrete-element-based transmission medium that uses tunable inductors and capacitors.

8.2.5 Summary of Significant Findings and Mission Impact

(A) The state-of-the-art COTS laser driver specifications and limitations have been comprehensively studied, and target performance metrics have been determined in terms of output current (>120-A), pulse repetition rate (>1-MHz), transient response (<200-ps risetime and <1-ns pulse width), and volume (<0.75 cu-ft). A preliminary feasibility study has signified the need for lock-on conduction mode with ~$10^{2.6}$ gain factor to drive at >1-MHz pulse repetition rate while limiting the amplification stages to 2. This reduces monetary costs to 10–12% of the conventional laser system, while achieving the expected goal of miniaturizing the optical subsystem by 90%.

(B) Pulse trigger requirements for the LDA/LDS have been identified based on Jenoptik's actively cooled quasi continuous wave vertical diode laser stacks to tailor the device parameters of the enabling switch accordingly.

(C) Silicon optodiodes have been evaluated against the identified performance metrics for the enabling switch. The testing was performed at 200 V charge voltage with laser illumination energies between 20-µJ and 200-µJ. The device performance at low optical energies (~20-µJ) did not satisfy the expected metrics in terms of R_{on} and t_{rise}. Alternative switch technologies like avalanche transistors and silicon avalanche shapers will be evaluated in the next report cycle.

(D) Numerical calculations have been completed to estimate the electric fields and corresponding voltage bias required to induce lock-on operation while exploring ways to minimize the potential risks of high jitter at ~MHz order PRR switching, power reflections due to impedance mismatch, and negative ringing currents during PCSS recovery. Expected on-state resistance and power dissipation for 50 µm and 100 µm devices in lock-on conduction mode have been calculated to estimate cooling system requirements while retaining the expected SWaP-C^2 factor.

(E) The second iteration of the MOSFET-enabled FWG prototype has been fabricated and tested with a goal to demonstrate a 1.7-kV MOSFET-switched compact tunable pulse generator capable of generating chirped pulse-widths. The primary operation of a FWG has been demonstrated at 150-V, using 2-, 4- and 8- transmission line segment topologies with balanced and unbalanced load configurations. The pulse overlap, ringing, and deconstructive interference issues will be addressed using a different transmission line configuration and the next design iteration will be implemented using discrete tunable component-based transmission media.

9.0 Thermal Management

9.1 Nanofluid Heat Transfer Fluid Development

(Jordan Berg, Roy Allen, and Sarvenaz Sobhansarbandi)

9.1.1 Problem Statement, Approach, and Context

Primary Problem: Dielectric fluids (non-conductive coolant) used in thermal management systems (TMSs), while suitable for high-voltage HPM-based technologies, possess inherent thermophysical fluid properties (low thermal conductivity, high viscosity) that inhibit their ability to achieve >1 GW/m^3 cooling densities.

Solution Space: Develop a nanofluid by entraining ceramic nanoparticles and dispersants within the dielectric base-fluid, pure silicon fluid (PSF), to increase the nanofluid's thermophysical properties and cooling density capabilities with a similar form-factor. Investigate the performance of the semiconductor through computational fluid dynamics (CFD) modeling of the system and experimentally implementing the developed nanoparticle-modified PSF-20cSt.

Sub-Problem: While the dynamic viscosity of the dielectric fluid used, PSF-20cSt, is 'low' relative to other silicone-based fluids, it is ~15 times more viscous than water, and therefore requires increased pumping power within the TMS. Compounding this issue is the necessity to increase the flowrate of the fluid to achieve an equivalent heat removal rate compared to that of a water-based coolant.

State-of-the-Art (SOTA): Nanofluids, with optimal ratios of fluid-to-nanoparticles, have been shown to increase the thermal conductivity of dielectric fluids by 87% in comparison to the generic dielectric fluid alone; resulting in either greater cooling density, decreased pumping power, or reduced mass flow rate requirements.

Deficiency in the SOTA: The addition of nanoparticles within a base-fluid results in a tradeoff between one or more thermophysical properties. For example, adding nanoparticles may increase thermal conductivity of the nanofluid but may result in increased viscosity; i.e., heat removal rate may increase, but the required pumping power along with it. To the best of our knowledge, no one has attempted to create a nanofluid mixture with a goal of keeping the viscosity low. Therefore, the optimal nanoparticle-to-fluid ratio and specific nanoparticle type for the HPM thermal management systems needs to be identified and optimized with an attempt to maintain the viscosity of the mixture as low as possible.

Solution Proposed: Develop a nanofluid with both desirable thermal properties and a relatively low viscosity that can serve as a viable heat transfer fluid (HTF) for TMSs in HPM topologies and other high power density applications. Utilize systematic numerical and experimental strategies to evaluate a large sample set of various nanoparticles (with surfactants and dispersants).

Relevance to OSPRES Grant Objective: Increase cooling densities for HPM systems without requiring TMS design permutations, while decreasing pumping power requirements, in-line with the SWaP-C^2 objective.

Risks, Payoffs, and Challenges:

Risk: The pressures incurred by using a silicone-based fluid in a high-flow regime are not insignificant; large pump-chiller systems may still be necessary.

Challenges: Creating low volume-fraction samples of nanoparticles and surfactants is near equipment precision limit. Maintaining accuracy is critical to properly study modified fluids.

Payoff: A modified nanofluid dielectric fluid can be used to increase cooling capacity of any high power density system. An optimized nanofluid has the potential to extract 20% up to several factors more than the base fluid.

9.1.2 Final Summary of Results

Dielectric fluids (non-conductive coolant) used in thermal management systems, while suitable for high-voltage HPM-based technologies, possess inherent thermophysical fluid properties (low thermal conductivity, high viscosity) that inhibit their ability to achieve >1 GW/m^3 cooling densities. To overcome the poor thermophysical properties of dielectrics, this project aims to develop a nanofluid by entraining ceramic nanoparticles and dispersants within the dielectric base-fluid, pure silicon fluid (PSF), to increase the nanofluid's thermophysical properties and cooling density capabilities with a similar form-factor. While the dynamic viscosity of the dielectric fluid used, PSF-20cSt, is 'low' relative to other silicone-based fluids, it is ~15 times more viscous than water, and therefore requires increased pumping power within the TMS. Compounding this issue is the necessity to increase the flowrate of the fluid to achieve an equivalent heat removal rate compared to that of a water-based coolant. The addition of nanoparticles within a base-fluid results in a tradeoff between one or more thermophysical properties. For example, adding nanoparticles may increase thermal conductivity of the nanofluid but may result in increased viscosity; i.e., heat removal rate may increase, but so will the required pumping power along with it. To the best of our knowledge, no one has attempted to create a nanofluid mixture with a goal of keeping the viscosity low. Therefore, the optimal nanoparticle-to-fluid ratio and specific nanoparticle type for the HPM thermal management systems needs to be identified and optimized with an attempt to maintain the viscosity of the mixture as low as possible. The goal is to develop a nanofluid with both desirable thermal properties and a relatively low viscosity that can serve as a viable heat transfer fluid (HTF) for TMSs in HPM topologies and other high-power density applications. Our methodology is to utilize systematic numerical and experimental strategies to evaluate a large sample set of various nanoparticles (with surfactants and dispersants).

Based on the literature, the creation of a dielectric nanofluid for use as a coolant in the HPM system could potentially improve cooling performance. The thermal dissipation requirements for HPM systems are not insignificant and could, therefore, benefit from performance enhancement from every aspect (geometric optimization, reduction of thermal resistances, coolant selection, material selection, etc.). A sample of the PSF-20cSt that was used in the experimental testing of the JI-TMS was tested with a differential scanning calorimeter (DSC). The specific heat of the fluid was found to significantly differ from that of the manufacturer's value. The vendor's reported value of

the PSF-20cSt specific heat capacity was 1.6 $\frac{J}{gC}$, while DSC measurements showed it to be closer to 1.4 $\frac{J}{gC}$. This difference hinders the average deviation of 5.89% between the computational fluid dynamics (CFD) modeling and experimental results. To meet the need for a high thermal performance coolant, nanoparticle-modified PSF-20cSt was determined to be a necessary and useful undertaking. Three different ceramic nanoparticles were chosen to be studied: alumina, silicon carbide, and iron (II,III) oxide. Ceramics were chosen to maintain HTF dielectric properties. 18 nanofluid samples were tested for heat capacity enhancement. Of the 18 samples tested, the sample that showed the greatest heat capacity decrease was chosen, as theoretically, the largest heat capacity decrease correlates with the largest thermal conductivity increase. The sample that achieved the greatest heat capacity drop was the 0.25 wt.% silicon carbide with surfactants, achieving a value of 1.254 $\frac{J}{gC}$ (Table 9.1.1).

Table 9.1.1. DSC heat capacity values of nanofluid samples

Sample #	Sample	C_p (J/gC)	Std Dev (%)
1	Silicon Carbide 0.25 wt %	1.254	0.04
2	Silicon Carbide 0.5 wt %	1.441	0.38
3	Silicon Carbide 0.75 wt %	1.442	0.39
4	Silicon Carbide 0.25 wt %*	1.538	2.33
5	Silicon Carbide 0.5 wt %*	1.570	1.14
6	Silicon Carbide 0.75 wt %*	1.451	0.10
7	Iron Oxide 0.25 wt %	1.464	0.26
8	Iron Oxide 0.5 wt %	1.549	0.50
9	Iron Oxide 0.75 wt %	1.59	0.86
10	Iron Oxide 0.25 wt %*	1.458	0.23
11	Iron Oxide 0.5 wt %*	1.462	0.13
12	Iron Oxide 0.75 wt %*	1.402	0.69
13	Aluminum Oxide 0.25 wt %	1.632	1.21
14	Aluminum Oxide 0.5 wt %	1.399	0.79
15	Aluminum Oxide 0.75 wt %	1.544	0.18
16	Aluminum Oxide 0.25 wt %*	1.376	0.25
17	Aluminum Oxide 0.5 wt %*	1.378	0.54
18	Aluminum Oxide 0.75 wt %*	1.430	1.17
19	PSF-20cSt	1.391	0.58

* No surfactant sample

In order to investigate the performance of the semiconductor by implementing the developed nanoparticle-modified PSF-20cSt, the same CFD modeling techniques as described in section 13.3.1 of Appendix B was performed, but with the utilization of the thermophysical properties of sample 1 (0.25 wt% SiC with surfactants). The new CFD simulations were performed for the 100 W and 200 W average power tests. Using the same setup, boundary, and initial condition described in the Appendix, but with the theoretical and experimental values of thermal conductivity of the HTF, simulations were run using the 1.639 M node mesh, as the mesh was shown to give accurate results when

compared to the experimental results. After a convergence of 10^{-5} was seen for every residual, the simulations were stopped.

Table 9.1.2. Comparison of heat transfer fluid performance on maximum semiconductor device temperature

Max Semiconductor Temperature					
Test	**PSF k CFD**	**Theoretical k CFD**	**Measured k CFD**	**Experimental**	**% Improvement**
100 W	54.7	54.36˚C	46.67˚C	57.5˚C	18.8
200 W	99.0	90.18˚C	83.49˚C	98.2˚C	14.9

The goal of this project is to maintain the temperature of the semiconductor under 80 °C during operation. As it can be seen in Table 9.1.2., the max semiconductor temperature values from CFD modeling were shown for both cases of implementing thermal conductivity (k value) of the sample similar to the reported value in the literature (0.147 W/mK), and the measured value by the thermal conductivity device (0.197 W/mK), which are shown as theoretical k CFD and measured k CFD, respectively. The results from Table 9.1.2. show that in every case, the 100 W average power dissipated by the PCSS was kept well below 80 °C. For the 200 W average power case, the 80 °C threshold was always exceeded. However, with the utilization of nanofluids as a coolant, the maximum PCSS temperature decreased significantly. The measured thermal conductivity CFD model shows a 18.8% and 14.9% decrease in maximum PCSS temperature seen by the device. The results show that a significant heat transfer performance for the thermal management system is achievable using a small mass fraction of nanoparticles in the heat transfer fluid. For this reason, a heat transfer nanofluid will likely be implemented in future thermal management systems for the PCSS and similar high-power density electronics. With the promising results, the nanofluid implementation will be further analyzed along with the next generation thermal management system.

9.2 Ultra-Compact Integrated Cooling System Development

(Justin Clark, Roy Allen, and Sarvenaz Sobhansarbandi)

9.2.1 Problem Statement, Approach, and Context

Primary Problem: A cooling unit is desired to thermally manage semiconductor-based pulsed-power devices. The semiconductor device must maintain a temperature below 80 °C to prevent malfunctioning. The ambitious end goal is to create an ultra-compact cooling unit with the ability to remove 1 kW/cm^2 of heat in a short time frame. To achieve such high heat flux, a turbulent flow profile must be achieved. The objective will be reached as the micron scaled cooling unit is to be integrated onto a semiconductor device, allowing more heat extraction to occur.

Solution Space: In recent literature, over 1 kW/cm^2 has been achieved with minimal pumping power. The pumping power will be kept to a minimum since the unit to be

prototyped will represent 1 cm^2 surface area. This enables less power to be consumed to create a turbulent flow. An array of micro-sized jet nozzles will provide a turbulent flow onto a microchannel section directly on the semiconductor device. The ultra-compact design will reach turbulency at a faster rate while requiring less energy consumption.

Sub-Problem: The array of nozzles creates an extreme pressure loss. With a large amount of jet nozzles (over 200) and a flow diameter of nearly 100 microns, the pressure across the system will decrease tremendously. The pressure must be sustained to enable proper cooling and circulation processes. Another way to sustain pressure is to use different liquids. Different types of coolant will be simulated to determine effects from fluid density and viscosity. Preliminary studies show that pressure loss can be maintained using DI water or a type of gas while still requiring a small amount of pumping power.

State-of-the-Art (SOTA): Integrated chip cooling, used to dramatically increase the operational power of high voltage silicon-based power devices. This is done by increasing the power device heat-removal via an integrated active cooling microelectromechanical system (MEMS) within the power chip device.

Deficiency in the SOTA: The manufacturing techniques of the integrated chip cooling systems are limited due to low tolerance of the manufacturing process. The pressure difference is a large contributor to a fully functional cooling device.

Solution Proposed: Refine in-chip jet-impingement geometry through leveraging theory and a parametric evaluation of nozzle geometry and flow channel arrangements. With theory proposed and constraints implemented a 1 cm^2 surface area, Si-base unit will be prototyped to maneuver high heat dissipation.

Relevance to OSPRES Grant Objective: Increase cooling densities for high pressure microwave (HPM) systems, while decreasing pumping power requirements, in-line with the SWaP-C^2 objective.

9.2.2 Tasks and Milestones / Timeline / Status

(A) Write an STTR proposal for an ultra-compact integrated cooling system. / APR21–DEC21 / In Progress.

(B) Use manufacturing constraints to design a Si base 1 cm^2 unit to achieve high heat dissipation. The design must be able to be produced by manufacturing techniques such as etching and lithographic layering processes / MAY21–JUL21 / Completed

(C) Using the optimal design, perform ANSYS simulations using either water or Si-C nanofluid. Other fluid types may be researched as pressure drop is a large factor / JUL21–SEP21/ In Progress

9.2.3 Progress Made Since Last Report

(A) Discussed future design possibilities and partnership with RDT to manufacture micro-integrated cooling devices. Design possibilities are directly related to the manufacturing process for MEMS devices. The manufacturing techniques proposed were discussed how, if possible, to produce the in-chip cooling technology. Such designs were discussed involving cross flow microchannels. An ideal system to

produce would push towards an on-chip TMS and could be attached to such semiconductor devices as needed instead of directly embedded on the chip.

(B) Since the manufacturing ability has a tolerance of nearly 10 microns, the optimal jet diameter will be initially tested at 100 microns (0.1 mm). An initial design using the manufacturing constraints was created, following future computational fluid dynamics analysis. The design implements a variety of units found in literature.

(C) Simulation was set-up using the optimal design of a 1 cm^2 unit, although meshing errors occur in the nozzles. A section of the optimal design was created and beginning the setup stage for simulation results.

9.2.4 Technical Results

Ratios regarding nozzle diameter and height were concluded to set around H/D=0.5-0.8 to enable the most interactive fluid contact. The simulation modeling is on-going and results will be achieved in the upcoming reports.

9.2.5 Summary of Significant Findings and Mission Impact

- A water-cooled, cross-flow microchannel cooling system with various microchannel widths etched into GaN and Al/GaN monolithically. An experimentally achieved heat flux of 1.7 kW/cm^2 using 0.056 W of pumping power. Although the cross-flow design is not the best fit under manufacturing constraints, the theory of using channels is remarkable and further analyzed.
- A water-cooled hybrid of microchannels with impinging jets. This design implemented the idea of having jets confined in their own individual spaces reaching up to 900 W/cm^2 with 0.83 W of pumping power.
- A hybrid consisting of multiple jet arrays with microchannel draining ways produced up to 1200 W/cm2 using 1.52 W of pumping power.
- Two types of jet impingement/microchannel heat sinks were experimentally tested with a constant heat flux of 100 W/cm^2. The temperature difference was from 60 to 35 C which proposed giving the design more power. Having oblique angled fins caused 20 percent greater heat transfer.
- Geometry and microchannel techniques were thoroughly reviewed based on manufacturing tolerances and techniques. An initial design was conducted following the beginning of the simulation process in ANSYS, as meshing issues occur within the large number of micro-scaled nozzles.

10.0 UAS Engagement Wargaming & Modeling and Simulation (M&S)

10.1 Fixed-Effector Wargaming Simulation Toolkit Development

(Nolan Petersen and Travis Fields)

10.1.1 Problem Statement, Approach, and Context

Primary Problem: Wargaming simulations enable rapid evaluation of different weapon systems and strategies. However, the lack of easy to use, high-fidelity software tools makes producing and studying different engagement scenarios (i.e., one friendly system versus five hostile agents) difficult and time-consuming.

Solution Space: We propose developing a simulation environment using the Unity real-time development platform to offer an easy-to-use, medium-fidelity environment for the purpose of studying different blue vs. red engagement scenarios. Unity is a well-established game development software, with a strong community base for tutorials, training, and software assistance. This makes Unity an ideal solution for a medium-fidelity simulation environment to narrow down optimal fixed effector configurations, which could then be studied further in a higher fidelity environment.

State-of-the-Art (SOTA): Current software tools for this purpose are tedious to adapt and/or modify for running different scenarios due to a lack of support as well as documentation.

Relevance to OSPRES Grant Objective: The ability to simulate and benchmark performance of different scenarios, such as different fixed-effector positions, types, and targeting strategies to provide insight into the ideal utilization of HPM-related systems.

Risks, Payoffs, and Challenges:

Risk: There is an infinite number of scenarios and configurations, making generalizations difficult from within a simulation environment.

Challenges: Focusing the tradespace while simultaneously capturing sufficient realism.

Payoff: The simulation tool could provide tremendous insight and actionable information for both source development and laydown/asset allocation.

10.1.2 Tasks and Milestones / Timeline / Status

(A) Reproduction of previous results obtained from the previously used wargame software Modern Air Power by John Tiller Software, which is no longer in development, using the Unity environment / MAY21 – JUN21 / Completed.

(B) Implementation of radar uncertainty into simulation environment, enabling increased realism to better simulate current targeting capabilities / JUN21 – JUL21 / In Progress.

(C) Trade-space study of microwave, tracking, and hostile agent performance to identify key limitations and low-risk, low-cost improvements, enabling increased weapon efficacy / JUL21 – SEP21 / In Progress.

10.1.3 Progress Made Since Last Report

(B) A Gaussian random number generator has been implemented to simulate radar uncertainty.

10.1.4 Technical Results

(B) After the reproduction of previous results from Modern Air Power by John Tiller Software was completed, we determined that realism in targeting would be important to generating meaningful results. To implement more realistic targeting, we chose to first simulate the use of radar. After performing a radar literature review, three values most important to accurately simulating radar were identified: (1) maximum detection range, (2) signal to noise ratio (SNR), and (3) radar uncertainty. The maximum detection range is dependent on system-specific radar parameters (e.g. transmitter power, receiver power, etc.) and the SNR is dependent on the maximum detection range, distance to the target, as well as terrain interference. Because maximum detection range could change so drastically depending on different system parameters, we decided to model it with an average detection range of multiple radar systems for the time being. As for the SNR, it will still be dependent on the previously mentioned parameters but can be further abstracted for modeling as a simple time factor from initial detection to localize the target in space. In contrast, the radar uncertainty is much simpler to model primarily because modern radar manufacturers provide the known uncertainties in each measurement. We chose to model this uncertainty with a Gaussian distribution because its parameters could be fit to match behavior associated with real radar data. This was done by adding randomly sampled, Gaussian-distributed displacements to the true x, y, and z coordinates of the target(s) to produce a “perceived” UAV position, which our simulated weapons system will use for targeting in future studies. To visualize this treatment, we considered a scenario in which 32 equally spaced UAV attackers began on a 700-meter radius circle and moved towards a radar system located at the center of the circle. For this example, the mean and standard deviation of the Gaussian distribution were set to 0 and 12.5 m, respectively, and we assume each UAV has entered the maximum detection range and has been localized in space. At two different times, the true and perceived two-dimensional coordinates of each UAV in the plane of the circle were determined as indicated in Figure 10.1.1.

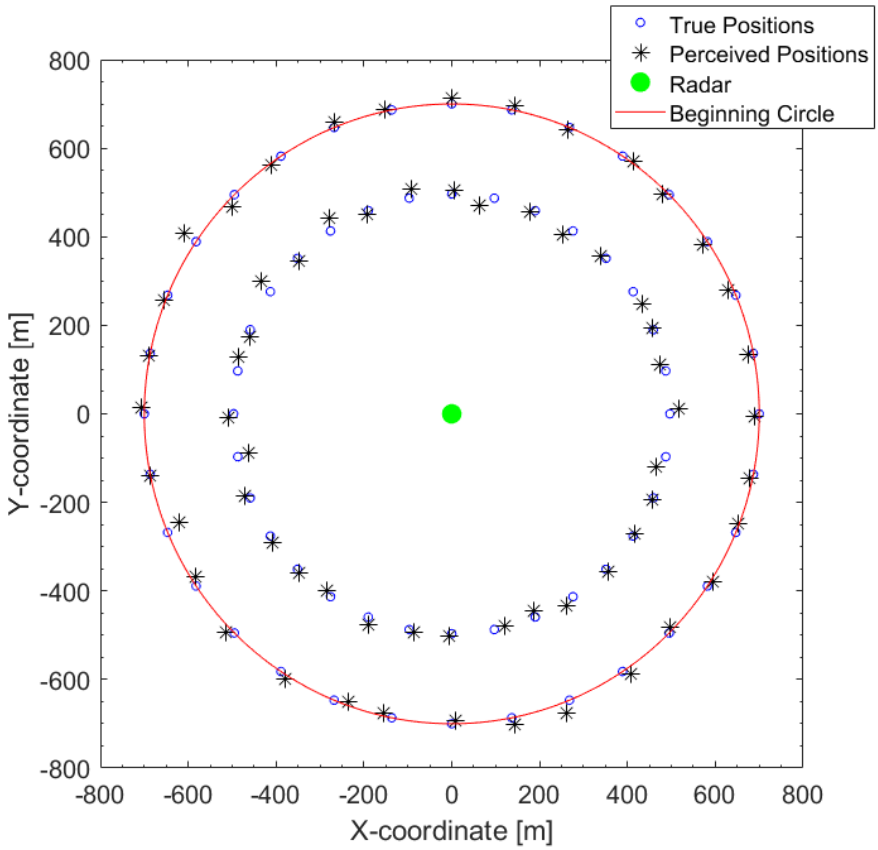


Figure 10.1.1. True and perceived positions of UAVs.

10.1.5 Summary of Significant Finding and Mission Impact

(A) Reproduction of previous results obtained from Modern Air Power by John Tiller Software was completed, which provided a framework to implement new features.

(B) Implementation of radar uncertainty into the simulation environment was completed.

10.2 Airborne Effector Weapons Target Assignment

(Cody Smith and Travis Fields)

10.2.1 Problem Statement, Approach, and Context

Primary Problem: Unmanned aircraft technological development trends suggest the potential for the application of both coordinated and cooperative hostile sUAS attacks in the near future. Defense strategies are currently under development which primarily utilize aerial- or ground-based defense systems or a layered combination of the two. An engagement with multiple blue (friendly) vehicles against many red (hostile) vehicles

presents an interesting challenge in assigning which blue engages which red(s) as the computational burden grows factorially.

Solution Space: We propose using various heuristics like the Genetic Algorithm (GA) to solve the Multiple Weapons to Multiple Targets Assignment Problem (MWMTAP) (a generalization of the Multiple Traveling Salesman Problem with Moving Targets (MTSPMT) and an extension of the Weapon Target Assignment (WTA) Problem) in order to produce computationally efficient task assignment allocations to the blue forces.

State-of-the-Art (SOTA): Many current techniques consider stationary targets and/or holonomic vehicles, which within the proposed scenario are not applicable. Considering the target assignment problem with constrained (or realistic flight-like) motion with many potential targets that must be intercepted with several friendly assets is a unique (at least in the literature) problem.

Relevance to OSPRES Grant Objective: The concepts for WTA are applicable to both fixed and airborne weapon systems. Developing the strategies for assigning assets is critically important for considering layered defense scenarios, as the battlefield is now heterogeneous with a diverse array of capabilities, performance, and cost.

Risks, Payoffs, and Challenges:

Risk: The computational complexity of task assignment can quickly become unrealizable, particularly for onboard hardware.

Challenges: Creating an efficient, robust, and effective task assignment framework that can be computed on low power onboard microcomputers.

Payoff: A robust task assignment framework is the first step in creating an automated decision engine that could be used for any DEW weapon system.

10.2.2 Tasks and Milestones / Timeline / Status

(A) Literature review on task-assignment-related studies/research activities / MAR21–MAY21 / Completed.

(B) Implementation and evaluation of engagement-level WTA (one vs. few) in simulated environment / MAY21–JUN21 / Completed.

(C) Implementation and evaluation of mission-level WTA (few vs. many) in simulated environment / JUN21–JUL21 / In Progress (Final Stages).

(D) Dissemination of the performance of various metaheuristics such as the GA for realistic mission and engagement-level scenarios / AUG21–SEP21 / In Progress.

10.2.3 Progress Made Since Last Report

(B) Final verification of the programmatic implementation of the brute force algorithm was completed for engagement-level WTA (one vs. few) scenarios.

(C) Implementation and initial verification of the programmatic implementation and evaluation of mission-level WTA (few vs. many) scenarios.

(D) Development is underway in implementing metaheuristics such as the genetic algorithm to solve for the MWMTAP, and a comparative analysis on various encoding, crossover, and mutation techniques for the GA is being performed.

10.2.4 Technical Results

The current study aims to develop a framework comprised of the necessary algorithms required for effective path-planning optimization and weapons target assignment (WTA) for both aerial- and ground-based weapons during hostile unmanned aerial threat engagements. Historically, various types of algorithms such as the auction, genetic, and brute force algorithms have been used for path planning and WTA. The development of an effective WTA framework will require algorithms that are capable of handling a combination of features from several of the common path planning problems: for example, the Traveling Salesman Problem with Neighborhoods to manage conditions where direct interception is not required, the Moving Traveling Salesman Problem where incoming hostile targets are known to be moving, and the Dynamic Traveling Salesman Problem where assigned paths are updated with the emergence of previously unknown threats. Various heuristics are to be studied and a comparative analysis is to be performed using popular path planning algorithms (i.e. auction and genetic algorithms) to gain insight and develop situational strategies for potential aerial threats. Currently, an analysis tool has been developed using brute force that is capable of outputting the optimal path, path length, and time of completion for one or multiple friendly systems to intercept a small number of incoming hostile threats ($n < 9$). We developed this software to be used as a tool for comparative analysis with heuristic approaches like the genetic and auction algorithms. Customizable parameters include blue starting position, red starting positions, red starting speeds, minimum protection radius, and number of reds. Additionally, various aspects such as patrol and detection radius will be evaluated. An example 1 vs. 4 brute force engagement solution is provided in Figure 10.2.1 and a 4 vs. 6 brute force engagement solution is provided in Figure 10.2.2. Work in progress includes a final verification of the brute force tool for few vs. few scenarios and the beginning stages of construction and implementation of the genetic algorithm for solution comparisons.

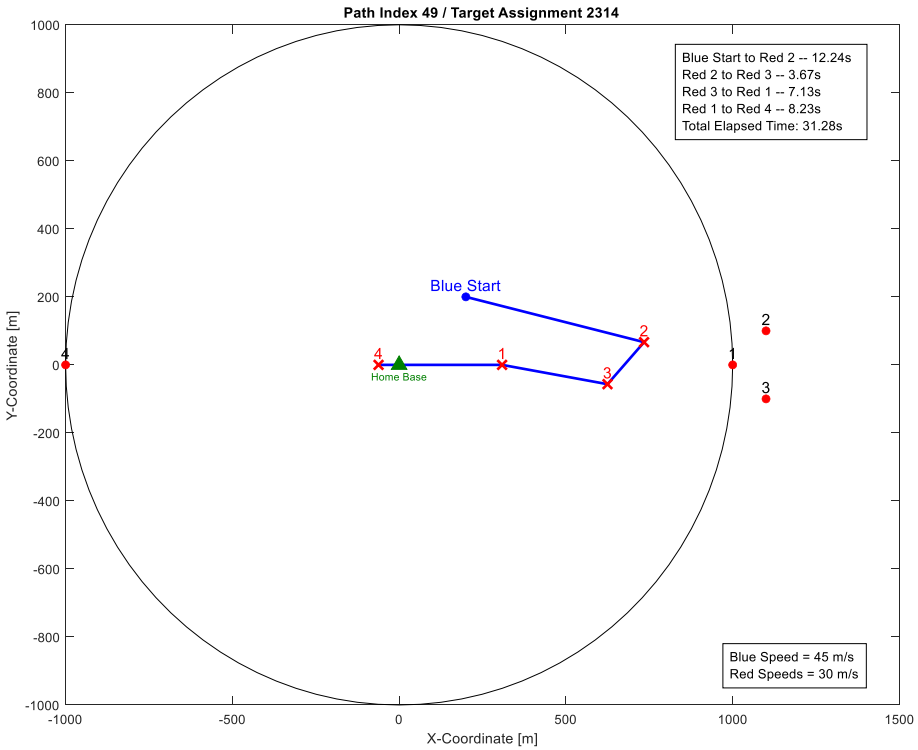


Figure 10.2.1. One versus four brute force-derived optimal trajectory.

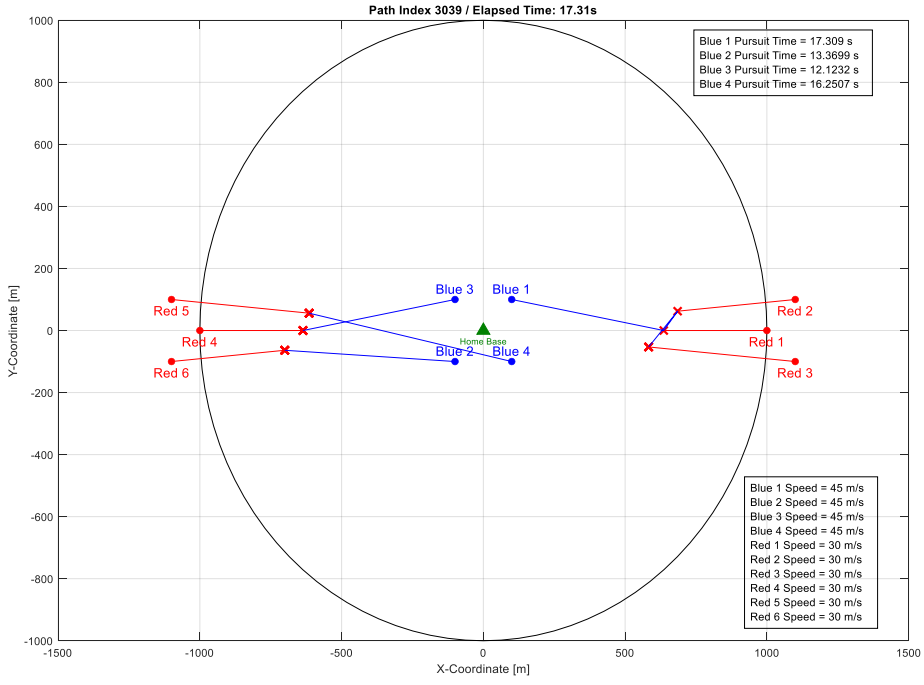


Figure 10.2.2. Few versus few brute force-derived optimal trajectory.

10.2.5 Summary of Significant Findings and Mission Impact

(A) A review of the task assignment literature was completed and two key strategies were identified: genetic algorithm and auction algorithm.

(B) A programmatic solution using the brute force algorithm to solve for the engagement-level WTA was constructed. This tool is capable of finding optimal solutions in one vs. few scenarios.

(C) A programmatic solution using the brute force algorithm to solve for the mission-level WTA was constructed. This tool is capable of finding optimal solutions in few vs. few scenarios and will be used to compare output solutions from the previously described heuristic approaches.

11.0 Program Management

11.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

11.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

11.3 Major Procurement Actions

11.4 Travel

Destination	Purpose	Attendees	Estimated Costs

11.5 Pending or Upcoming Public Release Requests

12.0 Appendix A: Academic and IP Output

12.1 Students Graduated

Name	Degree	Currently
Al-Shaikhli, Waleed	MS Spring 19	Kansas City National Security Campus, Honeywell
Berg, Jordan	MS Spring 21	
Bissen, Bear	MS Spring 19	UMKC/MIDE (Staff)
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Hanif, Abu	PhD May 21	
Harmon, Aaron	BS	Missouri University of Science & Technology
Harp, Joshua	MS	Small Business
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Klappa, Paul	MS Spring 21	
Labrada, Dario	BS Spring 20	UMKC/MIDE (MS Student)
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory
Renzelman, Jeff	MS Spring 18	Kansas City National Security Campus, Honeywell
Roy, Sourov	PhD Spring21	UMKC/MIDE (Staff)
Wagner, Adam	MS Fall 20	Kansas City National Security Campus, Honeywell
Xia, Shengxuan	BS	Missouri University of Science & Technology

12.2 Journal Publications

12.2.1 In Preparation

[1] N. Gardner, A. N. Caruso, and P. Doynov, “Diode-Based Non-Linear Transmission Line: A Bandwidth and Center Frequency Tuning Study,” *Transactions on Microwave Theory and Technique*, In Preparation, **2021**.

[2] B. Barman, D. Chatterjee, and A. N. Caruso, “Tradespace analysis of wideband coaxial probe-fed microstrip patch electrically small antenna elements,” In preparation, **2021**.

[3] M. Z. M. Hamdalla, B. Bissen, J. D. Hunter , L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, “Experimental Evaluation of CMA Predictions and Control of Electromagnetic Interference to UAVs,” In Preparation, **2021**.

[4] S. Xia, J. Hunter, A. Harmon, M. Hamdalla, A. Hassan, V. Khilkevich, D. Beetner, “Simulation Driven Statistical Analysis of the Electro-magnetic Coupling to Microstriplines,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[5] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, “Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field Coupling to Randomly Shaped Wires,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

12.2.2 Submitted / Under Revision

[6] W. Azad, F. Khan, and A. N. Caruso, "A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Featuring Custom Isolated Gate Driver Circuit Combined With Coupling and Snubber Circuits," *IEEE Transactions on Power Electronics*, Submitted, **2021.**

[7] J. N. Berg, R. C. Allen, and S. Sobhansarbandi. "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation." *International Journal of Thermal Sciences*, Submitted, **2021**.

[8] Khulud Alsultan, Mohamed Hamdalla, Sumitra Dey, A. N. Caruso, Praveen Rao, and A. M. Hassan, "Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform," *IEEE Open Journal of Antennas and Propagation,* Submitted, **2020**.

[9] John Keerthi Paul Bhamidipati, Eliot R. Myers, Adam M. Conway, Lars F. Voss, and Anthony N. Caruso, "Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches," *IEEE Transactions on Electronic Devices*, Under Revision, **2020**.

12.2.3 Published / In Press

[10] W. Azad, F. Khan, and A. N. Caruso, "A Medium Power, Self-Sustaining, Configurable RF Pulse Generation Circuit Using a Nonlinear Transmission Line and Power Amplifier in a Closed Loop Configuration, *IEEE Transactions on Plasma Science*, **2021** [doi].

[11] S. Roy, W. Azad, S. Baidya and F. Khan, "A Comprehensive Review on Rectifiers, Linear Regulators and Switched-mode Power Processing Techniques used for Powering Biomedical Sensors and Implants utilizing In-body Energy Harvesting and External Power Delivery," *IEEE Transactions on Power Electronics*, Early Access, **2021** [doi].

[12] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems," *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364-373, **2019** [doi].

12.3 Conference Publications

12.3.1 Submitted / Accepted

[1] B. Barman, D. Chatterjee, and A. N. Caruso, "Effect of Ground Plane Shape and Size on the Input Impedance of a Monopole embedded in a Grounded Dielectric Substrate," submitted to the *2021 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*, Marina Bay Sands, Singapore, December 4-10, 2021.

[2] B. Barman, D. Chatterjee, and A. N. Caruso, “Comparison of Q-Factor Calculation Methods for Wideband Microstrip Patch Antennas,” submitted to the *2021 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*, Marina Bay Sands, Singapore, December 4-10, 2021.

[3] S. R. Shepard and H. A. Thompson, “Self-focusing in Guided and Un-guided Media,” submitted to the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, 2021.

[4] B. Barman, D. Chatterjee, and A. N. Caruso, “Probe-location Optimization in a Wideband Microstrip Patch Antenna using Genetic Algorithm, Particle Swarm and Nelder-Mead Optimization Methods,” accepted in *2021 International Applied Computational Electromagnetics Society (ACES) Symposium*, USA, August 1-5, 2021.

12.3.2 Presented

[5] W. Azad, S. Roy, and F. Khan, "A Single Gate Driver-based Four-stage High-voltage SiC Switch Having Dynamic Voltage Balancing Capability," *2021 IEEE Applied Power Electronics Conference and Exposition* (APEC), Phoenix, AZ, USA, June 9-12, 2021.

[6] W. Azad, S. Roy, F. Khan and A. N. Caruso, "A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuits," *2021 IEEE Kansas Power and Energy Conference* (KPEC), Manhattan, KS, USA, April 19-20, 2021 [doi].

[7] T. Layman, T. D. Fields, and O. A. Yakimenko, “Evaluation of Proportional Navigation for Multirotor Pursuit,” AIAA SciTech Forum, Virtual Event, January 11-21, 2021 [doi].

[8] P. J. Klappa, and T. D. Fields, “Assessment of Fixed-Wing UAV System Identification Models during Actuator and Payload Drop Failures,” AIAA Atmospheric Flight Mechanics Conference, Virtual Event, January 11-21, 2021 [doi].

[9] J. Hunter, S. Xia, A. Harmon, A. M. Hassan, V. Khilkevich, and D. Beetner, “Modeling and Statistical Characterization of Electromagnetic Coupling to Electronic Devices,” *IEEE International Symposium on Antennas and Propagation and NSRM USNC-URSI National Radio Science Meeting*, Boulder, CO, January 4-9, 2021 [doi].

[10] B. Barman, K. C. Durbhakula, B. Bissen, D. Chatterjee, and A. N. Caruso, “Performance Optimization of a Microstrip Patch Antenna using Characteristic Mode and D/Q Analysis,” *2020 XXXIIIrd General Assembly and Scientific Symposium of the International Union of Radio Science*, Rome, Italy (online conference), Aug 29-Sept 5, 2020, pp. 1-4 [doi].

[11] J. Berg, and S. Sobhansarbandi. “CFD Modeling of Thermal Management Systems for a Silicon Semiconductor Switch.” *ASME 2020 Heat Transfer Summer Conference collocated with the ASME 2020 Fluids Engineering Division Summer*

Meeting and the ASME 2020 18th International Conference on Nanochannels, Microchannels, and Minichannels, Virtual, July 13–15, 2020, American Society of Mechanical Engineers Digital Collection [doi].

[12] B. Barman, D. Chatterjee, and A. N. Caruso, “Performance Optimization of Electrically Small Microstrip Patch Antennas on Finite Ground Planes,” 2020 *IEEE International Symposium on Antennas and Propagation and North American Radio Science Meeting*, Montreal, Quebec, Canada, July 5-10, 2020, pp. 1–2 (online conference) [doi].

[13] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, “Scalable Characteristic Mode Analysis: Requirements and Challenges (White Paper),” *Large Scale Networking (LSN) Workshop on Huge Data: A Computing, Networking and Distributed Systems Perspective Sponsored by NSF*, Chicago, IL, April 13-14, 2020.

[14] M. Hamdalla, A. N. Caruso, and A. M. Hassan, “Predicting Electromagnetic Interference to a Terminated Wire Using Characteristic Mode Analysis,” *Proceedings of the Annual Review of Progress in Applied Computational Electromagnetics (ACES)*, Monterey, CA, March 22-26, 2020. [doi]

[15] W. Azad, F. Khan, and A. Caruso, "Self-sustaining High-power RF Signal Generation Using LDMOS Based Power Amplifier and Nonlinear Transmission Line," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 3567-3572 [doi].

[16] A. Hanif, W. Azad, and F. Khan, "Detection of Bond Wire Lift Off in IGBT Power Modules Using Ultrasound Resonators," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 345-350 [doi].

[17] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, “Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS,” *Annual Directed Energy Science and Technology Symposium*, March 2020 (abstract appeared, but talk cancelled due to pandemic).

[18] B. Barman, D. Chatterjee, and A. N. Caruso, “Some Investigations into Mutual Coupling Analysis for Trade Space Studies of Linear Arrays,” *2019 IEEE International Symposium on Phased Array Systems and Technology (PAST)*, Waltham, MA, October 2019, pp. 1-8 [doi].

[19] B. Barman, D. Chatterjee, and A. N. Caruso, “Characteristic Mode Analysis of a straight and an L-probe fed Microstrip Patch,” *2019 IEEE Indian Conference on Antennas and Propogation (InCAP)*, Ahmedabad, India, Dec 2019, pp. 1-3 [doi].

[20] M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of the Effect of the UAV Frame Material on Coupling and Interference," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019 [doi].

[21] M. Hamdalla, J. Hunter, Y. Liu, V. Khilkevich, D. Beetner, A. Caruso, and A. M. Hassan, "Electromagnetic Interference of Unmanned Aerial Vehicles: A Characteristic Mode Analysis Approach," *IEEE International Symposium on*

Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages), Georgia, USA, July 7-12, 2019 [doi].

[22] B. Barman, D. Chatterjee, and A. N. Caruso, "Analytical Models for L-Probe fed Microstrip Antennas," *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

[23] K. C. Durbhakula, J. Lancaster, A. M. Hassan, D. Chatterjee, A. N. Caruso, J. D. Hunter, Y. Liu, D. Beetner, and V. Khilkevich, "Electromagnetic Coupling Analysis of Printed Circuit Board Traces using Characteristic Mode Analysis," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (2 pages)*, Atlanta, Georgia, USA, July 7-12 2019 [doi].

[24] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "On the Location of Transverse Electric Surface Wave Poles for Electrically Thick Substrates," Proceedings of the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 [doi].

[25] M. Hamdalla, B. Bissen, A. N. Caruso, and A. M. Hassan, "Experimental Validations of Characteristic Mode Analysis Predictions Using GTEM Measurements," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Montréal, Québec, Canada, July 5-10, 2020 [doi].

[26] W. Azad and F. Khan, "Sustaining High-power RF Signal Generation in a Positive Feedback Network," *2019 IEEE Pulsed Power and Plasma Science Conference (PPPS)*, Orlando, FL, USA, June 23-28 2019.

[27] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, "Scalable characteristic mode analysis using big data techniques," *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[28] M. Hamdalla, W. Al-Shaikhli, J. Lancaster, J. D. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of Electromagnetic Coupling to Wires with Realistic Shapes," *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[29] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, "Location of Surface Wave Poles in Sommerfeld Integrals: A Mittag-Leffler Expansion Approach," *Proceedings of the URSI-B International Symposium on Electromagnetic Theory*, URSI Commission, San Diego, USA, May 2019 [doi].

[30] K. C. Durbhakula, D. Chatterjee and A. M. Hassan, "Analytical Evaluation of Sommerfeld Integral Tails Present in Two-layered Media Green's Functions," *Proceedings of the Indian Conference on Antennas and Propagation* (InCAP), Hyderabad, India, December 2018 [doi].

[31] D. Beetner, V. Khilkevich, A. M. Hassan, J. Hunter, Y. Liu, and D. Floyd, "Characterization of the Electromagnetic Coupling to UAVs," *DE Systems Symposium*, September 24-27, 2018

[32] C. Hartshorn, K. Durbhakula, D. Welty, D. Chatterjee, J. Lancaster, A. M. Hassan, and A. N. Caruso, "Crosstalk and Coupling to Printed Circuit Board Metallic Traces

with Arbitrary Shapes," *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[33] M. Hamdalla, J. Roacho-Valles, J. Hunter, D. Beetner, A. M. Hassan, and A. N. Caruso, "Electromagnetic Analysis of Unmanned Aerial Vehicles Using Characteristic Mode Analysis," *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[34] C. Hartshorn, M. Hamdalla, J. Lancaster, A. M. Hassan, and A. N. Caruso, "Electromagnetic Vulnerability of Wires with Arbitrary Shape," *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[35] K. C. Durbhakula, D. Chatterjee, A. M. Hassan, and M. S. Kluskens, "Studies on Numerical Evaluation of Sommerfeld Integrals for Multilayer Topologies," *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018.

[36] J. Lancaster, D. Chatterjee, and A. N. Caruso, "Some Investigations into the Dispersion Characteristics of Localized Bessel Beams," published in the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018 (1 page URSI Abstract).

[37] M. Hamdalla, A. M. Hassan, and A. N. Caruso "Characteristic Mode Analysis of Unmanned Aerial Vehicles with Realistic Shapes and Material Composition," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Boston, MA, July 8-13, 2018.

[38] W. Azad, S. Roy, A. S. Imtiaz, and F. Khan, "Microelectromechanical System (MEMS) Resonator: A New Element in Power Converter Circuits Featuring Reduced EMI," *2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, Niigata, May 20-24, 2018, pp. 2416-2420 [doi].

[39] J. Hunter, Y. Liu, D. Floyd, A. Hassan, V. Khilkevich, and D. Beetner, "Characterization of the Electromagnetic Coupling to UAVs," Annual Directed Energy Science and Technology Symposium, Feb 26-March 2, 2018.

12.4 Conference Presentations

[1] W. Azad, S. Roy, and F. Khan, "A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver," *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, 2020 (oral).

DEPS Posters and Presentations 2020

[2] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[3] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

GOMAC 2019

[4] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[5] Eliot Myers, Picosecond High Power Switching Technologies

[6] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium, Destin, Florida, USA, April 2019:

[7] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[8] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[9] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[10] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[11] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[12] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[13] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[14] Deb Chatterjee, Studies On Antenna Characterization And Propogation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

DEPS Posters and Presentations 2018

[15] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[16] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[17] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

DEPS Posters and Presentations 2017

[18] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

12.5 IP Disclosures Filed

Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, 19UMK005, 28SEPT2018

Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal”, 19UMK008, 28DEC2018.

Doynov, “Pulse Differential High-power Microwave Generation”, 19UMK007, 02JAN2019.

Doynov, “Scalable Modular System for High-power Microwaves Generation”, 20UMK010, 19APR2020.

Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna”, 20UMK011, 19APR2020.

Shepard, “A Novel Optical Fiber Amplifier”, 20UMK012, 02JUN2020.

Doynov, Caruso, “High-efficiency High-power Microwave Generation using Multipass Non-linear Network Topologies”, 19UMK017, 29AUG2020.

Shepard, “A Low Noise Optical Amplifier”, 21UMK007, 14SEPT2020.

Bhamidipati, Myers, Caruso, “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources”, 21UMK009, 04NOV2020.

12.6 Provisional Patents Filed

Doynov, Caruso, “High-efficiency High-power Microwave Generation using Multipass Non-linear Network Topologies”, filed 26NOV2019.

12.7 Non-Provisional Patents Filed

None to date

13.0 Appendix B: Jet Impingement Thermal Management System

(Jordan Berg, Roy Allen, and Sarvenaz Sobhansarbandi)

13.1 Executive Summary

HPM systems require powerful and compact cooling systems in order to maintain operational capabilities. A key component that requires significant heat extraction (several hundreds of watts up to 1 kW) are silicon photoconductive semiconductor switches (Si-PCSS). Many methods of thermal management have been studied, which include (in order from lowest to highest heat extraction performance) passive cooling (heat sinks, cooling fins), passive multi-phase cooling (heat pipes), active single-phase liquid cooling (microchannel cooling systems), or active single-phase turbulent cooling (jet impingement systems). To dissipate up to 1 kW of heat, a single-phase jet impingement cooling system was designed. The jet impingement thermal management system (JI-TMS) was studied computationally using fluid dynamics modeling and experimentally through prototype fabrication and testing. The system used a pure silicone fluid (PSF) heat transfer fluid (HTF), chosen for its dielectric strength for operation in close proximity to kilovolt-scale electric fields. The JI-TMS design demonstrated the ability to compensate 200 W (200 MW/m^3) average power and maintain the average temperature of the Si-PCSS source at 50 °C (10 °C lower than a microchannel laminar-flow-based design of equivalent volumetric form-factor). The performance analysis of the optimized geometry and dielectric fluid had certain restrictions with regard to pressure threshold as the system's pressure should not be dramatically increased. Further iterations of the current design are unlikely to meet the stretch goal cooling requirement of >1 kW (1 GW/m^3) due to the large pressure drop that occurs. While jet impingement as a method of heat transfer should still be considered a viable method, the viscosity of the fluid presented a challenge in being able to create turbulent regimes in the JI-TMS. To overcome this challenge, decreasing the JI-TMS nozzle diameters by a factor of 10 and increasing the nozzle count by the same has the potential to increase convection of the coolant, thereby increasing heat extraction capabilities.

13.2 Technical Background

Managing thermal load is critical to the success of HPM systems. Traditional single-phase liquid cooling technologies such as laminar flow microchannels are ubiquitous in cooling applications (primarily for electronics). The microchannel systems are relatively easy to manufacture and perform comparatively with two-phase cooling systems such as heat pipes, but are performance limited and therefore not useful for power density systems. The major drawback with microchannel liquid cooling is associated with the laminar flow heat transfer fluids. Laminar flow has little to no convection. This lack of convection means that the primary driver of heat transfer in a microchannel cooling system is conduction of the fluid and the temperature differential of the fluid and heat sink. The largest temperature differential is created through a higher flow rate. If fluid convection is employed, the thermal management system would then utilize the conduction of the fluid as well as the convection of the fluid to drive heat away from the heat component. With this additional medium of heat transfer, the heat extraction performance could be

increased. This forced convection method is considered for HPM thermal management systems.

While a microchannel TMS fluid traverses the length of the heated surface in a laminar flow regime, a jet impingement (JI) TMS directs fluid normal to the heated surface though an array of nozzles. Figure 1.1 shows this process more clearly.

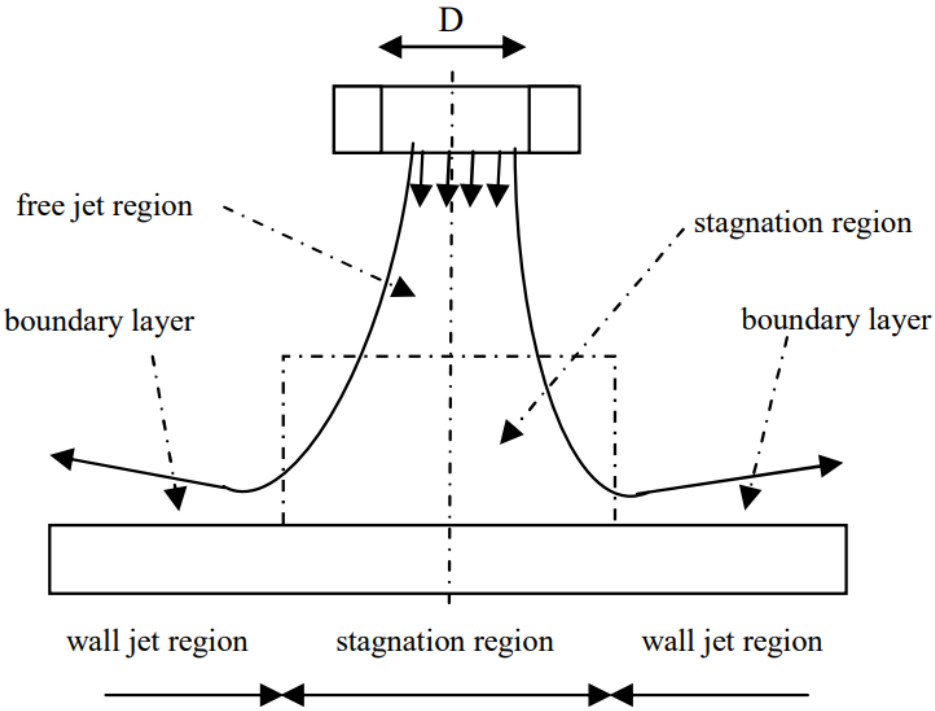


Figure 1.1. Diagram of jet impingement flow regimes.

Ideally, this flow orientation creates a central region (known as the stagnation region) that produces the maximum heat transfer of the fluid due to extreme turbulence. As fluid spreads out radially away from the stagnation region, the HTF creates vortices along the heated surface, which dramatically increase the heat transfer coefficient (HTC, *h*, units of W/m^{2}K. This increase in the HTC drives the heat transfer due to convection shown in the following equation.

$$Q = hA\Delta T$$

where Q is the heat removed in Watts, A is the area of focus that heat flux occurs, and ΔT represents the temperature difference between the heated surface and the fluid that contacts the wall.

Successful JI systems can yield HTC values of $4 \times 10^4 – 1 \times 10^5$ W/m^{2}K or more [1], and have seen heat removal rates more than 40% higher than those of microchannel cooling systems [2]. In reality, there is no limit to the HTC value, though increasing it further comes at the cost of exponentially increasing system pressure, as pressure is the driving force

of the flow. This compares to laminar flow systems that maintain HTC levels on the order of hundreds to a few thousands of W/m^2K.

The specific HPM system component of interest is a photoconductive semiconductor switch (PCSS). The threshold goal for cooling the PCSS is to extract ~200 W of heat, with a stretch goal of removing 1 kW. With these goals in mind, we decided to pursue a JI-TMS design given its high HTC capabilities.

13.3 Methods

13.3.1 Computational Fluid Dynamics Modeling

Initially, computational fluid dynamics (CFD) modeling was used to model a microchannel TMS. The microchannel TMS that was modeled was based off of an experimentally tested TMS for PCSS cooling. With the experimental values of PCSS temperature, HTF flow rate, and applied average power to the PCSS, validation of the CFD model was performed. The HTF used in all simulations was a pure silicone fluid with a viscosity of 20 centistokes (hereafter known as PSF-20-cSt). As the PCSS will complete a circuit that handles kV's of electricity, PSF-20cSt was chosen for its dielectric strength. The high dielectric strength of the PSF-20-cSt provides a layer of safety to equipment and personnel in the event of leaks or other system malfunctions by acting as an electrical insulator.

Once confidence in simulating 3D multiphysics problems was gained, an initial jet impingement CAD model was created. The first model utilized 11 1-mm diameter nozzles that were evenly spaced and aligned along the center of the PCSS. The second model consisted of 26 nozzles that were arranged in a staggered pattern. Figure 1.2 shows a top down view of the outline of the PCSS (the large oval) and nozzle locations of each described geometry. An exploded cross section view of the staggered geometry is shown in Figure 1.3. Each of these models utilized the optimal design characteristics suggested by Tadhg S. O'Donovan, et al. and Aaron M. Huber, et al.[3,4]. The characteristics include nozzle to nozzle spacing, distance from nozzle exit to impingement surface, and nozzle diameter.

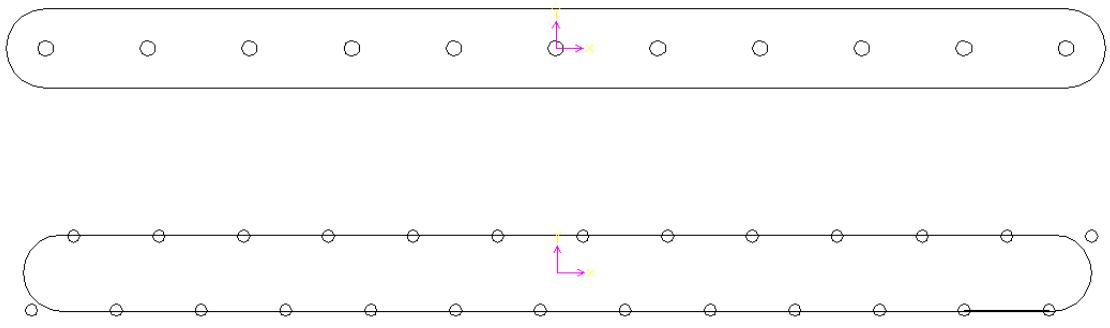


Figure 1.2. The jet impingement geometries showing nozzle locations relative to PCSS.

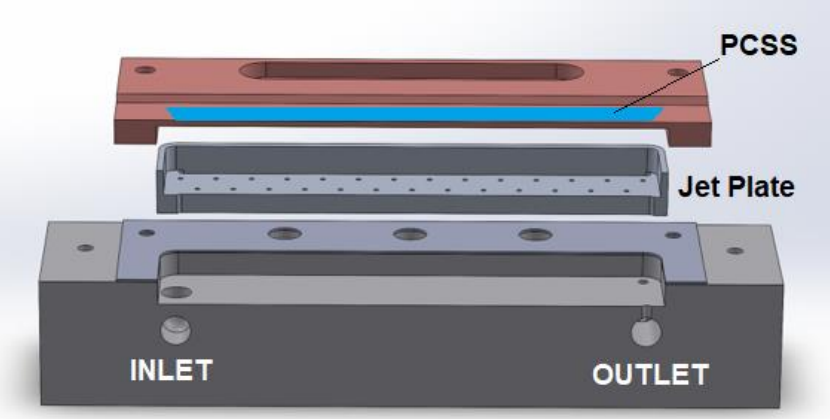


Figure 1.3. Exploded view of the CAD model.

Each geometry was modeled using a flow rate of 0.06 kg/s (approx. 1 gal/min). This flow rate corresponded to the flow rate used for the microchannel TMS used in prior experimentation. Two average powers of 100 and 200 W heat flux were applied to the PCSS. All geometries were studied with varying mesh sizes, with the largest mesh seeing approximately 1.7 million nodes. The CFD simulation utilized the Transition SST numerical solver. Each CFD simulation was set to run for 10000 iterations, or until no change in convergence was seen. Each model's finest mesh saw convergence of all residual error values below 10^{-4}.

13.3.2 Experimental Setup

The prototype staggered array JI-TMS consisted of five parts: a lid, a gasket, a base, a jet-plate, and the PCSS. The lid of the TMS was created from a copper-tungsten (Cu-W) alloy. A gasket was cut from a sheet of butyl-rubber and positioned between the lid and base for the purpose of leak mitigation. Once the parts were assembled, the semiconductor was soldered onto the Cu-W lid using a reflow oven to ensure a uniform bond. A 7 cm wide copper tab was soldered to the topside of the device to allow for a positive DC power supply connection and isolated from all other components using a dielectric sheet made from Rodgers 3003 laminate. A ground wire was secured to the Cu-W component to facilitate completing the current path loop. A chiller/pump was connected to the JI-TMS and was filled with PSF-20-cSt sourced from Clearco. An inline, spring-actuated flow meter was used to monitor the flow rate. Pressure readings were taken from an inline pressure gauge. A FLIR camera was mounted directly above the PCSS and JI-TMS to monitor real-time temperature. The complete setup can be seen in Figure 1.4. A view from the FLIR camera can be seen in Figure 1.5.

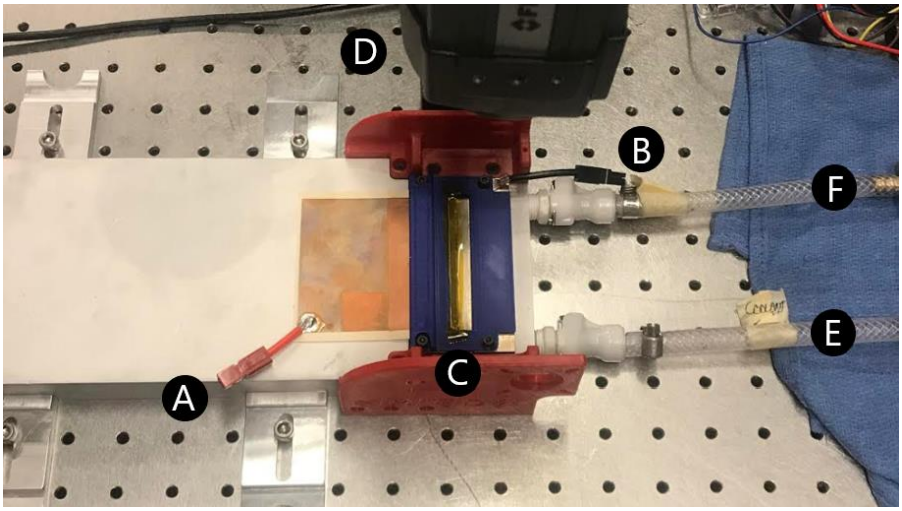


Figure 1.4 Experimental setup, A: Power, B: Ground, C: JI-TMS and device, D: FLIR camera, E: Inlet, F: Outlet.

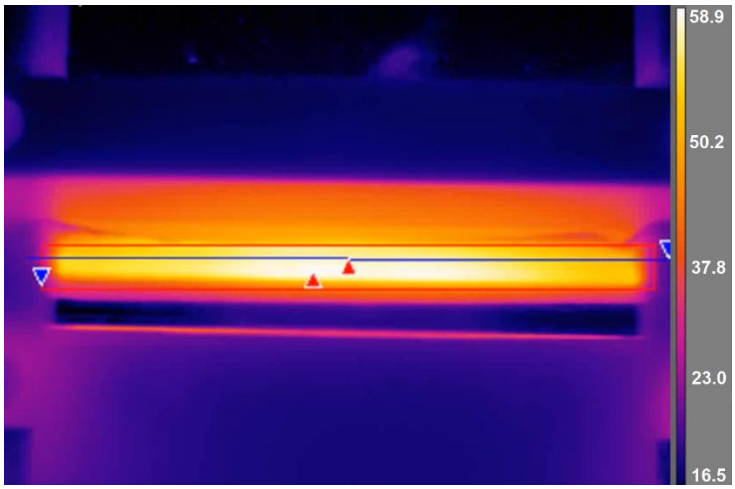


Figure 1.5 FLIR image of PCSS during experiment (°C).

Once the setup was completed, the camera and pump were turned on, followed by the power supply. The temperature of the PCSS was monitored until a steady state was reached, after which the power supply was turned off. The PCSS was allowed to cool until it reached near-ambient temperature.

13.4 Results and Discussion

According to the CFD results, the CFD staggered geometry model performed better than the single-row configuration in regard to keeping the PCSS at a lower temperature. Table 1.1 below summarizes the performance of each model.

Table 1.1. CFD and experimental results of the two JI-TMS designs.

	Single Row CFD	Staggered Array CFD	Experimental*
Pressure Drop (psi)	47.0	46.12	44.7
Heat Trans. Coef. At 200 W (W/m^2K)	20,071	28,472	N/A
Max Switch Temp at 100 W avg power (°C)	57.8	52.6	57.5
Max Switch Temp at 200 W avg power (°C)	114.0	99.0	98.2

*Only staggered geometry tested

The staggered geometry performed better than the single-row geometry by keeping the PCSS at a lower maximum temperature. The HTC value of the staggered geometry was nearly 30% greater than the single-row geometry. This higher HTC value in the staggered geometry is the primary reason for the temperature difference of 15.8 °C for the maximum PCSS temperature, as all boundary and initial conditions were the same for each CFD simulation, as well as the numerical method used. The staggered geometry was able to provide more cooling and keep the PCSS at a lower temperature. For this reason, a prototype of the staggered geometry was created, and the single-row geometry was not studied further.

The results from the CFD simulations were representative of the experimental values, though the temperature and pressure were overestimated slightly. Even though the TMS designs were able to cool the PCSS at 100 W, the numerical and experimental results show that the JI-TMS is unable to maintain the PCSS at a maximum temperature of 80 °C at 200 W of average power. The performance shortcoming stemmed from the requirement of the JI-TMS pressure head. The flow rate of 0.06 kg/s yielded a pressure drop of greater than 38 psi. This flow rate generates an HTC of the fluid of approximately 2.8×10^4 W/m^2K. As mentioned earlier, this HTC is lower than the 4×10^4 W/m^2K value that is indicative of the lower bounds of jet impingement TMS design. While the 4×10^4 W/m^2K value does not represent a hard boundary for achieving true jet impingement flow regimes, it could definitely be considered the lower bound of performance for this JI-TMS. To achieve the desired HTC, JI geometry calculations were utilized to determine the necessary flow rate to achieve a Reynold's number of 2200, a value indicative of transitioning from laminar to turbulent flow. To achieve this value, a flow rate of approximately 0.7 kg/s would be required (an order of magnitude greater). To determine the pressure head requirements for this flow rate, a CFD simulation was run at 0.2 kg/s (this value was chosen rather than the full 0.7 kg/s flow rate to maintain simulation stability).

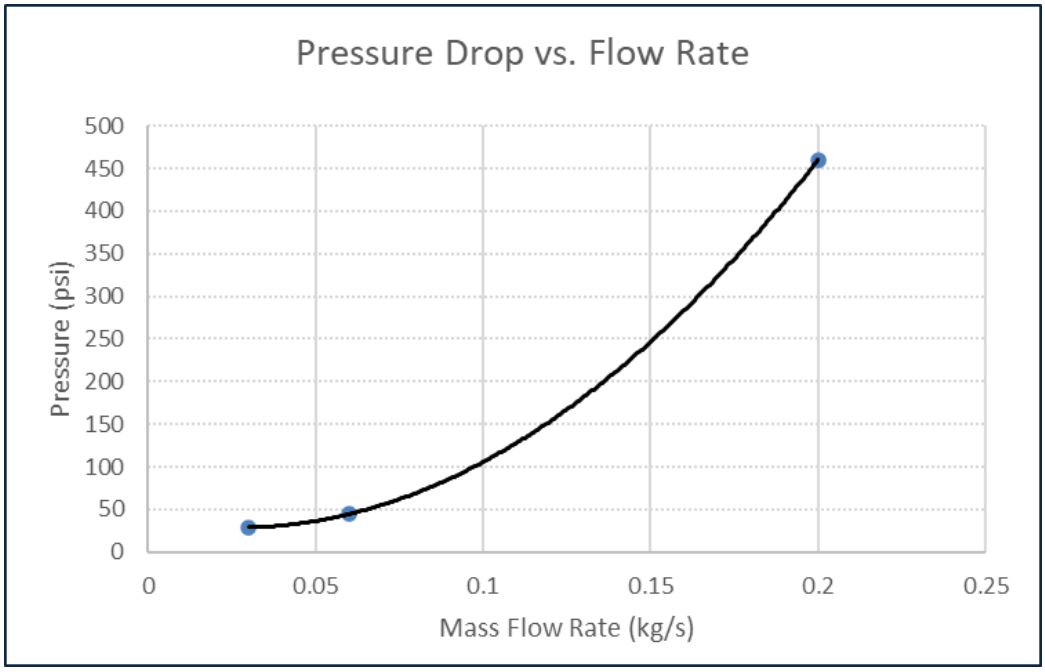


Figure 1.6. CFD results of the pressure drop increase due to increased flow rate.

According to the CFD model, at 0.2 kg/s flow rate, the pressure requirement is more than 450 psi, as shown in Figure 1.6. This pressure is achievable, though it goes against SWaP-C goals and, more importantly, it is still not enough to generate turbulent flow within the system thereby causing significant heat extraction rates. It was determined from these results that at this scale, no amount of geometric optimization would allow for the flow regimes necessary to remove ~1 kW/cm² without generating absurd system pressures requiring large and expensive support equipment.

13.5 Significant Findings

The JI-TMS optimized design was found to be able to compensate 200 W (i.e., >200 MW/m^3) average power and maintain the Si-PCSS source average temperature at 50 °C, which is 10 °C lower than the laminar-flow-based design of equivalent volumetric form-factor (cross-flow thermal management system) – used for the OSPRES Contract's source array demonstrator at the time of this writing. The performance analysis of the optimized geometry and dielectric fluid had certain restrictions with regard to pressure threshold as the system's pressure should not be dramatically increased. Further iterations of the current design are unlikely to meet the stretch goal cooling requirement of dissipating >1 kW (1 GW/m^3) due to the large pressure drop that occurs. While jet impingement as a method of heat transfer is still considered viable, the viscosity of the fluid presented a challenge in being able to create turbulent regimes in the JI-TMS. To overcome this challenge, decreasing the JI-TMS nozzle diameters by a factor of 10 and increasing the nozzle count by the same has the potential to increase convection of the coolant, thereby increasing heat extraction capabilities.

13.6 Publications

[1] Berg, J. N., Allen, R. C., and Sobhansarbandi, S. (2021, Pending), A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation, International Journal of Thermal Sciences.

[2] Berg, J. N. (2021). Development of a Jet Impingement Thermal Management System for a Semiconductor Device with the Implementation of Dielectric Nanofluids. University of Missouri-Kansas City.

[3] Berg, J. N., & Sobhansarbandi, S. (2020, July). CFD Modeling of Thermal Management Systems for a Silicon Semiconductor Switch. In Heat Transfer Summer Conference (Vol. 83709, p. V001T09A011). American Society of Mechanical Engineers.

13.7 References

[1] K. Gould, S. Q. Cai, C. Neft, A. Bhunia, “Liquid jet impingement cooling of a silicon carbide power conversion module for vehicle applications”, IEEE Transactions on Power Electronics 30 (6) (2015) 2975–2

[2] M. K. Sung, I. Mudawar, “Single-phase hybrid micro-channel/micro-jet impingement cooling”, International Journal of Heat and Mass Transfer 51 (17-18) (2008) 4342–4352.

[3] Tadhg S. O’Donovan, et al. "Jet impingement heat transfer – Part I: Mean and root-mean-square heat transfer and velocity distributions". International Journal of Heat and Mass Transfer 50. 17(2007): 3291-3301.

[4] Aaron M. Huber, et al. "Effect of jet-jet spacing on convective heat transfer to confined, impinging arrays of axisymmetric air jets". International Journal of Heat and Mass Transfer 37. 18(1994): 2859-2869.

ONR HPM Program - Monthly Status Report (MSR) – AUGUST 2021

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 SEPTEMBER 2021

Distribution Statement ~A: Distribution authorized to all OSPRES Grant and Contract performers, and any OSPRES uncompensated collaborators. Further dissemination per the Office of Naval Research, Ryan Hoffman (ryan.hoffman@navy.mil, 703-696-3873) or higher DoD Authority.

OSPRES Grant Goal: address and transition technologies and capabilities that enable the OSPRES Grant Objective using the OSPRES Grant Approach, while educating the next generation of pulsed power and defense minded, stewards and innovators.

OSPRES Grant Objective: to execute high-risk, high-payoff efforts that mitigate, fill or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable and electronically steerable high power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average-power space, and includes the kill chain considerations including the target and its responsivity to radiofrequency stimuli.

OSPRES Metrics of Success: developed technologies and capabilities that are published in the peer review, protected as intellectual property, and/or, transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use, as enabling/integratable capability(ies).

OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

OSPRES Grant Security: All efforts should be fundamental and publically releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

1.0 Contents

2.0 Executive Summary 4
2.1 Progress, Significant Findings, and Impact 4
2.2 Completed, Ongoing, and Cancelled Sub-Efforts 6
2.3 Running Total of Academic and IP Program Output 8
3.0 Prime Power and Conditioning 9
3.1 HV Switch Pulsed Chargers 9
4.0 Switch Evaluation and Innovation 12
4.1 GaN:C PCSS Direct RF Modulation 12
4.2 Drift-Step Recovery Diode and Pulse Shaping Device Optimization 14
4.3 Pioneering Drift-Step Recovery Diode Processing and Manufacturing 39
4.4 Characterization of SOS Diode Performance through DOE Augmentation 47
4.5 DSRD-Based Pulsed Power Source Systematic Topological Optimization 53
4.6 Optimizing SOS-IES Pulse Generator Performance with Machine Learning 61
4.7 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners 64
4.8 Characterizing and Optimizing On-state Resistance in GaN:X PCSS 70
5.0 Pulse Forming Networks 74
5.1 Diode-Based NLTLs 74
6.0 Tradespace Analysis of Ultra-Wide-Band Antenna Arrays 79
6.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs) 79
6.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna 86
6.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna 94
6.4 Tradespace Analysis of Ultra-Wide-Band (UWB) Fractal Antenna 101
7.0 RF Coupling 109
7.1 Enclosure Effects on RF Coupling 109
8.0 Laser Development 114
8.1 Fiber Lasers and Optical Amplifiers 114
8.2 WBG-PCSS Enabled Laser Diode Array Driver 121
9.0 Thermal Management 127
9.1 Ultra-Compact Integrated Cooling System Development 127
10.0 UAS Engagement Wargaming & Modeling and Simulation (M&S) 130
10.1 Fixed-Effector Wargaming Simulation Toolkit Development 130
10.2 Airborne Effector Weapons Target Assignment 133
11.0 Software-Defined Medium-Power Microwave Pulse Generator 136
11.1 Development of a GaN-Based Power Amplifier RF Source 136
12.0 Program Management 143
12.1 Issues 143
12.2 Interactions with Others 143
12.3 Major Procurement Actions 143
12.4 Travel 143
12.5 Pending or Upcoming Public Release Requests 143
13.0 Appendix A: Academic and IP Output 144

13.1 Students Graduated 144
13.2 Journal Publications 144
13.3 Conference Publications 146
13.4 Conference Presentations 149
13.5 Theses and Dissertations 152
13.6 IP Disclosures Filed 152
13.7 Provisional Patents Filed 153
13.8 Non-Provisional Patents Filed 153
14.0 Appendix B: Si-PCSS Top Contact Optimization 154
14.1 Executive Summary 154
14.2 Objective 154
14.3 Technical Background 155
14.4 Tasks, Milestones, and Status 157
14.5 Methods and Approach 159
14.6 Results and Discussion 160
14.7 Summary and Recommendations 166
14.8 Outputs 167
14.9 References 167

2.0 Executive Summary

2.1 Progress, Significant Findings, and Impact

IES Pulsed Power Source Technology Leveraging DSRDs. Multi-physics simulations, fed from new I(V) and C(V) data now yield a <10% error in the peak voltage, risetime and FWHM for a 1x1 pulse generator topology. From this result, we can now execute the full NxM topology optimization effort. DSRDs are also being studied for pulse compression and compared with classical options, as a means of drastically improving the compression technology SWaP.

Diode-Based Nonlinear Transmission Line. Both the K50F and K100F D-NLTLs were tested using a 3-kV Marx input. The K50F line successfully yielded solitons with a center frequency of 595-MHz and a Bragg frequency of 961-MHz. The K100F line did not break the waveform into solitons, but produced a Bragg frequency of 1.25 GHz, showing that even with the slower rise and longer pulse length Marx (relative to the previously reported sources), excitation in the 1-GHz regime is still possible and opens potential source offerings with the ultralight weight and volume diode-based NLTLs.

Antennas. A single wideband coaxial probe-fed microstrip ESA element has been designed and prototyped from a 1-inch-thick, circular shaped, copper-backed TMM-10i substrate for the UHF range (684-944 MHz), and characterized. A parametric study of a 5×5 array of the ESA elements was performed on an infinite ground plane, as a function of inter-element spacing; the best average gain 16-dBi over a radiating area of 0.53-m^2 has been identified. If the ground plane can be reduced in area and voltage holding prevails, this work has a good shot at beating the lower risk BAVAs.

The first 3D printed prototype of the Koshelev and Shark antennas have been completed and are currently undergoing electroplating. Time domain simulations of the Koshelev array antenna show that a bipolar signal input yields 10x greater radiation efficiency than the monopolar counterpart (10x is a lot; it's not clear why and we'll prove it out for next month). The Shark array antenna additionally displayed good time domain radiating properties with less signal distortion and an adequate rE/V of 7.4. Finally, the root mean square error (RMSE) for the ML models for antenna response prediction is below 1%; we expect good match to forthcoming empirical measurements.

RF Coupling. A UAV wire tool and full validation of the Predictive-package for Electromagnetic Coupling to Nonlinear-electronics using Equivalent-circuits & Characteristic-modes" (PECNEC) tool was added/completed. PECNEC is used to compute the RF-induced overvoltage conditions on linear/non-linear circuit elements using SPICE solvers at ~100x faster than full-wave simulations with no loss in accuracy. The objective of PECNEC is a predictive tool for effects teams to reduce total measurements burden of the excitation/load parameter space. Validation of our package versus the full-wave solver demonstrated agreement against the FEKO full-wave solver with a maximum error of 5%. Moreover, the computational time of the package is significantly less than that of the full-wave solver.

Fiber Laser. Advancements in the very high-power operating point of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) are shown to permit a single laser to trigger an array of N PCSS – reducing the laser system cost, by N and eliminating the optical timing jitter constraint. We have pushed the state of the possible into the realm of tens of GW (within a single tubular waveguide) which could drive N = 100 Si-PCSS (at 10 MW peak power each) and we present a power splitter design for N = 12 (to drive a 4x4 Si-PCSS array). The optical power tube could be incorporated as the last stage of our fiber laser system – the development and empirical demonstration of which is on schedule.

Laser Diode Array Driver. The frozen wave generator (FWG) prototype implementing coaxial cable delay lines has been retested for 2-, 4-, and 8-segment configurations with varied delay line arrangements for balanced and unbalanced loads. Pulse overlap and pulse deformation observed in the 8-segment unbalanced load configuration has been addressed partially, but the issue with non-simultaneous switching of the transmission line still exists. A more efficient way to connect the transmission lines and the switch needs to be explored. In parallel, a 4-segment FWG implementing lumped-element LC networks as delay lines has been successfully demonstrated on an integrated PCB. Parasitics are presently dominating the performance of the 8-segment configuration, which will be addressed in the next iteration. Also, tunable LC networks will be implemented in the next iteration to facilitate dynamic/controlled delay/waveform-tuning.

Thermal Management. Toward development of the ultra-compact integrated cooling system, geometry and microchannel techniques were thoroughly reviewed based on manufacturing tolerances and techniques. An initial design was developed following the beginning of the simulation process in ANSYS; meshing the large number of micro-scaled nozzles presents a computational challenge that we're addressing.

UAS Engagement Modeling and Simulation. Evaluation of tracking uncertainty on the effector slew rate indicates the effectiveness can be decreased; however, incorporation of off-beam effects can increase effectiveness (and improves realism). Technical development of the machine learning algorithms has been completed and is now being fine tuned prior to task assignment assessment.

GaN-Based Power Amplifier RF Source. We have begun development of a non-MMIC (i.e., discrete transistor) RF amplifier, leveraging the ones-of-kW GaN HEMTS now available (e.g., MACOM 2600-W A1500). When the long pulse width signals are compressed, the peak power and energy are commensurate that required from the OSPRES contract program, and a strong differentiator from GaN MMIC based array technologies. Magnetic Pulse Compression (MPC) and time reversal (Drikas collaboration) are two foci. If MPC lives up to its literature-based promise, and a narrow high gain antenna is employed, portable GaN-based amplifier systems with >100-m range-to-effect could be realizable.

Summary Report. A summary report has been provided in Appendix B for the Si-PCSS Top Contact Optimization sub-project.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

2.2.1 Ongoing Sub-Efforts

	Start	End
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
HV Switch Pulsed Chargers	DEC 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Enclosure Effects on RF Coupling	OCT2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization	JAN 2021	Present
UAS Engagement M&S	MAR 2021	Present
DSRD-Based IES Pulse Generator Development	APR 2021	Present
Drift-Step Recovery Diode Manufacturing	MAY 2021	Present
IES Diode Characterization	MAY 2021	Present
IES Pulser Machine Learning Optimization	MAY 2021	Present
Sub-Nanosecond Megawatt Pulse Shaper Alternatives	MAY 2021	Present
Ultra-Compact Integrated Cooling System Development	MAY 2021	Present
GaN-Based Power Amplifier RF Source	AUG 2021	Present
Reconfigurable RF Pulsed-Power Source	AUG 2021	Present
RF Driver Unit for GaN SD-MPM Power Amplifier	SEPT 2021	Present
Reconfigurable RF Antenna for SD-MPM Sources	SEPT 2021	Present

2.2.2 Completed Sub-Efforts

Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
Nanofluid Heat Transfer Fluid	NOV 2020	JUL 2021

2.2.3 Cancelled/Suspended Sub-Efforts

Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019

Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020
Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021
Bistable Operation of GaN	FEB 2021	MAR 2021

2.3 Running Total of Academic and IP Program Output

See Appendix for authors, titles and inventors (this list is continuously being updated)

Students Graduated	*5 BS, 8 MS, 3 PhD*
Journal Publications	*3 (6 submitted/under revision)*
Conference Publications	*33 (4 submitted/accepted)*
External Presentations/Briefings	*17 (23 submitted/accepted)*
IP Disclosures Filed	*11*
Provisional Patents Filed	*3*
Non-Provisional Patents Filed	*0*

3.0 Prime Power and Conditioning

3.1 HV Switch Pulsed Chargers

(Wasekul Azad and Faisal Khan)

3.1.1 Problem Statement, Approach, and Context

Primary Problem: Commercially available high-voltage solid-state switches made by BEHLKE are the best in SWaP-cooling, but are expensive, have long lead times (2–3 months), and are made outside of the US. For the Navy afloat mission to be successful, we need a sustainable supply of US-manufactured switches at a much lower cost.

Solution Space: Design and demonstrate modular high-voltage (~10 kV) and fast (repetition frequency = 100 kHz) solid-state switches using a combination of series- and parallel-connected commercially available inexpensive discrete MOSFETs and custom high-voltage (~10 kV) isolated gate drivers.

Sub-Problem: Voltage balancing among the series-connected MOSFETs, minimization of gate signal delays, cooling of the individual MOSFETs, balancing resistors, high-voltage isolation required for the power supplies, and the controlling pulse width modulated (PWM) signal as well as differential voltage feedback measurement across individual MOSFETs.

State-of-the-Art (SOTA): Direct liquid-cooled solid-state switch from BEHLKE (e.g., HTS-151-30).

Deficiency in the SOTA:

1. BEHLKE-made switches are expensive. For instance, a single HTS-151-30 switch costs around $5,000.
2. BEHLKE switches along with direct liquid cooling units occupy a considerable amount of space. For instance, an HTS-151-30 switch from BEHLKE has a footprint of approximately 225*85*75 mm without considering the liquid cooling system. Some key parameters of this switch are as follows.

   i) Maximum operating voltage = 15 kV

   ii) Maximum continuous load current = 2.52 A (without cooling), 30 A (with liquid cooling)

   iii) Maximum turn-ON peak current = 300 A (pulse width = 200 µs, duty cycle <1%)

   iv) Turn-ON resistance = 1.3 Ω
3. Once the switching frequency is greater than 10 kHz, a liquid cooling system is required to operate the BEHLKE switch.
4. Without liquid cooling, the maximum continuous power dissipation (P_{cont}) of the BEHLKE switch is limited (e.g., for HTS-151-30, P_{cont} is 10 W without liquid cooling).
5. At a higher switching frequency (>20 kHz), the BEHLKE switch requires multiple ancillary DC power supplies, i.e., 5, 15, and 60 V.

6. The switches made by BEHLKE cannot be reconfigured to withstand a higher voltage exceeding their recommended rating. BEHLKE offers separate products to operate them at higher voltage/currents.

Solution Proposed: Designing a modular high-voltage (~10 kV) switch using a single custom isolated gate driver for each module and having a construction cost lower than the BEHLKE switch with equivalent or better performance in all specification categories (Specifications for the BEHLKE switches can be found in the following link: http://www.behlke.com/separations/separation_c4.htm).

Relevance to OSPRES Grant Objective: The proposed modular high-voltage switch is expected to facilitate controlled hundreds-of-nanosecond charging of an array of transmission lines of pulse forming networks to drive an array of PCSSs, thereby producing controlled hundreds-of-picosecond scale high-voltage pulses.

Risks, Payoffs, and Challenges:

I. Lack of rigid control over voltage balancing can lead to a cascaded failure among the series-connected MOSFETs.

II. In the absence of an adequate mitigation scheme, voltage overshoot due to the fast switching speed can exceed the voltage rating of an individual MOSFET, thereby damaging the switch.

III. At high voltage (~10 kV) and high repetition rate (>100 kHz), mitigating EMI to safeguard the individual MOSFETs from false turn-ON is a major challenge.

3.1.2 Tasks and Milestones / Timeline / Status

(A) Design a surface-mount MOSFET-based four-stage switch (6.8 kV rated) and control it using the in-house gate driver, then test its voltage-withstanding ability with a DC supply voltage up to 4–5 kV and evaluate the effectiveness of the thermal management at its current state / DEC 2020 / Completed.

(B) Design and develop a modular HV switch (~10 kV rated) using the concept of the tested four-stage high-voltage switch module and an in-house modular gate driver to drive the modular switch /JAN–FEB 2021 / Completed.

(C)

(i) Test the voltage withstanding ability of the modular HV switch with a DC supply voltage up to 10 kV and switching frequency up to 50 kHz using a resistive load (5–10 kΩ) and evaluate the effectiveness of the thermal management at its current state / FEB–JULY 2021 / Ongoing.

(ii) Test the isolation capability and evaluate the synchronization accuracy of the gate drive signal generated from the modular in-house gate driver / FEB–JULY 2021 / Ongoing.

(iii) Encapsulate the gate driver board with potting material with a high (~15–20 kV) breakdown voltage rating to prevent possible flashover/arcing in between the HV switch and this board / MAR–JULY 2021 / Ongoing.

(D) Design and fabricate a compact power conditioner circuit based on a 12 kV rated SiC switch made by BEHLKE (HTS 121-15) / APR–MAY 2021 / Completed.

(E) Test this modular HV switch coupled with a Si PCSS device up to a DC supply voltage of 5–6 kV and a switching frequency of 50 kHz / On hold.

(F)

(i) Design and develop a 20 kV rated modular (two modules, each with four MOSFETs) HV switch based on the design concept of the 10 kV rated modular switch using 3.3 kV rated SiC MOSFETs (new product made by GeneSiC Semi) / On hold.

(ii) Design and develop a 20 kV rated modular gate driver based on a WPT based planar transformer topology to ensure adequate galvanic isolation (~30–40 kV) for the power supplies of the gate driver / On hold.

3.1.3 Progress Made Since Last Report

This sub-project is currently on hold due to a transition in personnel (student graduation and replacement). We expect work to resume in the next 1–2 months.

3.1.4 Summary of Significant Findings and Mission Impact

(A) The 6.8 kV rated four-stage surface-mount MOSFET developed in-house was successfully tested up to a DC supply voltage of 4 kV and at a switching frequency up to 20 kHz with a 3.2 kΩ resistive load.

(B) A modular (two modules) 10 kV rated HV switch has been designed and a prototype has been developed using 1.7 kV rated SMD MOSFETs (C2M1000170J). An in-house 10 kV rated HV gate driver has been designed and incorporated with the HV switch to drive it. A manuscript on the HV switch and the custom isolated gate driver has been submitted in IEEE Transaction on Power Electronics.

(C) The HV switch coupled with the custom HV gate driver has been tested at a supply voltage up to 6.5 kV at a switching frequency up to 15 kHz. We have observed gate driver malfunctioning at around 6.5 kV and have designed a revised modular gate driver with an alternative optical fiber link.

4.0 Switch Evaluation and Innovation

4.1 GaN:C PCSS Direct RF Modulation

(Heather Thompson and Scott Shepard)

4.1.1 Problem Statement, Approach, and Context

Primary Problem: Need for a more compact, cost-effective RF pulse generation system for Navy afloat missions on smaller vessels and vehicles.

Solution Space: Improve efficiency and reduce necessary material, size, and thermal requirements by utilizing gallium nitride (GaN) in PCSSs through exploitation of its theoretical material properties which allow for higher operating voltages, frequencies, and temperatures, while also eliminating the need for pulse-shaping transmission lines through direct RF modulation using the laser/photon source driving the PCSS.

Sub-Problem: Lack of maturity in compensated gallium nitride semiconductor (i.e., GaN:X with X=C,Fe) PCSS manufacturing, development, and optimization.

State-of-the-Art (SOTA): Si-based PCSS with >10 kV operational voltage, cooling system capacity of 500 W/cm^2, and theoretical breakdown of 1.3 MW/cm.

Deficiency in the SOTA: Si-based technologies requiring ~100 µJ optical pulses per 4 MW of RF output power, increasing the laser energy (per pulse) required for device triggering; long recovery time (ones-of-µs), limiting quick opening and high pulse-repetition-rate operation along with increased heating in the PCSS; critical electric field of 0.3 MV/cm, leading to devices that are ones-of-cm^2 in area for the target peak power; and operating temperature of <160°C, leading to increased cooling requirements.

Solution Proposed: Replace Si-PCSS device with GaN:C utilizing direct RF modulation — eliminating the need for a bulky pulse-forming transmission line (~3 ft long) — capable of handling >3 MW (peak power) with ~20 µJ of incident optical energy, device area <1 cm^2, and operating temperature ~500°C (theoretical temperature which will be limited by circuit components and solder).

Relevance to OSPRES Grant Objective: Reduction in size and cost for cooling system that prevents damage to the PCSS device and components along with eliminating need for a bulky pulse-shaping system, as well as decrease in material cost and needed incident laser energy, leading to enhanced SWaP-C^2 capability with greater modularity and scalability.

Risks, Payoffs, and Challenges: Due to manufacturing limitations, GaN PCSS devices tend to be limited to lateral geometries (both contacts on the top side of the device), limiting operating voltage due to current crowding and surface flashover. The recovery time (ones-to-tens-of-ns) may lead to device heating and increased DC, or zero-frequency, component when generating RF with a period on the same order as the recovery time.

4.1.2 Tasks and Milestones / Timeline / Status

(A) **Start Jan 2021** Demonstrate RF unipolar modulation in the 1–2 GHz regime and up to 2 kV operating voltage with current PCB setup and automated optical delay system. Achieving 2 kV operating voltage should allow for preliminary effects testing before (or in conjunction with) striving towards higher operating voltages. **On hold**

(B) **Start June 2021** Demonstrate RF bipolar modulation using an advanced test setup with two GaN:C PCSSs triggered using the same optical delay, but with the second device connected to a negative power supply. **On hold**

(C) **Start June 2021** Achieve higher center frequency content in unipolar and bipolar modulation by using a faster (rise-time and pulse-width) laser to activate GaN:C PCSS. **On hold**

(D) **Start May 2021** Complete study of recovery for differing gap lengths, incident energies, and operating voltages and find solutions to reduce the recovery time. **On hold**

4.1.3 Progress Made Since Last Report

Section 4.1 is being put on hold until a study on minimizing/optimizing the on-state resistance of GaN:X PCSSs using a combination of experimental results and simulation results from COMSOL Multiphysics and TCAD (see Section 4.8). Once completed, focus will return to Section 4.1 and demonstration of both unipolar and bipolar direct modulation at up to 2kV charge voltage and 1-2 GHz frequency regime.

4.1.4 Technical Results

4.1.5 Summary of Significant Findings and Mission Impact

(A) Towards showing direct RF modulation in the 1–2 GHz range, unipolar modulation has been demonstrated using an open-space time-optical delay using one GaN:C PCSS (lateral device with 500 μm gap length) of up to 1.2 kV charge voltage. The limiting factor to achieving higher charge voltage was flashover occurring in air-bubbles formed during curing of the Sylgard encapsulant. Previously, ~1.8 kV charge voltage was achieved using a 1 μm gap length GaN:C PCSS, so demonstration will continue using similar methods (corona-dope) to the Si-PCSS studies to achieve 2 kV+ charge voltage, with this being limited by the power supply being used to 2.5 kV.

(B) Demonstration of direct RF generation began with low-voltage (50 V charge voltage) testing to determine the feasibility of the bipolar setup and modulation. A bipolar pulse was achieved, but with high on-state resistance due to limitations in the available laser energy when using the neoLASE system. After conversion from 1064 nm to 355 nm, 6 μJ of energy was available to split into two beams for free-space optical delay. Future testing will commence using the laser sent to UMKC from BAE once that is setup.

(E) To continue towards a feasibility test of fiber coupling with GaN:C PCSS, single-mode waveguide modeling was initiated in COMSOL. This initial model will be modified to show optical fiber coupling to GaN:C PCSS.

4.2 Drift-Step Recovery Diode and Pulse Shaping Device Optimization

(Jay Eifler)

4.2.1 Problem Statement, Approach, and Context

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS but do not require a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times requires optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening device within the pulse shaping head circuit. Additional goals for pulse repetition frequency are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies. Also optimize the pulse sharpening device (PSD) within the pulse shaping head circuit.

Sub-Problem 1: TCAD and SPICE models of the DSRD are 40% accurate and must be improved. PSD models have not been developed.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetimes have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current. PSD have sharpened DSRD pulses to 100 ps-order.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power and minimum risetime, but also for low-jitter, reduced cooling, and compactness. Additionally, optimize pulser with PSD and pulse shaping head circuit.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2 cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities. DSRD and

PSD must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD and PSD modeling.

4.2.2 Tasks and Milestones / Timeline / Status

(A) Milestone – TCAD and SPICE models of the DSRD and MOSFET, respectively, developed which match experimental values of both the diode and circuit within 5% accuracy [*Estimated completion by AUG21*].

1. Task – Develop baseline DSRD model in TCAD [*completed JAN–APR21*];
2. Task – Develop SPICE model of DSRD within LTSPICE [*Estimated completion AUG-SEP 2021*];
3. Task – Develop SPICE model of MOSFET within Silvaco [*JUL–SEP21*];
4. Task – Compare results of models developed in TCAD to the simulation values achieved using LTspice and experimentally (see Section 4.5) [*JUL–SEP21*];
5. Task – Incorporate parasitic capacitance, inductance, and resistance models for both single die and DSRD diode stacks (multiple dies in series) as well as for the DSRD-based pulser circuits [*discontinued after MAR–JUN21*];

(B) Milestone – Optimal characteristics of epitaxially-grown DSRD pinpointed from parametric study which produce the maximum waveform fidelity characteristics (e.g., maximum peak voltage, shortest risetime, highest dV/dt) [*Estimated completion by AUG21*].

1. Task – Determine carrier lifetime effect on risetime [*completed FEB–APR21*];
2. Task – Determine effect of including avalanche modeling on DSRD performance [*completed FEB–MAY21*];
3. Task – Determine effect of the width of outer edge contact on current density and breakdown in device [*discontinued after MAR–MAY21*];
4. Task – Model TCAD process in Silvaco Athena and Victory Process for DSRD diffused and epitaxial processes (and pulse sharpening devices) used for DSRD fabrication and DSRD device modeling [*discontinued after MAR–JUN21*];
5. Task – Determine optimal doping profile for Semiconductor Power Technologies (SPT) DSRD epitaxial designs [*completed MAY–JUL21*];
6. Task – Determine best doping profile from fabricated and optimal conceptual designs by comparing performance in the 2x2 DSRD pulser [***completed JUL21***];
7. Task – Complete DSRD performance study on epitaxial doping profile (n-side) variation manufactured by SPT in conjunction with LSRL [***completed JUL21***];
8. Task – Complete gain study for DSRD stack height and gain staging design [***completed JUL21***];

9. Task – Verify accuracy of TCAD simulations by comparing to experiment for DSRD-based pulser circuit topologies [*JUL–AUG21*];

(C) Milestone – Pulse sharpening devices developed within TCAD which improve the risetime and peak voltage of the IES pulse generator developed in Section 4.5 [***transitioned to Section 4.7 JUL21***].

1. Task – Develop preliminary pulse sharpening devices (PSD) models within TCAD [*discontinued after DEC20*];
2. Task – Develop standard PSD models within TCAD to reproduce results from published work [*discontinued APR–JUN20*];
3. Task – PSD simulated with DSRD 3-stack for more complete DSRD-based system modeling excluding only the primary switch model [*APR–JUN20*];
4. Task – Determine current carrying capacity of PSD and DSRD stacks [*discontinued MAR–JUN21*];

4.2.3 Progress Made Since Last Report

(A.2) A DSRD SPICE model within LTSPICE has been developed and greatly improves upon our earlier LTSPICE DSRD model using the standard Berkeley 'level 1' diode model. The new DSRD model has been compared and calibrated to experiment through standard diode tests (forward and reverse I-V, forward and reverse C-V and reverse recovery) and single-bar pulser tests.

(A.3) A MOSFET SPICE model usable in TCAD has been developed. The tuning of the parameters has now been further refined to fit the datasheet. An exacting comparison with experiment has yet to be performed, but comparison to 2x2 DSRD pulser with TCAD has shown the same optimal 340 ns trigger duration. The advantage of the TCAD simulation is the DSRD model is a TCAD model capable of predicting breakdown effects (as well as possible other yet unidentified effects) which have not been included or tested in a SPICE-style DSRD model. It is more difficult to match the SiC MOSFET model, as a TCAD model, to experiments due to no known accurate SiC TCAD MOSFET models having been reported in the literature. As well, the integrated circuit fabrication methods used to produce SiC MOSFETS do not have a clear relationship to the half- and full-cell models used in TCAD to simulate MOSFETS. SPICE models can be more easily fit to experimental data and reduce computational costs of simulation.

In short, the SPICE models provide the ability to predict experiment when well-tuned and allow device and circuit topology design and optimization for meeting peak power and risetime requirements of the pulser system, as well as, addressing SWAPC^2 cooling requirements. The simulations within TCAD and SPICE are based on the device model development and testing for DSRD-based pulser circuit topologies and are central to device and pulser development connecting the various DSRD efforts (Section 4.2-4.7 of grant report) as shown in Figure 4.2.19.

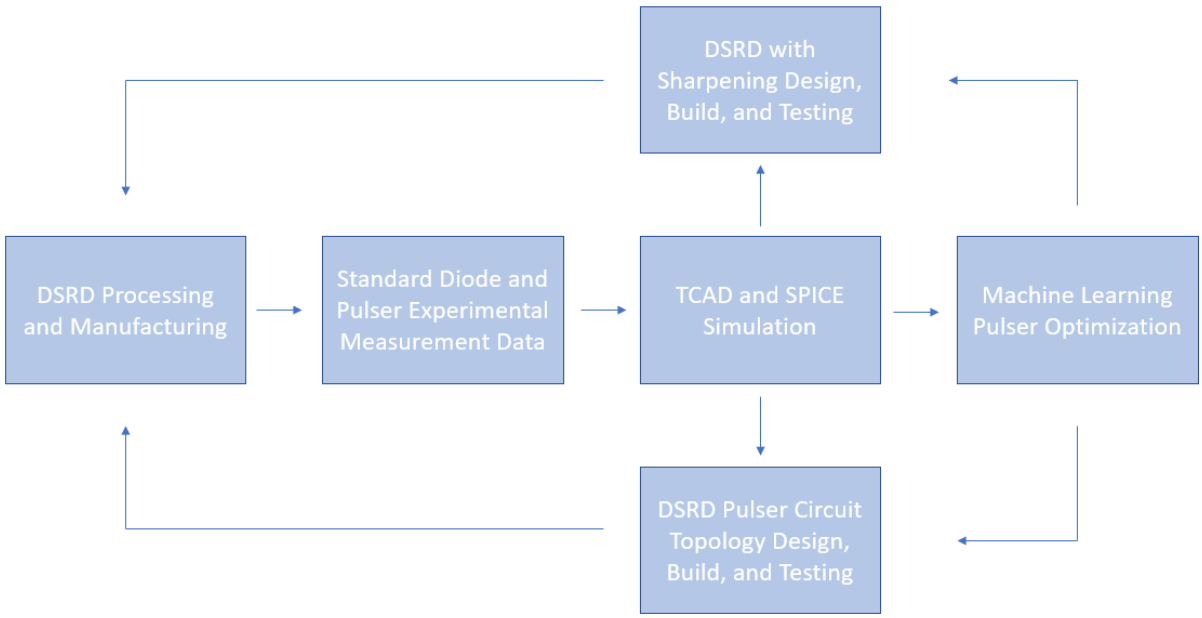


Figure 4.2.19. Flowchart of overall DSRD effort and how TCAD and SPICE simulation connect to various DSRD efforts.

(A.4) TCAD simulation and experiment have been compared for the 2x2 DSRD pulser with some discrepancy due to DSRD stacks usable in simulation. The main result is TCAD successfully predicts the optimal trigger duration. LTSPICE simulation with a new LTSPICE DSRD model has been compared to TCAD and experiment for the single bar DSRD pulser. Deficiencies exists in the experiment (unusually long risetimes inconsistent with earlier experiments of DSRDs), TCAD (SPICE MOSFET model not well calibrated between datasheet and pulser experiments), and LTSPICE (not yet fully calibrated to correct experiments) and require further improvement. Overall, the new LTSPICE DSRD model is greatly improved over the old version.

4.2.4 Technical Results

(A.2) A new DSRD LTSPICE model has been developed based on the approach of the old, original model. The old model used the standard Berkeley ‘level 1’ diode model widely used (as opposed to [1]). The old model input parameters were largely default parameters with a few measured parameters averaged over the individual diode measurements for a general DSRD model. The measured parameters were: IS or saturation current (a static, legacy value), CJO or zero-bias capacitance, RS or series resistance, VJ or junction voltage, BV or breakdown voltage, and TT or transit time. The default parameters were: N or emission coefficient, M or capacitance grading coefficient, and FC or forward-bias capacitance coefficient. The new model makes use of the same diode model and parameters. The old model additionally used a single diode to represent various stack heights with a new model for each stack height. This approach was initially followed in an attempt to improve the old model. However, forward I-V and reverse C-V

were difficult to match well through fitting. A new approach was adopted using the same number of diodes in the model as in the DSRD stack, for example, a 7-stack DSRD used 7 individual diode models connected in series. This proved to make matching the forward I-V and reverse C-V much easier even using mostly default model parameters.

One difference that should be made between the TCAD and LTSPICE DSRD models is that the TCAD model includes breakdown effects whereas the LTSPICE DSRD model does not. How to include breakdown or impact ionization effects is still being explored and do exist in some diode models but is not yet clear if this is possible in LTSPICE. The implication of not including breakdown is that limits to achievable peak voltage and risetime have to be made from experiment and/or TCAD until such an effect can be included into SPICE. Another limitation of having no breakdown effects is IMPATT-style oscillations of the DSRD cannot be simulated in LTSPICE currently.

The forward I-V using the LTSPICE DSRD single diode model is compared to TCAD and experiment in Figure 4.2.1 in semi-log plot. The old model (gray) has a much higher conductivity than the other results. The TCAD result (light blue) could be adjusted with an additional series resistance best determined from experimental measurement (not yet done). In the figure, there are a couple of experimental results for diode (d) 363 (new measurements) and d890 (older measurements). The older measurements were over a lesser range of current and voltage. It should be noted that higher voltage forward I-V experimental measurements of the DSRD are in progress and should fully turn-on the DSRD to achieve lower on-state resistance (or forward voltage drop) and currents within the ampere range. Using the three-point parameter extraction method [2], RS, IS and N were extracted from the d363 result and modeled in LTSPICE (orange) with the curve showing the differences. An additional method employing the forward knee current parameter (IKF), which is an extension of the standard model commonly available, was used to more closely match experiment (light green). Also, another method using additional modeling diodes [3] was employed to more closely match the forward I-V to experiment (dark green). These methods proved to be capable of matching the forward I-V closely but were not necessary when using the 7-diode DSRD model.

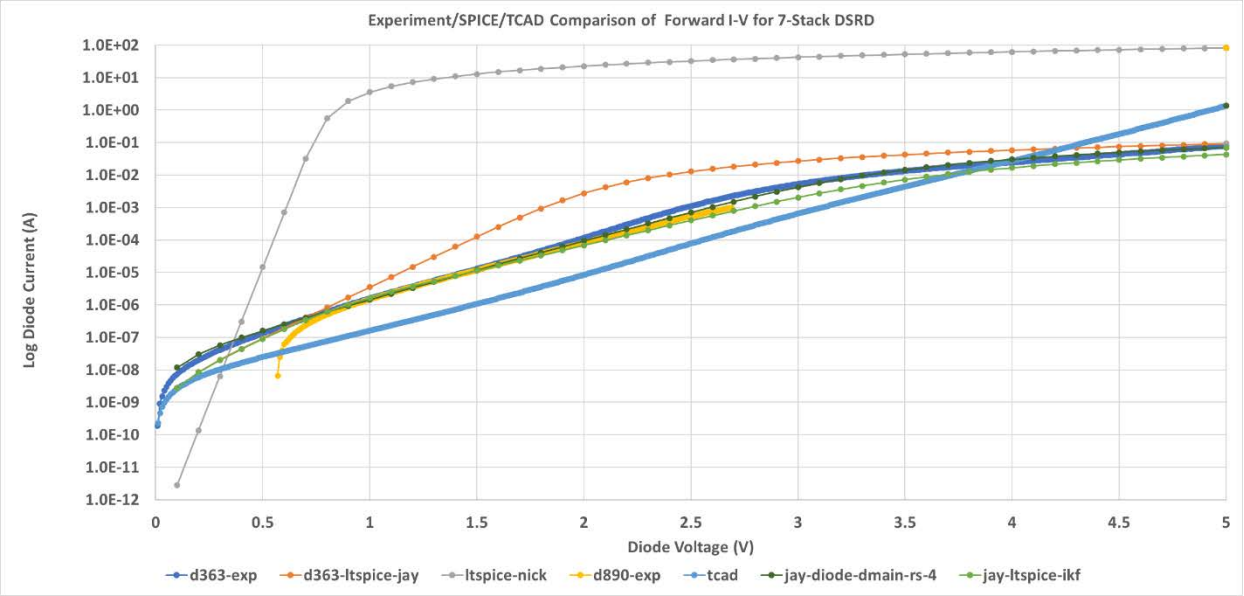


Figure 4.2.1. Semi-log plot of forward I-V comparing experimental measurements, TCAD and various LTSPICE DSRD models for lower current and voltages.

The forward I-V comparing the new 7-diode DSRD LTSPICE model with other LTSPICE DSRD models and newer experiments is shown in Figure 4.2.2 on non-semi-log plot. One interesting experimental result is that there are two groups (with several diodes per group) of forward I-V pointing to some aspect of the device history and/or fabrication (to be later analyzed with larger dataset-Section 4.4). The 7-diode model falls between or within the two experimental groups using only default parameters except the 10 mΩ RS (RS derived from TCAD simulation from pulser operation during forward DSRD pumping). Ultimately, all relevant parameters must be adjusted and the forward I-V should be very closely fit for both semi-log and non-semi-log plots. The forward I-V results will be consistent with the DSRD operation with forward (and high conductivity reverse) current and voltages since the SPICE models use the DC equations along with capacitances to model transient, large-signal operation. It should be noted the IKF and multiple diode modeling results also fall within the experimental results, but the 7-diode DSRD model is more easily very closely fit.

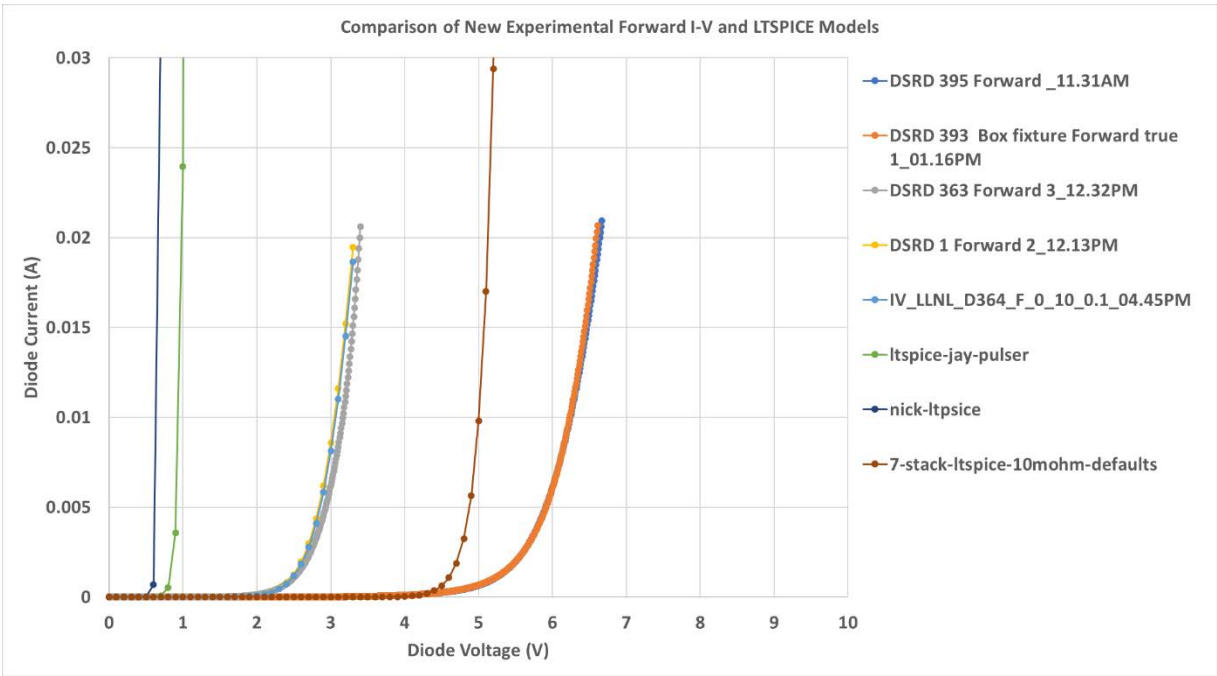


Figure 4.2.2. Non-semi-log forward I-V comparing 7-diode DSRD model, 1-diode DSRD models and experiment. The 7-diode model falls within the experiment.

Reverse I-V is compared between TCAD, LTSPICE and experiment in Figure 4.2.3. In this case, the LTSPICE model (yellow) proves the most inaccurate due to IS being extracted from the forward I-V (or using default values) and having to account for the reverse current. No breakdown is shown in the figure. A couple of experimental results are shown that indicate the wide variance often seen in semiconductor devices for the leakage current (for example our own Si-PCSS devices showed such wide variance experimentally). The TCAD results show two methods (DC and transient) to determine the reverse I-V. The DC (gray) method fails to converge past ~18 V. The transient TCAD method result is lower in current at higher voltages which may be due to a differing amount of impact ionization, the effects of which start much earlier than actual breakdown (exponential-like rise of current). The wide variance in reverse current is often attributed to the process and fabrication of the device and is used to cull bad devices with the effect being caused by doping non-uniformity, defects and interface defects/states or other factors of manufacturing. It is not yet known how much the exactness of the reverse I-V affects device simulation accuracy. The forward C-V is also more difficult to fit properly to experiment.

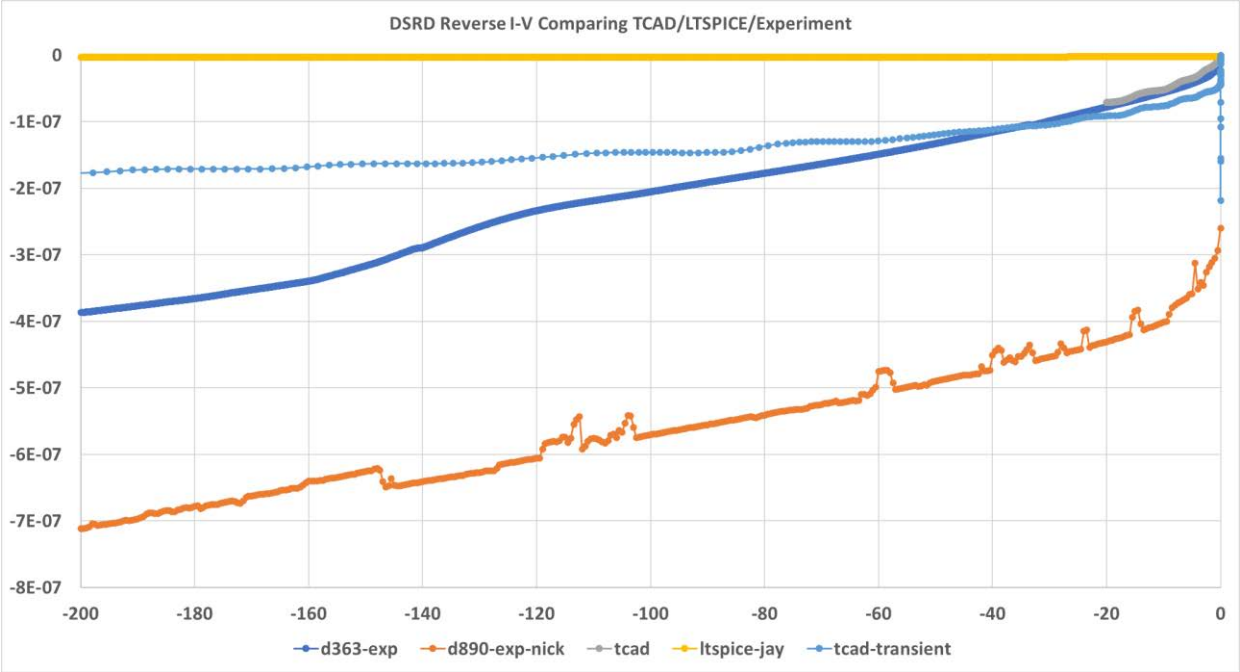


Figure 4.2.3. Reverse I-V comparison for TCAD, LTSPICE, and experiment. A DC (gray) and transient (light blue) method of convergence is used in TCAD. The experimental results show the typical wide variance in reverse I-V.

Next the forward and reverse C-V curves have been compared between LTSPICE, TCAD and experiment in Figure 4.2.4. Results are shown for TCAD, both 1- and 7-diode LTSPICE models and experiment (and divided into positive and negative sides, note backwards values due to reverse current being positive here). The reverse C-V for diode 363 (green) is close to the 7-diode LTSPICE DSRD model (yellow) which has been adjusted using CJO and M but using single diode parameters in a 7 diode model (7-diode CJO is 7 times the CJO of the 1-diode model). The reverse C-V for the 1-diode LTSPICE model (medium blue) is seen to be different than the experiment. The reverse C-V from TCAD has a CJO or zero-bias capacitance that is 1/3 of the experiment and is still under investigation to correct. The forward C-V (as with reverse I-V) is generally more problematic to match. Likely, all the results including experiment are in error for the forward C-V. The LTSPICE forward C-V have not included correct modeling for higher voltage but possibly can be corrected using the earlier multiple diode technique. The experimental forward C-V is very crude in part due to controversy over the Cp-Rp model used to determine capacitance from the real and imaginary components of impedance [4]. The forward C-V is important for switching characteristics of high-power devices such as the DSRD and is being investigated.

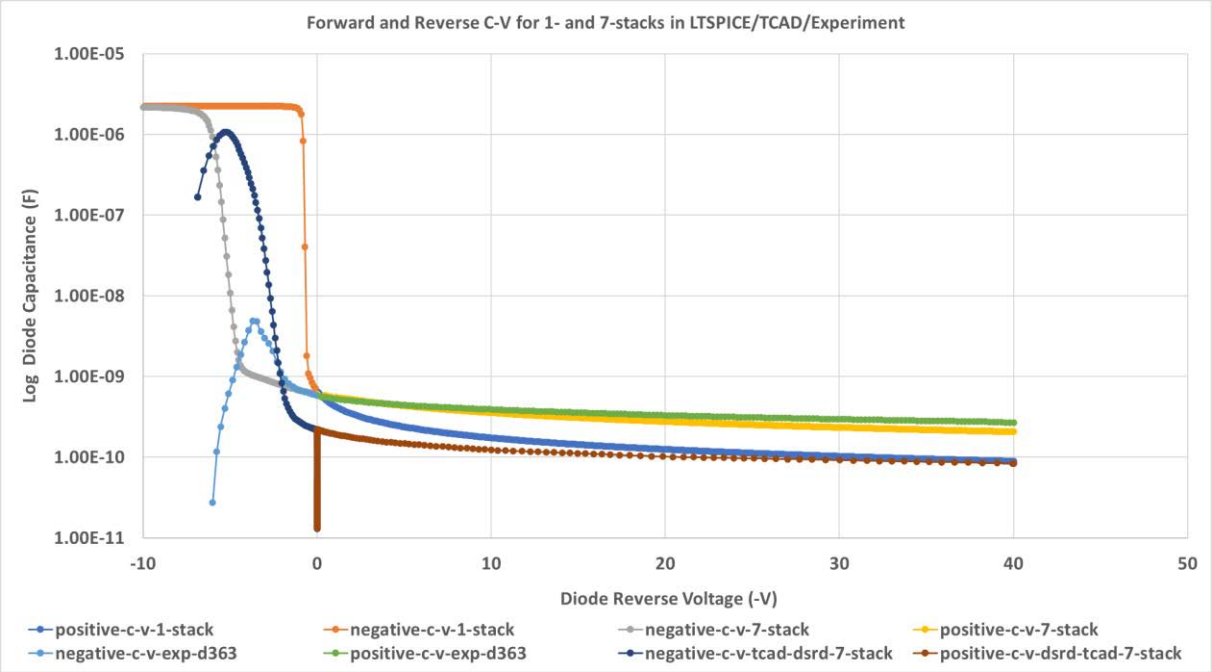


Figure 4.2.4. Forward and reverse C-V comparison for LTSPICE, TCAD and experiment. The 7-diode model is close to the experiment. The forward C-V, including experiment, are all likely inaccurate.

Last, the reverse recovery is compared between LTSPICE, TCAD and experiment in Figure 4.2.5. The LTPICE model shown is for the 1-diode model but the 7-diode model is nearly the same. The LTSPICE model uses the transit time to model reverse recovery effects and mostly adjusts the charge-storage (relative flat reverse current) time. An additional parameter available in LTSPICE XVII is used to adjust the transition time to recovery or zero current. This parameter is called the minority carrier charge viscosity or Vp [5] and is a soft recovery parameter adjusted here to only slightly lengthen the transition time. Overall the fit is close. A forward recovery peak can be seen around 6 µs but the experimental bump is smaller and not visible. The differences between experiment and simulation in the forward current (between 2-4 µs) have not yet been understood.

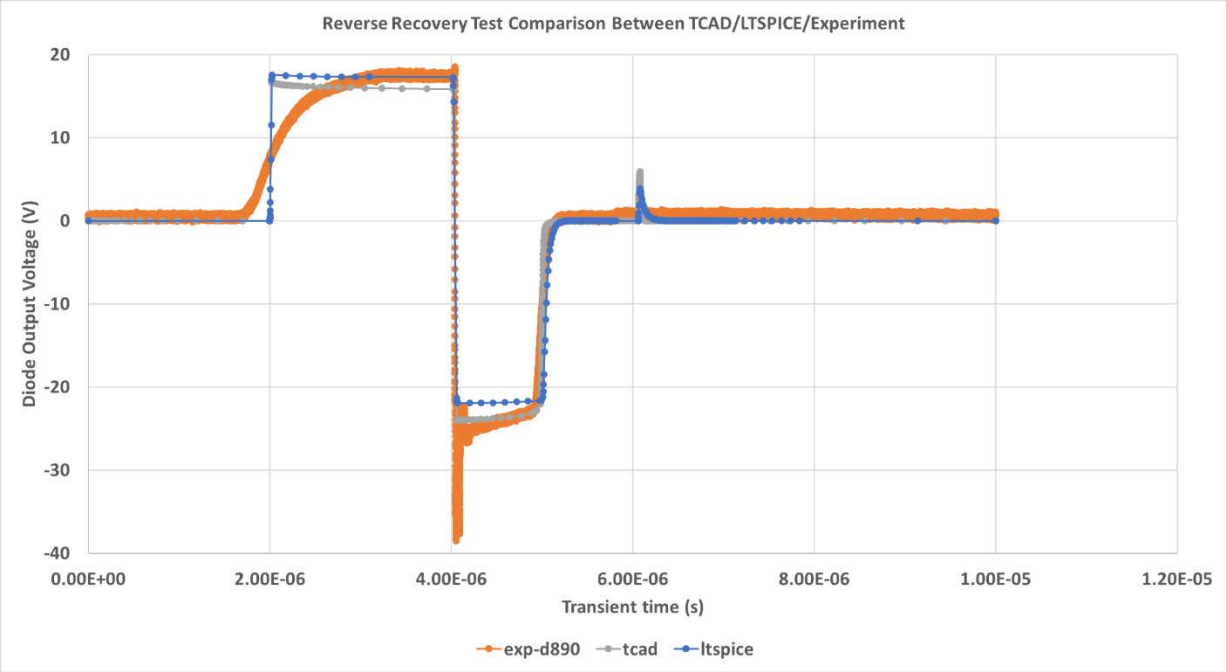


Figure 4.2.5. Reverse recovery comparison between LTSPICE, TCAD and experiment. Overall, the match is close.

The DSRD models have been characterized using the standard diode tests of forward and reverse I-V, forward and reverse C-V, and reverse recovery. The reverse I-V and forward C-V are more problematic to match, but the forward I-V and reverse C-V have been matched well (TCAD still has a zero-bias capacitance discrepancy that should be correctable). The use of these models and comparison to experiment for the pulser tests is done under task (A.4). Closer adjustments of the LTSPICE and TCAD models and more extensive experimental testing are in progress.

(A.3) The TCAD SPICE MOSFET model was improved to more closely match the datasheet than in the July 2021 grant report. One aspect was to improve the current saturation in the TCAD SPICE MOSFET model which occurs at a higher drain-source voltage in the LTSPICE Cree MOSFET model but is not shown in the Cree datasheet. This saturation point is one factor altering the peak load voltage seen in experiment vs simulation, since the MOSFET current controls the forward pumping current of the DSRD which affects the maximum reverse DSRD current mostly responsible for the peak load voltage (along with the DSRD breakdown and circuit component values). Otherwise, the MOSFET output characteristic, transfer curve, bodydiode characteristic and MOSFET capacitances were more closely matched to the LTSPICE Cree MOSFET model.

Two additional versions of the TCAD MOSFET SPICE model beyond the version 1 of last month were developed. Version 2 only included alterations to the output characteristic representative of the LTSPICE Cree model's saturation current and the transfer curve that resulted. Version 3 includes improved bodydiode characteristic and MOSFET capacitances when compared to LTSPICE Cree model. In Figures 4.2.15 and 4.2.16 are

shown the output characteristics and transfer curves, respectively, for version 2 between Cree datasheet and SPICE and TCAD models. The version 2 model uses the bodydiode and capacitances of last month's version 1 (see July 2021 Grant Report). The purpose of this model was to test having a higher saturation current at higher drain-source voltages as seen in pulser simulations when higher trigger durations and prime voltages are used and for matching the peak load voltages seen in experiment . The datasheet (light blue) only extends to ~12V. The Cree LTSPICE model (yellow) extends to much higher currents and voltages and saturates only at higher drain-source voltages. To note, SiC MOSFETs are well known not to operate in saturation as opposed to other kinds of MOSFETs except at sufficiently high drain-source voltages. Also shown is the effect of increasing the MOSFET width (or transconductance) to better fit the LTSPICE Cree model curve. To note, the saturation occurring well beyond the ~12 V datasheet value is obtained in the TCAD SPICE MOSFET model by increasing the channel-length modulation parameter (λ) to a value of 0.1642 which is much higher than often seen but still within values seen in diode models and extractable from datasheets. The trick is that λ is usually employed in the saturation region whereas I use it here for non-saturation region to fit the LTSPICE Cree model.

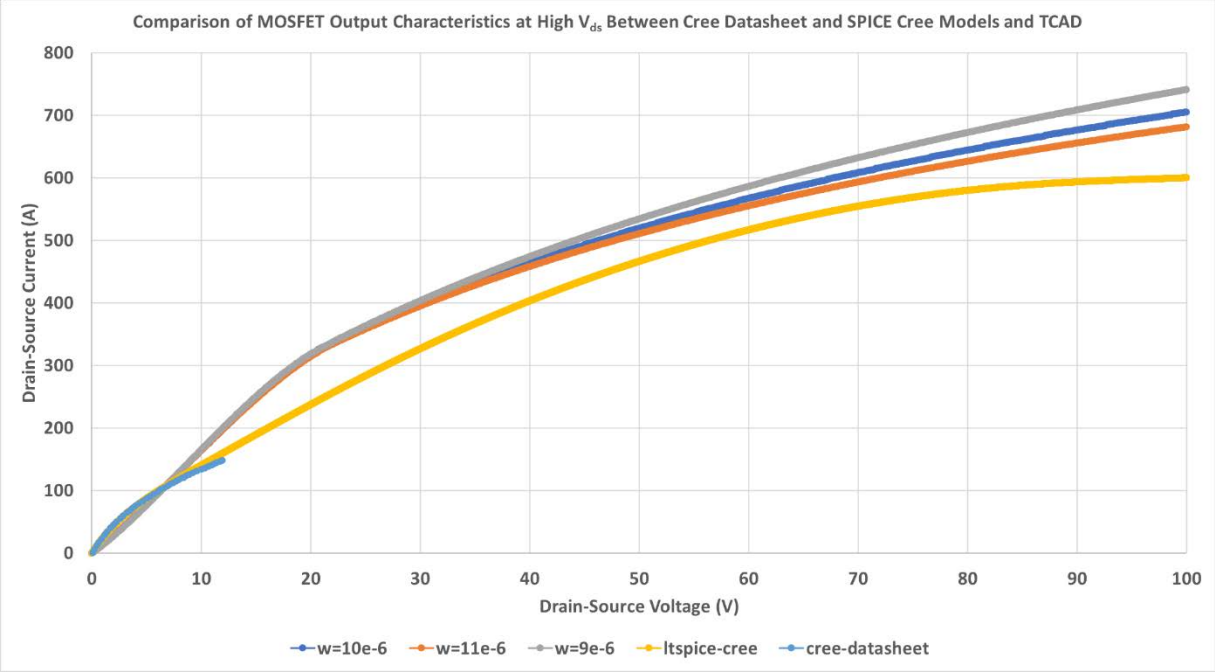


Figure 3.2.15. MOSFET output characteristic comparison between Cree datasheet and LTSPICE model and TCAD using the TCAD SPICE MOSFET model. The models only saturate at high drain-source voltages.

The transfer curves compare better between the datasheet and the TCAD SPICE MOSFET model for various widths or transconductance used than to the LTSPICE Cree model. The transfer curve was not adjusted since the effects of the output characteristic

on the MOSFET current levels was more important but can be fit more closely with enough iterations. One can see the decrease in current for the datasheet (gray) at higher gate-source voltages modeled in the LTSPICE Cree model with discontinuities in the transfer curve. How to adjust the transfer curve to show this decrease is being explored.

Figure 4.2.16. MOSFET transfer curves compared between Cree datasheet and LTSPICE model and TCAD MOSFET SPICE model with various widths or transconductances.

The bodydiode model is now fit better in version 3 of the TCAD SPICE MOSFET model as shown in Figure 4.2.17. Note, version 3 uses the version 2 output characteristic and transfer curves. No breakdown is seen in the curve and breakdown is not modeled in any of these models (but were previously in a strictly TCAD MOSFET model). The Cree LTSPICE model and the TCAD SPICE MOSFET model are fit as nearly as well as possible since the diode model within the TCAD SPICE MOSFET model cannot be turned off and is a relatively simple diode model. More options may be available.

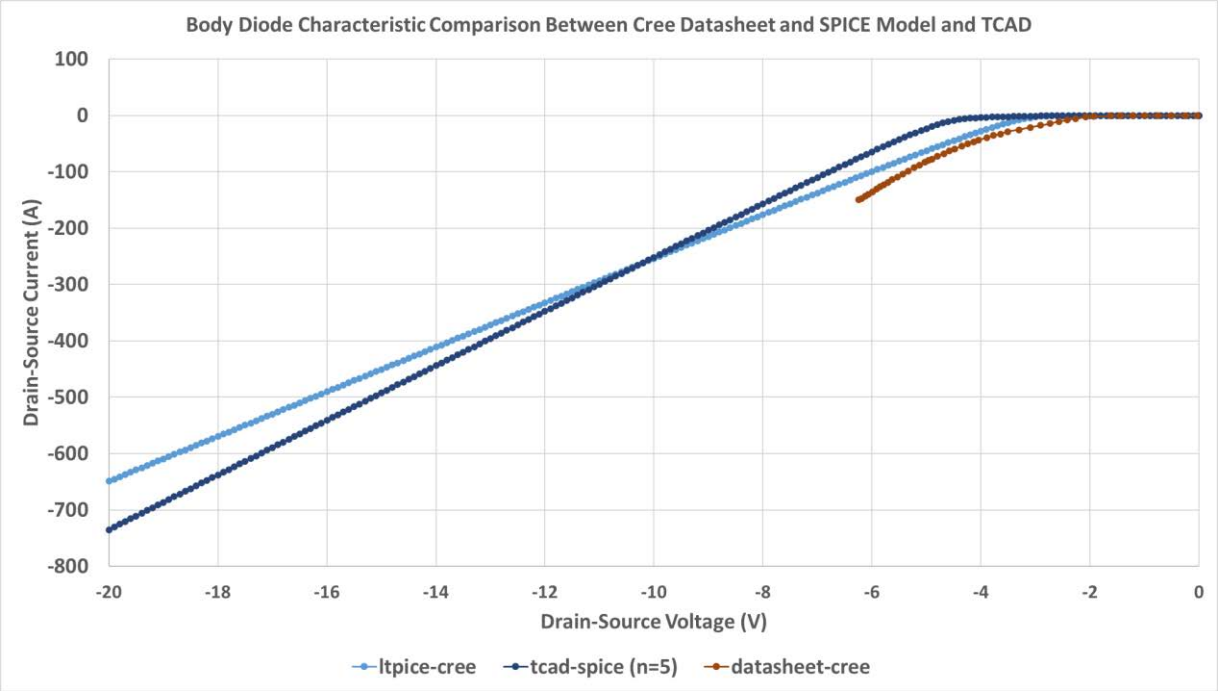


Figure 4.2.17. Bodydiode characteristic compared between Cree datasheet and LTSPICE model and TCAD SPICE MOSFET model.

The MOSFET capacitances are compared between the Cree datasheet and LTSPICE model and the version 3 TCAD SPICE MOSFET model in Figure 4.2.18. Overall, the fit is very close except for the elbow and minimum value of the reverse transfer capacitance (C_{rss}) and can be likely further matched.

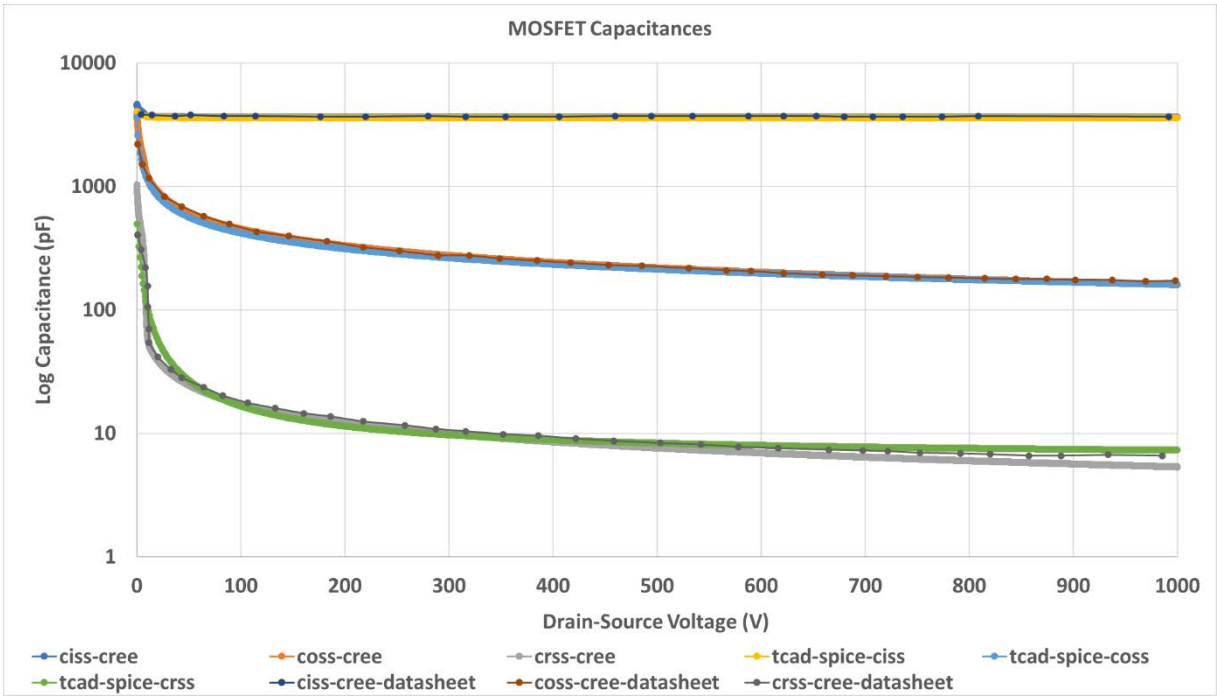


Figure 4.2.18. MOSFET capacitances compared between Cree datasheet and LTSPICE model and version 3 TCAD SPICE MOSFET model.

The gate charge has also been modeled but due to an unclear description in the datasheet (not uncommon) of the gate charge measurements is not shown. The Cree LTSPICE model and TCAD SPICE MOSFET model compare well but neither match the datasheet due to the differences in test circuit and conditions but can be improved as more tests are studied. As in last month's July grant report, the switching characteristics are even more problematic to match with datasheet due to poor testing descriptions and is likewise reported in [6].

The operation of the TCAD SPICE MOSFET model has required an adjustment after the above fitting to the Cree LTSPICE model to match pulser experiments (see task (A.4) below for results) by again adjusting the device width or transconductance which is the usual method to adjust MOSFET current in these models to experiment. However, the width adjustment is large and the above fitting must be recalibrated for a good overall match between pulser performance and Cree LTSPICE model and datasheet. One factor complicating the match is the DSRD stack heights used in the experiments differ than used in the TCAD modeling. Better matching experiments will be compared to in the future. Another future comparison can also be made into the MOSFET operation between the manufacturer model and the TCAD SPICE MOSFET model now that a DSRD LTSPICE of some accuracy has been developed, along with the operation of the gate driver in LTSPICE. With exacting enough experimental measurements and device models, very close fits can be achieved but with the available measurements and LTSPICE models, especially, some limit may be approached to the modeling accuracy of

the DSRD pulser systems. Future reports will report more quantitative and provide tabulated comparisons.

(A.4) Comparisons are made between LTSPICE, TCAD and experiment for single bar and 2x2 pulser systems. The MOSFET model in LTSPICE is the manufacturer's and uses an LTSPICE gate driver model as well. The DSRD model is the new LTSPICE model developed in task (A.2). For the TCAD modeling, the MOSFET model used is from task (A.3) and is a SPICE model. No gate driver model is used or available for the core-Smartspice integrated into TCAD. The DSRD model is a TCAD model within the TCAD simulations. Both trigger duration and prime voltage are varied in the pulser tests for the single bar and 2x2 for a convincing and comprehensive dataset for simulation and experimental comparison.

First, the 2x2 DSRD pulser experiments are compared to TCAD results for both the version 1 (current saturates at low levels of drain-source voltage) and version 2 (current saturates at higher levels) SPICE MOSFET models. The TCAD simulations are limited in the number of nodes available to model multiple DSRD of various stack heights. The largest TCAD simulation yet performed is for 7-stack first-stage DSRDs and a 26-stack second-stage DSRD and uses close to the maximum available mesh points or nodes (re-meshing may allow for first-stage 13-stack DSRDs and a 26-stack second-stage DSRD). In these comparisons, the TCAD uses 7-stack first-stage DSRD and a 13-stack second-stage DSRD which is different from the experiment which uses 13-stack first-stage DSRDs and a 26-stack second-stage DSRD (can but has yet to be modeled within LTSPICE for comparison).

Peak voltage and risetime are compared for TCAD and experiment in Figure 4.2.6. The version 2 model with high-level saturation is seen to improve over the version 1 model slightly (high-level saturation is consistent with the LTSPICE manufacturer model from CREE but is not included in the CREE datasheet). The main deficiency of the modeling is that the optimum prime voltage is different (180 V for experiment, 160 V for TCAD) and the boundaries of the peak voltage and risetime are also different. Otherwise, the TCAD models have some accuracy, especially considering that the stack heights of the DSRDs are different (has been accomplished by adjusting the TCAD SPICE MOSFET model device width or transconductivity, as is usually done to adjust the MOSFET current). It is desirable that the TCAD SPICE MOSFET model and TCAD DSRD model fit closely to datasheet and standard diode experimental measurements (respectively) as possible while predicting the optimum prime voltage (or trigger duration) and boundary limits. Currently none of the device models other than the TCAD DSRD model include breakdown effects (no breakdown effects in the output load pulses observed in the TCAD modeling currently under discussion).

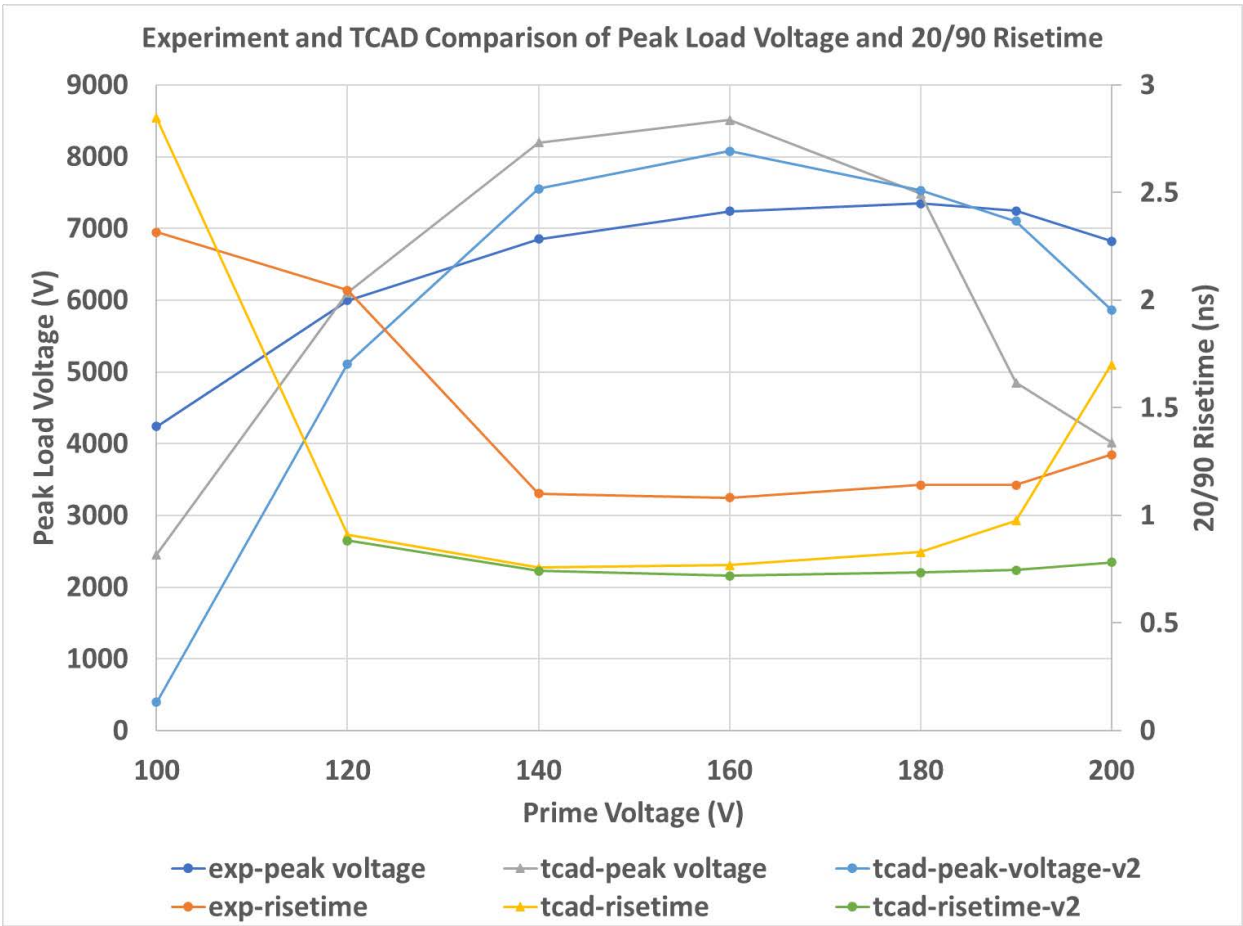


Figure 4.2.6. DSRD 2x2 pulser comparison of TCAD and experiment for peak voltage and risetime. The TCAD and experiment use different stack heights of the DSRDs in the first and second stages.

TCAD and experiment were also compared for the 2x2 DSRD pulser for varied trigger duration in Figure 4.2.7. The match does not appear very good due to the differences in the high prime voltage boundary between experiment and TCAD seen in Figure 4.2.6 earlier (likely due in part to differences in actual DSRD stack heights). For this reason, a trigger duration sweep was done at 160 V prime voltage even though the experimental data consisted of one data point.

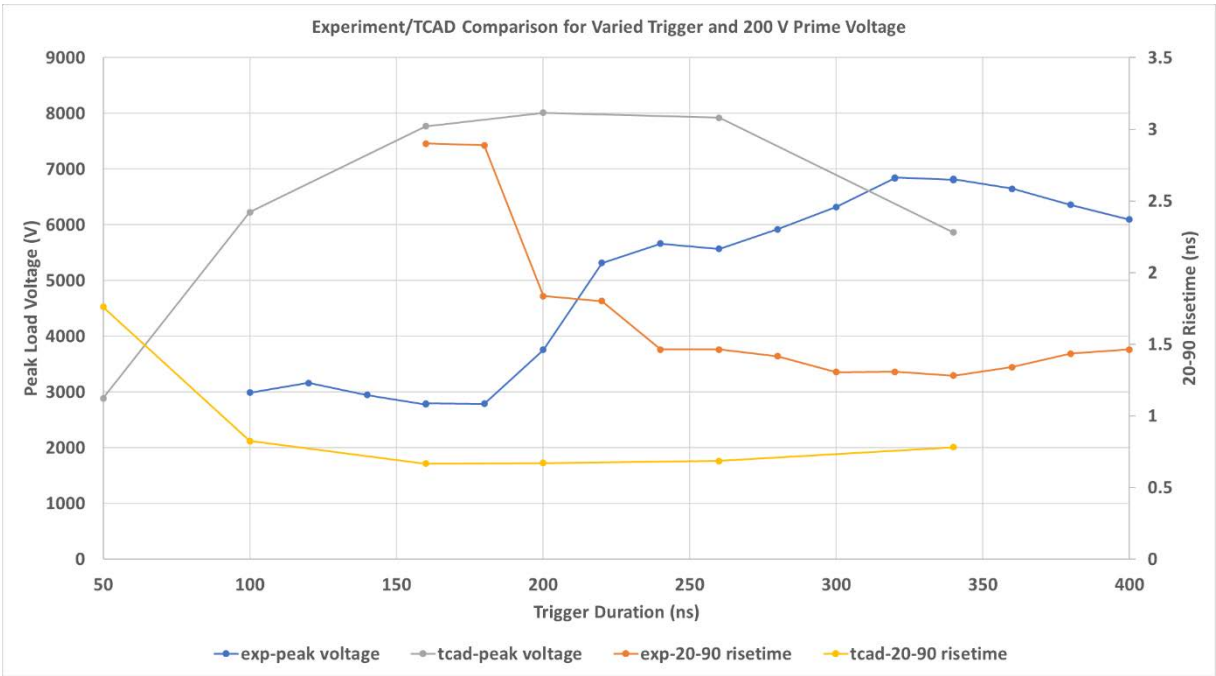


Figure 4.2.7. TCAD and experiment comparison for varied trigger duration in the 2x2 DSRD pulser. The match is not good due to mismatch at 200 V prime voltage between experiment and TCAD and is mostly likely due to mismatched DSRD stack heights used.

The TCAD and experiment comparison for varied trigger duration at 160 V prime voltage for the 2x2 DSRD pulser is shown in Figure 4.2.8. There is only one data point for the experiment for reference of the peak voltage and risetime. The TCAD model correctly predicts the 340 ns optimal trigger duration (based on peak voltage) now that the prime voltage in the TCAD model has not reached the boundary for rapidly decreasing peak voltage. This is considering both the mismatch of DSRD stack heights and difference in prime voltage.

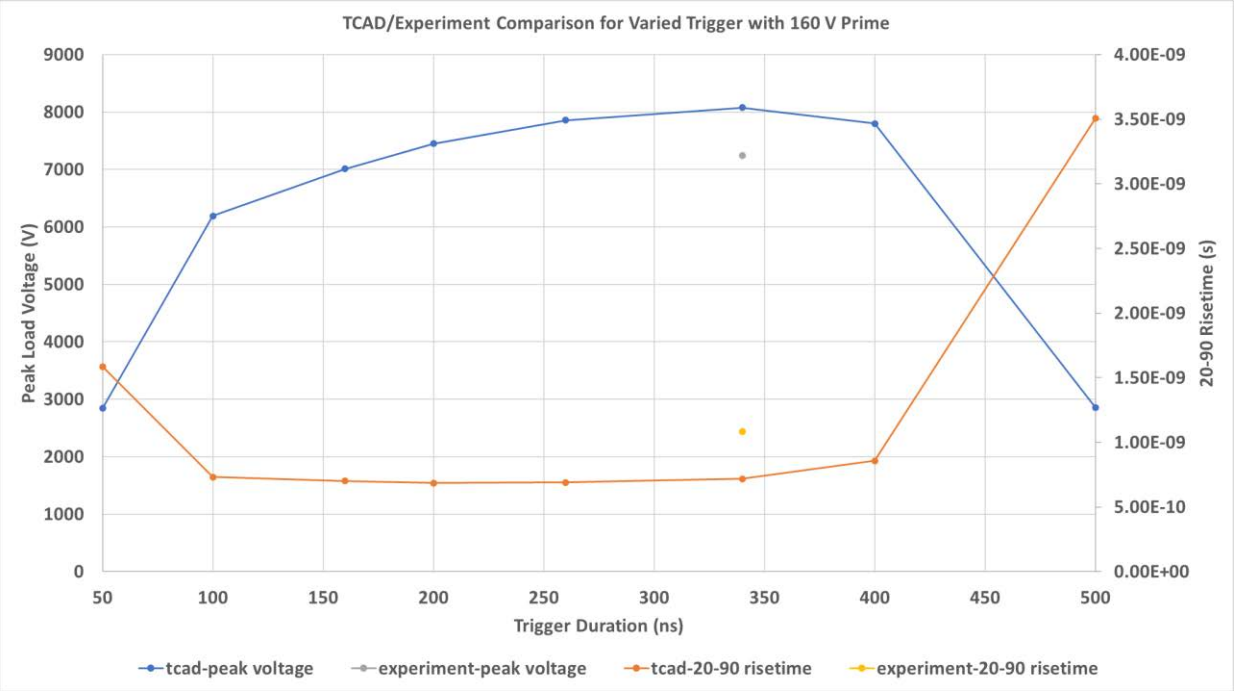


Figure 4.2.8. Comparison of TCAD and experiment for varied trigger duration of 160 V prime voltage for the 2x2 DSRD pulser. The TCAD simulation correctly predicts the 340 ns optimal trigger duration seen in experiment.

Next, LTSPICE (uses the new LTSPICE DSRD model and manufacturer LTSPICE MOSFET model), TCAD (uses TCAD DSRD model and TCAD SPICE MOSFET model) and experiments in the single bar DSRD pulser are compared for peak voltage, risetime and FWHM pulsewidth for 7-stack DSRD. One point to stress is that none of the models or the experiment are very accurate. The experiment relies on a new fixture for ease of trading various and different DSRD stack sizes but may have high enough parasitics and/or reflections such that the measurements do not agree well with previous results or most published results. This experimental difference is related, most likely, to a greatly increased risetime not indicative of DSRD action and correspondingly high pulsewidth (~twice the risetime). The TCAD model for the DSRD and LTSPICE model for the DSRD must both be calibrated to appropriate experimental data and will also need to include circuit parasitics in the simulation, if significant, to match experiment. The LTSPICE DSRD model has yet to be very closely matched to experimental standard diode tests and is limited by both the quality of experimental data (for example high power data) and the models used (does not include breakdown, reverse knee currents, forward capacitance fitting). That said, the TCAD and LTSPICE pulser simulations match well to earlier experimental data, which was not as comprehensive in prime voltage and trigger duration sweeps and should match new experiments well. These comparisons represent the best LTSPICE DSRD model known to us by far and the most comprehensive experimental comparisons to date.

In Figures 4.2.9-11 are shown the new LTSPICE DSRD model and experimental comparisons for the single bar pulser using 7-stack DSRD for varied prime voltages with a 340 ns trigger duration. In Figures 4.2.12-14 are shown the same comparisons but for varied trigger duration at a prime voltage of 115 V. Both sets of results use a V_{bias} of 100 V. What is missing from the experimental results (seen previously in other experiments) is a falloff of peak voltage at higher or lower prime voltages and trigger durations. This holds for risetime and pulsewidth as well but is an increase. In some cases, the LTSPICE and experiment trend together, in others the TCAD and experiment, and in others the TCAD and LTSPICE (descriptions in figure captions). Overall, there is no clear, consistent match and will need to wait for more careful experimental studies to verify the models. The TCAD simulation models use the version 3 MOSFET TCAD SPICE model incorporating higher drain-source voltage current saturation and improved matching of capacitances and bodydiode. The LTSPICE MOSFET used for the LTSPICE simulations is for an earlier MOSFET used in earlier pulser studies. The new MOSFET used in experiments is a 1200 V maximum higher current rated (~400 A) MOSFET and its modeled has not been used yet. The LTSPICE simulations can also be performed with the manufacturer (encrypted) MOSFET model and the TCAD MOSFET SPICE model can be fit to the new MOSFET datasheet. However, it is not yet clear how different the results would be with the new MOSFET from the old.

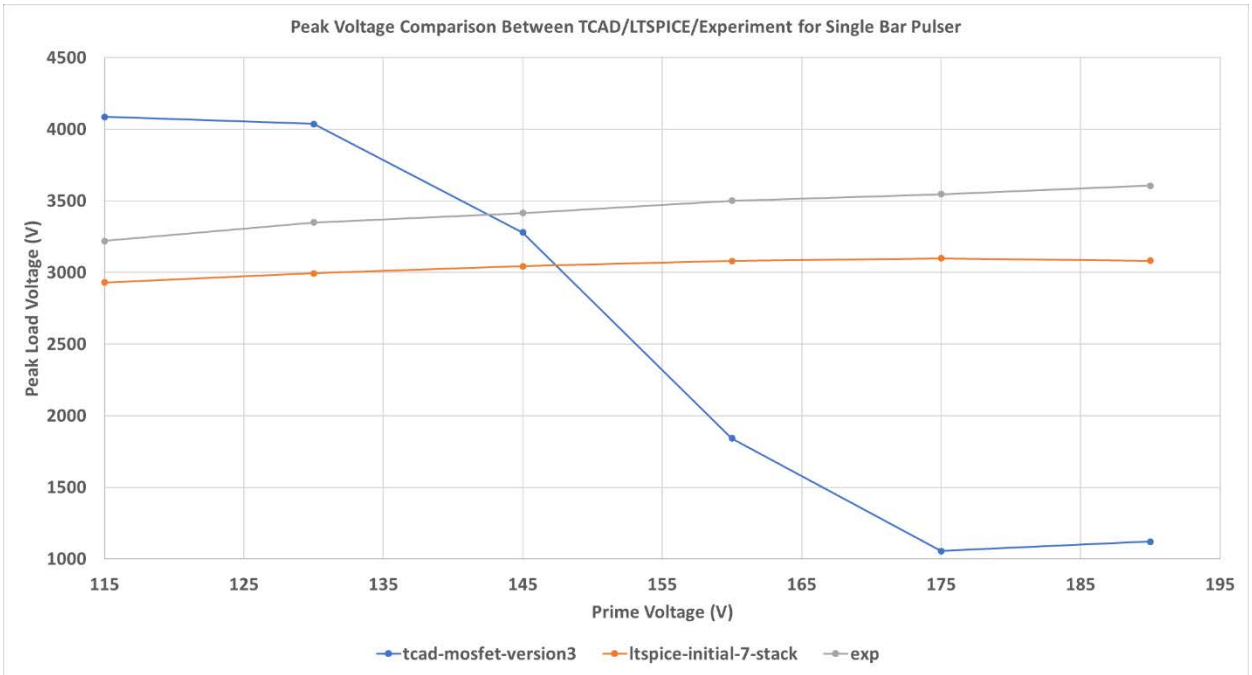


Figure 4.2.9. Peak voltage compared between experiment, TCAD and the new LTSPICE DSRD model for single bar pulser using 7-stack DSRD and varied prime voltage at 340 ns trigger duration. LTSPICE and experiment trend well together but do not show the falloff in peak voltage often seen with increasing prime voltage.

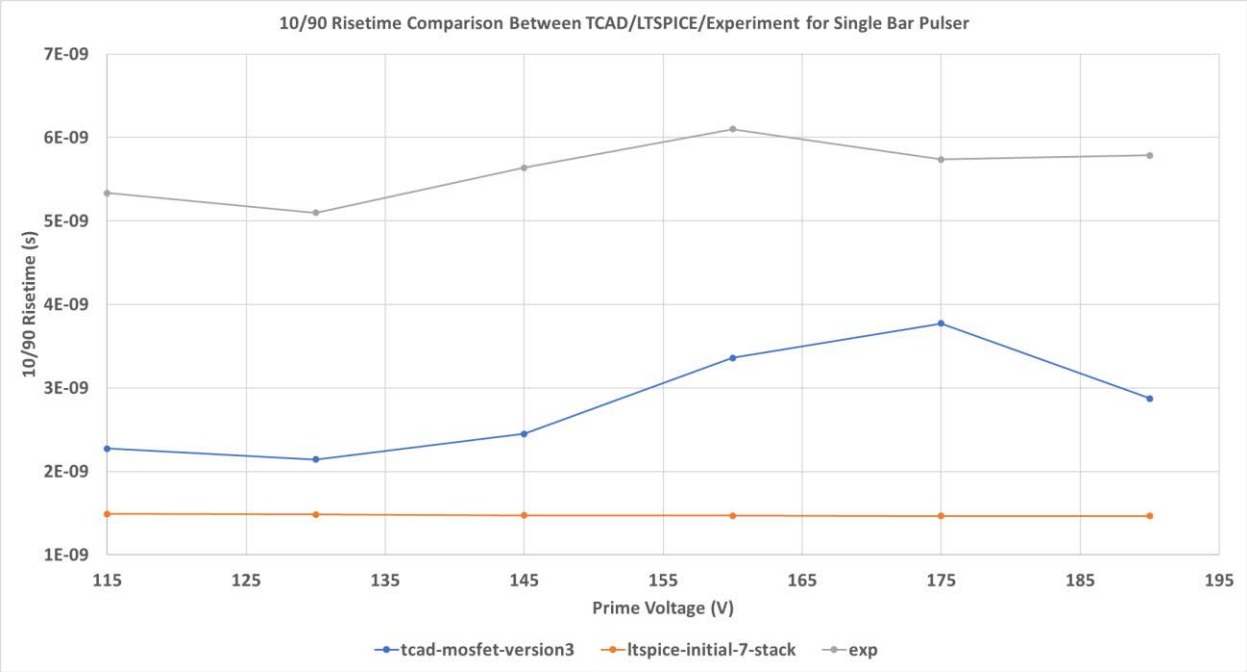


Figure 4.2.10. Risetime comparison between experiment, TCAD and the new LTSPICE DSRD model for single bar pulser using 7-stack DSRD and varied prime voltage at 340 ns trigger duration. LTSPICE and TCAD have more realistic risetime of DSRD operation. The LTSPICE model decreases very slight in risetime. Experiment and TCAD exhibit an increasing risetime with prime voltage until a maximum is reached.

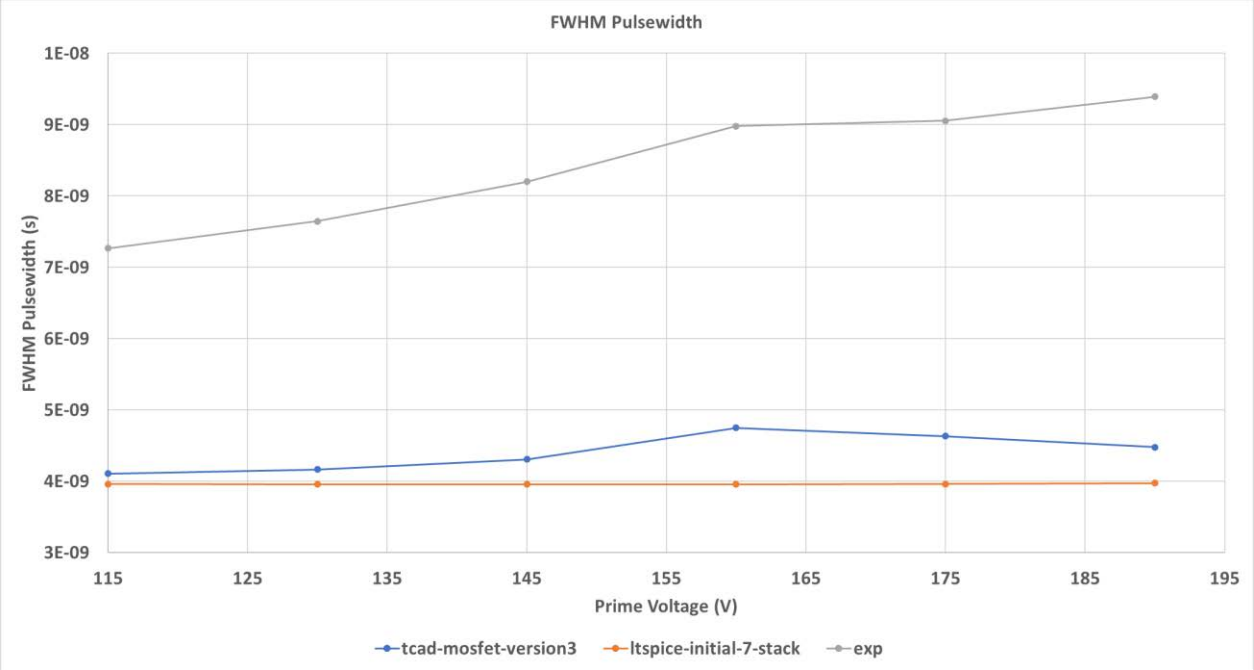


Figure 4.2.11. FWHM pulsewidth comparison for experiment, TCAD and the new LTSPICE DSRD model for single bar pulser using 7-stack DSRD and varied prime voltage

at 340 ns trigger duration. The experiment shows wide pulsewidths due to high risetimes not indicative of DSRD action. The TCAD and LTSPICE results are close as with the risetime results.

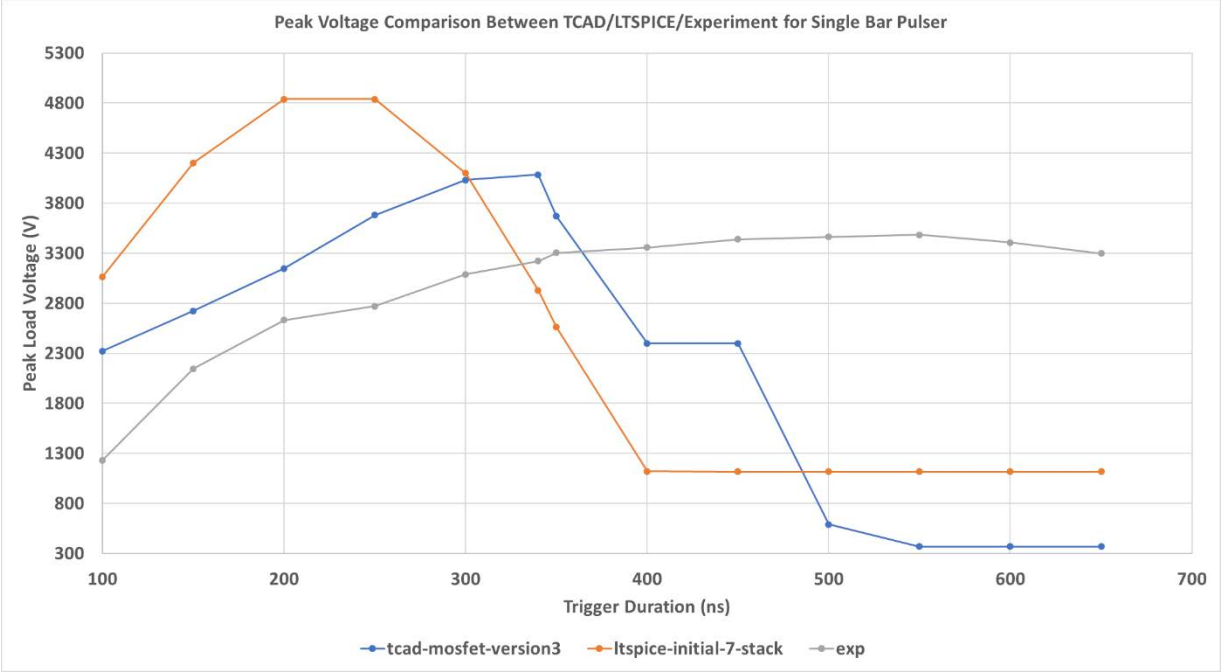


Figure 4.2.12. Peak voltage comparison between experiment, TCAD and the new LTSPICE DSRD model for single bar pulser using 7-stack DSRD and varied trigger duration at 115 V prime voltage. Both the TCAD and LTSPICE models trend together but are different than the experimental curve.

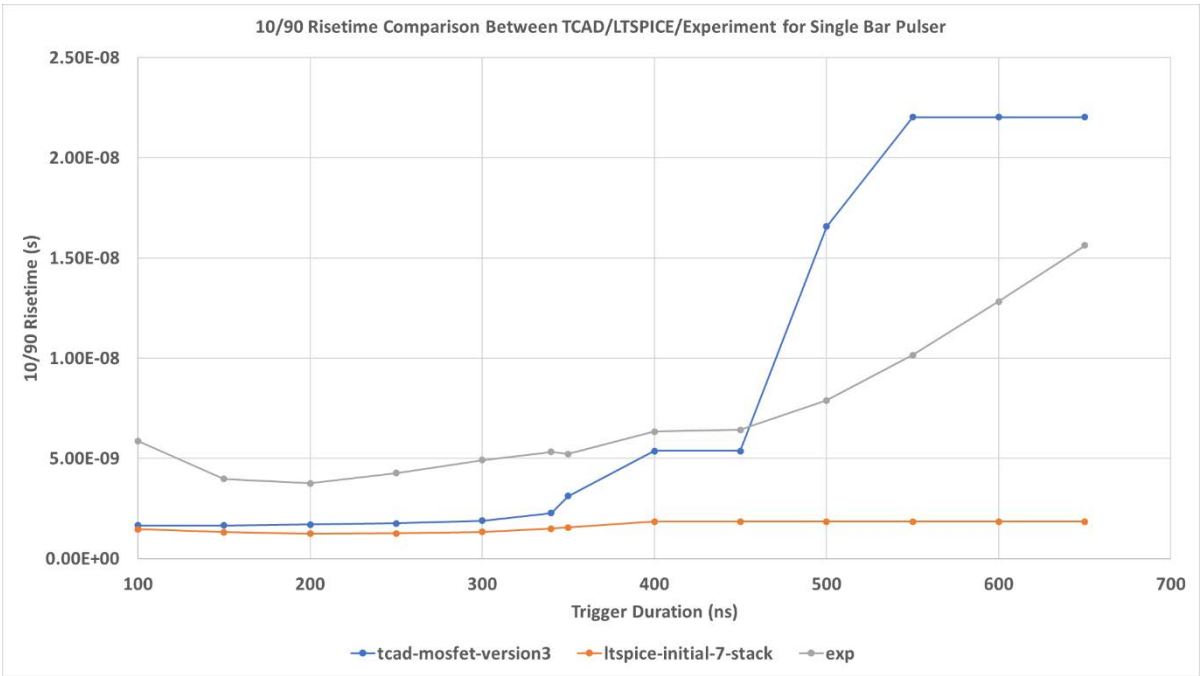


Figure 4.2.13. Risetime comparison between experiment, TCAD and the new LTSPICE DSRD model for single bar pulser using 7-stack DSRD and varied trigger duration at 115 V prime voltage. Again, the experimental risetime is not indicative of DSRD action. The TCAD and LTSPICE model results trend together until the TCAD and experiment both increase in risetime with increasing trigger duration with TCAD making a larger shift.

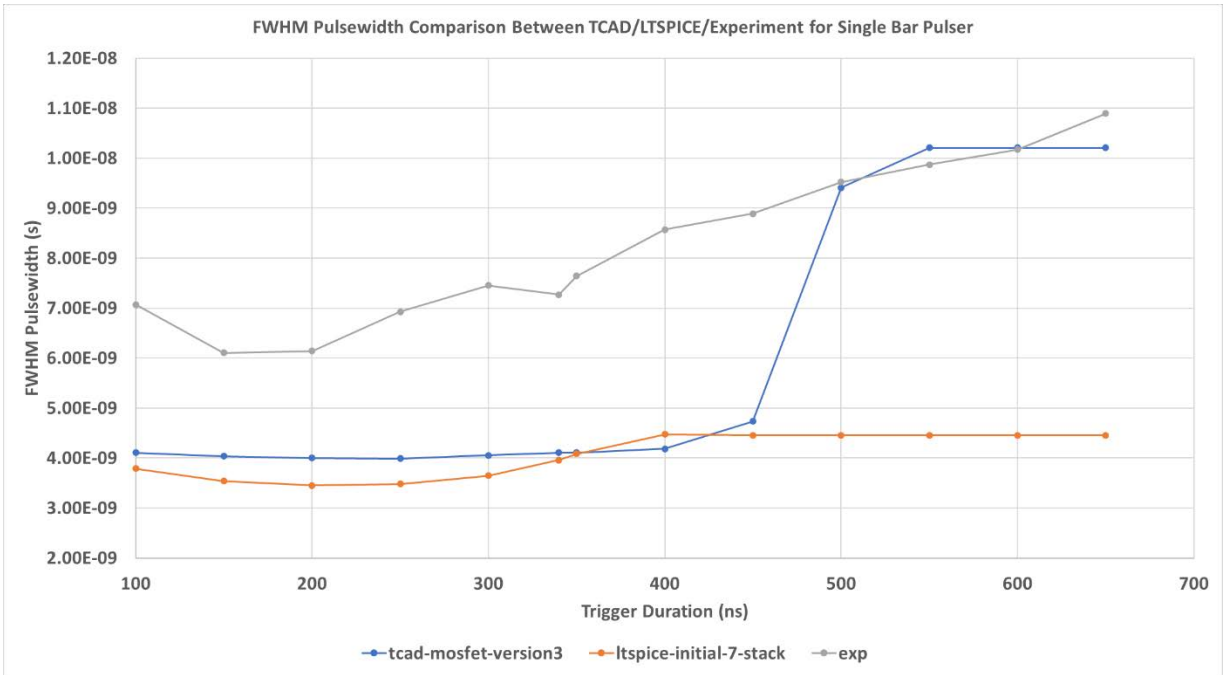


Figure 4.2.14. FWHM pulsewidth comparison between experiment, TCAD and the new LTSPICE DSRD model for single bar pulser using 7-stack DSRD and varied trigger

duration at 115 V prime voltage. The TCAD and LTSPICE model results trend together until the TCAD jumps in pulsewidth with increasing trigger duration.

4.2.5 Summary of Significant Findings and Mission Impact

DSRD TCAD simulation started by replicating published TCAD DSRD results and then simulating devices similar with actual in-house DSRD. The variation of the sinewave pulse voltage input magnitude and period on DSRD charge storage were collected. Charge storage timing (when the diode empties charge stored from forward pulsing) of ~50% was achievable with sufficiently long voltage input period which is necessary for maximum reverse current cutoff.

DSRD stacks, as opposed to individual die DSRD, were simulated showing reduced risetime from single die to 5-stacked DSRDs consistent with published and earlier in-house data. Series resistance to model metal resistance between DSRD in stacks and doping variability in stacks was also modeled in TCAD showing metal resistance must be large to have an impact on peak voltage and risetime and that doping variations proportionally effect risetime.

(A.1) Accurate DSRD TCAD models have been developed that include both carrier-carrier scattering and Selberherr breakdown and are suitable for DSRD operation below the dynamic breakdown threshold. Peak voltage and risetime were limited by the breakdown model and more closely match experimental pulse data.

(A.2) Work on TCAD SPICE MOSFET models has been done for the primary switch model (MOSFET) with conversion of the code to TCAD SPICE being partly completed to allow for modeling the complete DSRD-based pulser system (except driver). However, the conversion to TCAD of the MOSFET primary switch model, developed by CREE, to TCAD SPICE is complicated by having to develop custom behavioral models in TCAD SPICE which would be high-risk. Instead, a published model usable in TCAD SPICE was implemented and fit to the datasheet and then tested in a DSRD pulser simulation. The new MOSFET SPICE model usable in TCAD showed improvement in not having a first output pulse peak that was higher. This higher pulse had occurred in the TCAD MOSFET model (not SPICE model) and had not occurred in the voltage-controlled resistor MOSFET model (inaccurate model). Further refinement and testing of the new MOSFET SPICE model for use in TCAD has been more closely fit with the Cree LTSPICE model and compared to the Cree datasheet. The model can also be adapted to a new MOSFET in use within current DSRD pulsers. Further fitting can still be accomplished and matching both the Cree datasheet and LTSPICE model for gate charge and switching characteristics can be completed with more research into the test circuits used which are commonly not well explained in datasheets.

(A.3) A new DSRD LTSPICE model has been developed following the method used for developing a TCAD SPICE MOSFET model and by matching to experimental standard diode tests. The forward I-V and reverse C-V have been well matched using a 7-diode model for a 7-stack DSRD, as opposed to using only a 1-diode model for all DSRD stack heights. The reverse I-V and forward C-V are generally more problematic to fit to and proved to be so. More research and effort will be

necessary to improve these matches and understand the impact on pulser simulation. The reverse recovery experiments have also been well matched and complete the matching of all the standard diode tests. Pulser performance has been difficult to assess due to the experimental data gathered thus far. The new DSRD LTSPICE model will also enable improvements in the TCAD SPICE MOSFET model. Overall, the new DSRD model represents a vast improvement over the previous model but has yet to include breakdown effects possible in the TCAD DSRD model and therefore breakdown limits of DSRD operation.

(A.4) LTSPICE, TCAD and experiment have been compared for the single bar pulser using a 7-stack DSRD, however there is some discrepancy for these experiments with earlier experiments (which the LTSPICE and TCAD simulations match better with) likely due to the new DSRD switch integration used for ease of switching out DSRD of various stack heights and combinations. As more experimental data is acquired for the pulsers the comparisons with simulation will yield more useful results. The 2x2 DSRD pulsers have been compared to TCAD simulation incorporating the latest TCAD SPICE MOSFET models showing some similarities in predicted peak voltage and risetime, but the most significant result is the matching of the experimental optimum trigger duration of 340 ns with TCAD results. With further experiments and simulation refinement it is expected that the models will be predictive of experiment within the quality of the experimental data and models used.

(B.1) DSRD risetime performance was collected from TCAD simulations for variable carrier lifetime. Changes in lifetime had no significant effect on risetime other than the output pulse starting earlier.

(B.2) DSRD peak voltage and risetime were simulated in TCAD to include avalanche modeling or not. TCAD avalanche models limited peak voltage and risetime at the load over a range of voltage input magnitudes. A TCAD parameter study for DSRD stack height and DSRD area for several doping profiles with and without avalanche modeling was performed (Spring 2021 UMKC OSPRES Grant Review and Technical Exchange). The avalanche model and model parameters were also modified to account for dynamic breakdown rather than static and then compared to the no avalanche case and experimental data. From the improved avalanche modeling and TCAD parameter study, the optimal area of the DSRD can be obtained. However, for the 500 V voltage input magnitude used, the DSRD output were all in breakdown and are not predictive of non-breakdown behavior. Future studies for optimal area will include a range of voltage magnitudes to study DSRD performance and breakdown.

(B.4) TCAD process and device modeling for the development of process steps and their resultant doping profiles and device operation was begun. This modeling will enable a connection between the fabrication parameters and the device operation for DSRD (and PSD).

(B.5) Exponential doping profiles were shown (via TCAD) to outperform Gaussian and error function profiles slightly. Exponential profiles have an optimal minimum doping of 5×10^{13}–$1\text{x}10^{14}$ dopant atoms/cm^3, while Gaussian and error function

profiles have an optimal minimum doping of 1×10^{13}-5×10^{13} dopant atoms/cm^3. Further exponential doping parameter studies were carried out in circuits A and B of Figure 4.2.1 (see JUN 2021 Grant Report) which included a broader doping parameter space for minimum doping, junction placement, basewidth and peak doping over a wider range of voltage input magnitudes (for breakdown limitations). The results are similar to before and show the optimally performing doping profile has a minimum doping of 5×10^{13}, no basewidth, junction placement of 95 μm, and peak doping of 1×10^{18} (p-side) and 1×10^{19} (n-side) dopant atoms/cm^3. A comparison was made for the optimal exponential doping profiles to optimal error function, LLNL and SPT DSRD designs within the 2x2 DSRD pulser system. The TCAD study showed the exponential doping profile performs the best overall when considering peak voltage, risetime, voltage riserate, maximum reverse current, FWHM pulsewidth, prepulse and gain. Epitaxy designs with realistic deviations from the ideal exponential profile from the SRP data were shown in TCAD to not significantly affect the performance.

(B.7) A more complete gain study for varying prime voltage input and stack height was completed. The results show a variety of considerations must be made for determining the better stack heights to use in DSRD pulsers. The design of the pulsers can be improved when considering the gain staging in multi-staged DSRD pulsers as caused by the DSRD stack heights used. The 7- and 13-stacks showed the best gain. However, the peak voltages were best for the 13-stack while the 26-stack required unrealistic MOSFET currents to achieve its maximal peak voltage (or gain). For gain per die within a DSRD stack, 1-stacks showed the best gain per single and showed that gain ‘efficiency’ drops with stack height. Still, higher 7- and 13-stacks had the highest gain. How best to use this new data for DSRD pulsers is under discussion.

(C.1) Pulse sharpening has been verified for PSD devices for the standard design and another non-conventional design. The PSD was also modeled within a DSRD-based pulser circuit combining for the first time TCAD modeling of both DSRD and PSD together within the same circuit with only the primary switch model not included.

(E) DSRD pulser circuits for the single-bar (Circuit B of Figure 4.2.1) and 2x2 (circuit C of Figure 4.2.1) have been simulated within TCAD allowing the use of a TCAD DSRD model, whereas in SPICE no accurate DSRD SPICE model is available. Currently, the primary switch MOSFET is modeled in TCAD, as well, but SPICE models can also be developed for the SPICE within TCAD as and will allow for better use of computational resources within TCAD. The MOSFET model and pulse repetition are being studied in detail to more closely match experiment and TCAD.

4.2.6 References

[1] Kyuregyan, A. S. "Theory of drift step-recovery diodes." *Technical physics* 49, no. 6 (2004): 720-727.

[2] Russell, Howard Jr. “The SPICE Diode Model.’ OPAL Engineering, Inc. Chapter 3.

[3] Sischka, Franz. “Diode Modeling Tutorial.”

[4] Han, Dong-Pyo, Young-Jin Kim, Jong-In Shim, and Dong-Soo Shin. "Forward-capacitance measurement on wide-bandgap light-emitting diodes." *IEEE Photonics Technology Letters* 28, no. 21 (2016): 2407-2410.

[5] Tseng, K. J., and S. Pan. "Modified charge-control equation for more realistic simulation of power diode characteristics." In *Proceedings of Power Conversion Conference-PCC'97*, vol. 1, pp. 439-444. IEEE, 1997.

[6] Arribas, Alejandro Pozo, Mahesh Krishnamurthy, and Krishna Shenai. "A simple and accurate circuit simulation model for high-voltage SiC power MOSFETs." *ECS Transactions* 64, no. 7 (2014): 99.

4.3 Pioneering Drift-Step Recovery Diode Processing and Manufacturing

(Alex Usenko)

4.3.1 Problem Statement, Approach, and Context

Primary Problem: Since Boff, Moll, and Shen's discovery of the high-speed switching effect inherent in initially forward-biased solid-state diodes that are suddenly reverse-biased in 1960 [1]; DSRD's (as termed by Grekhov and Kardo-Sysoev in 1985 [2]) performance has not increased as their deep-diffusion manufacturing process remains the same as it was over 60 years ago – the voltage-to-risetime, dV/dt, of these silicon-based diodes remain on the order of 10^{12} V/s. Furthermore, all possible ways to improve pulse performance of DSRD made by deep diffusion have been extensively investigated and exhausted. To achieve the 10^{13} V/s (10 kV/ns) voltage-to-risetime required by an all-solid-state HPM pulse generation utilized to support of the Naval afloat mission, improving DSRD manufacturing techniques must ensue.

Solution Space: Leverage applicable concepts from mainstream silicon chipmaking industry and apply new/novel manufacturing methods to DSRD processing.

Sub-Problem 1 – Diode stack sidewall insulation/passivation: The SOTA uses polyimide coating on side surface of diode stack. This limits the pulsed performance of diode stack by silicon surface properties. Improved side termination and passivation will increase pulsed performance to a level limited by bulk Silicon properties.

Sub-Problem 2 – Deep diffusion technology restricts optimization of doping profile: SOTA DSRDs are manufactured using deep diffusion technology exclusively; a technology which is extremely limited in its ability to produce an optimal doping profile. Diffusion allows only one doping profile, the erfc function.

Sub-Problem 3 – Stacking of DSRD dies: SOTA uses soldering of diode dies into a stack. The soldering additionally limits breakdown voltage thus limiting pulsed performance.

Sub-Problem 4 – Packaging of stacked dies: SOTA uses bare stacked DSRDs. Mounting the bare stack into a press-pack type package will improve long term stability, so the stack will survive much higher number of pulses before it burn out.

State-of-the-Art (SOTA): In a recently published paper (2019) from the Russian St. Petersburg team at the Ioffe institute [3] reported achieving a peak current density of 5 kA/cm^2 with a rise time of the output pulse front being ~ 2.3 ns, and the peak voltage

across the load is 900 V (i.e., the peak switching power is 4.5×10^6 W/cm^2). The St. Petersburg team utilized deep diffusion technology. The team at NPO Energomodule, Moscow, Russia [6] who also use the deep diffusion method to report simulation results where a 1.35 ns rise time was achieved for ~ 1000 V peak voltage impulse. In a paper published by the team at Ekaterinburg, Russia, a voltage pulse amplitude of 540 kV with a 20%–90% rise time of ~1.2 ns corresponding to a voltage rise rate of ~0.3 MV/ns was reported. To achieve these higher performance metrics however, a deep diffusion SOS diode was used with additional dynistor pulse sharpener. Neither dynistor design nor the fabrication process described within [8].

As one can see, without additional pulse compression methods like those used in [8] which compensate for the DSRDs produced using deep diffusion, there has not been any significant improvement in DRSR pulse performance compared to pioneering work done in 1960 [1].

Deficiency in the SOTA: First, no DSRDs have been manufactured using epitaxy technology with doping profile optimization. Second, no DSRD processing method exists which integrates side passivation with silicon dioxide. Finally, an acceptable DSRD stacking process has yet to be developed.

Solution Proposed: Manufacture DSRDs within the continental United States using epitaxy growth process leveraging the optimal characteristics (e.g., doping profile, carrier concentration) determined through the work performed in Section 4.2 through working with industry partners at Semiconductor Power Technologies (SPT), Livermore Semiconductor Research Laboratories (LSRL) and Lawrence Livermore National Laboratory (LLNL – Voss Group).

Relevance to OSPRES Grant Objective: DSRD manufacturing technology is a major building block of short-pulse high-peak power defense systems. Our new disruptive process flow for DSRDs enables not only manufacturing of DSRDs at scale, but within the continental United States (CONUS). In doing so we will redefine the SOTA by producing optimal DSRDs which are used within best-in-class HPM pulse generators which become part of more advanced defense systems within the Navy's arsenal of protecting the warfighter and its high-value assets.

Risks, Payoffs, and Challenges:

Risks: As the process of producing DSRDs using Epitaxial growth is both novel and uncharted territory, there is inherent risk to its success. Additionally, post-processing methods based on the discussions provided in the ***Sub-Problems*** section have yet to be matured.

Payoffs: Deep diffusion technology allows to make DSRD that use about 1/3 of theoretical silicon capabilities. Our epi DSRD expected to approach theoretical limit of silicon. 3X improvements in pulse time performance, and 3X improvement in pulse voltage magnitude are expected.

Challenges:

1. Develop process for much thicker ~ 200-micron epitaxial layers; previously 100 microns was considered as a limit for growing defect free silicon epitaxial layer.

2. Discover an optimal doping profile for DSRD and develop epitaxial recipes resulting in this profile.
3. Develop new die stacking technology that allow to achieve pulse performance close to theoretical limit.
4. Develop new silicon surface passivation technology for vertical side surface of diodes that allow to achieve pulse performance close to theoretical limit.
5. Find process integration solution (make compatible) for steps of forming p-n junction, die stacking, and side passivation.
6. Solve packaging issues to make packaged DSRD with lower than SOTA parasitics
7. Solve packaging issues limiting diode lifetime
8. Solve packaging issues related to thermal management.

4.3.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Produce epitaxial DSRDs which contain optimal exponential doping profile and carrier concentrations [*Estimated completion by SEP21*].

1. Task – Obtain quotes from potential vendors for epitaxy [*MAR—APR21*]; Quotes from Silicon Valley Microelectronics Inc. and from Lawrence Semiconductor Research Laboratory obtained.
2. Task – Design of Experiment on 25 wafers through negotiations with vendors [*MAY–JUL21*]; Completed
3. Task – Perform DSRD stack epitaxy on 25 wafers. [*JUN–AUG21*]; Completed.
4. Develop process integration scheme that uses epitaxy and diode stacking on wafer level [*JUL–OCT21*];

(B) Milestone – Develop processing techniques able to manufacture loose-stack press-pack DSRDs from epitaxial wafers [*on hold until Milestone A is completed*].

4.3.3 Progress Made Since Last Report

Epitaxy on 25 wafers finished.

4.3.4 Technical Results

(A) 24 wafers have been processed with epitaxy at outside vendor Lawrence Semiconductor Research Laboratory, Tempe, AZ. Each wafer has different doping profile. Some profiles grown are shown on **Figure 4.3.4.** All grown profiles follow TCAD predicted optimal profile - exponential. Slopes, base width, and base doping were varied. If no losses during manufacturing, it will allow to produce 10 sets of 7-stack diodes per wafer.

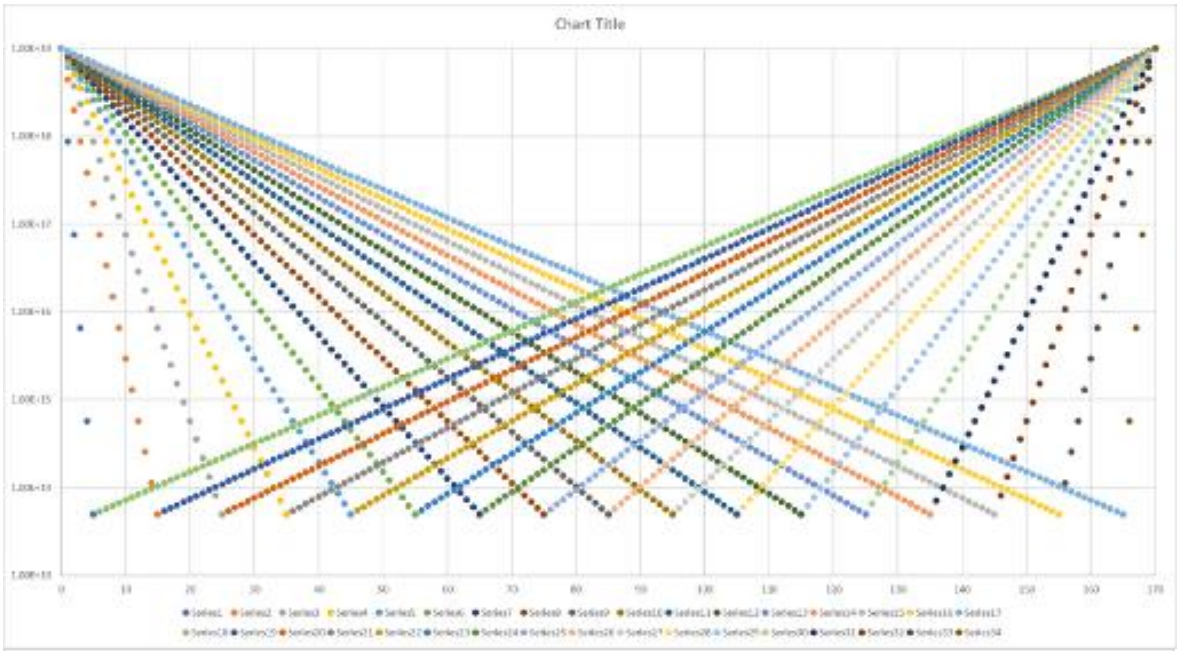


Chart Title

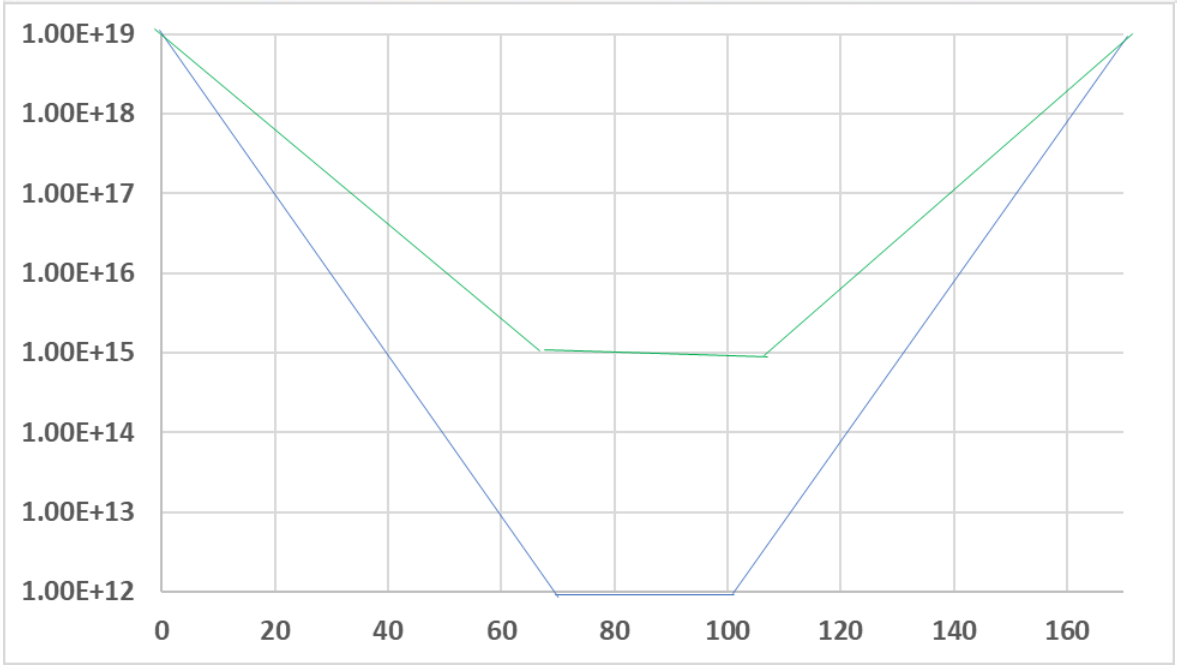

1.00E+19
1.00E+18
1.00E+17
1.00E+16
1.00E+15
1.00E+14
1.00E+13
1.00E+12
0
20
40
60
80
100
120
140
160

Figure 4.3.4 (TOP) some of epitaxial doping profiles grown, n- and p- slopes varied; (MIDDLE) some of epitaxial profiles grown: undoped base width varied, and undoped concentration varied; (BOTTOM) deviation from ideal doping profile (straight line) and real SRP (spreading resistance profile) obtained.

DoE (design of experiment) has final epitaxy split shown in table **Figure 4.3.5**. The incoming data as a function of doping profiles and resulting electrical performances of the DSRDs from each wafer will be loaded into Minitab software. The Minitab analysis will extrapolate data and predict the doping profile that gives the best DSRD performance, see section **4.4**.

The 100-micron limit of epitaxy thickness was successfully exceeded. Typical total epi thickness grown was 170 microns, and 200 micron was the thickest grown in this run.

No significant defects observed in the grown diode' p-i-n structure. Only misfit dislocations found in epi crown area – beyond 3 mm edge exclusion zone, shown in **Figure 4.3.6** .

		1st pass	2nd pass	3rd pass	Run 1st			
		N-type				P-type		
Table spli	R11 Thickness	R11 Intrinsic	Product wafers	Test wafers(SRP)	Total	R5 Intrinsic	R5 Thickness	R5 Thickness
5498.A	70um(1E+14)	0um	2	1	3	0um	70um(5498.AA)	85um(5498.AD)
5498.A	70um(1E+14)	0um	2	0	2	15um(E+13)	70um(5498.AB)	85um(5498.AE)
5498.A	70um(1E+14)	0um	2	1	3	30um(E+13)	70um(5498.AC)	85um(5498.AF)
5498.B	85um(1E+13)	0um	2	1	3	0um	70um(5498.BA)	85um(5498.BD)
5498.B	85um(1E+13)	0um	2	0	2	15um(E+13)	70um(5498.BB)	85um(5498.BE)
5498.B	85um(1E+13)	0um	2	1	3	30um(E+13)	70um(5498.BC)	85um(5498.BF)
5498.C	70um(1E+14)	15um(1E+12)	2	0	3	0um	70um(5498.CA)	85um(5498.CB)
5498.D	85um(1E+13)	15um(1E+12)	2	0	3	0um	70um(5498.DA)	85um(5498.DB)
5498.E	70um(1E+14)	30um(1E+12)	2	1	3	0um	70um(5498.EA)	85um(5498.EB)
5498.F	85um(1E+13)	30um(1E+12)	2	1	3	0um	70um(5498.FA)	85um(5498.FB)
5498.G	70um(1E+14)	30um(1E+14)	2	0	2	0um	70um(5498.GA)	85um(5498.GB)
5498.H	70um(1E+14)	15um(1E+14)	2	0	2	0um	70um(5498.HA)	85um(5498.HB)
			24	6	30			

Figure 4.3.5 Final split table of epitaxy run.

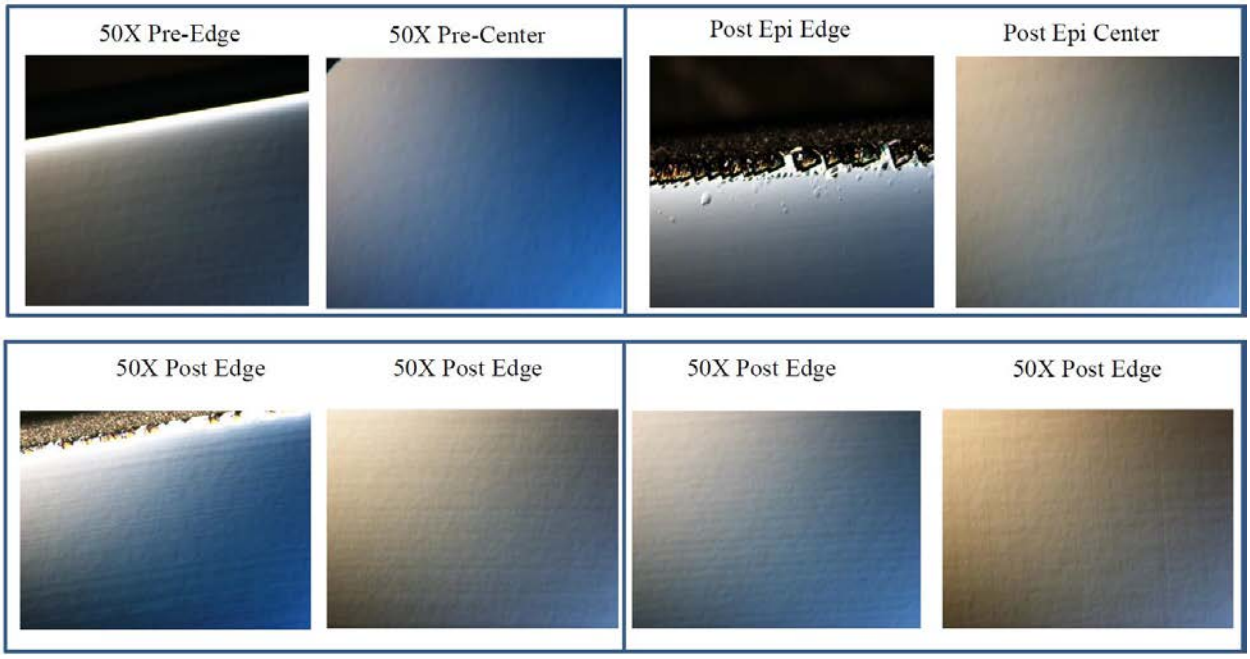


Figure 4.3.6 Optical inspection of defects before/after epi with Nomarski microscope.

(B) A new approach to sidewall passivation was investigated, consisting of SiO2 with a porous silicon double layer. In this approach, porous Silicon layer is first grown on diode sidewalls at room temperature. A short loop run using blanket silicon wafers executed first. The blanket wafers are submersed in a 1000:1 mixture of concentrated HF and HNO3. It converts silicon on wafer surface into porous silicon layer. The thickness of the porous layer achieved is about 1 micron. Then the wafers were rinsed and dried in air.

During drying, the upper part of porous silicon layer oxidizes thus converts into SiO2. The bottom part of the porous layer is now sealed. Porous silicon is a semi-insulator. It forms a “bleeding” layer – film that passivates silicon surface, but not able to collect electrical charge that forms a parasitic conductive channel in silicon. As this process proven technical feasibility in the short loop run, next plan is to implement it in 3rd Gen DSRD run.

(A.1) 2nd and 3rd generation DSRD lots have been started. Both based on epitaxy (1st generation was based on old deep diffusion technology.

2nd and 3rd epitaxy ‘runs’ (i.e., manufacturing processes) ongoing. Both are at the final stage and near completing epitaxy step. 2nd run uses epi vendor SVM (Silicon Valley Microelectronics, Inc.) where doping profile used are similar to those of deep diffusion. 3rd run uses epi vendor LSRL (Lawrence Semiconductor Research Laboratory) and doping profile is best-predicted-by-simulation (exponential).

Upon receiving wafer lots from epi vendors, diode fabrication will continue for metallization, cutting into individual dies, stacking of dies, and side wall passivation. Finished DSRD stacks will be tested on static and pulse performances.

Some wafers from 2nd and 3rd generation lots will be processed using new techniques that were recently suggested: (1) side wall passivation by fluorinated SiO2 deposited at room temperature; (2) side wall passivation by staining in HF/HNO3 1:1000 mixture; (3) stacking on wafer level using SLID wafer bonding process; (4) side insulation of individual diodes by etched V-grooves and thermal oxidation.

IP disclosure and provisional patent application [10] have been filed on one of 4 new techniques. Rest 3 will be filed in next reporting period.

4.3.5 Summary of Significant Findings and Mission Impact

(A) Technical feasibility analyzed: can we switch from 60-years old deep diffusion DSRD process to epitaxy-based process? Rigorously analyzed with analytical and simulation approaches. Decision made to concentrate on the new epitaxy process.

New process integration scheme suggested. It combines side diode insulation by anisotropic V-groove etch Figure. 4.3.4 and thermal SiO2 and stacking on wafer level instead of die level Figure 4.3.5. This scheme will be implemented on ongoing 3rd generation DSRD run.

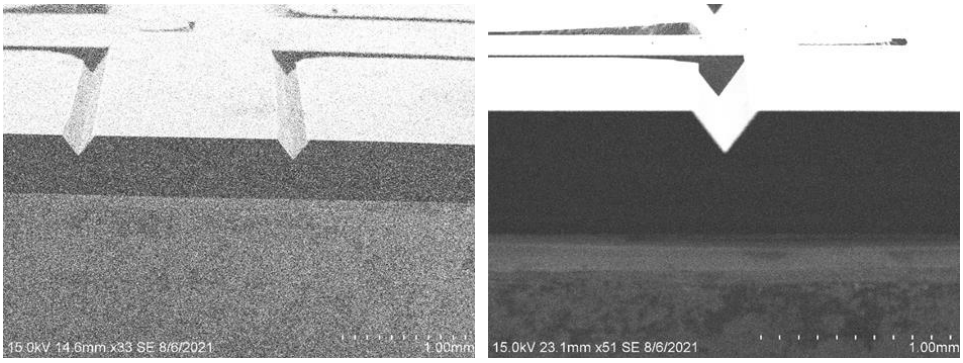


Figure 4.3.4. Side insulation by anisotropic groove etch. Technical feasibility ran on blanket wafer.

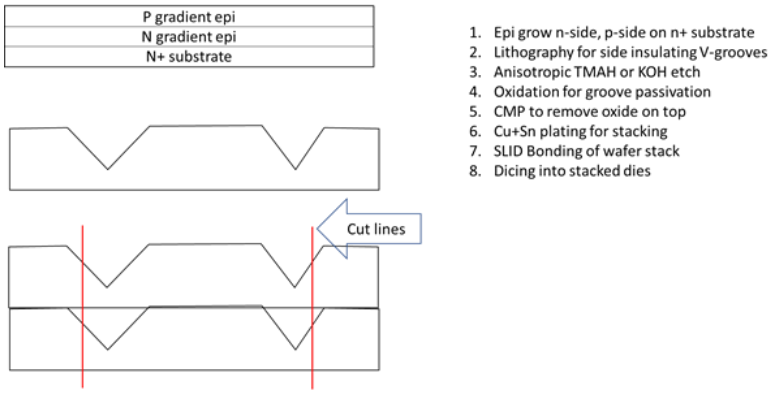


Figure 4.3.5. Process integration scheme.

Two new processes suggested for diode side wall passivation – staining, and liquid phase SiO2 deposition, both room temperature. Experimental setups for both processes have been built. Short loop runs on blanket wafers to prove technical feasibility planned. Experiment on staining in HF/HNO3 finished. Results show that near 1-micron thick SiO2 film is successfully grown. Experiment on SiO2 deposition from liquid phase is ongoing.

New DSRD fabrication process based on out-diffusion of dopants and wafer bonding is suggested. Experiment planned and ongoing. Vendors for out-diffusion – THAT Corp. and SVM Inc., and vendor for wafer bonding – EV Group chosen. Quotes requested. IP disclosure filed. Provisional patent application filed with USPTO. Abstract [9] describing the process flow submitted to upcoming Pulsed Power Conference.

4.3.6 References

[1] Boff, A., J. Moll, and R. Shen. "A new high-speed effect in solid-state diodes." in 1960 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, vol. 3, pp. 50-51. IEEE, 1960

[2] Grekhov, I. V., V. M. Efanov, A. F. Kardo-Sysoev, and S. V. Shenderey. "Power drift step recovery diodes (DSRD)." Solid-State Electronics 28, no. 6 (1985): 597-599.

[3] Lyublinsky, A. G., E. I. Belyakova, and I. V. Grekhov. "Numerical and Experimental Study of an Optimized p-SOS Diode." Technical Physics 64, no. 3 (2019): 373-379.

[4] Люблинский, А. Г., Е. И. Белякова, and И. В. Грехов. "Численное и экспериментальное исследования оптимизированного p-SOS-диода." Журнал технической физики 89, no. 3 (2019): 409-415.

[5] Kesar, Amit S., Yaakov Sharabani, Inbar Shafir, Shoval Zoran, and Ariel Sher. "Characterization of a drift-step-recovery diode based on all epi-Si growth." IEEE Transactions on Plasma Science 44, no. 10 (2016): 2424-2428.

[6] Voss, Lars F., and Adam M. Conway. "Tunnel drift step recovery diode." U.S. Patent Application 17/081,902, filed April 29, 2021.

[7] Kyuregyan, A. S. "High-Voltage Diffused Step Recovery Diodes: I. Numerical Simulation." Semiconductors 53, no. 7 (2019): 962-968.

[8] Rukin, S. N. "Pulsed power technology based on semiconductor opening switches: A review." Review of Scientific Instruments 91, no. 1 (2020): 011501.

[9] S. V. Korotkov, Yu. V. Aristov, V. B. Voronkov, and D. A. Korotkov, “Studying dynistor switches with nanosecond switching times,” Instrum. Exp. Tech. 57, 437–442 (2014).

[10] Alex Usenko, Anthony Caruso, Steven Bellinger “New Paradigm on Making Semiconductor Opening Switches for Pulsed Power” abstract #456, 23th IEEE Pulsed Power Conference 12-16 December, 2021, Denver, CO

[11] A.Usenko, Diode and Method of Making the Same, US Provisional Patent Application 63/216550 filed 06/30/2021.

4.4 Characterization of SOS Diode Performance through DOE Augmentation

(Megan Hyde)

4.4.1 Problem Statement, Approach, and Context

Primary Problem: Drift step recovery diodes (DSRDs) are planar diodes that are capable of nanosecond, high frequency (10-10^3 KHz) pulses [1] with applications as opening switches in inductive energy storage (IES) pulse generation circuits. The theory provided by Benda et al is the primary physical explanation for DSRDs, but it does not provide explanations to both the current interruption mechanism and the current loop inductance [3]. This discrepancy within the physical model of the diode reduces the ability to design and produce IES pulse generating circuits. In addition to the incomplete theory on DSRDs, there is no characterization process for assessing diode performances, leaving the entire DSRD lifecycle riddled with systemic uncertainties.

Solution Space: We will develop a methodology for assessing diode performance to provide an empirical solution to the IES pulse generating circuit designer in Section 4.5. Our diode assessment methodology will leverage data analytics coupled with a design of experiment (DOE) to process the parametric information provided by fabrication design (Section 4.3), to align the diode performance with simulation modeling (Section 4.2), and finally to provide an output for an optimized DSRD that meets the specific needs of the designer for the IES pulse generating circuit (Section 4.5).

***Sub-Problem 1*:** We do not yet understand the how the diode performance is affected by variations within the diode parameters due to unstandardized testing methodologies.

Sub-Problem 2: Correlating the diode (Key Performance Indicators) KPIs to IES pulser generator performance through a cohesive, standardized method does not exist.

Sub-Problem 3: The non-linear separable data generated from the DOE is too complex to leverage traditional data analytics.

State-of-the-Art (SOTA): Characterization methods for DSRDs include electrical curve tracing techniques. The curve tracing techniques are performed by a parameter analyzer, such as a Keysight B1500A Semiconductor Device Parameter Analyzer. Transient characteristics of the DSRDs are measured through an Avtech Pulser, or a similar measurement device.

Deficiency in the SOTA: Unlike other commercial off the shelf (COTS) diodes, DSRDs do not come with a manufacturing datasheet. A COTS manufacturing data sheet contains all the testing and performance specifications relevant to the purchased diode. This leads to a difficulty in correlating the performance of a diode, or stack of diodes, to be utilized within a pulse generating circuit since the performance specifications are unknown to the purchaser.

Solution Proposed: Develop a holistic evaluation network to characterize the KPIs of DSRDs. This network will include a DOE that will be a continuously evolving model as new KPIs are discovered between each of the stages within the network (Sections 4.2 to 4.6) and shall be labeled “augmented DOE”. Machine learning will be used as the primary decision-making tool for augmenting the DOE. Once the network is established, it will be used to outline the optimal parameters for stacks of DSRDs within an IES pulse generator.

Relevance to OSPRES Grant Objective: Bridging the gap between the theoretical and the physical performance of DSRDs enables closing the gap between a low fidelity TRL3 breadboard pulse generation system, to one which is at high fidelity TRL4 prototype level. At the TRL4 level, the DSRD-IES pulse generator system would be sufficient to replace the costly laser-based Si-PCSS HPM generator without compromise to scalability required to support the Naval afloat mission.

Risks, Payoffs, and Challenges:

Challenges: Traditional predictive analytics will be difficult to correlate with the augmented DOE due to the large volume of data. Machine learning is expected to assist with decision making processes for the DOE, but only if the proper KPIs have been established and good data has been used to train the machine learning model.

4.4.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Establish preliminary DOE and SOP for identifying KPIs of DSRDs [*estimated completion by DEC21*].

1. Task – Ascertain current KPIs used to optimize diodes simulated, manufactured, and utilized within the IES pulse generating circuit (from Sections 4.2–6) [JUN–AUG21];
2. Task – Construct preliminary DOE to acquire data on all KPIs based on Task 1 to produce an optimal output for the IES pulse generating circuit (Section 4.5) [AUG–SEP21];

3. Task – Leverage existing Python script to process legacy DSRD KPI data [*AUG—SEP21*];
4. Task – Develop new and review existing SOPs for experimental testing apparatuses used to evaluate individual KPIs and measure their performance [*AUG–OCT21*];
5. Task – Identify gaps/deficiencies in legacy KPI data, evaluate existing theoretical relationships to bridge gap and minimize DOE if possible [*SEP–OCT21*];
6. Task – Using SOPs developed in Task 4, acquire experimental data from legacy DSRDs, refine SOP(s) *pro re nata,* and assess repeatability and reproducibility [*SEP–OCT21*];
7. Task – Begin training machine learning model with legacy data to determine statistical correlations and significance of KPIs, and their interdependent relationships [*OCT–DEC21*];

(B) Milestone – Evaluate DSRD performance by the developed SOPs and facilitated by the preliminary DOE [*on hold until Milestone A is completed*].

1. Task – Augment DOE to include previously unidentified yet relevant KPIs based on new findings [*Est. Spring22*];
2. Task – Acquire data on newly manufactured epitaxial DSRDs from Section 4.3 using refined SOPs from Milestone A [*Est. Spring22*];
3. Task – Correlate KPIs to TCAD simulation model, manufactured diode characteristics, and 'M×N' IES pulser's performance to aid in simulation model development, fabrication procedures, and circuit topology development [*Est. Spring22*];

(C) Milestone – SOS diode network evaluation [*on hold until Milestone B is completed*].

1. Task – Refine Python script to incorporate new correlations based on findings from Milestones A&B [*Est. Fall22*];
2. Task – Amend ML training model with data acquired on new DSRDs (as characterized by Sections 4.2-3) to investigate statistical correlation of diode performance [*Est. Summer22*];
3. Task – Work with TCAD simulation team to address discrepancies between the DSRD's performance obtained experimentally, and that achieved within simulations [*Est. Summer22*];
4. Task – Collaborate with DSRD manufacturing team to address discrepancies between the DSRD's characteristics evaluated experimentally, and that desired by manufacturing process [*Est. Summer22*];
5. Task – Investigate relationships between statistical significance of individual diode KPIs to the peak performance of the IES pulser with the pulse generator team. [*Est. Summer22*];

6. Task – Incorporate findings from Tasks 1-5 into ML model, pinpoint KPI correlations of interest, and provide recommendations to IES sub-teams accordingly [*Est. Summer22*];

(D) Milestone – SOS diode network evaluation [*on hold until Milestone C is completed*].

1. Task – Augment DOE network to streamline diode evaluation and identify checkpoints/gates within simulation, manufacturing, and circuit development process to ensure optimal diodes are selected and utilized to produced robust high-fidelity IES pulse generator prototypes [*Est. Fall22*];

4.4.3 Progress Made Since Last Report

(A.1) Created a new KPI test matrix template to store information on each diode and to easily transfer parametric information to Sections 4.2–4.6.

(A.2) Installed Minitab and currently reviewing the literature on DOE analysis.

(A.3) Updated test file naming convention for easier processing in Python scripts. Successfully plotted and calculated 3 established KPIs from newly measured data from legacy diodes.

(A.4) Created a cover sheet for all testing SOP documents to maintain catalog of testing procedures. Established capacitance–voltage testing procedure and updated current method into SOP document. Currently working to train others in procedure for repeatability study. Updated the capacitance–voltage testing procedure, beginning with fixture compensation for open and short circuits, as well as updated the actual testing conditions such as the range of the DC voltage measurements. Determined that the legacy current–voltage procedure was insufficient due to equipment limitations. New process involves the use of a picoammeter, so the range is insufficient for determining breakdown voltages.

(A.6) Acquired capacitance-voltage and current-voltage measurements from several legacy diodes. Evaluation of 4 diodes showed that the present current–voltage measurement is insufficient.

4.4.4 Technical Results

(A.3) Developed new python scripts for capacitance-voltage and current-voltage data processing. These new scripts have been used to visually assess performance of the current SOPs with the legacy DSRDs. Refer to both Figure 4.4.1 and 4.4.2 in (A.4) for updates in SOPs.

(A.4) Figure 4.4.1 shows both the forward current-voltage (IV) and the capacitance-voltage (CV) measurements of three legacy DSRDs. An alternate testing apparatus is required for to provide information about the breakdown voltages. Visual comparisons between legacy and new capacitance-voltage measurements provided additional information, as can be seen in Figure 4.4.2.

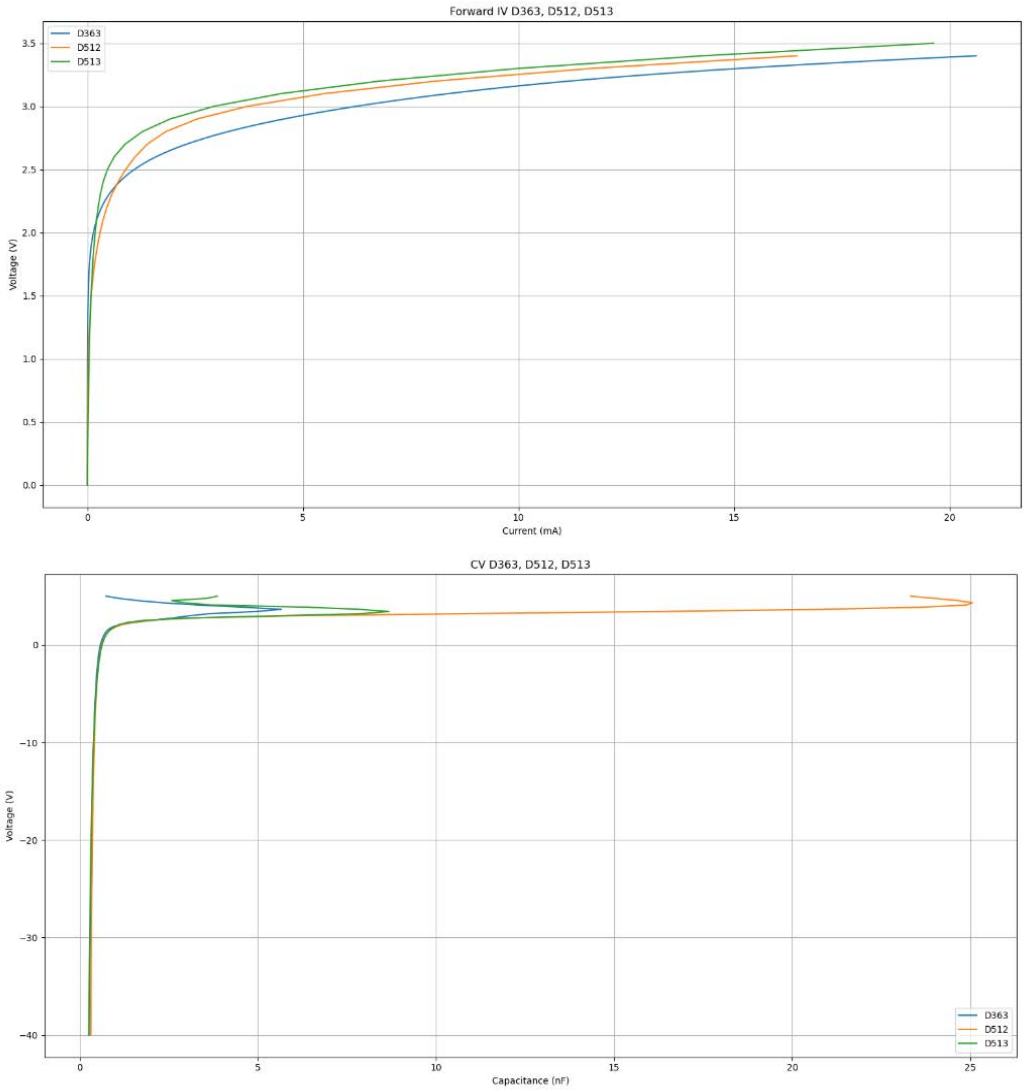


Figure 4.4.1 Shown above is the forward current-voltage (IV) data and the capacitance-voltage (CV) data collected from three legacy diodes.

(A.5) Evaluated the current-voltage testing procedure and concluded that the testing equipment is insufficient. Previous method for measuring capacitance started at -40V and stopped at 0V. New method now includes the measurements up to 5V. Differences between legacy and new data from the same diode can be seen in Figure 4.4.2.

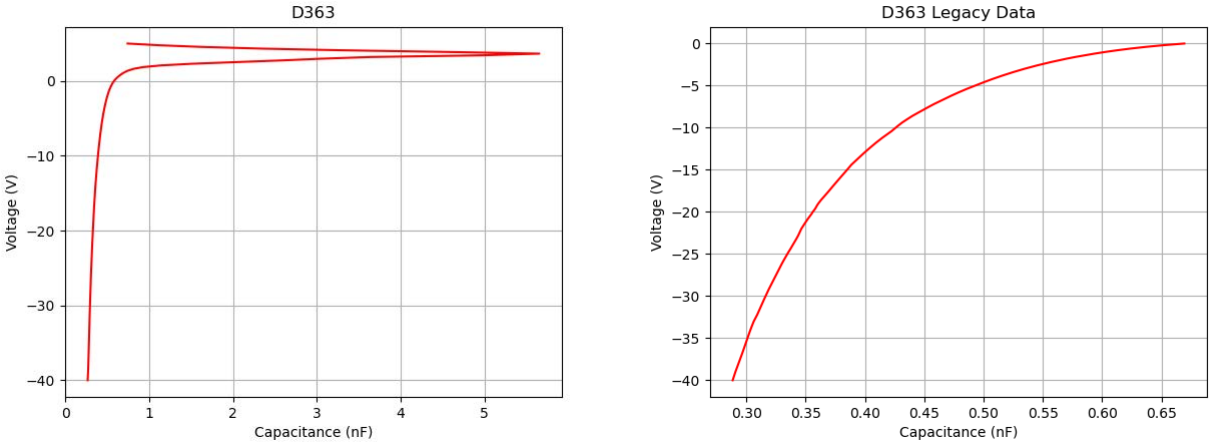


Figure 4.4.2 Shown above is an example of the new information captured within the new capacitance-voltage testing procedure. Previous methods would characterize each diode from -40V to 0V. The newly updated method captures information from -40V to 5V.

4.4.5 Summary of Significant Findings and Mission Impact

We have identified several KPIs pertaining to the diode characterization procedures. These KPIs have been stored within a matrix template that will also serve as a logistical catalog of legacy diodes and testing procedures.

The SOP for the CV testing method has been updated to include the fixture compensation as recommended by Agilent, an increased range for DC bias measurements, and a cover sheet for the SOP document to catalog changes to the method. This SOP doubles as a training tool to two new users who will be collecting data on future diodes that will be subject to a future repeatability study.

4.4.6 References

[1] Benda, H., & Spenke, E. (1967). Reverse recovery processes in silicon power rectifiers. Proceedings of the IEEE, 55(8), 1331-1354.

[2] Kozlov, V. A., Smirnova, I. A., Moryakova, S. A., & Kardo-Sysoev, A. F. (2002, June). New generation of drift step recovery diodes (DSRD) for subnanosecond switching and high repetition rate operation. In Conference Record of the Twenty-Fifth International Power Modulator Symposium, 2002 and 2002 High-Voltage Workshop. (pp. 441-444). IEEE.

[3] Sharabani, Y., Rosenwaks, Y., & Eger, D. (2015). Mechanism of Fast Current Interruption in p− π− n Diodes for Nanosecond Opening Switches in High-Voltage-Pulse Applications. Physical Review Applied, 4(1), 014015.

4.5 DSRD-Based Pulsed Power Source Systematic Topological Optimization

(Sourov Roy)

4.5.1 Problem Statement, Approach, and Context

Primary Problem: Drift step recovery diodes used in inductive energy storage (IES) and release pulse generators, when able to achieve ones of gigawatts in ones of nanoseconds, are large, heavy, and require liquid-based cooling systems to dissipate the excess heat they generate during operation; therefore rendering them impracticable for Navy afloat missions.

Solution Space: Systematically develop a modular architecture of a pulser circuit using DSRDs by determining the optimal permutation of series and parallel combinations of the base pulser unit, and its component parameters, in order to maximize the peak voltage, peak power, and volumetric power density without sacrificing the desired nanosecond risetime of the pulses generated nor requiring liquid-based cooling.

***Sub-Problem 1*:** Traditionally drift-step recovery diodes, or DSRDs are manufactured OCONUS and are difficult to procure. Domestically manufactured (U.S.-based) DSRDs are not matured enough (sub-optimal doping profile) and there exists a large sample-to-sample parameter variability. In addition, SPICE models of these diodes are not accurate and do not account for their sample-to-sample parameter variability. The above-mentioned reasons may lead to an inaccurate simulation model of the pulser that may result in a difference between the simulation and experimental results.

Sub-Problem 2: The performance of DSRD pulse generator is considerably impacted by the forward pumping current and its influence on the reverse current interruption. Moreover, the optimum forward pumping current and the corresponding reverse current interruption are governed by the LC oscillation of the associate Rayleigh PFN and the ongoing recombination of the diode's free carriers. However, the general solution of Rayleigh PFN tends to become complicated progressively with an increasing number of series-parallel permutations of the base pulser unit. Therefore, deriving the mathematical modeling of the series-parallel permutation of the IES storage and release topology for the simulation and analysis of its parameter space is not time-and cost-effective. Inaccurate DSRD spice model and large sample-to-sample parameter variability further escalate the complexity of the model derivation.

State-of-the-Art (SOTA): Large pulsers ($\geq$1-m^3, $\geq$300-kg) that are comprised of sixteen parallel-branches of semiconductor opening switches (SOS, s.c., DSRD relatives) can achieve a voltage gain factor of ~33 (i.e., power amplification level ~9.5 dB) by producing 400 kV pulse amplitudes across a 100 Ω load with full-width half-maximum (FWHM) values of 60 ns. Pulse repetition frequencies up to 4 MHz have also been produced across similar load values. Smaller DSRD-based pulsers (equivalent in size to the pulse generators developed for this effort, i.e., ~0.01-m^3, ~2-kg) are able to achieve 6-kV, 200-ps risetime, and <500 ps FWHM across a 50 Ω load.

Deficiency in the SOTA: The large SOS-IES pulse generators which can achieve the foregoing performance parameters are traditionally limited by mechanical design constraints (onboard itinerant vehicles) and power supply limitations, are large (case

lengths <1 m), and require transformer oil for cooling purposes, which lead to undesirable system mass values up to 300 kg. The smaller DSRD-based air-cooled versions are limited to PRFs of < 15 kHz. Additionally, current studies on SOS-IES pulse generators attempt to present only the best-case circuit configurations meaning a comprehensive study on optimizing the number and ratio of parallel branches and series-connected stages aiming to achieve maximum gain and efficiency (reducing thermal load) is missing in the SOTA.

Solution Proposed: Systematically determine topological SOS-IES circuit configurations and the necessary components therein that maximize voltage gain and efficiency and minimize the rise-time achieved by the pulser.

Relevance to OSPRES Grant Objective: IES pulse generators using DSRDs can remove the need for photo-triggered switches and their laser sub-systems. They are ideal for triggering sub-nanosecond rise-time sharpeners (SAS, D-NLTL, etc.), reducing overall cost, volume, and weight.

Risks, Payoffs, and Challenges:

Risks: Domestically manufactured (U.S.-based) DSRDs which possess sub-optimal doping profiles may lead to sub-optimal pulse generators with sub-optimal performance. The data gathered from these sub-optimal circuits would then be used to train the genetic/machine learning algorithms developed and the redesign of future topologies constructed; ultimately leading to spurious conclusions regarding ideal topological circuit configurations with ‘N’ number of series-connected stages, each containing ‘M’ parallel branches.

Payoffs: Leveraging collaborative partnerships with U.S.-based manufacturers of DSRDs, the ability to refine and control the performance characteristics of the diodes themselves, along with the ability to simulate and manufacture the DSRD pulsers in-house, enables a holistic soup-to-nuts capability to optimize, produce, and evaluate these nanosecond pulse generators.

Challenges: Determining the superlative ratio of design/development (through numerical analysis) to the effort put towards experimental testing/evaluation of the DSRD pulser is challenging due to the novelty of the approach. The complexity of the theoretical model is extreme given the M×N number of DSRD base unit stages within the pulse forming network along with inaccurate DSRD spice model and large sample-to-sample variability.

4.5.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Construct/demonstrate a DSRD-based 2×2 IES pulse generator prototype capable of producing ≥4 kV peak voltage, ≤1 ns risetime, ≤5 ns FWHM, ≥320 kW peak-power, ≥1 kHz PRF, ≥100 shots-per-burst, ≥5 number of bursts [***Completed JUL21***].

(B) Milestone – Construct/demonstrate a DSRD-based 4×2 IES pulse generator prototype capable of producing ≥12 kV peak voltage, ≤1 ns risetime, ≤5 ns FWHM, ≥2 MW peak-power, ≥1 kHz PRF, ≥1,000 shots-per-burst, ≥500 number of bursts [*Ongoing, estimated completion by AUG21*].

1. Task – Work with TCAD simulation team (see Section 3.6) to compare-to, revise/update diode simulation model towards achieving refined and accurate diode performance and pulse generator circuit simulation output [***Ongoing–JUL21***];
2. Task – Refine and simulate circuit topological permutation(s) to include an increased number of parallel branches within an electrically optimal layout using Altium [*JUL–AUG21*];

(C) Milestone – Construct/demonstrate a DSRD-based 1×1 IES pulse generator prototype capable of testing individual and combinations of diode stacks to acquire performance data [*Ongoing, estimated completion by SEP21*].

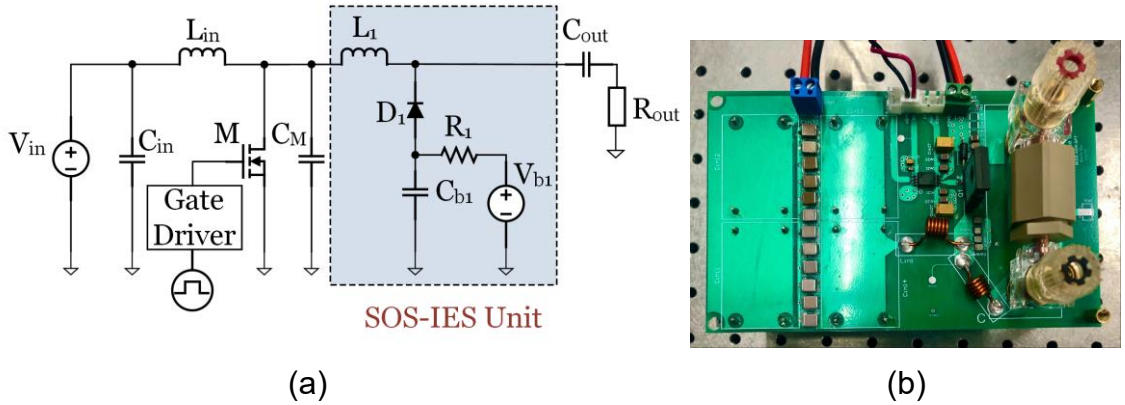
1. Task – Acquire data [***Ongoing–XXX21***];
2. Task – Refine and simulate circuit topological permutation(s) to include an increased number of parallel branches within an electrically optimal layout using Altium [*JUL–AUG21*];

(D) Milestone – Construct/demonstrate a M×N pulse generator prototype capable of producing $\geq$20 kV peak voltage, $\leq$1 ns risetime, $\leq$2 ns FWHM, $\geq$8 MW peak-power, $\geq$1 kHz PRF, and $\geq 2\sigma_{Vpeak}$, which operates in continuous-burst mode as a viable candidate for OSPRES Contract source alternative [*on hold until Milestone B is completed*].

(E) Milestone – Construct/demonstrate a 8×2 pulse generator prototype capable of producing $\geq$48 kV peak voltage, $\leq$1 ns risetime, $\leq$2 ns FWHM, $\geq$46 MW peak-power, $\geq$10 kHz PRF, $\geq 2\sigma_{Vpeak}$, $\geq$10,000 shots-per-burst, with a $\geq$50% duty cycle [*on hold until Milestone C is completed*].

4.5.3 Progress Made Since Last Report

(C) The 1×1 DSRD-based pulse generator (base-unit) with a custom-designed cylindrical DSRD clamp/housing has been tested in the laboratory in order to evaluate the performance of the DSRDs of the new lot received from LLNL. The schematic diagram and the photograph of the 1×1 DSRD-based pulse generator are shown in Figure 4.5.1. The pulser circuit was tested using different series-combinations of 7-stack diodes. Furthermore, another set of 1×1 DSRD-based pulse generator PCB board has been populated with required components and sent it to RDT Inc.



(a) (b)

Figure 4.5.1. (a) Schematic diagram and (b) photograph of the 1×1 DSRD-based pulse generator (base-unit).

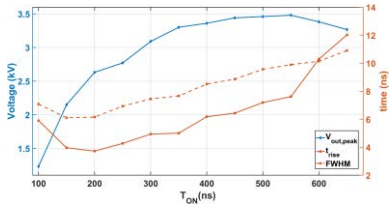


Figure 4.5.2. Resulting peak voltage, risetime and FWHM achieved as a function of trigger length (T_{ON}) utilized in the 1×1 DSRD-based SOS-IES pulse generator using "7-stack DSRD: A".

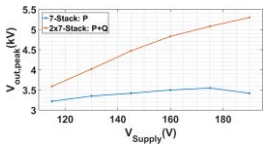
4.5.4 Technical Results

(C) Total six sets of 7-stack DSRDs were used in the pulser circuit where they are denoted as "A", "B", "C", "D", "P", and "Q", respectively. First, the 1×1 DSRD-based pulse generator (base-unit) circuit using "7-stack DSRD: P" was tested to perform a parametric study varying the ON time of the trigger signal (T_{ON}) while keeping the V_{Supply} constant (=115V). The resulting peak voltage ($V_{out,peak}$), risetime (t_{rise}; 10%-90%) and FWHM were recorded while increasing T_{ON} from 100–650 ns. The obtained results are presented in Fig. 4.5.2. As shown in this figure, $V_{out,peak}$ increases and then decreases whereas t_{rise} as well as

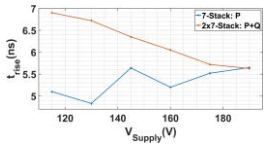
FWHM decrease and then increase with the increasing T_{ON} which is in accordance with the 2×2 DSRD-based pulse generator test results.

Figure 4.5.3 shows the trend in $V_{out,peak}$, t_{rise} and FWHM with variation in the V_{supply} while T_{ON} was kept constant at 340-ns for the 1×1 DSRD-based pulse generator using both "7-stack DSRD: P" and "2x7-stack DSRD: P+Q". From 4.5.3 (a), it can be seen that $V_{out,peak}$ of both 7-stack and 2x7-stack diode-based pulser follow the same trend with increasing V_{supply}, however, the latter produce much higher $V_{out,peak}$ for a given V_{supply}. A possible explanation for this might be that 7-stack diode-based pulse generator output has a lower breakdown voltage compared to that of the 2x7-stack diode-based pulse generator and therefore, it reaches its breakdown voltage limit earlier. Please note that the breakdown voltage of a single diode is limited to about 1 kV meaning the breakdown voltage of a 7-stack diode should be 7 kV. However, due to passivation, heating and other non-ideality effects, the diode breakdown voltage is unstable and drops during diode operation in pulser circuit (please refer to section 4.3). We also observe from Figure 4.5.3 (b) and (c) that both t_{rise} and FWHM of the 7-stack DSRD-based pulse generator output pulse increase and the same of the 2x7-stack DSRD-based pulse generator output pulse decrease with increasing V_{supply}. This discrepancy could be attributed to the difference in the Rayleigh PFN (RLC circuit) of the forward pumping path pertaining to 7-stack and 14-stack DSRD. Interestingly, the rise-time of the 14-stack DSRD-based pulser output is much higher than that of the 7-stack DSRD-based pulser output for a given V_{Supply}. The addition of parasitic inductance and capacitance due to loose stack (kept by mechanical pressure) of two sets of series-connected 7-stack diodes might be resulted in the pulse front to lose its sharpness. In addition, the rise-time and FWHM of the 1×1 DSRD-based pulse generator output are comparatively higher than that of the 2×2 DSRD-based pulse generator output and we envision that this is due to the additional parasitic inductive, capacitive, and resistive elements of the customized DSRD clamp/housing in the equivalent circuit of the PFN network. Based on the abovementioned observations, it can be infered that the peak voltage increases and the risetime decreases with the increasing V_{supply} as we add the number of diode stacks.

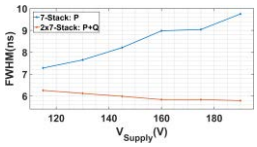
Later, the 1×1 DSRD-based pulse generator (base-unit) circuit was further tested in order to confirm the observed trends in Figure 4.5.3 for multiple stacks of different diodes. The resultant $V_{out,peak}$ and t_{rise} with variation in the V_{supply} while T_{ON} was kept constant at 340-ns are plotted in Figure 4.5.4 (a) and (b), respectively. However, it is evident from these plots that although adding two 7-stacks DSRD increases peak voltage and decreases risetime with the increase in V_{supply}, further addition of 7-stack DSRDs upto 3-or-4 stacks does not guarantee the trend.



(a)

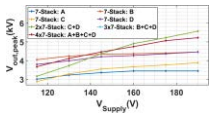


(b)

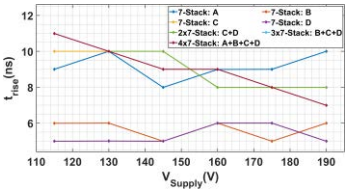


(c)

Figure 4.5.3. Resulting (a) peak-voltage, (b) risetime, and (c) FWHM achieved for "7-stack DSRD: P" and "2x7-stack DSRD: P+Q" as a function of supply voltage utilized in the 1×1 DSRD-based pulse generator.



(a)



(b)

Figure 4.5.4. Resulting (a) peak-voltage and (b) risetime for multiple series combinations of 7-stack DSRDs as a function of supply voltage (utilized in the 1×1 DSRD-based pulse generator).

4.5.5 Summary of Significant Findings and Mission Impact

(A) Successful construction and operation of a 2×2 DSRD-based IES pulse generator prototype has been completed which meets or exceeds the milestone's required key

performance metrics. Shown in Table 4.5.1 are the previous and current pulse generator's performance specifications in comparison to a similar 2×2 pulser developed by Kesar et al. [1] using DSRDs, and to that of a commercial off-the-shelf (COTS) DSRD pulser of similar space and weight developed by Megaimpulse (i.e., PPM-0731) which also uses DSRDs with silicon avalanche shapers (SAS) [2]. Although the Megaimpulse pulser utilizes a SAS with a <500 ps risetime (a threshold we do not intend to go below due to Commerce Controlled List limitations), it is interesting to compare the results of linear voltage gain and peak power of this system, to that of one that utilizes a SAS.

Table 4.5.1 Comparison of DSRD-based IES Pulse Generator Performance

KPM	**Units**	**MIDE - V1** Previous	**MIDE - V2** Current	**Kesar *et al.*** SOTA	**MI-PPM0731** COTS
V_{supply}	V	225	180	300	160
T_{ON}	ns	100	340	?	200
V_{peak}	kV	5.59	**7.35**	5	6.3
Gain	V/V	24.8	**40.8**	16.7	39.4
$\tau_{rise,20\text{-}90\%}$	ns	1.2	1.142	1.96	0.12
dV/dτ	kV/ns	4.66	6.44	2.55	**52.50**
FWHM	ns	2	5.48	2.27	0.35
PW	ns	5	7	3.5	2.5
Z_{LOAD}	Ω	50	50	50	50
P_{peak}	MW	0.625	**1.080**	0.500	0.794
E_{pp}	mJ	0.125	0.154	0.143	0.318
PRF_{max}	kHz	100	100	100	15
Burst	shots	100	100	*N/A*	100
	%	100	100	*N/A*	100
SD_{Vpeak}	σ	> 2	**> 2**	*N/A*	*N/A*
	%	96.5	**97.8**	*N/A*	*N/A*

The current permutation of the 2×2 SOS-IES pulser developed by MIDE under the ONR OSPRES Grant is able to achieve a higher peak voltage and shorter risetime than DSRD-based pulsers reported in the literature of comparable space and weight as well as those commercially available. The ability to generate a linear voltage gain of 40.8 to produce over a Megawatt of peak power into a 50 Ω load while achieving a peak voltage output standard deviation of 2σ when operating at a PRF of at least 100 kHz, brings this technology to the forefront of viable options to potentially support the Naval afloat mission.

(C) Discrepancies exist in the obtained data for different series combinations and different samples of 7-stack DSRDs which may be attributed to the inconsistencies in their manufacturing process. Future works in the coming months include carrying out

further testing on the 1×1 DSRD-based pulse generator (base-unit) circuit using more combinations of series-connected as well as parallel-connected DSRD stacks.

4.5.6 References

[1] https://www.onsemi.com/pdf/datasheet/nvh4l020n120sc1-d.pdf

[2] https://cms.wolfspeed.com/app/uploads/2020/12/C2M0045170P.pdf

4.6 Optimizing SOS-IES Pulse Generator Performance with Machine Learning

(Dewan Noor and Sourov Roy)

4.6.1 Problem Statement, Approach, and Context

Primary Problem: For the majority of HPM-based pulse generators, it is easier to find out the relation between the waveform output parameters produced, (e.g. peak voltage, rise time) and the input parameters utilized to achieve them (e.g. charge voltage, bias capacitors, bias voltage, snubber capacitor, trigger time etc. of a single cell). However, for the DRSD-based pulser, multiple input parameters exist within each M×N stage of the pulse generator's circuit when increasing the number of cells (i.e., stages) in series, and parallel branches thereof, to achieve the desired output beyond what is possible with a single cell. Here, statistical correlations between the non-linear separable data of the multiple component's characteristics and the pulser's performance is ill-suited for traditional linear regression methods.

Solution Space: To develop an accurate model which correlates the non-linear relationship between the input and output parameters of the M×N stages comprising the pulse generator's circuit, we need to explore machine learning (ML), deep learning, and artificial intelligence methodologies to generate training data and determine the shape of the underlying statistical model with minimal error.

***Sub-Problem 1*:** Machine learning algorithms such as K-nearest neighbor (KNN) and random forest require 'big data' sets to train the model towards optimizing the parameters for desired pulser topology. Manually gathering both experimental and numerical data to train the ML model is time consuming, computationally expensive, and requires a large amount of memory to store the data acquired.

Sub-Problem 2: Individual datasets from experiments or simulations has its own unique output metrics pattern(s). Hence, each one will behave differently while training a certain machine learning algorithm. Therefore, the training model might act complete different while using a testing dataset if it is not from the same set of experiments (e.g., a training sample from the simulation and testing sample from the experimental setup). So, testing with the experimental model data may produce a different outcome than the result achieved by training the ML model using simulation data.

Sub-Problem 3: A similar type of problem to that of Sub-Problem 2 arises while choosing correct machine learning algorithm for a certain solution to generate the relationship between input and output parameters. Dataset's patterns can be altered by increasing the number of parameters as the number of M parallel branches in N series is increased.

Therefore, a supervised ML algorithm (e.g., random forest, K-nearest neighbors) might work well for smaller number of stages but mat not produce statistically correlated results as the number of stages is altered; ultimately causing variations in the patterns of the existing variables.

State-of-the-Art (SOTA): To characterize the relation among the multiple components of each M-parallel and N-series connected stage of the pulse generator's circuit, non-machine learning approach e.g. genetic algorithm and polynomial regression are mostly usually applied to optimize the parameters if they are not linearly correlated. Polynomial regression with higher degree often generates a relation among the input and output parameters. Hence, they also take less time and space complexity.

Deficiency in the SOTA: Genetic algorithm and polynomial regression often fail if the variables are not mutually exclusive. Their interdependency usually overfit the data within their certain range. So, when we want to establish the relationship for higher number of M and N (multiple stages), the more the interdependency among the variables, the less effective the algorithm would be. Hence, the model is bound to fail in the end.

Solution Proposed: In order to train the model with certain parameters, we need to find out the top (i.e., most relevant, and statistically significant) parameters/features contributing most towards the circuits output. A machine learning algorithm e.g., random forest (RF), K-nearest neighbor (KNN), etc., can be used or the feature selection method using the dataset with variable sweeping of the input parameters (Input voltage, biasing voltage, capacitance, inductance etc.) for the output parameters (Peak voltage, rise time etc.). Once the top features are selected, those selected parameters can be trained against a machine learning algorithm for a certain desired output. Hence, we can find the optimized value of the parameters for out desired output parameters.

Relevance to OSPRES Grant Objective: DSRD-based IES pulse generators with desired output which leverage a circuit topology design modeled by a machine learning algorithm can remove the need for photo-triggered switches and their laser sub-systems without reducing the desired peak power levels required. This leads to increases in SWaP metrics by reducing overall cost, volume, and weight.

Risks, Payoffs, and Challenges:

Risks: The model generated from machine learning algorithm using the simulated training dataset might have high bias if the generated sample size is of low volume. On the other hand, the variance may be high if we try to generate high volume data using data augmentation algorithm like bootstrapping or k-fold cross validation. The tradeoff between bias and variance are somewhat a risky assignment to take care of while applying the machine learning algorithm.

Payoffs: If the loss ratio between training and testing dataset is kept minimal with maintaining a certain volumetric unbiased and low-variance data, the input parameters can be optimized for the desired output.

Challenges: The main challenge is to maintain the trained model's stability from the beginning of training the ML model, to the testing dataset. Specifically, the testing dataset is basically the data generated from the experimental setup which uses circuit

components having variations in manufacturing and having different models than the simulated components. Hence, the algorithm should be able to forecast the trend of behavioral patterns among the components and variance between components which are alike.

4.6.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Automated script generating thousands of LTSpice simulations in Python in the batch mode to accumulate large volume of data for model training developed [***Completed JUL21***].

(B) Milestone – Machine learning model utilizes feature selection method to determine the statistically significant input parameters and their optimal/maximum values peak voltage/rise time [***Completed JUL21***].

(C) Milestone – Sweep the top features/input parameters contributing most towards peak voltage/rise time and find out the trend. [*estimated completion by OCT21*].

1. Task – Select the top features to sweep after being computed from the feature selection method and prepare the script [*JUL–SEP21]*
2. Task – Generate the trend of the top peak voltage/rise time varying the top selected features. [*AUG–OCT21]*

4.6.3 Progress Made Since Last Report

(C) Using the feature selection method, top features among the input variables are studied. A plan has been discussed and, in the process, to sweep the input variables from their priority list acquired from the feature selection method. From the feature selection result, ON time of the trigger signal has been found the most import parameter. Bias voltage and supply voltage are found as the next parameters of interest. As snubber capacitor and series inductance are less important found from previous study in milestone B, they are to varied last.

4.6.4 Technical Results

(C) The experiment and the simulation to carry out the plan for the milestone C are in progress. The results will be achieved after we carry out milestone C successfully.

4.6.5 Summary of Significant Findings and Mission Impact

(A-B) The Python automated script generation is completed marking the completion of milestone A. Feature selection method is applied to find out the top features contributing towards the output marking the completion of milestone B. Milestone C is in progress with the completion of task-1 to vary the important features and modify the script accordingly.

(C) As we have the important features selected from the input parameters list, the simulation to sweep the important variables can show us a range of values as the design parameters to get the desired output .

4.7 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners

(Gyanendra Bhattarai)

4.7.1 Problem Statement, Approach, and Context

***Primary Problem*:** Broadband high-power microwave (HPM) systems need sub-nanosecond tens-of-MW pulses. Hydrogen spark gaps (HSG), traditionally used for such purposes, are severely limited by their low pulse repetition frequency (PRF ~1 kHz) and poor device lifetime (shot life ~1000 pulses), ill-suited to achieve the SWaP metrics necessary for HPM pulse generators for the Navy afloat mission. Competitive solid-state solutions, such as Inductive energy storage (IES) systems, utilizing a series stack of fast-opening diodes (drift-step recovery diodes (DSRD) and semiconductor opening switches (SOS)), are not shown to break nanosecond barriers.

***Solution Space*:** Use viable pulse shaping/compression technologies based on semiconductor closing switches (e.g., delayed breakdown diodes (DBD), and fast ionization dynistors (FID)) to increase the peak power and shorten the rise time of the pulses produced by the DSRD-based pulse generator. Pulse sharpening/compression reduces the otherwise additional complexity of increased M×N stages within the pulser's topology; a desired result towards achieving optimal SWaP metrics of the pulse generation system without sacrificing PRF, shot lifetime, and thermal management requirements. (*Please refer to the June 2021 MSR for full problem and solution space description).*

***Sub-Problem 1*:** Achieving an order of magnitude increase in peak power (1-to-10 MW) through compression/sharpening methods requires series and parallel stacks of semiconductor closing switches (SCS) ultimately resulting in increased pulse risetime. Determining the optimal combination of diode stacks to decrease pulse risetime and increase output power requires additional SPICE circuit simulations. However, device models for SCS are not commercially available and thus require maturing SCS device models based on experimental results and physics-based simulations, such as using packages such as T-CAD, which can be time consuming.

***Sub-Problem 2 (Fundamental Physics)*:** Sub-nanosecond high-power pulse sharpening using semiconductor devices is based on ultrafast delayed avalanche breakdown under steeply increasing reverse voltage applied, thereby initiating an impact ionization front. However, the phenomenon behind the origin of free carriers that trigger the impact ionization at higher-than-breakdown fields is not completely known. Further, it is not clear whether the switching (generation of electron–hole plasma) is uniform across the device area or is localized (filamentary). Such different mechanisms are believed to be dependent on device geometry and doping concentration, and are detrimental to the switching speed. A University of New Mexico study [1] has concluded that the operation of a silicon avalanche shaper (SAS) is inconsistent with the theory described by Russian scientists. More understanding of device operation from a fundamental physics perspective is necessary to enhance their performances.

***State-of-the-Art (SOTA)*:** Prototype sub-nanosecond solid-state pulsers based on semiconductor opening switches (SOS) and semiconductor sharpeners are shown to

produce peak voltages (~500 kV), and peak power outputs (~5 GW). Solid-state power supplies providing peak power up to 800 MW are available to purchase from FID Technologies, Germany. *Please refer to Table 4.7.1 of the June MSR for list of devices and their performance metrics.*

***Deficiency in the SOTA*:** Prototype ~5 GW power supplies, such as SOS based S-500 system with semiconductor sharpeners, are large (>1 m^3). Commercially available moderate-power (~1 GW) all solid-state pulsers utilizing semiconductor sharpeners have long purchase lead time (~4 months). Their PRF capability is limited to ~1 kHz due to physical constraints in thermal management.

***Solution Proposed*:** Downselect viable pulse compression/shaping technologies which meet or exceed the performance parameters set forth in Section 4.5's Milestones A-D towards produce an all-solid-state, tens-of-megawatts, sub-nanosecond pulse generator with semiconductor sharpener without sacrificing PRF, shot lifetime, and thermal management requirements.

***Relevance to OSPRES Grant Objective*:** The alternative all-solid-state technologies discussed could individually, or in combination, provide the means to produce order(s) of magnitude greater peak power, without severe limitation to PRF, as SWaP-centric means to increase the capability and extent of protecting naval assets.

Risks, Payoffs, and Challenges:

***Risks*:** Semiconductor closing switches, such as DBD and FID are not available to purchase within the United States. Procuring devices from abroad could lead to significant delay in experiments and development of device fabrication technology. Undergoing time-intensive and complex simulations to then down-select one technology based on peak power output alone presents risk to other secondary or tertiary performance metrics such as PRF and pulse energy, which risks developing ill-suited technologies to support the float mission. Additionally, as new technology emerges via research, scope creep to numerically and experimentally evaluate new technologies may delay transitioning these technologies into viable systems.

***Payoffs*:** The SWaP tradeoff of generating a non-laser-based system with any number of these systems can yield a higher fidelity pulsed-power waveform output. Determining which technology is viable and feasible in terms of the key performance metrics should yield a more ultracompact form factor pulse generator with order(s) of magnitude greater power density without compromise to overall size and weight to the system.

***Challenges*:** Determining the true performance metrics of interest based on these highly different devices is challenging. Without a more robust and deep understanding of their operation, and how to utilize them within a pulse generator topology, in a swappable configuration or otherwise, requires additional time and consideration. Managing the tradeoff between the academic understanding of the technologies of interest presented in the foregoing table, and the transition to prototype effort/mentality, will require both a delicate balance and leveraging the pulsed-power team's combined effort.

4.7.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Downselect viable pulse compression/shaping technology to be used in addition to currently utilized DSRD, which increases at least one of the key performance metrics by an order of magnitude without compromise to the overall volume of the system [*Estimated completion by AUG21*].

1. Task – Finalize literature study of different technologies and topologies of SCS based pulse generators and compare SWaP tradeoff evaluation to PCSS- and DSRD/SOS-based pulse generators [*JUN–JUL21*]; [*behind schedule*]
2. Task – Determine commercially available technologies that could be used as pulse shaper/sharpening devices to improve pulse generator performance, and select appropriate devices for further experimental verification of their performance metrics [*JUN–AUG21*]; [*behind schedule*]

(B) Milestone – Model and experimentally verify the performance of the downselected technology as an additional component to the DSRDs utilized within a SOS-IES pulse generator. [*Estimated completion by NOV21*].

1. Task – Develop T-CAD device model for the selected devices (DBD/ DLD) based on available device information from literature and perform device simulation for their performance under nanosecond input pulse conditions. *[SEP–OCT21]*;
2. Task – Develop Spice device model for the selected device based on T-CAD simulation. [*SEP-OCT21*]
3. Task – Design experimental circuit with one selected diode or dynistor and obtain theoretical performance metrics using standard electronic simulation tools such as LT-Spice using the device model developed in task 2. [*SEP–NOV21*];
4. Task – Experimentally verify whether the selected device topology can produce peak power and pulse risetime equivalent to or better than that of SOTA. [*OCT–NOV21*];

(C) Milestone – Model diode/dynistor topologies and fabrication process. [*on hold until Milestones A and B are completed*].

1. Task – Model silicon diode and dynistors, with optimized device cross section (size, geometry) based on theory and simulations to increase current and thermal dissipation. [*OCT–NOV21*];
2. Task – Model/design fabrication process with optimum device topology and doping concentration. [*NOV–DEC21*]

4.7.3 Progress Made Since Last Report

(A.1) Additional scientific literature on semiconductor pulse sharpeners has been reviewed. A brief review of semiconductor pulse sharpening is given below.

Delayed Impact ionization Breakdown: When semiconductor structures, such as diodes and dynistors, are overvolted in reverse bias within a few nanoseconds, the delayed breakdown starts at higher than stationary breakdown voltage. The

breakdown is termed as ‘delayed’ in a sense that the breakdown does not start at the time when the applied voltage reaches the stationary breakdown voltage. As the applied voltage approaches twice the stationary breakdown voltage, the free carriers present in the depleted region acquire sufficient energy to initiate impact ionization. An ionization front propagates through the device at a speed much faster than the saturation velocity of the carriers, thereby filling the whole device with dense electron-hole plasma within 100s of picoseconds.

Although delayed impact ionization breakdown has been observed in devices and are being actively researched in wide-band high-power microwave systems, the origin of initial carriers in the depleted structure is an unsolved problem in physics. Mechanisms such as thermal generation, ionization by majority carriers in undepleted part, and Zener tunneling are not found to be responsible for delayed breakdown [2]. As delayed breakdown has also been observed in devices without deep electron traps, the possible mechanisms for the initial carriers are considered as field-enhanced ionization of deep electron traps, surface deep level assisted band-to-band electron tunnelling –– resulting in even faster filamentary breakdown, electron injection from non-ideal contact of the metal electrode and p^+ layer initiated by dV/dt-effect, and complex combination of two or more mechanisms.

Delayed Breakdown Diode (DBD): Semiconductor devices of different structures containing one p-n junction, such as p^+-n-n^+ and p^+-p-n-n^+, with different layer thickness and doping profiles have shown to exhibit delayed impact ionization breakdown when they are overvolted by nanosecond pulses. Such diodes are generally termed as delayed breakdown diodes (DBD). Delayed breakdown has been observed in silicon and GaAs diodes. However, because of superior performance of silicon diodes compared to GaAs, they are now widely used in sub-nanosecond high power pulse sharpening and are known as silicon avalanche sharpeners (**SAS**). Sometimes, the term SAS has also been used as a collective name for semiconductor avalanche sharpeners, which may include diodes, dynistors, and thyristors.

In silicon avalanche sharpeners, both structures (p^+-n-n^+ and p^+-p-n-n^+) can achieve steep current ramp, however, the residual voltage in the later remains at ∼1 kV compared to ∼200 V in the former [3]. This results in much lower power delivery to the load and increased heat dissipation in the diode, making p^+-n-n^+ structure preferable.

Fast Ionization Dynistor (FID): Semiconductor devices containing two p-n junctions in series, such as p^+-n-p-n^+ and p^+-p-n-p-n^+, which undergo delayed impact ionization under overvolted conditions are known as fast ionization dynistors (FID). Conventional FIDs have generally wide n-base regions compared to other doped regions so that when a small constant reverse bias is applied, the space-charge region (SCR) formed remains localized in the vicinity of p-n junctions. When a sufficiently high reverse voltage is applied, the impact ionization is initiated by the majority carriers. As holes are created due to ionization, they migrate towards the higher electric field SCR region and initiate impact ionization

front, thereby filling the n-base with dense electron–hole plasma and increasing the conductivity sharply within 100s of picoseconds. As dynistor, by their nature, are bistable devices due to a feedback mechanism (similar to a p-n-p and a n-p-n transistor combined), once the dynistor turns on, it remains conducting, however with much higher residual voltage compared to DBDs.

Deep Level Dynistor (DLD): conventional FIDs have large residual voltage due to their thick n-base region required for initiation of the impact ionization. Deep level dynistors (DLD) are modern variation of FIDs where the n-base region is made significantly thinner, however, the initiation of the impact ionization is achieved via field enhanced ionization of deep electron traps. Thus, DLD is referred as FID in many articles. Because DLDs remain in conducting state once they are turned on, eliminating the time of current passage, and retain lower residual voltage, stacks of DLDs have been used to achieve as high as 5 GW peak power sub-nanosecond pulse generator by IOFFE.

(A.2) Based on the review of semiconductor pulse sharpening technologies, sharpening the output pulses from DSRD/SOS based pulsers using DBD (p^+-n-n^+) and DLD are identified as the best alternatives to hydrogen spark gaps, which can produce comparable pulsed power, with shorter pulse risetime and higher PRF. Delayed breakdown diodes (DBD) and DLD can be acquired, however, from Russia.

(B.1) Silvaco TCAD license is being renewed and a simulation workstation is being configured. TCAD simulation and device modeling materials are being reviewed.

4.7.4 Technical Results

(A) Based on the review materials [2]–[18], the ranges of peak power and risetime of different switches is presented in Figure 4.7.1.

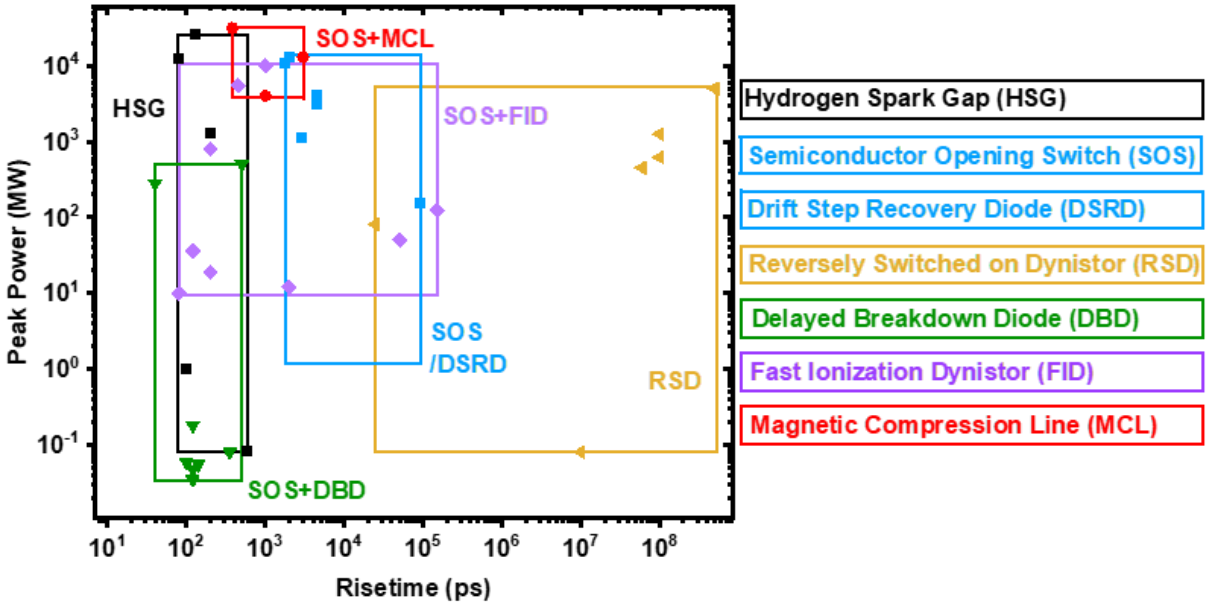


Figure 4.7.1 Ranges of peak power and pulse risetime of different types of high-power switches.

(B) DSRD (p^+–n–n^+) and SOS (p^+–p–n–n^+) are [ideally] similar to different structures of delayed breakdown diodes (DBD). The only difference between them is their working principles. DSRD and SOS pulsers need a forward pumping current and their switching is based on extracting the injected charge, while DBDs work completely on reverse bias by switching these devices due to the delayed impact ionization by a steep reverse voltage rise rate of ∼10 kV/ns. In presence of certain process-induced (PI) defect states in silicon, they are switched by voltage pulses with rise rate of ∼1–2 kV/ns. Therefore, we can at least try a single DSRD or SOS die in a DBD configuration to test pulse sharpening performance given that power switches producing about 3 kV with 10kV/ns rise rate are available.

4.7.5 Summary of Significant Findings and Mission Impact

(A) No single technology appears to meet or exceed the key performance metric requirements across the board. Where HSG lead in peak voltage and peak power, in comparison to the other technologies of interest, they lack in their ability to meet the required PRF, device lifetime, and SWaP-C metrics. All solid-state switching power supplies utilizing SOS and semiconductor sharpeners seem viable technology to compete against HSG with comparable or better SWaP-C metrics.

4.7.6 References

[1] E. Schamiloglu, C. B. Fleddermann, R. Focia, and J. Gaudet, “A STUDY OF ADVANCED SEMICONDUCTOR SWITCH PHYSICS AND TECHNOLOGY PHILLIPS LABORATORY Advanced Weapons and Survivability Directorate AIR FORCE MATERIEL COMMAND KIRTLAND AIR FORCE BASE, NM 87117-5776,” 1997.

[2] V. Brylevskiy, I. Smirnova, A. Gutkin, P. Brunkov, P. Rodin, and I. Grekhov, “Delayed avalanche breakdown of high-voltage silicon diodes: Various structures exhibit different picosecond-range switching behavior,” *J. Appl. Phys.*, vol. 122, no. 18, 2017, doi: 10.1063/1.5004524.

[3] V. I. Brylevskiy, I. A. Smirnova, A. V. Rozhkov, P. N. Brunkov, P. B. Rodin, and I. V. Grekhov, “Picosecond-Range Avalanche Switching of High-Voltage Diodes: Si Versus GaAs Structures,” *IEEE Trans. Plasma Sci.*, vol. 44, no. 10, pp. 1941–1946, 2016, doi: 10.1109/TPS.2016.2561404.

[4] S. Schneider and T. F. Podlesak, “Reverse switching dynistor pulsers,” *IEEE Trans. Plasma Sci.*, vol. 28, no. 5, pp. 1512–1519, 2000, doi: 10.1109/27.901224.

[5] I. V. Grekhov, A. K. Kozlov, S. V. Korotkov, I. A. Rol’nik, and A. L. Stepanyantz, “A High-Voltage Reverse Switch-on Dynistor Switch with a Transistor Control Circuit,” *Instruments Exp. Tech.*, vol. 45, no. 5, pp. 679–681, 2002, doi: 10.1023/A:1020466420755.

[6] P. Rodin, A. Minarsky, and I. Grekhov, “Impact ionization fronts in semiconductors: Numerical evidence of superfast propagation due to nonlocalized preionization,” *J. Appl. Phys.*, vol. 108, no. 3, pp. 9–11, 2010, doi: 10.1063/1.3465302.

[7] A. I. Gusev, S. K. Lyubutin, S. N. Rukin, B. G. Slovikovsky, and S. N. Tsyranov, “On the picosecond switching of a high-density current (60 kA/cm2) via a Si closing switch based on a superfast ionization front,” *Semiconductors*, vol. 48, no. 8, pp. 1067–1078, 2014, doi: 10.1134/S1063782614080132.

[8] V. I. Brylevskiy, I. A. Smirnova, N. I. Podolska, Y. A. Zharova, P. B. Rodin, and I. V. Grekhov, “Picosecond-range avalanche switching of bulk semiconductors triggered by steep high-voltage pulses,” *IEEE Trans. Plasma Sci.*, vol. 47, no. 1, pp. 994–999, 2019, doi: 10.1109/TPS.2018.2875423.

[9] V. Brylevskiy, N. Podolska, I. Smirnova, P. Rodin, and I. Grekhov, "Picosecond-Range Avalanche Switching Initiated by a Steep High-Voltage Pulse: Si Bulk Samples Versus Layered pn Junction Structures," *Phys. Status Solidi Basic Res.*, vol. 256, no. 6, pp. 1–6, 2019, doi: 10.1002/pssb.201800520.

[10] C. E. Baum *et al.*, "JOLT: A highly directive, very intensive, impulse-like radiator," *Proc. IEEE*, vol. 92, no. 7, pp. 1096–1107, 2004, doi: 10.1109/JPROC.2004.829011.

[11] S. N. Rukin, "Pulsed power technology based on semiconductor opening switches: A review," *Rev. Sci. Instrum.*, vol. 91, no. 1, 2020, doi: 10.1063/1.5128297.

[12] V. M. Efanov, V. V. Karavaev, A. F. Kardo-Sysoev, and I. G. Tchashnikov, "Fast ionization dynistor (FID)-a new semiconductor superpower closing switch," in *Digest of Technical Papers. 11th IEEE International Pulsed Power Conference (Cat. No.97CH36127)*, 1997, vol. 2, pp. 988–991, doi: 10.1109/PPC.1997.674523.

[13] I. V. Grekhov and P. B. Rodin, "Triggering of superfast ionization fronts in silicon diode structures by field-enhanced thermionic electron emission from deep centers," *Tech. Phys. Lett.*, vol. 37, no. 9, pp. 849–853, 2011, doi: 10.1134/S1063785011090203.

[14] V. I. Brylevskii, I. A. Smirnova, P. B. Rodin, and I. V. Grekhov, "Subnanosecond avalanche switching in high-voltage silicon diodes with abrupt and graded p-n junctions," *Tech. Phys. Lett.*, vol. 40, no. 4, pp. 357–360, 2014, doi: 10.1134/S1063785014040166.

[15] C. A. Frost, R. J. Focia, T. C. Stockebrand, and M. J. Walker, "Multi-kilovolt solid-state picosecond switch studies," *IEEE Int. Conf. Plasma Sci.*, p. O1H7, 2001, doi: 10.1109/PPPS.2001.960861.

[16] S. K. Lyubutin, S. N. Rukin, B. G. Slovikovsky, and S. N. Tsyranov, "High-power ultrafast current switching by a silicon sharpener operating at an electric field close to the threshold of the Zener breakdown," *IEEE Trans. Plasma Sci.*, vol. 38, no. 10 PART 1, pp. 2627–2632, 2010, doi: 10.1109/TPS.2010.2045396.

[17] A. I. Bushlyakov *et al.*, "Solid-state SOS-based generator providing a peak power of 4 GW," *IEEE Trans. Plasma Sci.*, vol. 34, no. 5 I, pp. 1873–1878, 2006, doi: 10.1109/TPS.2006.881300.

[18] I. V. Grekhov, A. G. Lyublinskiy, and S. A. Yusupova, "High-power subnanosecond silicon avalanche shaper," *Tech. Phys.*, vol. 62, no. 5, pp. 812–815, 2017, doi: 10.1134/S1063784217050115.

4.8 Characterizing and Optimizing On-state Resistance in GaN:X PCSS

(Heather Thompson)

4.8.1 Problem Statement, Approach, and Context

Primary Problem: Traditionally, RF generation using photoconductive semiconductor switches (PCSS) have relied on materials such as silicon (Si) or gallium arsenide (GaAs), due to their availability and low cost; however, as these applications begin to require higher operating frequencies, powers, and temperatures, with the same or reduced system form-factor, the theoretical operating limits of these materials are being pushed up against.

Solution Space: By exploiting the 3.4 eV bandgap, 1000 cm^2/Vs electron mobility, and thermal properties of GaN, it is possible to realize pulsed-power applications requiring up to a 5 MV/cm critical field, high-frequency operation, and ~400 °C operating temperature, respectively.

Sub-Problem 1: One of the most important problems in minimizing conduction losses, maximizing efficiency, and reducing thermal issues in compensated, semi-insulating

GaN:X (i.e., GaN:X with X=C, Fe…) PCSS-based systems is achieving <1 Ω on-state resistance by optimizing the modifiable parameters of GaN:X at the material, device, and system levels.

***Sub-Problem 2*:** Due to lack of maturity in the manufacturing and commercial availability of GaN:X PCSSs, there is limited knowledge available about how to minimize the on-state resistance in these devices while still maintaining quick switch turn-off time and low turn-off losses leading to the need for a parametric study of what affects on-state resistance to be completed.

***State-of-the-Art (SOTA*):** PCSS-based RF generation systems using Si, SiC, or GaAs can achieve MW-range output power, ones-of-gigawatts frequency content, and electrical efficiency of ~60%.

***Deficiency in the SOTA*:** Si-, SiC-, and GaAs-based PCSS require ones-of-mJ of incident laser energy to achieve <1 Ω on-state resistance, leading to increased incident laser requirements, increased heating in devices, and devices that are ones-of-cm^2 in area for the peak power and operating temperatures needed.

***Solution Proposed*:** Use simulation and available experimental results, from literature and collected results at UMKC, to optimize the variable parameters of GaN:X PCSS to achieve <1 Ω on-state resistance while maintaining a quick switch turn-off time and low turn-off losses.

Risks, Payoffs, and Challenges:

***Challenges*:** The high cost of material leads to a limited number of devices available for experimental testing and analysis, requiring much of the optimization studies to be performed using simulation software (COMSOL and TCAD).

***Risks*:** Simulation results may vary from experimental results for certain PCSS parameters due to the need of an encapsulating material to prevent surface flashover in lateral GaN:X PCSS devices during high-voltage experimental testing, which may need to be accounted for.

***Payoffs*:** By minimizing the conduction losses in GaN PCSS, a compact, tunable RF source can be realized with increased efficiency and SWAP-C^2 capabilities.

4.8.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Determine material, device, and system parameters that affect on-state resistance and which of these can be best leveraged to reduce on-state losses and heating [*Estimated completion by OCT 21*].

1. Task – Literature study of photoelectric on-state resistance to understand how this parameter can be optimized to reduce conduction and on-state losses during PCSS operation *[SEPT–OCT21].*
2. Task – Literature review of on-state resistance studies performed using GaN-based photoelectric devices to determine areas to further study *[SEPT–OCT21].*
3. Task – Determine project milestones, tasks, and timeline for optimizing on-state resistance in GaN PCSS *[OCT21]*.

(B) Milestone – Build model of GaN PCSS in TCAD and/or COMSOL to begin simulation studies *[OCT–NOV21].*

4.8.3 Progress Made Since Last Report

(A) Literature pertaining to on-state resistance in opto-electric devices, of various semiconductor materials, has been collected and is being analyzed to determine the parameters at the material, device, and system levels that affect on-state resistance.

4.8.4 Technical Results.

(A) There are several parameters (Figure 4.8.1) that affect the on-state resistance of opto-electric devices at the material (bandgap, necessary activation energy, compensation concentrations, etc.), device (geometry, illumination location, etc.), and system (incident photon source characteristics, encapsulation material, etc.) levels that can be altered to minimize on-state resistance, with certain parameters being more easily manipulated than others. By finding out which parameters most affect the on-state resistance, how they relate to one another, and which are easily changeable, this will provide a starting point for optimizing these devices.

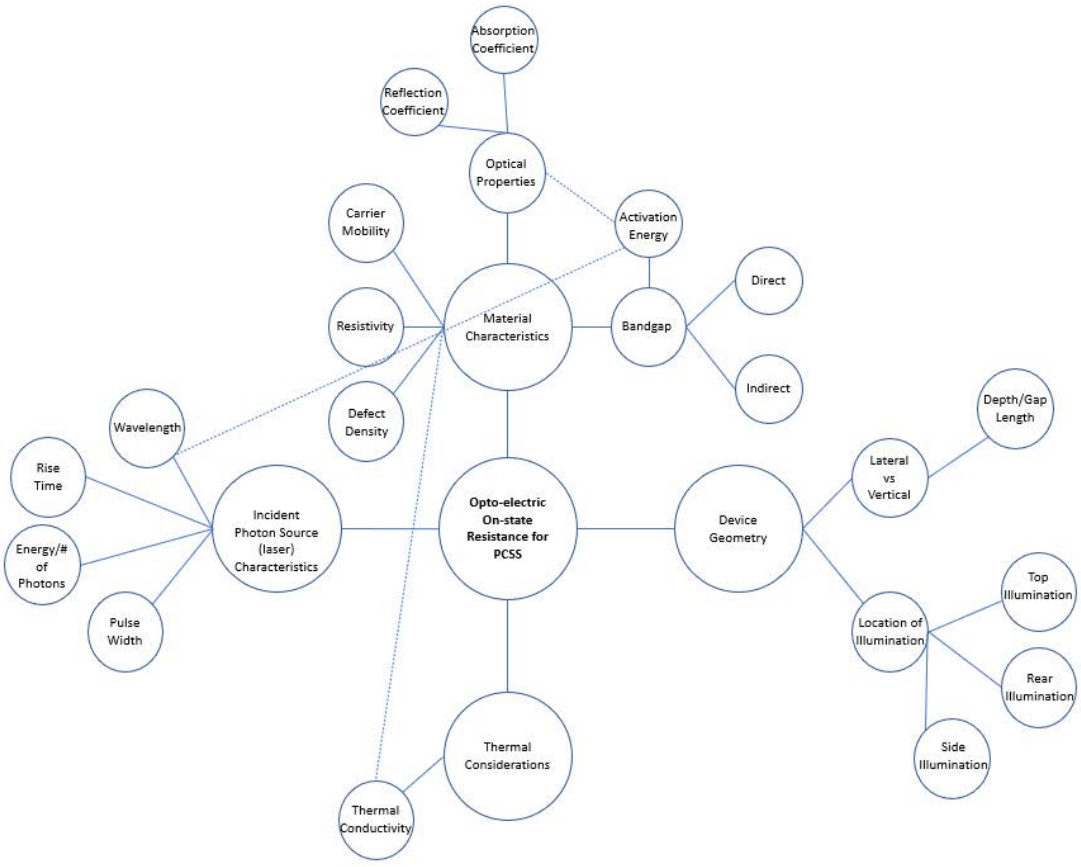


Figure 4.8.1: Flow chart of parameters affecting on-state resistance in PCSS, which will be iterated upon as the literature study progresses.

4.8.5 Summary of Significant Findings and Mission Impact

(A) A preliminary literature study of the on-state resistance of opto-electric devices was initiated to find the parameters that affect the on-state resistance of GaN PCSS and similar devices of differing materials. This study will lead to the determination of what parameters can be manipulated to optimize on-state resistance in GaN PCSS leading to a material option that provides increased efficiency and SWAP-C^2 capabilities of a PCSS-based RF generation system.

5.0 Pulse Forming Networks

5.1 Diode-Based NLTLs

(Nicholas Gardner)

5.1.1 Problem Statement, Approach, and Context

Primary Problem: The size, weight, and cost of pulse forming/shaping networks (PFNs) need to be reduced and optimized for Navy afloat missions.

Solution Space: Develop a diode-based nonlinear transmission line (D-NLTL) as a pulse shaping network for the conversion of energy to the ultra-high frequency (UHF) band (0.3–3 GHz) at single MW peak power.

Sub-Problem: Metrics used for component selection are designed for D-NLTLs operating at sub 0.1 GHz frequencies. Using such metrics alone to design D-NLTLs capable of single GHz frequency generation introduces a trial by error nature to the design process wherein frequency/power generation predictions and measurements can differ by a few hundred MHz or the design potentially fails to operate at all.

State-of-the-Art (SOTA): D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit. Simulations of LE-NLTLs indicate achievable frequencies in the single GHz range.

Deficiency in the SOTA: Simulation/measurement agreement becomes increasingly sensitive to parameters and factors outside of inductive and capacitive element choice alone at frequencies above ~100 MHz. Disparities between measurement and simulation above contribute to a trial by error design process for D-NLTL networks.

Solution Proposed: Identify and characterize diode parameters affecting frequency generation in the context of a NLTL application via simulation and experiment, and identify limits/desired ranges required for UHF generation. Such parameters include, but are not limited to: diode frequency response, diode reverse bias hold-off voltage, diode small signal capacitance, diode chip/package parasitics, and diode relaxation time. The improved understanding of the explored parameters will be used to design and fabricate a D-NLTL capable of GHz center frequency generation at single MW peak powers.

Relevance to OSPRES Grant Objective: The SWaP-C^2 capabilities of D-NLTLs (shown in Figure 5.5.1) represent a potential solution to the size, weight, and cost optimization issue for PFNs on Navy afloat missions.

Figure 5.1.1 20 cell D-NLTL of dimensions 1.1 x 23.45 cm constructed with commercial off the shelf components.

Risks, Payoffs, and Challenges: There exists a potential tradeoff between power and frequency generation. Devices such as ceramic capacitors may be used in a D-NLTL to generate high peak power due to their break down potentials in the 10s of kV, however,

such devices become highly resistive at 0.1–0.2 GHz frequencies. Diodes have been shown to be operational at frequencies upwards of 0.4 GHz, however, possess low hold-off potentials limiting peak output power. The payoff to overcoming these challenges is significant reductions in PFN size and cost.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Construct/demonstrate a prototype capable of UHF generation at low voltages (1–100 V excitation amplitude)

(A1) Break a low-voltage pulse into a sequence of solitons (SEP20)
(A2) Increase frequency generation past 200 MHz (NOV20)
(A3) Select diode candidate (junction capacitance <50 pF) and simulate expected results (Ongoing)
(A4) Design/fabricate/test line (Ongoing)

(B) Milestone – Demonstrate tuning of waveform at low voltages using electrical or mechanical means (**Completed with voltage biasing APR21**)

(C) Milestone – Construct/demonstrate a prototype capable of frequency generation above 1 GHz at single MW peak powers (Completed MW peak power but not GHz center frequency – Ongoing)

(C1) Identify diode candidates with a hold-off voltage of several kV and a low signal junction capacitance under 100 pF (Completed JAN21)
(C2) Design/fabricate single diode prototypes (Completed JAN21)
(C3) Perform initial tests using half-barrel pulse source (Completed FEB21)
(C4) Refine simulation using measurements (Completed FEB21)
(C5) Test a prototype using two diodes in series (Completed FEB–MAR21)
(C6) Test lines using Mega Impulse source (Completed MAY21**)**
(C7) Test K50F D-NLTL using PCSS as a source (Completed JUN21)
(C8) Use simulations and tests to refine line for increased frequency generation (Completed JULY21)
(C9) Rebuild lines for negative polarity pulses (Completed JULY21)
(C10) Test lines using PCSS as a source with various cell inductances (Completed JULY**)**
(C11) Test lines using Marx Generator as a source (**Completed AUG21**)
(C12) Reconstruct PCSS strip line to produce a pulse similar to 5.1.2 (left) and retest (**Ongoing AUG21)**

(D) Milestone – Demonstrate power scalability using an array of D-NLTLs (**On Hold – Prioritizing Milestone C**)

(D1) Design a prototype capable of running two D-NLTLs simultaneously off of the same excitation pulse (Completed JUN21)
(D2) Build a circuit capable of measuring the CV curve of low-voltage diodes and measure the CV curves of unused diodes and heavily used diodes (Completed JUN21)

5.1.3 Progress Made Since Last Report

(C) Both the K50F and K100F based HV D-NLTLs were excited with a pulse generated from a marx generator. The K50F line broke the Marx generator pulse into solitons with a center frequency of 595 MHz and a Bragg frequency of 961 MHz. The K100F did not break the pulse into solitons but did sharpen the rising edge to produce a Bragg frequency of 1.25 GHz.

5.1.4 Technical Results

GHz MW D-NLTL Prototype (C): The results of the marx-generator-produced excitation pulse this month for the K50F and K100F D-NLTLs revealed one of the few major differences in line behavior between the two networks. Both D-NLTLs were successfully excited by a pulse generated by a Marx generator, and the results are displayed in Figure 5.1.2. The K50F line successfully broke the pulse into solitons with a center frequency of 595 MHz and a Bragg frequency of 961 MHz. The waveform produced by the K50F D-NLTL (5.1.2-a) represents the first time we have broken a waveform into solitons using a HV line. The K100F line only sharpened the rising edge of the pulse to a Bragg frequency of 1.25 GHz as has been previously demonstrated with other HV sources. Since the K100F D-NLTL did not break the pulse into solitons no center frequency estimate could be measured.

One possible source of the difference may have to do with how the diodes become saturated in a stacked diode setup. On paper, the two K50F diodes wired in series should behave very similarly to the single K100F diode. However, it is possible that due to the lower reverse bias breakdown voltage of the K50F diode, the excitation pulse is able to drive the K50F line into soliton formation at lower amplitudes than the K100F line.

It should be noted that there were difficulties during the tests with inconsistent waveform generation or a failure to produce any waveform by the Marx generator. To obtain data, the Marx generator was triggered 100 times while connected to each D-NLTL and all waveforms were collected. The waveforms depicted in Figure 5.1.2 represent 4 of the 100 tests for the K50F line and 14 of the 100 tests for the K100F line. Due to the kV level signals involved in the HV D-NLTL tests, a cell zero measurement cannot safely be taken between the source-line interface and the first inductor. Therefore, we do not know the exact behavior of the excitation pulse each line was driven with for those tests, we only know the geometry of the original marx generator pulse shown in Figure 5.1.3.

At this time, it is not yet clear if the presence of the D-NLTLs caused the amplitude spike or not. The D-NLTL has not caused alterations to the produced pulse when tested with the DSRD, Megaimpulse, or PCSS-based sources. Prior to the final marx + D-NLTL tests, the marx generator was demonstrating issues in consistently producing the same waveform. Figure 5.1.3 represents one burst of marx generator waveforms. Prior to that measurement, the marx pulse generator geometry was inconsistent, or the system failed to produce a pulse at all. The data shown in Figure 5.1.2 has been included and reported on as it represents expected D-NLTL behavior for a pulse similar to Figure 5.1.3, but with an increased amplitude. The D-NLTL and Marx generator groups have decided to cease Marx/D-NLTL tests until the issues with the Marx generator are rectified and more reliable excitation pulses can be extracted.

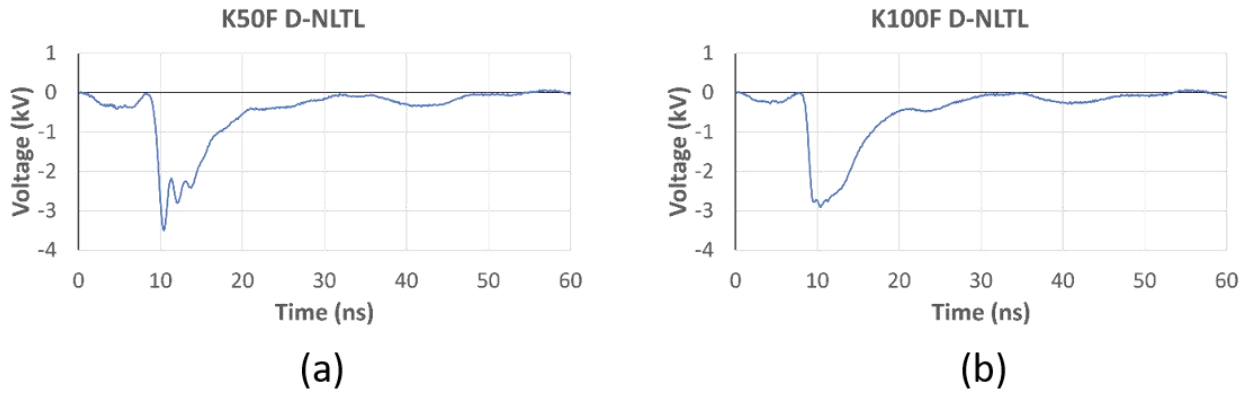


Figure 5.1.2: (A) Results for the K50F D-NLTL when driven by the Marx Generator. (B) Results for the 100F D-NLTL when driven by the Marx Generator. The K50F line produced a center frequency of 595 MHz with a Bragg frequency of 961 MHz. The K100F line produced a Bragg frequency of 1.25 GHz, but did not produce a second soliton to obtain the center frequency from.

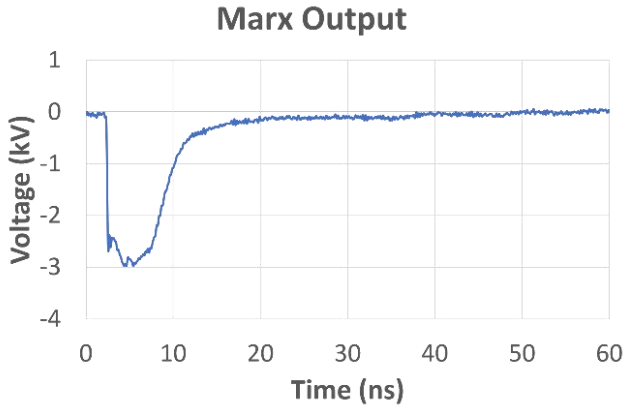


Figure 5.1.3: Marx generator waveform without D-NLTL attached.

5.1.5 Summary of Significant Findings and Mission Impact

(A) After a failure of the high-voltage diode-based nonlinear transmission lines (D-NLTLs) to reproduce simulated results, work refocused on low-voltage D-NLTLs to determine the source of the discrepancy. In NOV2020 a center frequency of ~250 MHz was achieved using a D-NLTL design based on the diode model SMV1702.

(B) Following the success of the SMV1702 D-NLTL, a circuit was designed capable of electrically tuning the center frequency utilizing DC biasing of the diodes. In FEB–APR2021 the circuit demonstrated a linear relationship between DC bias up to a limiting potential. Negative DC biases decreased center frequency while positive DC biases increased center frequency.

(C) In JAN2021 two diode candidates (models K100F and K50F) were identified for a HV D-NLTL design. FEB2021 saw successful tests of both D-NLTLs with each sharpening the rise time of a pulse produced by a DSRD based source down from ~1 ns to ~600 ps. In AUG2021 the first major variation between the K50F and K100 F D-NLTLs were observed with the K50F line breaking the pulse into solitons while the K100F line primarily sharpened the rising edge of the pulse.

(D) During MAY2021 a line topology capable of feeding two identical D-NLTLs with the same pulsed source at the same time was fabricated. Initial results were collected, and a prototype is currently being designed to test the ability to parallelize D-NLTLs.

6.0 Tradespace Analysis of Ultra-Wide-Band Antenna Arrays

6.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

6.1.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wideband (UWB) antenna elements in a phased array for high-power microwave (HPM) transmissions.

Deficiency in SOTA: Large physical aperture size of the antennas.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters, followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area. Using stochastic and machine learning (ML) algorithms to optimize antenna element and array performance.

Relevance to OSPRES Grant Objective: Provides design and optimization guidelines for UWB ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

6.1.2 Tasks and Milestones / Timeline / Status

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN–MAY 2021 / Completed code.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN–MAY 2021 / Completed investigations of arrays on infinite ground planes.

(C) Build minimum viable validation prototypes of single ESA elements on substrates that have good power handling capabilities for HPM transmissions at UHF range (such as FR-4, TMM-10i, TMM-6) / JAN–SEP 2021 / Ongoing fabrication and time-domain analysis of the designed antenna elements.

(D) Optimization of ESA (single element) performance using regular, and ML based stochastic search algorithms / JUN–SEP 2021 / Ongoing.

(E) Build minimum viable validation prototypes for arrays of ESA elements / JUN–SEP 2021 / Ongoing fabrication of a 2×2 array of ESAs.

6.1.3 Progress Made Since Last Report

(C) Build minimum viable validation prototypes of single ESA elements:

a. Modeled and characterized a coaxial probe-fed wideband rectangular microstrip patch ESA element, via FEKO, on a 1-inch-thick TMM-10i ($\epsilon_r = 9.8$) substrate in the UHF range (684–944 MHz).

b. A coaxial probe-fed microstrip patch antenna element (0.9–1 GHz) design, on 6.35 mm thick TMM-10i substrate, is currently under manufacture.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

a. Modeled and characterized a 5×5 array (square lattice), composed of the ESA elements, mentioned in Part (C), on an infinite PEC-backed TMM-10i substrate.

b. Ongoing manufacturing of a 2×2 array of microstrip patch ESA elements (0.9–1 GHz) on a 0.65-inch-thick polyethylene substrate.

6.1.4 Technical Results

(C) Build minimum viable validation prototypes of single ESA elements:

<u>Design and characterization of a UWB microstrip ESA element at the UHF range:</u>

In this section, the methodology that has been used to design a wideband coaxial probe-fed microstrip patch ESA element, is presented briefly, followed by the modeling and characterization of an ESA prototype.

To begin with, coaxial probe-fed microstrip patch antennas have been chosen as array elements because of their light weight and compact size (SWaP considerations), constructional simplicity, and performance tractability. However, conventional microstrip patch antennas have low impedance BW (~8–10%). In addition, excitation of surface waves (SW) is a common phenomenon in microstrip patch antennas, which often manifests itself in the form of low radiation efficiency and edge diffractions that lead to back radiation and interference with the main pattern in the forward region [1]. Complete elimination of SW modes in a microstrip patch is difficult as the dominant TM_0 SW mode propagates unattenuated with zero cut-off frequency ($n = 0$ in eq. 6.1.1). The cut-off frequencies (f_c) of the higher order SW modes can be computed as [2]:

$$f_c = \frac{n}{4h\sqrt{\epsilon_d \mu_d - \epsilon_0 \mu_0}} \ldots (6.1.1)$$

where h is the substrate thickness, ϵ_d and μ_d are the permittivity and permeability of the dielectric substrate, and ϵ_0 and μ_0 are the free space permittivity and permeability, respectively.

The next higher order mode is excited at $n = 1$ and is referred to as the TE_1 SW mode. Our goal is to minimize the SW excitations and we attempt to do so by selecting the substrate parameters ($h\sqrt{\epsilon_r}/\lambda$) in such a way that excitation of SWs is limited only to the dominant TM_0 mode. Excitation of the next higher order TE_1 mode is prohibited by forcing the antenna operating frequency, $f_{operating} < f_c^{TE_1}$. Once the optimum substrate parameters are chosen, the patch is designed using the standard microstrip antenna equations [3]. Next, to improve the impedance BW, we implement our proposed BW enhancement technique in which the feed probe is placed along 2/3rd of the patch diagonal. Using this technique, it is possible to obtain $\geq 30\%$ 2:1 VSWR BW from a simple microstrip patch antenna.

Now, to design a wideband microstrip patch ESA element in the UHF (0.6-1 GHz) range, we chose a 1-inch-thick, circular-shaped, TMM-10i ($\epsilon_r = 9.8$) substrate as shown in Fig. 6.1.1. For the selected dielectric material, $f_c^{TE_1} = 0.994$ GHz. Therefore, our target is to design an antenna, whose entire operating frequency range < 0.994 GHz. Two antennas have been modeled via FEKO and compared. Table 6.1.1 shows the antenna parameters and the corresponding VSWR and gain of the antennas are shown in Fig. 6.1.2.

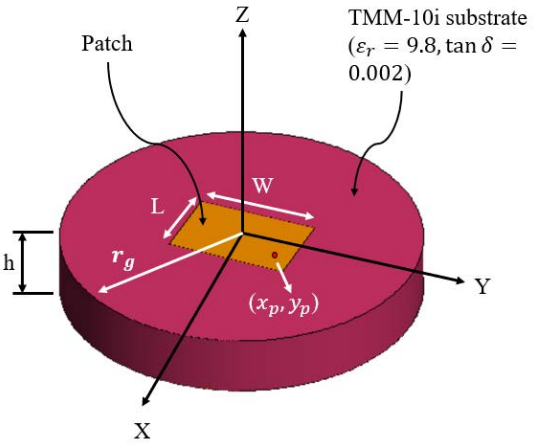


Figure 6.1.1 FEKO simulation model of the designed microstrip ESA element on a 1-inch-thick PEC-backed TMM-10i substrate.

Table 6.1.1 Antenna Dimensions

Ant #	L (mm)	W (mm)	(x_p, y_p) (mm, mm)	r_p (mm)	r_g (inch)	f_L (GHz)	f_c (GHz)	f_U (GHz)	%BW	ka at f_C
1	38.44	57.67	(12.81, 19.22)	3	3	0.684	0.814	0.944	31.94	0.59
2	34.45	51.70	(11.48, 17.23)	3	3	0.725	1.048	1.371	61.64	0.68

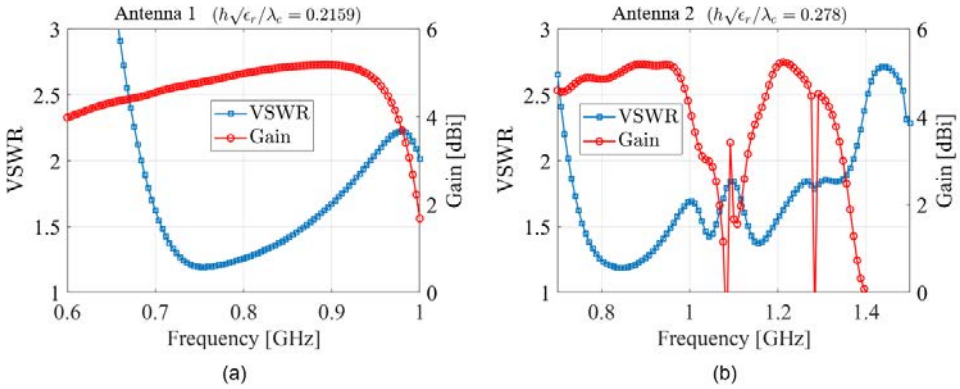


Figure 6.1.2 VSWR and gain of (a) Antenna 1 and (b) Antenna 2.

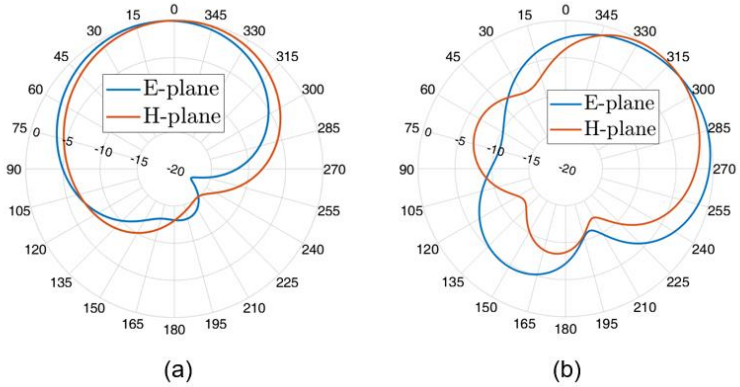


Figure 6.1.3 E-plane ($\phi = 0°$) and H-plane ($\phi = 90°$) radiation pattern of (a) Antenna 1 at $f_U = 944$ MHz and (b) Antenna 2 at $f_U = 1371$ MHz.

Figs. 6.1.2 and 6.1.3 show that the operating frequency range (0.684–0.944 GHz) of Antenna 1 is well below the cut-off frequency of TE_1 SW mode (0.994 GHz) and hence Antenna 1 has very stable gain and VSWR performances. Whereas, for Antenna 2 (0.725–1.371 GHz), the excitation of the TE_1 mode results in distorted gain performance (Fig. 6.1.2b) and pattern degradation (Fig. 6.1.3b). In an array, the excitation of higher order SW modes can lead to scan blindness (drop in gain when the array main beam is steered/scanned from boresight), thus limiting the steerability of the array. Therefore, between the two antenna designs, we choose Antenna 1 as an array element, even though it has lower BW than Antenna 2. Additionally, Antenna 1 qualifies as a quasi-ESA element as its $ka = 0.59$ (Table 6.1.1). To qualify as an ESA, an antenna's $ka \leq 0.5$, where $k = \frac{2\pi}{\lambda}$ is the wavenumber and a is the radius of the minimum sphere that circumscribes the antenna [4].

Antenna 1 is now subjected to two different input signals, available in CST: (1) Gaussian and (b) Impulse. The time-domain electric fields at different distances from Antenna 1, subjected to these input signals, are obtained. Fig. 6.1.4 and 6.1.5 show the input signals

and the resultant time-domain E-field of the antenna at various distances. In both the cases, the E-fields have been normalized to facilitate comparison.

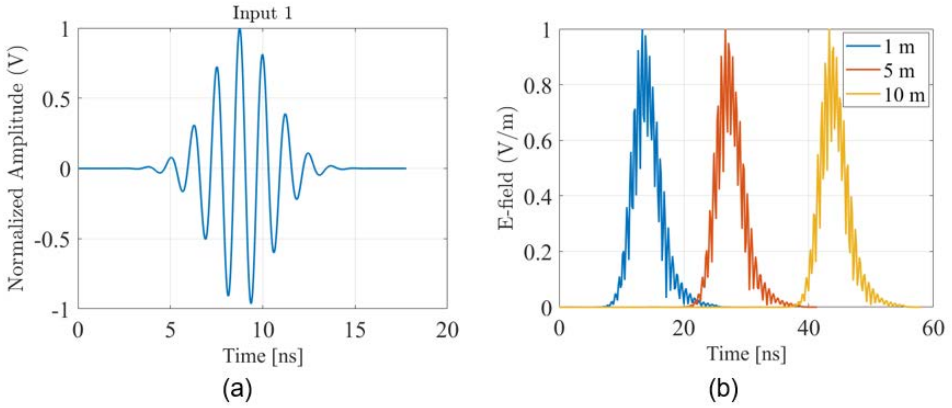


Figure 6.1.4 (a) Input Gaussian signal and (b) normalized time-domain E-field of Antenna 1 at various distances.

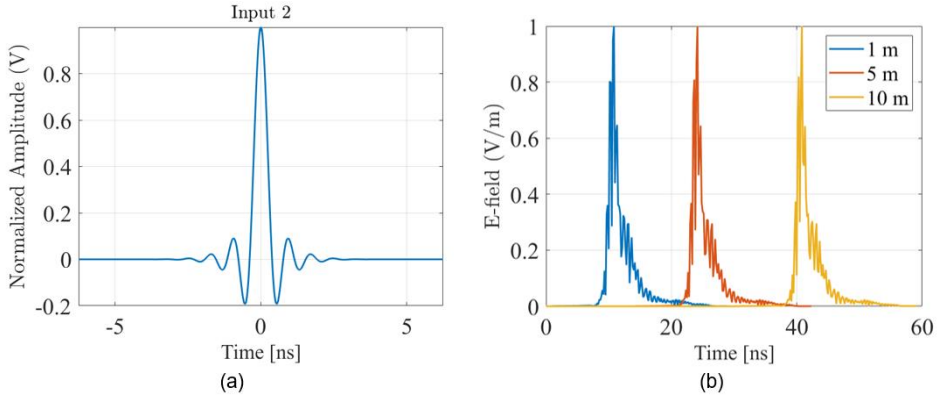


Figure 6.1.5 (a) Input impulse and (b) resultant normalized time-domain E-field of Antenna 1 at various distances.

Table 6.1.2 Antenna Dimensions

Distance (m)	rE/V	
	Gaussian Input	Impulse Input
1	0.7476	0.3678
5	0.7552	0.3808
10	0.7592	0.3928

The rE/V values are found to be quite low when the antenna is subjected to an impulse signal. Methods to improve the rE/V values will be investigated. In addition, the antenna will be subjected to other input pulses and the corresponding time-domain analysis will be performed.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

The wideband coaxial probe-fed microstrip patch ESA element design (Antenna 1), reported in Part (C), is now integrated to form a 5×5 array. For initial characterization of the array, we have considered an infinitely large PEC-backed TMM-10i substrate. The geometry of the array is shown in Fig. 6.1.6.

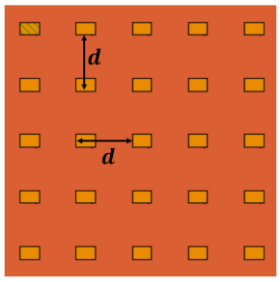


Figure 6.1.6 VSWR and gain of (a) Antenna 1 and (b) Antenna 2.

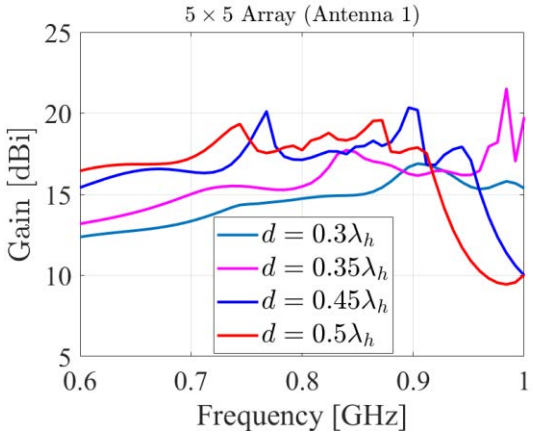


Figure 6.1.7 Gain vs. frequency of the 5×5 array having different inter-element spacing d.

Table 6.1.3 Comparison of the 5×5 array gain for different inter-element spacing d.

d (cm)	Radiating Aperture Area (cm^2)	Aperture Efficiency (%) at 800 MHz	Average Gain (dBi)
$11.24\ (0.3\lambda_h)$	2476.56	134.2827	14.00
$13.12\ (0.35\lambda_h)$	3278.82	120.3462	15.24
$16.86\ (0.45\lambda_h)$	5220.40	110.4712	16.07
$18.74\ (0.5\lambda_h)$	6359.70	103.9733	15.75

From Fig. 6.1.7 and Table 6.1.3 it can be concluded that the 5×5 array with inter-element spacing of $d = 0.45\lambda_h$ has the best average boresight gain over the frequency range of operation (684–944 MHz). Future work involves complete characterization of this antenna array (elements arranged in square lattice) on finite PEC-backed TMM-10i substrate followed by the consideration of hexagonal lattice arrangement for aperture area reduction.

6.1.5 Summary of Significant Findings and Mission Impact

(A) Developing Array Pattern Tool for large arrays calculations:

A MATLAB code has been developed for faster approximation of the radiation pattern of a linear/planar array of any size and composed of any type of antenna elements. The code requires the center element pattern of a small array (say, 3×3) composed of the same type of antenna elements, desired lattice arrangement, and total number of array elements, as user inputs. This work will be included in future publications.

(B) Investigate the effects of array aperture area reduction on different array parameters:

The effect of different array aperture area and lattice arrangements on the array parameters (such as array gain, beamwidth, electronic beam steerability, etc.) have been reported for arrays modeled on infinite ground planes (DEC 2020 ONR-OSPRES-Grant MSR). The results show that, with 30% reduction in the aperture area ($\approx 50\%$ reduction in # of elements), the gain drops by < 3.5 dBi without any scan blindness spotted as the main beam is steered from boresight to $\pm 60°$ in the $640-990$ MHz range.

The array parameters for large arrays ($\geq 15 \times 15$) on finite ground planes could not be computed using the commercial EM solvers (FEKO and CST) due to excessive memory and time consumption. This work will be resumed after developing a method to estimate array performances on finite ground planes, either through ML or conventional approaches.

(C) Build minimum viable validation prototypes of single ESA elements:

Investigated different bandwidth enhancement techniques applicable to single layer microstrip patch ESAs:

a. Method I: Bandwidth enhancement by strategically placing the coaxial probe along 2/3rd of the patch diagonal – This method is proposed and experimentally validated using prototypes manufactured on TMM-6 and TMM-10i substrates at $2.5-5$ GHz. An antenna has been modeled on a G10/FR-4 substrate, at the UHF range ($0.6-1$ GHz), and is being considered for manufacturing.
b. Method II: Coaxial probe-fed U-slot loaded rectangular microstrip ESAs – A prototype is manufactured on a G10/FR-4 substrate ($0.9-1.3$ GHz) and tested.
c. Method III: L-probe-fed U-slot-loaded rectangular microstrip ESAs – An antenna has been modeled on a TMM-4 substrate that operates in the $0.52-1.17$ GHz range ($\approx 77\%$ 2:1 VSWR bandwidth). Due to the fabrication complexity of the L-probe proximity coupled feed, this antenna will not be manufactured.

(D) Optimization of ESA (single element) performance using regular, and ML based stochastic search algorithms:

Investigated the bandwidth enhancement of the coaxial probe-fed microstrip patch antennas, using regular and ML based stochastic search algorithms (GA, PSO, and Simplex methods), by optimizing the feed-probe location and ground plane shape and size. Compared to regular search algorithms, ML algorithms are found to be less computationally intensive (in terms of time and memory consumption).

(E) Build minimum viable validation prototypes for arrays of ESA elements:

A 3×3 array of microstrip ESA elements, on a TMM-10i substrate, has been manufactured and tested at the $2.5-5$ GHz range. We have modeled and submitted a work order for manufacturing a 2×2 array of narrowband microstrip ESAs, on a 0.25" TMM-10i substrate, for operation at the UHF range ($0.9-1$ GHz). We have initiated modeling and characterization of a 5×5 array of wideband ESA elements for future prototyping.

6.1.6 References

[1] V. R. Komanduri, D. R. Jackson, J. T. Williams, and A. R. Mehrotra, "A general method for designing reduced surface wave microstrip antennas," *IEEE Trans. Antennas Propag.*, vol. 61, no. 6, pp. 2887–2894, Jun. 2013.
[2] R. F. Harrington, *Time-Harmonic Electromagnetic Fields*. New York, USA: McGraw-Hill, 1961.
[3] D. R. Jackson, "Introduction to microstrip patches, short course notes," in *2013 IEEE International Symposium on Antennas and Propagation and USNC-URSI National Radio Science Meeting*, July 2013.
[4] J. L. Volakis, C. C. Chen, and K. Fujimoto, *Small Antenna Miniaturization Techniques and Applications*. New York, NY, USA: McGraw-Hill, 2010.

6.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna

(Kalyan Durbhakula)

6.2.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelev antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem:

(i) The integration of impedance transformer to single element Koshelev antenna to simulate and test the combined (transformer-antenna) performance is currently not feasible using commercial EM simulators.

(ii)The total surface currents on the Koshelev antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not yet clearly understood.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelev antenna array that effectively reduce its physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelev antenna has been shown in the literature to withstand higher voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelev antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelev antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelev antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelev antenna.

(iii) The large electrical size (>5λ) of the Koshelev antenna at its highest operating frequency poses huge computational challenges.

6.2.2 Tasks and Milestones / Timeline / Status

(A) Complete literature search to identify and list antenna elements that satisfy UWB properties and HPM requirements, and down-select accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelev antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB–MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t, \phi, \theta)$) in receive or transmit mode / MAR–APR21 / Complete.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelev antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / MAR21/ Complete.

- Milestone: Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain over the desired bandwidth, and aperture efficiency.

(F) Reduce Koshelev antenna aperture size (H×W) to equal to or less than 90 mm × 90 mm, equal to that of the SOTA BAVA, for direct antenna metrics comparison / MAR–APR21 / Complete.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, aperture efficiency equal to or greater than 130% at 900 MHz.

(G) Using the optimized model from (F), build various array simulation models/topologies to perform a tradespace study and report tradeoffs between array antenna metrics such as center element reflection coefficient (S11) value, gain vs theta at constant phi, physical aperture area, aperture efficiency, and rE/V / MAY–JULY21 / Complete.

- Milestone: Develop/showcase an optimized Koshelev array model that exceeds an aperture efficiency of 130% with a high rE/V.

(H) Perform literature search to investigate, understand, and determine the applicability of special electromagnetic (EM) techniques to the antennas under consideration. / JAN–APR21 / Complete.

(I) Explore different impedance taper (microstrip based and coax based) designs that can interface well (both mechanically and electrically) to transition the signal from a coax cable to the input of the Koshelev antenna element / JULY21–AUG21 / Ongoing.

- Milestone: Recommend the optimum impedance taper design (with minimum reflections and maximum power transfer) with the optimum dimensions to successfully convert the high-voltage, short-rise time input signal from a coax cable to the feed of the Koshelev array.

(J) Study response from optimized Koshelev antenna array when excited with different monopolar, differential, and bipolar pulse signals of significant interest **(NEW)** / AUG21–OCT21 / Ongoing.

- Milestone: Provide a table comparing the Koshelev antenna array response metrics and narrow down the suitable pulse signals. Recommend (if any) changes to the

downselected pulse signal(s) that can further improve the radiation efficiency, and/or transient gain.

(K) Prototype single element Koshelev antenna and test for reflection coefficient, gain as a function of frequency, radiated electric field at 1-m, 2.5-m, 5-m and 10-m (if feasible) distances.(followed by optimized Koshelev antenna array) **(NEW)** / AUG21–DEC21 / Ongoing.

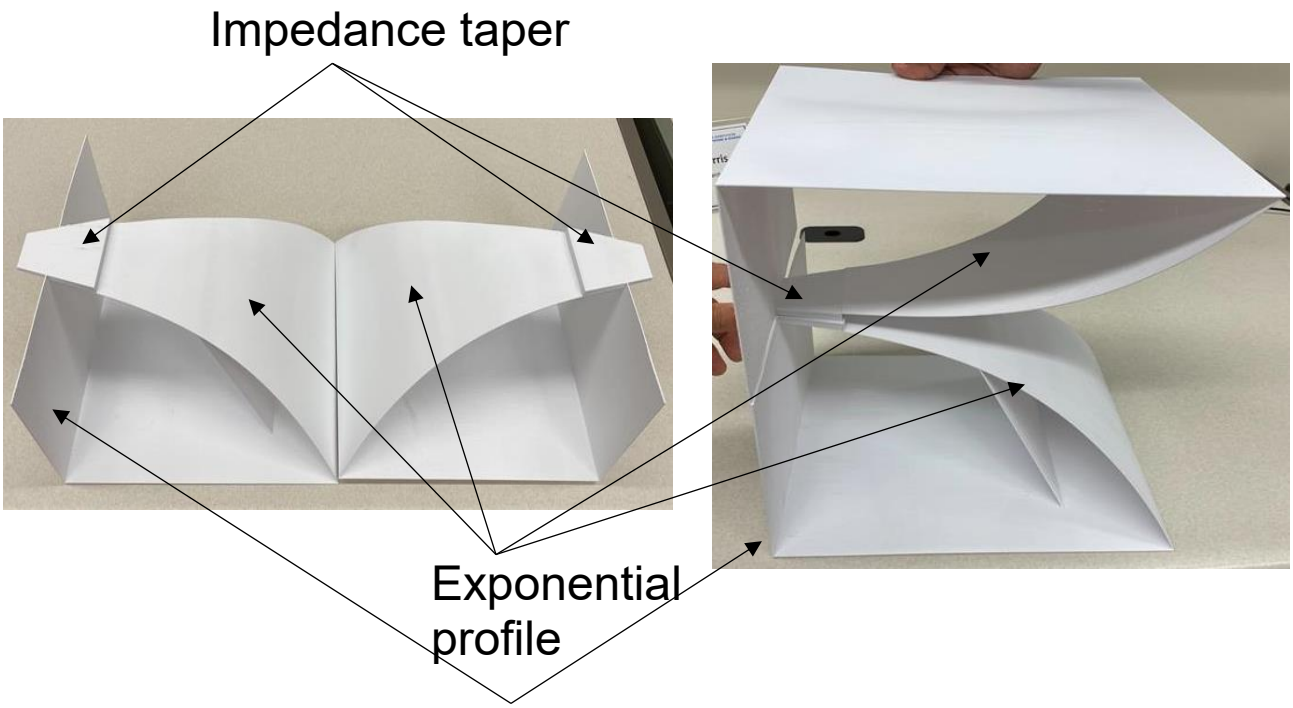
- Milestone: Report measured data and recommend any improvements to the fabrication/prototyping/testing methods.

6.2.3 Progress Made Since Last Report

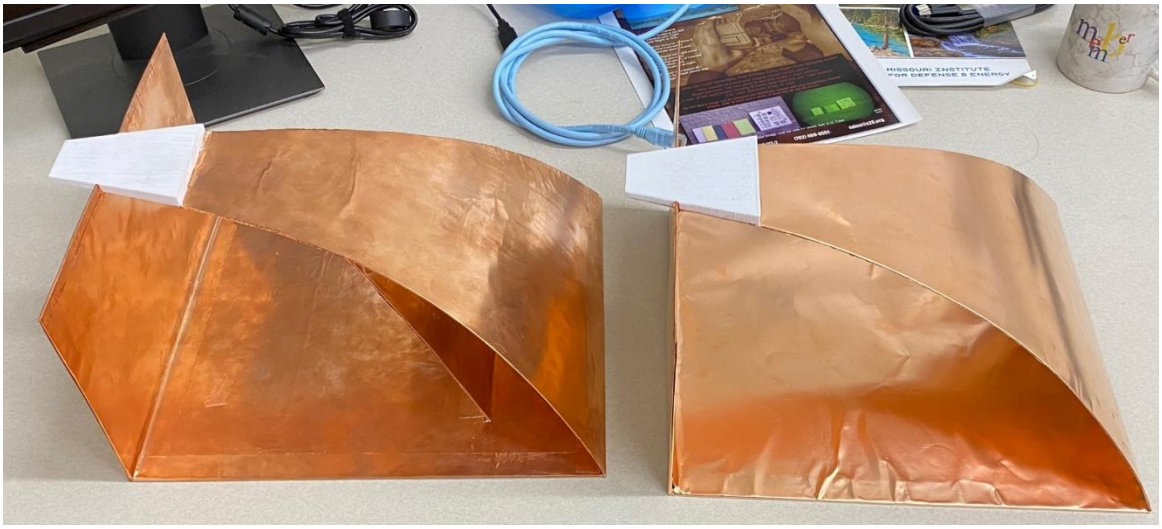
(I) A time-domain analysis of the microstrip-based linear impedance taper has been carried out. This is to ensure the signal from the coax side of the taper is being carried to the feed end of the Koshelev antenna with minimal amplitude losses and minimum signal distortion.

(J) All elements of the hexagonal Koshelev antenna array have been excited with an open source megaimpulse signal, which is monopolar (unipolar) in nature. In addition, the monopolar signal has been converted into a bipolar signal by applying inverse and time shifting techniques. The bipolar signal has been fed to the antenna array and the resulting radiated electric field is compared against the monopolar case.

(K) The first 3D printed prototype of the Koshelev antenna (single element) has been initiated and is currently undergoing post 3D printing processing such as sanding to reduce surface roughness, electroplating to metallize, and assembling. Fig. 6.2.1(a) shows the 3D printed Koshelev with the impedance transformer. Fig. 6.2.1(b) shows the metallized Koshelev antenna parts using a copper foil. The white sides in Fig. 6.2.1(b) indicates the dielectric region of the linear impedance taper.



(a)

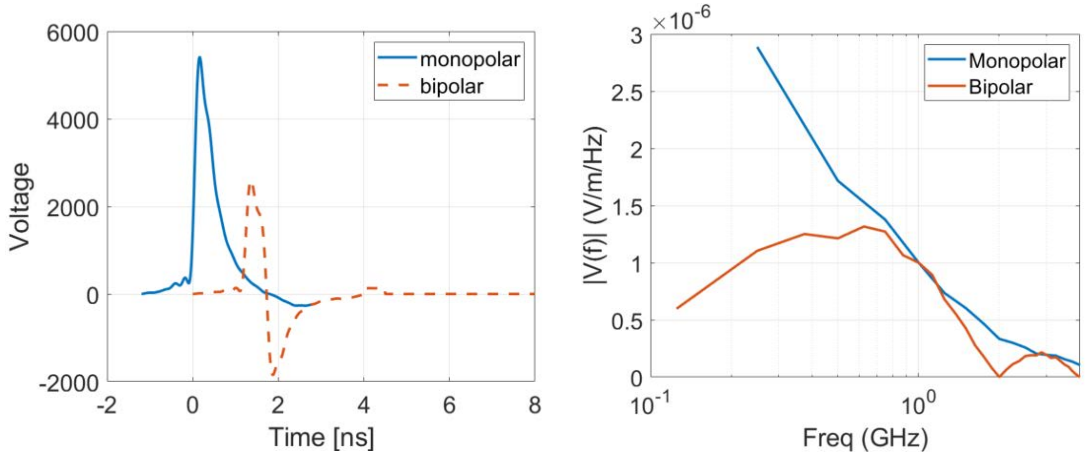


(b)

Figure 6.2.1 3D printed prototype of the Koshelev antenna with integrated linear impedance taper.

6.2.4 Technical Results

(I) In the previous MSR, a linear impedance taper design was introduced that connects the coax type connector/adaptor to the input feed of the Koshelev antenna. The reflection coefficient (S11) vs frequency response of the linear impedance taper has been shown in the previous MSR. In addition to the frequency domain response, it is necessary to verify the time-domain response. To carry out this task, an open source megaimpulse (MI) signal has been utilized. The MI signal is a monopolar signal. To be able to truly characterize the taper and therefore the antenna, the monopolar signal has been converted into a bipolar signal with a certain time shift. Fig. 6.2.2(a) shows the MI monopolar and bipolar signals. The monopolar signal has a peak voltage of 5.7 kV, which is converted to a bipolar one with a peak-to-peak voltage of 5.7 kV. Fig. 6.2.2(b) shows the frequency spectrum of monopolar and bipolar time domain signals. As it can be seen, the bipolar signal has good frequency content between 500 MHz and 1 GHz.



(a) (b)

Figure 6.2.2 (a) Time-domain megaimpulse signals, and (b) frequency spectrum of the time-domain megaimpulse signals.

The bipolar signal has been fed to the input of the taper and the output voltage at the load of the taper has been recorded. In Fig. 6.2.3, the blue curve shows the input voltage signal to the taper while the dotted red is the output from the taper, which will eventually be fed to the input of the Koshelev antenna. In addition to the phase shift of the signal at the taper output, the peak voltage dropped by 200 volts, whereas the peak-to-peak voltage dropped by about 250 volts. The shape of the signal has been retained. In other words, this preserves the signal information as well as the frequency content.

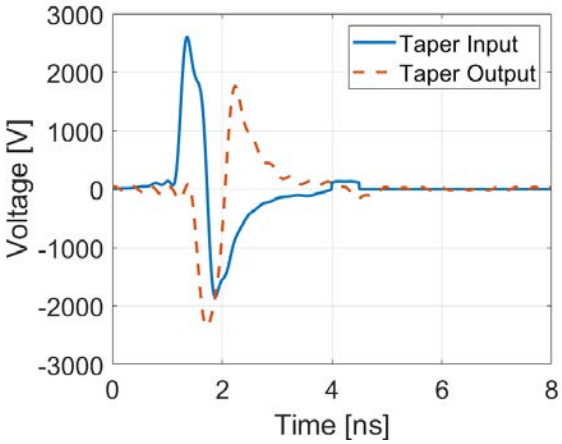
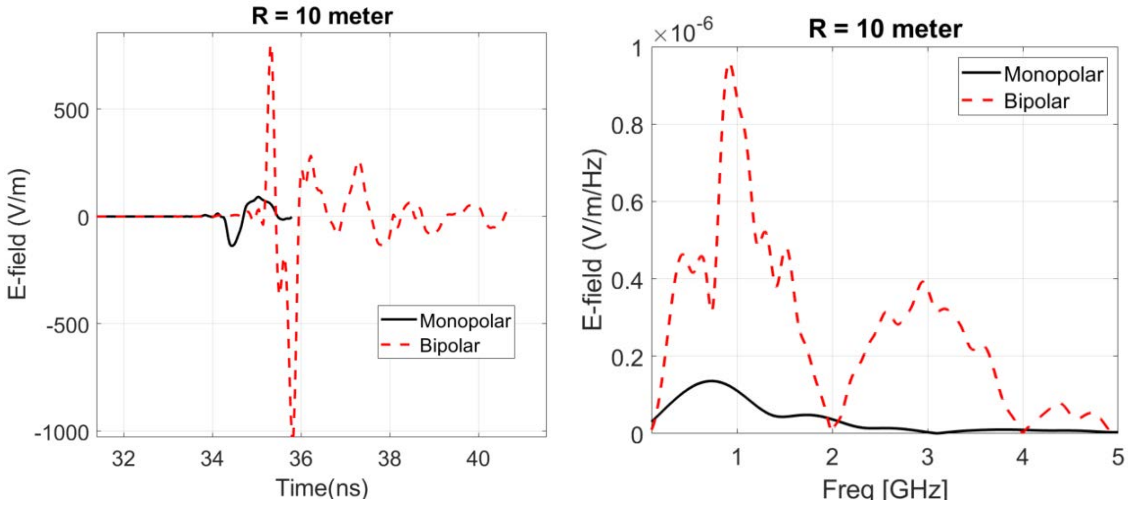


Figure 6.2.3 Input and output voltage of the linear impedance taper.

(J) The MI monopolar and bipolar signals have been simultaneously verified by feeding them to the Koshelev antenna array. Fig. 6.2.4(a) shows the time-domain radiated electric field from the Koshelev antenna array at a distance of 10-meters when excited with a monopolar signal and a bipolar signal separately. Fig. 6.2.4(a) clearly shows the advantage of feeding a bipolar signal as opposed to a monopolar signal due to the fact that the peak-to-peak electric field from a bipolar input signal is at least 10 times better than a monopolar input signal. A significant energy loss can be noticed from the black curve. This can be further validated by calculating the frequency response of time domain electric field for monopolar and bipolar input.. Fig. 6.2.4(b) shows the frequency spectrum for both responses and we can notice the huge difference between monopolar and bipolar signals.



(a) (b)

Figure 6.2.4 S11 value of the linear microstrip based impedance taper.

6.2.5 Summary of Significant Findings and Mission Impact

(A) An extensive literature search on various UWB antenna elements has resulted in finding three promising options. The down-selected elements are the Koshelev, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the single antenna element. Later, the single antenna element will be converted into a planar array.

(B) Initial validation of the Koshelev antenna simulated using CST software agreed well with the antenna metrics published in the open literature [1]. A UWB bandwidth response (10:1 bandwidth) and rE/V > 1 has been observed from our initial simulations of the Koshelev antenna. This validation ensured that the Koshelev antenna can be subjected to further tradespace studies to understand its performance followed by optimizing the design according to OSPRES grant requirements.

(C) The initial tradespace study and analysis of the Koshelev antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between the Koshelev antenna in [1] and aperture reduced Koshelev antenna are shown in Table 5.2.1 of the APR 21 MSR.

(D) An in-house code has been developed to calculate important UWB time domain antenna metrics such as full-width half maximum (FWHM) and ringing. These metrics have been calculated using in-house MATLAB code using the excitation voltage and radiated electric field information obtained from CST simulations. FWHM and ringing antenna metrics help with assessing or characterizing an antenna's UWB response.

(E) The tradespace study of feed position provided a deeper understanding of how its position impacts the S11 value bandwidth. An optimum value for feed position i.e., $F = 1/20 < L < 1/10$ is recommended to achieve maximum bandwidth. The tradespace study of the antenna length (L) is straightforward. A longer antenna length will radiate better at lower frequencies. However, physical size restrictions/requirements must be kept in mind in determining the antenna length. Finally, a larger α value (>120°) is recommended to avoid unnecessary reflections from the electric monopole.

(F) From a thorough tradespace study, the aperture size of the Koshelev antenna (single element) is determined to be 90 mm × 100 mm in order to achieve desired antenna metrics performance proposed in the milestone. All metrics described in the milestone have been successfully achieved except the desired bandwidth (200 MHz on both sides) at 900 MHz center frequency. The bandwidth achieved is 900 ± 100 MHz.

(G) The physical aperture area of the Koshelev array antenna largely depends on the interelement spacing and the shape of the array. We were able to determine that the diamond topology is the optimum shape for the Koshelev array antenna. Moreover, with the diamond Koshelev array, by making only element#3 passive we were able to obtain similar gain characteristics when compared against gain characteristics from all elements active case. From the non-symmetric interelement spacing values, we found that S_y has least effect on the output, therefore a small spacing value can be chosen to reduce the physical aperture area of the Koshelev array.

(H) The literature search on the special EM techniques expanded our knowledge and opened the door to opportunities to apply some of those techniques to the antennas under study. EM techniques such as non-symmetric and non-square array topologies have been applied to the development and study of the Koshelev array antenna.

(I) The first impedance taper design under consideration has shown good S11 values (< -10 dB) over the frequency range of interest. In addition, we have shown that the shape of the pulse can be easily retained at the output of the taper with less than 5% amplitude losses.

(J) The Koshelev antenna array response from feeding a monopolar vs bipolar signal has demonstrated a clear winner: that is, a bipolar signal will radiate at least 10 times better than a monopolar signal.

6.2.6 References

[1] Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

6.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna

(Sadie Brasel and Kalyan Durbhakula)

6.3.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of Shark antenna elements with an emphasis on inter-element and intra-element spacing effects is a good candidate for UWB HPM systems while having a reduced aperture area with respect to the current state-of-the-art. In the literature, the Shark antenna has already been shown to achieve a wide 20:1 impedance bandwidth, low dispersion, and a sectoral (also referred to as directional) radiation pattern.

Sub-Problem: The design parameter space of the Shark antenna has not been studied rigorously in the literature and therefore the effect of these parameters on the antenna metrics is not understood. In addition, the Shark antenna has been shown to be not very directive in the H-Plane. Preliminary studies have shown that aperture efficiencies at low frequencies are much better than at higher frequencies.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Explore the array tradespace by generating different array topologies/lattices (hexagon, octagon, square, ellipse) and with different intra and interelement spacing combinations.

Relevance to OSPRES Grant Objective: The Shark antenna dimensions were established to be frequency dependent and can be readily modulated to fit the spectrum characteristics of an ultra-fast rise time input pulse.

Risks, Payoffs and Challenges:

(i) The Shark antenna is comprised of flare-angle-dependent bicones that are truncated in the azimuthal angle. This still yields considerably higher half power beam width (HPBW) than other antenna elements under investigation. The significant reduction of HPBW in the H-plane may be unattainable and can be considered a major risk.

(ii) Payoffs include the development of a library of antenna metrics data for various shapes and sizes of the bicones and reflector plates in the shark antenna.

(iii) Computational challenges remain present with respect to automation of design parameter space on our currently used supercomputer (LEWIS). Design challenges persist in obtaining lower operating frequencies while not increasing the height of the antenna and surpassing the 90 mm × 90 mm size requirement.

6.3.2 Tasks and Milestones / Timeline / Status

(A) Complete initial design, simulation, and validation of the Shark antenna / JAN21 / Complete.

(B) Validate Shark antenna design using the LEWIS supercomputer over a wider range of frequency results (up to 20 GHz) / FEB–MAR21 / Complete.

(C) Identify Shark antenna design parameters which contribute significantly to bandwidth, gain, and physical aperture area. Determine which parameters contribute most to performance improvement/size reduction/ FEB–MAR21 / Complete.

(D) Perform a tradespace study by simulating the Shark antenna with varying cases of flare angle, cone length, and distance to backplane. Gain a general understanding of how these parameters affect impedance bandwidth, rE/V, gain and HPBW / FEB–MAY21 / Complete.

- Milestone: produce a detailed summary of change in impedance bandwidth, rE/V, HPBW in H-plane and E-plane as a function of flare angle (α), cone height (*h*), and distance to backplane (*d*) / Complete.
- Milestone: Choose optimal Shark antenna design that has the lowest operating frequency within size requirements based on tradespace study / Complete.

(E) Using the optimal Shark antenna design in (D), simulate various array geometries including hexagonal, rectangular, and circular arrays. Determine which array

geometries are optimal and analyze aperture fields and aperture efficiencies. / MAY–AUG21 / Ongoing.

- Milestone: Produce a report which states the effects of various array geometries for the Shark antenna. The optimal array geometry chosen should have the least interference between elements, therefore yielding higher impedance bandwidth and higher aperture efficiency. Overall, the optimal Shark array geometry should have at least 20% impedance bandwidth at 900 MHz center frequency for the centermost element with 130% array aperture efficiency, ± 60 degrees beam steering capability, and rE/V equal to or greater than 4.

(F) Begin prototyping and validation of optimal Shark antenna single element. / JUN–AUG21 / Ongoing.

- Milestone: have a finished Shark antenna prototype. Compare S11 and radiation pattern with simulated Shark antenna.

6.3.3 Progress Made Since Last Report

(E) The 8-element elliptical Shark antenna array has been chosen as the optimum array shape from the results presented in the previous MSR (July 2021). Moving forward, simulations have been performed to understand the interelement spacing effects on the bandwidth at the desired center frequency and on the radiated electric field.

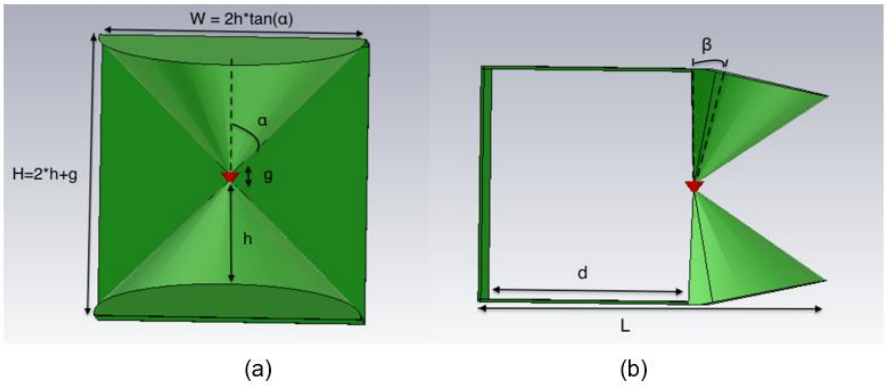


Figure 6.3.1 Shark antenna design parameters: *d, h, g,* α*,* β*.*

(F) The coax-based impedance transformer, the cones, and the back plate have been prototyped and are currently being electroplated.

6.3.4 Technical Results

(E) To reduce the physical aperture area of the Shark antenna array, the effects from varying interelement spacing variables in both axes must be studied and thoroughly understood. The relationship between the pulse duration and interelement spacing value for any antenna array has been provided in section 6.2 in the July MSR. Using the same relationship, we carried out a study by varying the pulse duration, as well as interelement

spacing values in the x-axis and y-axis. Fig. 6.3.2 shows the layout of the 8-element elliptical Shark antenna array with independent interelement spacing variables.

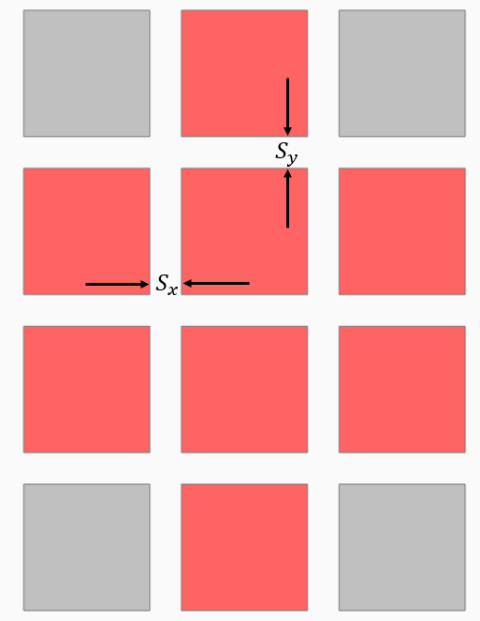


Figure 6.3.2 8-element Elliptical Shark antenna with different interelement spacing variables in the x-axis and y-axis.

(E) Firstly, the pulse duration of the incoming signal has been varied to study and identify the trend of the S11 curve and the associated bandwidth. Fig. 6.3.3 (a) shows the S11 values as a function of frequency for various pulse duration values by keeping other variables (d_x, d_y) constant. Increasing pulse duration value increases the interelement spacing value. A pulse duration of about 1.7 ns with the associated interelement spacing value would have around 100 MHz at 900 MHz center frequency. This is chosen as the optimum pulse duration value for this particular Shark element.

Similarly, the constants d_x and d_y have been varied with a pulse duration value of 1.712 ns to understand the S11 trend and the bandwidth associated with it. In Fig. 6.3.3 (b), the constant d_x has been varied and it was found that the smallest d_x value i.e., d_x=0.45, could give the optimum response. In Fig. 6.3.3 (c), a similar response can be seen from d_y=0.45, however, d_y=0.975 yielded the maximum bandwidth from 650 MHz to 1050 MHz. Therefore, the optimum values are P_d = 1.712 ns, d_x=0.45 and d_y = 0.975, which give the desired bandwidth (200 MHz) at the desired center frequency (900 MHz).

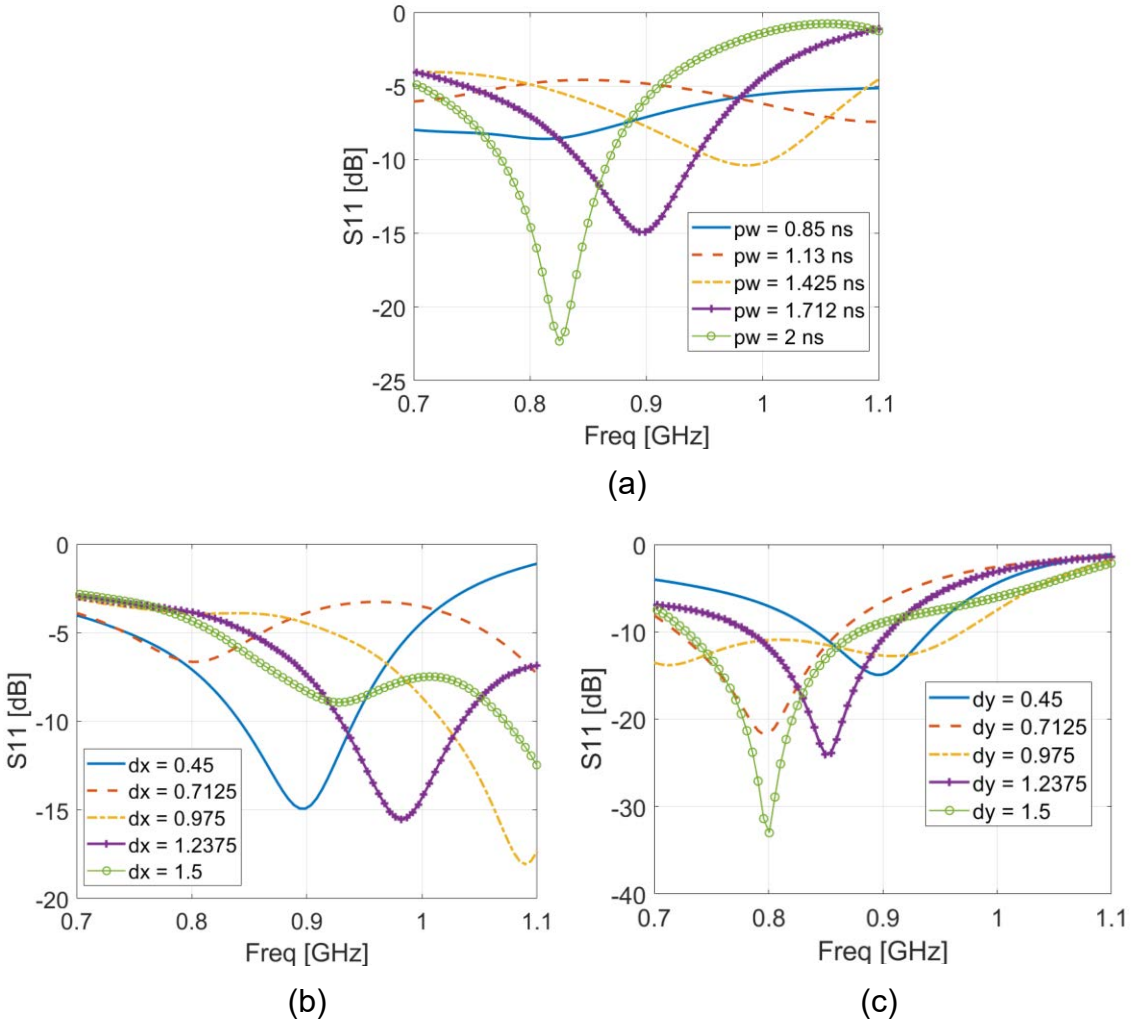
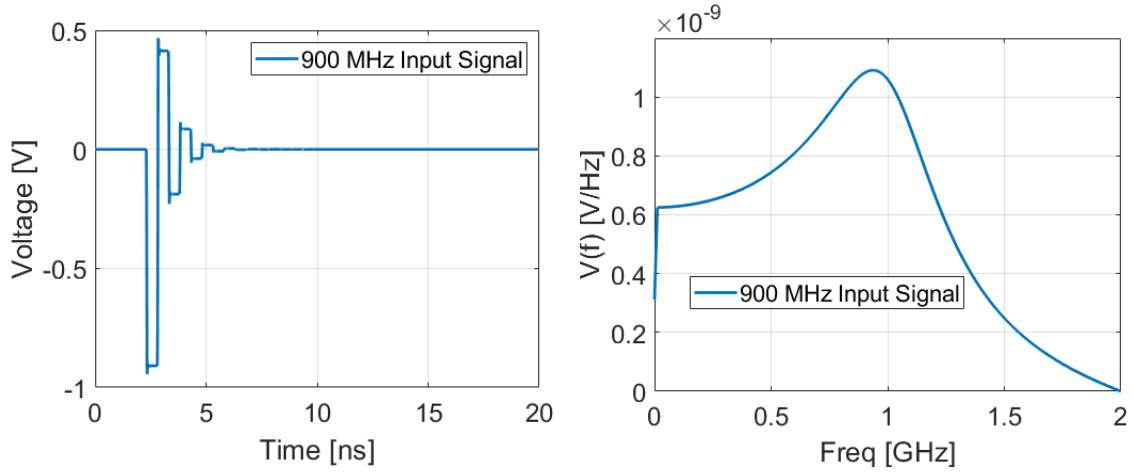


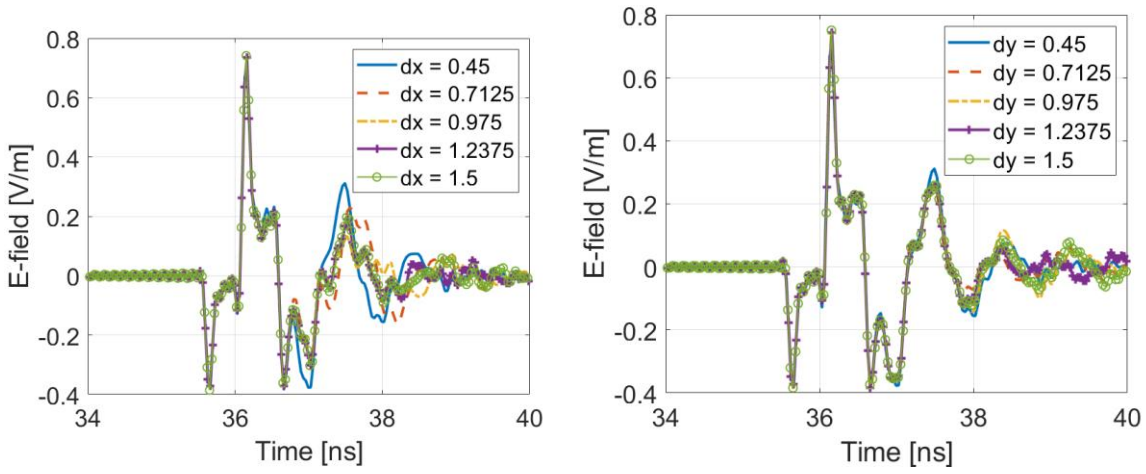
Figure 6.3.3 Center element S11 value as a function of frequency for different (a) pulse duration values, (b) interelement spacing values in the x-axis and (c) interelement spacing values in the y-axis.

In the next step, a normalized 900 MHz damped rectangular wave has been fed to the array elements to obtain the time domain radiated electric field at 10-meters distance from the aperture of the array antenna. The time domain and frequency domain properties of the input signal can be observed in Fig. 6.3.4. Fig. 6.3.5 and Fig. 6.3.6 show the radiated electric field and its frequency spectrum for varying d_x and d_y cases. The transient gain (rE/V) for all results in Fig. 6.3.5 is approximately 7.42. From comparing the frequency spectrum plots in Fig. 6.3.6(a) and Fig. 6.3.6(b), a significant difference can be noticed in Fig. 6.3.6(a), which shows that the radiated electric field is sensitive to interelement spacing variable in the x-axis than in the y-axis (Fig. 6.3.6(b)). In Fig. 6.3.6(a), the 900 MHz peak frequency spectrum has been obtained for the smallest value of d_x (= 0.45).



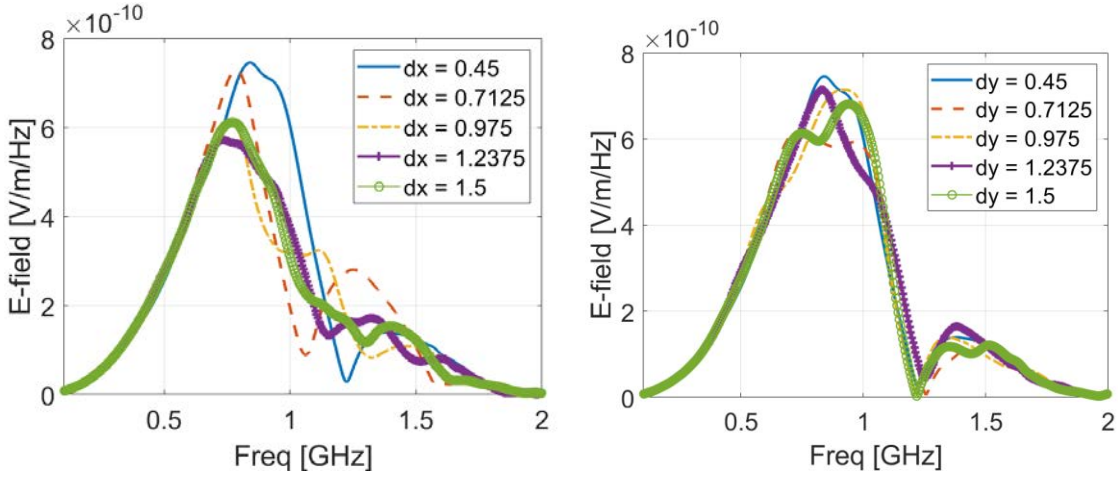
(a) (b)

Figure 6.3.4 900 MHz damped rectangular wave input signal in (a) time domain, and (b) frequency domain.



(a) (b)

Figure 6.3.5 Simulated electric field at 10-meter distance from the aperture of the elliptical Shark antenna for different (a) interelement spacing values in the x-axis, and (b) interelement spacing values in the y-axis.



(a) (b)

Figure 6.3.6 Frequency spectrum of the simulated electric field at 10-meter distance from the aperture of the elliptical Shark antenna for different (a) interelement spacing values in the x-axis, and (b) interelement spacing values in the y-axis.

(F) The optimized Shark antenna element has been prototyped. Fig. 6.3.7 shows two views of 3D and metallized Shark antenna. The back plate is cut out from an aluminum sheet, whereas the cones are 3D printed and coated using nickel paint.

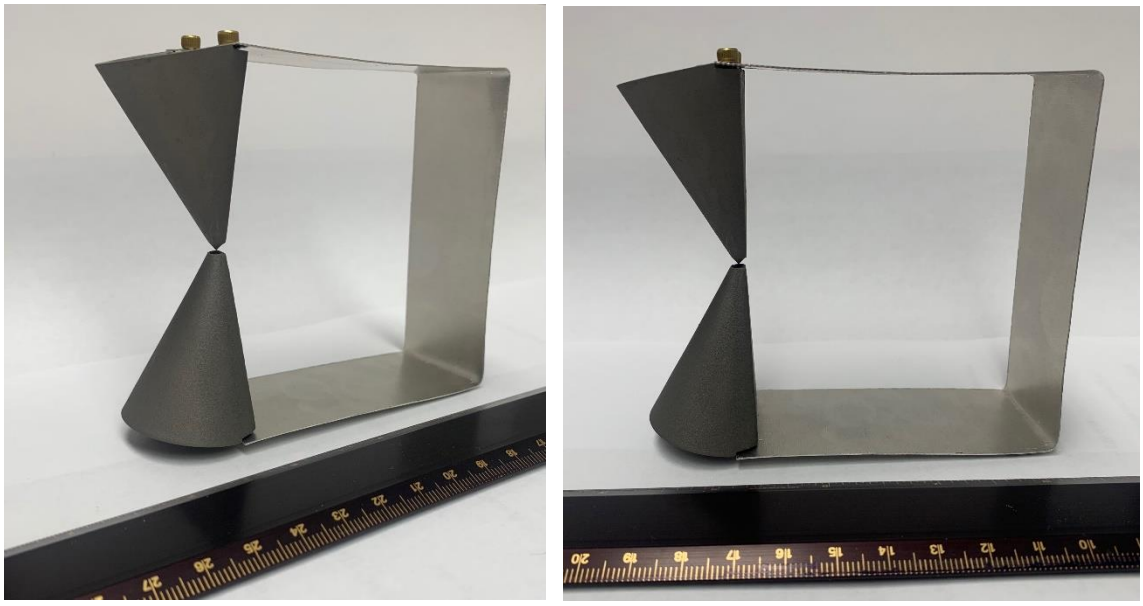


Figure 6.3.7. 3D printed Shark antenna .

6.3.5 Summary of Significant Findings and Mission Impact

(A-B) The Shark antenna has been designed, simulated, and validated according to [1]. (Figure 6.3.1)

(C) The Shark antenna design parameters that have been found to contribute significantly to bandwidth performance, directivity, and gain are the cone height (*h*) and distance to backplane (*d*).

(D) The Shark antenna tradespace study has been completed and has provided insight into the Shark antenna design space. Increasing the cone height *h* yields better impedance bandwidth at low frequencies and is more directive in the *e* and *h* planes. However, increasing *h* results in a larger aperture area. To remain within 90 x 90 mm, the maximum *h* value is 45 mm; with this a lowest operating frequency of 815 MHz is achievable.

(E) The study of array geometries has also confirmed that aperture efficiency decreases as more elements, and therefore more aperture area, is added to the array. The aperture efficiency metric is best used to compare arrays with the same or similar number of antenna elements. The square antenna array can also be ruled out as it has been shown to be much less directive in the E and H planes compared to the other geometries listed in Table 6.3.1 in July 2021 MSR. The elliptical Shark antenna has the optimum metrics, which can be found in Table 6.3.1 in July 2021 MSR. The metrics from elliptical Shark antenna are closer to desired metrics provided in milestone 6.3.2 (E)

The interelement spacing variable study has provided insight into the workings of Shark antenna array. The Shark antenna array is more sensitive to the interelement spacing variable in x-axis than in the y-axis. An optimum set of pulse duration, and other constant variable values have been given for the elliptical Shark antenna array.

6.3.6 References:

[1] L. Desrumaux, A. Godard, M. Lalande, V. Bertrand, J. Andrieu and B. Jecko, "An Original Antenna for Transient High Power UWB Arrays: The Shark Antenna," in IEEE Transactions on Antennas and Propagation, vol. 58, no. 8, pp. 2515- 2522, Aug. 2010, doi: 10.1109/TAP.2010.2050418.

6.4 Tradespace Analysis of Ultra-Wide-Band (UWB) Fractal Antenna

(Sai Indharapu and Kalyan Durbhakula)

6.4.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. Their high degree of freedom provides an opportunity to develop systematically modified patch shapes, which in turn leads to improved bandwidth while retaining high

fidelity factor values. Machine learning (ML) can be leveraged to predict the antenna array response for an arbitrary design parameter space upon sufficient training and validation.

Sub-Problem:

(i) Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

(ii) ML can suffer from underfitting or overfitting the training model which in turn leads to deviations in the predicted output.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed:

(i) Design, simulate, validate, and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

(ii) Train, validate, test and compare multiple ML models for quicker and accurate prediction of antenna array response for different physical aperture areas.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

6.4.2 Tasks and Milestones / Timeline / Status

(A) Perform tradespace analysis of the fractal element radius *b* over the desired frequency range (4 to 12 GHz) using the genetic algorithm (GA) optimization tool available in the commercial electromagnetic (EM) solver FEKO / FEB21 / Complete.

- Milestone: Provide a recommendation of an optimum value of *b* using OPTFEKO to minimize reflection coefficient or S11 (< –10 dB).

(B) Perform tradespace study on different fractal shapes by changing the number of fractal segments to understand the effect of this change on the impedance bandwidth / FEB21 / Complete.

- Milestone: Produce a detailed study of the antenna response such as S11, gain, and bandwidth by varying the number fractal segments.

(C) Apply the GA optimization tool on the fractal side length *b* over a wide frequency range (2 to 12 GHz with 201 discrete frequency points) and number of fractal segments using OPTFEKO on the LEWIS cluster / MAR21 / Complete.

- Milestone: Reduce physical aperture area by 10% of its present design, reported in the FEB MSR, and demonstrate minimal or no change in S11, gain, and fidelity factor values.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a* / MAR–APR21 / Complete.

- Milestone: Recommend a value of *a* to reduce the physical aperture area and increase aperture efficiency (>50%) with no variation in other antenna metrics.

(E) Frequency scale fractal antenna design such that the center frequency of the resulting antenna equals 1.3 GHz / MAY21 / Complete.

- Milestone: Modify antenna design with a center frequency equal to 1.3 GHz and achieve similar results (3:1 bandwidth at fc = 1.3 GHz, 3 dBi gain and >130% aperture efficiency at 900 MHz) to antenna design at center frequency ~7 GHz.

(F) Design and simulate various array antenna geometries composed of optimized fractal antenna elements (obtained from (E)) to analyze the effect of overall array antenna geometry on the desired array antenna response metrics (i.e., gain vs. frequency, gain vs. elevation angle at constant phi, rE/V, half-power beamwidth and side-lobe level.) / MAY–JUL21 / Complete

- Milestone: Recommend a best possible structure with reduced aperture area and minimal loss in gain.

(G) Apply ML models available in Altair Hyperstudy (2021) on the fractal antenna to try and understand the possibilities and limitations of ML models for fast and efficient antenna metrics prediction and optimization. Through successful testing, a ML model can replace conventional EM simulators for faster optimization and prediction. / MAY–OCT21 / Ongoing.

- Milestone: Recommend most accurate and efficient ML model available in Altair Hyperstudy (2021) for a fractal antenna.

(H) Apply ML models on the octagon fractal antenna array lattice to extend the prediction capabilities of ML models. / SEP–NOV21 / Ongoing.

- Milestone: Recommend the best suitable ML model available in Altair Hyperstudy(2021) for array antenna metrics prediction.

6.4.3 Progress Made Since Last Report

(G1) The predicted output from ML models and output response from the EM solver (FEKO) for the same antenna design is used to calculate the relative error (RE), which is mathematically represented in equation 1, Relative error explains the deviation from the target value numerically.

$$Relative\ error\ =\ log(abs((y\ -\ \hat{y}\ )./(y)).*\ 100) \qquad (1)$$

Where y is antenna output response from FEKO, $\hat{y}$ is output response from the ML models (RBF, LSR).

(G2) Apart from RE, root mean squared error (RMSE) is also calculated to understand and to compare the error of each ML model in predicting each of the antenna output metrics. RMSE is a standard and traditional way to measure error especially on ML predicted data. Unlike RE, RMSE yields a single value which is mathematically represented in equation 2

$$Root\ mean\ squared\ error\ (RMSE)\ =\ sqrt(mean((y\ -\ \hat{y}\ ).\hat{}2)); \qquad (2)$$

6.4.4 Technical Results

(G1) Previously, ML models available in Altair Hyperstudy are tested for the prediction of single element fractal antenna output responses such as S11, gain, and electric field strength values at 3 distances (i.e., 100 mm, 200 mm, and 300 mm). To validate, each of the output responses is plotted against the output response of FEKO for the same antenna design. To show the prediction accuracy of the ML models, relative error has been calculated and is plotted in Figure 6.4.1. Overall, the relative error values from the RBF ML model vary less abruptly than the LSR ML mode. However, there is room for improvement. One reason for high relative error values is the minimum number of frequency points employed to train these models. We plan to extend the number of frequency points to 201 (from 30) to improve overall prediction throughout the frequency range.

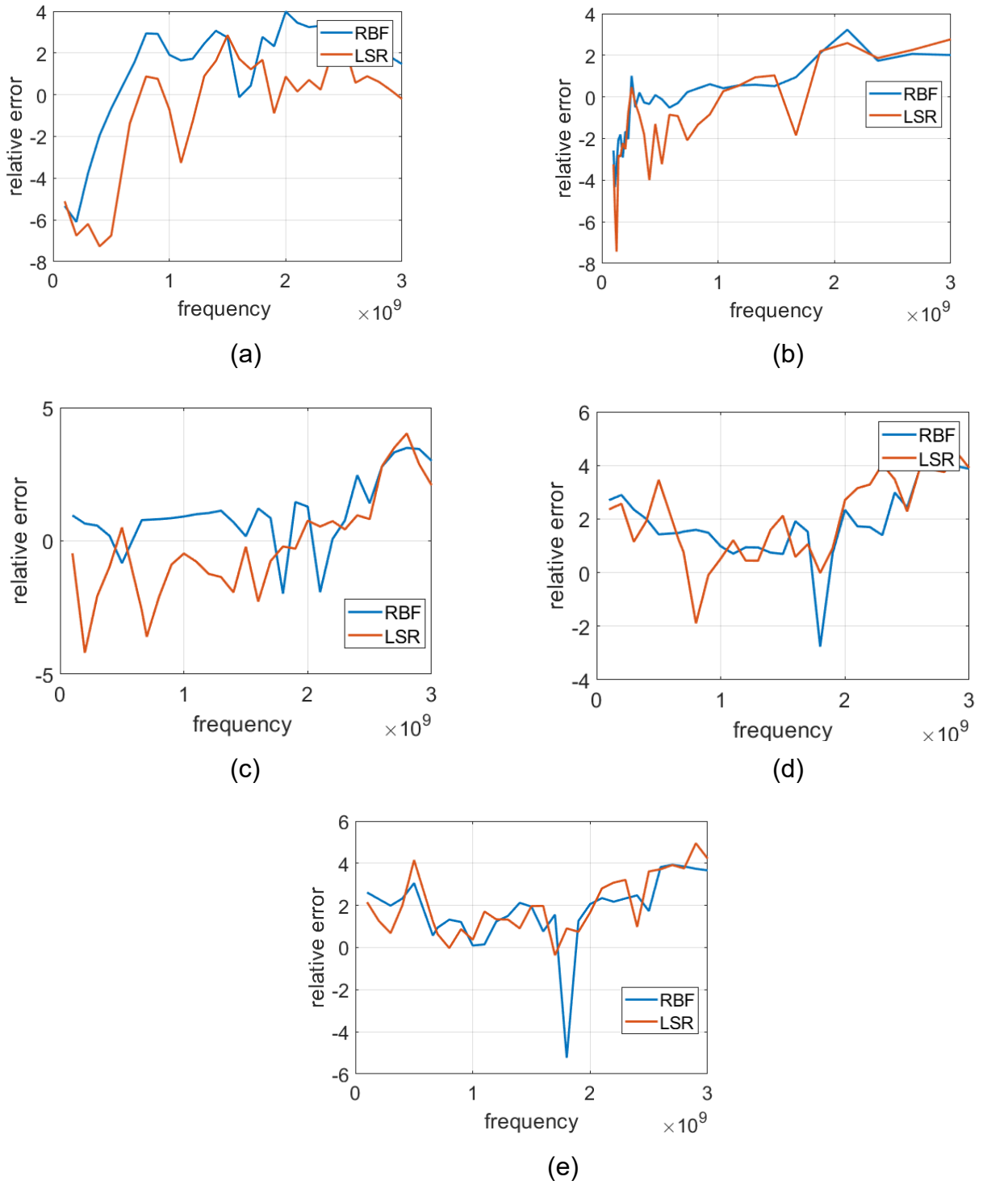


Figure 6.4.1: Relative error of ML models (RBF, LSR) and EM solver FEKO for (a) S11, (b) Gain, and the radiated E-field at a distance (c) 100 mm, (d) 200 mm, and (e) 300 mm from a fractal antenna.

(G2) RMSE is calculated between RBF and LSR for each of the antenna output response and tabulated in Table 6.4.1, RMSE for both RBF and LSR is less than zero indicating good generalization capability. In the comparison of RBF to LSR, the RMSE values from the RBF ML model are lower than the LSR ML model.

Table 6.4.1: RMSE comparison

Antenna output response		RMSE values	
		RBF	LSR
S11		0.0430	0.0108
Gain		0.4517	0.5325
E-field at	100 mm	0.0280	0.0268
	200 mm	0.3972	0.7249
	300 mm	0.3505	0.9228

6.4.5 Summary of Significant Findings and Mission Impact

(A) The initial analysis of the simulation results with fractal radius *b* equal to 1.8 mm yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO has been used as an optimization tool with fractal radius *b* as the optimization variable. The optimum value for *b* is found to be 1.66 mm. A comparison between reflection coefficient for initial *b* (= 1.8 mm) value and the optimized *b* (= 1.66 mm) can be found in Figure. 6.4.6. The optimization is carried out over 51 discrete frequency points.

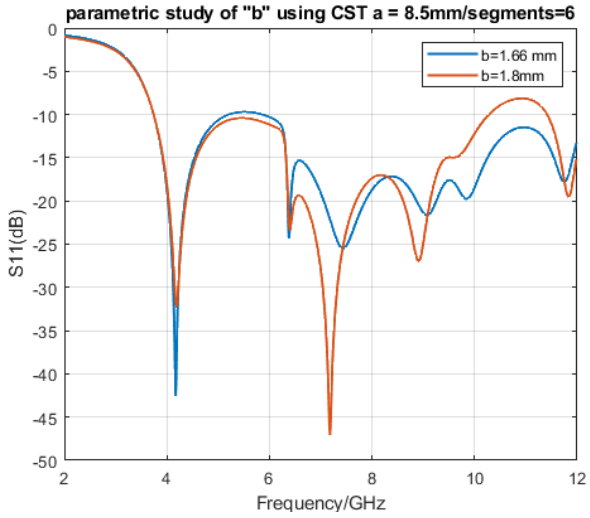


Figure 6.4.6 Reflection coefficient of fractal antenna for initial and optimized *b* value.

(B) The addition of fractal elements (*N*) to the simple hexagon improved antenna metrics such as S11. To further investigate and understand the fractal elements, the number of segments in the fractal geometry has been varied. The improvement in bandwidth is observed as the value of *N* is increased from 6 to 14.

(C) The initial optimum value of *b* over 51 discrete frequency points is reported as 1.66 mm in task (A). To further increase the accuracy of the optimization algorithm and to find a more precise value for *b*, optimization is further performed over wider frequency points (201 discrete points between 2 GHz to 12 GHz) which yielded the optimum value of b as 1.368 mm. The S11 response of antenna design with newly found *b* (i.e., 1.368 mm) hasn't produced any better bandwidth with respect to *b* (= 1.66 mm). Thus, *b* is set to be 1.66 mm for further research.

(D) The hexagonal patch radius *a* has a significant effect on the physical aperture area of the antenna. Therefore, Altair OPTFEKO has been utilized to find an optimum *a* value, which was found to be 8 mm over the range 7.2 to 9 mm. Antenna metrics such as S11, gain, and bandwidth have shown desired performance with the optimized *a* value.

(E) The initial antenna design has been modified to achieve a center frequency of ~1.3 GHz. The gain value at 900 MHz is 3.5 dBi and, with the modified antenna design, we were able to achieve an impedance bandwidth ratio of 3.3:1. The designed antenna has been fabricated and tested, and the S11 response of the fabricated antenna agrees well when compared against FEKO, CST.

(F) To summarize, four different fractal antenna array geometries (i.e., square, diamond, hexagon, and octagon) have been designed and simulated. The antenna array with square geometry has the largest physical aperture area (714.025 m^2) and the highest gain at 900 MHz (17.07 dBi). However, from the gain as a function of theta plot, square array geometry has very high sidelobe levels. Antenna array geometry with octagonal shape minimal sidelobe levels with gain (15.715 dBi) at 900 MHz close to that of square geometry with 32.27% lower physical aperture area than that of square

geometry. The octagonal fractal antenna array has been chosen as the optimum geometry with reduced aperture area and reduced side lobes while retaining the BW and gain milestone metrics.

(G) The initial prediction of reflection coefficient (S11) from the three ML models was satisfactory and has shown a good agreement against the FEKO response. In addition, radial basis function (RBF) and least square regression (LSR) were down selected from the initial three ML models basing upon the generalization capability. Further analysis of increasing training data set size has shown no improvement in prediction accuracy. As a result, the training data set is fixed to 10 for further studies. Moving forward, the above-mentioned ML models are trained and tested to predict the gain as a function of frequency, the electric field strength in the far field. The RMSE values shown in Table 6.4.1 indicate that the RBF ML model is superior to LSR for prediction of single element fractal antenna metrics.

6.4.6 References

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

7.0 RF Coupling

7.1 Enclosure Effects on RF Coupling

(Mohamed Hamdalla and Ahmed Hassan)

7.1.1 Problem Statement, Approach, and Context

Primary Problem: UAVs are typically considered metallic/dielectric enclosures depending on their frame material. The shielding effectiveness of such enclosures might be compromised due to the slots and gaps on these enclosures, creating upset susceptibility to the enclosed electronics. The goal of this work is to quantify how the thresholds for upset susceptibility of enclosed wires and integrated circuits differ from those in free space.

Solution Space: Study enclosures with different shapes, material compositions, and slots to quantify their effect on RF coupling to the enclosed wires and electronics typically used in UAVs. The study will focus on the low-frequency range where the incident wavelength is comparable to the size of the enclosure or larger.

Sub-Problem: UAVs are manufactured with a wide variety of shapes and composites to accomplish an exponentially expanding list of missions. The configurations previously reported in the literature have simplistic assumptions regarding the shape and material composition of UAV enclosures that might overestimate or underestimate susceptibility.

State-of-the-Art (SOTA): Simple statistical analysis of specific enclosure configurations using either brute force simulations/measurements or pure statistical methods. Also, simplified UAV wire distributions are assumed.

Deficiency in the SOTA: Brute force simulations/measurements of the voltages and currents induced in wires and integrated circuits contained in enclosures are computationally or experimentally complex and have several limitations. The computations are complicated by the multiscale nature of the simulations, and the experiments are complicated by the cost of the equipment and the extensive time needed to measure every variation to cover all possible scenarios. Statistical methods, such as the Random Coupling Model (RCM) for example [1], are only accurate for high frequencies where the wavelength is much smaller than the size of the enclosure. Another main deficiency of the RCM is that it can't predict the exact induced voltages and currents for a specific well-characterized system but it only provides the statistical properties of these induced currents and voltages.

Solution Proposed: Apply Characteristic Mode Analysis (CMA) to identify the fundamental modes of the enclosure, current distribution, and the field pattern of each mode. This will allow us to predict the worst-case RF coupling scenarios without the need for lengthy simulations and/or expensive experimental measurements. The proposed approach can predict measurements at a fraction of the cost/time. Moreover, we propose to study RF coupling to realistic UAV wire distributions, experimentally reconstructed, when they are placed inside metallic/dielectric UAV enclosures.

Relevance to OSPRES Grant Objective: Provide general guidelines on how the environment, in this case, the enclosure, affects RF coupling and subsequent electromagnetic absorption to UAV wires and integrated circuits.

Risks, Payoffs, and Challenges: The modes depend mainly on the shape and material of the enclosure. Since UAVs have a wide variety of shapes and material compositions, a library of several UAVs needs to be studied before general quantitative conclusions can be drawn. Challenges can be mitigated by the use of the classification techniques of Machine Learning (ML). That is, different ML techniques will be evoked to detect hidden patterns on how the shape, material composition, and the shape/size location of slots correlate with the field enhancement inside the enclosure.

7.1.2 Tasks and Milestones / Timeline / Status

A. Complete the CMA implementation for studying the shielding effectiveness of metallic enclosures. Validate whether CMA can predict the worst-case shielding effectiveness of metallic enclosures as a function of their shapes. / JAN21 / Complete.

   A1. Prepare a manuscript for IEEE AWPL to document the progress done in A. / Ongoing.

B. Progressively build an accurate representation of the UAV wiring system with all of the integrated circuit (ICs) and electronics to test assist the predictions of (c) and the experimental measurement of the actual UAV. / JUL21 / Complete.

C. Address the 2021 UAV's semi-annual review recommendations to study arbitrarily shaped UAV wire distribution. / JUNE21 / Complete.

D. Define the main RF coupling pathways to UAVs, i.e. is RF coupling to the wires/traces the dominant pathway or is it the direct coupling to the electronics, and also quantify the sensitivity of these coupling pathways to load and wire variations. / December 21 / Ongoing.

7.1.3 Progress Made Since Last Report

D1. Conclude a rule of thumb for the most sensitive parts of the UAV system.

D1.1. In the previous MSRs, we developed an accurate model for the completer wiring system of a UAV and developed the Equivalent Circuit Approach to efficiently run hundreds of RF coupling simulations to the UAV. The goal of these experiments is to examine if RF coupling to the wires/traces is what leads to the majority of voltage or power coupled to the UAV electronics. Figure. 7.1.1b shows the wiring diagram of the actual UAV with the different IC components. We built an accurate replica of the UAV in Fig. 7.1.1a using the full-wave electromagnetic solver FEKO which is shown in Fig. 7.2. The wires' length and diameters match the values in the actual UAV in Fig. 7.1.1a and match the values in Table 7.1. We also used the Equivalent Circuit Approach (ECA) as an effective tool to test different linear/nonlinear loads. This will facilitate studying many different loads accurately using minimal computationally time. The theory behind the approach has been discussed in detail in MSRs for N00014-17-1-2932.

This month we integrated the UAV wire system to our proposed Predictive-package for Electromagnetic Coupling to Nonlinear-electronics using Equivalent-circuits & Characteristic-modes ”PECNEC”. PECNEC also has been discussed in detail in contract reports for N00014-17-1-2932. PECNEC is a package that determines the RF-induced overvoltage conditions on linear/non-linear circuit elements using SPICE solvers ~ 100x faster than full-wave simulations with no loss in accuracy. Integrating the UAV model will allow users to run computational RF coupling simulations to a UAV and compare the simulations to their experimental measurements.

7.1.4 Technical Results

Figure 7.2 shows the UAV wire model implemented with PECNEC. All the blue dots in Fig. 7.2 represent 50 Ω loads. However, next month, we will update this version to let the user define all the blue dot impedance values based on experimental input impedance measurements from different electronics.

In the first version, the user will be able to vary one of the 4 loads connecting the signal wires to the ground plane of the main controller labeled 1,2,3, and 4 in Fig. 7.2. Once the user selects the load of interest, the other 3 loads will be automatically terminated by 50 Ω loads. This also will be updated next month to give the user the option to decide the values of all loads. The studied load can be any of the three supported loads in PECNEC namely, Parallel RLC load, series RLC load, or diode.

To test the accuracy of PECNEC to estimate the coupled voltage across one of the UAV loads, we picked Load 1 to be tested. For this analysis, a random RLC series load is selected to be tested at port 1 in the UAV in fig. 7.2. The load consists of a resistor R = 200 Ω, inductor = 1 μH, and a capacitor C= 1 nF.

We excited the UAV with 10 different Gaussian sinusoidal pulsed. Ten gaussian sinusoidal pulses centered at different 10 different frequencies, ranging from 0.1 GHz to 1 GHz with 100 MHz steps, are used to excite the UAV. The bandwidth of all pulses is kept constant, 38 MHz and they all have the same 240 V/m amplitude. The maximum induced time-domain voltage across the series RLC load is then calculated. Figure 7.3(a) illustrates the maximum induced voltage across the series RLC load when the 10 different pulses are used to excite the UAV model. Two curves are shown in Fig. 7.3(a), the red curve represents the values calculated directly from the full-wave solver and the blue curves represent the values calculated from PECNEC. If we pick a random point in the horizontal axis of Fig. 7.3(a), e.g. 200 MHz, the red curve reads ~ 70 V. This means that if the DUT in Fig. 7.2 is excited by a Gaussian pulse that is centered around 200 MHz, the maximum value of the induced time-domain voltage across the load will be ~ 70 v.

Figure 7.3(b) compares the relative difference between the FEKO and PECNEC values, and it shows that the relative error is less than 5%. Hence the package can accurately estimate the response of the UAV model for the specified sample load. It is important to re-emphasize that the circuit solver, LtSpice, is used to extract the time domain load voltage of the system circuit representation. Since the computational time of Spice is ~ 100x faster than full-wave simulations, several experiments can be done in spice efficiently. The proposed package will allow the user to test many load combinations in a few seconds since Zin and Voc of the system are independent of the load parameters.

Therefore, no need to repeat the full-wave simulations. Hence, huge computational time-saving yet high accuracy is achieved. This will help us answer the question if the RF coupling to the wires is what causes the majority of the voltage and power sensed by the electronics. We can also assess how variations in the electronics' impedances affect the coupled voltage and power.

Table 7.1. Quadcopter's main circuitry components and wires.

Part function	***Part #***	***Specs.***	***Length***
motor feed lines	1	18 AWG	
ESC out power lines	2	16 AWG	
ESC in power lines	3	16 AWG	~20 cm
esc in signal	4	22 AWG	25 cm
battery out	5	14 AWG	
battery to controller	6	22 AWG	
main controller (autopilot)	7		carrier board 9.5 cm x 4.5 cm
GP.1575.25.4.A.02 GPS/Galileo 25*25*4mm 1575.42MHz Patch Antenna2	8	22 AWG	~20 cm
Readytosky® 2212 920KV Brushless Motors	9		
SimonK 30A ESC Brushless Speed Controller	10		
Pixhawk Power Module 5.3V BEC XT60	11		

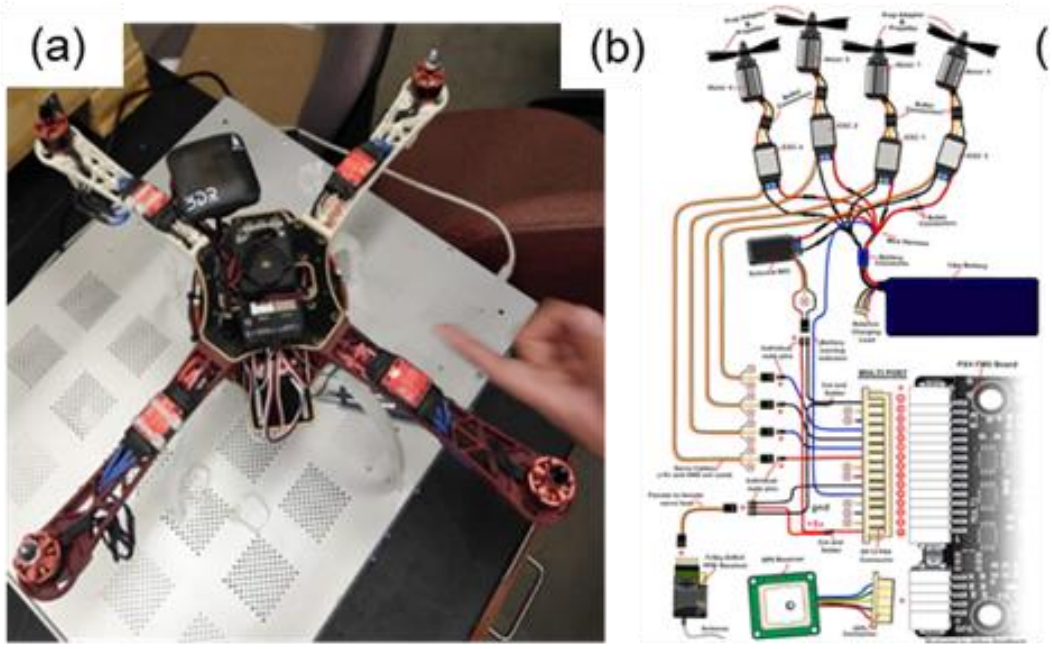


Fig. 7.1. (a) Model of the realistic UAV circuitry showing the wires, components, and frame, (b) the UAV wiring diagram showing all the wires and components.

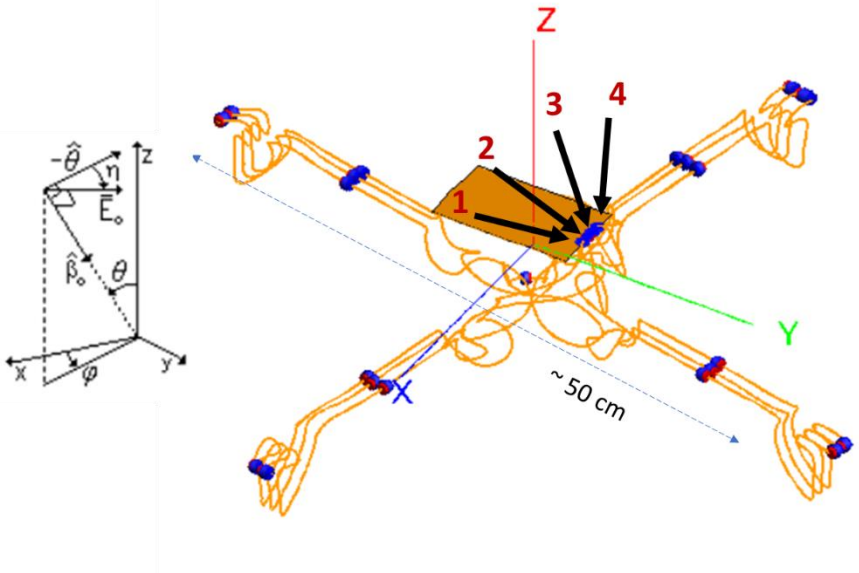


Fig. 7.2. The FEKO model of the UAV used in PECNEC

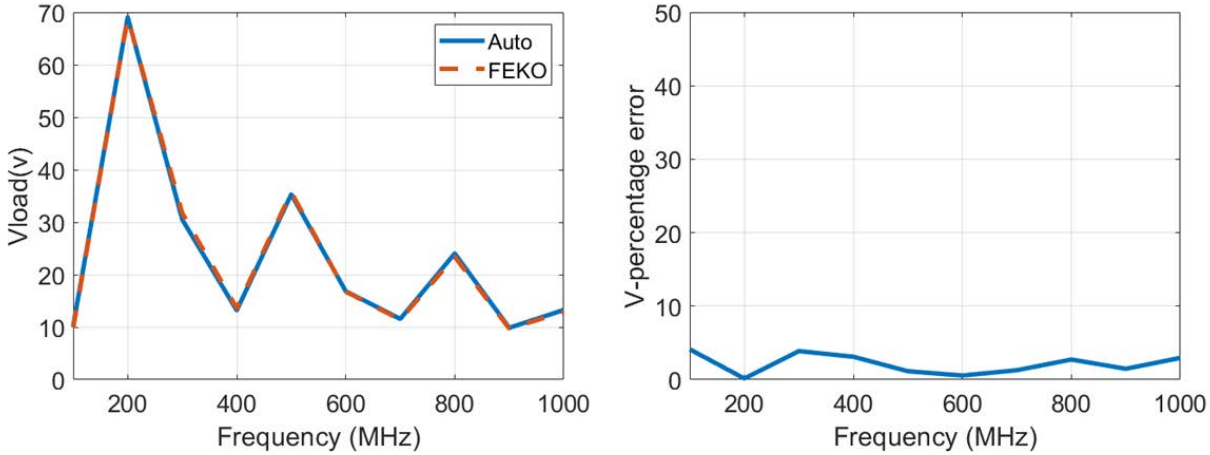


Fig. 7.3. Comparison between the maximum voltage across the series load calculated using FEKO (red color) versus the Package (blue color). (b) Percentage error between the maximum voltage across the load calculated using FEKO and the Package.

7.1.5 Summary of Significant Findings and Mission Impact

A. A fast full-wave tool that facilitates studying the effect of a metallic enclosure on shielding effectiveness has been developed using CMA.

B. Developed an accurate model for the complete wiring system of an UAV, integrated the model with PECNEC, and validated the implementation with rigorous full-wave simulations.

C. Two Second series equivalent circuit branches/resonance is the best combination for the RLC circuit to accurately represent Zin of the system.

8.0 Laser Development

8.1 Fiber Lasers and Optical Amplifiers

(Heather Thompson and Scott Shepard)

8.1.1 Problem Statement, Approach, and Context

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$100K to \$300K to drive our Si-PCSS applications.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution (with respect to traditional fiber and traditional free-space laser designs). Novel optical amplifier tubes, however, might operate at far higher power levels (over 1000 times greater), thus driving an entire array of PCSS with a single amplifier and thereby reducing the overall system costs and eliminating the optical pulse-to-pulse jitter constraints.

Sub-Problem (1): Optical pump power system costs account for over 50% of the budget for each laser (in this class, for normal/free-space, optical fiber, and tubular embodiments).

Sub-Problem (2): Fiber (as well as power tube) optical amplifier performance is degraded primarily by amplified spontaneous emission (ASE) noise, which limits the operating power point, and by nonlinearities, which distort the optical pulse shapes.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive for the PCSS applications until reduced by a factor of at least two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping technique (wherein we pump at a lower level over a longer time) which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments, we are pursuing the use of gain saturation and a staged design of different fiber diameters. We also apply these techniques to fiber amplifiers which incorporate our power amplifier tube in the final stage. The inclusion of our novel tubular-core power amplifier stage should permit a single laser to trigger an array of several PCSS (reducing system cost and mitigating timing jitter).

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system enables PCSS systems for viable deployment via: a factor of 40 in pumping cost reduction of each laser; and a factor of *N* in system cost reductions as a single laser could drive *N* (at least 12) PCSS in an array, while also eliminating the optical jitter constraints.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of

dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability. The main challenge for power tube implementation is the entrance optics design.

8.1.2 Tasks and Milestones / Timeline / Status

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Ongoing.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Ongoing.

(E) Demonstrate a cost-reduced fiber laser. / Ongoing.

(E1) **March 2021** Finalize design. / Complete.
(E2) **April 2021** Assemble and test-check seed LD (laser diode)/driver. / Completed.
(E3) **April 2021** Measure power vs current transfer function of seed LD/driver. / Completed.
(E4) **May–July 2021** Measure ASE and jitter of 1064 nm seed LD/driver. / Completed.
(E5) **May–July 2021** Measure ASE and jitter of 1030 nm seed LD/driver. / Completed.
(E6) **June–July 2021** Assemble and test-check pump LDs/drivers. / Completed.
(E7) **June–July 2021** Measure power vs current transfer function of pump LDs/drivers. / Completed.
/ (E8) – (E14) Delayed due to vendor issues (see MAY MSR).
(E8) **September 2021** Splice power combiners to Yb doped preamp fiber.
(E9) **September 2021** Connect seed and pumps to power combiners and test-check.
(E10) **September–October 2021** Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle.
(E11) **September–October 2021** Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle.
(E12) **November 2021** Splice power amplifier and its power combiner to best preamp.
(E13) **November–December 2021** Measure gain, ASE and jitter of entire amp assembly.
(E14) **December 2021** Analyze data and document.

(F) Design a new type of higher power, tubular core, fiber amplifier. / Ongoing.

(F1) Apply one high-power tubular amplifier to a system comprised of an array of several PCSS (e.g, 12 in a 4x4 array) thereby eliminating jitter constraints and reducing laser system cost by more than a factor of 100 (independent of burst profile). / Ongoing.

8.1.3 Progress Made Since Last Report

(E4–E5) A typical sample/run of a 1000 pulse set of optical pulse-to-pulse timing jitter measurements is exemplified in Fig. 8.1.1. In this sample data (for the 1030 nm seed

laser diode), 848 of the 1000 pulses were within +/- 15 ps, thus the performance is within spec. The ASE was measured to be negligible (below a detector noise floor of 0.8 nanowatts) for both the 1030 nm and 1064 nm laser diodes. This is as anticipated (but needed confirmation) since no additional optical amplifier was incorporated. Any laser, however, implies an amplification (of the vacuum state fluctuations). The measurement confirms our expectation that for our detector bandwidth (of 5 GHz) the ASE noise is below 1 nanowatt.

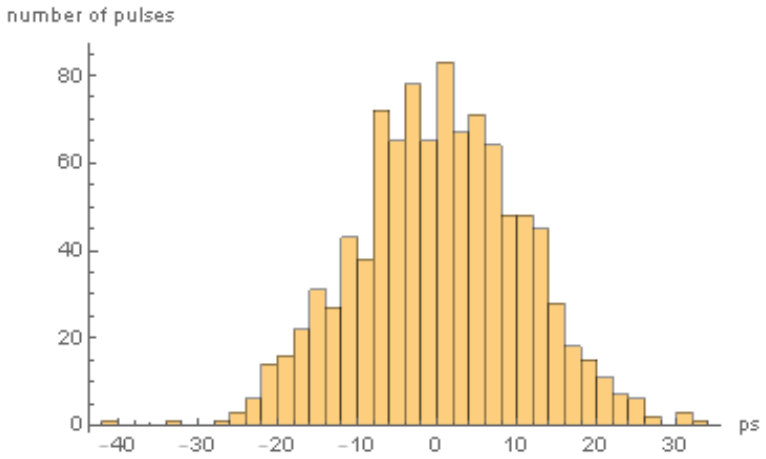


Fig. 8.1.1 Sample data of the optical pulse-to-pulse timing jitter for the 1030 nm seed laser diode.

(E6–E7) Pump laser diodes (which operate at 915nm) were assembled into the thermal mounts and their high-current/low-noise drivers were test-checked and configured. A measured power versus current transfer function, presented in Fig. 8.1.2, shows the anticipated linear dependence of output power on input current (apart from an almost quadratic dependence at low currents). The blue line is an LMS fit (to a line) of all the data (shown in red) which has a slope of 0.81 [W/A]. The diodes should be capable of an output power of 10 W, but we didn't want to risk damaging any before we can deploy them in the fiber preamp experiments. The splicing of the power combiners to the fiber preamp by an external vendor is nearly complete and is expected to arrive on schedule.

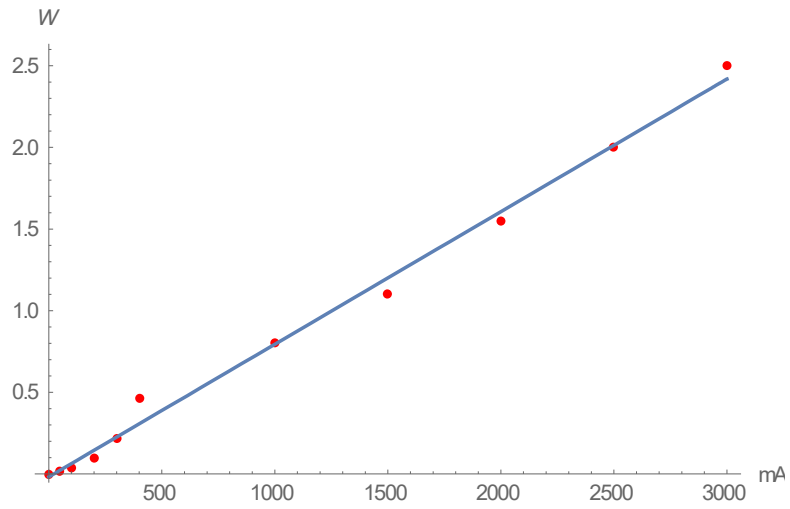


Fig. 8.1.2 Optical output power vs electrical input current of a 915 nm pump laser diode.

(F) In an optical fiber, or cylindrical-rod or rectangular-slab waveguide, the self-focusing process refracts energy out of the waveguide and this energy is lost (no longer guided). This limits the operating power of the waveguide. In a tubular core geometry, however, we suspected and confirmed that two effects dramatically alter the situation: 1) the energy is preferentially refracted into the inside of the tube – due to the symmetry breaking and 2) the would-be-lost energy is collected back into the waveguide, assisting in the growth of the hollow-core mode in air. Evidence of both the symmetry breaking and the accumulation effects are described in 8.1.4 and depicted in Fig. 8.1.3.

(F) We submitted an abstract to the DEPS 2012 DE Systems Symposium: Tubular Core Optical Power Amplifier, S. Shepard and A. Caruso.

(F1) Timing jitter between the elements (the individual PCSS) within an array is a major constraint on the overall system design, as it not only limits steerability of the microwave beam but it could also lead to uncontrollable collateral damage. These, in turn, have imposed stringent constraints on the lasers in a variety of system architectures. Even if the optical pulses from a single seed laser were to drive a larger number of optical amplifiers (one for each PCSS) the pulse-to-pulse timing jitter within each amplifier must be limited. The very high-power potential of our tubular optical amplifier (and the existence and uniformity of its air-core mode), however, introduces a new possibility. Uniformly splitting a large cross-sectional area of very high power from one tubular amplifier into several power-delivery fibers (one or more for each PCSS) would eliminate the optical pulse timing jitter constraint. Note, in this way the problem could be removed entirely, since each power delivery path is passive. Fig. 8.1.4 depicts a preliminary design in which we use 37 power-delivery fibers to drive an array of 12 PCSS, with 3 fiber legs each (resulting in one fiber to be used as a power monitor). Technical details described in 8.1.4.

demonstrate tubular amplifier power levels (and spatial uniformity) sufficient to drive over 12 PCSS at tens of MW peak power each.

8.1.4 Technical Results

(F) In addition to the simple geometric advantages inherent in a tubular core power amplifier (larger surface areas and thin walls) we have identified another mechanism for advancing the SOTA. Self-focusing refracts energy out of most waveguides and this energy would normally be lost (no longer guided), thus limiting the operating power of the waveguide. In a tubular core geometry however, such a process is dramatically opposed by both a symmetry breaking and an accumulation effect. Evidence of symmetry breaking is depicted in Fig. 8.1.3 a) and b) wherein part a) shows the electric field distribution from a Gaussian beam illuminating a spot on the glass tube at the input plane. Fig. 8.1.3 b) shows the electric field distribution after propagating only 1 micron away from the input plane and we note the preferential scattering of light towards the inside of the tube. If the tube was replaced by a flat rectangular slab waveguide then the scattering would be symmetric (i.e., equal on both sides). The curvature of the surface, in the tubular case, has broken the symmetry. Moreover, that energy, which otherwise would have been lost, is collected by the rest of the tube as it has created the hollow-core mode into which it couples. This accumulation effect is demonstrated in Fig. 8.1.3 c) which shows the growth of the hollow-core mode (in air) over a propagation distance of 10 microns.

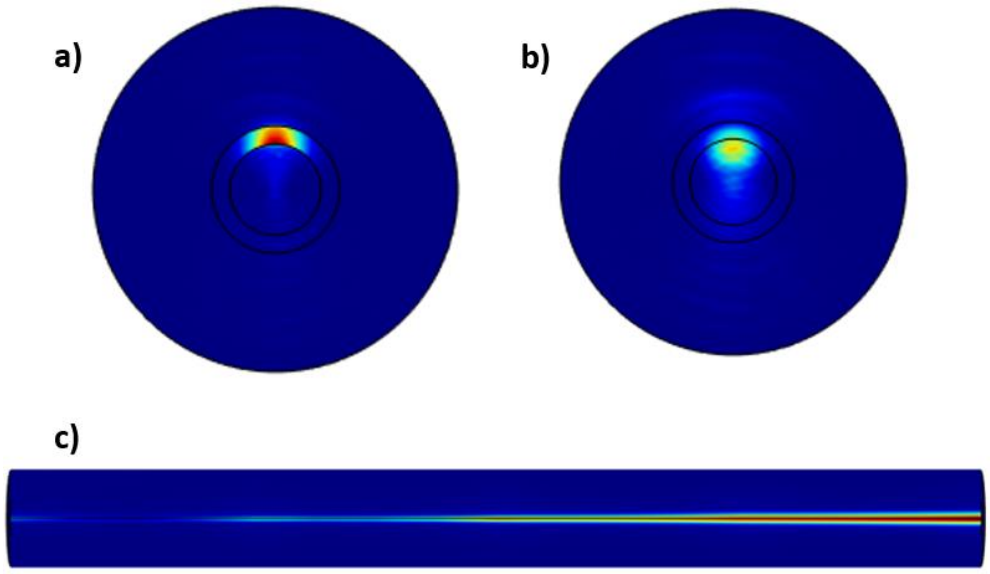


Fig. 8.1.3 a) Input beam spot on glass tube, providing **b)** evidence of symmetry breaking, leading to **c)** the accumulation of energy in the hollow-core mode of the tube.

The significance of these results should not be underestimated as they permit a dramatic increase in the operating power of optical waveguides and optical amplifiers. Whereas 100 kW fiber amplifiers are cutting-edge technologies; we are now pushing the state of

the possible into the realm of tens of GW (within a single tubular waveguide). The impacts for OSPRES include dramatic cost reductions as a single amplifier could drive a large number of PCSS in an array. An example of how this can also lead to an elimination of optical jitter constraints is presented in the following.

(F1) The very high-power potential of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) introduces new applications and architectures. Uniformly splitting a large cross-sectional area of very high power from one tubular amplifier into several power delivery fibers (one or more for each PCSS within an array) would eliminate the optical pulse timing jitter constraint. Since each power delivery path is passive they cannot contribute to jitter (even the thermal expansions of their lengths will be identical because each contains an identical stream of optical pulses). Fig. 8.1.4 depicts a preliminary design in which we use 37 power-delivery fibers to drive an array of 12 PCSS, with 3 fiber legs each (resulting in one fiber to be used as a power monitor).

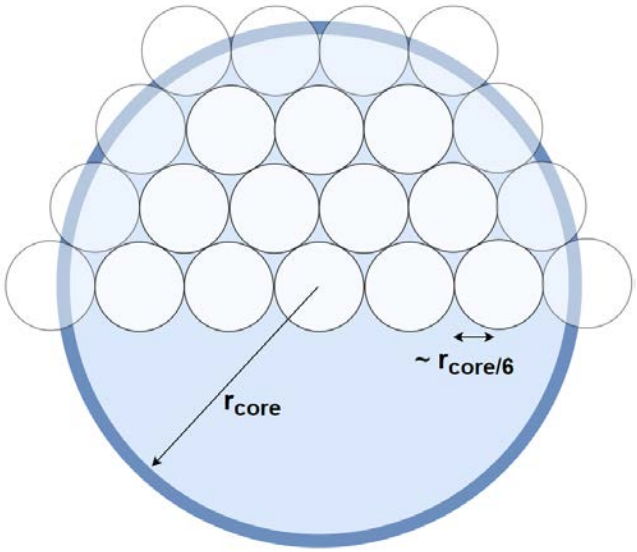


Fig. 8.1.4. Splitting a tubular amplifier output into 37 passive power-delivery fibers.

The optimal stacking of small circles (fibers) to cover the area of a larger circle (a tube) results in a hexagonal shape of 7, 19, 37, 69… fibers. Within our choice of 37, the fiber diameters and tube wall thickness can be optimized (given a desired tube radius) for minimal power loss and/or uniformity of power distribution. A rigorous optimization would require some development; however, this can be circumvented via approximations and a close to optimal solution produced. Given a desired 2.5 mm outer diameter tube, we find that the fibers can be uniformly illuminated within 10% via a fiber radius of 202.7 microns and a tube wall thickness of 67.6 microns; when the power in the tube's glass wall is four times the power in its air core. Uniform illumination of the fibers is not an overriding factor since if required it is readily accomplished via attenuation.

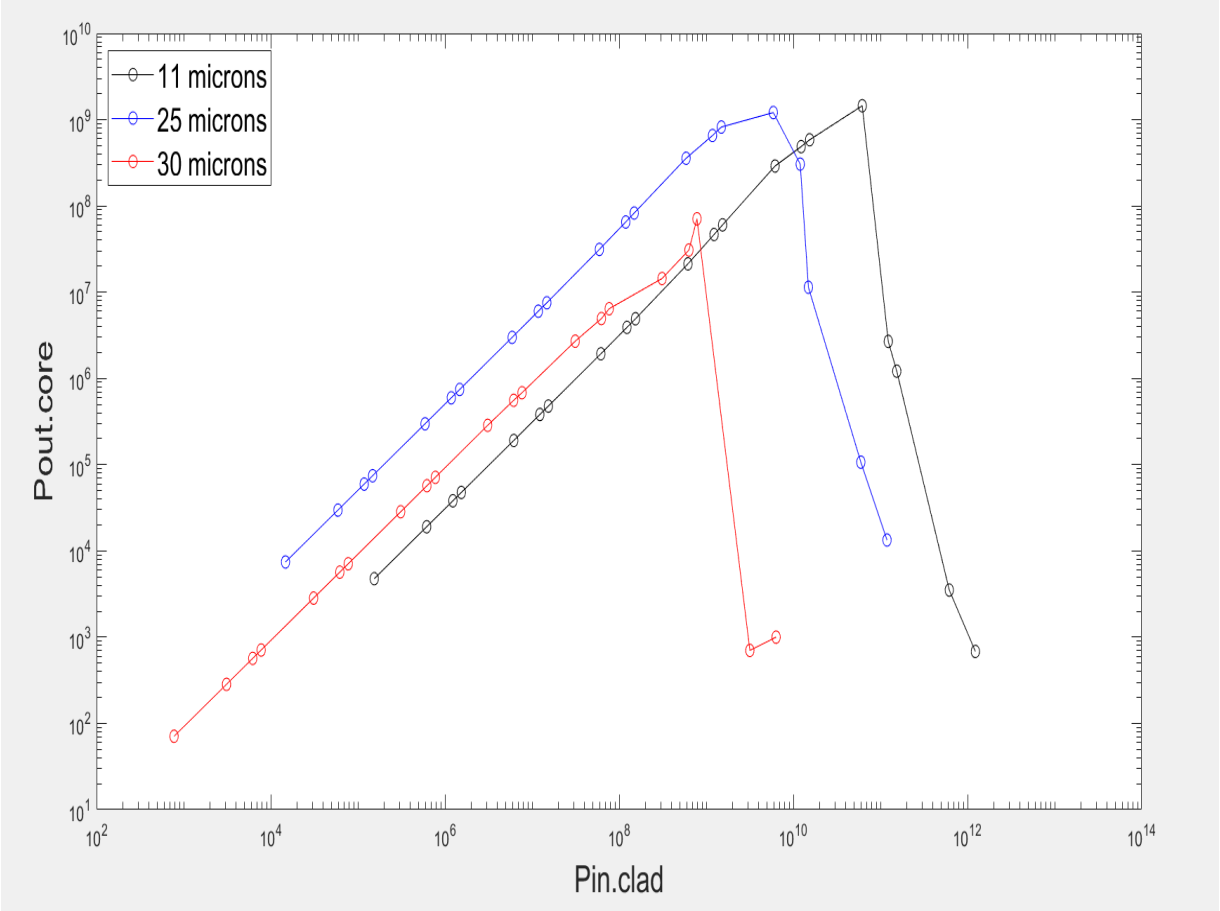


Fig. 8.1.5 Air-core power vs glass-cladding operating power at various tube wall thickness.

In the JULY2021 MSR we noted that equal amounts of power can be achieved in the tube's core/air mode and its cladding/glass mode, when the operating point is near 0.5 GW (for a wall thickness of 100 microns). In August we find that we can greatly extend that operating point by decreasing that thickness, as demonstrated in Fig. 8.1.5. For example, we could (with a wall thickness of 11 microns) operate the amplifier near 40 GW while supporting an air-core power of 1 GW. Note that if a PCSS required a laser pulse energy of 240 μJ, in a pulse width of 24 ps, we need a laser capable of handling 10 MW of peak power. In terms of the limitations imposed by self-focusing, a single tubular optical power amplifier could withstand the peak power required to simultaneously drive 100 such PCSS, and since it holds thermal and other nonlinear scattering advantages (just from the merits of its geometric scale) this is a technology worthy of consideration.

8.1.5 Summary of Significant Findings and Mission Impact

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with pre-burst ASE power levels below the heating level tolerance of 100 μW. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our heating level spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) The design of a proof-of-concept experiment demonstrating a cost-reduced optical pumping scheme was finalized MAR2021.

(F) We made (to our knowledge) the first observation of self-focusing effects that are not determined by beam power alone. We found instead that these can also be controlled via the geometric factors within a waveguide (such as fiber core diameter) MAY2021.

We additionally made (to our knowledge) the first observation that a mode exists in the air within a simple glass tube into which we can couple energy from the mode in the glass. Thus, an amplifier (in the doped and pumped glass) can operate at higher powers JUNE2021.

8.2 WBG-PCSS Enabled Laser Diode Array Driver

(John Bhamidipati)

8.2.1 Problem Statement, Approach, and Context

Primary Problem: Need for heavy (~125 lbs.), bulky (~10 cu-ft), and expensive (~$120,000) conventional laser systems (1064 nm) in PCSS-based HPM applications, with an additional need for second and third harmonic generation (SHG/THG) optics to trigger wide bandgap (WBG) solids (GaN/SiC).

Solution Space: Design and implement a compact (~1.1 cu-ft), lightweight (10–15 lbs.), and inexpensive (<$15,000) alternative for conventional high average power optical trigger (laser) system to improve SWaP-C^2 index of HPM systems.

Sub-Problem: Unavailability of commercial-off-the-shelf (COTS) miniature optical sources with sub-nanosecond pulse widths and tens-of-μm beam width, delivering >1-Watt power to implement as a makeshift/turnkey solution for the laser system.

State-of-the-Art (SOTA): High average power picosecond pulsed lasers available up to 50 W output power with a gain factor up to 40 dB (~10,000x power) with laser amplifier.

Deficiency in the SOTA: High average power 1064-nm pulsed lasers are bulky and require auxiliary systems as well as additional optics for SHG/THG generation for WBG device triggering.

Solution Proposed: Multi-stage laser diode array/stack (LDA/LDS) driver powered by seed-laser-diode-driven avalanche WBG-PCSS as a compact, inexpensive laser replacement.

Relevance to OSPRES Grant Objective: Provides an enhanced SWaP-C^2 compliant solution for the laser (optical trigger) subsystem, with a subsequent impact on overall HPM system cost, volume, and power (optical and electrical) requirements.

Risks, Payoffs, and Challenges: Complex interconnect and thermal management system (TMS) design at high temperature (130–175°C) operation; unavailability of COTS high power pulsed laser diodes could potentially raise a need for research in laser diodes (arrays).

8.2.2 Tasks and Milestones / Timeline / Status

(A) Complete initial feasibility study for the cascaded multi-stage optical amplifier design and determine functional requirements for the laser diodes (arrays) and source driver [DEC–JAN 2020 / completed].

(B) Complete initial stage experimental implementation of the PCSS-based driver and demonstrate positive current gain using GaN-PCSS, triggered with a 404 nm laser diode. [AUG–SEP 2021 / in progress].

(C) In addition to (B), investigate potential alternatives to GaN-PCSS in both PCSS and non-PCSS domains. [AUG–SEP 2021 / in progress].

(D) Define performance metrics for PCSS-based driver and complete numerical calculations for required output current at each stage and corresponding PCSS (GaN/GaAs) operating voltages in light of electric fields required for lock-on/avalanche mode, establish real-time implementation timeline, cost estimates, jitter limitation, and explore ways to protect LDA from PCSS ringing. [MAR 2021 / partially complete / revisit after completing (B)].

(E) Demonstrate a tunable SiC-MOSFET-powered frozen wave generator (FWG) prototype on a custom-built PCB with Cree/Wolfspeed MOSFET(s), and 50 Ω coaxial cables and/or microstrip transmission lines capable of generating chirped pulse widths. [JUL–AUG 2021 / complete]

(F) Demonstrate a MOSFET-enabled tunable FWG on a 3″ × 4″ PCB using lumped-element-based transmission lines [AUG–SEP 2021]

(G) Proof of concept testing of the two-stage PCSS-enabled driver system with a 50 Ω load at 1 kHz pulse repetition rate (PRR) [OCT–NOV 2021]

(H) Working prototype demonstration at ~MHz PRR with laser diode array/stack and ancillary optics based on HPM source driver needs including thermal management system (TMS). [NOV–DEC 2021]

8.2.3 Progress Made Since Last Report

(E) The second iteration of a chirp-capable SiC-MOSET-powered FWG has been retested for repeatability and the results for 2-, 4-, and 8-segment coaxial

transmission line configurations with balanced (BL) and unbalanced (UBL) loads have been tabulated in Table 8.2.1. Non-simultaneous switching phenomena resulting in pulse overlap and/or deconstructive interference still need to be addressed. The fabricated 8-segment coaxial cable transmission line is shown in *Figure 8.2.1.*

Figure 8.2.1: An 8-segment coax-based chirp-capable SiC-MOSFET-driven FWG.

(F) To demonstrate an improved form factor, a modular lumped-element (L-C networks) based FWG prototype capable of operating in 4- or 8-segment configuration has been designed on a 4″ ×5.5″ PCB and was tested under balanced and unbalanced load configurations. Surface mount inductors and capacitors were selected such that a 50-Ω characteristic impedance is maintained in every transmission line segment. While the experimental implementation of 4-segment configuration was found to be in agreement with the simulated results and demonstrated up to 76% power transfer for balanced and unbalanced loads, the 8-segment configuration under unbalanced load behaved like a 4-segment configuration with higher output voltage amplitudes. Parasitics induced by the additional traces included for modularity are suspected to prevent the transmission line charge/discharge, which will be investigated in the next report cycle. The lumped-element-based FWG prototype is shown in *Figure 8.2.2*.

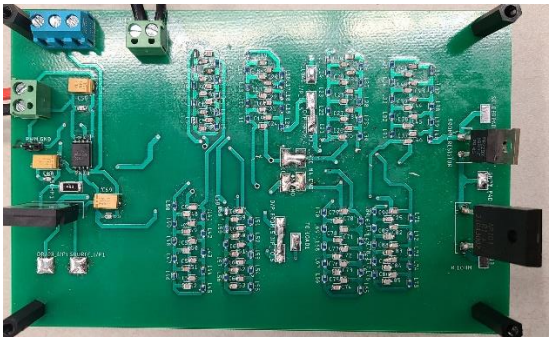


Figure 8.2.2: Lumped-element-based 8-segment FWG prototype

8.2.4 Technical Results

(E) The SiC-MOSFET-powered pulse-width chirp-capable FWG with coaxial transmission lines has been retested for repeatability. The design implements a 1.7-kV Cree/Wolfspeed SiC-MOSFET (C2M1000170D) rated for 10.5-ns rise-time driven using a Texas Instruments UCC5390 driver. 2-, 4-, and 8-segment transmission line versions of the FWG, each with balanced and unbalanced load configurations, have been tested. For the transmission line segments, 4 pairs of coaxial cables with 0.66 velocity factor were used, each pair with lengths 5-, 4-, 3- and 1-meters inducing propagation delays of 25-ns, 20-ns, 15-ns, and 5-ns, respectively. The testing was performed upto 150 V charge voltage and 100 kHz repetition rates with 30% gate trigger duty cycle. The results for each iteration have been tabulated below.

With an increase in number of transmission line segments, an increase in pulse overlap, and pulse deformation due to deconstructive interference was noticed. Test results for 2-, 4- and 8-segment configurations are reported in the table below.

Table 8.2.1: Coax-based FWG prototype test results for 2-, 4-, and 8-segment configurations with balanced (BL) and unbalanced (UBL) loads.

Segments	Load	Charge voltage (V)	Output voltage (V)	Output pulse	Pulse deformation	Comments
2	50Ω & 0.1Ω (UBL)	100	~98.5	Conventional bipolar	No	No noticeable loss and constructive interference noticed due to matched transmission line lengths.
4	50Ω & 0.1Ω (UBL)	100	93	Clumped bipolar	No	Pulse overlap noticed due to difference in transmission line lengths. Second pulse moves in before the first one discharges completely.
4	50Ω & open (UBL)	100	47	Unipolar	Partial	Partially deconstructive interference. Significant pulse overlap noticed.
4	50Ω & 50Ω (BL)	100	90	Conventional Bipolar	No	90% power transfer noticed. Maybe better impedance matching between traces and coax could result in better
8	50Ω & 0.1Ω (UBL)	100	~66	Clumped bipolar	Yes	Pulse overlap noticed. *Non-simultaneous switching suspected.*
8	50Ω & open (UBL)	100	~40.7	Unipolar	Partial	Non-simultaneous switching.

8	50Ω & 50Ω (BL)	100	~53.028	Conventional bipolar	No	Significant ringing noticed after the expected pulse output. *Better impedance matching between trace and connecting cable needed.*
8	100Ω & 100Ω (BL)	100	~70.634	Conventional bipolar	No	Higher pulse output voltage noticed compared with 50Ω load.
8	100Ω & 0.1Ω (UBL)	100	~88.264	Clumped bipolar	Yes	Significant pulse overlap. Suspected non-simultaneous switching by MOSFET. *Need more efficient way to connect switch with transmission lines.*

**UBL – unbalanced, *BL – balanced*

(F) Tunable lumped-element-based (LC) ladder networks were considered a potential alternative to overcome the non-ideal characteristics of coaxial lines in terms of size and weight. This also provides an advantage of integrating the transmission lines into the PCB, minimizing the distance between the switch (MOSFET) and charged lines. The lumped elements were selected such that a 50-Ω characteristic impedance is maintained in each transmission line. An L-C combination of 75-nH and 30-pF was found to induce about 1.5-ns delay while maintaining 50-Ω characteristic impedance. These L-C values were used in the ladder networks to induce ~12-ns and ~21-ns delays. The PCB was designed to be used as either a 4-segment or an 8-segment configuration. Pulse widths of ~12-ns and ~20-ns were seen in the 4-segment FWG implementation with an output voltage ~60% of the charge voltage (V_{chg}). The voltage attenuation was considered to be due to the charging and discharging losses within the LC networks. However, when the 8-segment configuration was tested, a difference in pulse distribution over time was not observed. Rather, an increase in output pulse amplitude was noticed (~76% of V_{chg}). It is assumed that the parasitics induced by the additional traces included in the PCB design to make it modular were affecting charge/discharge of the transmission lines 5 to 8. This issue will be evaluated and addressed in the next report cycle.

8.2.5 Summary of Significant Findings and Mission Impact

(A) The state-of-the-art COTS laser driver specifications and limitations have been comprehensively studied, and target performance metrics have been determined in terms of output current (>120-A), pulse repetition rate (>1-MHz), transient response (<200-ps risetime and <1-ns pulse width), and volume (<0.75 cu-ft). A preliminary feasibility study has signified the need for lock-on conduction mode with ~$10^{2.6}$ gain factor to drive at >1-MHz pulse repetition rate while limiting the amplification stages to 2. This reduces monetary costs to 10–12% of the conventional laser system, while achieving the expected goal of miniaturizing the optical subsystem by 90%.

(B) Pulse trigger requirements for the LDA/LDS have been identified based on Jenoptik's actively cooled quasi continuous wave vertical diode laser stacks to tailor the device parameters of the enabling switch accordingly.

(C) Silicon optodiodes have been evaluated against the identified performance metrics for the enabling switch. The testing was performed at 200 V charge voltage with laser illumination energies between 20-µJ and 200-µJ. The device performance at low optical energies (~20-µJ) did not satisfy the expected metrics in terms of R_{on} and t_{rise}. Alternative switch technologies like avalanche transistors and silicon avalanche shapers will be evaluated in the next report cycle.

(D) Numerical calculations have been completed to estimate the electric fields and corresponding voltage bias required to induce lock-on operation while exploring ways to minimize the potential risks of high jitter at ~MHz order PRR switching, power reflections due to impedance mismatch, and negative ringing currents during PCSS recovery. Expected on-state resistance and power dissipation for 50 µm and 100 µm devices in lock-on conduction mode have been calculated to estimate cooling system requirements while retaining the expected SWaP-C^2 factor.

(E) A MOSFET-switched FWG prototype implementing coaxial transmission lines has been fabricated and tested with a goal to demonstrate a tunable pulse generator capable of demonstrating chirped pulse-widths. The primary operation of a FWG has been demonstrated with upto 8 transmission line segments under balanced and unbalanced load configurations. The experimental implementation results on pulse chirp were found to be in agreement with the simulation results. However, pulse overlap, and deconstructive interference were observed in the 8-segment configuration, which will be addressed using a different transmission line topology/configuration.

(F) LC ladder networks were implemented as lumped-element-based delay lines instead of the coaxial cables. Multiples of 75-nH and 30-pF were used in the LC ladder networks to induce 12-ns and 21-ns delays. A 150-V 4-segment tunable FWG has been demonstrated on a 3″ × 5″ PCB under balanced and unbalanced load conditions. Transmission line charging/discharging issues with 8-segment FWG prototype will be addressed in the next report cycle.

9.0 Thermal Management

9.1 Ultra-Compact Integrated Cooling System Development

(Justin Clark, Roy Allen, and Sarvenaz Sobhansarbandi)

9.1.1 Problem Statement, Approach, and Context

Primary Problem: A cooling unit is required for the thermal management of semiconductor-based pulsed-power devices, with the goal of maintaining the semiconductor device temperature below 80 °C. The goal is to create an ultra-compact cooling unit with the ability to rapidly remove 1 kW/cm^2 of heat.

Solution Space: To achieve such high heat flux, a turbulent flow profile must be achieved. The approach we are going to take is to create an ultra-compact unit integrated onto a semiconductor device, allowing more heat extraction to occur. The pumping power will be kept to a minimum since the unit to be prototyped will represent 1 cm^2 surface area. This enables less power to be consumed to create a turbulent flow. An array of micro-sized jet nozzles will provide a turbulent flow onto a microchannel section directly on the semiconductor device. The ultra-compact design will reach turbulency at a faster rate while requiring less energy consumption.

Sub-Problem: The turbulency formed from the array of nozzles creates an extreme pressure loss. With a large amount of jet nozzles (over 200) and a flow diameter of nearly 100 microns, the pressure across the system will decrease tremendously. The pressure must be sustained to enable proper cooling and circulation processes. Another way to sustain pressure is to use different liquids. Different types of coolant will be simulated to determine effects from fluid density and viscosity. Preliminary studies show that pressure loss can be maintained using DI water or a type of gas while still requiring a small amount of pumping power.

State-of-the-Art (SOTA): Integrated chip cooling, used to dramatically increase the operational power of high voltage silicon-based power devices is reached by increasing the power device heat-removal via an integrated active cooling microelectromechanical system (MEMS) within the power chip device.

Deficiency in the SOTA: The manufacturing techniques of the semiconductor chips have not yet been used for integrated chip cooling systems. These designs are limited due to low tolerance of the manufacturing process. With a proper design implemented, the pressure drop, and heat dissipation rate are large contributors to a properly functioning system.

Solution Proposed: A compact cooling unit is proposed by refining in-chip jet-impingement geometry through leveraging theory and a parametric evaluation of nozzle geometry and flow channel arrangements. With the on-chip theory proposed and manufacturing constraints implemented, a 1 cm^2 surface area, Si-base unit will be prototyped to maneuver high heat dissipation.

Relevance to OSPRES Grant Objective: Increase cooling densities for high pressure microwave (HPM) systems, while decreasing pumping power requirements, in-line with the SWaP-C^2 objective.

9.1.2 Tasks and Milestones / Timeline / Status

(A) Use manufacturing tolerances to design a Si base 1 cm^2 unit to achieve high heat dissipation. The design must be able to be produced by manufacturing techniques such as etching and lithographic layering processes / MAY21–AUG21 / Completed

(B) Using the optimal design, perform ANSYS simulations using either water or Si-C nanofluid. Other fluid types may be researched as pressure drop is a large factor / JUL21–SEP21/ In Progress

9.1.3 Progress Made Since Last Report

(A) Simulation results are in place to confirm geometry sizing and overall design of the device to be capable of highest heat extraction.

(B) The optimal design began simulation process in Ansys Design Modeler to produce a fluid domain. Following this step, a general mesh with adaptive sizing was applied to the part. Meshing errors occurred due to the wide range of element sizing. The varied dimensions from the 3 mm base to the 0.035 mm nozzles caused many elements with orthogonal quality < 0.1, causing a bad mesh and poor simulation results.

9.1.4 Technical Results

(A) Applying a constant temperature of 300 K at the heat source proved the microchannel fins dissipated heat better than impingement on a flat surface. The microchannel fin design increases the fluid-to-solid contact enabling higher heat extraction.

(B) Individually face sizing the elements of each nozzle and microchannel achieved a minimum quality of 0.172 with 1.5 million nodes. Previous literature has shown up to 8 million nodes for a slightly larger system with larger nozzle diameters. The simulation is on-going, and results will be achieved in the upcoming reports.

9.1.5 Summary of Significant Findings and Mission Impact

(A) A water-cooled, cross-flow microchannel cooling system with various microchannel widths achieved a heat flux of 1.7 kW/cm^2 using 0.056 W of pumping power. Although this particular design is not the best fit under manufacturing constraints, the theory of using channels is remarkable and further analyzed. A similar design implemented the idea of having jets confined in their own individual spaces, reaching up to 900 W/ cm^2 with 0.83 W of pumping power. Two types of heat sinks with flat and oblique angled fins were experimentally tested with a constant heat flux of 100 W/cm^2. The temperature difference was from 60 °C to 35 °C which proposed giving the design more power. The oblique angled fins caused 20 percent greater heat transfer than flat fins.

(B) To achieve a higher quality mesh, the nozzle element size was initially set to 20 microns, or until the shape of the nozzles were more profound in a cylindrical shape. The surface which connects to the nozzles resulted with an element size of 15 microns. This value had to be near the nozzle element size to maintain mesh quality. Each surface with poor quality was selected and set to individual face sizing.

10.0 UAS Engagement Wargaming & Modeling and Simulation (M&S)

10.1 Fixed-Effector Wargaming Simulation Toolkit Development

(Nolan Petersen and Travis Fields)

10.1.1 Problem Statement, Approach, and Context

Primary Problem: Wargaming simulations enable rapid evaluation of different weapon systems and strategies. However, the lack of easy to use, high-fidelity software tools makes producing and studying different engagement scenarios (i.e., one friendly system versus five hostile agents) difficult and time-consuming.

Solution Space: We propose developing a simulation environment using the Unity real-time development platform to offer an easy-to-use, medium-fidelity environment for the purpose of studying different blue vs. red engagement scenarios. Unity is a well-established game development software, with a strong community base for tutorials, training, and software assistance. This makes Unity an ideal solution for a medium-fidelity simulation environment to narrow down optimal fixed effector configurations, which could then be studied further in a higher fidelity environment.

State-of-the-Art (SOTA): Current software tools for this purpose are tedious to adapt and/or modify for running different scenarios due to a lack of support as well as documentation.

Relevance to OSPRES Grant Objective: The ability to simulate and benchmark performance of different scenarios, such as different fixed-effector positions, types, and targeting strategies to provide insight into the ideal utilization of HPM-related systems.

Risks, Payoffs, and Challenges:

Risk: There is an infinite number of scenarios and configurations, making generalizations difficult from within a simulation environment.

Challenges: Capturing sufficient realism without significantly reducing performance.

Payoff: The simulation tool could provide tremendous insight and actionable information for both source development and laydown/asset allocation.

10.1.2 Tasks and Milestones / Timeline / Status

(A) Reproduction of previous results obtained from the previously used wargame software Modern Air Power by John Tiller Software, which is no longer in development, using the Unity environment / MAY21 – JUN21 / Completed.

(B) Implementation of radar uncertainty into simulation environment, enabling increased realism to better simulate current targeting capabilities / JUN21 – JUL21 / Completed.

(C) Trade-space study of microwave, tracking, and hostile agent performance to identify key limitations and low-risk, low-cost improvements, enabling increased weapon efficacy / JUL21 – SEP21 / In Progress.

(D) Optimization of current simulation framework to facilitate more quickly obtaining results / SEP21 – OCT21 / In Progress

(E) Implementation of Electro-Optical/Infra-Red and lidar sensor capabilities into simulation environment, enabling increased realism to better simulate current targeting capabilities / OCT 21 – NOV 21 / Upcoming.

10.1.3 Progress Made Since Last Report

(C) A trade-space study was performed that considered the effect of slew-rate and radar uncertainty on the average number of UAVs neutralized.

(D) Optimization has begun with the development of a custom UMKC M&S C# library to facilitate running simulations at much greater speeds.

10.1.4 Technical Results

(C) A trade-space study was conducted where the average number of UAVs neutralized was measured against a variable slew-rate both with and without radar uncertainty. For this study, due to a lack of sources on elevation uncertainty, we considered a radar uncertainty (denoted as δ) of 0.6° in only the azimuth angle (angular position in the plane parallel to the ground) of each UAV. 100 UAV attackers began evenly spaced on a 700 m radius circle with a speed of 10.3 m/s and flew in a straight-line path towards a fixed-position HPM defender at the center of the circle. The HPM defender had a firing delay of 1 s, a probability of effect of 0.8 at 600 m, and did not affect any UAVs off-boresight. The objective of the HPM defender was to keep the UAV attackers from penetrating a 100 m exclusion radius centered at the HPM defender. The range of slew-rates that were tested was normalized using a normalization factor of x_0. Our results for the described scenarios are shown below in Figure 10.1.1.

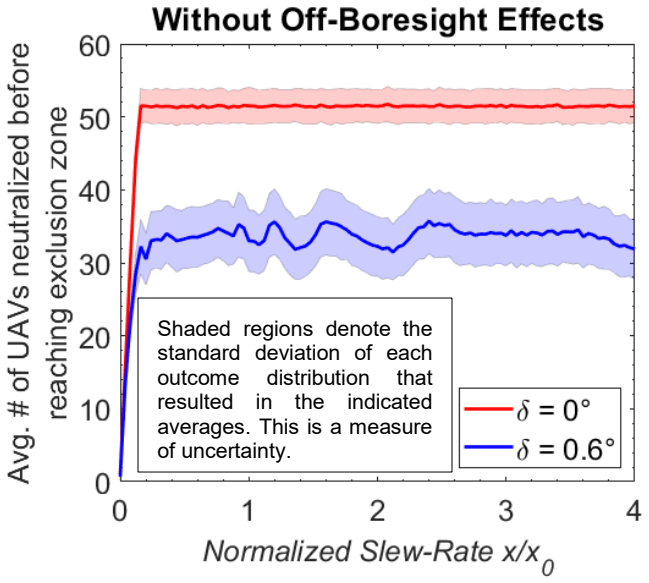


Figure 10.1.2. UAVs neutralized vs normalized slew-rate. δ = azimuth uncertainty

Next, we performed the same slew-rate tests WITH off-boresight effects. To do this, we modeled off-boresight effects with a correction factor that is a function of the angle between the HPM effector boresight to the UAV position. We then multiply this correction factor by the probability of effect at the given range. This correction factor was informed by the UMKC effects testing team. Our results for the same scenarios with off-boresight effects are given below in Figure 10.1.2.

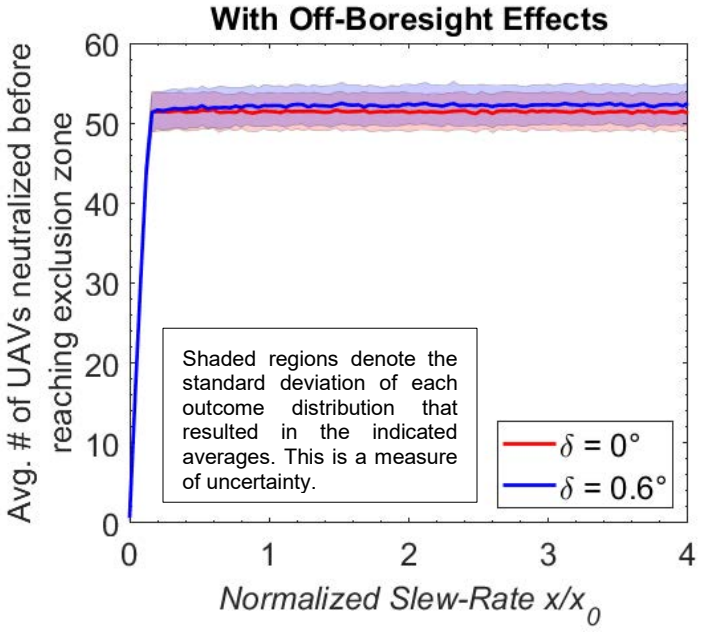


Figure 10.1.2. UAVs neutralized vs normalized slew-rate with off-boresight effects. δ = azimuth uncertainty.

From Figure 10.1.1., we found that without off-boresight effects, even small uncertainties in the azimuth angle (δ = 0.6) significantly lowered the average. Additionally, in Figure 10.1.1. and Figure 10.1.2., we can see that the average number of UAVs neutralized plateaus very quickly over the range of slew-rates tested. This is because after a certain threshold slew-rate, the 1 s firing delay acts as a bottleneck, making it impossible to kill any more UAVs. However, in Figure 10.1.2., with off-boresight effects, the average number of UAVs neutralized for an azimuth angle uncertainty of 0.6° is ~1 more than the average for no azimuth angle uncertainty. This is because, in this scenario, a higher degree of radar uncertainty gives the HPM defender a higher chance of pointing the boresight between two UAVs rather than directly at one, giving it a higher probability to neutralize 2 UAVs in one shot.

(D) The previous slew-rate study utilized the Monte Carlo method, where the simulation is run many times over until our average approaches the true value and stops significantly changing. This takes longer and longer to do with more complex simulations. Unity only supports speeding up your simulation by a maximum of 100x. Because of this, our simulations using the Monte Carlo method have taken much longer than necessary. To fix this, we have begun development of a custom library for C#, the language in which Unity is written, that will allow us to run the same scripts we use for Unity in a console

window. This lets the simulation run as fast as it possibly can and removes the graphical overhead of Unity when not needed.

10.1.5 Summary of Significant Finding and Mission Impact

(A) Reproduction of previous results obtained from Modern Air Power by John Tiller Software was completed in Unity, which provided a framework to implement new features.

(B) Implementation of radar uncertainty into the Unity simulation environment was completed.

(C) A trade-space study of the effect of slew-rate on HPM effectors with and without radar uncertainty and off-boresight effects was performed. This study showed that beyond a threshold slew-rate, additional kills are not possible without decreasing firing delay. It also showed that the performance of energy weapons without off-boresight effects is susceptible to the effects of radar uncertainty, while energy weapons with off-boresight effects may mitigate the effects of radar uncertainty on performance.

(D) Optimization of the simulation through development of a custom C# library was started.

10.2 Airborne Effector Weapons Target Assignment

(Cody Smith and Travis Fields)

10.2.1 Problem Statement, Approach, and Context

Primary Problem: Unmanned aircraft technological development trends suggest the potential for the application of both coordinated and cooperative hostile sUAS attacks in the near future. Defense strategies are currently under development which primarily utilize aerial- or ground-based defense systems or a layered combination of the two. An engagement with multiple blue (friendly) vehicles against many red (hostile) vehicles presents an important yet difficult question in assigning which blue engages which red(s) as the computational burden grows rapidly with increases in scenario complexity.

Solution Space: We propose using various heuristics like the Genetic Algorithm (GA) to solve the Multiple Weapons to Multiple Targets Assignment Problem (MWMTAP) (a generalization of the Multiple Traveling Salesman Problem with Moving Targets (MTSPMT) and an extension of the Weapon Target Assignment (WTA) Problem) in order to produce computationally efficient task assignment allocations to the blue forces.

State-of-the-Art (SOTA): Many current techniques consider stationary targets and/or holonomic vehicles, which within the proposed scenario are not applicable. The target assignment problem with constrained (or realistic flight-like) motion and many potential targets that must be intercepted with several friendly assets is a unique (at least in the literature) problem.

Relevance to OSPRES Grant Objective: The concepts for WTA are applicable to both fixed and airborne weapon systems. Developing the strategies for assigning assets is critically important for considering layered defense scenarios, as the battlefield is now heterogeneous with a diverse array of capabilities, performance, and cost.

Risks, Payoffs, and Challenges:

Risk: The computational complexity of the task assignment problem is still too great for onboard UAS microcomputers even after the application of heuristic solutions.

Challenges: Creating an efficient, robust, and effective task assignment framework that not only can be used on typical workstations, but can be utilized on low power onboard UAS microcomputers.

Payoff: A robust task assignment framework is the first step in creating an automated decision engine that could be used for any DEW weapon system.

10.2.2 Tasks and Milestones / Timeline / Status

(A) Literature review on task-assignment-related studies/research activities / MAR21–MAY21 / Completed.

(B) Implementation and evaluation of engagement-level WTA (one vs. few) in simulated environment / MAY21–JUN21 / Completed.

(C) Implementation and evaluation of mission-level WTA (few vs. many) in simulated environment / JUN21–JUL21 / Completed.

(D) Dissemination of the performance of various metaheuristics such as the GA for realistic mission and engagement-level scenarios / AUG21–SEP21 / In Progress.

10.2.3 Progress Made Since Last Report

(D) A comparative analysis on various encoding, crossover, and mutation techniques for the GA was performed. A decision was made to utilize a GA technique called Multi-Chromosome encoding to reduce the potential solution space, and at this time, all efforts are directed toward programmatically implementing the GA to solve for the MWMTAP.

10.2.4 Technical Results

Currently, an analysis tool has been developed using brute force that is capable of outputting the optimal path, path length, and time of completion for one or multiple friendly systems to intercept a small number of incoming hostile threats ($n < 9$). We developed this software to be used as a tool for comparative analysis with heuristic approaches like the genetic and auction algorithms. Customizable parameters include blue starting position, red starting positions, red starting speeds, minimum protection radius, and number of reds. Additionally, various aspects such as patrol and detection radius will be evaluated. The beginning stages of the construction and implementation of the genetic algorithm has commenced. Various GA chromosomal encoding schemes, including the Single Chromosome, Double Chromosome, and Multiple Chromosome, were evaluated based on their computational efficiency and ease of implementation. Though the Multiple

Chromosome technique is significantly more difficult to implement programmatically, the reduction in solution space by eliminating redundancies makes it the ideal encoding scheme for onboard UAS microcomputers and thus the chosen encoding scheme for this work. Additionally, a number of complex crossover and mutation operators such as gene sequence inversion and gene sequence transposition were written for both in-route and cross-route operations. Quantitative efficiency results will be included upon final construction of the GA.

10.2.5 Summary of Significant Findings and Mission Impact

(A) A review of the task assignment literature was completed and two key strategies were identified: genetic algorithm and auction algorithm.

(B) A programmatic solution using the brute force algorithm to solve for the engagement-level WTA was constructed. This tool is capable of finding optimal solutions in one vs. few scenarios.

(C) A programmatic solution using the brute force algorithm to solve for the mission-level WTA was constructed. This tool is capable of finding optimal solutions in few vs. few scenarios and will be used to compare output solutions from the previously described heuristic approaches.

11.0 Software-Defined Medium-Power Microwave Pulse Generator

11.1 Development of a GaN-Based Power Amplifier RF Source

(Abu Hanif)

11.1.1 Problem Statement, Approach, and Context

Primary Problem: To achieve the SWAP-C2 performance metrics necessary to support the cUAV Naval afloat mission, Gallium Nitride-based high electron mobility transistors (GaN HEMT) require multiple amplification stages in series to transition a low voltage/power signal (1-V, 1-GHz), to the high-power levels. Even the best high-power GaN HEMTs are limited to 2-3kW of peak power. Achieving the necessary effective radiated power (ERP) out of a high gain (≥ 10-dBi) narrow-band antenna requires input powers increase of two to three orders of magnitude and thus multiple parallel branches of HEMTs and/or power combining and pulse compression to achieve ERP at the MWs scale.

Solution Space: Pulse compression and power combination techniques are utilized to increase the peak power and lessen the pulse width in high power microwave (HPM) applications. Adapting multiple pre-amplification stages to increase the power levels to the appropriate inputs required by GaN HEMTs in a reconfigurable fashion facilitates leveraging commercially available off the shelf (COTS) devices and combiners to be pulse compressed and thus achieve sufficient ERP with an optimal radiating element.

***Sub-Problem 1*:** The analytical relationship between pulse compression ratio (PCR) and peak output power (P_{out_peak}) and the compression limit are not yet clearly understood. Thus, leveraging the findings from this study will enable us to develop the RF source with minimum number of compression and combination stages with maximum PCR that will meet the required ERP.

Sub-Problem 2: SPICE models for sate of the art (SOTA) high power GaN HEMT power amplifiers (PAs) which can produce higher than 1-kW peak power, are needed to be developed as they are not available yet. The developed model will create a platform to simulate them in conjunction with pulse compression stages which will eventually help in developing the RF source meeting the SWAP-C2 requirements.

Sub-Problem 3: A custom built prime power unit with adjustable output power needs to be developed to supply the necessary voltage and current for the PA unit. For example, MACOM MAPC-A1500 requires 65V, 1.3A prime power unit for an efficient operation whereas INTEGRA IGN1011S3600 requires 100V 150mA unit. Therefore, the design needs to be dynamic since the required power will vary depending on the number of series and parallel stages of the GaN HEMTs PAs as well as the module to be used since different manufacturer require different power levels for their respective PA module.

State-of-the-Art (SOTA): Large modular RF pulse generators (>1-m^3, >1000-lbs) which are comprised of at least 8 parallel-combiners, have demonstrated peak output power up to a few GWs. All these prototypes are stationery and rack mounted. Smaller versions (~0.125-m^3, 50-lbs to 100-lbs) can achieve 50kV peak voltage with PCR of 667 at 70ns FWHM terminated at 307Ω load [1]. Another power amplifier manufactured by Amplifier

Research has an output of only 800W peak power which weighs 70lbs [2]. However, none of them are suitable for Navy afloat missions due to weight to peak output power ratio.

Deficiency in the SOTA: Large RF pulse generators are traditionally limited by mechanical design constraints and power supply limitations. They are large (few meters long), leverage huge transformers, and require liquid coolant such as transformer oil for cooling purposes, which lead to undesirable system mass values even more than 1000-lbs. In addition, a comprehensive analytical study on pulse compression and peak output power is missing in SOTA; specifically, as it pertains to GaN-based RF sources.

Solution Proposed: Developing a highly efficient and cost effective GaN-based power amplifier RF source capable of achieving 1-5 W/cm^2 at 10-50m away with the minimum number of series connected modules (i.e., M×N) with maximum volumetric power density. Therefore, methodically the optimum peak output power and maximum pulse compression ratio through topological GaN based power amplifier design including the power combination including reconfigurable antenna design and the necessary components therein that maximize power/voltage gain and efficiency achieved by the RF source as well as the output parameters such as peak power, pulse width, etc., are adjustable in real time at will to meet the mission needs.

Relevance to OSPRES Grant Objective: Reconfigurable RF source with adjustable RF parameters (e.g., output power, pulse width, bandwidth, frequency) will enable the system to exercise dynamic MPM missions (i.e., multi mission) with optimal SWaP-C2 parameters.

Risks, Payoffs, and Challenges:

Risks: Existing GaN based high output peak power yielding amplifiers such as MAPC-A1500 (peak power of 2600W) and IGN1011S3600 (peak power of 3600W) are out of stock. Lower-power versions produced by the same manufacturer that have been quoted have long lead times (26-weeks ARO) and require minimum of 50 to order making them thousands of dollars to purchase. Alternatively, building the amplifier module from scratch will take its toll in time as well as the performance of the built prototype might be poor in terms of efficiency and form factor.

Payoffs: Building the amplifier module from scratch will payoff in terms of utilizing the lead time to find the most suitable pulse compression method that can achieve 2-3 orders of peak power and compression gain which will eventually meet the mission needs and therefore, the appropriate compression method can be immediately deployed with the COTS GaN amplifiers once they are received.

Challenges: High power PAs and pulse compression methods are usually lossy in nature and generate considerable amount of heat, therefore, designing a proper cooling method must be carried out which may inadvertently increase the volume (size and weight) of the overall design.

11.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Achieve 2-3 orders of peak power and compression gain using magnetic pulse compression (MPC) [*estimated completion by DEC21*].

1. Task – Simulate MPC circuit in LTSpice to find out the electrical parameters for the MPC unit design [*AUG–SEP21*].
2. Task – Design pulse transformer (PT) and magnetic switch (MS) required for the MPC unit [*SEP21–OCT21*].
3. Task –Build and test the MPC prototype using bench top power supply [OCT*21–DEC21*].

(B) Milestone – Achieving comparable peak power level given in datasheet using MACOM MAPC-A1500 based evaluation board [*on hold until the evaluation board is received-lead time is about 26 weeks*].

(C) Milestone – Obtaining 2-3 orders of peak power and compression gain using MAPC-A1500 GaN HEMT PA and MPC prototype built in milestone A [on hold until milestone B is complete]

11.1.3 Progress Made Since Last Report

(A.1) Since this is the first report, this section will be updated in the next month.

11.1.4 Technical Results

(A) Pulse compression is a technique which shrinks the width of the pulse and increases the peak power. It can be better realized from Fig. 11.1.4.1 [3].

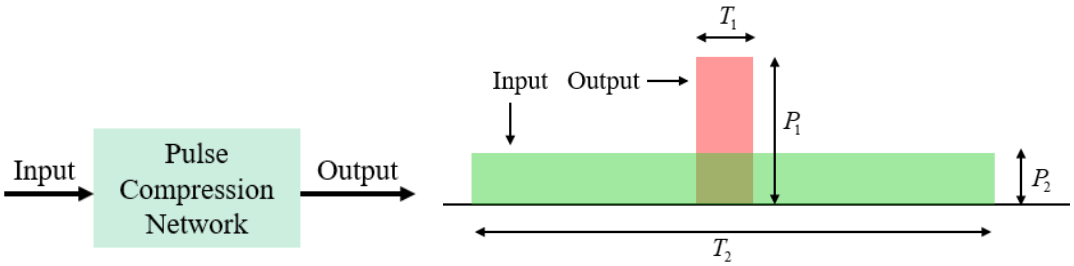


Fig. 11.1.4.1: Peak Power vs Pulse Width [3]

Assuming the pulse compression network (PCN) is lossless, the energy content of an output pulse would be equal to the energy content of the input pulse which is expressed in equation (1) [8].

$$T_1 P_1 = T_2 P_2 \qquad (1)$$

From equation (1), when the pulse is compressed into a width of T_1 from T_2, the peak power should increase to P_1 from P_2 to maintain energy conservation. However, for any real system, there are losses in the medium; the equation (1) relationship is non-linear and depends on the method of pulse compression used.

(B) The analysis articulated below articulates the importance of pulse and power combination. Consider that we need to generate a power level of 1-W/cm^2 at 10-m from the antenna. Now, we will calculate the number of PAs required from numerous manufacturers to meet the specified power density without any compression stages. Equation (4) was utilized to calculate the data summarized in Table II.

$$P_t = \frac{4\pi r^2 P_D}{G_t} \qquad (4)$$

Where, P_t = Transmitted power, G_t = Antenna gain, and P_D = power density at distance r meters. Fig. 11.1.4.2 illustrates transmitted power (P_t) and power density (P_D)at distance r.

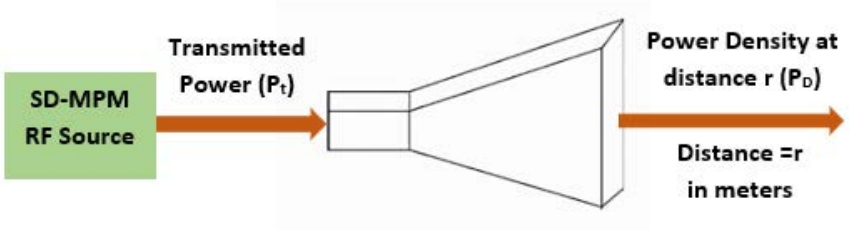


Fig. 11.1.4.2: Illustration of transmitted power and power density at a distance r

Table 11.1.4.1 Comparison between the Number and Power Rating of Different GaN PAs from Various Manufacturers

G_t(dBi)	G_t(linear)	P_t (MW)	No. of MACOM (MAPC-A1500-2600W)	No. of Wolfspeed (GTVA101K42EV-1400W)	No. of Qorvo (QPD1025L-1800W)	No. of Integra (IGN0450M-1500W)
10	10.00	1.257	484	898	699	838
15	31.62	0.397	153	284	221	265
20	100.00	0.126	49	90	70	84
25	316.23	0.040	16	29	23	27

From Table 11.1.4.1, it can be easily realized that without compression we will require 484 GaN PAs from MACOM to achieve 1-W/cm^2 power density at 10-m with a typical antenna gain of 10dBi. If other PAs are considered, the required number is even higher. However, if we design the antenna for a higher gain the number can be significantly reduced. Unfortunately, designing an antenna at a much higher gain (>25) will require a greater volume, which will eventually become a drawback in meeting the form factor. Yet, a gain factor of 20 dBi is achievable without compromising the size of the antenna. This will bring down the number of required PAs by ten times. In addition, if pulse compression is applied, the peak output power of each PA module will increase, as a result, the total number of PA required to achieve the required power density will go down even further. Fig. 11.1.4.3 has been plotted to illustrate the relationship between the number of GaN amplifier and required transmitted power vs the antenna gain for the MACOM and Qorvo amplifiers.

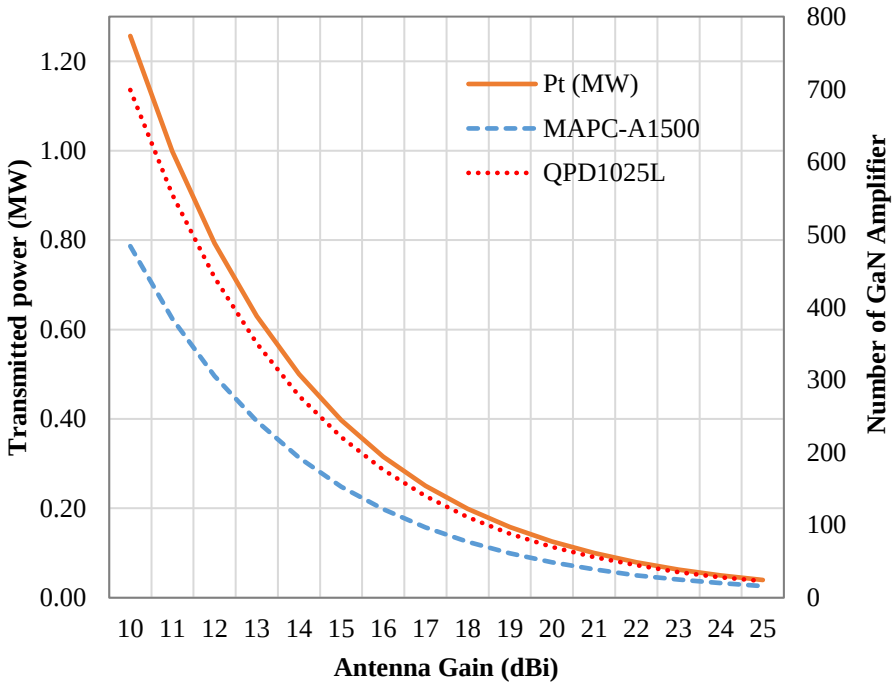
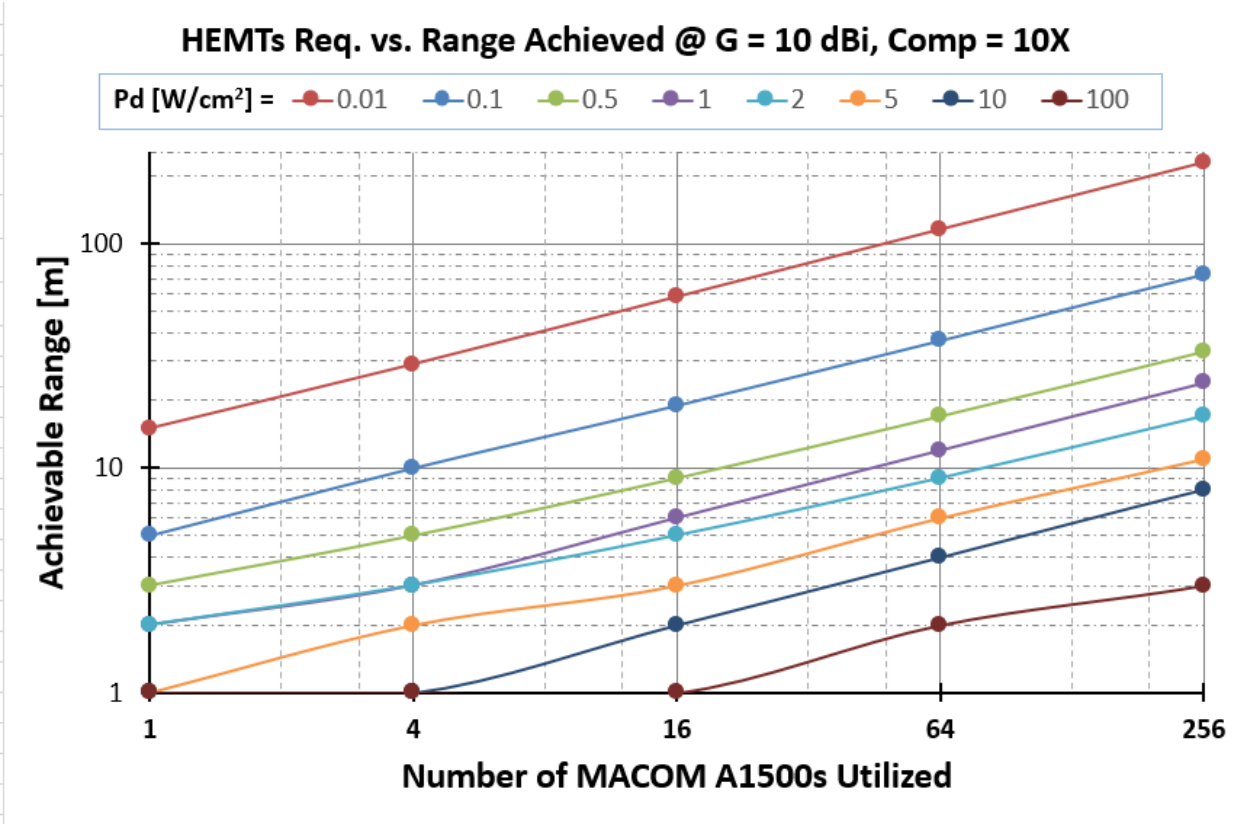
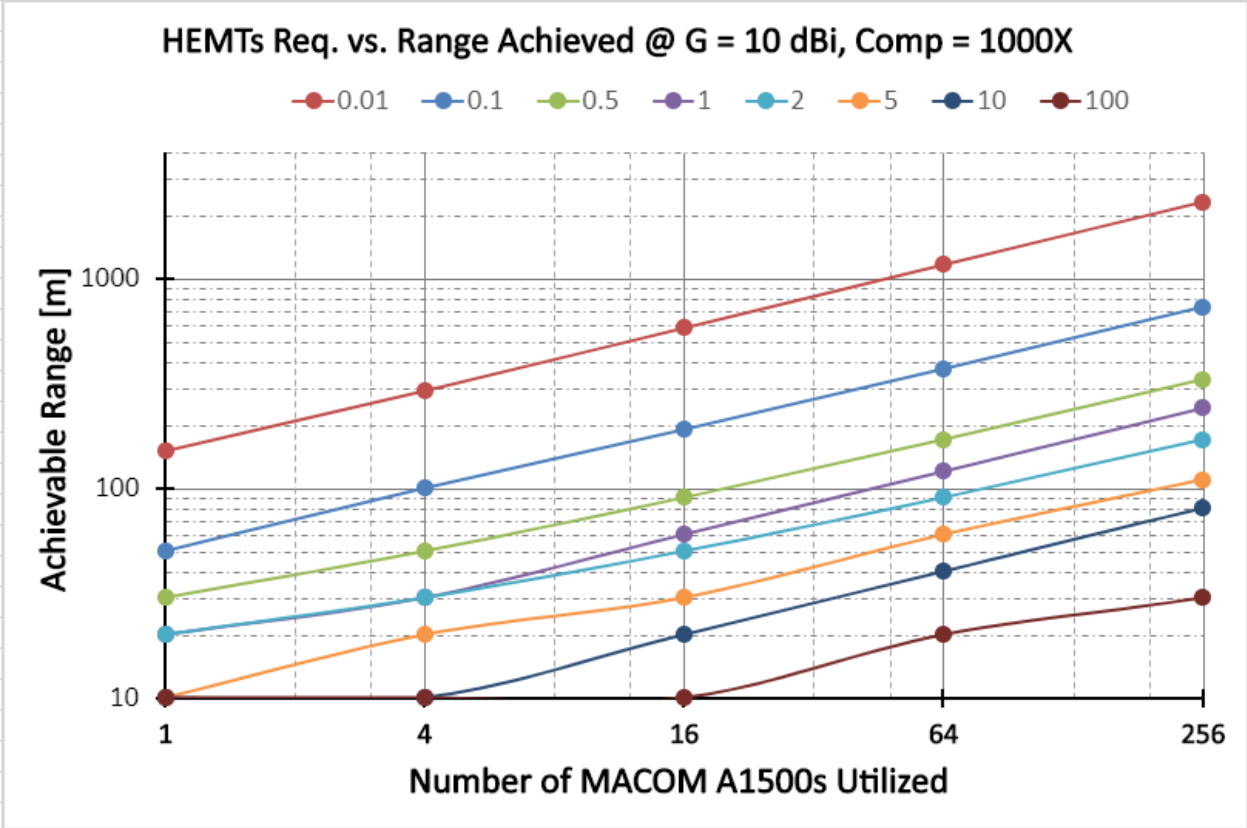


Fig. 11.1.4.3: Power & No. of GaN PA required vs Gain @ P_D = 1 W/cm^2 @ 10m


HEMTs Req. vs. Range Achieved @ G = 10 dBi, Comp = 10X
Pd [W/cm²] =
0.01
0.1
0.5
1
2
5
10
100
Achievable Range [m]
100
10
1
1
4
16
64
256
Number of MACOM A1500s Utilized


HEMTs Req. vs. Range Achieved @ G = 10 dBi, Comp = 1000X
0.01
0.1
0.5
1
2
5
10
100
Achievable Range [m]
1000
100
10
1
4
16
64
256
Number of MACOM A1500s Utilized

Therefore, pulse compression is indispensable in developing the MPM RF source as well as power combination will be required since the design will require multiple power amplifiers to be used to meet the necessary power transmission. The number of PAs required can further be lowered (<10) by using pulse transformers (PT) and including multiple MPC stages (<5) which is one of the possible solutions and other compression methods will be explored as well. In addition, if the antenna is designed such that the gain can be adjusted over a range (e.g., 15-25dBi), it would be an added advantage in further reducing the number of PAs required in the design.

11.1.5 Summary of Significant Findings and Mission Impact

(A-B) Pulse compression and power combination is inevitable in achieving the goal of the mission. However, the most appropriate method for compression is yet to be identified. To achieve the mission goals, several pulse compression methods with be studied and experimental results will be compared to identify the most viable method. For now, task 1 under milestone A needs to be carried out with highest importance to accomplish the objectives in a timely manner.

11.1.6 References

[1] D. Zhang, Y. Zhou, J. Wang and P. Yan, "A compact, high repetition-rate, nanosecond pulse generator based on magnetic pulse compression system," in IEEE Transactions on Dielectrics and Electrical Insulation, vol. 18, no. 4, pp. 1151-1157, August 2011, doi: 10.1109/TDEI.2011.5976109.

[2] https://www.arww-modularrf.com/rack-mount-amplifiers.cfm

[3] https://www.ieee802.org/15/pub/05/

12.0 Program Management

12.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

12.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

12.3 Major Procurement Actions

12.4 Travel

Destination	Purpose	Attendees	Estimated Costs

12.5 Pending or Upcoming Public Release Requests

13.0 Appendix A: Academic and IP Output

13.1 Students Graduated

Name	Degree	Currently
Al-Shaikhli, Waleed	MS Spring 19	Kansas City National Security Campus, Honeywell
Azad, Wasekul	PhD Summer 21	UMKC/MIDE (Postdoc)
Berg, Jordan	MS Spring 21	
Bissen, Bear	MS Spring 19	UMKC/MIDE (Staff)
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Hanif, Abu	PhD Spring 21	
Harmon, Aaron	BS	Missouri University of Science & Technology
Harp, Joshua	MS	UMKC/MIDE (Senior Engineer)
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Klappa, Paul	MS Spring 21	
Labrada, Dario	BS Spring 20	UMKC/MIDE (MS Student)
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory
Renzelman, Jeff	MS Spring 18	Kansas City National Security Campus, Honeywell
Roy, Sourov	PhD Spring21	UMKC/MIDE (Postdoc)
Wagner, Adam	MS Fall 20	Kansas City National Security Campus, Honeywell
Xia, Shengxuan	BS	Missouri University of Science & Technology

13.2 Journal Publications

13.2.1 In Preparation

[1] N. Gardner, A. N. Caruso, and P. Doynov, “Diode-Based Non-Linear Transmission Line: A Bandwidth and Center Frequency Tuning Study,” *Transactions on Microwave Theory and Technique*, In Preparation, **2021**.

[2] B. Barman, D. Chatterjee, and A. N. Caruso, “Tradespace analysis of wideband coaxial probe-fed microstrip patch electrically small antenna elements,” In preparation, **2021**.

[3] S. Xia, J. Hunter, A. Harmon, M. Hamdalla, A. Hassan, V. Khilkevich, D. Beetner, “Simulation Driven Statistical Analysis of the Electro-magnetic Coupling to Microstriplines,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[4] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, “Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field Coupling to Randomly Shaped Wires,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

13.2.2 Submitted / Under Revision

[5] B. K. Lau, M. Capek, and A. M. Hassan, “Characteristic Modes–Progress, Overview, and Future Perspectives,” *IEEE Antennas and Propagation Magazine*, Submitted, **2021**.

[6] K. Alsultan, M. Z. M. Hamdalla, S. Dey, P. Rao, and A. M. Hassan, “Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform,” *ACES*, Submitted, **2021**.

[7] M. Z. M. Hamdalla, B. Bissen, J. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, “Prediction of Experimental Electromagnetic Coupling to a UAV Model Using Characteristic Mode Analysis,” *IEEE Access*, Submitted, **2021**.

[8] W. Azad, F. Khan, and A. N. Caruso, “A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Featuring Custom Isolated Gate Driver Circuit Combined With Coupling and Snubber Circuits,” *IEEE Transactions on Power Electronics*, Submitted, **2021.**

[9] J. N. Berg, R. C. Allen, and S. Sobhansarbandi. “A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation.” *International Journal of Thermal Sciences*, Submitted, **2021**.

[10] John Keerthi Paul Bhamidipati, Eliot R. Myers, Adam M. Conway, Lars F. Voss, and Anthony N. Caruso, “Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches,” *IEEE Transactions on Electronic Devices*, Under Revision, **2020**.

13.2.3 Published / In Press

[11] W. Azad, F. Khan, and A. N. Caruso, “A Medium Power, Self-Sustaining, Configurable RF Pulse Generation Circuit Using a Nonlinear Transmission Line and Power Amplifier in a Closed Loop Configuration, *IEEE Transactions on Plasma Science*, vol. 49, no. 7, pp. 2183–2194, **July 2021** [doi].

[12] S. Roy, W. Azad, S. Baidya and F. Khan, “A Comprehensive Review on Rectifiers, Linear Regulators and Switched-Mode Power Processing Techniques for Biomedical Sensors and Implants utilizing In-body Energy Harvesting and External Power Delivery,” *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 12721–12745, **Nov. 2021** [doi].

[13] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems,” *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364–373, **2019** [doi].

13.3 Conference Publications

13.3.1 Submitted / Accepted

[1] B. Barman, D. Chatterjee, and A. N. Caruso, “Effect of Ground Plane Shape and Size on the Input Impedance of a Monopole embedded in a Grounded Dielectric Substrate,” submitted to the *2021 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*, Marina Bay Sands, Singapore, December 4-10, 2021.

[2] B. Barman, D. Chatterjee, and A. N. Caruso, “Comparison of Q-Factor Calculation Methods for Wideband Microstrip Patch Antennas,” submitted to the *2021 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*, Marina Bay Sands, Singapore, December 4-10, 2021.

[3] S. R. Shepard and H. A. Thompson, “Self-focusing in Guided and Un-guided Media,” submitted to the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, 2021.

[4] B. Barman, D. Chatterjee, and A. N. Caruso, “Probe-location Optimization in a Wideband Microstrip Patch Antenna using Genetic Algorithm, Particle Swarm and Nelder-Mead Optimization Methods,” accepted in *2021 International Applied Computational Electromagnetics Society (ACES) Symposium*, USA, August 1-5, 2021.

13.3.2 Presented

[5] W. Azad, S. Roy, and F. Khan, "A Single Gate Driver-based Four-stage High-voltage SiC Switch Having Dynamic Voltage Balancing Capability," *2021 IEEE Applied Power Electronics Conference and Exposition* (APEC), Phoenix, AZ, USA, June 9-12, 2021.

[6] W. Azad, S. Roy, F. Khan and A. N. Caruso, "A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuits," *2021 IEEE Kansas Power and Energy Conference* (KPEC), Manhattan, KS, USA, April 19-20, 2021 [doi].

[7] T. Layman, T. D. Fields, and O. A. Yakimenko, “Evaluation of Proportional Navigation for Multirotor Pursuit,” AIAA SciTech Forum, Virtual Event, January 11-21, 2021 [doi].

[8] P. J. Klappa, and T. D. Fields, “Assessment of Fixed-Wing UAV System Identification Models during Actuator and Payload Drop Failures,” AIAA Atmospheric Flight Mechanics Conference, Virtual Event, January 11-21, 2021 [doi].

[9] J. Hunter, S. Xia, A. Harmon, A. M. Hassan, V. Khilkevich, and D. Beetner, “Modeling and Statistical Characterization of Electromagnetic Coupling to Electronic Devices,” *IEEE International Symposium on Antennas and Propagation and NSRM USNC-URSI National Radio Science Meeting*, Boulder, CO, January 4-9, 2021 [doi].

[10] B. Barman, K. C. Durbhakula, B. Bissen, D. Chatterjee, and A. N. Caruso, “Performance Optimization of a Microstrip Patch Antenna using Characteristic Mode and D/Q Analysis,” *2020 XXXIIIrd General Assembly and Scientific Symposium of the International Union of Radio Science*, Rome, Italy (online conference), Aug 29-Sept 5, 2020, pp. 1-4 [doi].

[11] J. Berg, and S. Sobhansarbandi. “CFD Modeling of Thermal Management Systems for a Silicon Semiconductor Switch.” *ASME 2020 Heat Transfer Summer Conference collocated with the ASME 2020 Fluids Engineering Division Summer Meeting and the ASME 2020 18th International Conference on Nanochannels, Microchannels, and Minichannels*, Virtual, July 13–15, 2020, American Society of Mechanical Engineers Digital Collection [doi].

[12] B. Barman, D. Chatterjee, and A. N. Caruso, “Performance Optimization of Electrically Small Microstrip Patch Antennas on Finite Ground Planes,” 2020 *IEEE International Symposium on Antennas and Propagation and North American Radio Science Meeting*, Montreal, Quebec, Canada, July 5-10, 2020, pp. 1–2 (online conference) [doi].

[13] M. Hamdalla, B. Bissen, A. N. Caruso, and A. M. Hassan, “Experimental Validations of Characteristic Mode Analysis Predictions Using GTEM Measurements,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Montréal, Québec, Canada, July 5-10, 2020 [doi].

[14] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, “Scalable Characteristic Mode Analysis: Requirements and Challenges (White Paper),” *Large Scale Networking (LSN) Workshop on Huge Data: A Computing, Networking and Distributed Systems Perspective Sponsored by NSF*, Chicago, IL, April 13-14, 2020.

[15] M. Hamdalla, A. N. Caruso, and A. M. Hassan, “Predicting Electromagnetic Interference to a Terminated Wire Using Characteristic Mode Analysis,” *Proceedings of the Annual Review of Progress in Applied Computational Electromagnetics (ACES)*, Monterey, CA, March 22-26, 2020. [doi]

[16] W. Azad, F. Khan, and A. Caruso, "Self-sustaining High-power RF Signal Generation Using LDMOS Based Power Amplifier and Nonlinear Transmission Line," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 3567-3572 [doi].

[17] A. Hanif, W. Azad, and F. Khan, "Detection of Bond Wire Lift Off in IGBT Power Modules Using Ultrasound Resonators," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 345-350 [doi].

[18] B. Barman, D. Chatterjee, and A. N. Caruso, “Some Investigations into Mutual Coupling Analysis for Trade Space Studies of Linear Arrays,” *2019 IEEE International Symposium on Phased Array Systems and Technology (PAST)*, Waltham, MA, October 2019, pp. 1-8 [doi].

[19] B. Barman, D. Chatterjee, and A. N. Caruso, “Characteristic Mode Analysis of a straight and an L-probe fed Microstrip Patch,” *2019 IEEE Indian Conference on Antennas and Propogation (InCAP)*, Ahmedabad, India, Dec 2019, pp. 1-3 [doi].

[20] M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of the Effect of the UAV Frame Material on Coupling and Interference," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019 [doi].

[21] M. Hamdalla, J. Hunter, Y. Liu, V. Khilkevich, D. Beetner, A. Caruso, and A. M. Hassan, "Electromagnetic Interference of Unmanned Aerial Vehicles: A Characteristic Mode Analysis Approach," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019 [doi].

[22] K. C. Durbhakula, J. Lancaster, A. M. Hassan, D. Chatterjee, A. N. Caruso, J. D. Hunter, Y. Liu, D. Beetner, and V. Khilkevich, "Electromagnetic Coupling Analysis of Printed Circuit Board Traces using Characteristic Mode Analysis," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (2 pages)*, Atlanta, Georgia, USA, July 7-12 2019 [doi].

[23] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “On the Location of Transverse Electric Surface Wave Poles for Electrically Thick Substrates,” Proceedings of the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 [doi].

[24] W. Azad and F. Khan, “Sustaining High-power RF Signal Generation in a Positive Feedback Network," *2019 IEEE Pulsed Power and Plasma Science Conference (PPPS)*, Orlando, FL, USA, June 23-28 2019.

[25] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, “Scalable characteristic mode analysis using big data techniques,” *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[26] M. Hamdalla, W. Al-Shaikhli, J. Lancaster, J. D. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, “Characteristic Mode Analysis of Electromagnetic Coupling to Wires with Realistic Shapes,” *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[27] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “Location of Surface Wave Poles in Sommerfeld Integrals: A Mittag-Leffler Expansion Approach,” *Proceedings of the URSI-B International Symposium on Electromagnetic Theory*, URSI Commission, San Diego, USA, May 2019 [doi].

[28] K. C. Durbhakula, D. Chatterjee and A. M. Hassan, “Analytical Evaluation of Sommerfeld Integral Tails Present in Two-layered Media Green’s Functions,” *Proceedings of the Indian Conference on Antennas and Propagation* (InCAP), Hyderabad, India, December 2018 [doi].

[29] D. Beetner, V. Khilkevich, A. M. Hassan, J. Hunter, Y. Liu, and D. Floyd, *“*Characterization of the Electromagnetic Coupling to UAVs,*”* *DE Systems Symposium*, September 24-27, 2018

[30] C. Hartshorn, K. Durbhakula, D. Welty, D. Chatterjee, J. Lancaster, A. M. Hassan, and A. N. Caruso, “Crosstalk and Coupling to Printed Circuit Board Metallic Traces with Arbitrary Shapes,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[31] M. Hamdalla, J. Roacho-Valles, J. Hunter, D. Beetner, A. M. Hassan, and A. N. Caruso, “Electromagnetic Analysis of Unmanned Aerial Vehicles Using Characteristic Mode Analysis,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[32] C. Hartshorn, M. Hamdalla, J. Lancaster, A. M. Hassan, and A. N. Caruso, “Electromagnetic Vulnerability of Wires with Arbitrary Shape,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[33] K. C. Durbhakula, D. Chatterjee, A. M. Hassan, and M. S. Kluskens, “Studies on Numerical Evaluation of Sommerfeld Integrals for Multilayer Topologies,” *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018.

[34] J. Lancaster, D. Chatterjee, and A. N. Caruso, “Some Investigations into the Dispersion Characteristics of Localized Bessel Beams,” published in the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018 (1 page URSI Abstract).

[35] M. Hamdalla, A. M. Hassan, and A. N. Caruso “Characteristic Mode Analysis of Unmanned Aerial Vehicles with Realistic Shapes and Material Composition,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Boston, MA, July 8-13, 2018.

[36] W. Azad, S. Roy, A. S. Imtiaz, and F. Khan, "Microelectromechanical System (MEMS) Resonator: A New Element in Power Converter Circuits Featuring Reduced EMI," *2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, Niigata, May 20-24, 2018, pp. 2416-2420 [doi].

[37] J. Hunter, Y. Liu, D. Floyd, A. Hassan, V. Khilkevich, and D. Beetner, “Characterization of the Electromagnetic Coupling to UAVs,” *Annual Directed Energy Science and Technology Symposium*, Feb 26-March 2, 2018.

13.4 Conference Presentations

13.4.1 Submitted / Accepted

[1] S. Bellinger, A. Caruso, A. Usenko, “Stacked Diodes for Pulsed Power Applications,” GOMACTech-22, Miami, FL, March 21–24 2022 (submitted, oral).

[2] S. Bellinger, A. Caruso, A. Usenko, “New Paradigm on Making Semiconductor Opening Switches for Pulsed Power,” 2021 23rd IEEE Pulsed Power Conference, Denver, CO, Dec. 12–16, 2021 (accepted, oral).

Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29 2021 (submitted):

[3] B. Barman, D. Chatterjee, A. Caruso, and K. Durbhakula, “Tradespace Analysis of a Phased Array of Microstrip Patch Electrically Small Antennas (ESAs)” (Poster)

[4] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation” (Poster)

[5] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures” (Poster)

[6] J. Bhamidipati, M. Paquette, R. Allen, and A. Caruso, “Photoconductive Semiconductor Switch Enabled Multi-Stage Optical Source Driver” (Poster)

[7] G. Bhattarai, J. Eifler, S. Roy, M. Hyde, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “All Solid-State High-Power Pulse Sharpeners” (Poster)

[8] S. Brasel, K. Norris, R. Allen, A. Caruso, and K. Durbhakula, “Efforts to Reduce Physical Aperture Area of Ultra-Wideband Arrays” (Poster)

[9] A Caruso, “ONR Short Pulse Research and Evaluation for c-sUAV: Supporting and Sub-Programs Overview” (Oral)

[10] J. Clark, R. C. Allen, and S. Sobhansarbandi, “Ultra-Compact Integrated Cooling System Development” (Poster)

[11] J. Eifler, S. Roy, M. Hyde, G. Bhattarai, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “TCAD Optimization of Epitaxially Grown Drift-Step Recovery Diodes and Pulser Performance” (Poster)

[12] N. Gardner, M. Paquette, and A. Caruso, “Diode-Based Nonlinear Transmission Lines Capable of GHz Frequency Generation at Single MW Peak Powers” (Poster)

[13] M. Hamdalla, A. Caruso, and A. Hassan, “The Shielding Effectiveness of UAV Frames to External RF Interference” (Poster)

[14] M. Hamdalla, A. Caruso, and A. Hassan, “A Predictive-Package for Electromagnetic Coupling to Nonlinear-Electronics using Equivalent-Circuits and Characteristic-Modes (PECNEC)” (Poster)

[15] M. Hyde, J. Eifler, S. Roy, G. Bhattarai, A. Usenko, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Development of an Evaluation Network for Drift Step Recovered Diodes through and Augmented Design of Experiment” (Poster)

[16] S. Indharapu, A. Caruso, and K. Durbhakula, “Machine Learning Based Ultra-Wideband Antenna Array Optimization and Prediction” (Poster)

[17] F. Khan, W. Azad, and A. Caruso, “A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Architecture for Pulsed Power Applications” (Poser)

[18] D. F. Noor, J. Eifler, M. Hyde, G. Bhattarai, S. Roy, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “DSRD-IES Pulsed-Power Generator Topology Study Using Machine-Learning-Based Feature Selection Optimization and Predictive Learning” (Poster)

[19] S. Roy, J. Eifler, M. Hyde, G. Bhattarai, D. Noor, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "Systematic Topological Optimization of DSRD-Based IES Pulse Generator" (Poster)

[20] S. Shepard and A. Caruso, "Tubular Core Optical Power Amplifier" (Poster)

[21] H. Thompson, M. Paquette, and A. Caruso, "Minimizing On-State Resistance in GaN:X Photoconductive Semiconductor Switches (PCSSs) for Direct Modulation (Poster)

[22] A. Usenko, J. Eifler, S. Roy, G. Bhattarai, M. Hyde, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "New Paradigm in Fabrication of Semiconductor Opening Switches for Pulsed Power" (Poster)

***

[23] S. Bellinger, A. Caruso, A. Usenko, "Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme," 240th Electrochemical Society Meeting, Orlando, FL, Oct. 10–14, 2021 (submitted, oral).

13.4.2 Presented

[24] W. Azad, S. Roy, and F. Khan, "A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver," *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, 2020 (oral).

[25] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, "Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS," *Annual Directed Energy Science and Technology Symposium*, March 2020 (abstract appeared, but talk cancelled due to pandemic).

***

DEPS Posters and Presentations 2020

[26] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[27] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

***

GOMAC 2019

[28] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[29] Eliot Myers, Picosecond High Power Switching Technologies

[30] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

***

[28] B. Barman, D. Chatterjee, and A. N. Caruso, "Analytical Models for L-Probe fed Microstrip Antennas," *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

***

Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium, Destin, Florida, USA, April 2019:

[29] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[30] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[31] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[32] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[33] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[34] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[35] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[36] Deb Chatterjee, Studies On Antenna Characterization And Propogation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

***

DEPS Posters and Presentations 2018

[37] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[38] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[39] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

***

DEPS Posters and Presentations 2017

[40] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

13.5 Theses and Dissertations

[1] Jordan N. Berg, “Development of a Jet Impingement Thermal Management System for a Semiconductor Device with the Implementation of Dielectric Nanofluids,” MS Thesis in Mechanical Engineering, University of Missouri-Kansas City, **2021** [doi].

13.6 IP Disclosures Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” 12AUG2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same,” 28JUNE2021.

[3] Bhamidipati, Myers, Caruso, “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources,” 21UMK009, 04NOV2020.

[4] Shepard, “A Low Noise Optical Amplifier,” 21UMK007, 14SEPT2020.

[5] Shepard, “A Novel Optical Fiber Amplifier,” 20UMK012, 02JUN2020.

[6] Shepard, “A Novel Optical Fiber Amplifier,” 20UMK012, 02JUN2020.

[7] Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna,” 20UMK011, 19APR2020.

[8] Doynov, “Scalable Modular System for High-power Microwaves Generation,” 20UMK010, 19APR2020.

[9] Doynov, “Pulse Differential High-power Microwave Generation,” 19UMK007, 02JAN2019.

[10] Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal,” 19UMK008, 28DEC2018.

[11] Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output,” 19UMK005, 28SEPT2018

13.7 Provisional Patents Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” filed 09/10/2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same” US Provisional Patent Application 63/216,550, filed June 30, 2021.

[3] P. Doynov, A. Caruso, “High-Efficiency High-Power Microwave Generation using Multipass Non-Linear Network Topologies,” filed 26NOV2019.

13.8 Non-Provisional Patents Filed

None to date

14.0 Appendix B: Si-PCSS Top Contact Optimization

(Jay Eifler)

14.1 Executive Summary

The silicon photoconductive semiconductor switch (Si-PCSS) requires a high energy laser to trigger the closing of the switch, with 1064-nm lasers being widely available and less expensive than other lasers. But high-average-power 1064-nm picosecond class lasers are too large and monetarily expensive for Navy afloat missions. To reduce laser size and cost, a redesign of the Si-PCSS top contact geometry has been completed using TCAD solutions to allow more efficient use of laser energy. The top contact geometry optimization is for a fixed 10-μm metal line width and for determining the best spacing between the metal lines (see Figure 1.3.1). A doping-dependent free carrier absorption photogeneration model is also employed to account for the laser illumination passing through the p-side anode contact first to reach the intrinsic region of the Si-PCSS and improves the simulation accuracy. Simulations have shown a 30% maximum possible percent laser energy reduction is possible when using the optimal 350-μm laser windowing spacing. Experiments with a small number of devices have shown a qualitative percent laser energy reduction when using optimal spacings. Further experimental data from a larger number of devices (due to device variability) is recommended to confirm simulation results of the possible percent laser energy reduction for the OSPRES mission.

14.2 Objective

High-average-power 1064-nm picosecond class lasers, necessary for activating silicon photoconductive semiconductor switches (Si-PCSS), are too large (1100 cm^3/W) and monetarily expensive ($1000/μJ*pulse) for the Navy afloat missions. For example, a laser of this class might occupy a volume of 1-m x 30-cm x 30-cm = 90,000-cm^3 and provide an average power of 50-W (thus, 1800-cm^3/W). A lab laser might cost $100,000 and deliver 100 μJ of laser energy to the Si-PCSS through fiber with 50% energy losses. By altering only Si-PCSS device parameters, one can enable both a laser size and cost reduction. Specifically, the laser energy required by the Si-PCSS can be reduced by altering the Si-PCSS top contact laser windowing spacing.

Si-PCSS top contact pattern designs are not known to have been published in detail. In-house patterns have used only an outer ring for the contact (resulting in high on-state resistance) and were improved by metallizing across the ring with filaments (to reduce current density high-points), similar to solar cell top contact designs. The Si-PCSS laser windowing spacings used were 10- and 20-μm, with 20-μm spacings achieving sufficiently low sub-ohm on-state resistance using in-house laser energy of ~100-μJ delivered to the Si-PCSS. However, there is no justification for 20-μm spacing being optimal for producing low sub-ohm on-state resistance with the least required laser energy. The solution is to optimize the OSPRES Si-PCSS top contact patterns using TCAD to meet reduced laser energy over a range of possible on-state resistances. Optimized top contact patterns require less laser energy, which enhances SWaP-C^2 for the laser system needed to drive the Si-PCSS.

14.3 Technical Background

Solar cells and photoconductive semiconductor switches (PCSS) both rely on metal contacts at the anode and cathode of the device (a diode) for electrical connection to outer circuits and both require an aperture in the anode electrode (or transparent electrodes) to allow light to enter the semiconducting material (here we are concerned with silicon). This top contact electrode has a metal geometry design that can be optimized for some specific application/performance metrics(s) by altering the geometry, referred to as geometric optimization (as opposed to topology optimization) [1]. Topology optimization (a mathematical method) has been applied to many multiphysics problems and does not require predefined configurations and can obtain any shape within the design space, for example leaf shaped solar cell contact designs. Solar cell top contact designs are optimized for the larger size of the solar cell/module and often for absorbing sunlight and comprise the bulk of top contact design in the literature [2-10]. PCSS are equivalent to a small solar cell in size and mostly use laser light. Due to the smaller size of the PCSS, the regular metal grid design (see Figures 1.3.1 and 1.3.2) without fingers suffices. We have also explored and fabricated the fingered grid of Figure 1.3.2 but have not optimized the design and it has not been compared to the regular grid designs (except, see Figure 1.6.5 for fishbone data).

The Si-PCSS studied in this report are 1-cm x 1-cm devices that are 1300-μm thick. The actual simulation model is 0.8-cm in width and is a 2D model (3D model with 1-μm thickness) that has a multiplicative length of 0.8-cm and is 1300-μm thick. Initial TCAD simulations used a 500-μm thick device for faster compute times. The results are meant to be applied to 7-cm x 0.5-cm devices which are too large to simulate in TCAD, but 1-cm x 1-cm devices have also been fabricated (see Figure 1.6.6) and are very close to the TCAD simulation model (0.8-cm x multiplicative 0.8-cm).

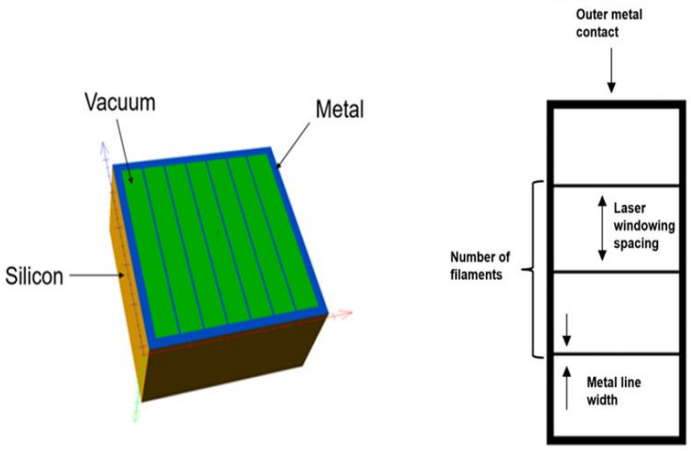


Figure 1.3.1. (Left) 3D mock-up of Si-PCSS with top contact pattern (blue). (Right) Top contact as 2D pattern from above/below showing laser windowing spacing between metal filament(s) of some metal line width (metal line width is 10 μm due to cost of manufacturing finer metal line widths.

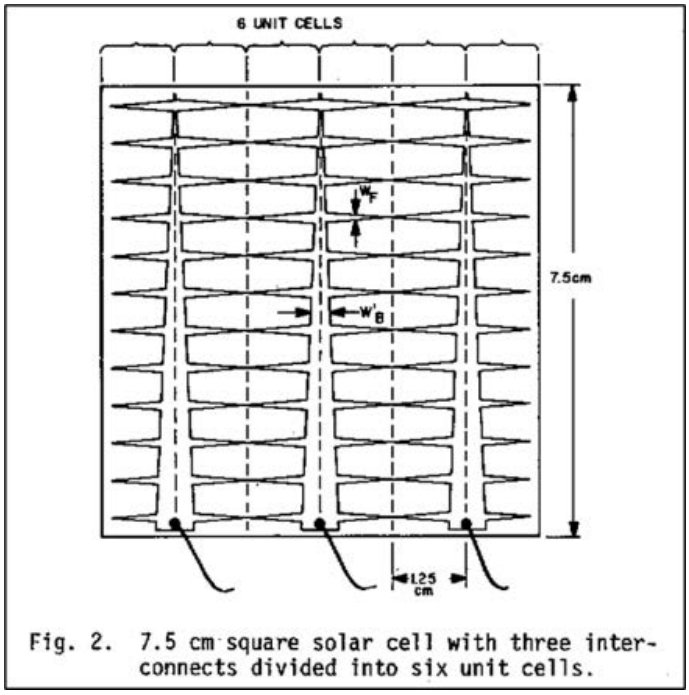


Fig. 2. 7.5 cm square solar cell with three interconnects divided into six unit cells.

Figure 1.3.2. Regular grid design with tapering and fingers with tapering [7].

It is also well known that a grid of crossed metal filaments is less efficient than a regular grid (regular grid is shown in Figure 1.3.1 at right). Choosing a regular grid as the basic top contact design leaves primarily the metal line width and laser windowing spacing as the geometric optimization parameters. (Other considerations can be made for the ends of the model—the extreme edges of the device where often the spacing is increased or filaments curved near the ends to improve performance—but we have not studied this effect.) The outer metal ring is made thicker (1-mm) for solderability. Solar cell top contact metal line optimization methods have been explored [8] showing that solar cell performance can be increased with narrower metal line widths. While metallization techniques have made finer metal dot resolution more cheaply available, cost effective metallization limits the metal line width to no less than 10-μm. The question then is what is the optimal spacing.

The simplest method of optimizing the spacing is increasing the width to allow more light in and therefore photogeneration of charge carriers in the silicon of the device. However, the current must travel to the metallization through the top-layer of the highly doped silicon. As the spacing widens to allow more light in, the current must travel further through the resistive top-layer. Ultimately there is a balance that is made between photogeneration and resistive losses [7]. For the PCSS in a simple pulse forming network (see Figure 1.3.3), the on-state resistance (R_{on}) is the measure of the efficiency with respect to the load resistance. Therefore, we use R_{on} to optimize the spacing for the PCSS (solar cells have different methods of determining efficiency and for optimizing top contact spacing).

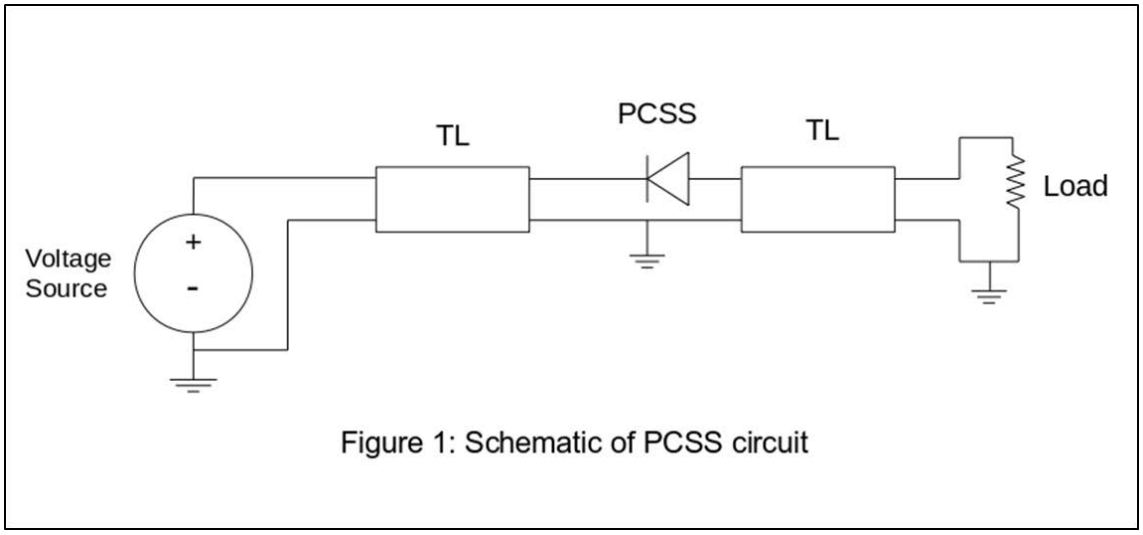


Figure 1: Schematic of PCSS circuit

Figure 1.3.3. Circuit schematic of the experimental on-state resistance test setup used for TCAD circuit simulation.

While various theoretical methods exist to calculate an optimal spacing [8,9], TCAD allows for a more detailed description of the device and modeling of the semiconductor device physics. Initial TCAD test simulations immediately showed the existence of an optimal spacing considering only R_{on}. Further TCAD simulations for fuller sized device models matched closely to the actual PCSS devices including doping-dependent free carrier absorption of laser light were carried out. The simulations were analyzed to determine the percent laser energy reduction vs window spacing and the optimal spacing producing the maximum amount of laser energy reduction.

The p-side doping of the Si-PCSS was originally chosen to allow more light to pass through and be absorbed in the intrinsic region of the device while balancing this concern with the higher p-side doping needed for an ohmic contact. In optimizing the top contact window spacing, a doping-dependent free carrier absorption method was needed in TCAD for the correct photogeneration and correct estimation of the required laser energy. A custom photogeneration model was developed considering doping dependent free carrier absorption in silicon [13-16].

14.4 Tasks, Milestones, and Status

(A) Perform literature review of solar cell top contact design / JUL 2020 / Solar cell top contact design useful for PCSS and theoretical methods best implemented in SPICE for the optimal metal line width and spacing.

The literature review provided understanding of the applicability and methods of solar cell top contact design to the PCSS. From this study, the metal line width was found to improve performance the narrower it can be made. Also, in practice, the optimal spacing is what is needed. The theoretical methods, implemented through SPICE circuit

simulation, provided the best method but are unavailable for PCSS or are difficult to self-implement.

(B) Determine if an optimal spacing based on on-state resistance exists with TCAD simulation / JUL 2020 / Milestone: TCAD successfully simulated the existence of an optimal spacing.

The earliest TCAD simulations performed for top contact optimization began to show the existence of optimal spacing, but it was not understood this should be examined until the literature review of solar cells. Further TCAD simulation conclusively showed the existence of the optimal spacing using on-state resistance as the performance metric for PCSSs.

(C) Develop doping-dependent free carrier absorption (DDFA) model for photogeneration in TCAD / 21 AUG 2020 / Milestone: TCAD DDFA modeled significant ~10% required laser energy increase.

Doping-dependent free carrier absorption (DDFA) was improved by refining the meshing used in TCAD simulations to produce no photogeneration underneath the top contact filaments. The top contact filaments are 10-μm wide and the mesh had to be refined to at least 5-μm with finer meshing down to 1-μm producing better results. Next, the TCAD model was implemented for 1-cm^2 area device models as opposed to earlier 1-mm^2 models. DDFA raised the required laser energy for an on-state resistance by 10%, showing it was non-negligible.

(D) Run parameter space study for 1300-μm thick Si-PCSS with DDFA / 12 NOV 2020 / Milestone: ~30% laser energy reduction;

Experimental on-state resistance versus laser energy results were almost exclusively conducted on 1300-μm thick Si-PCSS while TCAD simulations initially made use of thinner devices to reduce mesh points and save computational time. A new DDFA TCAD study has being completed for percent laser energy reduction vs spacing by first producing on-state resistance vs laser energy curves with a comparison to experimental data for 1300-μm devices. The inclusion of the DDFA photogeneration model greatly increased simulation time for the larger models. Due to mesh point limitations of a 1300-μm thick, 0.8-cm wide 2D device model was used. Simulation results indicate that a laser energy reduction of up to 30% is possible and needs experimental verification.

(E) Fabricate top contacts and test on-state resistance vs incident laser energy / 15 DEC 2020 to fabricate / Top contacts metallized / Milestone: FEB 2021 delivery of new top contacted Si-PCSS. MAR 2021 new top contacted Si-PCSS tested.

(F) TCAD determination of Si-PCSS variability in optimized top contacts dependent on p-doping profile peak concentration and doping depth for boron and aluminum. More accurate determination of optimal spacing in laser windowing of top contacts and switch

geometry dependence for general applicability of optimal top contact. / DEC 2020 / P-doping not found to effect optimal spacing. Finer determination on optimal spacing and geometry dependence of optimal spacing not completed.

P-doping was not found to significantly alter the optimal spacing. More accurate determination of the optimal spacing finer than 350-μm was never attempted but would help in distinguishing smaller shifts and trends in the optimal spacing varying with doping, applied voltage and laser energy. Additional simulations over a range of device sizes were not attempted to determine a scaling law for the results to larger devices (7-cm length scale).

14.5 Methods and Approach

Purely theoretical methods for solar cells were first consulted [7,8] in how to design and optimize PCSS top contacts. The theoretical approach suggested the regular metal grid design optimized for spacing was best, especially for smaller cells such as the PCSS. Theoretical methods are best realized in SPICE circuit simulation and methods exist to model full scale PCSS in detail but require manual development of the computer tools and are at the edge of computational feasibility [11,12]. Ready tools exist in TCAD for superior physical modeling, but for smaller scale PCSS models [3]. The approach then is to model a sufficiently large PCSS in TCAD for which the optimal spacing (considering a minimum 10-μm metal line width) will hold for both the smaller sized TCAD PCSS device models (0.8-cm width) and the actual full scale PCSS device (1-cm width). These two device sizes are nearly the same. The results of the 1-cm TCAD and experiments are then used for 7-cm width PCSS.

The window spacings studied for the TCAD simulations to determine the existence of an optimal spacing due to a lowest R_{on} were over a wide range as seen in Figure 1.6.1 and ranged from 10-μm to the full size of the device (no metal filaments) with a greater density of the studied spacings for smaller spacings. Later simulations for the percent laser energy reduction possible used 20-, 40-, 60-, 100-, 200- and 350-μm window spacings. The spacings larger than 350-μm were not studied since smaller spacings are thought to reduce the current density and heating, while larger spacings are useful when less metal is important for either cost or reflection of light back to the optics and the optical fiber. The computational cost of the simulations were also reduced by studying spacings less than or equal to the optimal spacing (note the earlier TCAD R_{on} vs spacing study for the existence of an optimal spacing less accurately determined the optimal spacing to be around 400-μm).

One factor of concern is the absorption of laser light (at 1064-nm in silicon) in the p-doped anode side of the PCSS since the light must first travel through the p-doped anode to the low n-doped intrinsic region. To account for additional doping-dependent free carrier absorption of 1064-nm in silicon, C programming code within TCAD function templates for photogeneration was modified. Other factors that could affect the R_{on} for various laser energies included area effects, reflectivity at the surface, and Gaussian vs uniform laser spatial profile (only uniform studied).

TCAD simulations determined that small enough width (and therefore area) devices had a different optimal spacing than for sufficiently wide devices for which the optimal spacing

no longer changed (also implies the applicability of the 1-cm simulation results to the 7-cm devices). The change in optimal spacing is in part due to the smaller number of possible metal filaments for a small width device (less than one hundred as opposed to several hundred metal filaments). The reflectivity of the TCAD model was matched to the R_{on} experimental testing conditions where the silicon surface (covered with an anti-reflective coating) is exposed to air directly, as opposed to being covered additionally with Silgard and plastic covering. There can be some experimental error on the reflectivity due to cleaning and finger smudges on the laser window.

A series of TCAD simulations in a 2D parameter study were performed. The 2D parameter study consisted of varying both laser energy delivered to the switch and window spacing. The simulations were performed isothermally at 300-K. The PCSS were simulated within a TL-circuit or simple pulse forming line (see Figure 1.3.3) closely resembling the actual experimental R_{on} test setup. R_{on} values from simulation were tabulated vs laser energy (figures in Section 1.6). These data were fit to power law functions, as R_{on} is known experimentally to be inversely proportional to the incident laser energy (rather than a purely linear interpolation of the data). From here, laser energy differences between different window spacings at a fixed R_{on} were collected relative to the 20-μm window spacing originally used. A percent laser energy reduction (E_{per}) vs R_{on} can then be tabulated:

$$E_{per} = \frac{E_{20} - E_{wid}}{E_{20}} * 100\%$$

where E_{20} is the baseline required laser energy for devices with a window spacing of 20-μm and E_{wid} is the wider window laser energy. Owing to the relatively flat or constant percent laser energy reduction per R_{on}, percent laser energy reduction vs spacing can be obtained.

14.6 Results and Discussion

Simulations

The first TCAD simulations were focused on verifying the existence of an optimal spacing based on R_{on} and not laser energy reduction. Subsequent TCAD simulations for laser energy reduction used a much lesser number of spacings and a greater number of laser energies. In Figure 1.6.1, spacings from 10-μm to the entire possible 8000-μm wide window (no metal filaments) are shown for the 1-cm device with 1-mm outer electrode. From about 100-μm to 1600-μm, R_{on} remains relatively low but outside these boundaries rises. For lower spacings the R_{on} rise is due to increasingly less laser light creating photogenerated carriers for conduction. For higher spacings the R_{on} rise is due to the increasing distance carriers must travel in the more highly conductive top-layer of silicon before reaching metal. It is thought that lower R_{on} should also result in better thermal management, but thermal studies are required. The optimal spacing is the spacing with the lowest R_{on} and was at 400-μm for this study (later studies refined the determination of the optimal spacing to 350-μm). Also, the optimal spacing is seen not to vary with increasing laser energy as R_{on} rises. Optimal spacing was also found (in other studies) to not vary much with p-side doping concentration or reverse-bias TL charge-side voltage.

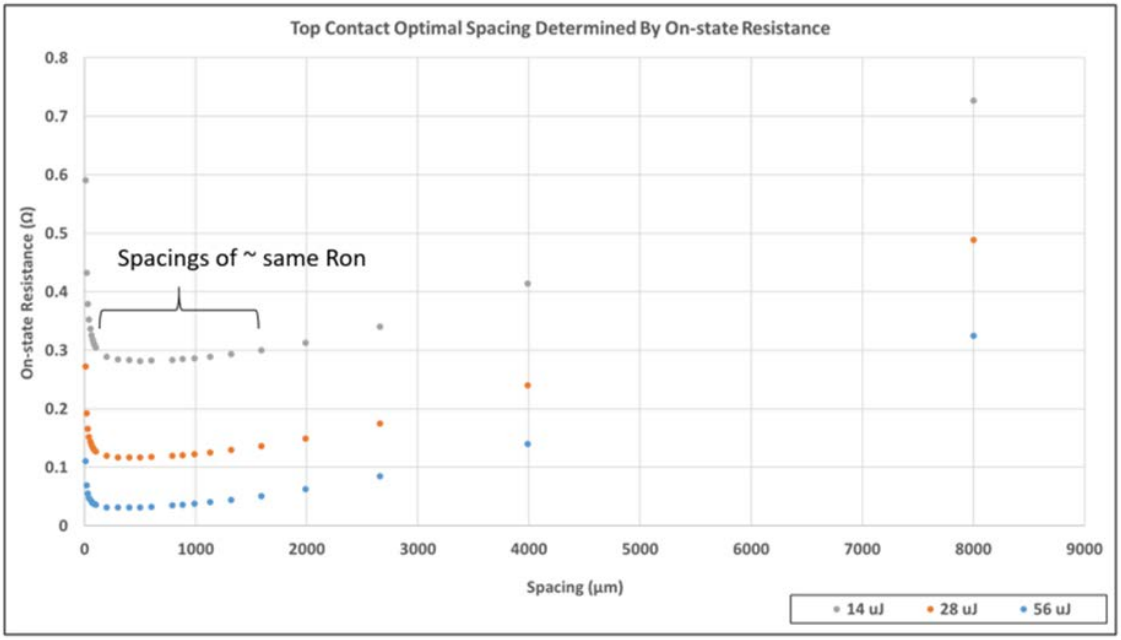


Figure 1.6.1. Window spacings show region of minimal on-state resistance (R_{on}) outside of which R_{on} increases dramatically.

A set of TCAD simulations were carried out with the goal of comparison to earlier experiments and a later set of planned experimental measurements using the R_{on} testing setup. A doping-dependent free carrier absorption (DDFA) model was added to the TCAD photogeneration model to account for absorption due to the highly doped p-side through which the laser light must travel to reach the thick intrinsic region of the Si-PCSS. Also, the reflectivity for the anti-reflective coating, silicon and air was added to the model to replicate test conditions. The data was visualized in the conventional R_{on} vs laser energy plots as in Figure 1.6.2. These additions to the modeling reduced the error between simulation and experiment.

The experimental data (exp) is seen to be within the ± 0.2-Ω error estimated for the R_{on} measurement when compared to the simulation results. Device variability plays a bigger role and must be averaged over enough devices to compare to experiment and simulation (for example see Figure 1.6.5). From the simulation curves, a power law is fit and the data points interpolated to more accurately estimate the laser energy difference between two spacing curves at a fixed R_{on} (due to the small number of simulation datapoints). The original spacing of 20-µm is used as reference to indicate improvement, as it happened the 20-µm spacing was not very optimal. A percent laser energy reduction curve vs R_{on} can then be tabulated as seen in Figure 1.6.3.

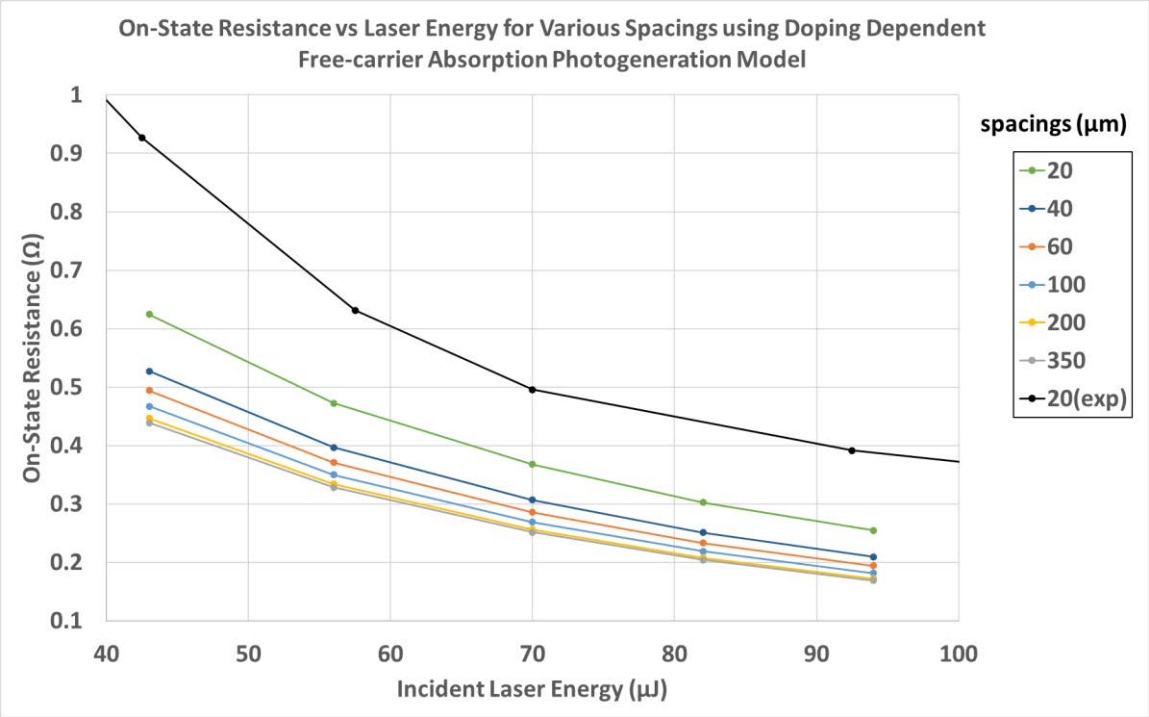


Figure 1.6.2. TCAD simulation results reproducing conventional on-state resistance vs laser energy curves as seen in experiment. (Black, top) exp line is for 20-μm spacing and is an experiment result.

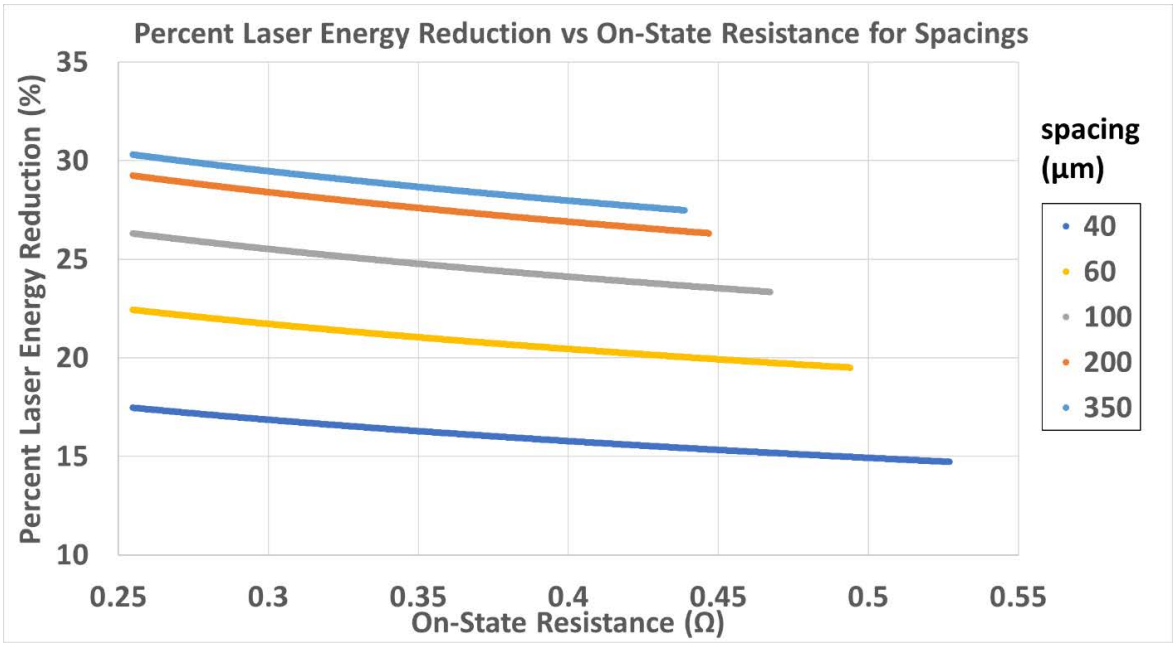


Figure 1.6.3. Percent laser energy reduction vs on-state resistance. The percent laser energy reduction across the on-state resistances tested (and laser energies used) is relatively flat or constant.

Since the percent laser energy reduction is nearly flat or constant over the range of R_{on} (and therefore laser energies) simulated, the average percent laser energy reduction can be plotted against the spacing, as in Figure 1.6.4.

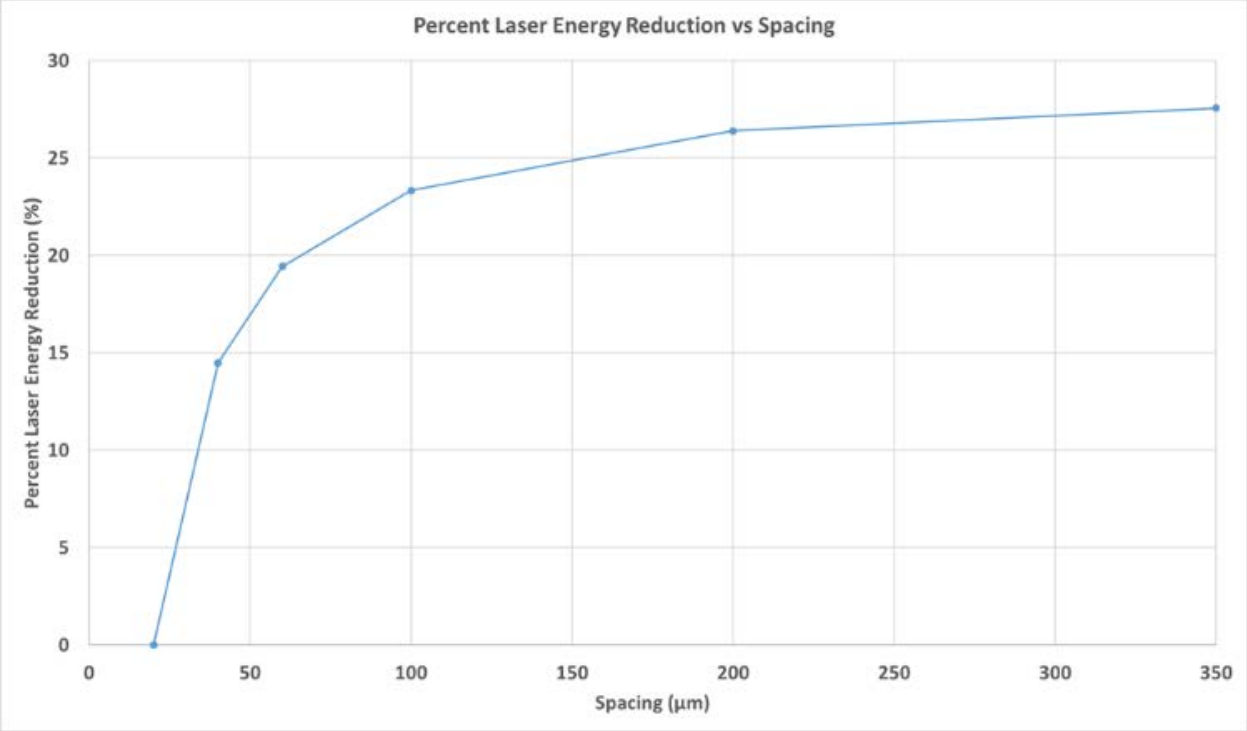


Figure 1.6.4. Percent laser energy reduction vs spacing curve shows 20-µm reference spacing with a zero percent laser energy reduction and the optimal 350-µm spacing with the maximum possible laser energy reduction (and minimum on-state resistance). Beyond 350-µm the percent laser energy reduction again reduces below the maximum possible.

The 20-µm spacing is assigned zero percent laser energy reduction as the reference spacing. After the 350-µm spacing, the percent laser energy reduction will decrease (see Figure 1.6.1) and 350-µm is the minimum R_{on} and maximum possible percent laser energy reduction spacing to the degree of accuracy of the simulated data test points (the optimal spacing could be slightly higher or lower). There are especially large gains in percent laser energy reduction in increasing the spacing from the original and reference spacing of 20-µm to 100-µm spacing (where R_{on} is approximately as low as it gets). From this simulation data, spacings between 100-µm and 350-µm can be considered as optimal with 350-µm having the maximum possible percent laser energy reduction and lowest possible R_{on}.

Experiments

Based on TCAD simulations, 2 wafers of Si-PCSS with variable window spacing were fabricated by Semiconductor Power Technologies (SPT). The metallization method itself is relatively cheap and fast. Table 1.6.1 shows the number of devices of each spacing for 1-cm and 7-cm devices from 2 wafers. Dicing damage on the 2 wafers resulted in only one 7-cm Si-PCSS being testable and fourteen 1-cm Si-PCSS. All the 1-cm devices showed higher resistance than expected which may have been due to dicing damage.

Table 1.6.1. Si-PCSS variable window devices fabricated by SPT.

Wafer spacing/devices	Spacings (µm) and number of devices fabricated per spacing						Total devices per wafer
1 cm spacings	20 µm	40 µm	60 µm	100 µm	200 µm	350 µm	
1 cm devices per spacing	6 devices	6 devices	6 devices	6 devices	6 devices	6 devices	36 devices
7 cm spacings	-	-	60 µm	-	-	350 µm	
7 cm devices per spacing	-	-	5 devices	-	-	5 devices	10 devices

Si-PCSS prior to this report were measured for their R_{on} vs laser energy curves and were all 7-cm devices. In Figure 1.6.5 the data for eight 7-cm devices are shown and all have 10-µm metal line width and 20-µm window spacing and are shown as open square symbols and are from an earlier study. A tenth new 7-cm device from this study is shown with black triangles which has a 350-µm window spacing. All the eight 7-cm devices (prior to this study) are fit to a power law as a dashed dark blue line (Power in the figure key) which can be compared to the new single 7-cm, 350-µm window spacing result (magnified in the top right figure inset where the black circle shows the laser energy difference at a fixed R_{on}). In the inset or larger figure can be seen the 20-µJ laser energy difference at ~0.8-Ω R_{on}. With only one device the results could be fortuitous due to device variability, but are encouraging. Note, the single surviving 7-cm device from this study was badly damaged from dicing but did have R_{on} within the previously tested 7-cm as seen in Figure 1.6.5, however the new 1-cm devices (Figure 1.6.6) had higher R_{on} than previously tested 1-cm devices (no data provided but within earlier grant reports).

In Figure 1.6.6 the experimental data between 50-µJ and 100-µJ of laser energy are shown. The open symbols can be seen to occupy mostly the lower R_{on} values obtained across the laser energies tested. By grouping the results into 100-µm and greater and less than 100-µm spacing, the R_{on} vs laser energy curves of the two groups can be compared, see Figure 1.6.7.

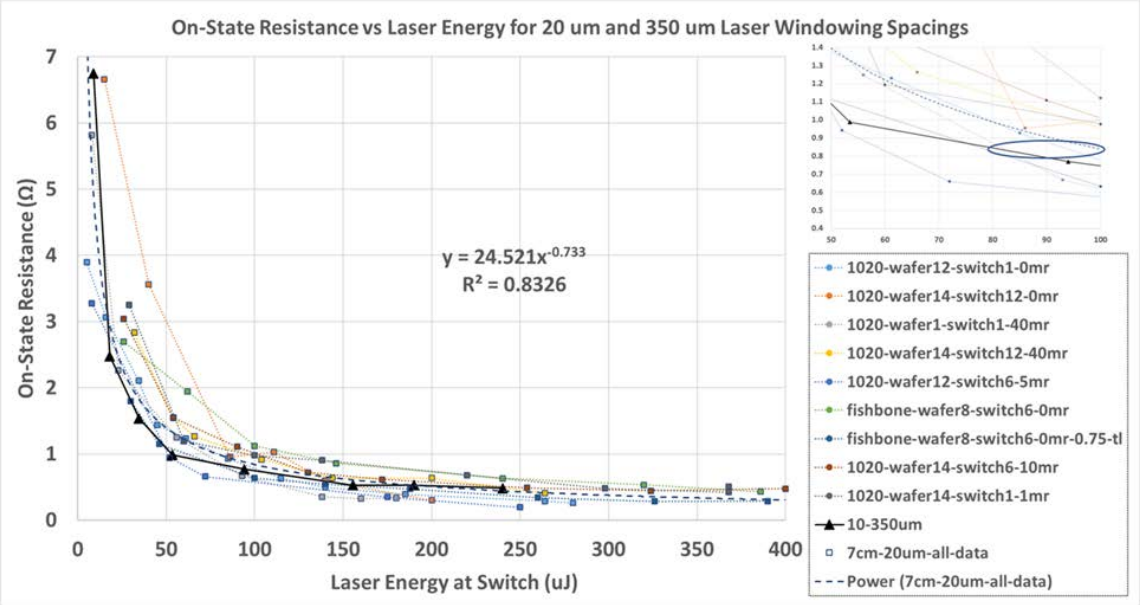


Figure 1.6.5. On-state resistance vs laser energy incident at switch for eight 7-cm, 20-μm window Si-PCSS and a single 7-cm, 350-μm Si-PCSS (large black triangles). Half of the 20-μm curves are nearly the same as the 350-μm curve. The dashed dark blue line is the power law fit to the 20-μm data. The inset is a magnification of the region comparing laser energy used at ~0.8-Ω on-state resistance between the 350-μm device and the 20-μm data. The circled region in the inset shows the 20-μJ laser energy reduction.

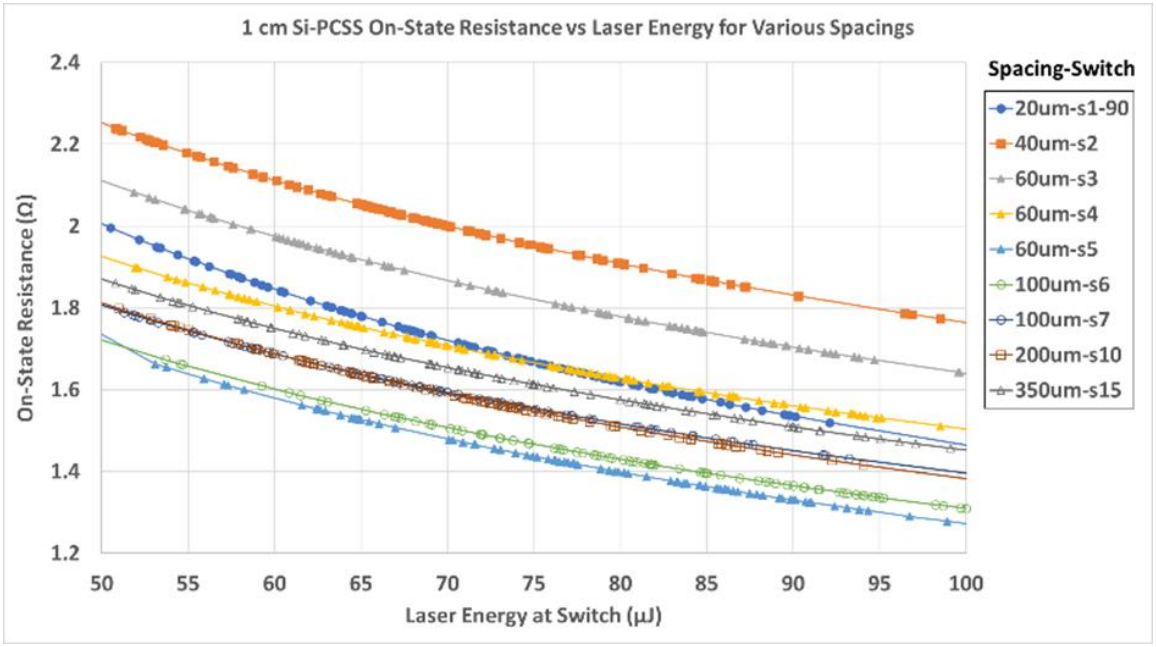


Figure 1.6.6. Experimental on-state resistance vs laser energy curves for SPT variable window Si-PCSS.

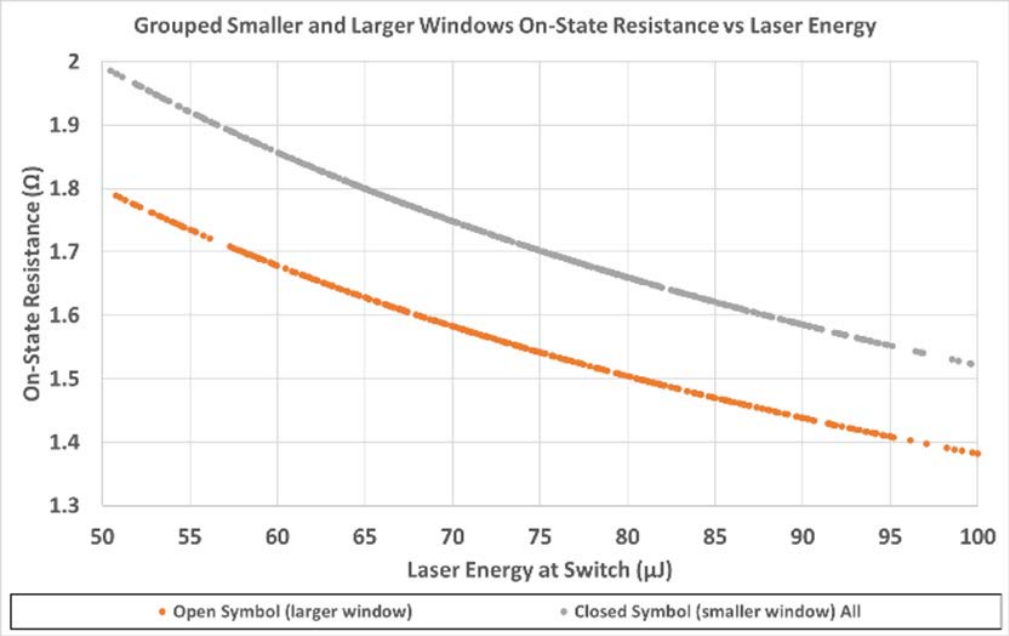


Figure 1.6.7. On-state resistance vs laser energy curve with the less than 100-µm window spacing results (gray) and 100-µm and greater results (orange) averaged together. A 22% laser energy reduction can be seen in the graph between the 100-µJ (gray) data point and the (orange) datapoint at the same on-state resistance (at ~1.52-Ω).

A 22% laser energy reduction can be deduced from the graph of the two groups which is over-estimated due to the device variability and low number of devices experimentally tested. The analysis of the experimental data provides a qualitative result of a significant percent laser energy reduction for devices that have approximately optimal R_{on} (100-µm to 350-µm spacing). Stronger experimental data would yield useful information for publication and inhouse device performance. A study of 2 or more wafers of 1-cm devices, where dicing damage does not occur will likely yield lower R_{on} devices, and a larger number of good devices. And should produce stronger data confirming or not the simulated R_{on} vs laser energy, percent laser energy reduction vs spacing, and the optimal spacing for maximal percent laser energy reduction. The experimental and simulation data were not comparable on an absolute scale due to a higher than usual R_{on} for the actual 1-cm devices that received dicing damage, but the relative trend of larger windows having greater percent laser energy reduction held between simulation and experiment.

14.7 Summary and Recommendations

A laser is necessary to trigger the closing of the Si-PCSS but requires a high laser energy which leads to higher costs and sizes of the laser system. To reduce the required laser energy, purely theoretical and SPICE methods were first explored for Si-PCSS top contact optimization, which led to exploring TCAD simulations to test for an optimal on-state resistance. After showing an optimal on-state resistance existed using TCAD simulation, more complete top contact window spacing and laser energy studies were performed with a doping-dependent free carrier absorption model being added to the

photogeneration model to improve the accuracy of the results. Further simulations with more realistic device sizes were executed and a percent laser energy reduction versus top contact window spacing was tabulated. TCAD simulation results showed a possible maximum ~30% laser energy reduction when using the optimal 350-μm spacing. Experimental results confirmed a qualitative effect of increased laser energy reduction with more optimal spacings. More and better devices will be needed to verify conclusively the simulation results with experimental data. It is recommended to fabricate and test another 2 wafers of 1-cm Si-PCSS with variable window spacing to experimentally confirm the TCAD optimal spacing and percent laser energy reduction.

14.8 Outputs

Photoconductive Contact Pattern for Enhanced Charge Collection, July 8, 2020, IP disclosure.

14.9 References

[1] Gupta, D. K., Matthijs Langelaar, Marco Barink, and Fred van Keulen. "Topology optimization of front metallization patterns for solar cells." Structural and Multidisciplinary Optimization 51, no. 4 (2015): 941-955.

[2] Wen, Liu, Li Yueqiang, Chen Jianjun, Chen Yanling, Wang Xiaodong, and Yang Fuhua. "Optimization of grid design for solar cells." Journal of Semiconductors 31, no. 1 (2010): 014006.

[3] “Optimizing Solar Cell Top Contact Design Introduction.” The Simulation Standard, April-May 2015.

[4] Van den Donker, M. N., P. A. M. Wijnen, S. Krantz, V. Siarheyeva, L. Janßen, M. Fleuster, I. G. Romijn et al. "The starfire project: Towards in-line mass production of thin high efficiency backcontacted multicrystalline silicon solar cells." Proc. of 23rd EU PVSEC, Valencia, Spain (2008).

[5] Mette, Ansgar. New concepts for front side metallization of industrial silicon solar cells. Verlag Dr. Hut, 2007.

[6] Schroder, Dieter K., and Daniel L. Meier. "Solar cell contact resistance—A review." IEEE Transactions on electron devices 31, no. 5 (1984): 637-647.

[7] Serreze, H. B. "Optimizing solar cell performance by simultaneous consideration of grid pattern design and interconnect configuration." 13th IEEE PVSC, 1978 609 (1978).

[8] Heizer, K. W., and T. L. Chu. "Solar cell conducting grid structure." Solid-State Electronics 19, no. 6 (1976): 471-472.

[9] Wong, Johnson. "Griddler: Intelligent computer aided design of complex solar cell metallization patterns." In 2013 IEEE 39th Photovoltaic Specialists Conference (PVSC), pp. 0933-0938. IEEE, 2013.

[10] Unsur, Veysel, Nian Chen, and Aba Ebong. "A mathematical investigation of the impact of gridline and busbar patterns on commercial silicon solar cell performance." Journal of Computational Electronics 19, no. 2 (2020): 854-865.

[11] Zekry, Abdelhalim, and Abdulhameed Yousef Al-Mazroo. "A distributed SPICE-model of a solar cell." IEEE Transactions on Electron Devices 43, no. 5 (1996): 691-700.

[12] Eidelloth, Stefan, Felix Haase, and Rolf Brendel. "Simulation tool for equivalent circuit modeling of photovoltaic devices." IEEE Journal of Photovoltaics 2, no. 4 (2012): 572-579.

[13] Vardanyan, R. R., V. K. Dallakyan, U. Kerst, and C. Boit. "Modeling free carrier absorption in silicon." *Journal of Contemporary Physics (Armenian Academy of Sciences)* 47, no. 2 (2012): 73-79.

[14] Falk, R. Aaron. "Near IR absorption in heavily doped silicon-an empirical approach." In *International symposium for testing and failure analysis*, pp. 121-128. ASM International; 1998, 2000.

[15] Horwitz, C. M., and R. M. Swanson. "The optical (free-carrier) absorption of a hole-electron plasma in silicon." *Solid-State Electronics* 23, no. 12 (1980): 1191-1194.

[16] Baker-Finch, Simeon C., Keith R. McIntosh, Di Yan, Kean Chern Fong, and Teng C. Kho. "Near-infrared free carrier absorption in heavily doped silicon." *Journal of Applied Physics* 116, no. 6 (2014): 063106.

ONR HPM Program - Monthly Status Report (MSR) – SEPTEMBER 2021

Anthony Caruso – Univ. Missouri – Kansas City

N00014-17-1-3016 [OSPRES Grant]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study

15 OCTOBER 2021

Distribution Statement ~A: Distribution authorized to all OSPRES Grant and Contract performers, and any OSPRES uncompensated collaborators. Further dissemination per the Office of Naval Research, Ryan Hoffman (ryan.hoffman@navy.mil, 703-696-3873) or higher DoD Authority.

OSPRES Grant Goal: address and transition technologies and capabilities that enable the OSPRES Grant Objective using the OSPRES Grant Approach, while educating the next generation of pulsed power and defense minded, stewards and innovators.

OSPRES Grant Objective: to execute high-risk, high-payoff efforts that mitigate, fill or rectify one or more grand-challenge or elementary gaps or deficiencies needed to achieve a modular, scalable and electronically steerable high power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission. The OSPRES HPM system and sub-system development/evaluation efforts are focused on the short-pulse high-average-power space, and includes the kill chain considerations including the target and its responsivity to radiofrequency stimuli.

OSPRES Metrics of Success: developed technologies and capabilities that are published in the peer review, protected as intellectual property, and/or, transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use, as enabling/integratable capability(ies).

OSPRES Grant Approach: A fail-fast philosophy is maintained, where if a technology or capability is deemed infeasible to be demonstrated or validated during the project period-of-performance, it shall be culled, results to date and basis of infeasibility documented, and the next major gap/deficiency area addressed by that part of the project sub-team. Students whose thesis depends on following through with a full answer during the life of the award will be given special dispensation to continue their work.

OSPRES Grant Security: All efforts should be fundamental and publically releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

1.0 Contents

2.0 Executive Summary 4
2.1 Progress, Significant Findings, and Impact 4
2.2 Completed, Ongoing, and Cancelled Sub-Efforts 7
2.3 Running Total of Academic and IP Program Output 9
3.0 Prime Power and Conditioning 10
3.1 HV Switch Pulsed Chargers 10
4.0 Laser Development 15
4.1 Fiber Lasers and Optical Amplifiers 15
4.2 WBG-PCSS Enabled Laser Diode Array Driver 21
5.0 Photoconductive Switch Innovation 26
5.1 Characterizing and Optimizing On-State Resistance in GaN:X PCSS 26
6.0 Drift-Step-Recovery-Diode-Based Source Alternatives 29
6.1 Drift-Step Recovery Diode and Pulse Shaping Device Optimization 29
6.2 Pioneering Drift-Step Recovery Diode Processing and Manufacturing 38
6.3 Characterization of SOS Diode Performance through DOE Augmentation 45
6.4 DSRD-Based Pulsed Power Source Systematic Topological Optimization 52
6.5 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners 57
7.0 GaN-Based Source Alternatives 65
7.1 Development of a GaN-Based Power Amplifier RF Source 65
8.0 Thermal Management 69
8.1 Ultra-Compact Integrated Cooling System Development 69
9.0 Pulse Forming Networks 73
9.1 Diode-Based Nonlinear Transmission Lines 73
9.2 Continuous Wave Diode-NLTL based Comb Generator 77
10.0 Antenna Development 81
10.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs) 81
10.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna 88
10.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna 95
10.4 Machine Learning Inspired Tradespace Analysis of UWB Antenna Arrays 101
11.0 RF Coupling 109
11.1 Enclosure Effects on RF Coupling 109
12.0 UAS Engagement Wargaming & Modeling and Simulation (M&S) 112
12.1 Fixed-Effector Wargaming Simulation Toolkit Development 112
12.2 Airborne Effector Weapons Target Assignment 116
13.0 Program Management 117
13.1 Issues 117
13.2 Interactions with Others 117
13.3 Major Procurement Actions 117
13.4 Travel 117
13.5 Pending or Upcoming Public Release Requests 117
14.0 Appendix A: Academic and IP Output 118

14.1 Students Graduated....118
14.2 Journal Publications....118
14.3 Conference Publications....120
14.4 Conference Presentations....123
14.5 Theses and Dissertations....126
14.6 IP Disclosures Filed....127
14.7 Provisional Patents Filed....127
14.8 Non-Provisional Patents Filed....127

2.0 Executive Summary

2.1 Progress, Significant Findings, and Impact

HV Switch. A completely redesigned optical fiber TX-RX module has been used to enhance the voltage breakdown rating of the driver circuit. A new gate driver board has been fabricated and tested. This modified architecture is likely to eliminate arcing at voltage levels greater than 6.5 kV.

Fiber Laser and Optical Amplifiers. In progressing our build of a proof-of-concept prototype, the power combiners have been assembled and spliced to the Yb doped optical fiber pre-amp. Towards the end of simplifying the entrance-optics (between fiber preamp and tubular power amp) while maintaining spatial uniformity in the power amp output (to within 25% for the simultaneous triggering of an array of PCSS) we consider illuminating the tube with a finite number of "spots" (e.g., 1, 2 or 4), which could be passively split from the fiber pre-amp, and find that 4 spots suffice but 2 spots or 1 spot will not.

Laser Diode Array Driver. A 150-V 8-segment frozen wage generator (FWG) with pulse width chirp (12–21 ns) capability has been demonstrated on a 2.3″ × 3.5″ PCB and the performance has been evaluated under balanced and unbalanced load configurations to compare their frequency response. Issues with negative pulse train overlap were noticed at >50 V charge voltage under unbalanced load (50 Ω and 0.1 Ω), resulting in a single ~200 ns long pulse with deteriorated frequency response. Parasitics along the reflected path are suspected for potentially causing delays in the LC segment charge/discharge cycle that led to the pulse overlap. This issue will be addressed in the next report cycle along with the implementation of a motorized FWG prototype to facilitate dynamic pulse width tuning.

On-State Resistance in GaN:X PCSS. Towards finding controllable parameters that affect on-state resistance in GaN:X-based photoconductive semiconductor switch (PCSS) systems to increase system efficiency and reduce conduction losses, the literature study was continued and the parameter chart from last month was updated. Much of the analysis in the literature for PCSS on-state resistance is based on vertical devices, so it will be necessary to compare available experimental data to simulation results of lateral devices to determine if simulation results are valid or if additional physics needs to be considered. The next steps will be to begin building a GaN:X PCSS model in COMSOL and/or TCAD.

IES Pulsed Power Source Technology Leveraging DSRDs. LTspice simulations, fed from expanded I(V) and C(V) data on varying drift-step recovery diodes (DSRDs), demonstrate a limit to the DSRD model accuracy (~90%) of matching the peak voltage and risetime measured experimentally. Alternative simulation software and enhanced models are being explored to mitigate this issue. New 'Gen2' diodes, provided by Semiconductor Power Technologies, are being experimentally evaluated to inform SPT which manufacturing procedure(s) enable(s) optimal diode performance parameters prior to processing the epitaxially grown Gen3 DSRDs. Incorporating lessons learned and new methods to increase peak performance, the latest iteration of the DSRD inductive energy

storage (IES) pulse generator (4×2) is nearing completion of the prototyping phase to facilitate testing. Accompanying this effort, the approach to utilize DSRDs as dynamic breakdown diodes operating in reverse bias and recovery mode, is being employed as a SWaP alternative to the limited COTS items. Combining the efforts, a multi-megawatt, sub-nanosecond, time-aligned pulse generator, using consistent/matching DSRDs, will be developed that can meet the required performance for use within the Naval afloat mission.

GaN-Based Power Amplifier RF Source. We have begun the development of a non-MMIC (i.e., discrete transistor) MPM RF amplifier that will generate several MWs of peak output power, leveraging the ones-of-kW GaN HEMTS now available (e.g., MACOM 2600-W A1500). When the long pulse width signals are compressed, the peak power and energy are commensurate with that required from the OSPRES contract program, and a strong differentiator from GaN MMIC based array technologies. Magnetic pulse compression (MPC) and time reversal (Drikas collaboration) are two foci. Components required to build the MPC unit have been purchased and it is currently being built to verify functionality. If MPC lives up to its literature-based promise, the built prototype along with a narrow high gain antenna , should facilitate a platform to realize a portable GaN-based amplifier systems with >100-m range-to-effect.

Thermal Management. Geometry and microchannel techniques for the ultracompact cooling system were thoroughly reviewed based on manufacturing tolerances and techniques. A preliminary design consisting of an array of 421 nozzles and 22 microchannel heat sinks embedded onto a semiconductor was obtained following the beginning of the simulation process in ANSYS. Poor mesh quality within the large number of micro-scaled nozzles arose leading to individually face sizing certain bodies within the 3 x 3 mm concept, following the good quality mesh simulation will take place to achieve a heat dissipation rate of 1 kW/cm^2.

Diode-Based Nonlinear Transmission Line. Simulations were performed on the lossy K50F D-NLTL simulation model with the goal of matching measurements from August. Using only changes to the R_L, C_L, L_D, and C_D sources of loss in the inductor and diode models, simulation was able to match center frequency and Bragg frequency within 5% of the measured values. However, pulse modulation depth measurements were not able to be matched. These results indicate good support for the use of R_L, C_L, L_D, and C_D in SPICE with the need for more accurate physical modeling of diode behavior.

Continuous Wave Diode-NLTL Based Comb Generator. This effort is aimed at taking advantage of the average impedance of a D-NLTL network to improve source–line impedance mismatch. Initial simulations were performed, along with low-voltage measurements to understand the potential effect of continuous-wave excitation on source–line impedance mismatch on D-NLTLs. Both simulation and experimental measurements indicated a minor improvement with continuous excitation, but no dependence on excitation frequency was observed. Improvements in impedance matching for low- and high-voltage prototypes under diode biasing will be studied in the next reporting cycle.

Antennas. Optimization of the design parameters of the previously designed microstrip patch ESA element at the UHF range (0.6-1 GHz), via ML algorithms, resulted in 22%

physical aperture area reduction and 6% bandwidth improvement, but at the cost of 12% loss in peak gain. The optimization of array parameters to reduce the mutual coupling between individual elements in a 5x5 array of ESA elements, via ML algorithms and Pareto optimality, was initiated.

The diamond Koshelev antenna array, which is 50% the size of a square Koshelev antenna array, resulted in at least 2 dBi higher gain than the square topology at 900 MHz when fed by a monopolar pulse. The elliptical Shark antenna array has significantly lower sidelobe levels (< -30 dB) and identical gain value at 900 MHz when compared against a square Shark antenna array. On the machine learning side, RBF was found to have smaller RMSE values than LSR for S11 prediction and vice-versa for gain and electric field predictions for test data outside the training range.

RF Coupling. In previous reports, we developed an accurate model for the wires and electronic circuitry of quadcopter Unmanned Aerial Vehicles (UAVs) using a desktop 3D scanner. The Equivalent Circuit Approach (ECA) was successfully applied to the complex 3D wiring system to develop a circuit representation, which is orders of magnitude faster than full-wave simulations. This month, we used the ECA to vary the electronic devices/loads over a wide range. Since the device/load value is unlikely to be known exactly, we wanted to answer the fundamental question: what matters most, traces/wires or the devices/loads? Our preliminary results show a frequency range where the RF coupling will be insensitive to the load variations, which will help predict the optimum waveform to maximize the coupling when the exact UAV loads are unknown. Detailed results will be presented next month upon completion of all simulations

UAS Engagement Modeling and Simulation. Experimental data was collected from a Navy UAS tracking event. Analysis is ongoing to create an empirically driven radar tracking model. Similarly, a literature review was initiated to characterize additional effectors and tracking platforms for inclusion into the simulation framework. Additionally, the development of a task assignment framework capable of directing many friendly forces against a swarm attack has demonstrated success (in simulation) and has transitioned to the PTERA program.

2.2 Completed, Ongoing, and Cancelled Sub-Efforts

2.2.1 Ongoing Sub-Efforts

	Start	End
GaN:C Modeling and Optimization	OCT 2017	Present
Diode-Based Non-Linear Transmission Lines	FEB 2018	Present
HV Switch Pulsed Chargers	DEC 2018	Present
Trade Space Analysis of Microstrip Patch Arrays	FEB 2019	Present
Enclosure Effects on RF Coupling	OCT2019	Present
Lasers and Optics	FEB 2020	Present
UWB Antenna Element Tradespace for Arrays	MAY 2020	Present
WBG-PCSS Enabled Laser Diode Array Driver	NOV 2020	Present
Si-PCSS Contact and Cooling Optimization	JAN 2021	Present
Drift-Step Recovery Diode Optimization	JAN 2021	Present
UAS Engagement M&S	MAR 2021	Present
DSRD-Based IES Pulse Generator Development	APR 2021	Present
Drift-Step Recovery Diode Manufacturing	MAY 2021	Present
IES Diode Characterization	MAY 2021	Present
Sub-Nanosecond Megawatt Pulse Shaper Alternatives	MAY 2021	Present
Ultra-Compact Integrated Cooling System Development	MAY 2021	Present
GaN-Based Power Amplifier RF Source	AUG 2021	Present
Reconfigurable RF Pulsed-Power Source	AUG 2021	Present
RF Driver Unit for GaN SD-MPM Power Amplifier	SEPT 2021	Present
Reconfigurable RF Antenna for SD-MPM Sources	SEPT 2021	Present
Continuous Wave Diode-NLTL Based Comb Generator	SEPT 2021	Present

2.2.2 Completed Sub-Efforts

Adaptive Design-of-Experiments	OCT 2017	APR 2019
Non-perturbing UAV Diagnostics	OCT 2017	OCT 2018
Noise Injection as HPM Surrogate	OCT 2017	MAR 2019
SiC:N,V Properties (w/ LLNL)	APR 2018	MAR 2019
Helical Antennas and the Fidelity Factor	JUL 2018	SEPT 2019
Si-PCSS Top Contact Optimization	APR 2020	OCT 2020
Nanofluid Heat Transfer Fluid	NOV 2020	JUL 2021

2.2.3 Cancelled/Suspended Sub-Efforts

Ab Initio Informed TCAD	OCT 2017	OCT 2020
Positive Feedback Non-Linear Transmission Line	NOV 2017	DEC 2018
Minimally Dispersive Waves	FEB 2018	SEPT 2018
Multiferroic-Non-linear Transmission Line	NOV 2018	APR 2019
Avalanche-based PCSS	SEPT 2018	SEPT 2019
Gyromagnetic-NLTL	DEC 2017	NOV 2020
Multi-Stage BPFTL	APR 2020	JUL 2020

Heat Transfer by Jet Impingement	MAY 2018	FEB 2021
Si, SiC, and GaN Modeling and Optimization	NOV 2018	FEB 2021
Bistable Operation of GaN	FEB 2021	MAR 2021
IES Pulser Machine Learning Optimization	MAY 2021	AUG 2021

2.3 Running Total of Academic and IP Program Output

See Appendix for authors, titles and inventors (this list is continuously being updated)

Students Graduated	*5 BS, 8 MS, 3 PhD*
Journal Publications	*3 (6 submitted/under revision)*
Conference Publications	*33 (4 submitted/accepted)*
External Presentations/Briefings	*17 (23 submitted/accepted)*
Theses and Dissertations	*4*
IP Disclosures Filed	*10*
Provisional Patents Filed	*4*
Non-Provisional Patents Filed	*0*

3.0 Prime Power and Conditioning

3.1 HV Switch Pulsed Chargers

(Sarwar Islam and Faisal Khan)

3.1.1 Problem Statement, Approach, and Context

Primary Problem: Commercially available high-voltage solid-state switches made by BEHLKE are the best in SWaP-cooling, but are expensive, have long lead times (2–3 months), and are made outside of the US. For the Navy afloat mission to be successful, we need a sustainable supply of US-manufactured switches at a much lower cost.

Solution Space: Design and demonstrate modular high-voltage (~10 kV) and fast (repetition frequency = 100 kHz) solid-state switches using a combination of series- and parallel-connected commercially available inexpensive discrete MOSFETs and custom high-voltage (~10 kV) isolated gate drivers.

Sub-Problem: Voltage balancing among the series-connected MOSFETs, minimization of gate signal delays, cooling of the individual MOSFETs, balancing resistors, high-voltage isolation required for the power supplies, and the controlling pulse width modulated (PWM) signal as well as differential voltage feedback measurement across individual MOSFETs.

State-of-the-Art (SOTA): Direct liquid-cooled solid-state switch from BEHLKE (e.g., HTS-151-30).

Deficiency in the SOTA:

1. BEHLKE-made switches are expensive. For instance, a single HTS-151-30 switch costs around $5,000.
2. BEHLKE switches along with direct liquid cooling units occupy a considerable amount of space. For instance, an HTS-151-30 switch from BEHLKE has a footprint of approximately 225*85*75 mm without considering the liquid cooling system. Some key parameters of this switch are as follows.

   i) Maximum operating voltage = 15 kV

   ii) Maximum continuous load current = 2.52 A (without cooling), 30 A (with liquid cooling)

   iii) Maximum turn-ON peak current = 300 A (pulse width = 200 µs, duty cycle <1%)

   iv) Turn-ON resistance = 1.3 Ω
3. Once the switching frequency is greater than 10 kHz, a liquid cooling system is required to operate the BEHLKE switch.
4. Without liquid cooling, the maximum continuous power dissipation (P_{cont}) of the BEHLKE switch is limited (e.g., for HTS-151-30, P_{cont} is 10 W without liquid cooling).
5. At a higher switching frequency (>20 kHz), the BEHLKE switch requires multiple ancillary DC power supplies, i.e., 5, 15, and 60 V.

6. The switches made by BEHLKE cannot be reconfigured to withstand a higher voltage exceeding their recommended rating. BEHLKE offers separate products to operate them at higher voltage/currents.

Solution Proposed: Designing a modular high-voltage (~10 kV) switch using a single custom isolated gate driver for each module and having a construction cost lower than the BEHLKE switch with equivalent or better performance in all specification categories (Specifications for the BEHLKE switches can be found in the following link: http://www.behlke.com/separations/separation_c4.htm).

Relevance to OSPRES Grant Objective: The proposed modular high-voltage switch is expected to facilitate controlled hundreds-of-nanosecond charging of an array of transmission lines of pulse forming networks to drive an array of PCSSs, thereby producing controlled hundreds-of-picosecond scale high-voltage pulses.

Risks, Payoffs, and Challenges:

I. Lack of rigid control over voltage balancing can lead to a cascaded failure among the series-connected MOSFETs.

II. In the absence of an adequate mitigation scheme, voltage overshoot due to the fast switching speed can exceed the voltage rating of an individual MOSFET, thereby damaging the switch.

III. At high voltage (~10 kV) and high repetition rate (>100 kHz), mitigating EMI to safeguard the individual MOSFETs from false turn-ON is a major challenge.

3.1.2 Tasks and Milestones / Timeline / Status

(A) Design a surface-mount MOSFET-based four-stage switch (6.8 kV rated) and control it using the in-house gate driver, then test its voltage-withstanding ability with a DC supply voltage up to 4–5 kV and evaluate the effectiveness of the thermal management at its current state / DEC 2020 / Completed.

(B) Design and develop a modular HV switch (~10 kV rated) using the concept of the tested four-stage high-voltage switch module and an in-house modular gate driver to drive the modular switch /JAN–FEB 2021 / Completed.

(C)

(i) Test the voltage withstanding ability of the modular HV switch with a DC supply voltage up to 10 kV and switching frequency up to 50 kHz using a resistive load (5–10 kΩ) and evaluate the effectiveness of the thermal management at its current state / FEB–SEP 2021 / Ongoing.

(ii) Test the isolation capability and evaluate the synchronization accuracy of the gate drive signal generated from the modular in-house gate driver / FEB–SEP 2021 / Ongoing.

(iii) Encapsulate the gate driver board with potting material with a high (~15–20 kV) breakdown voltage rating to prevent possible flashover/arcing in between the HV switch and this board / MAR–SEP 2021 / Ongoing.

(D) Design and fabricate a compact power conditioner circuit based on a 12 kV rated SiC switch made by BEHLKE (HTS 121-15) / APR–MAY 2021 / Completed.

(E) Test this modular HV switch coupled with a Si PCSS device up to a DC supply voltage of 5–6 kV and a switching frequency of 50 kHz / SEP 2021 / Ongoing.

(F)

(i) Design and develop a 20 kV rated modular (two modules, each with four MOSFETs) HV switch based on the design concept of the 10 kV rated modular switch using 3.3 kV rated SiC MOSFETs (new product made by GeneSiC Semi) / On hold.

(ii) Design and develop a 20 kV rated modular gate driver based on a WPT based planar transformer topology to ensure adequate galvanic isolation (~30–40 kV) for the power supplies of the gate driver / Ongoing.

3.1.3 Progress Made Since Last Report

A new 10 kV gate driver board with radically modified design was fabricated and tested in September 2021. A new optical fiber link and driver circuit has been used and bigger spacing between transmitter and receiver has been introduced to enhance breakdown voltage.

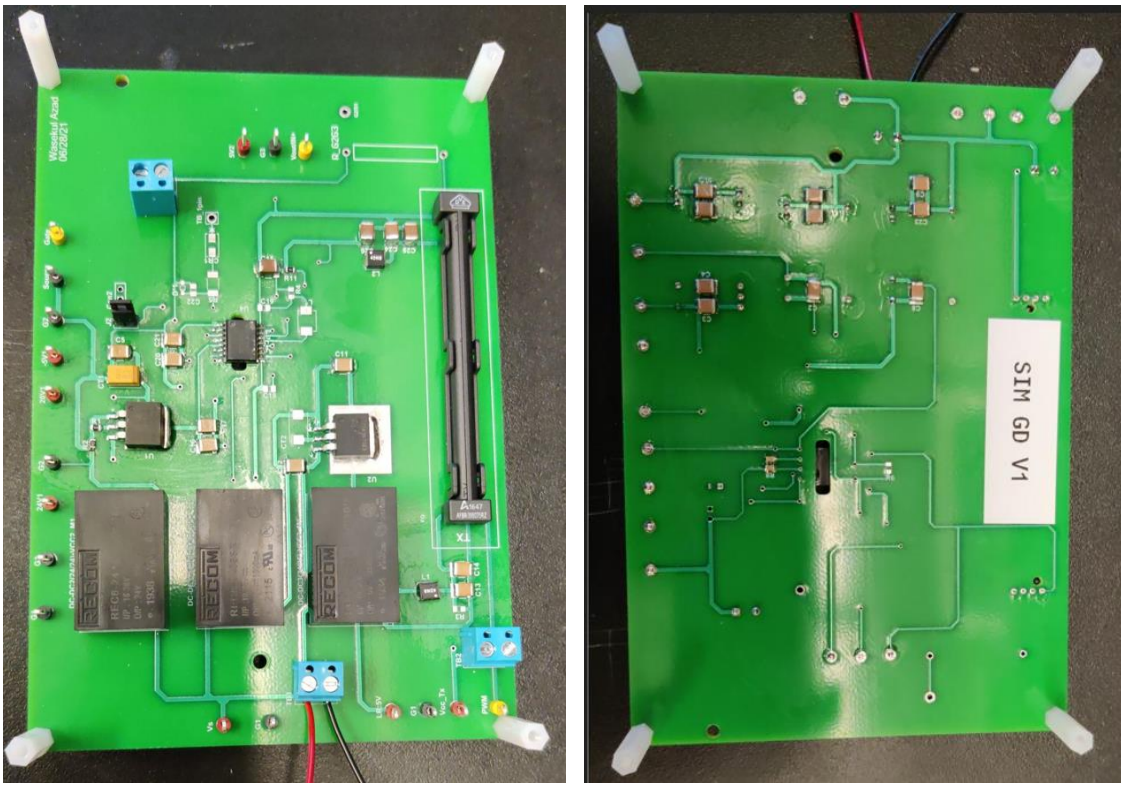


Figure 3.1. 1 Actual photograph of the modified gate driver circuit showing the integrated optical link (TX) on the left figure.

3.1.4 Technical Results

The new board has the following +5V, -5V,24V,20V buses, and they all were tested stable and within tolerance. Total input current = 100mA. The signal integrity and rise/fall behavior of the new driver board are shown in Figures 3.1.2 and 3.1.3.

(A)

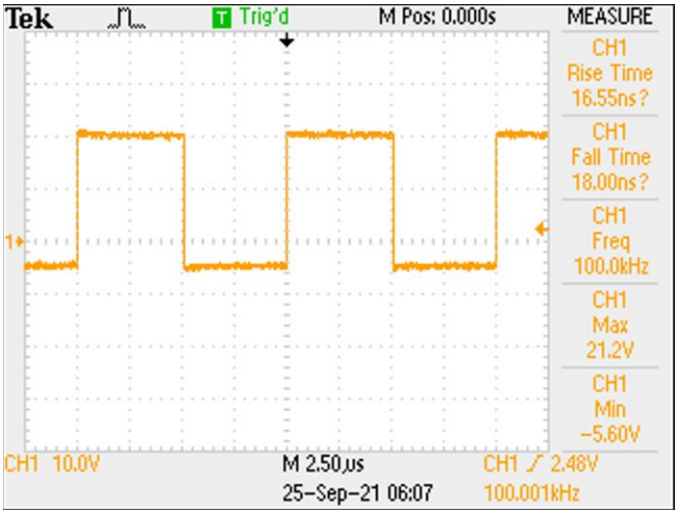


Figure 3.1. 2. Modified gate driver output at f = 100 kHz, D = 50%, no load

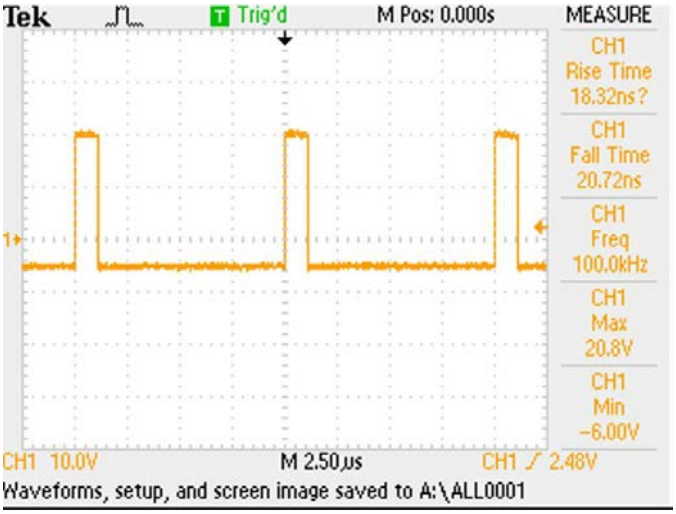


Figure 3.1. 3 Modified gate driver output at f = 100 kHz, D = 10%, no load

3.1.5 Summary of Significant Findings and Mission Impact

(A) The 6.8 kV rated four-stage surface-mount MOSFET developed in-house was successfully tested up to a DC supply voltage of 4 kV and at a switching frequency up to 20 kHz with a 3.2 kΩ resistive load.

(B) A modular (two modules) 10 kV rated HV switch has been designed and a prototype has been developed using 1.7 kV rated SMD MOSFETs (C2M1000170J). An in-house 10 kV rated HV gate driver has been designed and incorporated with the HV

switch to drive it. A manuscript on the HV switch and the custom isolated gate driver has been submitted to IEEE Transaction on Power Electronics.

(C) The HV switch coupled with the modified custom HV gate driver has been tested at a supply voltage up to 200 V just to observe the driver current and voltage balancing. The operation of the new driver architecture has been verified in LTSpice simulation platform as well.

4.0 Laser Development

4.1 Fiber Lasers and Optical Amplifiers

(Scott Shepard)

4.1.1 Problem Statement, Approach, and Context

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS (photoconductive semiconductor switch) embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$100K to \$300K to drive our Si-PCSS applications.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution (with respect to traditional fiber and traditional free-space laser designs). Moreover, our novel optical amplifier tubes, might operate at far higher power levels (over 1000 times greater), thus driving an entire array of PCSS with a single amplifier and thereby reducing the overall system costs and eliminating the optical pulse-to-pulse jitter constraints.

Sub-Problem (1): Optical pump power system costs account for over 50% of the budget for each laser (in this class, for normal/free-space, optical fiber, and tubular embodiments).

Sub-Problem (2): Fiber (as well as power tube) optical amplifier performance is degraded primarily by amplified spontaneous emission (ASE) noise, which limits the operating power point, and by nonlinearities, which distort the optical pulse shapes.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive for the PCSS applications until reduced by a factor of at least two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping technique (wherein we pump at a lower level over a longer time) which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments, we are pursuing the use of gain saturation and a staged design of different fiber diameters. We also apply these techniques to fiber amplifiers which incorporate our power amplifier tube in the final stage. The inclusion of our novel tubular-core power amplifier stage should permit a single laser to trigger an array of several PCSS (reducing system cost and mitigating timing jitter).

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system enables PCSS systems for viable deployment via: a factor of 40 in pumping cost reduction of each laser; and a factor of *N* in system cost reductions as a single laser could drive *N* (at least 12) PCSS in an array, while also eliminating the optical jitter constraints.

Risks, Payoffs, and Challenges: Optically pumping outside the laser pulse burst time can enhance the ASE; pump costs could be reduced by 40, but ASE in the presence of dispersion and/or nonlinearities could enhance timing jitter thereby limiting steerability. The main challenge for power tube implementation is the entrance optics design.

4.1.2 Tasks and Milestones / Timeline / Status

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Ongoing.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Ongoing.

(E) Demonstrate a cost-reduced fiber laser. / Ongoing.

(E1) **March 2021** Finalize design. / Complete.
(E2) **April 2021** Assemble and test-check seed LD (laser diode)/driver. / Completed.
(E3) **April 2021** Measure power vs current transfer function of seed LD/driver. / Completed.
(E4) **May–July 2021** Measure ASE and jitter of 1064 nm seed LD/driver. / Completed.
(E5) **May–July 2021** Measure ASE and jitter of 1030 nm seed LD/driver. / Completed.
(E6) **June–July 2021** Assemble and test-check pump LDs/drivers. / Completed.
(E7) **June–July 2021** Measure power vs current transfer function of pump LDs/drivers. / Completed.
/ (E8) – (E14) Delayed due to vendor issues (see MAY MSR).
(E8) **September 2021** Splice power combiners to Yb doped preamp fiber. /Completed.
(E9) **September 2021** Connect seed and pumps to power combiners and test-check. /Completed.
(E10) **September–October 2021** Measure gain, ASE and jitter of 1064 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle.
(E11) **September–October 2021** Measure gain, ASE and jitter of 1030 nm preamp assembly (forward, backward and bidirectional pumping) as a function of pump power and duty cycle.
(E12) **November 2021** Splice power amplifier and its power combiner to best preamp.
(E13) **November–December 2021** Measure gain, ASE and jitter of entire amp assembly.
(E14) **December 2021** Analyze data and document.

(F) Design a new type of higher power, tubular core, fiber amplifier. / Ongoing.

(F1) Apply one high-power tubular amplifier to a system comprised of an array of several (say N) PCSS. For example: N=12 in a 3x4 array (or 4x4 array with corners omitted) N=16 in a 4x4 array, etc.; thereby eliminating jitter constraints and reducing laser system cost by more than a factor of 100 (independent of burst profile). / Ongoing.

4.1.3 Progress Made Since Last Report

(E8–E9) Power combiners of fiber patch cords with connectors on one end and bare fiber on the other have been fabricated and spliced to the Yb-doped fiber amplifier by our collaborating vendor (3SAE). We decided to utilize connectors for a variety of reasons including: flexible replacement in the event of damaged pump laser diodes; and the fact that we can achieve sufficient power levels (3 W per each of 4 fiber pigtailed pumps, CW). Damage in fiber amplifiers is rarely in the fiber itself but more likely at any air-to-glass interface (such as within the small air gap within a fiber connector) since reflections at such increase the field strength. To mitigate such damaging effects we utilize an index matching gel (carefully injected onto the fiber end face before insertion into a connector.

(F) In cylindrical or rectangular core waveguides, self-focusing (due to the intensity dependent refractive index of glass) will refract energy out of the waveguide so that the operating power of the waveguide is limited. In a tubular core geometry, however: 1) this energy is preferentially refracted into the inside of the tube – due to symmetry breaking and 2) this energy can be coupled back into a guided mode; thereby permitting a much higher power operating point (tens of GW rather than tens of MW). The nonlinearity involved in the dynamics of the simple structure permits a surprisingly wide variety of behavior. For example, we find that roughly half of the total waveguide's power is carried in the hollow-air/core (while the other half remains in the glass-wall/cladding) until a break-point power is exceeded; after which the air core mode drops in power. The uniformity of the air core mode varies in a less predictable way, as described in 4.1.4.

(F) Our DEPS 2012 DE Systems Symposium abstract: Tubular Core Optical Power Amplifier, S. Shepard and A. Caruso was accepted for poster presentation.

(F1) Uniformly splitting a large cross-sectional area of very high power from one tubular amplifier into several power-delivery fibers (one or more for each PCSS) would eliminate the optical pulse timing jitter constraint. Note, in this way the problem could be removed entirely, since each power delivery path is passive. The main challenge for power tube implementation is the entrance optics design. To that end we consider the possibility of simply illuminating the tube with a finite number of "spots" (e.g., 1 or 2 or 4) which could be passively split from a single source (e.g., a seed laser with an optical fiber pre-amp). We find that the break-point power (i.e., the operating point at which roughly half the tubular amplifier's energy is in air) increases with the number of spots and with spot size. The later point supports the argument that a thinner wall should reduce the lensing effect, as described in 4.1.4.

4.1.4 Technical Results

(E8–E9) The power combiner is comprised of a tube around 6 pump fibers which encircle 1 seed/signal fiber; which is then tapered from a 740 micron outer-diameter down to a 240 micron outer-diameter, and then fusion spliced onto the input of 8 meters of Yb doped fiber as shown in Fig. 4.1.1. The combiner is encased in an aluminum block. Not all of the 6 pump fibers will be used initially but the hexagonal shape ensures structural integrity during the tapering process.

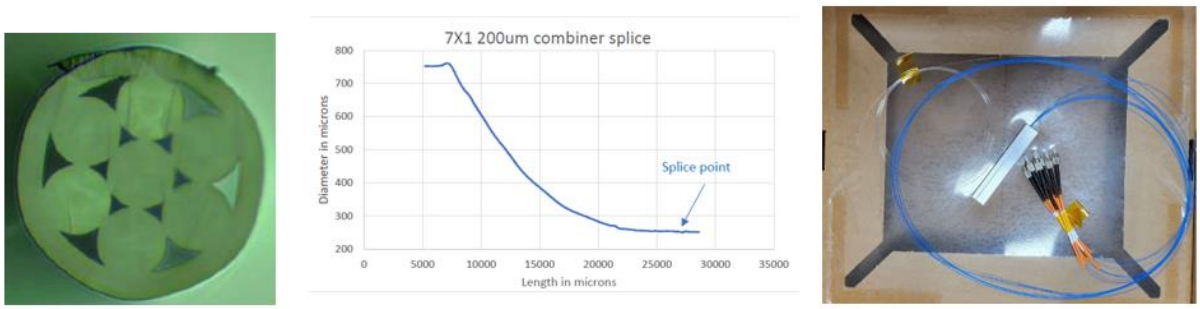


Fig. 4.1.1 Power combiner cross-section; taper dimensions; and final packaging.

In addition to the use of an index matching gel to prevent damage in the connectors an optoisolator further protects our one lower-power seed LD (at 1064 nm) but we don't utilize these for our higher-power pump laser diodes (at 915 nm) because initially we run these below one third of their maximum power (i.e., at 3 W instead of 10 W). Such power levels suffice for the initial objective – a proof-of-concept of the cost-reducing pre-burst pumping scheme. Operation at their maximum power of 10 W each will be reserved for use in other experiments (in which the purchase of more optoisolators is warranted).

(F1) In an attempt to simplify the entrance-optics design for the optical power tube we consider passively splitting (via e.g., a beam splitter such as a microscope slide) a single source into a finite number of "spots" (e.g., 1 or 2 or 4) to illuminate the wall of the tube. As shown in Fig. 4.1.2 for the case of 4 spots arranged with radial polarization (electric field vector pointing outwards from center) the uniformity of the air-core mode at the output varies considerably with the operating power of the amplifier, Pclad.

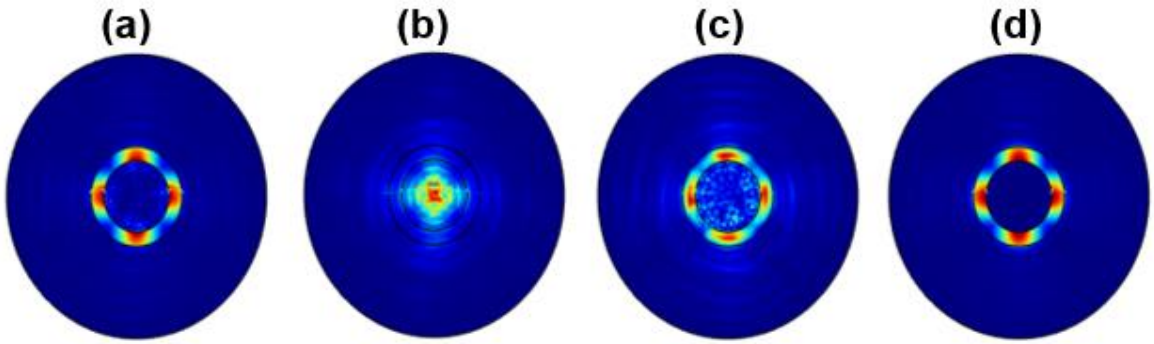


Fig. 4.1.2 Four radial polarized spots on tube at: (a) input; (b) output with Pclad = 0.235 GW; (c) output with Pclad = 2.35 GW; and (d) output with Pclad = 23.5 GW.

In Fig. 4.1.2 (b) we see an almost Gaussian distribution in contrast to the speckled pattern of Fig. 4.1.2 (c) and the virtual absence of an air-core mode in Fig. 4.1.2 (d). In the case of illumination from 1 or 2 spots the uniformity is further diminished (as anticipated) and further studies will include spots of various phase shift and polarization combinations.

The total amount of power in the air-core mode is more predictable and asymptotic to lines exemplified in Fig. 4.1.3 where roughly one-third of the total waveguide's power is carried in the hollow-air/core (while the other two-thirds remains in the amplifying glass-wall/cladding) until a break-point power is exceeded; after which the air-core mode drops in power.

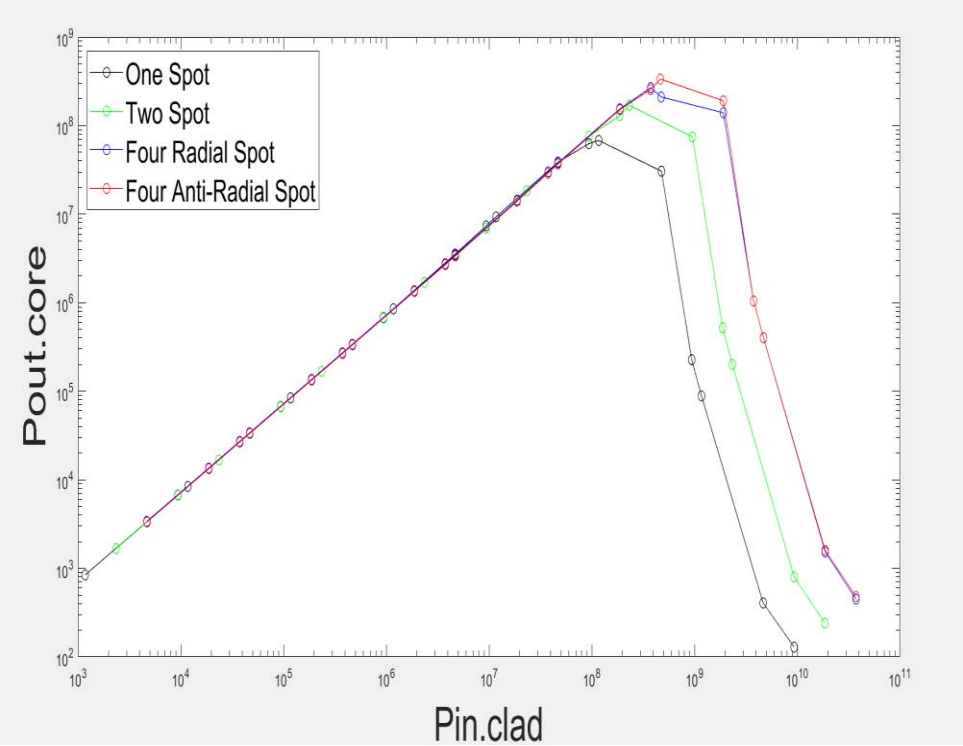


Fig. 4.1.3. Air-core power [Watts] vs operating power [Watts] for a various number of spots.

In Fig. 4.1.3 we see that we need a larger number of spots to achieve a higher operating power if we wish for roughly 1/3rd of that power to exist in the air-core mode. Radial vs anti-radial refers to the electric field lines pointing outward vs inward at the input plane (which made little difference, except at the break-point).

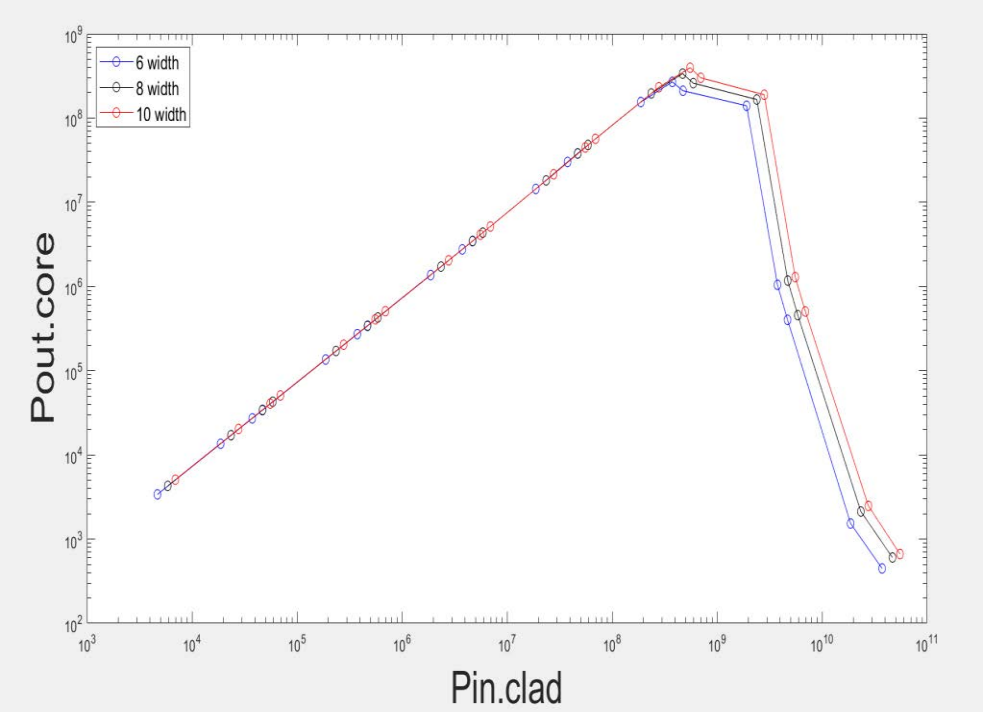


Fig. 4.1.4. Air-core power [Watts] vs operating power [Watts] for various spot size.

In Fig. 4.1.4 we see similar asymptotes in the same transfer function for a variety of beam spot sizes as characterized by the parameter, $width = 2\pi r^2$, in square microns, where r is the Gaussian beam waist in microns. The width parameter in Fig. 4.1.3 was 8 and the number of spots in Fig. 4.1.4 is 4 (radial polarization). The thickness of the tube wall in both figures was 2 microns. The effect of a larger beam width is seen to be similar to the use of a thinner wall (as anticipated).

Identifying these effects empowers the design by creating options. For example, the ratio of air-core to glass-cladding power can be set by choosing an operating point beyond the break-point and this can help optimize the uniformity of the passive power splitting at the output. Fig. 4.1.5 illustrates this point for the case of driving N=12 PCSS. We could drive each switch with 3 passive fibers via a 37 fiber splitter (as appropriate below the break-point) or drive each of the 12 with a single fiber, from the periphery of a 19 fiber hexagon (in case of negligible air-core mode power).

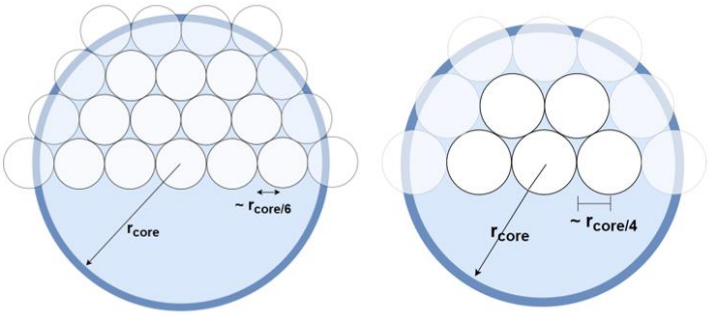


Fig. 4.1.5. Splitting a tubular amplifier output into 37 (left) vs 19 (right) passive power-delivery fibers.

4.1.5 Summary of Significant Findings and Mission Impact

(A) Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with pre-burst ASE power levels below the heating level tolerance of 100 μW. UMKC invention disclosure filed 02JUN2020.

(B) For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our heating level spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000. UMKC invention disclosure filed 14SEP2020.

(C) Achieved initial practical device designs that exploit gain saturation, which remained below damage thresholds, via staged designs of different mode diameters NOV2020.

(D) Models of the impact of ASE on timing jitter in the presence of dispersion and/or nonlinearities were established JUL2020.

(E) The design of a proof-of-concept experiment demonstrating a cost-reduced optical pumping scheme was finalized MAR2021.

(F) We made (to our knowledge) the first observation of self-focusing effects that are not determined by beam power alone. We found instead that these can also be controlled via the geometric factors within a waveguide (such as fiber core diameter) MAY2021.

We additionally made (to our knowledge) the first observation that a mode exists in the air within a simple glass tube into which we can couple energy from the mode in the glass. Thus, an amplifier (in the doped and pumped glass) can operate at higher powers JUNE2021.

We found conditions under which 0.25 GW of power can exist in the tube's air-core mode when its glass-cladding mode is at a power level near 0.5 GW JULY2021.

Advancements in the very high-power operating point (tens of GW) of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) were shown to permit a single laser to trigger an array of several (up to 100) Si-PCSS – reducing the laser system cost and eliminating the optical timing jitter constraint. The symmetry breaking of the scattering from self-focusing in a curved waveguide was shown to enable such AUG2021.

4.2 WBG-PCSS Enabled Laser Diode Array Driver

(John Bhamidipati)

4.2.1 Problem Statement, Approach, and Context

Primary Problem: Need for heavy (~125 lbs.), bulky (~10 cu-ft), and expensive (~$120,000) conventional laser systems (1064 nm) in PCSS-based HPM applications, with an additional need for second and third harmonic generation (SHG/THG) optics to trigger wide bandgap (WBG) solids (GaN/SiC).

Solution Space: Design and implement a compact (~1.1 cu-ft), lightweight (10–15 lbs.), and inexpensive (<$15,000) alternative for conventional high average power optical trigger (laser) system to improve SWaP-C^2 index of HPM systems.

Sub-Problem: Unavailability of commercial-off-the-shelf (COTS) miniature optical sources with sub-nanosecond pulse widths and tens-of-μm beam width, delivering >1-Watt power to implement as a makeshift/turnkey solution for the laser system.

State-of-the-Art (SOTA): High average power picosecond pulsed lasers available up to 50 W output power with a gain factor up to 40 dB (~10,000x power) with laser amplifier.

Deficiency in the SOTA: High average power 1064-nm pulsed lasers are bulky and require auxiliary systems as well as additional optics for SHG/THG generation for WBG device triggering.

Solution Proposed: Multi-stage laser diode array/stack (LDA/LDS) driver powered by seed-laser-diode-driven avalanche WBG-PCSS as a compact, inexpensive laser replacement.

Relevance to OSPRES Grant Objective: Provides an enhanced SWaP-C^2 compliant solution for the laser (optical trigger) subsystem, with a subsequent impact on overall HPM system cost, volume, and power (optical and electrical) requirements.

Risks, Payoffs, and Challenges: Complex interconnect and thermal management system (TMS) design at high temperature (130–175°C) operation; unavailability of COTS high power pulsed laser diodes could potentially raise a need for research in laser diodes (arrays).

4.2.2 Tasks and Milestones / Timeline / Status

(A) Complete initial feasibility study for the cascaded multi-stage optical amplifier design and determine functional requirements for the laser diodes (arrays) and source driver [DEC–JAN 2020 / completed].

(B) Complete initial stage experimental implementation of the PCSS-based driver and demonstrate positive current gain using GaN-PCSS, triggered with a 404 nm laser diode. [SEP–OCT 2021 / in progress].

(C) In addition to (B), investigate potential alternatives to GaN-PCSS in both PCSS and non-PCSS domains. [SEP–OCT 2021 / in progress].

(D) Define performance metrics for PCSS-based driver and complete numerical calculations for required output current at each stage and corresponding PCSS (GaN/GaAs) operating voltages in light of electric fields required for lock-on/avalanche mode, establish real-time implementation timeline, cost estimates, jitter limitation, and explore ways to protect LDA from PCSS ringing. [MAR 2021 / partially complete / revisit after completing (B)].

(E) Demonstrate a SiC-MOSFET-powered frozen wave generator (FWG) prototype on a custom-built PCB with Cree/Wolfspeed MOSFET(s), and 50 Ω coaxial cables and/or microstrip transmission lines capable of generating chirped pulse widths. [JUL–AUG 2021 / complete]

(F) Demonstrate a MOSFET-enabled motorized FWG on a 4″ × 5″ PCB to enable dynamic pulse width tunability using lumped-element-based transmission lines [SEP–OCT 2021]

(G) Proof of concept testing of the two-stage PCSS-enabled driver system with a 50 Ω load at 1 kHz pulse repetition rate (PRR) [OCT–NOV 2021]

(H) Working prototype demonstration at ~MHz PRR with laser diode array/stack and ancillary optics based on HPM source driver needs including thermal management system (TMS). [NOV–DEC 2021]

4.2.3 Progress Made Since Last Report

(F) To overcome the parasitic issues with 8-segment lumped-element based FWG prototype reported last month, an updated PCB with dimensions of 2.3″×3.5″ has been designed and was tested under balanced (50 Ω & 50 Ω) and unbalanced load (50 Ω & 0.1 Ω) configurations. Experimental results for unbalanced load configuration deviated from the simulation results at charge voltages >50V, potentially caused by parasitics/EMI along the reflected path.

4.2.4 Technical Results

(F) An 8-segment FWG with LC ladder network-based transmission line segments was designed and tested under balanced and unbalanced load configurations. The lumped elements were selected such that a 50-Ω characteristic impedance is maintained in each transmission line section. LC ladder networks were tuned to generate ~12-ns and ~21-ns delay along the segments 1-4-5-8 and 2-3-6-7, respectively. While the experimental results with balanced 50 Ω load configuration were found to be in agreement with the simulated results upto 150 V charge voltage with ~50% power transfer, unbalanced load configuration (50 Ω and 0.1 Ω) test results agreed with simulations only up to 50 V charge voltage. At voltages >50 V, negative train of pulses overlapped with each other to form a single pulse with ~200-ns pulse width. Parasitic(s) along the reflected path could have potentially caused a delay in the LC segment discharge that led to the pulse overlap. This effect will be studied and mitigated in the next reporting cycle along with tunable LC section implementation. The second iteration of lumped-element-based FWG prototype is shown in *Figure 4.2.1*.

Figure 4.2.1: Lumped-element-based 8-segment FWG prototype

4.2.5 Summary of Significant Findings and Mission Impact

(A) The state-of-the-art COTS laser driver specifications and limitations have been comprehensively studied, and target performance metrics have been determined in terms of output current (>120-A), pulse repetition rate (>1-MHz), transient response (<200-ps risetime and <1-ns pulse width), and volume (<0.75 cu-ft). A preliminary feasibility study has signified the need for lock-on conduction mode with ~$10^{2.6}$ gain factor to drive at >1-MHz pulse repetition rate while limiting the amplification stages to 2. This reduces monetary costs to 10–12% of the conventional laser system, while achieving the expected goal of miniaturizing the optical subsystem by 90%.

(B) Pulse trigger requirements for the LDA/LDS have been identified based on Jenoptik's actively cooled quasi continuous wave vertical diode laser stacks to tailor the device parameters of the enabling switch accordingly.

(C) Silicon optodiodes have been evaluated against the identified performance metrics for the enabling switch. The testing was performed at 200 V charge voltage with laser illumination energies between 20-µJ and 200-µJ. The device performance at low optical energies (~20-µJ) did not satisfy the expected metrics in terms of R_{on} and t_{rise}. Alternative switch technologies like avalanche transistors and silicon avalanche shapers will be evaluated in the next report cycle.

(D) Numerical calculations have been completed to estimate the electric fields and corresponding voltage bias required to induce lock-on operation while exploring ways to minimize the potential risks of high jitter at ~MHz order PRR switching, power reflections due to impedance mismatch, and negative ringing currents during PCSS recovery. Expected on-state resistance and power dissipation for 50 µm and 100 µm devices in lock-on conduction mode have been calculated to estimate cooling system requirements while retaining the expected SWaP-C^2 factor.

(E) A MOSFET-switched FWG prototype implementing coaxial transmission lines has been fabricated and tested with a goal to demonstrate a tunable pulse generator capable of demonstrating chirped pulse-widths. The primary operation of a FWG has been demonstrated with up to 8 transmission line segments under balanced and

unbalanced load configurations. The experimental implementation results on pulse chirp were found to be in agreement with the simulation results. However, pulse overlap, and deconstructive interference were observed in the 8-segment configuration, which will be addressed using a different transmission line topology/configuration.

(F) Tunable lumped-element-based (LC) ladder networks were considered a potential alternative to overcome the non-ideal characteristics of coaxial lines in terms of size and weight. This also provides an advantage of integrating the transmission lines into the PCB, minimizing the distance between the switch (MOSFET) and charged lines. An 8-segment FWG was implemented with LC ladder networks as lumped-element-based delay lines instead of the coaxial cables. Multiples of 75-nH and 30-pF were used in the LC ladder networks to induce 12-ns and 21-ns delays. A 150-V 8-segment tunable FWG has been demonstrated on a 2.3″ × 3.5″ PCB under balanced and unbalanced load conditions. Negative pulse train reflected from the 0.1 Ω load appeared to overlap with each other at high voltages, resulting in a sing ~200 ps FWHM pulse. This overlap could be due to the charge/discharge cycles of the parasitic(s) along the signal path that result in delays and leading to pulse overlap. This issue will be addressed in the next report cycle along with the implementation of a motorized FWG prototype to facilitate dynamic pulse width tuning.

4.2.6 References

[1] J. Y. Tsao, S. Chowdhury, M. A. Hollis, D. Jena, N. M. Johnson, K. A. Jones, R. J. Kaplar, et al. 2018. “Ultrawide-Bandgap Semiconductors: Research Opportunities and Challenges.” *Advanced Electronic Materials* 4 (1): 1–49. https://doi.org/10.1002/aelm.201600501.

[2] E. A. Hirsch *et al*., "High-Gain Persistent Nonlinear Conductivity in High-Voltage Gallium Nitride Photoconductive Switches," *2018 IEEE International Power Modulator and High Voltage Conference (IPMHVC)*, 2018, pp. 45-50, doi: 10.1109/IPMHVC.2018.8936660.

[3] C. V. Reddy, K. Balakrishnan, H. Okumura, *and* S. Yoshida , "The origin of persistent photoconductivity and its relationship with yellow luminescence in molecular beam epitaxy grown undoped GaN" , Applied Physics Letters 73 , 244-246 (1998) https://doi-org.proxy.library.umkc.edu/10.1063/1.1

[4] M. Zhang, R. Yang, N. Liu, and X. Wang, “Persistent photoconductivity in neutron irradiated GaN”, Journal of Semiconductors 34, Vol 9, doi: 10.1088/1674-4926/34/9/093005

[5] S. Best, M. F. Rose, Z. Shotts, M. Rader and L. L. Altgilbers, "Frozen Wave Generator technology as a source of constant amplitude high power high frequency radio frequency pulses," *2013 19th IEEE Pulsed Power Conference (PPC)*, 2013, pp. 1-6, doi: 10.1109/PPC.2013.6627507

[6] M. L. Forcier, M. F. Rose, L. F. Rinehart, and R. J. Gripshover, “Frozen-Wave Hertzian generators - Theory and applications”, in 2nd International Pulsed Power Conference, 1979, pp. 221–225.

5.0 Photoconductive Switch Innovation

5.1 Characterizing and Optimizing On-State Resistance in GaN:X PCSS

(Heather Thompson)

5.1.1 Problem Statement, Approach, and Context

Primary Problem: Traditionally, RF generation using photoconductive semiconductor switches (PCSS) have relied on materials such as silicon (Si) or gallium arsenide (GaAs), due to their availability and low cost; however, as these applications begin to require higher operating frequencies, powers, and temperatures, with the same or reduced system form-factor, the theoretical operating limits of these materials are being reached.

Solution Space: By exploiting the 3.4 eV bandgap, 1000 cm^2/Vs electron mobility, and thermal properties of GaN, it is possible to realize pulsed-power applications requiring up to a 5 MV/cm critical field, high-frequency operation, and ~400 °C operating temperature, respectively.

Sub-Problem 1: One of the most important problems in minimizing conduction losses, maximizing efficiency, and reducing thermal issues in compensated, semi-insulating GaN:X (i.e., GaN:X with X=C, Fe…) PCSS-based systems is achieving <1 Ω on-state resistance by optimizing the modifiable parameters of GaN:X at the material, device, and system levels.

***Sub-Problem 2*:** Due to a lack of maturity in the manufacturing and commercial availability of GaN:X PCSSs, there is limited knowledge available about how to minimize the on-state resistance in these devices while still maintaining quick switch turn-off time and low turn-off losses, leading to the need for a parametric study of on-state resistance.

***State-of-the-Art (SOTA*):** PCSS-based RF generation systems using Si, SiC, or GaAs can achieve MW-range output power, ones-of-gigawatts frequency content, and electrical efficiency of ~60%.

***Deficiency in the SOTA*:** Si-, SiC-, and GaAs-based PCSS require ones-of-mJ of incident laser energy to achieve <1 Ω on-state resistance, leading to increased incident laser requirements, increased heating in devices, and devices that are ones-of-cm^2 in area for the peak power and operating temperatures needed.

***Solution Proposed*:** Use simulation and available experimental results, from literature and collected results at UMKC, to optimize the variable parameters of GaN:X PCSS to achieve <1 Ω on-state resistance while maintaining a quick switch turn-off time and low turn-off losses.

Risks, Payoffs, and Challenges:

***Challenges*:** The high cost of material leads to a limited number of devices available for experimental testing and analysis, requiring a majority of the optimization studies to be performed using simulation software (COMSOL and TCAD).

***Risks*:** Simulation results may vary from experimental results for certain PCSS parameters due to the need for an encapsulating material to prevent surface flashover in

lateral GaN:X PCSS devices during high-voltage experimental testing, which may need to be accounted for.

***Payoffs*:** By minimizing the conduction losses in GaN PCSS, a compact, tunable RF source can be realized with increased efficiency and SWAP-C^2 capabilities.

5.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Determine material, device, and system parameters that affect on-state resistance and which of these can be best leveraged to reduce on-state losses and heating [*Estimated completion by OCT 21*].

1. Task – Literature study of photoelectric on-state resistance to understand how this parameter can be optimized to reduce conduction and on-state losses during PCSS operation *[SEPT–OCT21].*
2. Task – Literature review of on-state resistance studies performed using GaN-based photoelectric devices to determine areas to further study *[SEPT–OCT21].*
3. Task – Determine project milestones, tasks, and timeline for optimizing on-state resistance in GaN PCSS *[OCT21]*.

(B) Milestone – Build model of GaN PCSS in TCAD and/or COMSOL to begin simulation studies *[OCT–NOV21].*

5.1.3 Progress Made Since Last Report

(A) Literature pertaining to on-state resistance in opto-electric devices, of various semiconductor materials, has been collected and is being analyzed to determine the parameters at the material, device, and system levels that affect on-state resistance.

5.1.4 Technical Results.

(A) There are several parameters (Figure 5.1.1) that affect the on-state resistance of opto-electric devices at the material (bandgap, necessary activation energy, compensation concentrations, etc.), device (geometry, illumination location, etc.), and system (incident photon source characteristics, encapsulation material, etc.) levels that can be altered to minimize on-state resistance, with certain parameters being more easily manipulated than others. By finding out which parameters most affect the on-state resistance, how they relate to one another, and which are easily changeable, this will provide a starting point for optimizing these devices.

(B) In many existing publications for optimizing PCSS devices, the authors focus mainly on vertical devices, leading to the need to determine which results from vertical device studies are valid for lateral devices and what needs to be changed to make incompatible results accurate for vertical devices by altering assumptions, equations, etc.

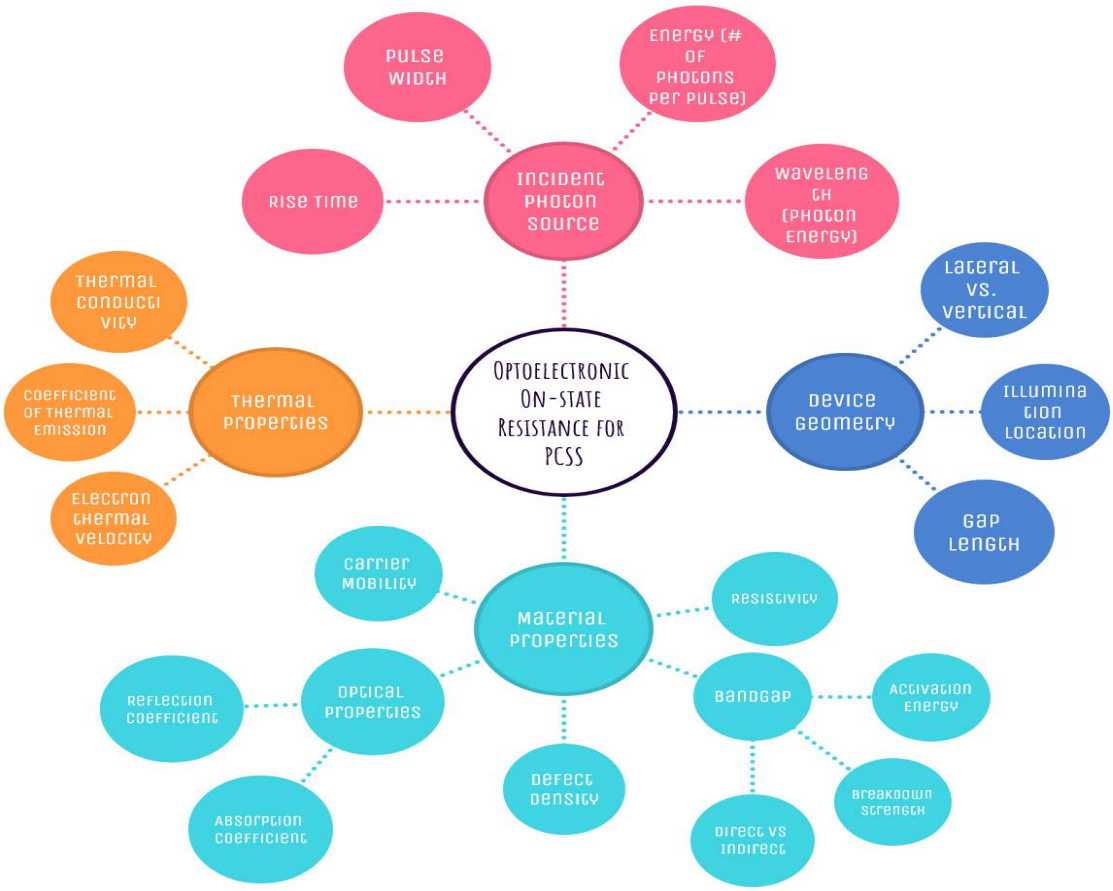


Figure 5.1.1: Chart of parameters affecting on-state resistance in PCSS, which will be iterated upon as the literature study progresses.

5.1.5 Summary of Significant Findings and Mission Impact

(A) A preliminary literature study of the on-state resistance of opto-electric devices was continued to find the parameters that affect the on-state resistance of GaN PCSS and similar devices of differing materials. This study will lead to the determination of what parameters can be manipulated to optimize on-state resistance in GaN PCSS, leading to a material option that provides increased efficiency and SWAP-C[2] capabilities of a PCSS-based RF generation system.

(B) Most publications on optimizing PCSSs focus on vertical devices, leading to a need for determining which assumptions and results for vertical devices are valid and invalid for lateral devices and adjust accordingly the ones that do not match lateral devices accordingly.

6.0 Drift-Step-Recovery-Diode-Based Source Alternatives

6.1 Drift-Step Recovery Diode and Pulse Shaping Device Optimization

6.1.1 Problem Statement, Approach, and Context

Primary Problem: Drift-step recovery diodes (DSRDs) and DSRD-based pulsed power systems are competitive with PCSS-based systems for HPM cUAS but do not require a laser. Maximizing peak power while maintaining characteristic ns-order DSRD rise times requires optimization of the DSRD device design and pulser. Other considerations are for compactness, low-jitter, cooling required, and additional pulse-sharpening device within the pulse shaping head circuit. Additional goals for pulse repetition frequency are also to be satisfied for various applications.

Solution Space: By altering DSRD device parameters (geometry, doping, irradiation), optimize single-die and stack designs for peak power and risetime within various inductive pulser circuit topologies. Also optimize the pulse sharpening device (PSD) within the pulse shaping head circuit.

Sub-Problem 1: TCAD and SPICE models of the DSRD are 40% accurate and must be improved. PSD models have not been developed.

Sub-Problem 2: Inductive pulser designs are complicated by the DSRD (and PSD) parameter variability. Use TCAD and/or SPICE models to account for variability and improve pulser design.

State-of-the-Art (SOTA): MW peak power and ns-order risetimes have been achieved in DSRD-based pulsed-power systems employing DSRD stacks for higher voltage holding and parallel lines of DSRD to increase current. PSD have sharpened DSRD pulses to 100 ps-order.

Deficiency in the SOTA: A lack of accurate TCAD and SPICE models make design of DSRD and DSRD-based inductive pulser circuit topologies (with or without PSDs) difficult to the level of tens of MW of peak power while maintaining ns-order risetime (or sharpened 100 ps-order). In addition, DSRD (and PSD) fabrication variabilities further complicate pulser design.

Solution Proposed: Develop further modeling capabilities in TCAD and SPICE for DSRD and DSRD-based inductive pulser circuit topologies to optimize DSRD and inductive pulser designs, especially for maximum peak power and minimum risetime, but also for low-jitter, reduced cooling, and compactness. Additionally, optimize pulser with PSD and pulse shaping head circuit.

Relevance to OSPRES Grant Objective: DSRD-based systems eliminate laser requirements necessary for PCSSs and are competitive in terms of thermal requirements and peak power. With sharpening, the DSRD-based systems can produce comparable risetimes. The SWaPC^2 cooling requirements of HPM cUAS systems can be solved with DSRD-based pulsed power systems, and low-jitter DSRD-based systems can be used for beam-steering in phased-arrays.

Risks, Payoffs, and Challenges: DSRD must be arrayed and staged to increase current since DSRD are limited in their ability to operate at high current densities. DSRD and PSD must also be stacked to operate at high voltages necessary for high peak power and maintain low risetimes. The stacking methods can damage dies and produce variable results in risetime and DSRD diffused doping profiles can be difficult to achieve and may require epitaxial methods. SPICE device models for DSRD are unavailable and must be developed, and questions remain about TCAD limitations for DSRD and PSD modeling.

6.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – TCAD and SPICE models of the DSRD and MOSFET, respectively, developed which match experimental values of both the diode and circuit within 5% accuracy [*Estimated completion by AUG21*].

1. Task – Develop baseline DSRD model in TCAD [*completed JAN–APR21*];
2. Task – Develop SPICE model of DSRD within LTSPICE [*Estimated completion AUG-SEP 2021*];
3. Task – Develop SPICE model of MOSFET within Silvaco [*JUL–SEP21*];
4. Task – Compare results of models developed in TCAD to the simulation values achieved using LTSPICE and experimentally (see Section 4.5) [*JUL–SEP21*];
5. Task – Incorporate parasitic capacitance, inductance, and resistance models for both single die and DSRD diode stacks (multiple dies in series) as well as for the DSRD-based pulser circuits [*discontinued after MAR–JUN21*];

(B) Milestone – Optimal characteristics of epitaxially-grown DSRD pinpointed from parametric study which produce the maximum waveform fidelity characteristics (e.g., maximum peak voltage, shortest risetime, highest dV/dt) [*Estimated completion by AUG21*].

1. Task – Determine carrier lifetime effect on risetime [*completed FEB–APR21*];
2. Task – Determine effect of including avalanche modeling on DSRD performance [*completed FEB–MAY21*];
3. Task – Determine effect of the width of outer edge contact on current density and breakdown in device [*discontinued after MAR–MAY21*];
4. Task – Model TCAD process in Silvaco Athena and Victory Process for DSRD diffused and epitaxial processes (and pulse sharpening devices) used for DSRD fabrication and DSRD device modeling [*discontinued after MAR–JUN21*];
5. Task – Determine optimal doping profile for Semiconductor Power Technologies (SPT) DSRD epitaxial designs [*completed MAY–JUL21*];
6. Task – Determine best doping profile from fabricated and optimal conceptual designs by comparing performance in the 2x2 DSRD pulser [***completed JUL21***];
7. Task – Complete DSRD performance study on epitaxial doping profile (n-side) variation manufactured by SPT in conjunction with LSRL [***completed JUL21***];

8. Task – Complete gain study for DSRD stack height and gain staging design [***completed JUL21***];
9. Task – Verify accuracy of TCAD simulations by comparing to experiment for DSRD-based pulser circuit topologies [*JUL–AUG21*];
10. Task – Perform first semiconductor opening switch (SOS) TCAD simulations for DSRD vs SOS mode of operation [SEP21];

(C) Milestone – Pulse sharpening devices developed within TCAD which improve the risetime and peak voltage of the IES pulse generator developed in Section 4.5 [***transitioned to Section 4.7 JUL21***].

1. Task – Develop preliminary pulse sharpening devices (PSD) models within TCAD [*discontinued after DEC20*];
2. Task – Develop standard PSD models within TCAD to reproduce results from published work [*discontinued APR–JUN20*];
3. Task – PSD simulated with DSRD 3-stack for more complete DSRD-based system modeling excluding only the primary switch model [*APR–JUN20*];
4. Task – Determine current carrying capacity of PSD and DSRD stacks [*discontinued MAR–JUN21*];

6.1.3 Progress Made Since Last Report

(A.2) LTSPICE DSRD Models were refined to better match standard diode tests. The standard extended Berkeley diode model within LTSPICE using the 7-diode configuration now uses the forward I-V, reverse C-V and reverse recovery to set the model parameters with the reverse I-V (excluding breakdown).

(A.4) Pulser performance using the new LTSPICE DSRD models were compared to experiment over a range of prime voltage inputs. The old LTSPICE model, the new LTSPICE model with no adjusted parameters, adjusted V_p (soft recovery parameter) and adjusted CJO are compared for peak voltage and risetime to experiment. The CJO adjusted model can fit experimentally observed risetimes, while the vp adjusted model can match risetimes up to ~4 ns. Using no adjusted parameters risetimes up to ~2 ns can be simulated. The peak voltages of individual pulses of fixed trigger duration and prime voltage input used were matchable with all the models by some adjustment but otherwise will rarely match well. The other issues are matching peak voltage and risetime over a range of trigger durations and prime voltages used, comparing DSRD models for different stack heights, and comparing the DSRD model accuracy between single bar and 2x2 and other DSRD pulser circuit topologies. The issue with the adjusted models is they no longer fit standard diode experiments in simulation. A more advanced diode model can improve the modeling capabilities along with improved standard diode tests (higher voltages and currents).

(B.10) The first semiconductor opening switch (SOS) TCAD simulations were performed in the single bar pulser used for DSRDs. A higher current density (1000 A/cm^2) fast opening SOS mode of operation with higher risetimes than seen in faster operating DSRDs was demonstrated. In remains to delineate the DSRD and SOS modes of

operation in detailed TCAD simulations and consolidate the known published experimental and theoretical results to clearly define DSRD and SOS operation. Known SOS pulser circuit topologies can also be used.

6.1.4 Technical Results

(A.2) Last month (AUG 2021 Grant Report) the new LTSPICE DSRD model was presented for standard diode tests (forward and reverse I-V, forward and reverse C-V, and reverse recovery). Work has continued in improving the DSRD LTSPICE model. First all curves were fit. The reverse I-V proves problematic fit but can be fit with adjusting the GMIN parameter but this affects all diodes and transistors in a circuit and cannot be used in pulser simulation. Some initial review of the relevant literature has not shown improved modeling of reverse I-V exists but likely methods do exist and will be collected. The forward C-V was matched for maximum forward capacitance and matching the forward bias at which the maximum capacitance occurs has yet to be completed. The forward C-V is not used in our model of the DSRD as is standard practice with the standard diode model. The transit time sets the maximum of the forward capacitance but recovery time is substituted from experiment or transit time is adjusted to fit peak voltage (while RS fixed) and to some extent risetime (with RS adjusted with transit time ~3 ns risetimes can be simulated).

The forward I-V was fit in a different method (as opposed to last month grant report). RS was not extracted from experimental curves or set first this time, but IS and N were adjusted to fit the forward I-V as closely as possible with a minimum of iterations. Next, IKF is adjusted to more closely fit the shape of the forward I-V see Figure 6.1.1.1.

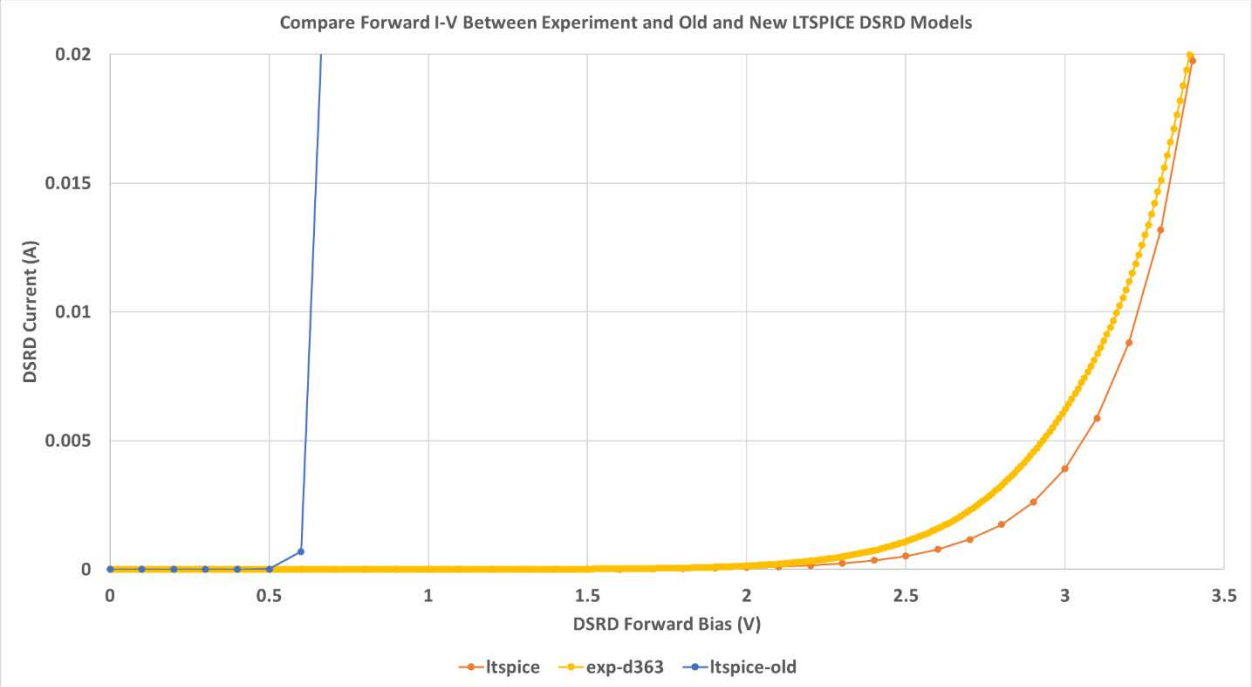


Figure 6.1.1.1. Forward I-V comparison between experiment for diode d363 and the new and old LTSPICE models.

The simulated LTSPICE curves are fit to experimental data over a narrower range of voltages and currents due to the limit of the measurement setup used. Higher voltage and current forward I-V tests allow RS to be set more accurately and cannot be adjusted with any accuracy with the current testing ranges.

The reverse C-V were set in the same method as used in the earlier reports and did not change. The zero-bias capacitance (CJO) parameter was set to experiment and grading coefficient (M) were set to fit reverse C-V curves more closely. The main difference is if CJO is used to adjust the risetime of the pulser output in LTSPICE simulation. Single bar pulser experiments have shown higher risetimes for the DSRD in our older inventory and show the variability of peak voltage and risetime in the devices. In Figure 6.1.1.2 is shown the reverse C-V for experiment, and old and new LTSPICE models. The adjustment of CJO (disregarding M) throws off the entire reverse C-V which is matched well without adjustment (not shown).

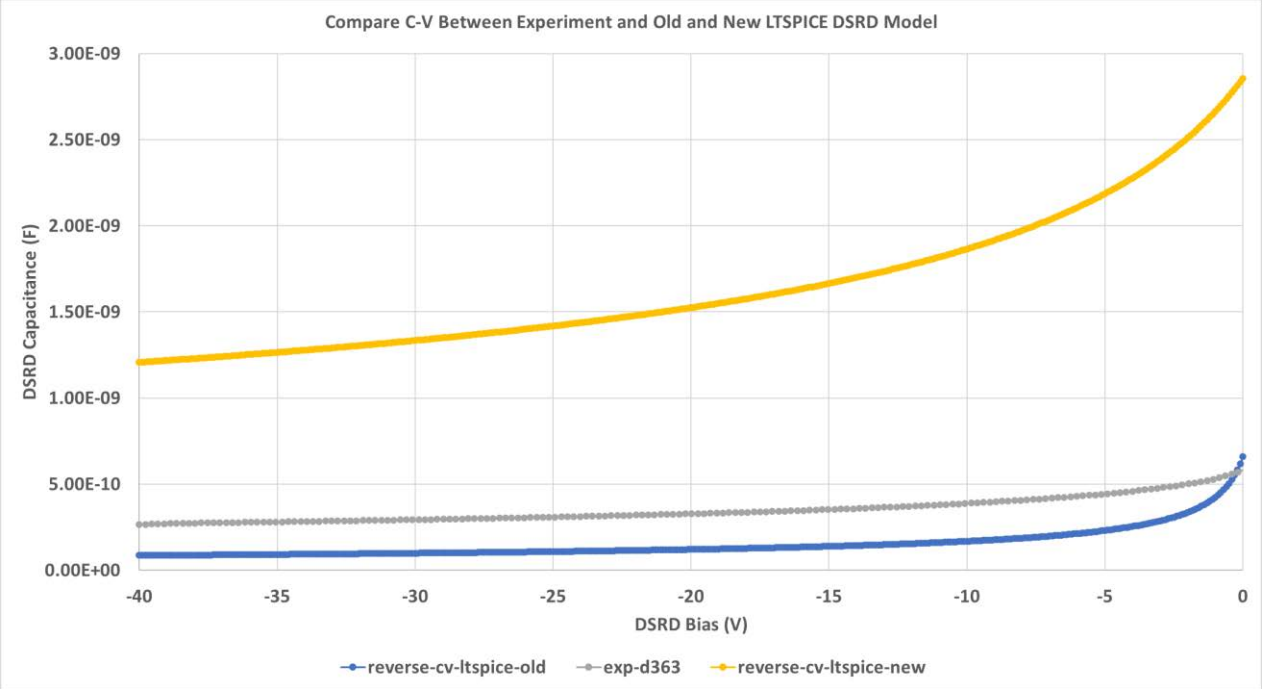


Figure 6.1.1.2. Reverse C-V comparison between experiment for diode d363 and old and new LTSPICE models.

Reverse recovery from experiment and LTSPICE were matched for the first time using the measured recovery time for the transit time in the LTSPICE DSRD model. This has been the standard practice in using the standard diode model and in our old LTSPICE model.

(A.4) The old LTSPICE DSRD model and the new, improved LTSPICE DSRD model are compared in the single bar DSRD pulser with both adjusted and non-adjusted parameters in the new model (adjusting the zero-bias capacitance CJO). The comparison is over a range of prime voltage inputs corresponding to experiments. In Figure 6.1.1.3 and Figure 6.1.1.4 are shown the peak voltages at the load and 10/90 risetime, respectively, over a range of prime voltages.

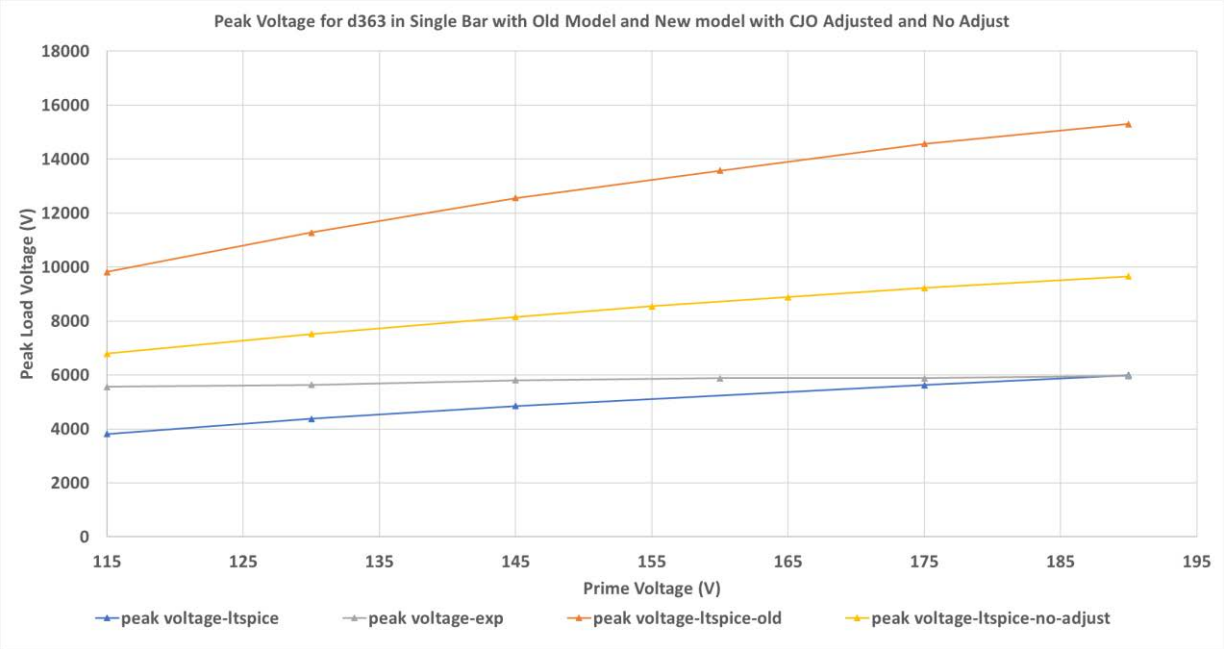


Figure 6.1.1.3. Peak voltage at load vs prime voltage input for LTSPICE models and experiment in the single bar pulser.

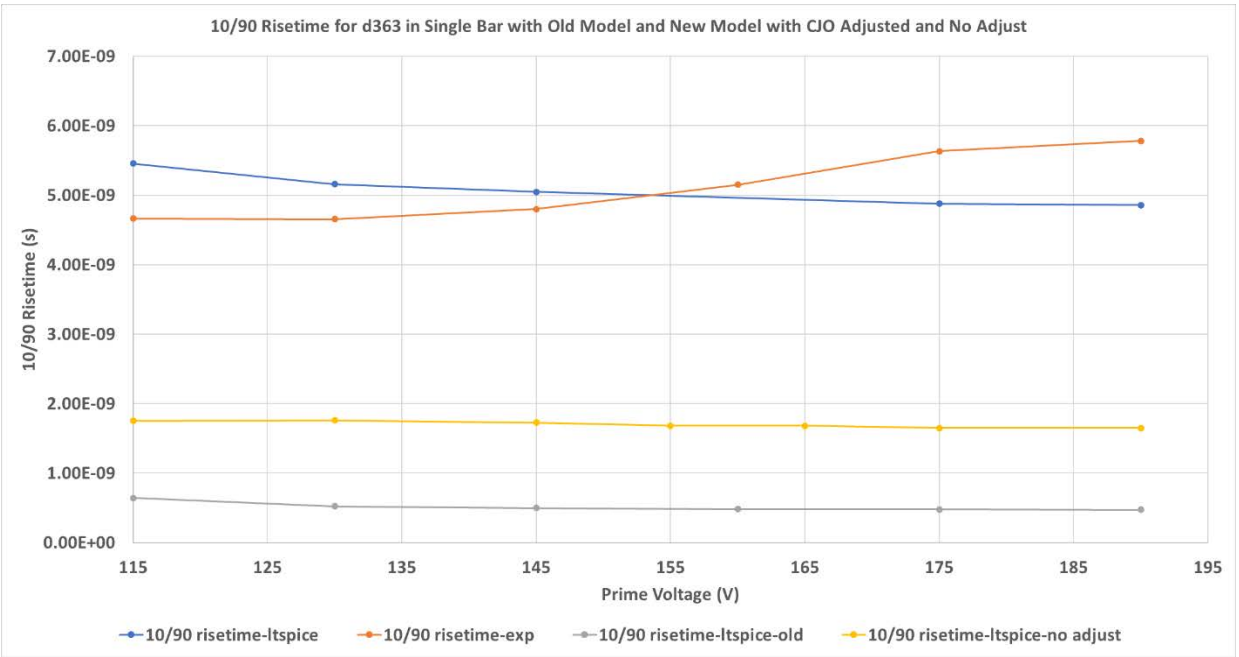


Figure 6.1.1.4. 10/90 risetime of load voltage vs prime voltage used for LTSPICE models and experiment in the single bar pulser.

The LTSPICE simulations have been performed with 340 ns trigger duration. For peak load voltage, the new LTSPICE model with adjusted CJO is the closest to experiment with no adjustments second closest and the old LTSPICE the most in error. The 10/90 risetimes are similar with the new model with adjustment matching experiment the best. The ability to adjust risetime is limited in the no adjustment models. CJO must be used to match risetimes over ~2-3 ns. The soft recovery parameter (V_p) was tested but did not allow for matching the risetimes beyond ~4 ns. For longer risetime DSRD or SOS the CJO in the current DSRD model is the only way to match risetime closely. The models can be iterated out to match more closely.

6.1.5 Summary of Significant Findings and Mission Impact

DSRD TCAD simulation started by replicating published TCAD DSRD results and then simulating devices similar with actual in-house DSRD. The variation of the sinewave pulse voltage input magnitude and period on DSRD charge storage were collected. Charge storage timing (when the diode empties charge stored from forward pulsing) of ~50% was achievable with sufficiently long voltage input period which is necessary for maximum reverse current cutoff.

DSRD stacks, as opposed to individual die DSRD, were simulated showing reduced risetime from single die to 5-stacked DSRDs consistent with published and earlier in-house data. Series resistance to model metal resistance between DSRD in stacks and doping variability in stacks was also modeled in TCAD showing metal resistance must be large to have an impact on peak voltage and risetime and that doping variations proportionally effect risetime.

(A.1) Accurate DSRD TCAD models have been developed that include both carrier-carrier scattering and Selberherr breakdown and are suitable for DSRD operation below the dynamic breakdown threshold. Peak voltage and risetime were limited by the breakdown model and more closely match experimental pulse data.

(A.2) A new DSRD LTSPICE model has been developed following the method used for developing a TCAD SPICE MOSFET model and by matching to experimental standard diode tests. The forward I-V and reverse C-V have been well matched using a 7-diode model for a 7-stack DSRD, as opposed to using only a 1-diode model for all DSRD stack heights. The reverse I-V and forward C-V are generally more problematic to fit to and proved to be so. More research and effort will be necessary to improve these matches and understand the impact on pulser simulation. The reverse recovery experiments have also been well matched and complete the matching of all the standard diode tests. Pulser performance has been difficult to assess due to the experimental data gathered thus far. The new DSRD LTSPICE model will also enable improvements in the TCAD SPICE MOSFET model. Overall, the new DSRD model represents a vast improvement over the previous model but has yet to include breakdown effects possible in the TCAD DSRD model and therefore breakdown limits of DSRD operation.

(A.3) Work on TCAD SPICE MOSFET models has been done for the primary switch model (MOSFET) with conversion of the code to TCAD SPICE being partly completed to allow for modeling the complete DSRD-based pulser system (except driver). However, the conversion to TCAD of the MOSFET primary switch model, developed by CREE, to TCAD SPICE is complicated by having to develop custom behavioral models in TCAD SPICE which would be high-risk. Instead, a published model usable in TCAD SPICE was implemented and fit to the datasheet and then tested in a DSRD pulser simulation. The new MOSFET SPICE model usable in TCAD showed improvement in not having a first output pulse peak that was higher. This higher pulse had occurred in the TCAD MOSFET model (not SPICE model) and had not occurred in the voltage-controlled resistor MOSFET model (inaccurate model). Further refinement and testing of the new MOSFET SPICE model for use in TCAD has been more closely fit with the Cree LTSPICE model and compared to the Cree datasheet. The model can also be adapted to a new MOSFET in use within current DSRD pulsers. Further fitting can still be accomplished and matching both the Cree datasheet and LTSPICE model for gate charge and switching characteristics can be completed with more research into the test circuits used which are commonly not well explained in datasheets.

(A.4) LTSPICE, TCAD and experiment have been compared for the single bar pulser using a 7-stack DSRD, however there is some discrepancy for these experiments with earlier experiments (which the LTSPICE and TCAD simulations match better with) most likely due to the variability in DSRD and some to the new DSRD switch integration used for ease of switching out DSRD of various stack heights and combinations. As more experimental data is acquired for the pulsers the comparisons with simulation will yield more useful results. The 2x2 DSRD pulsers have been compared to TCAD simulation incorporating the latest TCAD SPICE

MOSFET models showing some similarities in predicted peak voltage and risetime, but the most significant result is the matching of the experimental optimum trigger duration of 340 ns with TCAD results. LTSPICE simulationshave been performed with the new DSRD LTSPICE models and show the standard diode model used can match experimental peak voltages and risetimes but only by adjusting mainly CJO parameter. Without adjust there is considerable error in simulated results. Better diode models exist that incorporate impact ionization effects and recovery time modeling the later of which circumvents CJO adjustment. With further experiments and simulation refinement it is expected that the models will be predictive of experiment within the quality of the experimental data and models used.

(B.1) DSRD risetime performance was collected from TCAD simulations for variable carrier lifetime. Changes in lifetime had no significant effect on risetime other than the output pulse starting earlier.

(B.2) DSRD peak voltage and risetime were simulated in TCAD to include avalanche modeling or not. TCAD avalanche models limited peak voltage and risetime at the load over a range of voltage input magnitudes. A TCAD parameter study for DSRD stack height and DSRD area for several doping profiles with and without avalanche modeling was performed (Spring 2021 UMKC OSPRES Grant Review and Technical Exchange). The avalanche model and model parameters were also modified to account for dynamic breakdown rather than static and then compared to the no avalanche case and experimental data. From the improved avalanche modeling and TCAD parameter study, the optimal area of the DSRD can be obtained. However, for the 500 V voltage input magnitude used, the DSRD output were all in breakdown and are not predictive of non-breakdown behavior. Future studies for optimal area will include a range of voltage magnitudes to study DSRD performance and breakdown.

(B.4) TCAD process and device modeling for the development of process steps and their resultant doping profiles and device operation was begun. This modeling will enable a connection between the fabrication parameters and the device operation for DSRD (and PSD).

(B.5) Exponential doping profiles were shown (via TCAD) to outperform Gaussian and error function profiles slightly. Exponential profiles have an optimal minimum doping of 5×10^{13}–$1\text{x}10^{14}$ dopant atoms/cm^3, while Gaussian and error function profiles have an optimal minimum doping of 1×10^{13}-5×10^{13} dopant atoms/cm^3. Further exponential doping parameter studies were carried out in circuits A and B of Figure 4.2.1 (see JUN 2021 Grant Report) which included a broader doping parameter space for minimum doping, junction placement, basewidth and peak doping over a wider range of voltage input magnitudes (for breakdown limitations). The results are similar to before and show the optimally performing doping profile has a minimum doping of 5×10^{13}, no basewidth, junction placement of 95 µm, and peak doping of 1×10^{18} (p-side) and 1×10^{19} (n-side) dopant atoms/cm^3. A comparison was made for the optimal exponential doping profiles to optimal error function, LLNL and SPT DSRD designs within the 2x2 DSRD pulser system. The

TCAD study showed the exponential doping profile performs the best overall when considering peak voltage, risetime, voltage riserate, maximum reverse current, FWHM pulsewidth, prepulse and gain. Epitaxy designs with realistic deviations from the ideal exponential profile from the SRP data were shown in TCAD to not significantly affect the performance.

(B.7) A more complete gain study for varying prime voltage input and stack height was completed. The results show a variety of considerations must be made for determining the better stack heights to use in DSRD pulsers. The design of the pulsers can be improved when considering the gain staging in multi-staged DSRD pulsers as caused by the DSRD stack heights used. The 7- and 13-stacks showed the best gain. However, the peak voltages were best for the 13-stack while the 26-stack required unrealistic MOSFET currents to achieve its maximal peak voltage (or gain). For gain per die within a DSRD stack, 1-stacks showed the best gain per single and showed that gain 'efficiency' drops with stack height. Still, higher 7- and 13-stacks had the highest gain. How best to use this new data for DSRD pulsers is under discussion.

(B.10) First semiconductor opening switch (SOS) TCAD simulations have been performed for demonstrating a hgiher current density mode of operation. Future SOS TCAD simulations can help delineate the difference in DSRD and SOS for current density snappy recovery according to doping profile and mode of device operation.

(C.1) Pulse sharpening has been verified for PSD devices for the standard design and another non-conventional design. The PSD was also modeled within a DSRD-based pulser circuit combining for the first time TCAD modeling of both DSRD and PSD together within the same circuit with only the primary switch model not included.

(E) DSRD pulser circuits for the single-bar (Circuit B of Figure 4.2.1) and 2x2 (circuit C of Figure 4.2.1) have been simulated within TCAD allowing the use of a TCAD DSRD model, whereas in SPICE no accurate DSRD SPICE model is available. Currently, the primary switch MOSFET is modeled in TCAD, as well, but SPICE models can also be developed for the SPICE within TCAD as and will allow for better use of computational resources within TCAD. The MOSFET model and pulse repetition are being studied in detail to more closely match experiment and TCAD.

6.2 Pioneering Drift-Step Recovery Diode Processing and Manufacturing

(Alex Usenko)

6.2.1 Problem Statement, Approach, and Context

Primary Problem: DSRDs have not increased in performance due to deep diffusion manufacturing since the 60's. Their voltage-to-risetime, dV/dt remains on the order of 10^{12} V/s. To achieve the 10^{13} V/s (10 kV/ns) voltage-to-risetime required by an all-solid-state

HPM pulse generator in support of the Naval afloat mission, improving DSRD manufacturing techniques is critical.

Solution Space: Leverage applicable concepts from the mainstream silicon chipmaking industry and apply new manufacturing methods to DSRD processing.

Sub-Problem 1 – Diode silicon surface termination/passivation: The SOTA uses a diode termination by a vertical wall. This design results in low breakdown voltage as it is limited by surface breakdown. To increase the diode breakdown voltage closer to bulk silicon breakdown voltage value, DSRD side termination technique, vertical side wall design must be avoided.

Sub-Problem 2 – Stacking of DSRD dies: The SOTA is based on soldering of diode dies into a stack, which limits the stack lifetime by below 10^{12} pulses. Also, the SOTA never used opportunity to stack wafer first, then cut into dies. Switching to wafer level stacking will decrease the number of stacking operations by more than 100X.

Sub-Problem 3 – Packaging of stacked dies: *The* SOTA uses bare stacked DSRDs. Mounting the bare stack into a press-pack type package will improve long term stability, so the stack will survive much higher number of pulses before it burns out.

State-of-the-Art (SOTA): In a recently published paper (2019),[3] the Russian St. Petersburg team at the Ioffe institute reported achieving a peak current density of 5 kA/cm^2 with a rise time of the output pulse front of ~2.3 ns, and a peak voltage across the load of 900 V (i.e., the peak switching power is 4.5×10^6 W/cm^2). The St. Petersburg team utilized deep diffusion technology. A competing team at Ekaterinburg, Russia [8] reports similar pulse performance. Both teams use outdated deep diffusion technology. As one can see, there has not been any significant improvement in DSRD pulse performance since the pioneering work done in 1960 [1].

Deficiency in the SOTA: First, no DSRDs have been manufactured using epitaxy technology with doping profile optimization. Second, no DSRD processing method exists that integrates side passivation with silicon dioxide. Finally, an acceptable DSRD stacking process has yet to be developed.

Solution Proposed: Manufacture DSRDs within the continental United States using an epitaxial growth process leveraging the optimal characteristics (e.g., doping profile, carrier concentration) determined through the work performed in Section 6.1 and through working with industry partners at Semiconductor Power Technologies (SPT), Livermore Semiconductor Research Laboratories (LSRL) and Lawrence Livermore National Laboratory (LLNL – Voss Group).

Relevance to OSPRES Grant Objective: DSRD manufacturing technology is a major building block of short-pulse high-peak-power defense systems. Our new disruptive process flow for DSRDs enables not only manufacturing of DSRDs at scale, but within the continental United States (CONUS). In doing so we will redefine the SOTA by producing optimal DSRDs. Further, DSRDs will be used within best-in-class HPM pulse generators which become part of more advanced defense systems within the Navy arsenal.

Risks, Payoffs, and Challenges:

Risks: As the process of producing DSRDs using epitaxial growth with doping profile design is novel, uncharted territory, there is inherent risk to its success. Additionally, post-processing methods based on the discussions provided in the ***Sub-Problems*** section are not well-established.

Payoffs: Replacing traditional deep diffusion technology with new process integration scheme would allow better DSRD pulse performance. Electrical breakdown voltage is expected to increase, rise time on a load is expected to decrease, reliability and lifetime also expected to increase.

6.2.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Produce epitaxial DSRDs that contain optimal exponential doping profiles and carrier concentrations /estimated *DEC21*/.

1. Task – Design of experiment on 25 wafers through negotiations with vendors / *MAY–JUL21* / Completed.
2. Task – Perform DSRD stack epitaxy on 13 wafers at SVM Inc., and 25 wafers at LSRL / *JUN–AUG21* / Completed.
3. Develop process integration scheme that uses epitaxy instead of deep diffusion /estimated / *JUL–OCT21*.
4. Compare traditional DSRD technology and suggested integration scheme. List disadvantages of traditional processes and define potential advantages of new processes /estimated / MAY–NOV21.
5. Run Gen2 and Gen3 lots. Gen2 is on wafers with epi from SVM, Inc., Gen3 is on wafers with epi from LSRL. Gen2 uses the same BEOL as Gen1. Run BEOL of Gen3 – using our new patented processing scheme – Si3N4 masking, TMAH etch, oxidation, selective electroless metal deposition, wafer bonding, sawing into diode stacks / OCT–DEC21.
6. Submit Gen2 and Gen3 diode lots to UMKC team for pulsed performance measurements; collaborate with team on determining optimal doping profile through DoE analysis by Minitab software / OCT21–JAN22.

(B) Milestone – Develop diode separation technique while keeping wafer integrity /Estimated completion NOV21/;

1. Design lithography masks for short loop experiment, submit order to vendor. /MAR-APR21/; Completed.
2. Design short loop experiment for V-groove etching for diode separation. /MAR-APR21/; Completed.
3. Run short loop experiment for the diode separation by anisotropic etch, analyze results /MAY-OCT21/. Completed.
4. Design lithography masks for epi DSRD run, submit order to vendor. /estimated OCT21/.

5. Run Gen3 lot through V-groove etch step, transfer lot to next process step. /estimated NOV21/.

(C) Develop Ohmic contact deposition technique integrable with epitaxy, diode side termination/passivation, and wafer bonding steps /estimated AUG-NOV21/.

1. Design short loop experiment to determine technical feasibility of selective electroless deposition of metal stack as a method of Ohmic contact forming in the DSRD process integration scheme. /OCT21/. Completed.
2. Determine vendor from which to order electroless deposition kits; obtain quotes, order, receive the kits. [OCT21]. Completed.
3. Run short loop experiment – nickel-copper-tin stack electroless deposition on a blanket wafer. Analyze results /estimated NOV21/.
4. Develop process recipe for the metal stack deposition to use in Gen3 DSRD lot manufacturing /estimated NOV21/.
5. Run the selective metallization step on Gen3 lot, transfer the lot to next processing step. /estimated NOV21/.

(D) Develop wafer stack bonding technique integrable with the rest of Gen3 process flow /estimated SEP-NOV21/.

1. Design short loop experiment for bonding 2 blanket wafers with Ni-Cu-Sn layers by solid–liquid interdiffusion. /SEP21/. Completed.
2. Run 2-wafers short loop experiment. Analyze results. /estimated OCT-NOV21/.
3. Test technical feasibility of multiple wafer bonding by bonding 10-wafer stack. /estimated NOV21/.
4. Upon proof of technical feasibility of 10-wafer stacking, develop process recipe to use for processing of Gen3 DSRD lot /estimated NOV21/.
5. Run wafer bonding step on Gen3 lot, transfer the lot to next processing step. /estimated DEC21/.

(E) Develop wafer stack sawing technique into DSRD stacks, integrable with the rest of Gen3 process flow /estimated NOV-DEC21/.

1. Design sawing process using Disco saw available at Semiconductor Power Technologies for cutting 10-wafer stack /estimated DEC21/
2. Run short loop cutting of blanket bonded 10-wafer stack. Analyze results /estimated DEC21/.
3. Develop process recipe for Disco saw tool to use for Gen3 lot /estimated DEC21/.
4. Run sawing step on Gen3 lot [DEC21].

(F) Develop diode side passivation process integrable with the rest of DSRD process flow.

1. Test compatibility of thermal oxidation for the diode side passivation with preceding anisotropic etch step [NOV21]

2. Alternative diode side passivation process: design short loop experiment on room temperature oxidation by forming porous Si film and oxidizing the porous film [APR-OCT21]. Completed
3. Run part of Gen3 lot using the oxidized porous Si as diode side passivation.
4. Second alternative diode side passivation process: Design short loop experiment on room temperature oxide deposition from oversaturated fluorosilicic acid. [MAY-NOV21].
5. Run part of Gen3 lot using the oxidized porous Si as diode side passivation [DEC21].
6. Choose the best from 3 methods of diode side surface passivation techniques [JAN22].

(G) Develop a DSRD process based on out-diffusion (opposite to traditional in-diffusion process).

1. Process Gen4 lot based on process integration scheme described in our patent application filed in Aug. 21.

(H) Find vendor that manufactures press-pack parts, order the parts, and encapsulate the DSRD stacks into the press-packs.

6.2.3 Progress Made Since Last Report

(A4) Provisional patent application on the integration scheme filed with USPTO on Sept.17

(A5) Three vendors identified for placing an order for silicon nitride deposition on Gen3 lot: University of Louisville, Roque Valley Microdevices, and Nova Inc. Quotes were requested and obtained. An order to Nova is planned.

(A6) 1 of 13 wafers in Gen2 lot were processed. Non-stacked DSRDs were manufactured.

(A7) Non-stacked Gen2 DSRDs were submitted to the UMKC pulse performance measuring team. The team will first characterize single diodes, then characterize a “loose stack”.

(B3) Image vertexes in short-loop v-groove samples by optical microscopy and analyze them. Optimal etch mask window width was determined – 350 microns. Adjustment to the next mask design was performed.

(C2) Electroless deposition kits were purchased from Nano3D Systems for nickel, copper, and tin.

6.2.4 Technical Results

(F.2) A new approach to sidewall passivation was investigated, consisting of SiO2 with a porous silicon double layer. In this approach, porous Silicon layer is first grown on diode sidewalls at room temperature. A short loop run using blanket silicon wafers executed first. The blanket wafers are submersed in a 1000:1 mixture of concentrated HF and

HNO3. It converts silicon on wafer surface into porous silicon layer. The thickness of the porous layer achieved is about 1 micron. Then the wafers were rinsed and dried in air. During drying, the upper part of porous silicon layer oxidizes thus converts into SiO2. The bottom part of the porous layer is now sealed. Porous silicon is a semi-insulator. It forms a “bleeding” layer – film that passivates silicon surface, but not able to collect electrical charge that forms a parasitic conductive channel in silicon. As this process proven technical feasibility in the short loop run, next plan is to implement it in 3rd Gen DSRD run.

(A.1) 2nd and 3rd generation DSRD lots have been started. Both based on epitaxy (1st generation was based on old deep diffusion technology.

2nd and 3rd epitaxy ‘runs’ (i.e., manufacturing processes) ongoing. Both are at the final stage and near completing epitaxy step. 2nd run uses epi vendor SVM (Silicon Valley Microelectronics, Inc.) where doping profile used are similar to those of deep diffusion. 3rd run uses epi vendor LSRL (Lawrence Semiconductor Research Laboratory) and doping profile is best-predicted-by-simulation (exponential).

Upon receiving wafer lots from epi vendors, diode fabrication will continue for metallization, cutting into individual dies, stacking of dies, and side wall passivation. Finished DSRD stacks will be tested on static and pulse performances.

Some wafers from 2nd and 3rd generation lots will be processed using new techniques that were recently suggested: (1) side wall passivation by fluorinated SiO2 deposited at room temperature; (2) side wall passivation by staining in HF/HNO3 1:1000 mixture; (3) stacking on wafer level using SLID wafer bonding process; (4) side insulation of individual diodes by etched V-grooves and thermal oxidation.

IP disclosure and provisional patent application [10] have been filed on one of 4 new techniques. Rest 3 will be filed in next reporting period.

(F.2, F.4) Two new processes suggested for diode side wall passivation – staining, and liquid phase SiO2 deposition, both room temperature. Experimental setups for both processes have been built. Short loop runs on blanket wafers to prove technical feasibility planned. Experiment on staining in HF/HNO3 finished. Results show that near 1-micron thick SiO2 film is successfully grown. Experiment on SiO2 deposition from liquid phase is ongoing.

(B.3) Optical microscopy pictures of vertexes of v-groove etched dummy wafers are shown on Fig.6.2.6. These show that diode corners will have shape slightly different from a simple square.

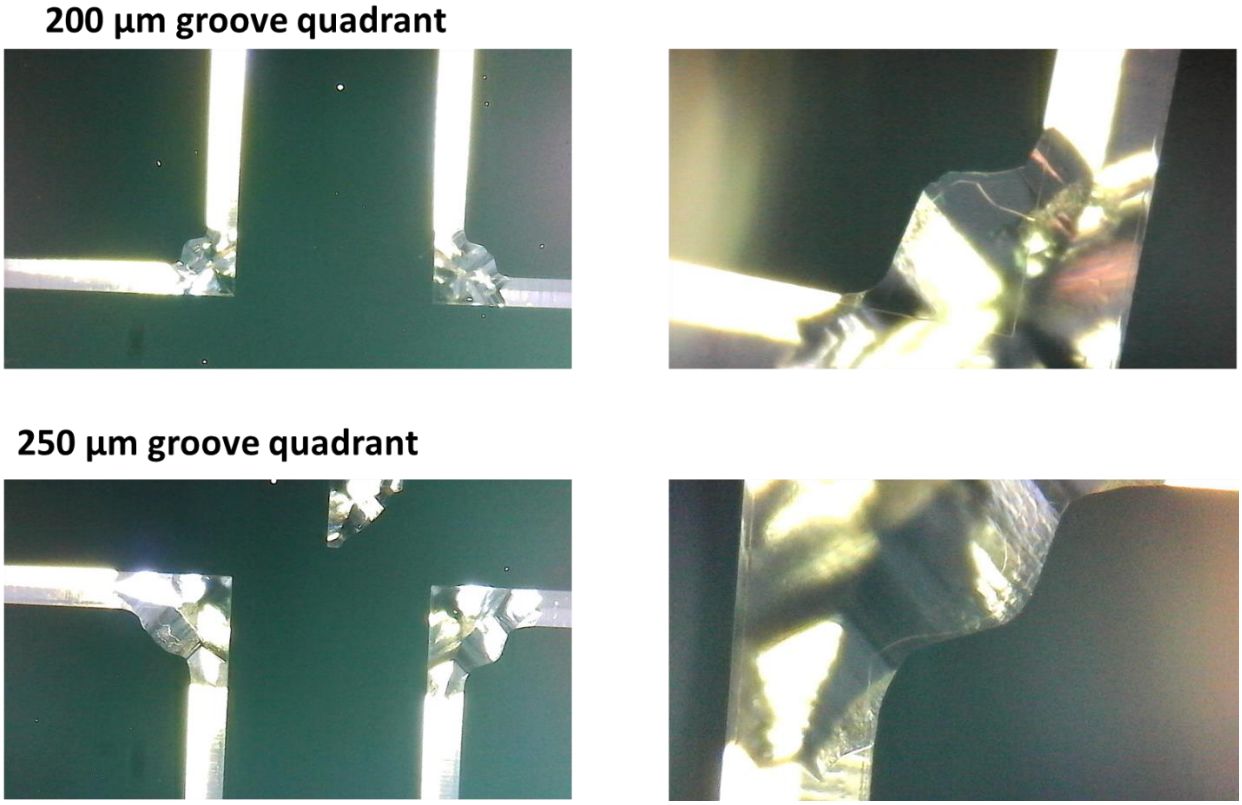


Figure 6.2.6. Optical microscope images of vertexes of V-groove etched dummy wafer.

(B.3) New DSRD fabrication process based on out-diffusion of dopants and wafer bonding is suggested. Experiment planned and ongoing. Vendors for out-diffusion – THAT Corp. and SVM Inc., and vendor for wafer bonding – EV Group chosen. Quotes requested. IP disclosure filed. Provisional patent application filed with USPTO. Abstract [9] describing the process flow submitted to upcoming Pulsed Power Conference.

6.2.5 Summary of Significant Findings and Mission Impact

(A) First sub-lot of epitaxy based Gen2 DSRDs finished and submitted for electrical measurements (static and pulsed) to UMKC team. These are made from 1st wafer from 12-wafers full Gen2 lot.

(B) Improving side termination of diodes. Short loop experiment for anisotropic etching of V-grooves finished. Technical feasibility of using this process for termination of side surface of diodes is confirmed. Thus, we can exclude undesirable vertical side wall in diodes and replace it by beveled wall.

(C) Replacement of unreliable metal contact deposition technique (by electron beam sputtering in vacuum chamber). All materials and equipment required for short loop experiment on selective electroless deposition of metals on silicon are collected, ready to start the experiment.

6.2.6 References

[1] Boff, A., J. Moll, and R. Shen. "A new high-speed effect in solid-state diodes." in 1960 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, vol. 3, pp. 50-51. IEEE, 1960

[2] Grekhov, I. V., V. M. Efanov, A. F. Kardo-Sysoev, and S. V. Shenderey. "Power drift step recovery diodes (DSRD)." Solid-State Electronics 28, no. 6 (1985): 597-599.

[3] Lyublinsky, A. G., E. I. Belyakova, and I. V. Grekhov. "Numerical and Experimental Study of an Optimized p-SOS Diode." Technical Physics 64, no. 3 (2019): 373-379.

[4] Люблинский, А. Г., Е. И. Белякова, and И. В. Грехов. "Численное и экспериментальное исследования оптимизированного p-SOS-диода." Журнал технической физики 89, no. 3 (2019): 409-415.

[5] Kesar, Amit S., Yaakov Sharabani, Inbar Shafir, Shoval Zoran, and Ariel Sher. "Characterization of a drift-step-recovery diode based on all epi-Si growth." IEEE Transactions on Plasma Science 44, no. 10 (2016): 2424-2428.

[6] Voss, Lars F., and Adam M. Conway. "Tunnel drift step recovery diode." U.S. Patent Application 17/081,902, filed April 29, 2021.

[7] Kyuregyan, A. S. "High-Voltage Diffused Step Recovery Diodes: I. Numerical Simulation." Semiconductors 53, no. 7 (2019): 962-968.

[8] Rukin, S. N. "Pulsed power technology based on semiconductor opening switches: A review." Review of Scientific Instruments 91, no. 1 (2020): 011501.

[9] S. V. Korotkov, Yu. V. Aristov, V. B. Voronkov, and D. A. Korotkov, “Studying dynistor switches with nanosecond switching times,” Instrum. Exp. Tech. 57, 437–442 (2014).

[10] Alex Usenko, Anthony Caruso, Steven Bellinger “New Paradigm on Making Semiconductor Opening Switches for Pulsed Power” abstract #456, 23th IEEE Pulsed Power Conference 12-16 December, 2021, Denver, CO

[11] A.Usenko, Diode and Method of Making the Same, US Provisional Patent Application 63/216550 filed 06/30/2021.

6.3 Characterization of SOS Diode Performance through DOE Augmentation

(Megan Hyde)

6.3.1 Problem Statement, Approach, and Context

Primary Problem: Drift step recovery diodes (DSRDs) are planar diodes that are capable of nanosecond, high frequency (10–10^3 kHz) pulses [1] with applications as opening switches in inductive energy storage (IES) pulse generation circuits. The theory provided by Benda et al is the primary physical explanation for DSRDs, but it does not provide explanations for either the current interruption mechanism or the current loop inductance [3]. This discrepancy within the physical model of the diode reduces the ability to design and produce IES pulse generating circuits. In addition to the incomplete theory on DSRDs, there is no characterization process for assessing diode performances, leaving the entire DSRD lifecycle riddled with systemic uncertainties.

Solution Space: We will develop a methodology for assessing diode performance to provide an empirical solution to the IES pulse generating circuit designer in Section 6.5. Our diode assessment methodology will leverage data analytics coupled with a design of

experiments (DOE) to process the parametric information provided by fabrication design (Section 6.2), to align the diode performance with simulation modeling (Section 6.1), and finally to provide an output for an optimized DSRD that meets the specific needs of the designer for the IES pulse generating circuit (Section 6.4).

***Sub-Problem 1*:** We do not yet understand how the diode performance is affected by variations within the diode parameters due to unstandardized testing methodologies.

Sub-Problem 2: A cohesive, standardized method for correlating the diode key performance indicators (KPIs) to IES pulser generator performance does not exist.

Sub-Problem 3: The non-linear separable data generated from the DOE is too complex to leverage traditional data analytics.

State-of-the-Art (SOTA): Characterization methods for DSRDs include electrical curve tracing techniques. The curve tracing techniques are performed by a parameter analyzer, such as a Keysight B1500A Semiconductor Device Parameter Analyzer. Transient characteristics of the DSRDs are measured through an Avtech Pulser, or a similar measurement device.

Deficiency in the SOTA: Unlike other commercial off the shelf (COTS) diodes, DSRDs do not come with a manufacturing datasheet. A COTS manufacturing data sheet contains all the testing and performance specifications relevant to the purchased diode. This leads to a difficulty in correlating the performance of a diode, or stack of diodes, to be utilized within a pulse generating circuit since the performance specifications are unknown to the purchaser.

Solution Proposed: Develop a holistic evaluation network to characterize the KPIs of DSRDs. This network will include a DOE that will be a continuously evolving model as new KPIs are discovered between each of the stages within the network (Sections 6.1to 6.5) referred to as the “augmented DOE”. Machine learning will be used as the primary decision-making tool for augmenting the DOE. Once the network is established, it will be used to outline the optimal parameters for stacks of DSRDs within an IES pulse generator.

Relevance to OSPRES Grant Objective: Bridging the gap between the theoretical and the physical performance of DSRDs enables closing the gap between a low fidelity TRL3 breadboard pulse generation system, and one which is at high fidelity TRL4 prototype level. At the TRL4 level, the DSRD-IES pulse generator system would be sufficient to replace the costly laser-based Si-PCSS HPM generator without compromise to scalability required to support the Naval afloat mission.

Risks, Payoffs, and Challenges:

Challenges: Traditional predictive analytics will be difficult to correlate with the augmented DOE due to the large volume of data. Machine learning is expected to assist with decision making processes for the DOE, but only if the proper KPIs have been established and good data has been used to train the machine learning model.

6.3.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Establish preliminary DOE and SOP for identifying KPIs of DSRDs [*estimated completion by DEC21*].

1. Task – Ascertain current KPIs used to optimize diodes simulated, manufactured, and utilized within the IES pulse generating circuit (from Sections 6.2–6) [JUN–AUG21];
2. Task – Construct preliminary DOE to acquire data on all KPIs based on Task 1 to produce an optimal output for the IES pulse generating circuit (Section 6.4) [AUG–SEP21];
3. Task – Leverage existing Python script to process legacy DSRD KPI data [*AUG—SEP21*];
4. Task – Develop new and review existing SOPs for experimental testing apparatuses used to evaluate individual KPIs and measure their performance [*AUG–OCT21*];
5. Task – Identify gaps/deficiencies in legacy KPI data, evaluate existing theoretical relationships to bridge gap and minimize DOE if possible [*SEP–OCT21*];
6. Task – Using SOPs developed in Task 4, acquire experimental data from legacy DSRDs, refine SOP(s) *pro re nata,* and assess repeatability and reproducibility [*SEP–OCT21*];
7. Task – Begin training machine learning model with legacy data to determine statistical correlations and significance of KPIs, and their interdependent relationships [*OCT–DEC21*];

(B) Milestone – Evaluate DSRD performance by the developed SOPs and facilitated by the preliminary DOE [*on hold until Milestone A is completed*].

1. Task – Augment DOE to include previously unidentified yet relevant KPIs based on new findings [*Est. Spring22*];
2. Task – Acquire data on newly manufactured epitaxial DSRDs from Section 6.3 using refined SOPs from Milestone A [*Est. Spring22*];
3. Task – Correlate KPIs to TCAD simulation model, manufactured diode characteristics, and 'M×N' IES pulser's performance to aid in simulation model development, fabrication procedures, and circuit topology development [*Est. Spring22*];

(C) Milestone – SOS diode network evaluation [*on hold until Milestone B is completed*].

1. Task – Refine Python script to incorporate new correlations based on findings from Milestones A&B [*Est. Fall22*];
2. Task – Amend ML training model with data acquired on new DSRDs (as characterized by Sections 6.2-3) to investigate statistical correlation of diode performance [*Est. Summer22*];
3. Task – Work with TCAD simulation team to address discrepancies between the DSRD's performance obtained experimentally, and that achieved within simulations [*Est. Summer22*];

4. Task – Collaborate with DSRD manufacturing team to address discrepancies between the DSRD's characteristics evaluated experimentally, and that desired by manufacturing process [*Est. Summer22*];
5. Task – Investigate relationships between statistical significance of individual diode KPIs to the peak performance of the IES pulser with the pulse generator team. [*Est. Summer22*];
6. Task – Incorporate findings from Tasks 1–5 into ML model, pinpoint KPI correlations of interest, and provide recommendations to IES sub-teams accordingly [*Est. Summer22*];

(D) Milestone – SOS diode network evaluation [*on hold until Milestone C is completed*].

1. Task – Augment DOE network to streamline diode evaluation and identify checkpoints/gates within simulation, manufacturing, and circuit development process to ensure optimal diodes are selected and utilized to produced robust high-fidelity IES pulse generator prototypes [*Est. Fall22*];

6.3.3 Progress Made Since Last Report

(A.1) Created a new KPI test matrix template to store information on each diode and to easily transfer parametric information to Sections 6.1–6.5. This matrix also contains a diode naming inventory.

Test	IV Forward Voltage	IV Reverse Voltage	Capacitance Voltage	Reverse Recovery	Reverse Recovery	Reverse Recovery
Equipment	Picoammeter	Picoammeter	Impedence Spectrometer	Avtech Pulser	Avtech Pulser	Avtech Pulser
Conditions	Start: 0V	Start: 0V	Start: -40V	Forward: 20V	Forward: 50V	Forward: 100V
	Stop: 10V	Stop: -200V	Stop: 5V	Reverse: -20V	Reverse: -50V	Reverse: -100V
	Step: 0.1V	Step: -1V	Number of points: 201	pulse width: 2um	pulse width: 2um	pulse width: 2um
				In Progress		

Table 6.3.1 Shown above is an excerpt from the KPI matrix template that is used to document and track the conditions of each test performed.

(A.4) Tested several DSRDs using the AVTECH pulser for reverse recovery time measurements. The recommended testing conditions, as stated by the AVTECH pulser manual, are incompatible with the DSRDs due to the oscillations found in the recovery time. These oscillations (Figure 6.3.1) are due to the attenuators used to protect the oscilloscope.

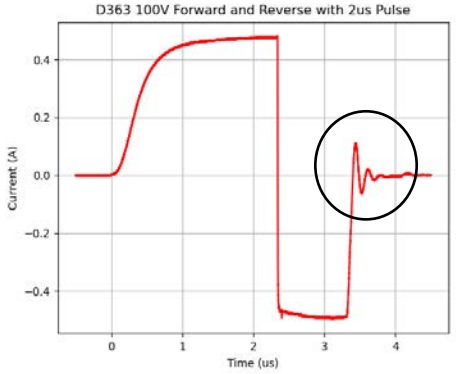


Figure 6.3.1 Reverse recovery time plot of a 7-stack DSRD with 100 forward and reverse voltages, 2 µs pulse widths, with a 46 dB attenuation (20 dB is built into the device testing fixture). The oscillations due to the attenuators are circled in black.

6.3.4 Technical Results

(A.4) Figure 6.3.2 shows the forward and reverse current-voltage (IV) measurements of 13 7-stack legacy DSRDs that were all measured on the picoammeter. All forward IV measurements maxed out the picoammeter sensor. Developing new measurement techniques that will not be limited by the equipment is currently an active area of research.

Shown in Figure 6.3.3 are two plots representing some of the 13-stack legacy DSRDs measured on the picoammeter for both the forward and reverse IV measurements. On the forward IV (graph on left), all the DSRDs maxed out the picoammeter sensor before reaching the desired 10 V maximum voltage as established in the IV measurement SOP. The reverse IV measurement, featured on the right-side in Figure 6.3.2, shows significant variability between each diode. The cause of this variation is currently unknown and is one of the reasons for pursuing a repeatability study.

Similarly, Figure 6.3.4 represents two plots for forward and reverse IV measurements, for 5 26 stack DSRDs. None of the DSRDs in the forward or reverse IV tests maxed out the picoammeter, as with the 7- and the 13-stack DSRDs, but there remains large variability in the measurements between each DSRD. Note that none of the DSRDs (7-, 13-, or 26-stack) achieved breakdown voltage.

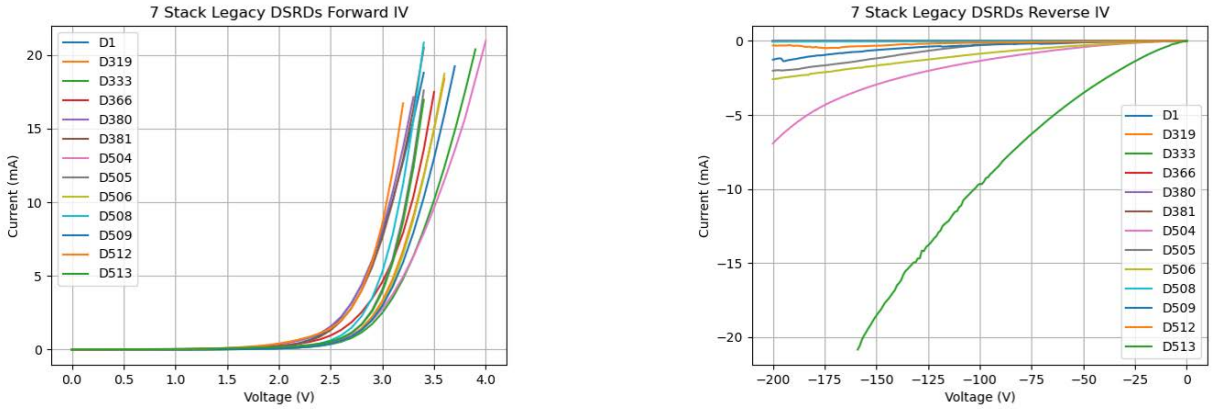


Figure 6.3.2 Forward and reverse current-voltage (IV) measurements of 13 legacy 7-stack DSRDs as measured by the picoammeter.

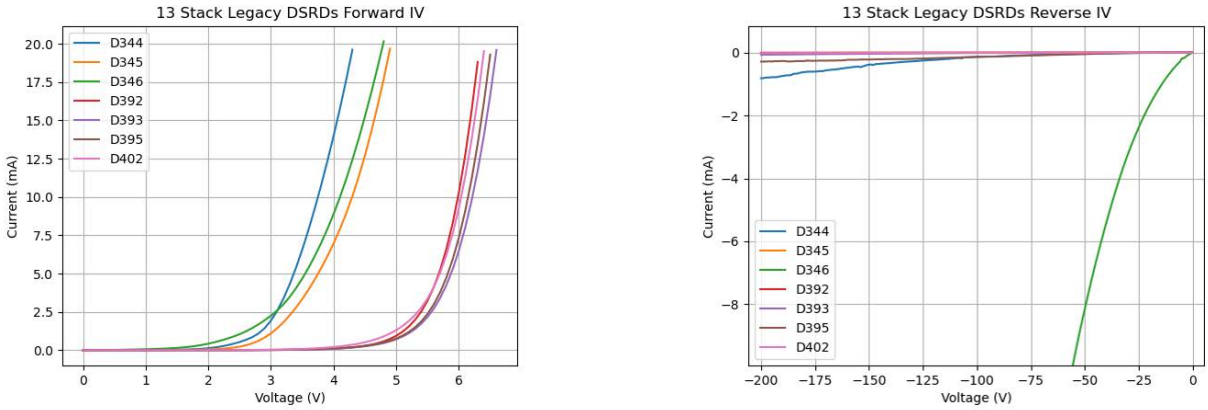


Figure 6.3.3 Forward and reverse current-voltage (IV) measurements of 7 legacy 13-stack DSRDs as measured by the picoammeter. D346 in the reverse IV graph (right) continued decreasing in current and eventually reached to –200V.

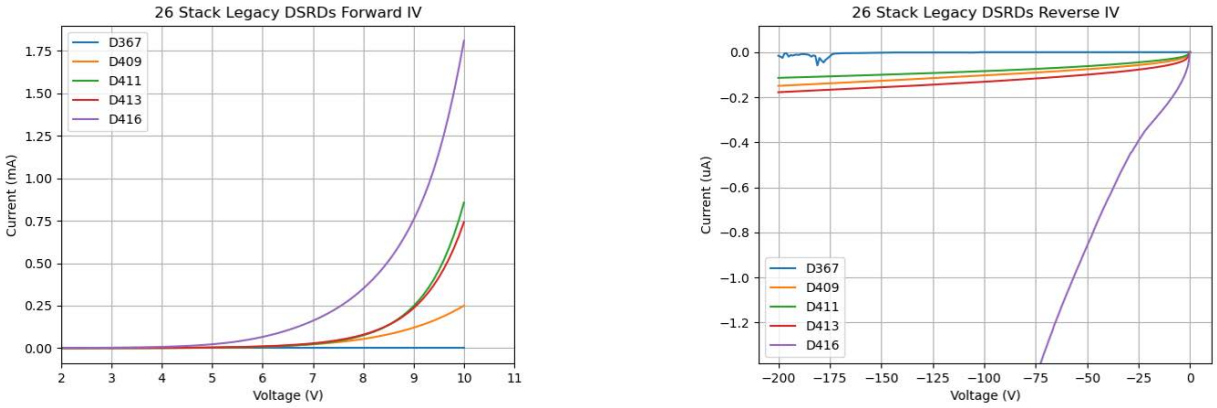


Figure 6.3.4 Forward and reverse current-voltage (IV) measurements of 5 legacy 26-stack DSRDs as measured by the picoammeter.

(A.6) The test fixture used for the IV measurements is a potential source of variability within the data. Often the DSRD must be measured 2 to 3 times before getting “nice” data. D402 in Figure 6.3.5 is an example of a “bad” measurement. The shape of the data trend (circled in red) could be caused by several things, such as bad electrical contacts, poor quality diode, poor connections from the test fixture to the picoammeter, etc. A repeatability study is currently in progress to help identify poor quality DSRDs from poor quality measurements.

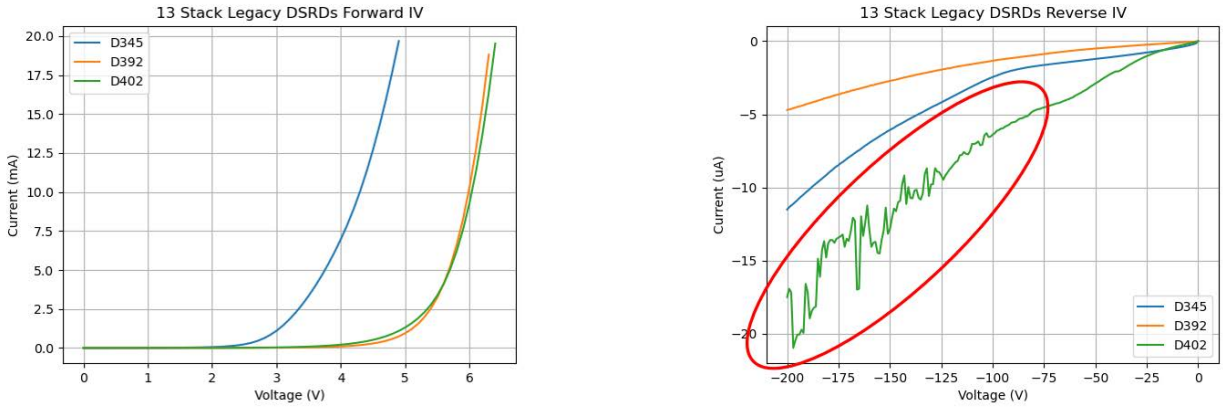


Figure 6.3.5 Forward and reverse current–voltage (IV) measurements of 3 legacy 13-stack DSRDs as measured by the picoammeter. Circled in red is a potential identification of error within the IV measurement process.

6.3.5 Summary of Significant Findings and Mission Impact

We have identified several KPIs pertaining to the diode characterization procedures. These KPIs have been stored within a matrix template that will also serve as a logistical catalog of legacy diodes and testing procedures.

Several diode characterization procedures have been updated. These procedures include both the IV and CV measurements. Both methods now have newly updated SOPs that track and catalog any changes made to the processes. All legacy DSRDs have now undergone IV and CV testing; several testing issues have presented themselves during this process. One issue is the large variability between each IV measurement. Several DSRDs had to be measured multiple times to get data that did not appear to be noise (refer to Figure 6.3.5). The IV measurement procedure is still in progress since the current equipment is only capable of achieving –200 V, which is far too low for measuring breakdown voltages.

The reverse recovery time (RRT) measurement procedure is also in need of improvement. Using the recommended diode testing conditions within the Avtech pulser manual is not a feasible option since the rise time is too fast for the attenuators to properly compensate for the 20 V or greater.

6.3.6 References

[1] Benda, H., & Spenke, E. (1967). Reverse recovery processes in silicon power rectifiers. Proceedings of the IEEE, 55(8), 1331-1354.

[2] Kozlov, V. A., Smirnova, I. A., Moryakova, S. A., & Kardo-Sysoev, A. F. (2002, June). New generation of drift step recovery diodes (DSRD) for subnanosecond switching and high repetition rate operation. In Conference Record of the Twenty-Fifth International Power Modulator Symposium, 2002 and 2002 High-Voltage Workshop. (pp. 441-444). IEEE.

[3] Sharabani, Y., Rosenwaks, Y., & Eger, D. (2015). Mechanism of Fast Current Interruption in p− π− n Diodes for Nanosecond Opening Switches in High-Voltage-Pulse Applications. Physical Review Applied, 4(1), 014015.

6.4 DSRD-Based Pulsed Power Source Systematic Topological Optimization

(Sourov Roy)

6.4.1 Problem Statement, Approach, and Context

Primary Problem: Drift step recovery diodes used in inductive energy storage (IES) and release pulse generators, when able to achieve ones of gigawatts in ones of nanoseconds, are large, heavy, and require liquid-based cooling systems to dissipate the excess heat they generate during operation; therefore, rendering them impracticable for Navy afloat missions.

Solution Space: Systematically develop a modular architecture of a pulser circuit using DSRDs by determining the optimal permutation of series and parallel combinations of the base pulser unit, and its component parameters, in order to maximize the peak voltage, peak power, and volumetric power density without sacrificing the desired nanosecond risetime of the pulses generated nor requiring liquid-based cooling.

***Sub-Problem*:** DSRDs are not domestically available COTs available components. The small-batch quantities that are manufactured have statistically significant variations in their performance parameters. In addition, SPICE models of these diodes are not accurate and do not account for their sample-to-sample parameter variability. The above-mentioned reasons may lead to an inaccurate simulation model of the pulser that may result in a difference between the simulation and experimental results.

State-of-the-Art (SOTA): DSRD-based pulsers (equivalent in size to the pulse generators developed for this effort, i.e., ~0.01-m^3, ~2-kg) can achieve 6-kV, 200-ps risetime, and <500 ps FWHM across a 50 Ω load.

Deficiency in the SOTA: DSRD-based air-cooled versions are limited to PRFs of < 15 kHz. Additionally, current studies on SOS-IES pulse generators attempt to present only the best-case circuit configurations meaning a comprehensive study on optimizing the number and ratio of parallel branches and series-connected stages aiming to achieve maximum gain and efficiency (reducing thermal load) is missing in the SOTA.

Solution Proposed: Systematically determine topological SOS-IES circuit configurations and the necessary components therein that maximize voltage gain and efficiency and minimize the rise-time achieved by the pulser.

Relevance to OSPRES Grant Objective: IES pulse generators using DSRDs can remove the need for photo-triggered switches and their laser sub-systems. They are ideal for triggering sub-nanosecond rise-time sharpeners (SAS, D-NLTL, etc.), reducing overall cost, volume, and weight.

Risks, Payoffs, and Challenges:

Risks: Domestically manufactured (U.S.-based) DSRDs which possess sub-optimal doping profiles may lead to sub-optimal pulse generators with sub-optimal performance. The data gathered from these sub-optimal circuits would then be used to train the genetic/machine learning algorithms developed and the redesign of future topologies constructed; ultimately leading to spurious conclusions regarding ideal topological circuit configurations with 'N' number of series-connected stages, each containing 'M' parallel branches.

Payoffs: Leveraging collaborative partnerships with U.S.-based manufacturers of DSRDs, the ability to refine and control the performance characteristics of the diodes themselves, along with the ability to simulate and manufacture the DSRD pulsers in-house, enables a holistic soup-to-nuts capability to optimize, produce, and evaluate these nanosecond pulse generators.

Challenges: Determining the superlative ratio of design/development (through numerical analysis) to the effort put towards experimental testing/evaluation of the DSRD pulser is challenging due to the novelty of the approach. The complexity of the theoretical model is extreme given the M×N number of DSRD base unit stages within the pulse forming network along with inaccurate DSRD spice model and large sample-to-sample variability.

6.4.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Construct/demonstrate a DSRD-based 2×2 IES pulse generator prototype capable of producing $\geq$4 kV peak voltage, $\leq$1 ns risetime, $\leq$5 ns FWHM, $\geq$320 kW peak-power, $\geq$1 kHz PRF, $\geq$100 shots-per-burst, $\geq$5 number of bursts [***Completed JUL21***].

(B) Milestone – Construct/demonstrate a DSRD-based 1×1 IES pulse generator prototype capable of testing individual and combinations of diode stacks to acquire performance data [***Completed AUG21***].

(C) Milestone – Construct/demonstrate a DSRD-based 4×2 IES pulse generator prototype capable of producing $\geq$12 kV peak voltage, $\leq$1 ns risetime, $\leq$5 ns FWHM, $\geq$3 MW peak-power, $\geq$100 kHz PRF, $\geq$1,000 shots-per-burst, $\geq$500 number of bursts [*Ongoing, estimated completion by OCT21*].

1. Task – Develop revised layout in Altium and order PCB and components. [***Completed – SEP21***];
2. Task – Populated pulse generator and begin testing & evaluation phase [*SEP – OCT21*];

(D) Milestone – Develop waveform inverter which, when combined with the pulser from Milestone C, enables a balanced differential waveform output with > 90 % inverted signal fidelity. [*on hold until Milestone C is completed*].

(E) Milestone – Construct/demonstrate a M×N pulse generator prototype capable of producing $\geq$20 kV peak voltage, $\leq$1 ns risetime, $\leq$2 ns FWHM, $\geq$8 MW peak-power, $\geq$100 kHz PRF, and $\geq 2\sigma_{V_{peak}}$, which operates in continuous-burst mode as a viable

candidate for OSPRES Contract source alternative [*on hold until Milestone C & D are completed*].

6.4.3 Progress Made Since Last Report

(C) The 4×2 DSRD-based pulse generator was designed using the PCB layout software Altium. The pulse generator's PCBs are currently being populated to enable testing of its performance.

6.4.4 Technical Results

(C) To increase the number of parallel branches to four (from the previous quantity two within the 2×2 pulser's design), a DC booster circuit was required to provide enough drive to each branch's SiC MOSFET from a single gate driver. The booster's design incorporates two bipolar transistors which are rated for a collector emitter voltage of 60 V and a collector current of 25 A.

In addition to the booster stage, the 4×2 redesign included relocating the primary capacitor bank to a separate board, the prime power board, which is positioned underneath the pulser board shown in Fig. 6.4.1. The prime power board hosts an increased number of capacitors to facilitate the increased number of parallel branches as well as pulser stage's DC bias voltage bus. In doing so, the pulser board layout now accommodates equivalent trace lengths of each parallel stage to facilitate matching of phase, impedance, inductance, and capacitance. Therefore, a single gate driver now supplies equally distributed and matched parallel branches with time-aligned triggering, to minimize offsets prior to power combining into the final stage within the DSRD pulse generator. These incorporated features are represented in the 2-D and 3-D views provided within Fig. 6.4.2.

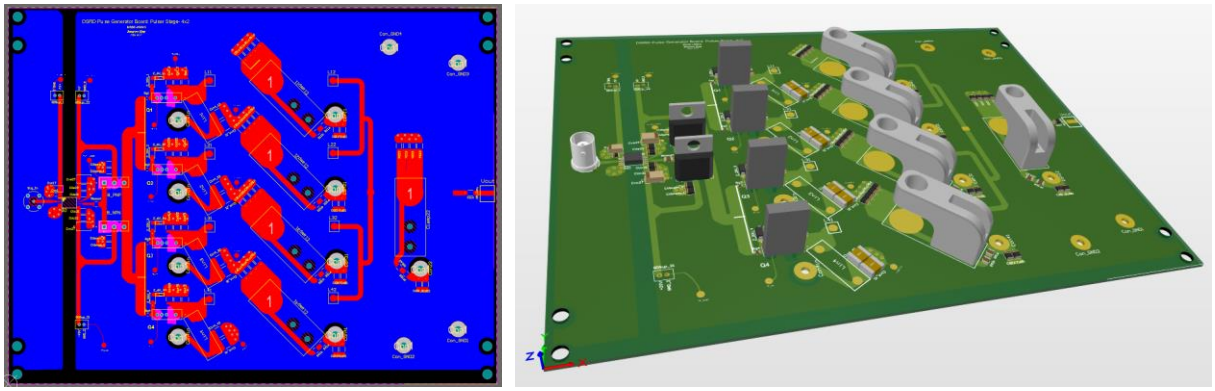


Figure 6.4.1. 4×2 DSRD-based pulser design layout in Altium: (*left*) top-view in 2-D and (*right*) 3-D view of pulse generator.

Once the design was completed in Altium, the PCB and components were ordered and are being populated. Although still in process, the present state of the 4×2 pulse generator is shown in Fig. 6.4.2.

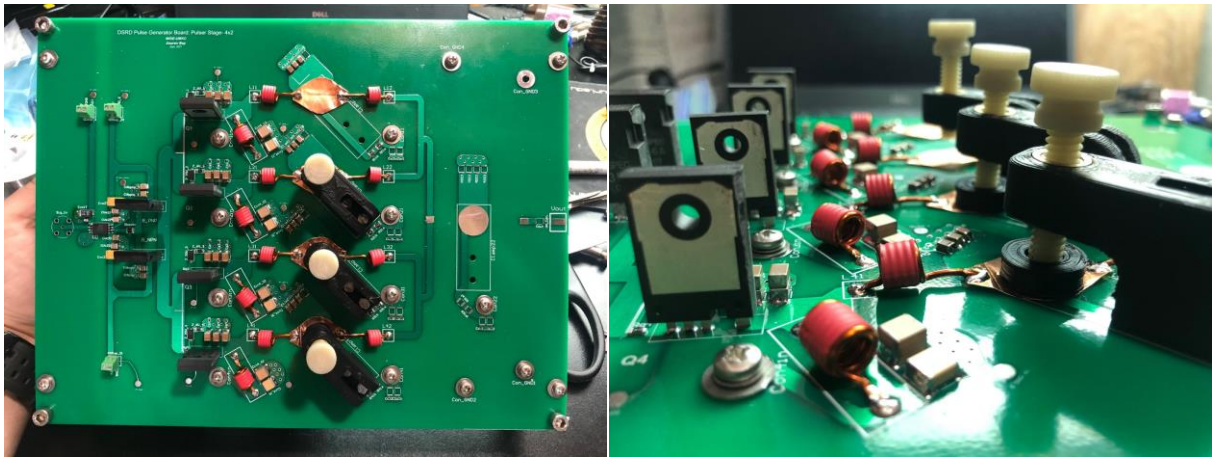


Figure 6.4.2. 4×2 prototype: (*left*) top-view in 2-D and (*right*) 3-D view of pulser.

The final stage of the pulser is still undergoing population. Once complete, the process of testing the new booster stage, ensuring time alignment from each of the MOSFETs is achieved, and full testing and evaluation of the pulser's performance will occur.

6.4.5 Summary of Significant Findings and Mission Impact

(A) Successful construction and operation of a 2×2 DSRD-based IES pulse generator prototype has been completed which meets or exceeds the milestone's required key performance metrics. Shown in Table 6.4.1 are the previous and current pulse generator's performance specifications in comparison to a similar 2×2 pulser developed by Kesar et al. [1] using DSRDs, and to that of a commercial off-the-shelf (COTS) DSRD pulser of similar space and weight developed by Megaimpulse (i.e., PPM-0731) which also uses DSRDs with silicon avalanche shapers (SAS) [2]. Although the Megaimpulse pulser utilizes a SAS with a <500 ps risetime (a threshold we do not intend to go below due to Commerce Controlled List limitations), it is interesting to compare the results of linear voltage gain and peak power of this system, to that of one that utilizes a SAS. The current permutation of the 2×2 SOS-IES pulser developed by MIDE under the ONR OSPRES Grant is able to achieve a higher peak voltage and shorter risetime than DSRD-based pulsers reported in the literature of comparable space and weight as well as those commercially available. The ability to generate a linear voltage gain of 40.8 to produce over a Megawatt of peak power into a 50 Ω load while achieving a peak voltage output standard deviation of 2σ when operating at a PRF of at least 100 kHz, brings this technology to the forefront of viable options to potentially support the Naval afloat mission.

Table 6.4.1 Comparison of DSRD-based IES Pulse Generator Performance

KPM	Units	MIDE - V1 Previous	MIDE - V2 Current	Kesar *et al.* SOTA	MI-PPM0731 COTS
V_{supply}	V	225	180	300	160
T_{ON}	ns	100	340	?	200
V_{peak}	kV	5.59	**7.35**	5	6.3
Gain	V/V	24.8	**40.8**	16.7	39.4
$\tau_{rise,20\text{-}90\%}$	ns	1.2	1.142	1.96	0.12
dV/dτ	kV/ns	4.66	6.44	2.55	**52.50**
FWHM	ns	2	5.48	2.27	0.35
PW	ns	5	7	3.5	2.5
Z_{LOAD}	Ω	50	50	50	50
P_{peak}	MW	0.625	**1.080**	0.500	0.794
E_{pp}	mJ	0.125	0.154	0.143	0.318
PRF_{max}	kHz	100	100	100	15
Burst	shots	100	100	*N/A*	100
	%	100	100	*N/A*	100
SD_{Vpeak}	σ	> 2	**> 2**	*N/A*	*N/A*
	%	96.5	**97.8**	*N/A*	*N/A*

(B) Discrepancies exist in the obtained data for different series combinations and different samples of 7-stack DSRDs which may be attributed to the inconsistencies in their manufacturing process. Future works in the coming months include carrying out further testing on the 1×1 DSRD-based pulse generator (base-unit) circuit using more combinations of series-connected as well as parallel-connected DSRD stacks.

6.4.6 References

[1] https://www.onsemi.com/pdf/datasheet/nvh4l020n120sc1-d.pdf

[2] https://cms.wolfspeed.com/app/uploads/2020/12/C2M0045170P.pdf

6.5 All-Solid-State Sub-ns MW Pulse Generators with Semiconductor Sharpeners

(Gyanendra Bhattarai)

6.5.1 Problem Statement, Approach, and Context

***Primary Problem*:** Broadband high-power microwave (HPM) systems need sub-nanosecond tens-of-MW pulses. Hydrogen spark gaps (HSG), traditionally used for such purposes, are severely limited by their low pulse repetition frequency (PRF ~1 kHz) and

poor device lifetime (shot life ~1000 pulses), ill-suited to achieve the SWaP metrics necessary for HPM pulse generators for the Navy afloat mission. Competitive solid-state solutions, such as inductive energy storage (IES) systems, utilizing a series stack of fast-opening diodes (drift-step recovery diodes (DSRD) and semiconductor opening switches (SOS)), have not been shown to break nanosecond barriers.

***Solution Space*:** Use viable pulse shaping/compression technologies based on semiconductor closing switches (e.g., delayed breakdown diodes (DBD), and fast ionization dynistors (FID)) to increase the peak power and shorten the rise time of the pulses produced by the DSRD-based pulse generator. Pulse sharpening/compression reduces the otherwise additional complexity of increased M×N stages within the pulser's topology; a desired result towards achieving optimal SWaP metrics of the pulse generation system without sacrificing PRF, shot lifetime, and thermal management requirements. (*Please refer to the June 2021 MSR for full problem and solution space description).*

***Sub-Problem 1*:** Achieving an order of magnitude increase in peak power (1-to-10 MW) through compression/sharpening methods requires series and parallel stacks of semiconductor closing switches (SCS), ultimately resulting in increased pulse risetime. Determining the optimal combination of diode stacks to decrease pulse risetime and increase output power requires additional SPICE circuit simulations. However, device models for SCS are not commercially available and thus require maturing SCS device models based on experimental results and physics-based simulations, such as using packages such as T-CAD, which can be time consuming.

***Sub-Problem 2 (Fundamental Physics)*:** Sub-nanosecond high-power pulse sharpening using semiconductor devices is based on ultrafast delayed avalanche breakdown under steeply increasing reverse voltage applied, thereby initiating an impact ionization front. However, the phenomenon behind the origin of free carriers that trigger the impact ionization at higher-than-breakdown fields is not completely known. Further, it is not clear whether the switching (generation of electron–hole plasma) is uniform across the device area or is localized (filamentary). Such different mechanisms are believed to be dependent on device geometry and doping concentration, and are detrimental to the switching speed. A University of New Mexico study [1] has concluded that the operation of a silicon avalanche shaper (SAS) is inconsistent with the theory described by Russian scientists. More understanding of device operation from a fundamental physics perspective is necessary to enhance their performances.

***State-of-the-Art (SOTA)*:** Prototype sub-nanosecond solid-state pulsers based on semiconductor opening switches (SOS) and semiconductor sharpeners are shown to produce peak voltages (~500 kV), and peak power outputs (~5 GW). Solid-state power supplies providing peak power up to 800 MW are available to purchase from FID Technologies, Germany. *Please refer to Table 4.7.1 of the June MSR for list of devices and their performance metrics.*

***Deficiency in the SOTA*:** Prototype ~5 GW power supplies, such as SOS based S-500 system with semiconductor sharpeners, are large (>1 m^3). Commercially available moderate-power (~1 GW) all-solid-state pulsers utilizing semiconductor sharpeners have

long purchase lead time (~4 months). Their PRF capability is limited to ~1 kHz due to physical constraints in thermal management.

***Solution Proposed*:** Downselect viable pulse compression/shaping technologies which meet or exceed the performance parameters set forth in Section 4.5's Milestones A-D towards producing an all-solid-state, tens-of-megawatts, sub-nanosecond pulse generator with semiconductor sharpener without sacrificing PRF, shot lifetime, and thermal management requirements.

***Relevance to OSPRES Grant Objective*:** The alternative all-solid-state technologies discussed could individually, or in combination, provide the means to produce order(s) of magnitude greater peak power, without severe limitation to PRF, as SWaP-centric means to increase the capability and extent of protecting naval assets.

Risks, Payoffs, and Challenges:

***Risks*:** Semiconductor closing switches, such as DBD and FID are not available to purchase within the United States. Procuring devices from abroad could lead to significant delay in experiments and development of device fabrication technology. Undergoing time-intensive and complex simulations to then down-select one technology based on peak power output alone presents risk to other secondary or tertiary performance metrics such as PRF and pulse energy, which risks developing ill-suited technologies to support the float mission. Additionally, as new technology emerges via research, scope creep to numerically and experimentally evaluate new technologies may delay transitioning these technologies into viable systems.

***Payoffs*:** The SWaP tradeoff of generating a non-laser-based system with any number of these systems can yield a higher fidelity pulsed-power waveform output. Determining which technology is viable and feasible in terms of the key performance metrics should yield a more ultracompact form factor pulse generator with order(s) of magnitude greater power density without compromise to overall size and weight to the system.

***Challenges*:** Determining the true performance metrics of interest based on these highly different devices is challenging. Without a more robust and deep understanding of their operation, and how to utilize them within a pulse generator topology, in a swappable configuration or otherwise, requires additional time and consideration. Managing the tradeoff between the academic understanding of the technologies of interest presented in the foregoing table, and the transition to prototype effort/mentality, will require both a delicate balance and leveraging the pulsed-power team's combined effort.

6.5.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Downselect viable pulse compression/shaping technology to be used in addition to currently utilized DSRD, which increases at least one of the key performance metrics by an order of magnitude without compromise to the overall volume of the system [*AUG21*].

1. Task – Finalize literature study of different technologies and topologies of SCS based pulse generators and compare SWaP tradeoff evaluation to PCSS- and DSRD/SOS-based pulse generators [*JUN–JUL21*]; [*Ongoing*]

2. Task – Determine commercially available technologies that could be used as pulse shaper/sharpening devices to improve pulse generator performance, and select appropriate devices for further experimental verification of their performance metrics [*JUN–AUG21*]; [*behind schedule*]

(B) Milestone – Model and experimentally verify the performance of the downselected technology as an additional component to the DSRDs utilized within a SOS-IES pulse generator. [*NOV21*].

1. Task – Develop T-CAD device model for the selected devices (DBD/DLD) based on available device information from literature and perform device simulation for their performance under nanosecond input pulse conditions. *[SEP–OCT21]*;
2. Task – Develop Spice device model for the selected device based on T-CAD simulation. [*SEP-OCT21*]
3. Task – Design experimental circuit with one selected diode or dynistor and obtain theoretical performance metrics using standard electronic simulation tools such as LT-Spice using the device model developed in task 2. [*SEP–NOV21*];
4. Task – Experimentally verify whether the selected device topology can produce peak power and pulse risetime equivalent to or better than that of SOTA. [*OCT–NOV21*];

(C) Milestone – Use Semiconductor Power Technologies (SPT) developed DSRDs and Voltage Multiplier Inc. developed Axial-lead Glass-body Diodes as alternatives to delayed breakdown diodes for pulse sharpening. [*Alternative to Milestone B, OCT-NOV21]*].

1. Task – Fabricate test fixtures for connecting DSRD and VMI diodes to DSRD–IES pulse generator, as described in **Section 6.4** or MegaImpulse PP10731 pulse generator. [*OCT–NOV21*];
2. Task – Test pulse sharpening using single, 2-stack, and 3-stack SPT DSRD and/or VMI diodes using the fixtures developed in Task 1. [*OCT–NOV21*]
3. Task – Prepare a performance matrix of DSRD and VMI diodes as pulse sharpener as a function of variations in DSRD test parameters discussed in **Section 6.3**.

(D) Milestone – Model diode/dynistor topologies and fabrication process. [*on hold until Milestones A and B are completed*].

1. Task – Model silicon diode and dynistors, with optimized device cross section (size, geometry) based on theory and simulations to increase current and thermal dissipation. [*On hold*];
2. Task – Model/design fabrication process with optimum device topology and doping concentration. [*On hold*]

6.5.3 Progress Made Since Last Report

(A.1) Additional scientific literature on semiconductor pulse sharpeners has been reviewed.

(B.1) Our Silvaco TCAD license is being renewed and a simulation workstation is being configured. TCAD simulation and device modeling materials are being reviewed.

(C.1) Gen-2 diodes from SPT have been acquired.

(C.2) Test fixtures for pulse sharpening using DSRD as SAS/DBD have been designed and are being fabricated.

Figure 6.5.1 shows a schematic of a DSRD–IES pulse generator with a DSRD (DBD) connected as the pulse sharpener, and Figure 6.5.2 shows a fixture being made to test DSRD as sharpener. The output pulse from the DSRD–IES pulse generator is fed into the sharpener (DBD) through the output capacitor C_{out}.

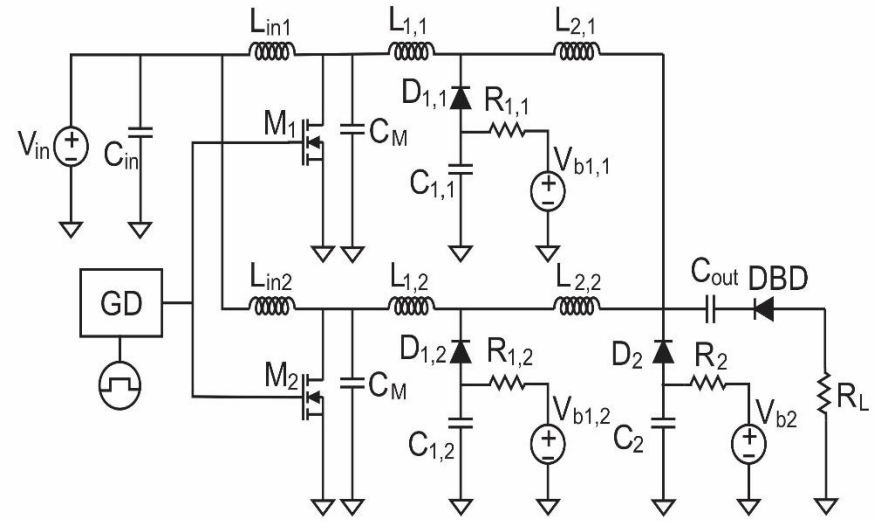


Figure 6.5.1 A schematic of a DSRD-IES pulse generator with a DSRD diode as SAS/DBD pulse sharpener.

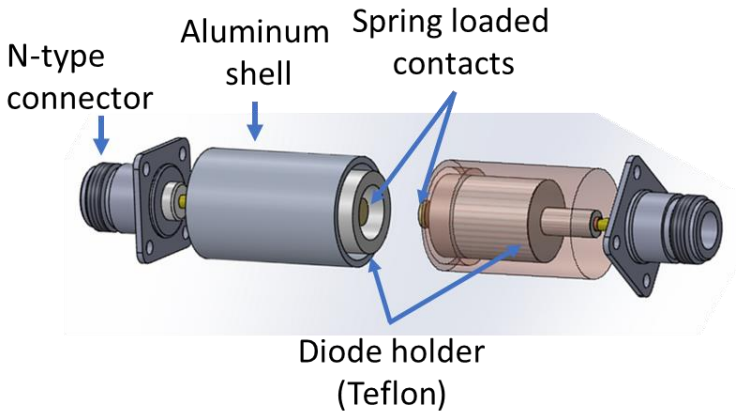


Figure 6.5.2 Test fixture for DSRD as SAS. A single DSRD or multiple stacks of DSRDs sit in between the two spring-loaded contacts inside an insulating housing.

6.5.4 *Technical Results*

(A) Based on the review materials [2], [3], [12]–[18], [4]–[11], the ranges of peak power and risetime of different switches is presented in Figure 6.5.3.

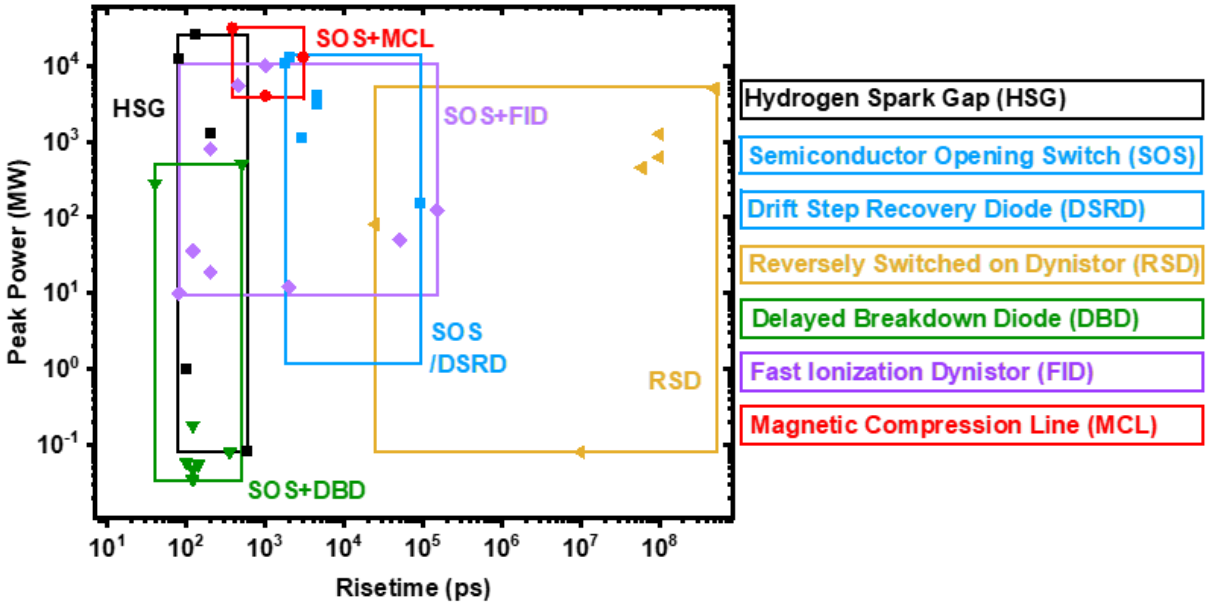


Figure 6.5.3 Ranges of peak power and pulse risetime of different types of high-power switches.

(B) DSRD (p^+–n–n^+) and SOS (p^+–p–n–n^+) are [ideally] similar to different structures of delayed breakdown diodes (DBD). The only difference between them is their working principles. DSRD and SOS pulsers need a forward pumping current and their switching is based on extracting the injected charge, while DBDs work completely on reverse bias by switching these devices due to the delayed impact ionization by a steep reverse voltage rise rate of ~10 kV/ns. In the presence of certain process-induced (PI) defect states in silicon, they are switched by voltage pulses with rise rate of ~1–2 kV/ns. Therefore, we can at least try a single DSRD or SOS die in a DBD configuration to test the pulse sharpening performance given that power switches producing about 3 kV with 10 kV/ns rise rate are available.

6.5.5 *Summary of Significant Findings and Mission Impact*

(A) We have reviewed a number of literature reports on different approaches for pulse power generation and sub-nanosecond pulse sharpening, such as hydrogen spark-gap (HSG), solid-state pulse generators including SOS–IES based generator with semiconductor sharpener, diode based non-linear transmission line, pulse generator based on Si and GaN photoconductive switches, and pulse generators with magnetic compression line. No single technology appears to meet or exceed the key performance metric requirements across the board. Where HSG lead in peak voltage and peak power, in comparison to the other technologies of interest, they lack in their ability to meet the required PRF, device lifetime, and SWaP-C metrics. All solid-state switching power supplies utilizing SOS and semiconductor sharpeners

seem viable technology to compete against HSG with comparable or better SWaP-C metrics.

6.5.6 References

[1] E. Schamiloglu, C. B. Fleddermann, R. Focia, and J. Gaudet, “A STUDY OF ADVANCED SEMICONDUCTOR SWITCH PHYSICS AND TECHNOLOGY PHILLIPS LABORATORY Advanced Weapons and Survivability Directorate AIR FORCE MATERIEL COMMAND KIRTLAND AIR FORCE BASE, NM 87117-5776,” 1997.

[2] S. Schneider and T. F. Podlesak, “Reverse switching dynistor pulsers,” *IEEE Trans. Plasma Sci.*, vol. 28, no. 5, pp. 1512–1519, 2000, doi: 10.1109/27.901224.

[3] V. I. Brylevskiy, I. A. Smirnova, A. V. Rozhkov, P. N. Brunkov, P. B. Rodin, and I. V. Grekhov, “Picosecond-Range Avalanche Switching of High-Voltage Diodes: Si Versus GaAs Structures,” *IEEE Trans. Plasma Sci.*, vol. 44, no. 10, pp. 1941–1946, 2016, doi: 10.1109/TPS.2016.2561404.

[4] V. M. Efanov, V. V. Karavaev, A. F. Kardo-Sysoev, and I. G. Tchashnikov, “Fast ionization dynistor (FID)-a new semiconductor superpower closing switch,” in *Digest of Technical Papers. 11th IEEE International Pulsed Power Conference (Cat. No.97CH36127)*, 1997, vol. 2, pp. 988–991, doi: 10.1109/PPC.1997.674523.

[5] I. V. Grekhov and P. B. Rodin, “Triggering of superfast ionization fronts in silicon diode structures by field-enhanced thermionic electron emission from deep centers,” *Tech. Phys. Lett.*, vol. 37, no. 9, pp. 849–853, 2011, doi: 10.1134/S1063785011090203.

[6] V. I. Brylevskii, I. A. Smirnova, P. B. Rodin, and I. V. Grekhov, “Subnanosecond avalanche switching in high-voltage silicon diodes with abrupt and graded p-n junctions,” *Tech. Phys. Lett.*, vol. 40, no. 4, pp. 357–360, 2014, doi: 10.1134/S1063785014040166.

[7] C. A. Frost, R. J. Focia, T. C. Stockebrand, and M. J. Walker, “Multi-kilovolt solid-state picosecond switch studies,” *IEEE Int. Conf. Plasma Sci.*, p. O1H7, 2001, doi: 10.1109/PPPS.2001.960861.

[8] S. K. Lyubutin, S. N. Rukin, B. G. Slovikovsky, and S. N. Tsyranov, “High-power ultrafast current switching by a silicon sharpener operating at an electric field close to the threshold of the Zener breakdown,” *IEEE Trans. Plasma Sci.*, vol. 38, no. 10 PART 1, pp. 2627–2632, 2010, doi: 10.1109/TPS.2010.2045396.

[9] A. I. Bushlyakov *et al.*, “Solid-state SOS-based generator providing a peak power of 4 GW,” *IEEE Trans. Plasma Sci.*, vol. 34, no. 5 I, pp. 1873–1878, 2006, doi: 10.1109/TPS.2006.881300.

[10] I. V. Grekhov, A. G. Lyublinskiy, and S. A. Yusupova, “High-power subnanosecond silicon avalanche shaper,” *Tech. Phys.*, vol. 62, no. 5, pp. 812–815, 2017, doi: 10.1134/S1063784217050115.

[11] I. V. Grekhov, A. K. Kozlov, S. V. Korotkov, I. A. Rol’nik, and A. L. Stepanyantz, “A High-Voltage Reverse Switch-on Dynistor Switch with a Transistor Control Circuit,” *Instruments Exp. Tech.*, vol. 45, no. 5, pp. 679–681, 2002, doi: 10.1023/A:1020466420755.

[12] P. Rodin, A. Minarsky, and I. Grekhov, “Impact ionization fronts in semiconductors: Numerical evidence of superfast propagation due to nonlocalized preionization,” *J. Appl. Phys.*, vol. 108, no. 3, pp. 9–11, 2010, doi: 10.1063/1.3465302.

[13] A. I. Gusev, S. K. Lyubutin, S. N. Rukin, B. G. Slovikovsky, and S. N. Tsyranov, “On the picosecond switching of a high-density current (60 kA/cm2) via a Si closing switch based on a superfast ionization front,” *Semiconductors*, vol. 48, no. 8, pp. 1067–1078, 2014, doi: 10.1134/S1063782614080132.

[14] V. I. Brylevskiy, I. A. Smirnova, N. I. Podolska, Y. A. Zharova, P. B. Rodin, and I. V. Grekhov, “Picosecond-range avalanche switching of bulk semiconductors triggered by steep high-voltage pulses,” *IEEE Trans. Plasma Sci.*, vol. 47, no. 1, pp. 994–999, 2019, doi: 10.1109/TPS.2018.2875423.

[15] V. Brylevskiy, N. Podolska, I. Smirnova, P. Rodin, and I. Grekhov, “Picosecond-Range Avalanche Switching Initiated by a Steep High-Voltage Pulse: Si Bulk Samples Versus Layered pn Junction Structures,” *Phys. Status Solidi Basic Res.*, vol. 256, no. 6, pp. 1–6, 2019, doi: 10.1002/pssb.201800520.

[16] V. Brylevskiy, I. Smirnova, A. Gutkin, P. Brunkov, P. Rodin, and I. Grekhov, “Delayed avalanche breakdown of high-voltage silicon diodes: Various structures exhibit different picosecond-range switching behavior,” *J. Appl. Phys.*, vol. 122, no. 18, 2017, doi: 10.1063/1.5004524.

[17] C. E. Baum *et al.*, “JOLT: A highly directive, very intensive, impulse-like radiator,” *Proc. IEEE*, vol. 92, no. 7, pp. 1096–1107, 2004, doi: 10.1109/JPROC.2004.829011.

[18] S. N. Rukin, “Pulsed power technology based on semiconductor opening switches: A review,” *Rev. Sci. Instrum.*, vol. 91, no. 1, 2020, doi: 10.1063/1.5128297.

7.0 GaN-Based Source Alternatives

7.1 Development of a GaN-Based Power Amplifier RF Source

(Abu Hanif)

7.1.1 Problem Statement, Approach, and Context

Primary Problem: To achieve the SWAP-C2 performance metrics necessary to support the cUAV Naval afloat mission, Gallium Nitride-based high electron mobility transistors (GaN HEMT) require multiple amplification stages in series to transition a low voltage/power signal (1-V, 1-GHz), to the high-power levels. Even the best high-power GaN HEMTs are limited to 2-3kW of peak power. Achieving the necessary effective radiated power (ERP) out of a high gain (≥ 10-dBi) narrow-band antenna requires input powers increase of two to three orders of magnitude and thus multiple parallel branches of HEMTs and/or power combining and pulse compression to achieve ERP at the MWs scale.

Solution Space: Pulse compression and power combination techniques are utilized to increase the peak power and lessen the pulse width in high power microwave (HPM) applications. Adapting multiple pre-amplification stages to increase the power levels to the appropriate inputs required by GaN HEMTs in a reconfigurable fashion facilitates leveraging commercially available off the shelf (COTS) devices and combiners to be pulse compressed and thus achieve sufficient ERP with an optimal radiating element.

***Sub-Problem 1*:** The analytical relationship between pulse compression ratio (PCR) and peak output power (P_{out_peak}) and the compression limit are not yet clearly understood. Thus, leveraging the findings from this study will enable us to develop the RF source with minimum number of compression and combination stages with maximum PCR that will meet the required ERP.

Sub-Problem 2: SPICE models for sate of the art (SOTA) high power GaN HEMT power amplifiers (PAs) which can produce higher than 1-kW peak power, are needed to be developed as they are not available yet. The developed model will create a platform to simulate them in conjunction with pulse compression stages which will eventually help in developing the RF source meeting the SWAP-C2 requirements.

Sub-Problem 3: A custom built prime power unit with adjustable output power needs to be developed to supply the necessary voltage and current for the PA unit. For example, MACOM MAPC-A1500 requires 65V, 1.3A prime power unit for an efficient operation whereas INTEGRA IGN1011S3600 requires 100V 150mA unit. Therefore, the design needs to be dynamic since the required power will vary depending on the number of series and parallel stages of the GaN HEMTs PAs as well as the module to be used since different manufacturer require different power levels for their respective PA module.

State-of-the-Art (SOTA): Large modular RF pulse generators (>1-m^3, >1000-lbs) which are comprised of at least 8 parallel-combiners, have demonstrated peak output power up to a few GWs. All these prototypes are stationery and rack mounted. Smaller versions (~0.125-m^3, 50-lbs to 100-lbs) can achieve 50kV peak voltage with PCR of 667 at 70ns FWHM terminated at 307Ω load [1]. Another power amplifier manufactured by Amplifier

Research has an output of only 800W peak power which weighs 70lbs [2]. However, none of them are suitable for Navy afloat missions due to weight to peak output power ratio.

Deficiency in the SOTA: Large RF pulse generators are traditionally limited by mechanical design constraints and power supply limitations. They are large (few meters long), leverage huge transformers, and require liquid coolant such as transformer oil for cooling purposes, which lead to undesirable system mass values even more than 1000-lbs. In addition, a comprehensive analytical study on pulse compression and peak output power is missing in SOTA; specifically, as it pertains to GaN-based RF sources.

Solution Proposed: Developing a highly efficient and cost effective GaN-based power amplifier RF source capable of achieving 1-5 W/cm^2 at 10-50m away with the minimum number of series connected modules (i.e., M×N) with maximum volumetric power density. Therefore, methodically the optimum peak output power and maximum pulse compression ratio through topological GaN based power amplifier design including the power combination including reconfigurable antenna design and the necessary components therein that maximize power/voltage gain and efficiency achieved by the RF source as well as the output parameters such as peak power, pulse width, etc., are adjustable in real time at will to meet the mission needs.

Relevance to OSPRES Grant Objective: Reconfigurable RF source with adjustable RF parameters (e.g., output power, pulse width, bandwidth, frequency) will enable the system to exercise dynamic MPM missions (i.e., multi mission) with optimal SWaP-C2 parameters.

Risks, Payoffs, and Challenges:

Risks: Existing GaN based high output peak power yielding amplifiers such as MAPC-A1500 (peak power of 2600W) and IGN1011S3600 (peak power of 3600W) are out of stock. Lower-power versions produced by the same manufacturer that have been quoted have long lead times (26-weeks ARO) and require minimum of 50 to order making them thousands of dollars to purchase. Alternatively, building the amplifier module from scratch will take its toll in time as well as the performance of the built prototype might be poor in terms of efficiency and form factor.

Payoffs: Building the amplifier module from scratch will payoff in terms of utilizing the lead time to find the most suitable pulse compression method that can achieve 2-3 orders of peak power and compression gain which will eventually meet the mission needs and therefore, the appropriate compression method can be immediately deployed with the COTS GaN amplifiers once they are received.

Challenges: High power PAs and pulse compression methods are usually lossy in nature and generate considerable amount of heat, therefore, designing a proper cooling method must be carried out which may inadvertently increase the volume (size and weight) of the overall design.

7.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Achieve 2-3 orders of peak power and compression gain using magnetic pulse compression (MPC) [*estimated completion by DEC21*].

1. Subtask – Simulate MPC circuit in LTSpice to find out the electrical parameters for the MPC unit design/AUG-OCT21/Ongoing.
2. Subtask – Design pulse transformer (PT) and magnetic switch (MS) required for the MPC unit/SEP–*OCT21*/Ongoing.
3. subtask –Build and test the MPC prototype using bench top power supply/OCT–*DEC21/Ongoing*.

(B) Milestone – Achieving comparable peak power level given in datasheet using MACOM MAPC-A1500 based evaluation board [*on hold until the evaluation board is received-lead time is about 26 weeks*].

(C) Milestone – Obtaining 2-3 orders of peak power and compression gain using MAPC-A1500 GaN HEMT PA and MPC prototype built in milestone A [on hold until milestone B is complete]

7.1.3 Progress Made Since Last Report

(A.1) An electrical equivalent circuit of MPC unit has been simulated in LTSPICE. In addition, the circuit components were purchased for the first iteration of MPC prototype.

7.1.4 Technical Results

(A) Following schematic of an MPC circuit was build in LTSPICE.

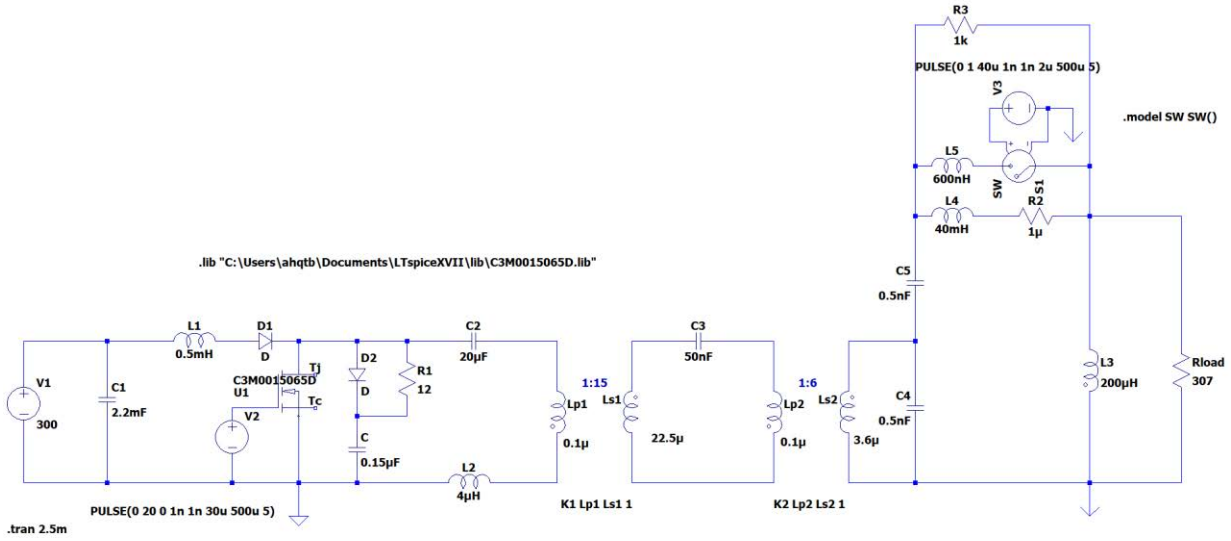


Figure 7.1.1. Schematic of a 3-stage MPC unit

Schematic of Figure 7.1.1 was constructed based on the circuit diagram given in [1]. However, pulse transformers (PT1 and PT2) and magnetic switch need further tuning to achieve the expected output. The magnetic switch was modeled based the study reported in [4]. Figure 7.1.2 show the electrical equivalent of the magnetic switch.

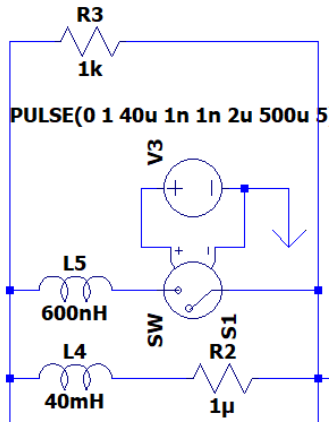


Figure 7.1.2. Electrical equivalent of a magnetic switch [4]

However, this electrical model is not yet an ideally equivalent model of a magnetic switch. It would need a significant effort to model the magnetic switch. Alternately, using a saturable inductor might be a viable solution to this problem where a B-H curve can be included to make the simulation more accurate. This avenue is currently being explored. In addition, components required to build the initial prototype of MPC unit have been ordered which will allow us to verify the system whether it will be a good fit for the intended use. Furthermore, the built prototype will be used to verify and tune the simulation results.

7.1.5 Summary of Significant Findings and Mission Impact

(A) Pulse compression and power combination is inevitable in achieving the goal of the mission. However, the most appropriate method for compression is yet to be identified. To achieve the mission goals, several pulse compression methods with be studied and experimental results will be compared to identify the most viable method. For now, task 1 under milestone A needs to be carried out with highest importance to accomplish the objectives in a timely manner.

7.1.6 References

[1] D. Zhang, Y. Zhou, J. Wang and P. Yan, "A compact, high repetition-rate, nanosecond pulse generator based on magnetic pulse compression system," in IEEE Transactions on Dielectrics and Electrical Insulation, vol. 18, no. 4, pp. 1151-1157, August 2011, doi: 10.1109/TDEI.2011.5976109.

[2] https://www.arww-modularrf.com/rack-mount-amplifiers.cfm

[3] https://www.ieee802.org/15/pub/05/

[4] M. Watanabe, J. Kamiya and T. Takayanagi, "Design and Circuit Simulation of a Magnetic Switching System for Kicker Magnet Power Supply of 3 GeV RCS in J-PARC," in IEEE Transactions on Applied Superconductivity, vol. 20, no. 3, pp. 1681-1684, June 2010, doi: 10.1109/TASC.2010.2040612.

8.0 Thermal Management

8.1 Ultra-Compact Integrated Cooling System Development

(Justin Clark, Roy Allen, and Sarvenaz Sobhansarbandi)

8.1.1 Problem Statement, Approach, and Context

Primary Problem: A compact cooling unit is required for the thermal management of semiconductor-based pulse-power devices, with the goal of maintaining the semiconductor device temperature below 80 °C. The goal is to create an ultra-compact cooling unit which increases cooling densities for high pressure microwave (HPM) systems, while decreasing pumping power requirements, in-line with the SWaP-C^2 objective.

Solution Space: To achieve such high heat flux, a turbulent flow profile must be achieved. The approach we are going to take is to create an ultra-compact unit integrated onto a semiconductor device, allowing more heat extraction to occur. The pumping power will be kept to a minimum since the unit to be prototyped will represent 1 cm^2 surface area. This enables less power to be consumed to create a turbulent flow. An array of micro-sized jet nozzles will provide a turbulent flow onto a microchannel section directly on the semiconductor device. The ultra-compact design will reach turbulency at a faster rate while requiring less energy consumption.

Sub-Problem: The turbulency formed from the array of nozzles creates an extreme pressure loss. With a large amount of jet nozzles (over 200) and a flow diameter of nearly 100 microns, the pressure across the system will decrease tremendously. The pressure must be sustained to enable proper cooling and circulation processes. Another way to sustain pressure is to use different liquids. Different types of coolant will be simulated to determine effects from fluid density and viscosity. Preliminary studies show that pressure loss can be maintained using DI water or a type of gas while still requiring a small amount of pumping power.

State-of-the-Art (SOTA): Integrated chip cooling will be used to dramatically increase the operational power of high voltage silicon-based power devices by increasing the power device heat-removal via an integrated active cooling microelectromechanical system (MEMS) within the power chip device. Current SOTA devices include individual parts which attach to a high-power device, causing less interaction between the semiconductor and coolant, degrading the heat removal rate.

Objective: A compact cooling unit is proposed, which will be based on refining in-chip jet-impingement geometry through leveraging theory and a parametric evaluation of nozzle geometry and flow channel arrangements. With the in-chip theory proposed and manufacturing constraints implemented, a 1 cm^2 surface area, Si-base unit will be prototyped to maneuver a higher capacity of heat removal.

Anticipated Outcome(s): To create an ultra-compact cooling unit with the ability to rapidly remove 1 kW/cm^2 of heat. This heat dissipation rate is a common goal for many defense applications. A design capable of such high heat removal can be implemented on many other applications such as high-power batteries.

Challenges: The manufacturing techniques of the semiconductor chips have not yet been used for integrated chip cooling systems. These designs are limited due to low tolerance of the manufacturing process. The manufacturing process of the device must be capable of etching microchannels and layering the silicon TMS onto the semiconductor.

Risks: With a system so compact, the pressure drop could be a large issue regarding the objective heat dissipation rate. An extreme pressure drop would potentially cause the coolant to have reverse flow effect, causing less fluid-to-solid interaction. If the system fails to produce high heat dissipation and will not keep the device under the threshold temperature of 80 °C, the device may degrade too rapidly.

8.1.2 Tasks and Milestones / Timeline / Status

(A) Design a Si base 1 cm^2 cooling unit, taking into account manufacturing tolerances, to achieve a heat dissipation rate of 1 kW/ cm^2. The design must be able to be produced by manufacturing techniques such as etching and lithographic layering processes. When modeling the device, each section was layered piece by piece to confirm the device can be manufactured as proposed / MAY21–AUG21 / Completed

(B) Using the optimal design, perform ANSYS simulations using either water or Si-C nanofluid. Other fluid types may be researched as pressure drop is a large factor / JUL21–DEC21 / In Progress

(C) With proper simulation results concluded, a prototype will be manufactured to begin experimental testing and evaluation / DEC21–MAR22 / Upcoming

8.1.3 Progress Made Since Last Report

(A) Simulation results are in place to confirm geometry sizing and overall design of the device, specifically the nozzle ratios and microchannel fins to confirm which method is capable of highest heat extraction.

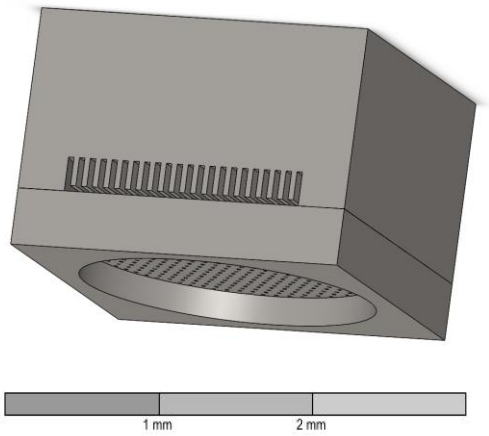


Figure 1.3.1: Preliminary Design of Ultra-Compact Device

(B) The chosen design began simulation process in Ansys Design Modeler to simulate the fluid interaction within the device. Following this step, a general mesh with

adaptive sizing was applied to the device and fluid domain. Meshing errors occurred due to the wide range of element sizing shown in Figure 1.3.2.

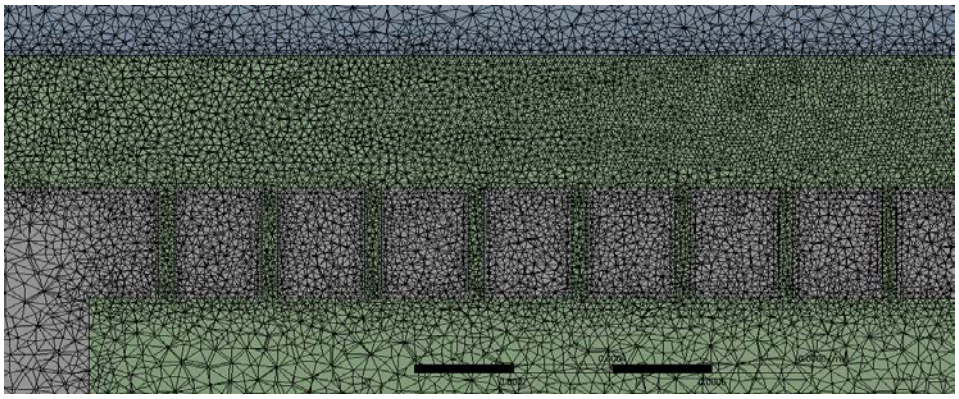


Figure 1.3.2: Cross Sectional View of Jet Nozzle Mesh

8.1.4 Technical Results

(A) Using ANSYS Fluent, a constant temperature of 360 K was applied at the simulated heat source, where the laser would interact with the semiconductor in the real-world application. This preliminary simulation proved the microchannel fins dissipated heat better than jet impingement on a flat surface as shown in Figure 1.4.1. The microchannel fin design increases the fluid-to-solid contact enabling higher heat extraction.

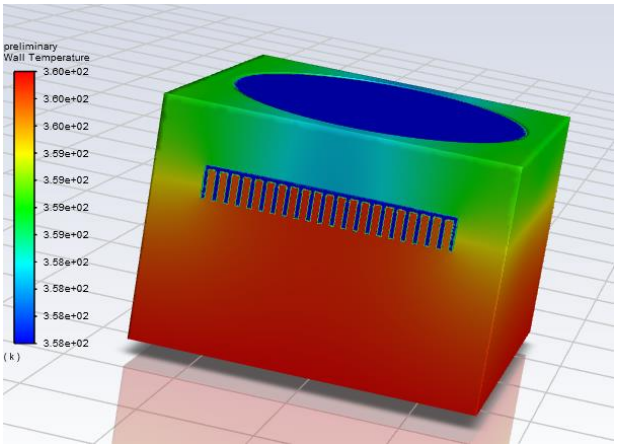


Figure 1.4.1: Preliminary Simulation

(B) The varied dimensions from the 3 mm base to the 0.035 mm nozzles caused many elements with orthogonal quality <0.1, causing a bad mesh and poor simulation results. Individually face sizing the elements of each nozzle and microchannel achieved a minimum quality of 0.172 with 1.5 million nodes. Previous literature has shown up to 8 million nodes for a slightly larger system with larger nozzle diameters. The simulation is on-going, and results will be achieved in the upcoming reports.

8.1.5 Summary of Significant Findings and Mission Impact

(A) From a literature review, similar designs were analyzed including a water-cooled, crossflow microchannel cooling system with various microchannel widths has been previously designed. The design achieved a simulated heat flux of 1.7 kW/cm^2 using 0.056 W of pumping power. Although this particular design is not the best fit when including the manufacturing constraints, the results using micro channel heat sinks are remarkable and design considerations are further analyzed. A similar design implemented the idea of having jets confined in their own individual spaces, experimentally reaching up to 900 W/ cm^2 with 0.83 W of pumping power. A third design analyzed two types of heat sinks with flat and oblique angled fins which were experimentally tested with a constant heat flux of 100 W/cm^2. The temperature difference was from 60 °C to 35 °C which proposed giving the design more power. The oblique angled fins caused 20 percent greater heat transfer than flat fins.

(B) To achieve a higher quality mesh around the nozzles and microchannels, the nozzles element size was initially set to 20 microns, or until the shape of the nozzles were more profound in a cylindrical shape. The surface which connects to the nozzles resulted with an element size of 15 microns and the nozzle sizing resulted in 13 microns. These values had to maintain a very similar size to reduce the skewness and maintain mesh quality. Each surface with poor quality was selected and set to individual face sizing and is currently undergoing simulation.

9.0 Pulse Forming Networks

9.1 Diode-Based Nonlinear Transmission Lines

(Nicholas Gardner)

9.1.1 Problem Statement, Approach, and Context

Primary Problem: The size, weight, and cost of pulse forming/shaping networks (PFNs) need to be reduced and optimized for Navy afloat missions.

Solution Space: Develop a diode-based nonlinear transmission line (D-NLTL) as a pulse shaping network for the conversion of energy to the ultra-high frequency (UHF) band (0.3–3 GHz) at single MW peak power.

Sub-Problem: Metrics used for component selection are designed for D-NLTLs operating at sub 0.1 GHz frequencies. Using such metrics alone to design D-NLTLs capable of single GHz frequency generation introduces a trial by error nature to the design process wherein frequency/power generation predictions and measurements can differ by a few hundred MHz or the design potentially fails to operate at all.

State-of-the-Art (SOTA): D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit. Simulations of LE-NLTLs indicate achievable frequencies in the single GHz range.

Deficiency in the SOTA: Simulation/measurement agreement becomes increasingly sensitive to parameters and factors outside of inductive and capacitive element choice alone at frequencies above ~100 MHz. Disparities between measurement and simulation above contribute to a trial by error design process for D-NLTL networks.

Solution Proposed: Identify and characterize diode parameters affecting frequency generation in the context of a NLTL application via simulation and experiment, and identify limits/desired ranges required for UHF generation. Such parameters include, but are not limited to: diode frequency response, diode reverse bias hold-off voltage, diode small signal capacitance, diode chip/package parasitics, and diode relaxation time. The improved understanding of the explored parameters will be used to design and fabricate a D-NLTL capable of GHz center frequency generation at single MW peak powers.

Relevance to OSPRES Grant Objective: The SWaP-C^2 capabilities of D-NLTLs (shown in Figure 9.1.1) represent a potential solution to the size, weight, and cost optimization issue for PFNs on Navy afloat missions.

Figure 9.1.1 20 cell D-NLTL of dimensions 1.1 x 23.45 cm constructed with commercial off the shelf components.

Risks, Payoffs, and Challenges: There exists a potential tradeoff between power and frequency generation. Devices such as ceramic capacitors may be used in a D-NLTL to generate high peak power due to their break down potentials in the 10s of kV, however,

such devices become highly resistive at 0.1–0.2 GHz frequencies. Diodes have been shown to be operational at frequencies upwards of 0.4 GHz, however, possess low hold-off potentials limiting peak output power. The payoff to overcoming these challenges is significant reductions in PFN size and cost.

9.1.2 Tasks and Milestones / Timeline / Status

(A) Milestone – Construct/demonstrate a prototype capable of UHF generation at low voltages (1–100 V excitation amplitude)

(A1) Break a low-voltage pulse into a sequence of solitons (SEP20)
(A2) Increase frequency generation past 200 MHz (NOV20)
(A3) Select diode candidate (junction capacitance <50 pF) and simulate expected results (Ongoing)
(A4) Design/fabricate/test line (Ongoing)

(B) Milestone – Demonstrate tuning of waveform at low voltages using electrical or mechanical means (**Completed with voltage biasing APR21**)

(C) Milestone – Construct/demonstrate a prototype capable of frequency generation above 1 GHz at single MW peak powers (Completed MW peak power but not GHz center frequency – Ongoing)

(C1) Identify diode candidates with a hold-off voltage of several kV and a low signal junction capacitance under 100 pF (Completed JAN21)
(C2) Design/fabricate single diode prototypes (Completed JAN21)
(C3) Perform initial tests using half-barrel pulse source (Completed FEB21)
(C4) Refine simulation using measurements (Completed FEB21)
(C5) Test a prototype using two diodes in series (Completed FEB–MAR21)
(C6) Test lines using Mega Impulse source (Completed MAY21**)**
(C7) Test K50F D-NLTL using PCSS as a source (Completed JUN21)
(C8) Use simulations and tests to refine line for increased frequency generation (Completed JULY21)
(C9) Rebuild lines for negative polarity pulses (Completed JULY21)
(C10) Test lines using PCSS as a source with various cell inductances (Completed JULY**)**
(C11) Test lines using Marx Generator as a source (**Completed AUG21**)
(C12) Reconstruct PCSS strip line to produce a pulse similar to 5.1.2 (left) and retest (**Ongoing AUG21)**

(D) Milestone – Demonstrate power scalability using an array of D-NLTLs (**On Hold – Prioritizing Milestone C**)

(D1) Design a prototype capable of running two D-NLTLs simultaneously off of the same excitation pulse (Completed JUN21)
(D2) Build a circuit capable of measuring the CV curve of low-voltage diodes and measure the CV curves of unused diodes and heavily used diodes (Completed JUN21)

9.1.3 Progress Made Since Last Report

(C) The waveform from the K50F based HV D-NLTL excited by a Marx Generator was compared to simulated results. Original measurements for the K50F line consisted of a center frequency of 595 MHz and a Bragg frequency of 961 MHz. Simulations displayed good success in replicating the frequency generation with an average center frequency of 559 MHz and average Bragg frequency of 1.225 GHz. Results are displayed in Fig. 9.1.2 and Table 9.1.1.

9.1.4 Technical Results

GHz MW D-NLTL Prototype (C): A consistent issue in D-NLTL design is agreement between simulated frequency generation and measured frequency generation with simulation tending to predict greater frequencies than prototypes produce. In the month of September, D-NLTL + Marx generator results were compared with simulation to both explain the origin of the amplitude spike from August and further refine simulation parameters. The SPICE schematic used is shown in Fig. 9.1.3 with R_L, C_L, L_D, and C_D representing sources of loss in the inductor and diode models; the three combinations with the best match are displayed in Fig. 9.1.2.

There are two results of interest to discuss. First, in the August tests the Marx generator was triggered 100 times, with 10 measurements occurring at a larger amplitude than the other 90. Simulation indicated the 10 large amplitude measurements occurred due to reflections at the source–line impedance mismatch resulting in a superposition of generated and reflected pulses with an amplitude of ~5 kV. Second, alterations to sources of loss in SPICE did a good job of matching the frequency generation of the measured prototype with an average center frequency of 559 MHz and average Bragg frequency of 1.225 GHz as compared to the measured 595 MHz center frequency and 961 MHz Bragg frequency. However, the modulation depth of the measured waveform was difficult to match.

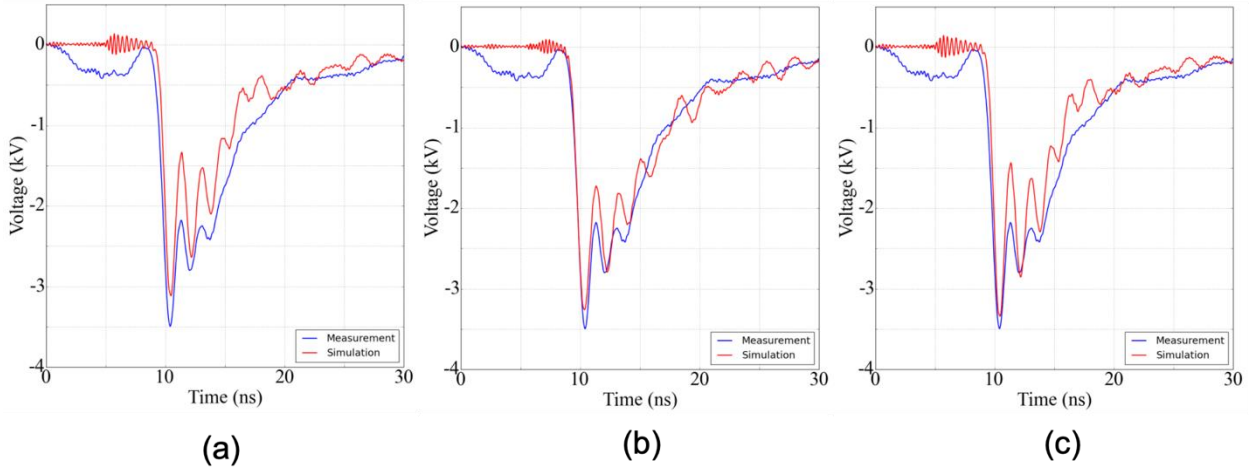


Figure 9.1.2: Results from Marx-D-NLTL measurement–simulation matching. In all images, blue shows the measured waveform and red shows the simulated waveform. Good agreement was achieved in matching the measured center and Bragg frequencies

by only altering sources of loss in the design. Values for the parasitic sources and frequency measurements are shown in Table 9.1.1.

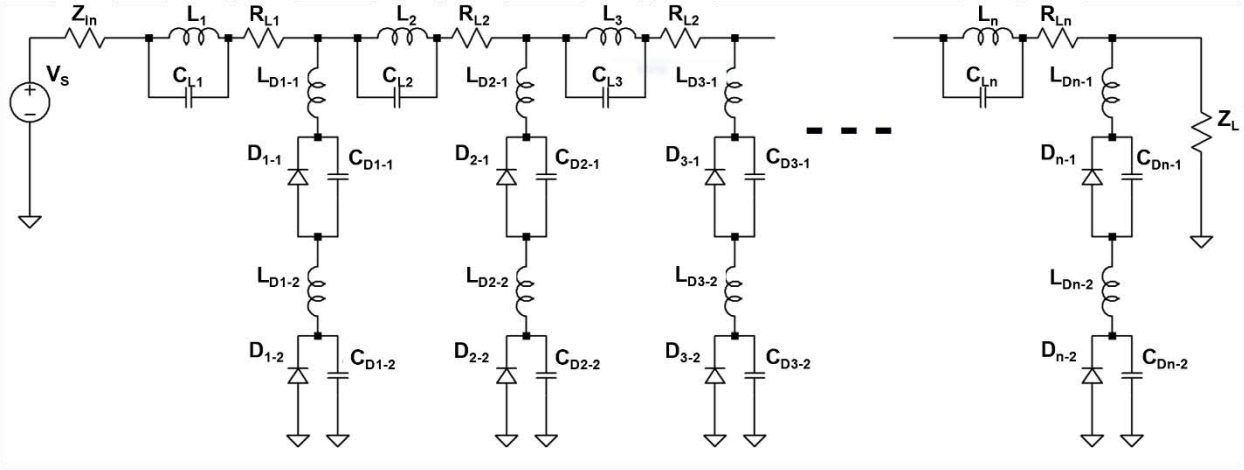


Figure 9.1.3: An example schematic for Marx-D-NLTL measurement–simulation matching using the K50F diode. In each cell R_L, C_L, L_D, and C_D represent sources of loss in the diode and inductor models. Starting and varied values are shown in Table 9.1.1.

Table 9.1.1: Values for the inductor and diode sources of loss and the frequencies generated by each combination. Lc is not included as it was not altered.

	L	R_L	L_{Dn-1}	L_{Dn-2}	C_{Dn}	Fc	Bragg
V1 (a)	5 nH	10 mΩ	1 nH	2 nH	10 pF	574 MHz	1.25 GHz
V2 (b)	2 nH	5.6 mΩ	0.5 nH	4 nH	14 pF	538 MHz	1.17 GHz
V3 (c)	5 nH	10 mΩ	1 nH	2 nH	10 pF	565 MHz	1.24 GHz

9.1.5 Summary of Significant Findings and Mission Impact

(A) After a failure of the high-voltage diode-based nonlinear transmission lines (D-NLTLs) to reproduce simulated results, work refocused on low-voltage D-NLTLs to determine the source of the discrepancy. In NOV2020 a center frequency of ~250 MHz was achieved using a D-NLTL design based on the diode model SMV1702.

(B) Following the success of the SMV1702 D-NLTL, a circuit was designed, capable of electrically tuning the center frequency utilizing DC biasing of the diodes. In FEB–APR2021 the circuit demonstrated a linear relationship between DC bias up to a limiting potential. Negative DC biases decreased center frequency while positive DC biases increased center frequency.

(C) In JAN2021 two diode candidates (models K100F and K50F) were identified for a HV D-NLTL design. FEB2021 saw successful tests of both D-NLTLs with each sharpening the rise time of a pulse produced by a DSRD based source down from

~1 ns to ~600 ps. In AUG2021 the first major variation between the K50F and K100 F D-NLTLs were observed with the K50F line breaking the pulse into solitons while the K100F line primarily sharpened the rising edge of the pulse. In SEPT2021 comparisons between measured and simulated results for Marx+K50F measurements indicate further success in modeling inductor and diode parasitics to predict frequency generation.

(D) During MAY2021 a line topology capable of feeding two identical D-NLTLs with the same pulsed source at the same time was fabricated. Initial results were collected, and a prototype is currently being designed to test the ability to parallelize D-NLTLs.

9.2 Continuous Wave Diode-NLTL based Comb Generator

(Nicholas Gardner and John Bhamidipati)

9.2.1 Problem Statement, Approach, and Context

Primary Problem: Diode-based nonlinear transmission lines (D-NLTLs) can be limited in power transfer efficiency and frequency response due to the source–line impedance mismatch caused by the dynamic impedance changes they undergo due to the varying diode capacitances when excited with discontinuous bursts of ultrashort pulse trains. This leads to signal/power reflection and standing wave generation and return power losses, resulting in size, weight, and cost optimization issue for PFNs on Navy afloat missions.

Solution Space: Develop a continuous wave (CW) mode D-NLTL based comb generator as a pulse shaping network to convert continuous signals from low frequency–very high frequency (LF–VHF) bands (0.03 MHz–30 MHz) to the ultra-high frequency (UHF) band (0.3–3 GHz) at ones-of-MW peak power.

Sub-Problem(s) (optional): Design parameters and component selection metrics for ~MW peak D-NLTLs have not been widely studied for frequencies >0.1 GHz. On the other hand, metrics for comb generators capable of generating ~50 GHz output frequencies are limited to <1 Watt output powers. Using such metrics alone to design D-NLTLs capable of single GHz frequency generation while handling MW-order peak powers introduces a trial by error nature to the design process wherein frequency/power generation predictions and measurements can differ by a few hundred MHz

State-of-the-Art (SOTA): Commercial-off-the-shelf (COTS) GaAs varactor diode based monolithic microwave integrated circuit (MMIC) D-NLTL comb generators are capable of operating at input and output frequencies up to 600 MHz and 30 GHz, respectively. However, these comb generators are not capable of handling powers higher than 27 dBm (0.51 W). In-house pulsed D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit.

Objective: Characterize the diode parameters such as frequency response, C–V characteristics, reverse bias hold-off voltage, small signal capacitance, packaging parasitics, and relaxation time in the context of a NLTL application and identify their limitations in terms of UHF generation to demonstrate a CW D-NLTL based comb generator capable of center frequencies on the order of ones-of-GHz at ~MW order peak power.

Anticipated Outcome(s): A successful demonstration of improvements to impedance matching at the source-line interface using a CW signal measured as a reduction in signal amplitude loss between the source and D-NLTL.

Challenges: Despite their 10s of kV voltage ratings, the resistive response of ceramic capacitors at 0.1–0.2 GHz impose a need for alternatives. Diodes have been shown to be operational at frequencies upwards of 0.4 GHz, however, possess low hold-off potentials limiting peak output power.

Risks: There exists a potential tradeoff between power and frequency generation. Limited component selection metrics for high-power UHF-capable D-NLTLs complicate simulation and prototyping.

9.2.2 Tasks and Milestones / Timeline / Status

(A) Demonstrate an ability to reduce source–line impedance mismatch effect on signal amplitude with CW D-NLTLs through simulations and validate the results experimentally using low voltage (LV) and high voltage (HV) prototypes.

(A1) Show the potential to improve source–line impedance mismatch in simulation (**Completed SEP21)**

(A2) Experimentally demonstrate a low voltage (LV) prototype receiving a CW input (**Completed SEP21**)

(A3) Compare measured results with simulation behavior (**Ongoing**)

(A4) Determine if there are improvements to system behavior if D-NLTL diodes are biased when receiving a CW input (**Ongoing**)

(A5) Demonstrate improvements to the source–line impedance mismatch in a LV prototype (**Ongoing**)

(A6) Demonstrate a high voltage (HV) prototype receiving a CW input (**Ongoing**)

(A7) Demonstrate improvements to the source–line impedance mismatch in a LV prototype

(B) Demonstrate UHF (0.3 – 3 GHz frequency) generation with a CW D-NLTL.

(C) Demonstrate UHF Generation at Single MW Power levels with a CW D-NLTL.

9.2.3 Progress Made Since Last Report

(A) Initial simulations were performed to see if there is a potential effect of continuous wave excitation on source–line impedance mismatch. Results are shown in Fig. 9.2.1 and indicate there could be a minor improvement to source–line impedance

mismatch, however no dependence on excitation frequency was observed. Measurements were taken on a prototype based on a diode of model

9.2.4 Technical Results

(A) Two initial measurements were collected on a low voltage D-NLTL for the purposes of observing effects of a CW input. All measurements and simulations were performed on a D-NLTL based on a schottky diode of model SMV1702 due to an ability to receive bipolar excitations and electrically alter diode behavior as documented by MIDE's D-NLTL work. Both simulation (Fig. 9.2.1) and measurement (Fig. 9.2.2) demonstrated little effect on the source–line impedance mismatch and no frequency dependence. However, the CW excitation is aimed at taking advantage of the average impedance of the network to improve impedance matching. At a 10 V pulse amplitude the average impedance of the D-NLTL used is $31\,\Omega$ which represents a significant mismatch with the 50 Ω source. In the coming month the results shown in Fig. 9.2.2 will be compared directly with simulation to determine if the simulation is producing realistic results. Initial tests will also be performed on the high voltage D-NLTL prototypes based on K50F and K100F diode models which each have an average impedance of 70 Ω and should match better with the source.

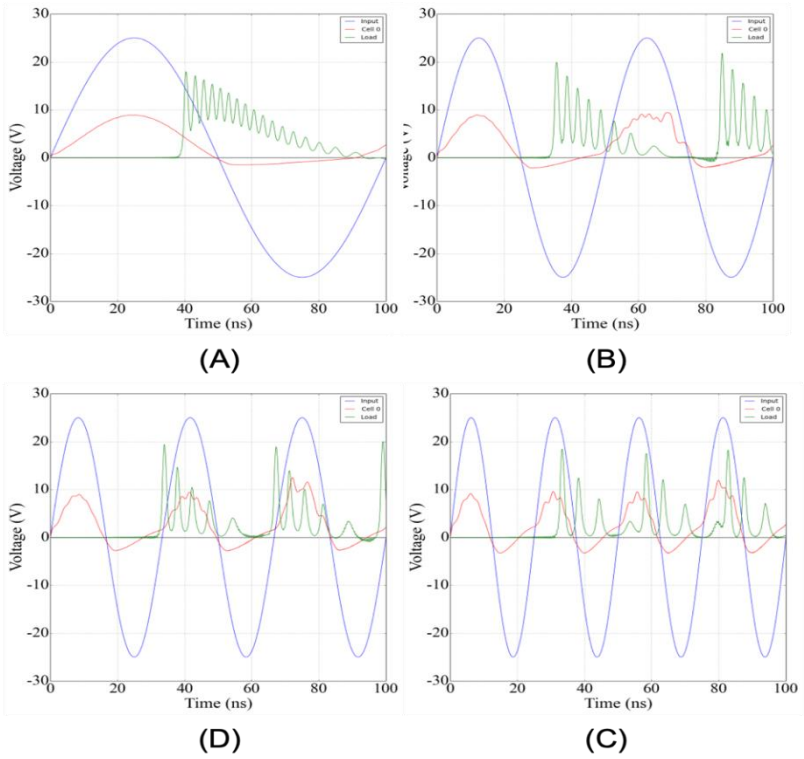


Figure 9.2.1: Initial simulation results for the CW D-NLTL. (A) A 10 MHz 50 V_{pp} sine wave excitation. (B) A 20 MHz 50 V_{pp} sine wave excitation. (C) A 30 MHz 50 V_{pp} sine wave excitation. (D) A 10 MHz 50 V_{pp} sine wave excitation. Initial indications show there could be a minor improvement at the source–line impedance mismatch. However, there was no dependence on excitation observed.

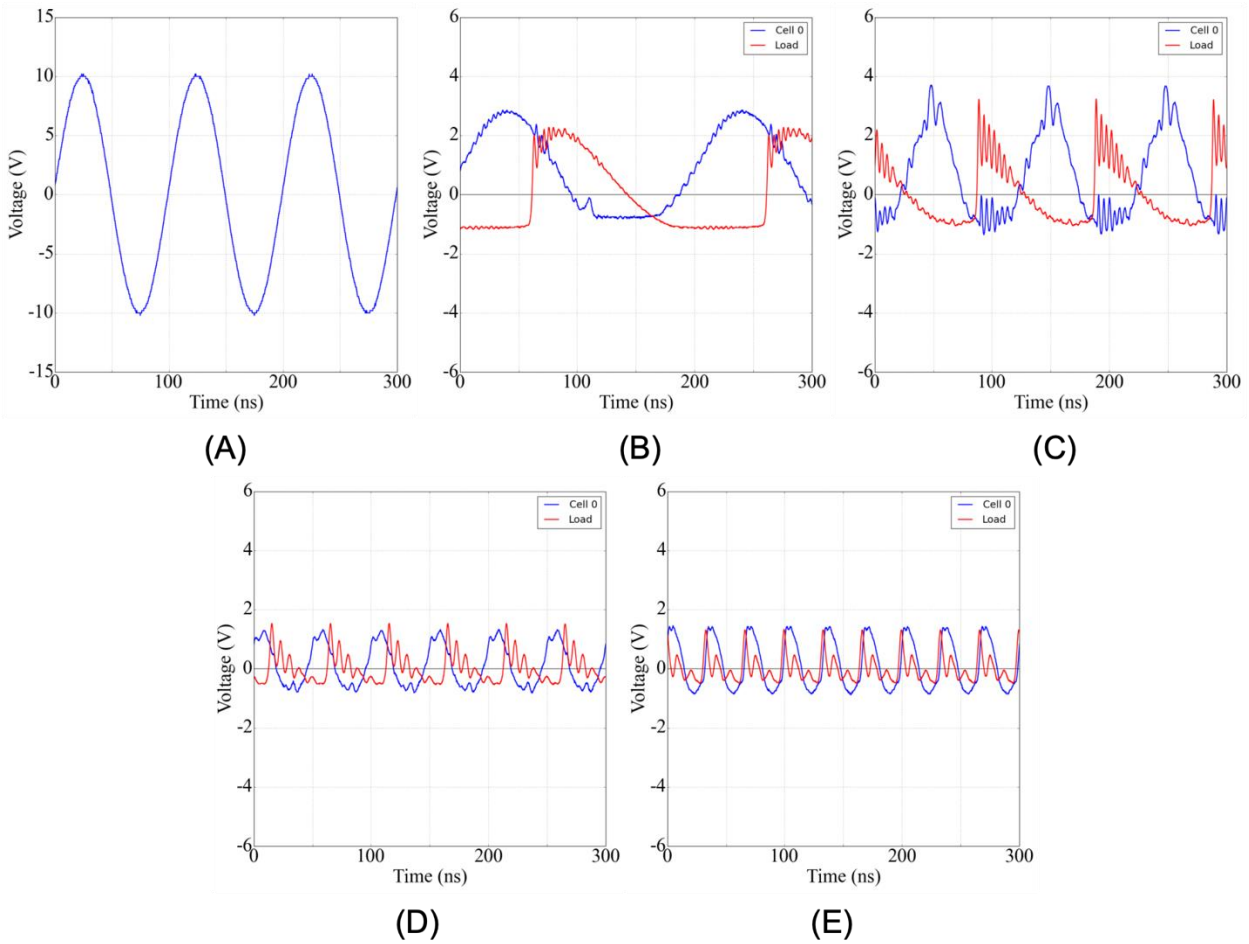


Figure 9.2.2: Measured results for D-NLTL continuous wave measurements. (A) 10 MHz 20 V_{pp} sine wave used, only frequency was altered for each D-NLTL measurement. (B) 5 MHz 20 V_{pp} sine wave excitation. (C) 10 MHz 20 V_{pp} sine wave excitation. (D) 20 MHz 20 V_{pp} sine wave excitation. (E) 30 MHz 20 V_{pp} sine wave excitation. Initial results show little to no improvement on the excitation impedance mismatch with little dependance on excitation frequency.

9.2.5 Summary of Significant Findings and Mission Impact

(A) Initial results were collected to determine the effect of continuous wave excitation on source–line impedance mismatch between the excitation source and D-NLTL with respect to signal amplitude. Little improvement was observed in source–line impedance matching when the line was excited with continuous wave sinusoidal input with cell zero measurements giving a 2 V amplitude for all frequencies tested.

10.0 Antenna Development

10.1 Tradespace Analysis of an Array of Electrically Small Antennas (ESAs)

(Bidisha Barman and Deb Chatterjee)

10.1.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of patch antenna elements whose feed, two-dimensional shape, and relative placement (i.e., intra-, and inter-element design) allow for the physical aperture size to be reduced by more than 20% compared with the present-art.

Sub-Problem: To overcome scan blindness (as the main beam is electronically steered), due to the excitation of surface waves (SW). (Note: scan blindness is a common phenomenon in electrically small microstrip patch antenna arrays).

State-of-the-Art (SOTA): Horn, reflector, Vivaldi, valentine, etc. are some of the commonly used ultra-wideband (UWB) antenna elements in a phased array for high-power microwave (HPM) transmissions.

Deficiency in SOTA: Large physical aperture size of the antennas.

Solution Proposed: Using electrically small antennas (ESAs) as array elements and optimizing their performance in terms of both near-field (bandwidth) and far-field (directivity) parameters, followed by arrangement of the ESAs in suitable lattice structures (preferably, hexagonal/triangular) to reduce the overall array aperture area. Using stochastic and machine learning (ML) algorithms to optimize antenna element and array performance.

Relevance to OSPRES Grant Objective: Provides design and optimization guidelines for UWB ESA elements, especially coaxial probe-fed microstrip patch antennas, and arrays for HPM applications.

10.1.2 Tasks and Milestones / Timeline / Status

(A) Develop an Array Pattern Tool in the context of lightweight calculations of large antenna arrays / JAN–MAY 2021 / Completed code.

(B) Investigate the effects of array aperture area reduction on different array parameters (such as gain, beamwidth, electronic beam steerability) and present a comparative study of antenna array parameters as a function of array aperture area / JAN–MAY 2021 / Completed investigations of arrays on infinite ground planes.

(C) Build minimum viable validation prototypes of single ESA elements on substrates that have good power handling capabilities for HPM transmissions at UHF range (such as polyethylene, FR-4, TMM-10i, TMM-6) / JAN–OCT 2021 / Ongoing fabrication of an antenna element on a polyethylene substrate.

(D) Optimization of ESA (single element) performance using regular, and ML based stochastic search algorithms / JUN–SEP 2021 / Ongoing.

(E) Build minimum viable validation prototypes for arrays of ESA elements / JUN–SEP 2021 / Ongoing fabrication of a 2×2 array of ESAs.

(F) Optimization of array performance using ML algorithms (**NEW**) / SEP 2021–JAN 2022 / Ongoing.

10.1.3 Progress Made Since Last Report

(C) Build minimum viable validation prototypes of single ESA elements:

a. Modeled and characterized a coaxial probe-fed wideband rectangular microstrip patch ESA element, via FEKO, on a 1.05-inch-thick TMM-10i ($\epsilon_r = 9.8$) substrate at the UHF range (638.2-990.6 MHz).

b. A coaxial probe-fed microstrip patch antenna element (0.9–1 GHz), on a 0.65-inch-thick polyethylene substrate, is still under manufacture.

(D) Optimization of ESA (single element) performance using ML algorithms:

a. Optimized the designed antenna parameters (viz. ground plane size, probe location and radius), via ML algorithms, to seek the best bandwidth in the desired UHF range (0.6-1 GHz).

(E) Build minimum viable validation prototypes for arrays of ESA elements:

a. Modeled and characterized a 5×5 array (square lattice), composed of the ESA elements, mentioned in Part (C), on a circular-shaped, 1.05” thick, PEC-backed, TMM-10i substrate.

b. Ongoing manufacturing of a 2×2 array of microstrip patch ESA elements (0.9–1 GHz) on 6.35 mm thick TMM-10i substrate

(F) Optimization of array performance using ML algorithms:

a. Optimized the 5×5 array parameters using ML based genetic algorithm (GA) to minimize the mutual coupling between the center-most and the corner-most element.

10.1.4 Technical Results

(C) Build minimum viable validation prototypes of single ESA elements:

<u>Design and characterization of a UWB microstrip ESA element at the UHF range:</u>

A single ESA element is modeled on a 1.05” thick TMM-10i substrate and characterized, via FEKO, in terms of its VSWR/S_{11}-parameter, gain, and radiation pattern.

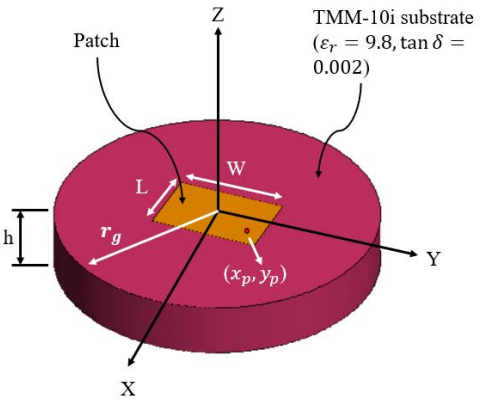


Figure 10.1.1 FEKO simulation model of the designed microstrip ESA element on a 1.05-inch-thick PEC-backed TMM-10i substrate. L = 41.3773, W = 62.066, (x_p, y_p) = (13.7924, 20.6886), r_p = 2, r_g = 106.93, h = 26.67 (all dimensions are in mm).

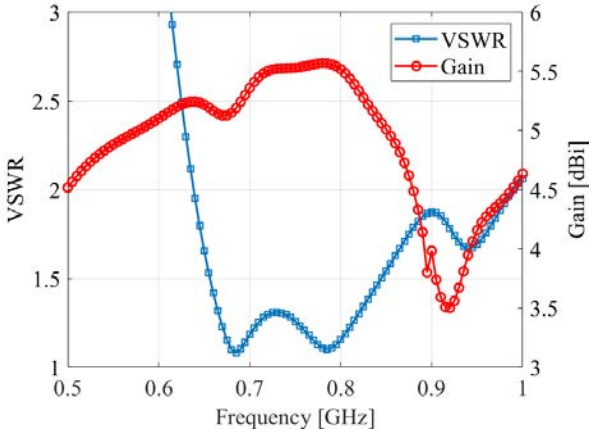


Figure 10.1.2 VSWR and gain of the designed antenna.

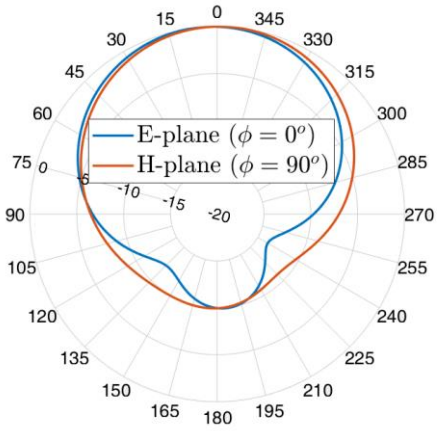


Figure 10.1.3 Normalized E-plane ($\phi = 0°$) and H-plane ($\phi = 90°$) radiation pattern of the designed antenna at the center frequency of 814.4 MHz.

(D) Optimization of ESA (single element) performance using ML algorithms:

To further improve the bandwidth of the designed microstrip ESA element (that was designed on a 1.05-inch-thick TMM-10i substrate), the size of the ground plane (r_g), the probe radius (r_p), and the probe location (x_p, y_p) are optimized using ML algorithm, via Altair HyperStudy, while keeping all other antenna dimensions constant. Using the full-wave MoM solver in FEKO, 40 input-output (X_i, Y_i) training data samples were generated. Here, $X_i = \{r_g, r_p, x_p, y_p\}$ and $Y_i = avg(S_{11}(f))$, with $S_{11}(f)$ being the S_{11}-parameter of the antenna over the frequency range, $f = 0.6 - 1$ GHz. The goal is to learn a behavioral model based on the training dataset, that best describes the relationship between design parameters X and the output Y, followed by the application of a stochastic search algorithm to optimize Y. In this case, the behavioral model is trained using the radial basis function (RBF) algorithm and then genetic algorithm (GA) is employed to minimize Y.

The initial and the optimized antenna parameters are enlisted in Table 10.1.2. Compared to the initial design, the optimized antenna has been shown to have $\approx 22\%$ reduction in the aperture area, while having $\approx 6\%$ BW enhancement, but at the cost of reduced maximum gain ($\approx 12\%$).

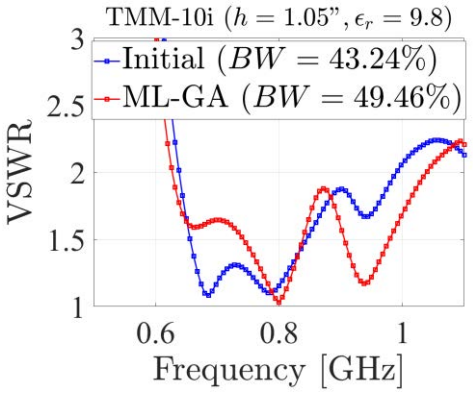


Figure 10.1.5 VSWR comparison of the initial and ML-optimized single ESA element.

Table 10.1.2 Performance comparison of the initial and the optimized single antenna element.

Antenna Design	(x_p, y_p) (mm, mm)	r_p (mm)	r_g (inch)	f_L-f_U (MHz)	BW (%)	Physical aperture area (m^2)	Max. Gain (dBi)
Initial	(13.7924, 20.6886)	2	106.93	638.2-990.6	43.24	0.0359	5.67
Optimized (GA)	(18.8665, 27.095)	1.8	94.2342	608-1025	49.46	0.0279	4.97

Future work will include multi-objective optimization (such as, minimization of average S_{11} along with gain maximization) of the ESA element using HyperStudy and Pareto optimality.

(E) Build minimum viable validation prototypes for arrays of ESA elements:

The wideband coaxial probe-fed microstrip patch ESA element design, is now integrated to form a 5×5 array.

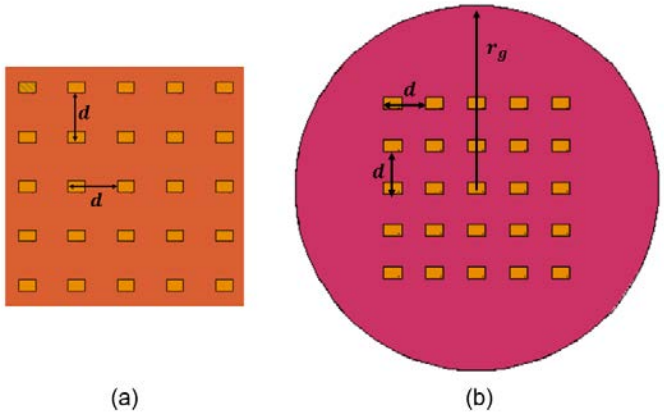


Figure 10.1.6 Geometry of the 5×5 array of ESA elements on TMM-10i substrate on (a) an infinite and (b) a finite circular-shaped (radius, $r_g = 25$") ground plane.

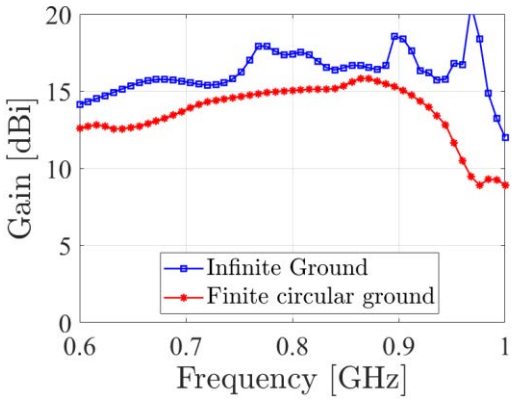


Figure 10.1.7 Gain vs. frequency of the 5×5 array having inter-element spacing $d = 0.485\lambda$ (λ is calculated at the highest frequency, 990.6 MHz).

(F) Optimization of array performances using ML algorithms:

One of the important array parameters is the mutual coupling between individual array elements. The mutual coupling affects all array parameters, such as its radiation pattern, steerability, pulse transmission capabilities, etc. Optimization of the mutual coupling between the corner-most and the center-most elements in the 5×5 array has been initiated. The results of the preliminary investigations are shown below:

Table 10.1.3 Summary of the array parameter optimization

Parameters	Description
Array antenna design	5×5 array of microstrip ESA elements on a 1.05" thick, infinite, PEC-backed, TMM-10i substrate.
Objective function	Minimization of S_{21}-parameter between center- and corner-most elements.
Optimization parameter(s)	Inter-element spacing (d)
ML algorithm	Radial Basis Function (via Altair HyperStudy)
No. of training samples	20
Search algorithm	Genetic Algorithm

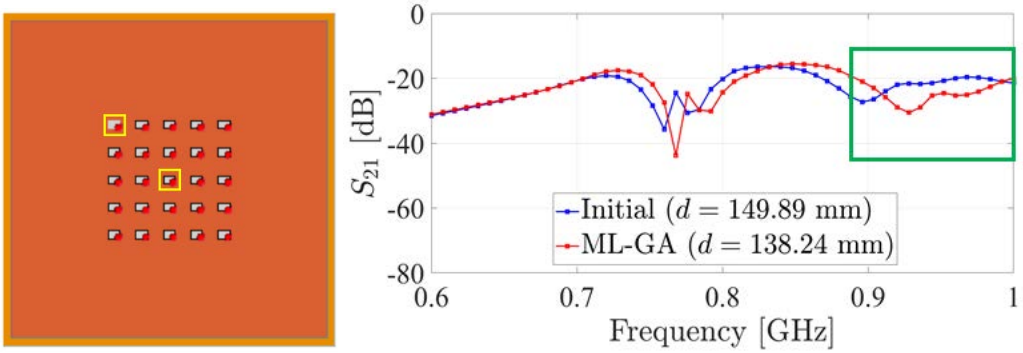


Figure 10.1.8 S_{21} between the center- and corner-most elements of the initial and the optimized 5×5 array models. (Only the two elements, marked in yellow boxes, were activated, while all other elements in the array were terminated in matched loads).

It can be observed that the mutual coupling has been reduced slightly, via optimization, only at the higher frequency end. For better improvement of the objective function, more design parameters will be considered next.

10.1.5 Summary of Significant Findings and Mission Impact

(A) Developing Array Pattern Tool for large arrays calculations:

A MATLAB code has been developed for faster approximation of the radiation pattern of a linear/planar array of any size and composed of any type of antenna elements. The code requires the center element pattern of a small array (say, 3×3) composed of the same type of antenna elements, desired lattice arrangement, and total number of array elements, as user inputs. This work will be included in future publications.

(B) Investigate the effects of array aperture area reduction on different array parameters:

The effect of different array aperture area and lattice arrangements on the array parameters (such as array gain, beamwidth, electronic beam steerability, etc.) have been reported for arrays modeled on infinite ground planes (DEC 2020 ONR-OSPRES-Grant MSR). The results show that, with 30% reduction in the aperture area ($\approx 50\%$ reduction in # of elements), the gain drops by < 3.5 dBi without any scan blindness spotted as the main beam is steered from boresight to $\pm 60°$ in the $640-990$ MHz range.

The array parameters for large arrays ($\geq 15 \times 15$) on finite ground planes could not be computed using the commercial EM solvers (FEKO and CST) due to excessive memory and time consumption. This work will be resumed after developing a method to estimate array performances on finite ground planes, either through ML or conventional approaches.

(C) Build minimum viable validation prototypes of single ESA elements:

Investigated different bandwidth enhancement techniques applicable to single layer microstrip patch ESAs:

a. Method I: Bandwidth enhancement by strategically placing the coaxial probe along 2/3rd of the patch diagonal – This method is proposed and experimentally validated using prototypes manufactured on TMM-6 and TMM-10i substrates at $2.5-5$ GHz. Antennas have been modeled on various substrates (polyethylene, G10/FR-4, TMM-10i) at the UHF range ($0.6-1$ GHz) and are being considered for manufacturing.
b. Method II: Coaxial probe-fed U-slot loaded rectangular microstrip ESAs – A prototype is manufactured on a G10/FR-4 substrate ($0.9-1.3$ GHz) and tested.
c. Method III: L-probe-fed U-slot-loaded rectangular microstrip ESAs – An antenna has been modeled on a TMM-4 substrate that operates in the $0.52-1.17$ GHz range ($\approx 77\%$ 2:1 VSWR bandwidth). Due to the fabrication complexity of the L-probe proximity coupled feed, this antenna will not be manufactured.

(D) Optimization of ESA (single element) performance using regular, and ML based stochastic search algorithms:

Investigated the bandwidth enhancement of the coaxial probe-fed microstrip patch antennas, using regular and ML based stochastic search algorithms (GA, PSO, and Simplex methods), by optimizing the feed-probe location and ground plane shape and size. Compared to regular search algorithms, ML algorithms are found to be less computationally intensive (in terms of time and memory consumption).

(E) Build minimum viable validation prototypes for arrays of ESA elements:

A 3×3 array of microstrip ESA elements, on a TMM-10i substrate, has been manufactured and tested at the $2.5-5$ GHz range. We have modeled and submitted a work order for manufacturing a 2×2 array of narrowband microstrip ESAs, on a 0.25" TMM-10i substrate, for operation at the UHF range ($0.9-1$ GHz). We have initiated modeling and characterization of a 5×5 array of wideband ESA elements for future prototyping.

(F) Optimization of array performance using ML algorithms:

Initiated investigations into the reduction of mutual coupling between individual elements in a small array (5×5) by seeking the best inter-element spacing using radial basis function algorithm.

10.2 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna

(Alex Dowell and Kalyan Durbhakula)

10.2.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: The Koshelev antenna has a unique design that is capable of generating an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic dipoles over a wide frequency range [1]. This opens up an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

Sub-Problem:

(i) The integration of impedance transformer to single element Koshelev antenna to simulate and test the combined (transformer-antenna) performance is currently not feasible using commercial EM simulators.

(ii)The total surface currents on the Koshelev antenna over the desired frequency range arising from the present positioning of TEM exponential flares, an electric monopole, and magnetic dipoles is not yet clearly understood.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the important design parameters of the Koshelev antenna array that effectively reduce its physical aperture area while maintaining its UWB properties, in both the frequency and time domains. The Koshelev antenna has been shown in the literature to withstand higher voltage levels (over 200 kV peak voltage), thereby making it a viable antenna element for detailed tradespace study and analysis.

Relevance to OSPRES Grant Objective: From the literature, it was shown that the Koshelev antenna can handle high input voltages (and therefore high power with 50 Ω input impedance), which satisfies the specific OSPRES objective related to high input voltage/power. In addition, this work can yield a center-frequency-dependent, bandwidth-controlled, and electronically steerable Koshelev antenna design that can be quickly modified to the spectrum properties of the ultra-fast rise time input pulse.

Risks, Payoffs, Challenges:

(i) The electrical size of the Koshelev antenna is approximately λ/4 at its lowest operating frequency. Further reduction of electrical size to λ/10 could considerably reduce frequency dependent gain, thereby decreasing the power spectral density.

(ii) Payoffs include the development of a library of antenna metrics data for different shapes and sizes of the individual parts within the Koshelev antenna.

(iii) The large electrical size (>5λ) of the Koshelev antenna at its highest operating frequency poses huge computational challenges.

10.2.2 Tasks and Milestones / Timeline / Status

(A) Complete literature search to identify and list antenna elements that satisfy UWB properties and HPM requirements, and down-select accordingly / NOV–DEC20 / Complete.

(B) Complete initial design, simulation, and validation of Koshelev antenna [1] / JAN21 / Complete.

(C) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area / FEB–MAR21 / Complete.

- Milestone: Using FEKO and/or CST electromagnetic (EM) simulators, reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency / Complete.

(D) Determine the full-width half-maximum (FWHM) and ringing metrics from the envelope of the time domain impulse response ($h_{rx/tx}(t, \phi, \theta)$) in receive or transmit mode / MAR–APR21 / Complete.

- Milestone: Produce a generalized code that calculates the impulse response envelope of the Koshelev antenna and plots the rate of change in FWHM and ringing values as a function of physical aperture size.

(E) Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / MAR21/ Complete.

- Milestone: Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain over the desired bandwidth, and aperture efficiency.

(F) Reduce Koshelev antenna aperture size (H×W) to equal to or less than 90 mm × 90 mm, equal to that of the SOTA BAVA, for direct antenna metrics comparison / MAR–APR21 / Complete.

- Milestone: Provide a recommendation on the optimum design parameters and the resulting metrics, with comparison to SOTA BAVA. The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, aperture efficiency equal to or greater than 130% at 900 MHz.

(G) Using the optimized model from (F), build various array simulation models/topologies to perform a tradespace study and report tradeoffs between array antenna metrics such as center element reflection coefficient (S11) value, gain vs theta at constant phi, physical aperture area, aperture efficiency, and rE/V / MAY–JULY21 / Complete.

- Milestone: Develop/showcase an optimized Koshelev array model that exceeds an aperture efficiency of 130% with a high rE/V.

(H) Perform literature search to investigate, understand, and determine the applicability of special electromagnetic (EM) techniques to the antennas under consideration. / JAN–APR21 / Complete.

(I) Explore impedance taper (microstrip based and coax based) designs that can interface well (both mechanically and electrically) to transition the signal from a coax cable to the input of the Koshelev antenna element / JULY21–AUG21 / Complete.

- Milestone: Recommend the optimum impedance taper design (with minimum reflections and maximum power transfer) with the optimum dimensions to successfully convert the high-voltage, short-rise time input signal from a coax cable to the feed of the Koshelev antenna array.

(J) Study response from optimized Koshelev antenna array when excited with different monopolar, differential, and bipolar pulse signals of significant interest **(NEW)** / AUG21–OCT21 / Ongoing.

- Milestone: Provide a table comparing the Koshelev antenna array response metrics and narrow down the suitable pulse signals. Recommend (if any) changes to the downselected pulse signal(s) that can further improve the radiation efficiency, and/or transient gain.

(K) Prototype single element Koshelev antenna and test for reflection coefficient, gain as a function of frequency, radiated electric field at 1-m, 2.5-m, 5-m and 10-m (if feasible) distances. / AUG21–DEC21 / Ongoing.

- Milestone: Report measured data and recommend any improvements to the fabrication/prototyping/testing methods.

10.2.3 Progress Made Since Last Report

(J) The Koshelev antenna array topologies (square v. diamond) have been simulated with different bipolar signals to record their time-domain electric field response and to distinguish subtle differences between the two topologies.

(K) The Koshelev antenna prototype showed in August 2021 MSR had a body thickness of 1 mm. The prototype turned out to be too thin to hold the TEM horn part of the Koshelev antenna in its place without an external support frame. This problem was solved by 3D printing the Koshelev antenna with a body thickness of 3 mm. Fig. 10.2.1 shows both thickness versions side by side.

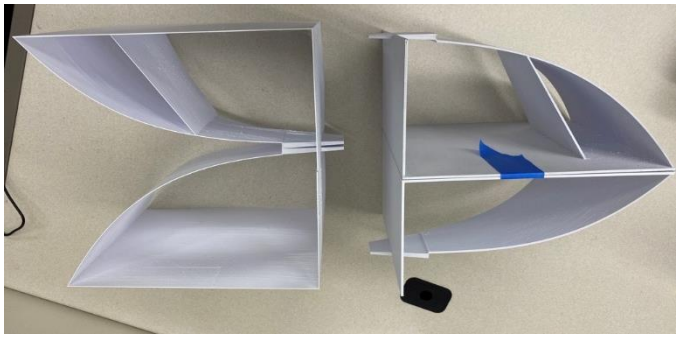
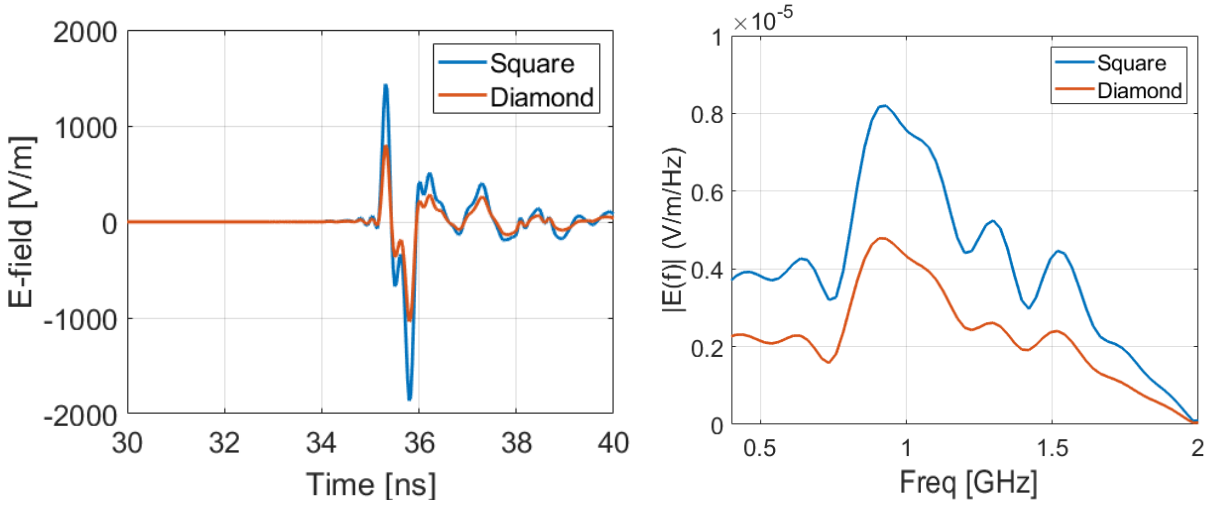


Figure 10.2.1 1 mm (left) and 3 mm (right) thickness 3D printed prototype of the Koshelev antenna with integrated linear impedance taper.

10.2.4 Technical Results

(J)

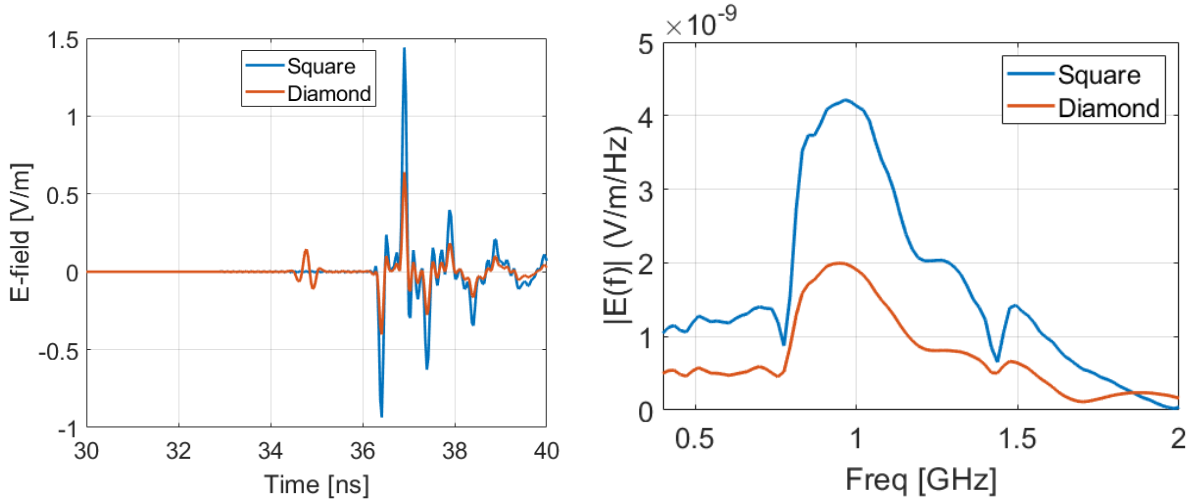
The traditional square array topology and unconventional diamond array topology were tested (using simulations) with a couple of time-domain pulses. Two bipolar signals (mega-impulse and 900 MHz damped rectangular) and a monopolar signal have been fed into the two array topologies (square and diamond). The square topology and the diamond topology consist of 9 elements and 5 Koshelev antenna elements, respectively. The far-field region for the studied topologies is estimated to start at 8 meters. Therefore, we simulated the electric field at 10 meters distance for both topologies. Fig. 10.2.2(a) shows E-field at 10 m distance for the two topologies when fed by the mega-impulse signal. The mega-impulse signal was shown in Fig. 6.2.2(a) in Aug 2021 MSR. From Fig. 10.2.2(a) and Fig. 10.2.2(b), it is evident that both topologies radiate the same frequency content, however, the diamond topology radiates with smaller peak values. Fig. 10.2.2(b) also confirms that the radiated electric field has maximum frequency spectrum around 900 MHz.



(a) (b)

Figure 10.2.2 Radiated electric field at 10 meters distance when fed with a bipolar signal. (a) Time domain electric field, and (b) Frequency spectrum of the radiated electric field.

In another study, two array topologies are excited with a 900 MHz damped rectangular waveform. The 900 MHz damped rectangular waveform can be found in Fig. 6.3.4(a) in Aug 2021 MSR. Fig. 10.2.3(a) shows the time domain radiated E-field at 10 m distance from the aperture of the array for the two array topologies. Consistent with Fig. 10.2.2 observations, the electric field from the diamond topology yielded a lower peak value than the electric field from the square topology. Fig. 10.2.3(b) shows the frequency spectrum for the radiated E-filed for two topologies. It is also clear that both topologies can effectively radiate the 900 MHz damped rectangular waveform without any distortion.



(a) (b)

Figure 10.2.3 Radiated electric field at 10 meters distance when fed with a 900 MHz input signal. (a) Time domain electric field, and (b) Frequency spectrum of the radiated electric field.

In addition, a frequency-dependent gain study is carried out when excited by different pulse signals. As mentioned above, two bipolar signals and one monopolar signal have been used for this study. Fig. 10.2.4(a) and Fig. 10.2.4(b) are excited by different bipolar signals, however, they yield the same response from both topologies. There are subtle differences in the off-boresight region despite having similar peak gain values for the two pulse signals and two topologies. On a closer comparison, one can identify that Fig. 10.2.4(b) has lower sidelobe levels when compared against sidelobe levels in Fig. 10.2.4(a). On the other hand, Fig. 10.2.4(c) yields an interesting response when excited by a monopolar pulse. The square topology radiated a lower peak E-field value than the diamond topology despite the latter having a fewer number of elements. An in-depth analysis is required to confirm these results.

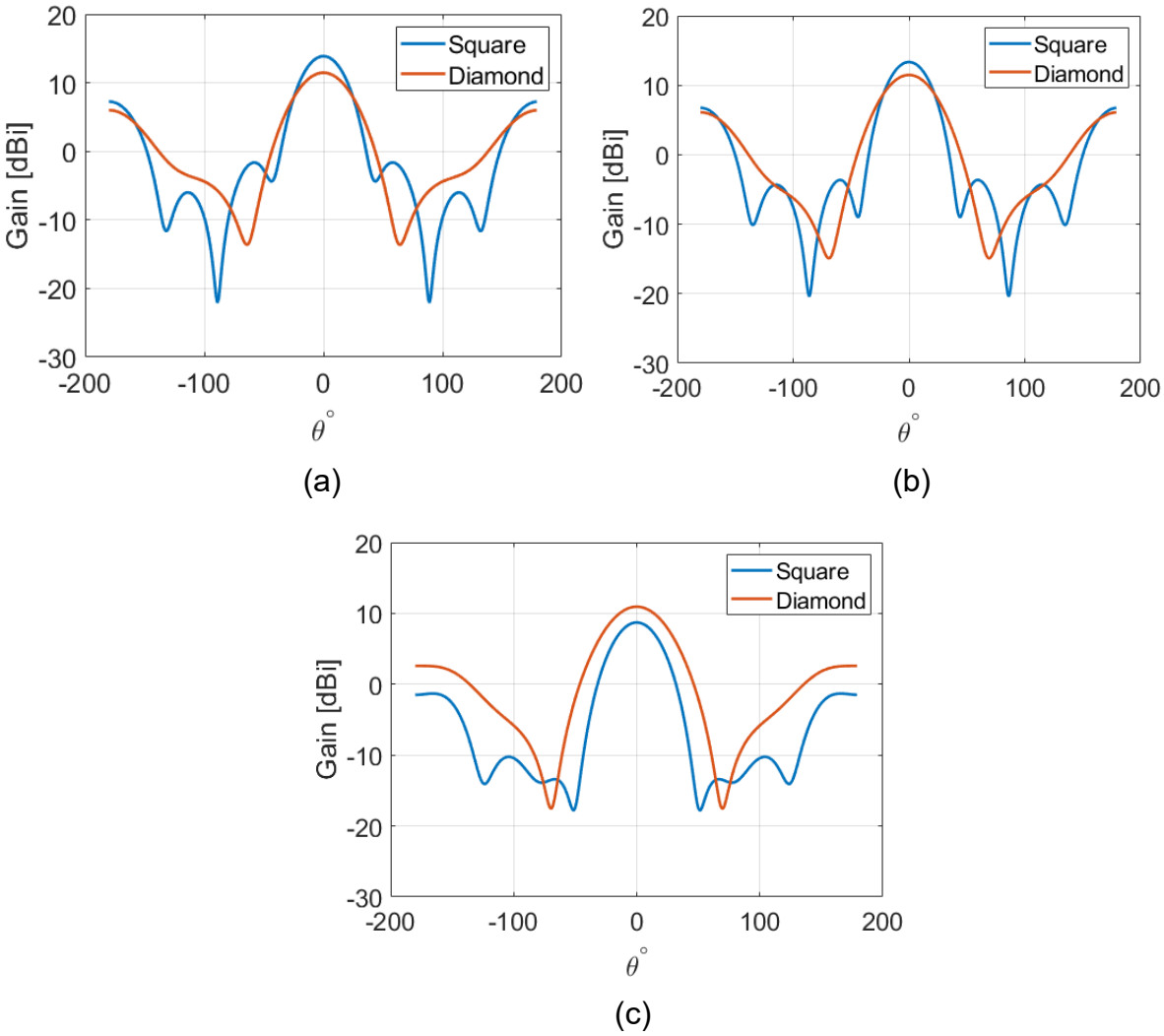


Figure 10.2.4 Gain as a function of elevation angle for (a) Bipolar signal, (b) 900 MHz signal and (c) Monopolar signal with > 1 ns rise time.

10.2.5 Summary of Significant Findings and Mission Impact

(A) An extensive literature search on various UWB antenna elements has resulted in finding three promising options. The down-selected elements are the Koshelev, Shark, and Fractal antennas, which will be extensively studied using their individual design parameter space, which could result in physical aperture area reduction of the single antenna element. Later, the single antenna element will be converted into a planar array.

(B) Initial validation of the Koshelev antenna simulated using CST software agreed well with the antenna metrics published in the open literature [1]. A UWB bandwidth response (10:1 bandwidth) and rE/V > 1 has been observed from our initial simulations of the Koshelev antenna. This validation ensured that the Koshelev antenna can be subjected to further tradespace studies to understand its

performance followed by optimizing the design according to OSPRES grant requirements.

(C) The initial tradespace study and analysis of the Koshelev antenna design yielded promising outputs to carry forward the investigation. A comparison of important antenna metrics between the Koshelev antenna in [1] and aperture reduced Koshelev antenna are shown in Table 5.2.1 of the APR 21 MSR.

(D) An in-house code has been developed to calculate important UWB time domain antenna metrics such as full-width half maximum (FWHM) and ringing. These metrics have been calculated using in-house MATLAB code using the excitation voltage and radiated electric field information obtained from CST simulations. FWHM and ringing antenna metrics help with assessing or characterizing an antenna's UWB response.

(E) The tradespace study of feed position provided a deeper understanding of how its position impacts the S11 value bandwidth. An optimum value for feed position i.e., $F = 1/20 < L < 1/10$ is recommended to achieve maximum bandwidth. The tradespace study of the antenna length (L) is straightforward. A longer antenna length will radiate better at lower frequencies. However, physical size restrictions/requirements must be kept in mind in determining the antenna length. Finally, a larger α value (>120°) is recommended to avoid unnecessary reflections from the electric monopole.

(F) From a thorough tradespace study, the aperture size of the Koshelev antenna (single element) is determined to be 90 mm × 100 mm in order to achieve desired antenna metrics performance proposed in the milestone. All metrics described in the milestone have been successfully achieved except the desired bandwidth (200 MHz on both sides) at 900 MHz center frequency. The bandwidth achieved is 900 ± 100 MHz.

(G) The physical aperture area of the Koshelev array antenna largely depends on the interelement spacing and the shape of the array. We were able to determine that the diamond topology is the optimum shape for the Koshelev array antenna. Moreover, with the diamond Koshelev array, by making only element#3 passive we were able to obtain similar gain characteristics when compared against gain characteristics from all elements active case. From the non-symmetric interelement spacing values, we found that S_y has least effect on the output, therefore a small spacing value can be chosen to reduce the physical aperture area of the Koshelev array.

(H) The literature search on the special EM techniques expanded our knowledge and opened the door to opportunities to apply some of those techniques to the antennas under study. EM techniques such as non-symmetric and non-square array topologies have been applied to the development and study of the Koshelev array antenna.

(I) The first impedance taper design under consideration has shown good S11 values (< -10 dB) over the frequency range of interest. In addition, we have shown that the shape of the pulse can be easily retained at the output of the taper with less than 5% amplitude losses.

(J) The Koshelev antenna array response from feeding a monopolar vs bipolar signal has demonstrated a clear winner: that is, a bipolar signal will radiate at least 10 times better than a monopolar signal.

10.2.6 References

[1] Gubanov, V. P., et al. "Sources of high-power ultrawideband radiation pulses with a single antenna and a multielement array." *Instruments and Experimental Techniques* 48.3 (2005): 312-320.

10.3 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna

(Kasey Norris and Kalyan Durbhakula)

10.3.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of Shark antenna elements with an emphasis on inter-element and intra-element spacing effects is a good candidate for UWB HPM systems while having a reduced aperture area with respect to the current state-of-the-art. In the literature, the Shark antenna has already been shown to achieve a wide 20:1 impedance bandwidth, low dispersion, and a sectoral (also referred to as directional) radiation pattern.

Sub-Problem: The design parameter space of the Shark antenna has not been studied rigorously in the literature and therefore the effect of these parameters on the antenna metrics is not understood. In addition, the Shark antenna has been shown to be not very directive in the H-Plane. Preliminary studies have shown that aperture efficiencies at low frequencies are much better than at higher frequencies.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Explore the array tradespace by generating different array topologies/lattices (hexagonal, octagon, square, elliptical) and with different intra and interelement spacing combinations.

Relevance to OSPRES Grant Objective: The Shark antenna dimensions were established to be frequency dependent and can be readily modulated to fit the spectrum characteristics of an ultra-fast rise time input pulse.

Risks, Payoffs and Challenges:

(i) The Shark antenna is comprised of flare-angle-dependent bicones that are truncated in the azimuthal angle. This still yields considerably higher half power beam width

(HPBW) than other antenna elements under investigation. The significant reduction of HPBW in the H-plane may be unattainable and can be considered a major risk.

(ii) Payoffs include the development of a library of antenna metrics data for various shapes and sizes of the bicones and reflector plates in the shark antenna.

(iii) Computational challenges remain present with respect to automation of design parameter space on our currently used supercomputer (LEWIS). Design challenges persist in obtaining lower operating frequencies while not increasing the height of the antenna and surpassing the 90 mm × 90 mm size requirement.

10.3.2 Tasks and Milestones / Timeline / Status

(A) Complete initial design, simulation, and validation of the Shark antenna / JAN21 / Complete.

(B) Validate Shark antenna design using the LEWIS supercomputer over a wider range of frequency results (up to 20 GHz) / FEB–MAR21 / Complete.

(C) Identify Shark antenna design parameters which contribute significantly to bandwidth, gain, and physical aperture area. Determine which parameters contribute most to performance improvement/size reduction/ FEB–MAR21 / Complete.

(D) Perform a tradespace study by simulating the Shark antenna with varying cases of flare angle, cone length, and distance to backplane. Gain a general understanding of how these parameters affect impedance bandwidth, rE/V, gain and HPBW / FEB–MAY21 / Complete.

- Milestone: produce a detailed summary of change in impedance bandwidth, rE/V, HPBW in H-plane and E-plane as a function of flare angle (α), cone height (*h*), and distance to backplane (*d*) / Complete.
- Milestone: Choose optimal Shark antenna design that has the lowest operating frequency within size requirements based on tradespace study / Complete.

(E) Using the optimal Shark antenna design in (D), simulate various array geometries including hexagonal, rectangular, and circular arrays. Determine which array geometries are optimal and analyze aperture fields and aperture efficiencies. / MAY–SEP21 / Ongoing.

- Milestone: Produce a report which states the effects of various array geometries for the Shark antenna. The optimal array geometry chosen should have the least interference between elements, therefore yielding higher impedance bandwidth and higher aperture efficiency. Overall, the optimal Shark array geometry should have at least 20% impedance bandwidth at 900 MHz center frequency for the centermost element with 130% array aperture efficiency, ± 60 degrees beam steering capability, and rE/V equal to or greater than 4.

(F) Begin prototyping and validation of optimal Shark antenna single element. / JUN–OCT21 / Ongoing.

- Milestone: have a finished Shark antenna prototype. Compare S11 and radiation pattern with simulated Shark antenna.

10.3.3 Progress Made Since Last Report

(E) Over the September month, three specific Shark antenna array topologies were considered for time-domain pulse Tradespace studies. These topologies are square (3 x 3), hexagonal (8-elements), and elliptical (8-elements). These topologies were excited using two bipolar signals (mega-impulse and damped rectangular) and a monopolar signal. The study is carried out first in the time domain and later in the frequency domain at the specific 900 MHz desired center frequency.

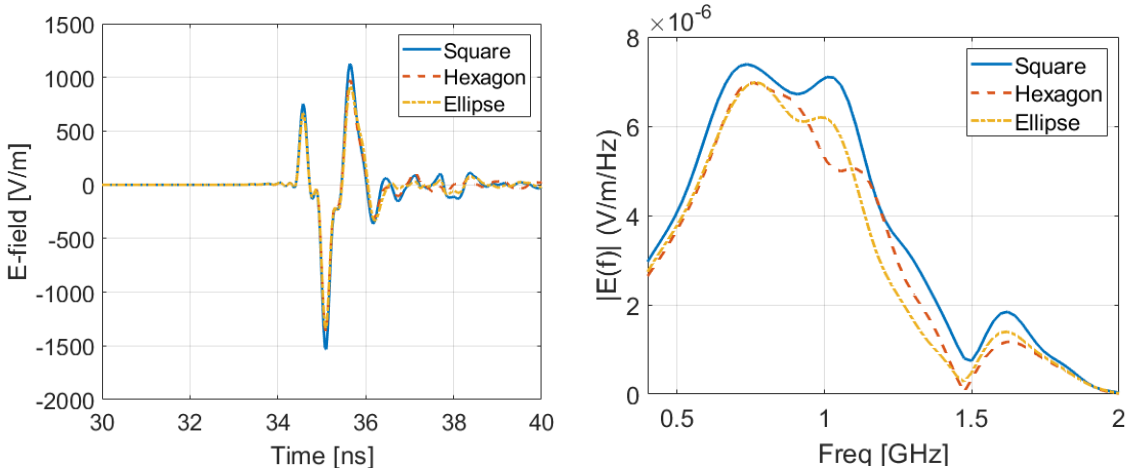
(F) Previous Shark antenna prototype had a thinner center conductor (0.161 mm) diameter at the 150 Ω end. The 0.161 mm center conductor diameter made fabrication and integration a challenging task. Therefore, we modified the center conductor diameter by considering hollow vacuum inside cones as the dielectric. The resultant center conductor diameter is around 0.5 mm. A new prototype was fabricated with the new center conductor.

10.3.4 Technical Results

(E)

In this report, we present the electric (E) field responses at 10 meters distance. Simulations yielded the E-field at 10 meters distance for three topologies of interest and, the topologies are excited by different time-domain input pulses. Fig. 6.2.2(a) in Aug 2021 MSR shows the mega-impulse bipolar signal and, Fig. 6.3.4(a) in Aug 2021 MSR shows the 900 MHz damped rectangular waveform.

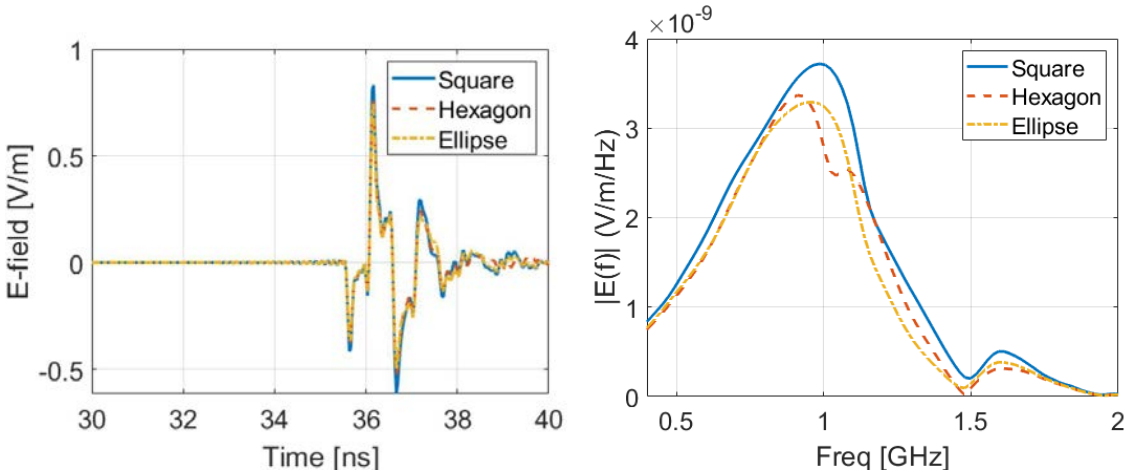
Fig. 10.3.1 shows the time domain E-field response at 10 m and its corresponding frequency spectrum when the three array topologies are excited by a mega-impulse bipolar signal. From Fig. 10.3.1(a), it is evident that square topology has the highest peak field values followed by hexagonal and elliptical. Furthermore, the frequency spectrum is spread evenly from 750 MHz and 1 GHz.



(a) (b)

Figure 10.3.1 Radiated electric field at 10 m distance from three array topologies when excited by mega-impulse bipolar signal (a) E-field in time domain and (b) Frequency spectrum of E-field.

Fig. 10.3.2 shows the time-domain E-field at 10 m and its corresponding frequency spectrum for the three array topologies excited by the 900 MHz damped rectangular signal. As predicted, the square topology yields a peak E-field value. The frequency spectrum of square and elliptical topologies in Fig. 10.3.2(b) shows a minor deviation with a peak around 1 GHz, while the hexagonal topology radiates much closer to 900 MHz.



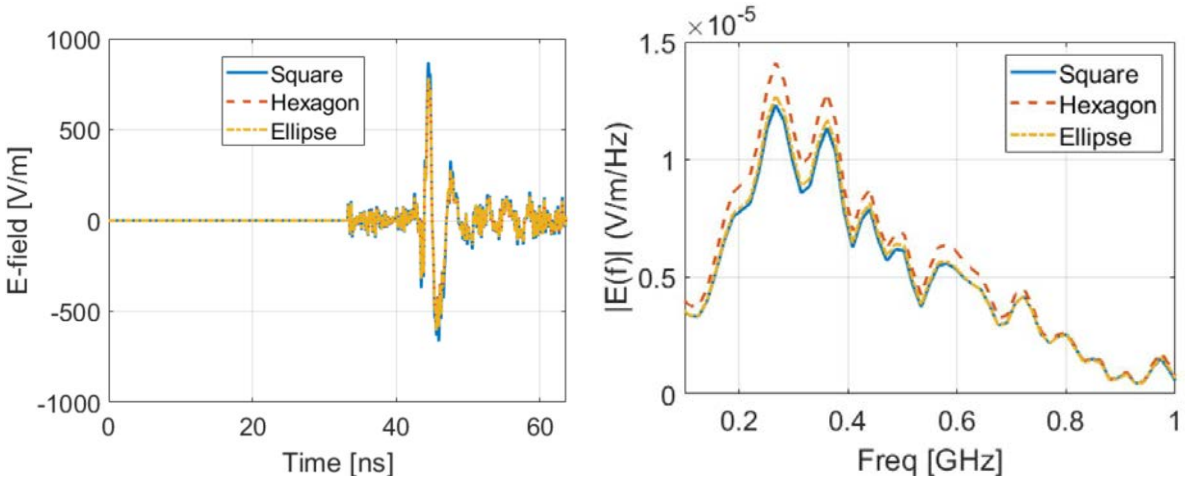
(a) (b)

Figure 10.3.2 Radiated electric field at 10 m distance from three array topologies when excited by the 900 MHz damped rectangular signal (a) E-field in time domain and (b) Frequency spectrum of E-field.

In addition to bipolar signals, a monopolar signal has also been fed to three array topologies. Fig. 10.3.3(a) shows the E-field at 10 m from the aperture of the arrays. Since an antenna cannot radiate a monopolar signal, the antenna feed tries to create a zero-potential difference by effectively converting it into a bipolar signal. This bipolar signal is radiated by the antenna but with a degraded radiation efficiency or electric field strength. Fig. 10.3.3(b) shows the frequency spectrum of the radiated E-field at the 10 m distance. Although there is minimum DC content, the antenna still tries to radiate the pulse at lower microwave frequencies. The peak E-field spectrum is around 300 MHz with little spectrum content around 900 MHz. Another interesting observation from Fig. 10.3.3(b) is that the hexagonal array topology has higher spectrum content than the other two topologies. More simulation study is necessary to validate Fig. 10.3.3(b) result. The array topologies will be excited with different monopolar signals. However, the rE/V would be smaller for any antenna from exciting it with a monopolar versus a bipolar signal.

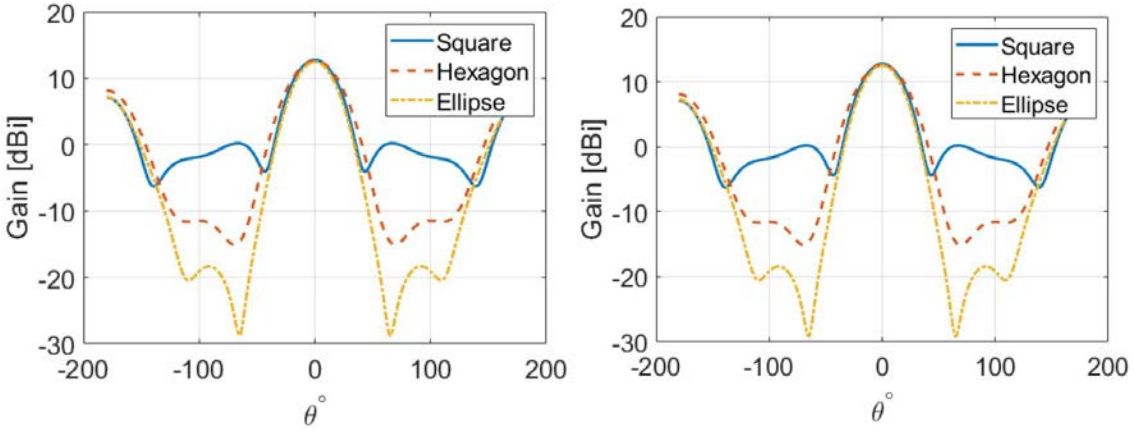
The decrease in gain value going from a bipolar input signal to a monopolar input signal can be further analyzed using Fig. 10.3.4 results. Gain as a function elevation angle results at 900 MHz are shown in Fig. 10.3.4. In Fig. 10.3.4, Fig. 10.3.4(a) and, Fig. 10.3.4(b) are the gain patterns at 900 MHz when excited by mega-impulse signal and

damped rectangular signal, respectively. It is evident from these two results that the peak gain is around 12.5 dBi. Furthermore, the elliptical topology has significantly lower sidelobe levels (almost 20 dB less than square topology) while having a similar peak gain value. In Fig. 10.3.4(c), array topologies are excited by the monopolar signal, which resulted in a decrease in peak gain value from 12.5 dBi to 10 dBi. In conjunction, the sidelobe levels remain small for an elliptical topology with at least 25 dBi less than the square topology.

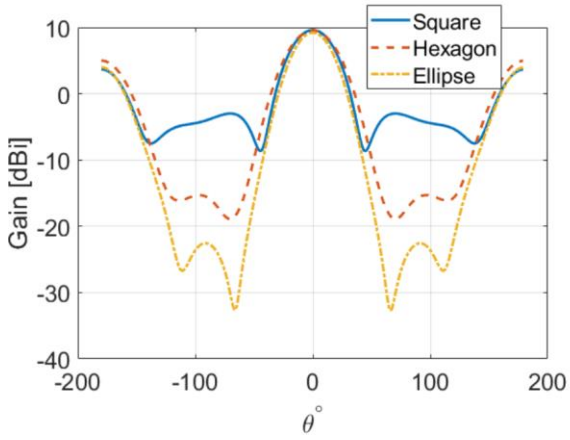


(a) (b)

Figure 10.3.3 Radiated electric field at 10 m distance from three array topologies when excited by the monopolar signal (a) E-field in time domain and (b) Frequency spectrum of E-field.



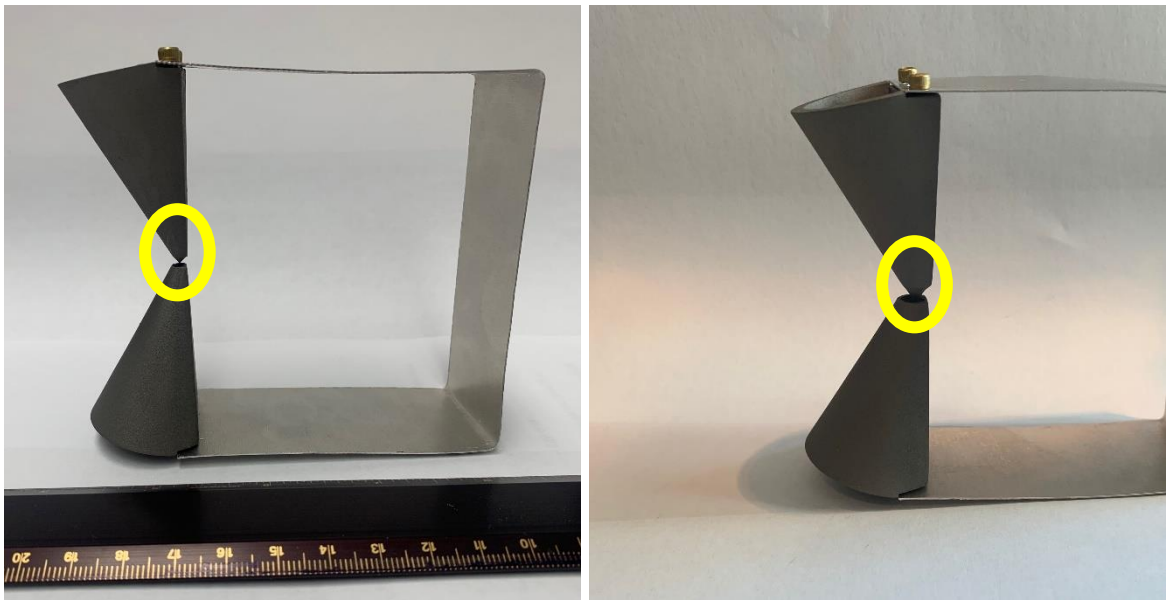
(a) (b)



(c)

Figure 10.3.4 Gain as a function of elevation angle at 900 MHz for three array topologies when excited by (a) Mega-impulse (b) 900 MHz damped rectangular and (c) Monopolar.

(F) The new prototype with increased center conductor diameter can be seen in Fig. 10.3.5(b) whereas Fig. 10.3.5(a) shows the initial center conductor diameter. Overall, a thicker center conductor provides improved structural rigidity, balance and yields better RF performance.



(a) (b)

Figure 10.3.5 Shark antenna prototype (a) 0.161 mm center conductor, and (b) 0.5 mm center conductor.

10.3.5 Summary of Significant Findings and Mission Impact

(A-B) The Shark antenna has been designed, simulated, and validated according to [1]. (Figure 6.3.1)

(C) The Shark antenna design parameters that have been found to contribute significantly to bandwidth performance, directivity, and gain are the cone height (*h*) and distance to backplane (*d*).

(D) The Shark antenna tradespace study has been completed and has provided insight into the Shark antenna design space. Increasing the cone height *h* yields better impedance bandwidth at low frequencies and is more directive in the *e* and *h* planes. However, increasing *h* results in a larger aperture area. To remain within 90 x 90 mm, the maximum *h* value is 45 mm; with this a lowest operating frequency of 815 MHz is achievable.

(E) The elliptical Shark antenna has the optimum metrics, which can be found in Table 6.3.1 in July 2021 MSR. The metrics from elliptical Shark antenna are closer to desired metrics provided in milestone 6.3.2 (E). The interelement spacing variable study has provided insight into the workings of Shark antenna array. The Shark antenna array is more sensitive to the interelement spacing variable in x-axis than in the y-axis. The elliptical topology has significantly smaller sidelobe level values and similar frequency-domain gain or transient gain values when compared against square and hexagonal topologies. If the input is a monopolar signal, a hexagonal or an elliptical topology is preferred. If the input is a bipolar signal, an elliptical topology is recommended for its decent transient gain value with significantly smaller sidelobe levels.

10.3.6 References:

[1] L. Desrumaux, A. Godard, M. Lalande, V. Bertrand, J. Andrieu and B. Jecko, "An Original Antenna for Transient High Power UWB Arrays: The Shark Antenna," in IEEE Transactions on Antennas and Propagation, vol. 58, no. 8, pp. 2515- 2522, Aug. 2010, doi: 10.1109/TAP.2010.2050418.

10.4 Machine Learning Inspired Tradespace Analysis of UWB Antenna Arrays

(Sai Indharapu and Kalyan Durbhakula)

10.4.1 Problem Statement, Approach, and Context

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. Their high degree of freedom provides an opportunity to develop systematically modified patch shapes, which in turn leads to improved bandwidth while retaining high fidelity factor values. Machine learning (ML) can be leveraged to predict the antenna array response for an arbitrary design parameter space upon sufficient training and validation.

Sub-Problem:

(i) Fractal antennas generate omni-directional radiation patterns in the H-plane over the desired frequency range.

(ii) ML can suffer from underfitting or overfitting the training model which in turn leads to deviations in the predicted output.

(iii) “can you add the .out file extraction problem here that is intrinsic to Altair hyperstudy/CADFEKO?”

State-of-the-Art (SOTA): Conventional full-wave EM solvers such as method of moments (MoM), multi-level fast multipole method (MLFMM), finite element method (FEM), and finite difference time domain (FDTD) method are currently being used to study, analyze and assess the performance of UWB antennas.

Deficiency in the SOTA: UWB antenna optimization using conventional EM solvers utilizes significant computational time and memory resource.

Solution Proposed:

(i) Design, simulate, validate, and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

(ii) Train, validate, test and compare multiple ML models for quicker and accurate prediction of antenna array response for different physical aperture areas.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omni-directional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations with respect to specific fractal shapes could arise after performing a certain number of iterations to further improve the bandwidth.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Achieving gain stability over the desired frequency range can be a significant challenge.

10.4.2 Tasks and Milestones / Timeline / Status

(A) Perform tradespace analysis of the fractal element radius *b* over the desired frequency range (4 to 12 GHz) using the genetic algorithm (GA) optimization tool available in the commercial electromagnetic (EM) solver FEKO / FEB21 / Complete.

- Milestone: Provide a recommendation of an optimum value of *b* using OPTFEKO to minimize reflection coefficient or S11 (< –10 dB).

(B) Perform tradespace study on different fractal shapes by changing the number of fractal segments to understand the effect of this change on the impedance bandwidth / FEB21 / Complete.

- Milestone: Produce a detailed study of the antenna response such as S11, gain, and bandwidth by varying the number fractal segments.

(C) Apply the GA optimization tool on the fractal side length *b* over a wide frequency range (2 to 12 GHz with 201 discrete frequency points) and number of fractal segments using OPTFEKO on the LEWIS cluster / MAR21 / Complete.

- Milestone: Reduce physical aperture area by 10% of its present design, reported in the FEB MSR, and demonstrate minimal or no change in S11, gain, and fidelity factor values.

(D) Perform a parametric study and analysis of antenna response by varying hexagon radius, *a* / MAR–APR21 / Complete.

- Milestone: Recommend a value of *a* to reduce the physical aperture area and increase aperture efficiency (>50%) with no variation in other antenna metrics.

(E) Frequency scale fractal antenna design such that the center frequency of the resulting antenna equals 1.3 GHz / MAY21 / Complete.

- Milestone: Modify antenna design with a center frequency equal to 1.3 GHz and achieve similar results (3:1 bandwidth at fc = 1.3 GHz, 3 dBi gain and >130% aperture efficiency at 900 MHz) to antenna design at center frequency ~7 GHz.

(F) Design and simulate various array antenna geometries composed of optimized fractal antenna elements (obtained from (E)) to analyze the effect of overall array antenna geometry on the desired array antenna response metrics (i.e., gain vs. frequency, gain vs. elevation angle at constant phi, rE/V, half-power beamwidth and side-lobe level.) / MAY–JUL21 / Complete

- Milestone: Recommend a best possible structure with reduced aperture area and minimal loss in gain.

(G) Apply ML models available in Altair Hyperstudy (2021) on the fractal antenna to try and understand the possibilities and limitations of ML models for fast and efficient antenna metrics prediction and optimization. Through successful testing, a ML model can replace conventional EM simulators for faster optimization and prediction. / MAY–OCT21 / Ongoing.

- Milestone: Recommend most accurate and efficient ML model available in Altair Hyperstudy (2021) for a fractal antenna.

(H) Apply ML models on the octagon fractal antenna array lattice to extend the prediction capabilities of ML models. / SEP–NOV21 / Ongoing.

- Milestone: Recommend the best suitable ML model available in Altair Hyperstudy(2021) for array antenna metrics prediction.

10.4.3 Progress Made Since Last Report

(G) In the last month, ten random combinations of *a* and *b* parameter values over the following range: a (39 mm to 42 mm) and b (7 mm to 7.5 mm) were used to generate the training data for training the ML models. To test the accuracy of trained ML models, each ML model is tested with five random pairs of *a* and *b* values, which are outside the training data range. The a and b pair values are shown in Table 10.4.1. In addition, Fig. 10.4.1 shows the positioning of each pair. The red dot in Fig. 10.4.1 represents the mid-point value of the training range, which is *a* = 40.5 mm and *b* = 7.25 mm.

Table 10.4.1: Test data.

	Pair-1 (d1)	Pair-2 (d2)	Pair-3 (d3)	Pair-4 (d4)	Pair-5 (d5)
a (mm)	38.5	43.5	36.5	45.5	34.5
b (mm)	6.75	8	6.25	8.50	5.75

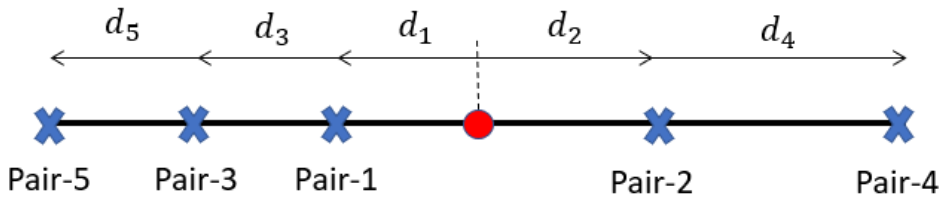


Fig 10.4.1: Illustrates each pair is at distance d from the center of training data.

10.4.4 Technical Results

(G) Figs. 10.4.2, 10.4.3, and 10.4.4 shows reflection coefficient (S11 values), gain, and electric field responses as a function of frequency calculated using traditional FEKO solver and predicted using trained RBF and LSR ML models. In total, five different pairs comprised of random *a* and *b* values were used as input variables to test the accuracy of trained ML models. In addition, the models were also applied on a combination of *a* and *b* values within the training range. On close observation of results in Figs. 10.4.2(a)-(e), 10.4.3(a)-(e), 10.4.4(a)-(e), one can notice that the accuracy of RBF and LSR ML models gradually decreased as the pair value moved

away from the mid-point of the training data. Pair-1 is the closest to the mid-point while pair-5 is the farthest. We can notice from Fig. 10.4.2(a) to Fig. 10.4.2(e) that both RBF and LSR ML models are moving away from the FEKO result. The same observation can be applied to Figs. 10.4.3(a)-(e) and Figs. 10.4.4(a)-(e). It is important to note that only ten samples have been used for training the ML models. The presented results and analysis can be helpful to understand the limitations of the trained ML models. Figs. 10.4.2(f), 10.4.3(f), 10.4.4(f) have better accuracy than the other five plots as the test data used to generate output response is within the training range.

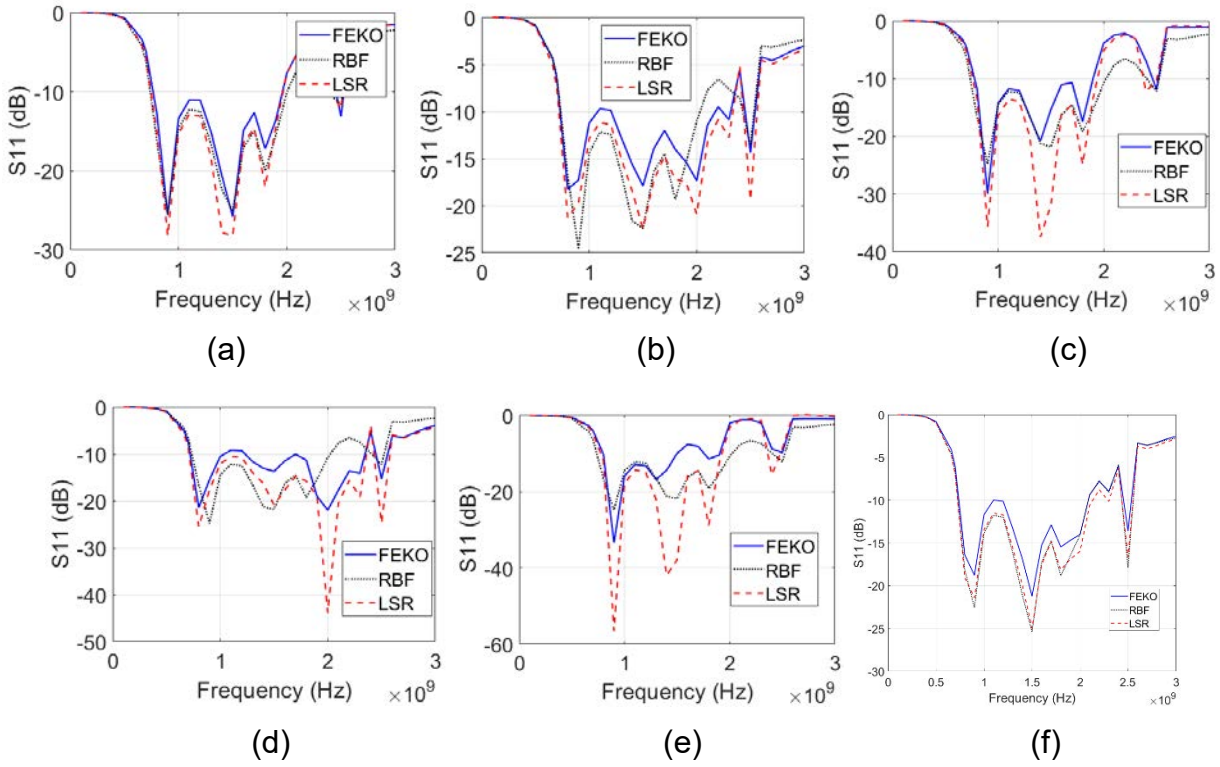
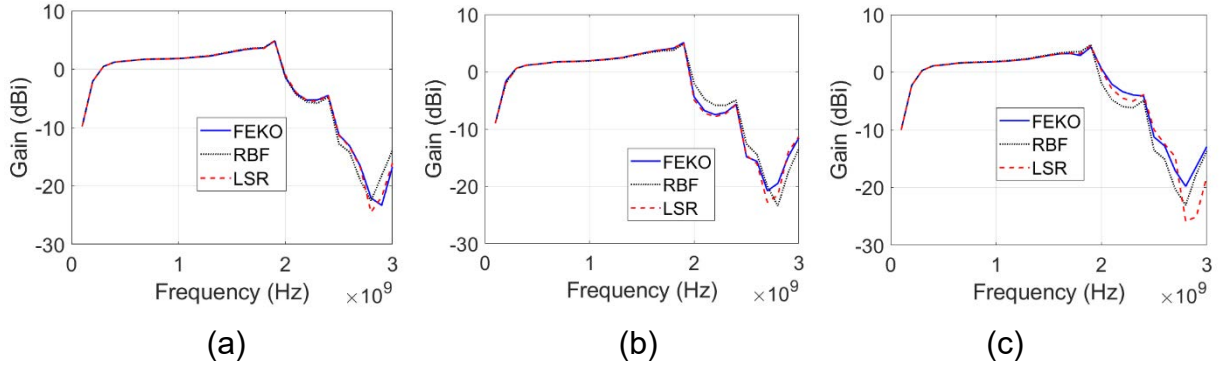
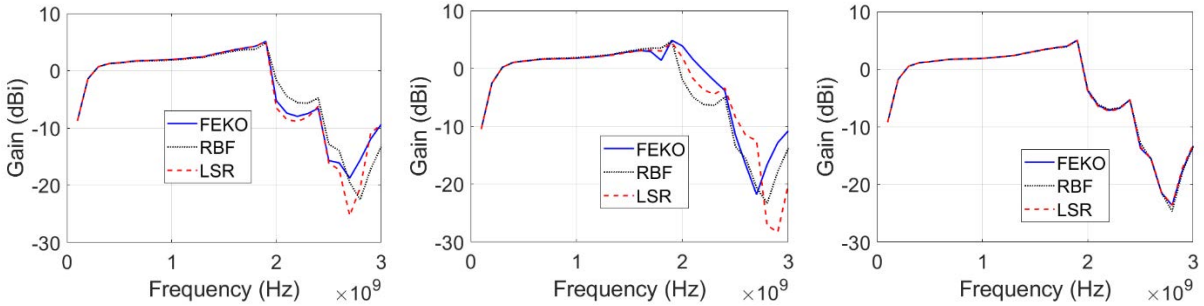


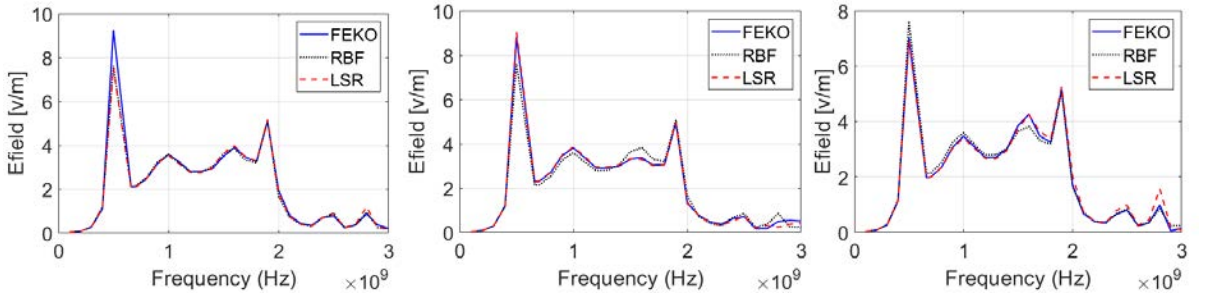
Figure 10.4.2: Comparison of S11 response from FEKO, RBF, and LSR for (a) pair-1, (b) pair-2, (c) pair-3, (d) pair-4, (e) pair-5, (f) test input within the training range.



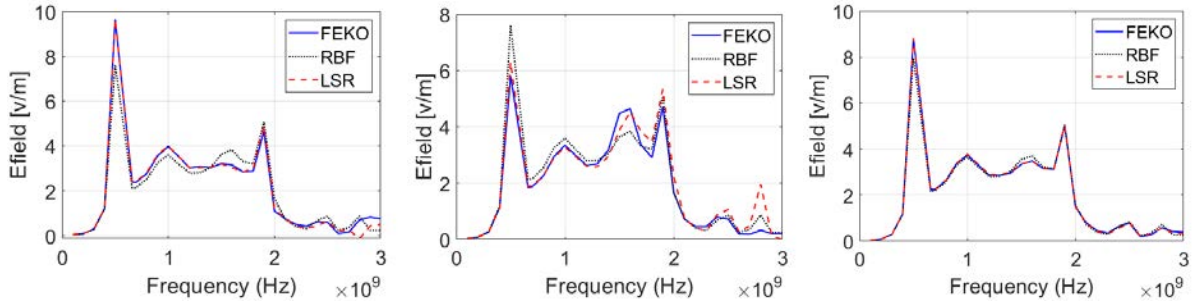


(d) (e) (f)

Figure 10.4.3: Comparison of Gain response from FEKO, RBF, and LSR for (a) pair-1, (b) pair-2, (c) pair-3, (d) pair-4, (e) pair-5, (f) test input within training range.



(a) (b) (c)



(d) (e) (f)

Figure 10.4.4: Comparison of E-field response from FEKO, RBF, and LSR for (a) pair-1, (b) pair-2, (c) pair-3, (d) pair-4, (e) pair-5, (f) test input within the training range.

RMSE values are calculated for S11, gain and E-field predicted using RBF and LSR ML models with the FEKO result being the reference result. The RMSE values increased with an increase in the distance of test data from the mean of training data. From Figure 10.4.5, RBF is always below LSR in the case of S11 while LSR has better RMSE in predicting the gain and E-field. Overall, the RMSE exponentially increased with an increase in distance from the training data.

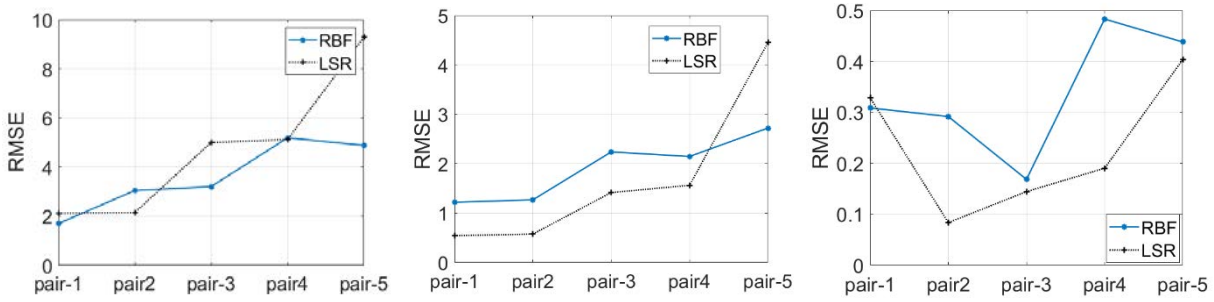


Figure 10.4.5: Comparison of RMSE values between RBF and LSR models for (a) S11, (b) Gain, (C) E-field predictions.

10.4.5 Summary of Significant Findings and Mission Impact

(A) The initial analysis of the simulation results with fractal radius *b* equal to 1.8 mm yielded multiple resonant frequencies with enhanced bandwidth. To further increase the bandwidth, OPTFEKO has been used as an optimization tool with fractal radius *b* as the optimization variable. The optimum value for *b* is found to be 1.66 mm. A comparison between reflection coefficient for initial *b* (= 1.8 mm) value and the optimized *b* (= 1.66 mm) can be found in Figure. 6.4.6. The optimization is carried out over 51 discrete frequency points.

(B) The addition of fractal elements (*N*) to the simple hexagon improved antenna metrics such as S11. To further investigate and understand the fractal elements, the number of segments in the fractal geometry has been varied. The improvement in bandwidth is observed as the value of *N* is increased from 6 to 14.

(C) The initial optimum value of *b* over 51 discrete frequency points is reported as 1.66 mm in task (A). To further increase the accuracy of the optimization algorithm and to find a more precise value for *b*, optimization is further performed over wider frequency points (201 discrete points between 2 GHz to 12 GHz) which yielded the optimum value of b as 1.368 mm. The S11 response of antenna design with newly found *b* (i.e., 1.368 mm) hasn't produced any better bandwidth with respect to *b* (= 1.66 mm). Thus, *b* is set to be 1.66 mm for further research.

(D) The hexagonal patch radius *a* has a significant effect on the physical aperture area of the antenna. Therefore, Altair OPTFEKO has been utilized to find an optimum *a* value, which was found to be 8 mm over the range 7.2 to 9 mm. Antenna metrics such as S11, gain, and bandwidth have shown desired performance with the optimized *a* value.

(E) The initial antenna design has been modified to achieve a center frequency of ~1.3 GHz. The gain value at 900 MHz is 3.5 dBi and, with the modified antenna design, we were able to achieve an impedance bandwidth ratio of 3.3:1. The designed antenna has been fabricated and tested, and the S11 response of the fabricated antenna agrees well when compared against FEKO, CST.

(F) To summarize, four different fractal antenna array geometries (i.e., square, diamond, hexagon, and octagon) have been designed and simulated. Upon comparing antenna array metrics, octagonal fractal antenna array has yielded minimal sidelobe levels with a gain of 15.7 dBi at 900 MHz close to that of square geometry with 32.27% lower physical aperture area than that of square geometry. The octagonal fractal antenna array has been chosen as the optimum geometry with reduced aperture area and reduced side lobes while retaining the bandwidth and gain milestone metrics.

(G) Radial basis function (RBF) and Least square regression (LSR) were down-selected from the initial three ML models based upon their generalization capability for prediction of reflection coefficient (S11), gain, and electric field. Further analysis of increasing training data set size has shown no improvement in prediction accuracy. Trained ML models were tested for design variable values outside the training range. The resulting RMSE increased as the values drifted away from the mid-point of the training range. RBF performed well in the prediction of S11, while LSR performed slightly better for gain and electric field predictions.

10.4.6 References

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

11.0 RF Coupling

11.1 Enclosure Effects on RF Coupling

(Mohamed Hamdalla and Ahmed Hassan)

11.1.1 Problem Statement, Approach, and Context

Primary Problem: UAVs are typically considered metallic/dielectric enclosures depending on their frame material. The shielding effectiveness of such enclosures might be compromised due to the slots and gaps on these enclosures, creating upset susceptibility to the enclosed electronics. The goal of this work is to quantify how the thresholds for upset susceptibility of enclosed wires and integrated circuits differ from those in free space.

Solution Space: Study enclosures with different shapes, material compositions, and slots to quantify their effect on RF coupling to the enclosed wires and electronics typically used in UAVs. The study will focus on the low-frequency range where the incident wavelength is comparable to the size of the enclosure or larger.

Sub-Problem: UAVs are manufactured with a wide variety of shapes and composites to accomplish an exponentially expanding list of missions. The configurations previously reported in the literature have simplistic assumptions regarding the shape and material composition of UAV enclosures that might overestimate or underestimate susceptibility.

State-of-the-Art (SOTA): Simple statistical analysis of specific enclosure configurations using either brute force simulations/measurements or pure statistical methods. Also, simplified UAV wire distributions are assumed.

Deficiency in the SOTA: Brute force simulations/measurements of the voltages and currents induced in wires and integrated circuits contained in enclosures are computationally or experimentally complex and have several limitations. The computations are complicated by the multiscale nature of the simulations, and the experiments are complicated by the cost of the equipment and the extensive time needed to measure every variation to cover all possible scenarios. Statistical methods, such as the Random Coupling Model (RCM) for example [1], are only accurate for high frequencies where the wavelength is much smaller than the size of the enclosure. Another main deficiency of the RCM is that it can't predict the exact induced voltages and currents for a specific well-characterized system but it only provides the statistical properties of these induced currents and voltages.

Solution Proposed: Apply Characteristic Mode Analysis (CMA) to identify the fundamental modes of the enclosure, current distribution, and the field pattern of each mode. This will allow us to predict the worst-case RF coupling scenarios without the need for lengthy simulations and/or expensive experimental measurements. The proposed approach can predict measurements at a fraction of the cost/time. Moreover, we propose to study RF coupling to realistic UAV wire distributions, experimentally reconstructed, when they are placed inside metallic/dielectric UAV enclosures.

Relevance to OSPRES Grant Objective: Provide general guidelines on how the environment, in this case, the enclosure, affects RF coupling and subsequent electromagnetic absorption to UAV wires and integrated circuits.

Risks, Payoffs, and Challenges: The modes depend mainly on the shape and material of the enclosure. Since UAVs have a wide variety of shapes and material compositions, a library of several UAVs needs to be studied before general quantitative conclusions can be drawn. Challenges can be mitigated by the use of the classification techniques of Machine Learning (ML). That is, different ML techniques will be evoked to detect hidden patterns on how the shape, material composition, and the shape/size location of slots correlate with the field enhancement inside the enclosure.

11.1.2 Tasks and Milestones / Timeline / Status

A. Complete the CMA implementation for studying the shielding effectiveness of metallic enclosures. Validate whether CMA can predict the worst-case shielding effectiveness of metallic enclosures as a function of their shapes. / JAN21 / Complete.

   A1. Prepare a manuscript for IEEE AWPL to document the progress done in A. / Ongoing.

B. Progressively build an accurate representation of the UAV wiring system with all of the integrated circuit (ICs) and electronics to test assist the predictions of (c) and the experimental measurement of the actual UAV. / JUL21 / Complete.

C. Address the 2021 UAV's semi-annual review recommendations to study arbitrarily shaped UAV wire distribution. / JUNE21 / Complete.

D. Define the main RF coupling pathways to UAVs, i.e. is RF coupling to the wires/traces the dominant pathway or is it the direct coupling to the electronics, and also quantify the sensitivity of these coupling pathways to load and wire variations. / December 21 / Ongoing.

11.1.3 Progress Made Since Last Report

In previous reports, we developed an accurate model for the wires and electronic circuitry of quadcopter Unmanned Aerial Vehicles (UAVs) using a desktop 3D scanner. The Equivalent Circuit Approach (ECA) was successfully applied to the complex 3D wiring system to develop a circuit representation, which is orders of magnitude faster than full-wave simulations. This month, we used the ECA to vary the electronic devices/loads over a wide range. Since the device/load value is unlikely to be known exactly, we wanted to answer the fundamental question: what matters most, traces/wires or the devices/loads? Our preliminary results show a frequency range where the RF coupling will be insensitive to the load variations, which will help predict the optimum waveform to maximize the coupling when the exact UAV loads are unknown. Detailed results will be presented next month upon completion of all simulations.

11.1.4 Summary of Significant Findings and Mission Impact

A. A fast full-wave tool that facilitates studying the effect of a metallic enclosure on shielding effectiveness has been developed using CMA.

B. Developed an accurate model for the complete wiring system of an UAV, integrated the model with PECNEC, and validated the implementation with rigorous full-wave simulations.

C. Two Second series equivalent circuit branches/resonance is the best combination for the RLC circuit to accurately represent Zin of the system.

12.0 UAS Engagement Wargaming & Modeling and Simulation (M&S)

12.1 Fixed-Effector Wargaming Simulation Toolkit Development

(Nolan Petersen and Travis Fields)

12.1.1 Problem Statement, Approach, and Context

Primary Problem: Wargaming simulations enable rapid evaluation of different weapon systems and strategies. However, the lack of easy to use, high-fidelity software tools makes producing and studying different engagement scenarios (i.e., one friendly system versus five hostile agents) difficult and time-consuming.

Solution Space: We propose developing a simulation environment using the Unity real-time development platform to offer an easy-to-use, medium-fidelity environment for the purpose of studying different blue vs. red engagement scenarios. Unity is a well-established game development software, with a strong community base for tutorials, training, and software assistance. This makes Unity an ideal solution for a medium-fidelity simulation environment to narrow down optimal fixed effector configurations, which could then be studied further in a higher fidelity environment.

State-of-the-Art (SOTA): Current software tools (e.g. AFSIM) for this purpose are tedious to adapt and/or modify for running different scenarios due to a lack of support as well as documentation.

Relevance to OSPRES Grant Objective: Wargaming simulations are relevant to the OSPRES Grant Objective because the ability to simulate and benchmark performance of different scenarios, such as different fixed-effector positions, types, and targeting strategies could provide insight into the ideal utilization of HPM-related systems.

Anticipated Outcome(s): The anticipated outcome of development of a wargaming simulation is a medium-fidelity user friendly wargaming simulation tool capable of simulating realistic engagement scenarios with the ability to easily manipulate the scenario and quickly obtain results.

Challenges: Capturing sufficient realism without significantly reducing performance.

Risks: The risk involved with wargaming simulations is the infinite number of scenarios and configurations, making generalizing difficult from within a simulation environment.

12.1.2 Tasks and Milestones / Timeline / Status

(A) Reproduction of previous results obtained from the previously used wargame software Modern Air Power by John Tiller Software, which is no longer in development, using the Unity environment / MAY21 – JUN21 / Completed.

(B) Implementation of radar uncertainty into simulation environment, enabling increased realism to better simulate current targeting capabilities / JUN21 – JUL21 / Completed.

(C) Trade-space study of microwave, tracking, and hostile agent performance to identify key limitations and low-risk, low-cost improvements, enabling increased weapon efficacy / JUL21 – OCT21 / In Progress.

(D) Optimization of current simulation framework to facilitate more quickly obtaining results / SEP21 – OCT21 / Completed.

(E) Implementation of more effector models such as kinetic weapons and radio jammers to better simulate a layered defense / OCT 21 – NOV 21 / Upcoming.

(F) Implementation of electro-optical/infra-red and lidar sensor capabilities into simulation environment, enabling increased realism to better simulate current targeting capabilities / OCT 21 – DEC 21 / Upcoming.

12.1.3 Progress Made Since Last Report

(C) A comparison between a scenario run in the current simulation environment, which now runs almost exclusively in .NET Framework code, and the same scenario run in a MATLAB version was performed.

(D) Optimization of the current simulation framework to facilitate more quickly obtaining results was completed.

12.1.4 Technical Results

(C) In the future, we would like to perform more trade space studies for a specific type of High-Powered Microwave (HPM) effector model that we often refer to as the Time to Effect (TTE) treatment. We already had the ability to perform simpler studies on the treatment using MATLAB, but this was a much more complex implementation that was hard to modify and would not be scalable due to how complex it would quickly become. Because of this, this month we chose to reproduce some results from the most recent TTE trade-space study. However, because most of the information associated with the TTE treatment is CUI, specific details have been obscured. The main purpose of this was to better understand the current simulation's behaviors and implement a working version of the TTE treatment to conduct further studies in the near future. For this study, a group of hostile Unmanned Aerial Vehicles (UAVs) were deployed beginning evenly spaced on a 5 km circle, after which they flew towards an effector at the center of the circle. A combination of HPM parameters given by x was normalized using a normalization factor denoted by x_0 and varied from 0.2e+08 to 2e+08. Each time, the radius of the final kill was recorded. Keep in mind each UAV was killed each time. Four versions of this test were performed for various combinations of HPM parameters, not including x, denoted by A, B, C, and D. The results are shown in Figure 12.1.1.

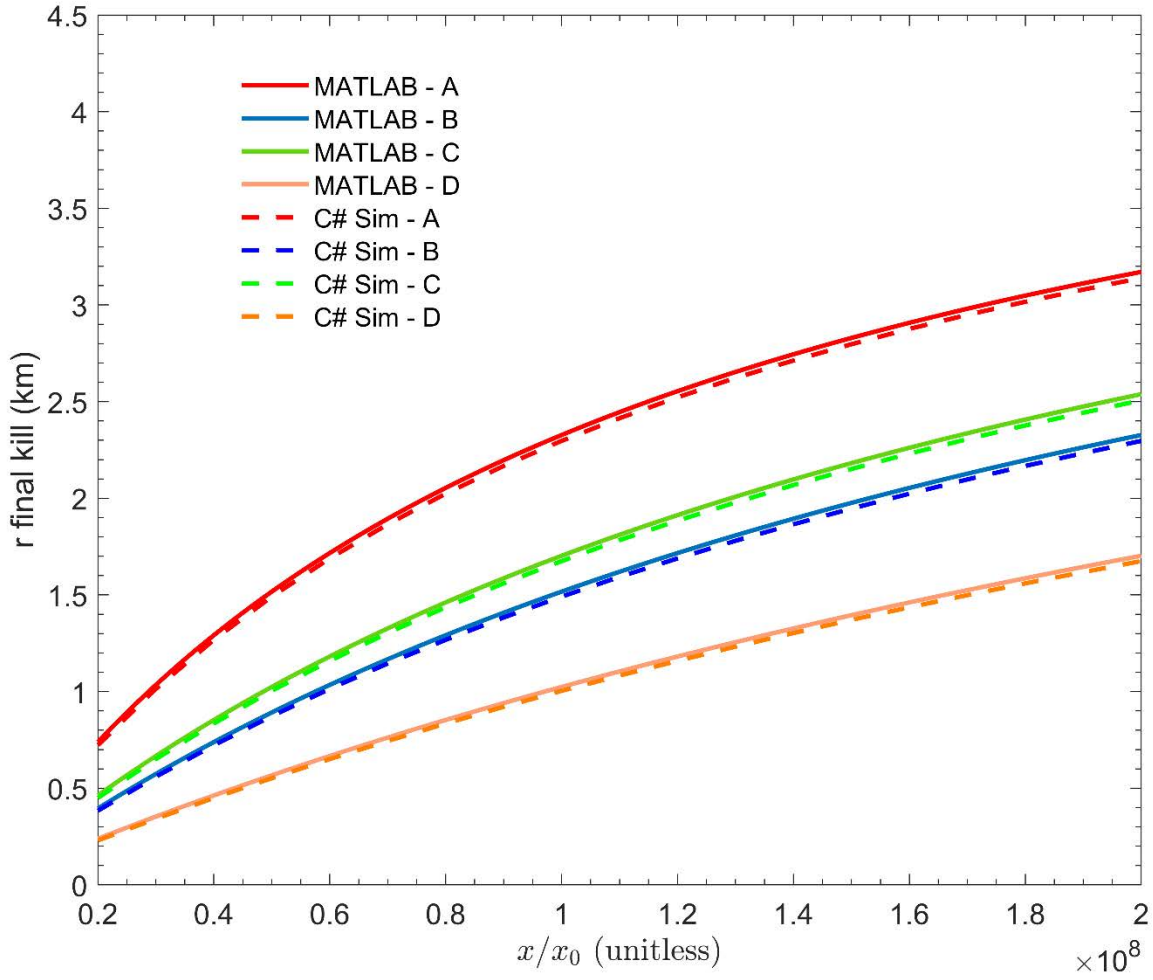


Figure 12.1.1. Normalized TTE parameter x/x_0 vs. the radial distance where the final UAV is killed.

From Figure 12.1.1. it is evident that the results from the C# simulation are close to those of the MATLAB simulation except for deviating slightly as x/x_0 increases. At higher values of x/x_0, the difference between the C# results and the MATLAB results is ~40 meters. While the results may not look very different on the graphs, 40 meters is still a significant difference. We aren't yet sure what is causing this discrepancy but believe it may have something to do with the time step with which the simulation was run. Additionally, the person who produced the MATLAB results mentioned that their simulation would also occasionally exhibit this behavior at specific time steps. Another strange behavior was observed where when the time step was sufficiently small enough, the r final kill curve would follow the same shape but be slightly lower at every x value than the MATLAB simulation. I believe this can be attributed to using a float value type to store information about an object's position. Float values are less accurate than other types of floating-point numbers such as doubles or decimals, but we used them because C#'s built in Vector3 data structure (which we use to store location data) uses float values.

As we make the time step smaller and smaller, the change in position of each object becomes smaller as well. Eventually when your time step is small enough, the change in position will be too small for a float value type to be able to approximate. This leads to the change in position being larger than it should be, thus making some objects move faster than they should. To possibly remedy this, we are looking into making our own Vector3 like data structure that uses doubles rather than floats.

(D) Previously we had begun work on a custom UMKC C# Modeling and Simulation (M&S) library to help facilitate optimizing the simulation as well as easily sharing our work with each other. We have now completed translating all code from the previous simulation which was exclusively run in Unity. This new UMKC C# M&S library is great because it allows the UMKC M&S team to easily collaborate by allowing each member to add their own objects with their own attributes and functions to one library. At which point, any other member of the UMKC M&S team will be able to access those objects using the library and implement said object after which they can make any necessary changes in their own version of the simulation. It also allows each of us to create useful functions to make things easier and share them with each other. For example, much of what was worked on this month in translating the original simulation's code was recreating built in Unity functions that make working with rotation easier. This was important to implement because there are many ways of representing rotation, but most of them involve angles. Using angles to represent rotation in our simulation is undesirable because if you want to find the forward vector of an object given its rotation, you'll have to use trig functions to obtain it. Likewise, if I want to turn a forward vector into a rotation, I'll again have to use trig functions to do so. This is a problem because small errors inherent in computer approximations of trig functions will compound, making my knowledge of the object's forward vector and its rotation less accurate. For example, if I wanted to check that my object is pointed in the direction of a specific vector, let's call it X, I would need to find the objects forward vector from its rotation and check if they are the same. I would find the forward vector from the object's angles of rotation about each axis by using sin and cos then compare my forward vector to the normalization of X. Unfortunately, this doesn't work because even if the two vectors were the exact same, every time that I try and extract the object's forward vector from its rotation, it will be slightly off because of the small trig errors. Additionally, I could not just check to see if the two vectors were within some small threshold of one another because even an error of ~0.05 m (which regularly happened with two identical vectors) would mean the point my object is looking at could be up to 5 cm away from the point I *want* it to look at. This is not accurate enough to model weapons such as High Energy Lasers (HELs) or kinetic weapons. To remedy this, I implemented quaternions which provide a system of representing rotations that is not susceptible to nearly as many problems as other methods such as Euler angles. In addition, they don't require the use of any trig functions and are far more accurate but also notoriously complicated. Unity uses quaternions and had built in functions to make working with quaternions easier, but these functions cannot be used outside of Unity, so we had to recreate our own.

12.1.5 Summary of Significant Finding and Mission Impact

(A) Reproduction of previous results obtained from Modern Air Power by John Tiller Software was completed in Unity, which provided a framework to implement new features.

(B) Implementation of radar uncertainty into the Unity simulation environment was completed.

(C) A trade-space study of the effect of slew-rate on HPM effectors with and without radar uncertainty and off-boresight effects was performed. This study showed that beyond a threshold slew-rate, additional kills are not possible without decreasing firing delay. It also showed that the performance of energy weapons without off-boresight effects is susceptible to the effects of radar uncertainty, while energy weapons with off-boresight effects may mitigate the effects of radar uncertainty on performance.

A trade-space study around a specific type of High-Powered Microwave (HPM) effector modeled by the Time to Effect (TTE) treatment was performed in both MATLAB and the C# simulation to both compare results and understand the behavior of the C# simulation. This provided insight into possible issues with the C# simulation which will be explored in the future.

(D) Optimization of the simulation through development of a custom C# library was completed.

12.2 Airborne Effector Weapons Target Assignment

(Cody Smith and Travis Fields)

Reporting for this topic has been transitioned under the PTERA award.

13.0 Program Management

13.1 Issues

i. Scope – No issues
ii. Budget – 12-month NCTE submitted/pending
iii. Schedule – No issues

13.2 Interactions with Others

Agency/Org	Performer	Project Name	Purpose of Research/ Collaboration

13.3 Major Procurement Actions

13.4 Travel

Destination	Purpose	Attendees	Estimated Costs

13.5 Pending or Upcoming Public Release Requests

14.0 Appendix A: Academic and IP Output

14.1 Students Graduated

Name	Degree	Currently
Al-Shaikhli, Waleed	MS Spring 19	Kansas City National Security Campus, Honeywell
Azad, Wasekul	PhD Summer 21	UMKC/MIDE (Postdoc)
Berg, Jordan	MS Spring 21	
Bissen, Bear	MS Spring 19	UMKC/MIDE (Staff)
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Hanif, Abu	PhD Spring 21	
Harmon, Aaron	BS	Missouri University of Science & Technology
Harp, Joshua	MS	UMKC/MIDE (Senior Engineer)
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Klappa, Paul	MS Spring 21	
Labrada, Dario	BS Spring 20	UMKC/MIDE (MS Student)
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory
Renzelman, Jeff	MS Spring 18	Kansas City National Security Campus, Honeywell
Roy, Sourov	PhD Spring21	UMKC/MIDE (Postdoc)
Wagner, Adam	MS Fall 20	Kansas City National Security Campus, Honeywell
Xia, Shengxuan	BS	Missouri University of Science & Technology

14.2 Journal Publications

14.2.1 In Preparation

[1] N. Gardner, A. N. Caruso, and P. Doynov, “Diode-Based Non-Linear Transmission Line: A Bandwidth and Center Frequency Tuning Study,” *Transactions on Microwave Theory and Technique*, In Preparation, **2021**.

[2] B. Barman, D. Chatterjee, and A. N. Caruso, “Tradespace analysis of wideband coaxial probe-fed microstrip patch electrically small antenna elements,” In preparation, **2021**.

[3] S. Xia, J. Hunter, A. Harmon, M. Hamdalla, A. Hassan, V. Khilkevich, D. Beetner, “Simulation Driven Statistical Analysis of the Electro-magnetic Coupling to Microstriplines,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

[4] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, “Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field Coupling to Randomly Shaped Wires,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2020**.

14.2.2 Submitted / Under Revision

[5] B. K. Lau, M. Capek, and A. M. Hassan, “Characteristic Modes–Progress, Overview, and Future Perspectives,” *IEEE Antennas and Propagation Magazine*, Submitted, **2021**.

[6] K. Alsultan, M. Z. M. Hamdalla, S. Dey, P. Rao, and A. M. Hassan, “Scalable and Fast Characteristic Mode Analysis Implementation Using a Hybrid CPU/GPU Platform,” *ACES*, Submitted, **2021**.

[7] M. Z. M. Hamdalla, B. Bissen, J. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, “Prediction of Experimental Electromagnetic Coupling to a UAV Model Using Characteristic Mode Analysis,” *IEEE Access*, Submitted, **2021**.

[8] W. Azad, F. Khan, and A. N. Caruso, “A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Featuring Custom Isolated Gate Driver Circuit Combined With Coupling and Snubber Circuits,” *IEEE Transactions on Power Electronics*, Submitted, **2021.**

[9] J. N. Berg, R. C. Allen, and S. Sobhansarbandi. “A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation.” *International Journal of Thermal Sciences*, Submitted, **2021**.

[10] John Keerthi Paul Bhamidipati, Eliot R. Myers, Adam M. Conway, Lars F. Voss, and Anthony N. Caruso, “Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches,” *IEEE Transactions on Electronic Devices*, Under Revision, **2020**.

14.2.3 Published / In Press

[11] W. Azad, F. Khan, and A. N. Caruso, “A Medium Power, Self-Sustaining, Configurable RF Pulse Generation Circuit Using a Nonlinear Transmission Line and Power Amplifier in a Closed Loop Configuration, *IEEE Transactions on Plasma Science*, vol. 49, no. 7, pp. 2183–2194, **July 2021** [doi].

[12] S. Roy, W. Azad, S. Baidya and F. Khan, “A Comprehensive Review on Rectifiers, Linear Regulators and Switched-Mode Power Processing Techniques for Biomedical Sensors and Implants utilizing In-body Energy Harvesting and External Power Delivery,” *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 12721–12745, **Nov. 2021** [doi].

[13] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems,” *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364–373, **2019** [doi].

14.3 Conference Publications

14.3.1 Submitted / Accepted

[1] B. Barman, D. Chatterjee, and A. N. Caruso, “Effect of Ground Plane Shape and Size on the Input Impedance of a Monopole embedded in a Grounded Dielectric Substrate,” submitted to the *2021 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*, Marina Bay Sands, Singapore, December 4-10, 2021.

[2] B. Barman, D. Chatterjee, and A. N. Caruso, “Comparison of Q-Factor Calculation Methods for Wideband Microstrip Patch Antennas,” submitted to the *2021 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*, Marina Bay Sands, Singapore, December 4-10, 2021.

[3] S. R. Shepard and H. A. Thompson, “Self-focusing in Guided and Un-guided Media,” submitted to the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, 2021.

[4] B. Barman, D. Chatterjee, and A. N. Caruso, “Probe-location Optimization in a Wideband Microstrip Patch Antenna using Genetic Algorithm, Particle Swarm and Nelder-Mead Optimization Methods,” accepted in *2021 International Applied Computational Electromagnetics Society (ACES) Symposium*, USA, August 1-5, 2021.

14.3.2 Presented

[5] W. Azad, S. Roy, and F. Khan, "A Single Gate Driver-based Four-stage High-voltage SiC Switch Having Dynamic Voltage Balancing Capability," *2021 IEEE Applied Power Electronics Conference and Exposition* (APEC), Phoenix, AZ, USA, June 9-12, 2021.

[6] W. Azad, S. Roy, F. Khan and A. N. Caruso, "A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuits," *2021 IEEE Kansas Power and Energy Conference* (KPEC), Manhattan, KS, USA, April 19-20, 2021 [doi].

[7] T. Layman, T. D. Fields, and O. A. Yakimenko, “Evaluation of Proportional Navigation for Multirotor Pursuit,” AIAA SciTech Forum, Virtual Event, January 11-21, 2021 [doi].

[8] P. J. Klappa, and T. D. Fields, “Assessment of Fixed-Wing UAV System Identification Models during Actuator and Payload Drop Failures,” AIAA Atmospheric Flight Mechanics Conference, Virtual Event, January 11-21, 2021 [doi].

[9] J. Hunter, S. Xia, A. Harmon, A. M. Hassan, V. Khilkevich, and D. Beetner, “Modeling and Statistical Characterization of Electromagnetic Coupling to Electronic Devices,” *IEEE International Symposium on Antennas and Propagation and NSRM USNC-URSI National Radio Science Meeting*, Boulder, CO, January 4-9, 2021 [doi].

[10] B. Barman, K. C. Durbhakula, B. Bissen, D. Chatterjee, and A. N. Caruso, “Performance Optimization of a Microstrip Patch Antenna using Characteristic Mode and D/Q Analysis,” *2020 XXXIIIrd General Assembly and Scientific Symposium of the International Union of Radio Science*, Rome, Italy (online conference), Aug 29-Sept 5, 2020, pp. 1-4 [doi].

[11] J. Berg, and S. Sobhansarbandi. “CFD Modeling of Thermal Management Systems for a Silicon Semiconductor Switch.” *ASME 2020 Heat Transfer Summer Conference collocated with the ASME 2020 Fluids Engineering Division Summer Meeting and the ASME 2020 18th International Conference on Nanochannels, Microchannels, and Minichannels*, Virtual, July 13–15, 2020, American Society of Mechanical Engineers Digital Collection [doi].

[12] B. Barman, D. Chatterjee, and A. N. Caruso, “Performance Optimization of Electrically Small Microstrip Patch Antennas on Finite Ground Planes,” 2020 *IEEE International Symposium on Antennas and Propagation and North American Radio Science Meeting*, Montreal, Quebec, Canada, July 5-10, 2020, pp. 1–2 (online conference) [doi].

[13] M. Hamdalla, B. Bissen, A. N. Caruso, and A. M. Hassan, “Experimental Validations of Characteristic Mode Analysis Predictions Using GTEM Measurements,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Montréal, Québec, Canada, July 5-10, 2020 [doi].

[14] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, “Scalable Characteristic Mode Analysis: Requirements and Challenges (White Paper),” *Large Scale Networking (LSN) Workshop on Huge Data: A Computing, Networking and Distributed Systems Perspective Sponsored by NSF*, Chicago, IL, April 13-14, 2020.

[15] M. Hamdalla, A. N. Caruso, and A. M. Hassan, “Predicting Electromagnetic Interference to a Terminated Wire Using Characteristic Mode Analysis,” *Proceedings of the Annual Review of Progress in Applied Computational Electromagnetics (ACES)*, Monterey, CA, March 22-26, 2020. [doi]

[16] W. Azad, F. Khan, and A. Caruso, "Self-sustaining High-power RF Signal Generation Using LDMOS Based Power Amplifier and Nonlinear Transmission Line," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 3567-3572 [doi].

[17] A. Hanif, W. Azad, and F. Khan, "Detection of Bond Wire Lift Off in IGBT Power Modules Using Ultrasound Resonators," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, March 15-19 2020, pp. 345-350 [doi].

[18] B. Barman, D. Chatterjee, and A. N. Caruso, “Some Investigations into Mutual Coupling Analysis for Trade Space Studies of Linear Arrays,” *2019 IEEE International Symposium on Phased Array Systems and Technology (PAST)*, Waltham, MA, October 2019, pp. 1-8 [doi].

[19] B. Barman, D. Chatterjee, and A. N. Caruso, “Characteristic Mode Analysis of a straight and an L-probe fed Microstrip Patch,” *2019 IEEE Indian Conference on Antennas and Propogation (InCAP)*, Ahmedabad, India, Dec 2019, pp. 1-3 [doi].

[20] M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Characteristic Mode Analysis of the Effect of the UAV Frame Material on Coupling and Interference," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019 [doi].

[21] M. Hamdalla, J. Hunter, Y. Liu, V. Khilkevich, D. Beetner, A. Caruso, and A. M. Hassan, "Electromagnetic Interference of Unmanned Aerial Vehicles: A Characteristic Mode Analysis Approach," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting at Atlanta (2 pages)*, Georgia, USA, July 7-12, 2019 [doi].

[22] K. C. Durbhakula, J. Lancaster, A. M. Hassan, D. Chatterjee, A. N. Caruso, J. D. Hunter, Y. Liu, D. Beetner, and V. Khilkevich, "Electromagnetic Coupling Analysis of Printed Circuit Board Traces using Characteristic Mode Analysis," *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (2 pages)*, Atlanta, Georgia, USA, July 7-12 2019 [doi].

[23] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “On the Location of Transverse Electric Surface Wave Poles for Electrically Thick Substrates,” Proceedings of the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 [doi].

[24] W. Azad and F. Khan, “Sustaining High-power RF Signal Generation in a Positive Feedback Network," *2019 IEEE Pulsed Power and Plasma Science Conference (PPPS)*, Orlando, FL, USA, June 23-28 2019.

[25] K. Alsultan, P. Rao, A. N. Caruso, and A. M. Hassan, “Scalable characteristic mode analysis using big data techniques,” *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[26] M. Hamdalla, W. Al-Shaikhli, J. Lancaster, J. D. Hunter, L. Yuanzhuo, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, “Characteristic Mode Analysis of Electromagnetic Coupling to Wires with Realistic Shapes,” *International Symposium on Electromagnetic Theory (EMTS 2019)*, San Diego, CA, USA, May 27-31, 2019.

[27] K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “Location of Surface Wave Poles in Sommerfeld Integrals: A Mittag-Leffler Expansion Approach,” *Proceedings of the URSI-B International Symposium on Electromagnetic Theory*, URSI Commission, San Diego, USA, May 2019 [doi].

[28] K. C. Durbhakula, D. Chatterjee and A. M. Hassan, “Analytical Evaluation of Sommerfeld Integral Tails Present in Two-layered Media Green’s Functions,” *Proceedings of the Indian Conference on Antennas and Propagation* (InCAP), Hyderabad, India, December 2018 [doi].

[29] D. Beetner, V. Khilkevich, A. M. Hassan, J. Hunter, Y. Liu, and D. Floyd, *“*Characterization of the Electromagnetic Coupling to UAVs,*”* *DE Systems Symposium*, September 24-27, 2018

[30] C. Hartshorn, K. Durbhakula, D. Welty, D. Chatterjee, J. Lancaster, A. M. Hassan, and A. N. Caruso, “Crosstalk and Coupling to Printed Circuit Board Metallic Traces with Arbitrary Shapes,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[31] M. Hamdalla, J. Roacho-Valles, J. Hunter, D. Beetner, A. M. Hassan, and A. N. Caruso, “Electromagnetic Analysis of Unmanned Aerial Vehicles Using Characteristic Mode Analysis,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[32] C. Hartshorn, M. Hamdalla, J. Lancaster, A. M. Hassan, and A. N. Caruso, “Electromagnetic Vulnerability of Wires with Arbitrary Shape,” *Proceedings of the AMEREM 2018 Conference*, Santa Barbra, CA, Aug 27-31, 2018.

[33] K. C. Durbhakula, D. Chatterjee, A. M. Hassan, and M. S. Kluskens, “Studies on Numerical Evaluation of Sommerfeld Integrals for Multilayer Topologies,” *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018.

[34] J. Lancaster, D. Chatterjee, and A. N. Caruso, “Some Investigations into the Dispersion Characteristics of Localized Bessel Beams,” published in the *IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Boston, Mass., USA, July 7-12, 2018 (1 page URSI Abstract).

[35] M. Hamdalla, A. M. Hassan, and A. N. Caruso “Characteristic Mode Analysis of Unmanned Aerial Vehicles with Realistic Shapes and Material Composition,” *IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting,* Boston, MA, July 8-13, 2018.

[36] W. Azad, S. Roy, A. S. Imtiaz, and F. Khan, "Microelectromechanical System (MEMS) Resonator: A New Element in Power Converter Circuits Featuring Reduced EMI," *2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, Niigata, May 20-24, 2018, pp. 2416-2420 [doi].

[37] J. Hunter, Y. Liu, D. Floyd, A. Hassan, V. Khilkevich, and D. Beetner, “Characterization of the Electromagnetic Coupling to UAVs,” *Annual Directed Energy Science and Technology Symposium*, Feb 26-March 2, 2018.

14.4 Conference Presentations

14.4.1 Submitted / Accepted

[1] S. Bellinger, A. Caruso, A. Usenko, “Stacked Diodes for Pulsed Power Applications,” GOMACTech-22, Miami, FL, March 21–24 2022 (submitted, oral).

[2] S. Bellinger, A. Caruso, A. Usenko, “New Paradigm on Making Semiconductor Opening Switches for Pulsed Power,” 2021 23rd IEEE Pulsed Power Conference, Denver, CO, Dec. 12–16, 2021 (accepted, oral).

Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29 2021 (submitted):

[3] B. Barman, D. Chatterjee, A. Caruso, and K. Durbhakula, “Tradespace Analysis of a Phased Array of Microstrip Patch Electrically Small Antennas (ESAs)” (Poster)

[4] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation” (Poster)

[5] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures” (Poster)

[6] J. Bhamidipati, M. Paquette, R. Allen, and A. Caruso, “Photoconductive Semiconductor Switch Enabled Multi-Stage Optical Source Driver” (Poster)

[7] G. Bhattarai, J. Eifler, S. Roy, M. Hyde, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “All Solid-State High-Power Pulse Sharpeners” (Poster)

[8] S. Brasel, K. Norris, R. Allen, A. Caruso, and K. Durbhakula, “Efforts to Reduce Physical Aperture Area of Ultra-Wideband Arrays” (Poster)

[9] A Caruso, “ONR Short Pulse Research and Evaluation for c-sUAV: Supporting and Sub-Programs Overview” (Oral)

[10] J. Clark, R. C. Allen, and S. Sobhansarbandi, “Ultra-Compact Integrated Cooling System Development” (Poster)

[11] J. Eifler, S. Roy, M. Hyde, G. Bhattarai, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “TCAD Optimization of Epitaxially Grown Drift-Step Recovery Diodes and Pulser Performance” (Poster)

[12] N. Gardner, M. Paquette, and A. Caruso, “Diode-Based Nonlinear Transmission Lines Capable of GHz Frequency Generation at Single MW Peak Powers” (Poster)

[13] M. Hamdalla, A. Caruso, and A. Hassan, “The Shielding Effectiveness of UAV Frames to External RF Interference” (Poster)

[14] M. Hamdalla, A. Caruso, and A. Hassan, “A Predictive-Package for Electromagnetic Coupling to Nonlinear-Electronics using Equivalent-Circuits and Characteristic-Modes (PECNEC)” (Poster)

[15] M. Hyde, J. Eifler, S. Roy, G. Bhattarai, A. Usenko, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Development of an Evaluation Network for Drift Step Recovered Diodes through and Augmented Design of Experiment” (Poster)

[16] S. Indharapu, A. Caruso, and K. Durbhakula, “Machine Learning Based Ultra-Wideband Antenna Array Optimization and Prediction” (Poster)

[17] F. Khan, W. Azad, and A. Caruso, “A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Architecture for Pulsed Power Applications” (Poser)

[18] D. F. Noor, J. Eifler, M. Hyde, G. Bhattarai, S. Roy, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “DSRD-IES Pulsed-Power Generator Topology Study Using Machine-Learning-Based Feature Selection Optimization and Predictive Learning” (Poster)

[19] S. Roy, J. Eifler, M. Hyde, G. Bhattarai, D. Noor, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "Systematic Topological Optimization of DSRD-Based IES Pulse Generator" (Poster)

[20] S. Shepard and A. Caruso, "Tubular Core Optical Power Amplifier" (Poster)

[21] H. Thompson, M. Paquette, and A. Caruso, "Minimizing On-State Resistance in GaN:X Photoconductive Semiconductor Switches (PCSSs) for Direct Modulation (Poster)

[22] A. Usenko, J. Eifler, S. Roy, G. Bhattarai, M. Hyde, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "New Paradigm in Fabrication of Semiconductor Opening Switches for Pulsed Power" (Poster)

***

[23] S. Bellinger, A. Caruso, A. Usenko, "Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme," 240th Electrochemical Society Meeting, Orlando, FL, Oct. 10–14, 2021 (submitted, oral).

14.4.2 Presented

[24] W. Azad, S. Roy, and F. Khan, "A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver," *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, 2020 (oral).

[25] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, "Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS," *Annual Directed Energy Science and Technology Symposium*, March 2020 (abstract appeared, but talk cancelled due to pandemic).

***

DEPS Posters and Presentations 2020

[26] William Spaeth, Wideband Parallel Plate to Coaxial Cable Taper

[27] Stefan Wagner, Quickly Determining Minimum HPC Source Requirements Using Binary Search

***

GOMAC 2019

[28] Cash Hauptmann, Reduced Recovery Time in SiPCSS Photoconductive Switches

[29] Eliot Myers, Picosecond High Power Switching Technologies

[30] Heather Thompson, GaN Optimization for Use in Photoconductive Switch

***

[28] B. Barman, D. Chatterjee, and A. N. Caruso, "Analytical Models for L-Probe fed Microstrip Antennas," *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, 2019 (1 page URSI Abstract).

***

Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium, Destin, Florida, USA, April 2019:

[29] Ryan Butler, Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources

[30] Steve Young, Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort

[31] Adam Wagner, Rapid Cost Effective RF Component Prototyping Using 3D Printers

[32] Heather Thompson, Cost to benefit analysis of GaN for Photoconductive Semiconductor Switches

[33] Colby Landwehr, Low Leakage Electroluminescence For Improving SiPCSS Hold Off

[34] James Kovarik, Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements

[35] Spencer Fry, Maximizing SiPCSS Efficiency For HPM Sources

[36] Deb Chatterjee, Studies On Antenna Characterization And Propogation Of High Power Pulsed Electromagnetic Waves With Minimal Dispersion

***

DEPS Posters and Presentations 2018

[37] Jeff Scully, ElectroLuminescence Studies of Silicon Based Photo-Switches

[38] Cash Hauptmann, Thermal Anlaysis of a PCSS through TCAD Simulation

[39] Nicholas Flippin, Fast Rise Time Switches: Drift Step Recovery Diode

***

DEPS Posters and Presentations 2017

[40] Noah Kramer, Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency

14.5 Theses and Dissertations

[1] Jordan N. Berg, “Development of a Jet Impingement Thermal Management System for a Semiconductor Device with the Implementation of Dielectric Nanofluids,” MS Thesis in Mechanical Engineering, University of Missouri-Kansas City, **2021** [doi].

[2] James C. Kovarik, “Wideband High-Power Transmission Line Pulse Transformers,” MS Thesis in Electrical Engineering, 2021.

[3] Wasekul Azad, “Development of Pulsed Power Sources Using Self-Sustaining Nonlinear Transmission Lines and High-Voltage Solid-State Switches,” PhD Dissertation in Electrical Engineering, 2021.

[4] Paul Klappa, “Implementation and Assessment of State Estimation Algorithms in Simulation and Real-World Applications,” MS Thesis in Mechanical Engineering, 2021.

14.6 IP Disclosures Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” 12AUG2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same,” 28JUNE2021.

[3] Bhamidipati, Myers, Caruso, “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources,” 21UMK009, 04NOV2020.

[4] Shepard, “A Low Noise Optical Amplifier,” 21UMK007, 14SEPT2020.

[5] Shepard, “A Novel Optical Fiber Amplifier,” 20UMK012, 02JUN2020.

[6] Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna,” 20UMK011, 19APR2020.

[7] Doynov, “Scalable Modular System for High-power Microwaves Generation,” 20UMK010, 19APR2020.

[8] Doynov, “Pulse Differential High-power Microwave Generation,” 19UMK007, 02JAN2019.

[9] Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal,” 19UMK008, 28DEC2018.

[10] Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output,” 19UMK005, 28SEPT2018

14.7 Provisional Patents Filed

[1] S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” filed 09/10/2021.

[2] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same” US Provisional Patent Application 63/216,550, filed June 30, 2021.

[3] P. Doynov, A. Caruso, “High-Efficiency High-Power Microwave Generation using Multipass Non-Linear Network Topologies,” filed 26NOV2019.

[4] Plamen Doynov, James Prager, Tim Ziemba, Anthony N. Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, USPTO Provisional Serial No. 62/737,185, filed 27SEPT2018.

14.8 Non-Provisional Patents Filed

None to date