Predicting Vertical GaN Diode Quality using Long Range Optical tests on Substrates

James C. Gallagher[1], Travis J. Anderson[1], Andrew D. Kohler[1], Mona A. Ebrish[2], Michael A. Mastro[1], Jennifer K. Hite[1], Karl D. Hobart[1], Francis J. Kub[1]

1. U.S. Naval Research Laboratory, Washington, DC, 20375 USA
2. National Research Council Postdoc Fellow Residing at The U.S. Naval Research Laboratory

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Abstract

It is well known that vertical GaN devices could surpass current lateral GaN switch technology due to higher critical electric fields and higher breakdown voltages from its different geometry, and lower impurity concentration from the superior quality of homoepitaxial films. However, the inconsistency of GaN substrate properties, both within wafer and vendor-to-vendor, makes reliable device fabrication difficult. Here we implement long-range spectroscopic studies of GaN substrates and epitaxial wafers using Raman, photoluminescence, and optical profilometry to assess incoming material and correlate to electrical performance of vertical diodes. We have classified incoming wafers into two general types, and determined that inhomogeneities in the wafers can negatively affect the reverse leakage current of PiN diodes.

INTRODUCTION

GaN is a candidate for the next-generation power switching technology as Si and SiC hit their theoretical limits. Currently, lateral GaN High Mobility Electron Transistors (HEMTs) are commercially successful for RF applications, but have limited blocking capability for high power applications, necessitating vertical devices. Recent advances in substrate technology have realized widely available free-standing 2” substrate as well as high quality bulk crystals with dislocation density ~1E3 cm^{-2}.

There are several challenges in utilizing vertical GaN technology. One major issue being that substrate manufacturing produces inconsistent properties at length scales relevant for power devices. To make this technology conceivable, quick non destructive screening techniques are needed similar to previous studies on SiC substrates [1], [2].

In our previous work [3]–[5], this was studied using four techniques: photoluminescence (PL) images, Raman spectroscopy, optical profilometry, and PL spectroscopy for incoming wafer screening. Additionally, we discovered that long range characterization is important for determining device quality as samples often passed short range scans but were inhomogeneous over longer ranges, which negatively affected diode performance. In this work we further study these techniques as well as study device performance to determine how the wafer screening techniques help predict device quality.

Our previous research [6] used the prementioned optical techniques to study wafers from 10 different vendors. Raman and photoluminescence mapping are used on native substrates to sort GaN substrates into 2 categories: those with homogeneous distribution of carriers (type I) and those with an inhomogeneous distribution (type II) [6]. The type II wafers could be further sorted into two categories: those with a regular distribution pattern of defects which often results from wafers synthesized with the dot core technique (type II-a) [7], and those with a random distribution of defects (type II-b). Though type I wafers have more consistent sample quality and device performance [6], they are more expensive than type II wafers, therefore there is much motivation in mapping wafers to determine which regions have higher quality device performance. Additionally, type I wafers can have defects in localized regions [3], making it important to screen these wafers as well.

We find that Raman mapping was the most useful of the optical techniques. Mostly because optical profilometry and PL spectroscopy are surface sensitive techniques, while the defects of interests may only appear deep in the substrates. Additionally, Raman spectroscopy can be used to probe the substrate quality after a homoepitaxial layer is grown. Since it is surface sensitive, the PL imaging technique can be implemented as a complementary technique to separate features in the epilayer from those in the substrate.

EXPERIMENTAL

For our experiment, we obtain multiple wafers from the same vendor. Homoepitaxial, unintentionally doped GaN drift layers were grown on using metal organic chemical vapor deposition. It was grown using a V/III of 3000, growth temperature of 1030 °C, and pressure of 200 Torr to a thickness of 5 μm. The ramp to growth temperature was performed under an ammonia atmosphere (11 slm). Anode layers were regrown by MBE with a 500 nm p-GaN ([Mg]>1E19) layer on a smaller selection of substrates. Using Raman spectroscopy, we analyzed two major peaks of interest in long-range wafer characterization. The E_2 peak around 567 cm^{-1} which is always present, with the peak position indicating changes in crystal stress and the peak position indicating crystal quality [8]–[10], The A_1 longitudinal optical peak, which is found at 734 cm^{-1} when the carrier concentration is low ($n < 10^{17}$ cm^{-3}) and shifts to larger wavenumber as the concentration increases and disappears around $n > 10^{19}$ cm^{-3} [10]. These peak were fit using a pseudo Voigt model with a linear background using Python's lmfit module as done in our previous research [3]. Analysis of the A_1 peak (figure 1) reveals that all three types of wafers can be detected. Our previous research [6] indicates that we have a more consistent diode performance with type I wafers than type II-b wafers. This project focus on studies diodes performance on type II-a wafers to correlate the Raman spectra with device quality.

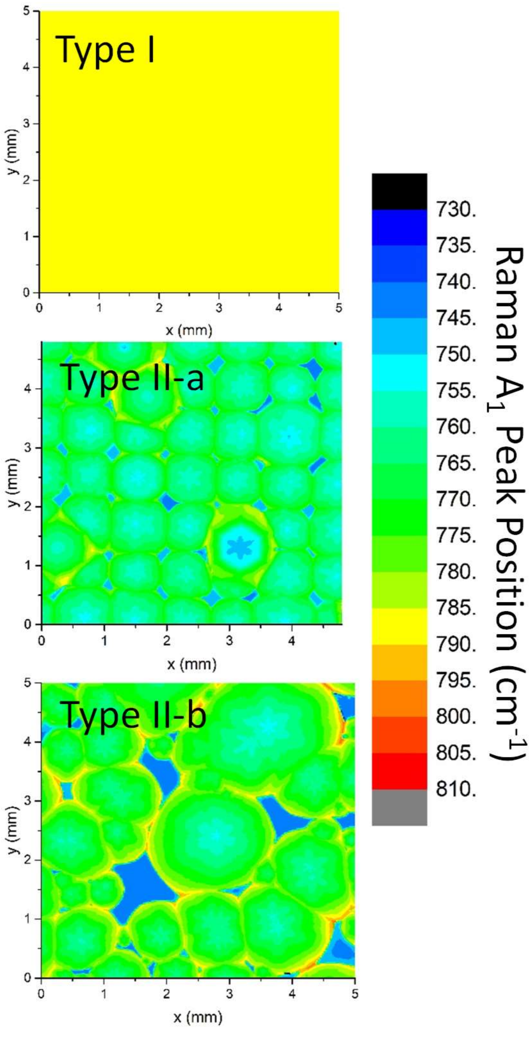

Figure 1. Raman map of Type I (Uniform), Type II-a (Patterned), and Type II-b (Irregular) samples.

Closer analysis of type II-a wafers indicate that regular patters of carrier concentrations exist in a regular pattern. Analysis of the E_2 peak (see figure 2b) shows that at the center of the regions there is a shift in peak position indicating large crystal stress. This shift is only about 0.1 cm^{-1} indicating that it is difficult to detect by E_2 peak analysis, but the crystal stress is likely the results of higher dislocation density, causing the larger carrier concentration detected using the A_1 peak, thus we would predict that high quality devices would occur outside these regions. In further discussion the high carrier concentration features are referred to as "high n" and the space between as "low n."

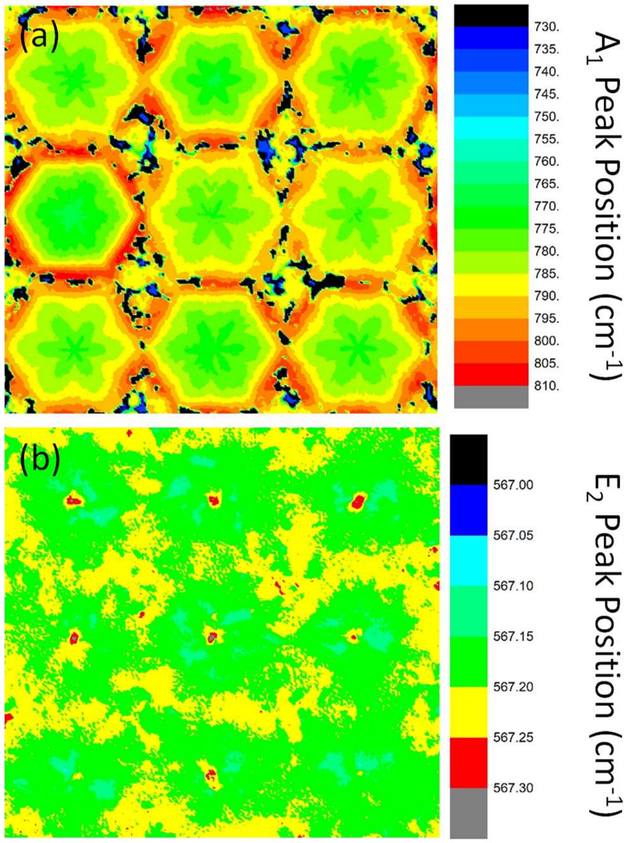

Figure 2. A_1 (a) and E_2 (b) peak position of the type II-a samples. The effects of the defects are apparent by analyzing both peaks. However, the E_2 peak is only present by a ~0.1 cm^{-1} shift, which is much more difficult to detect, though when it is detected it can pinpoint the location precisely.

Following Raman characterization, Schottky barrier diodes were fabricated on the bare drift layers and PiN diodes were fabricated on the regrown layers by the deposition of Pd/Au. The devices were arrays of circular dots with diameters of 200, 300, 400, and 500 µm. The diodes were intentionally patterned such that some devices were on the high defect density features of the samples, while others were off them. A backside contact was created with a blanket

Ti/Al/Ni/Au layer. The Results for the forward and reverse bias on the diodes are shown in figures 3 and 4.

DISCUSSION

Analysis of the Schottky diodes reveal that both forward and reverse bias curves have typical diode behaviour. The forward bias curve (figure 3a) reveals all diodes have an exponential increase in current as expected from a Pd contact to n-type GaN. The ideality factor ranges from 3.3-6.0 with no clear trend. The reverse leakage current (figure 3b) shows no clear dependence on the crystal stress or the carrier concentration.

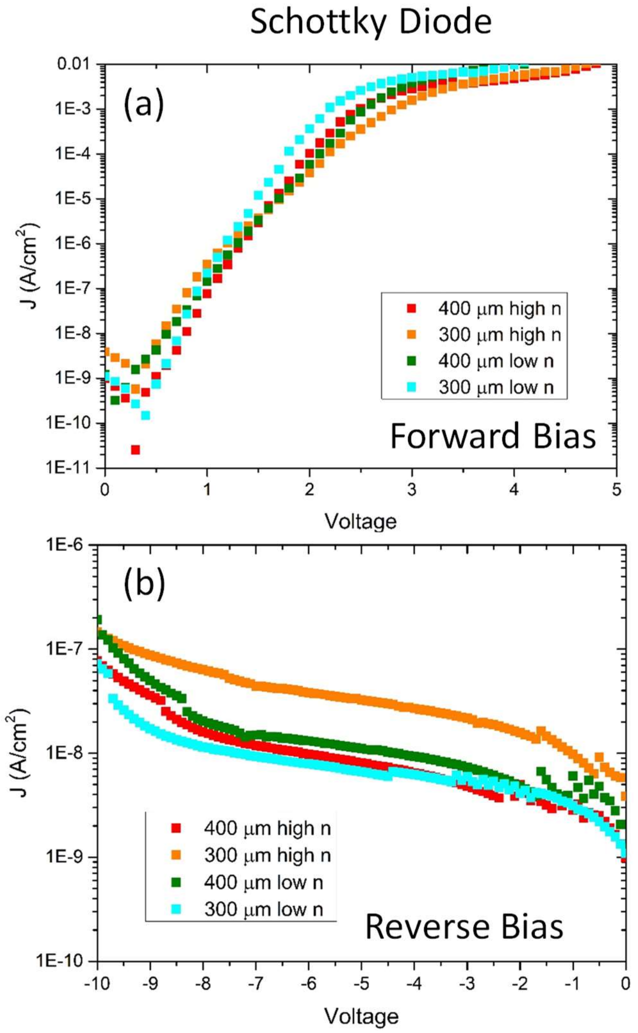

Figure 3. Forward (a) and reverse (b) bias I-V curves for vertical Schottky diodes of 300 -400 µm diameter both on and off the high crystal stress regions characterized by high carrier concentration (*n*) in Raman maps.

Analysis of the PiN diodes reveals a turn on voltage around 4 volts with an ideality factor of 3.5. The low quality of the on state and increased leakage at 2-3V is likely due to high concentrations of Si, C, and O at the MBE regrowth interface from the p-layer being grown ex-situ. However, all the samples have a consistent forward current (figure 4a). The reverse bias (figure 4b) shows a great leakage current when the diodes are on the features with higher crystal stress and larger carrier concentration. It is likely that defects from the substrate extend into the p-layer causing n-type defects to lower the fermi level thus reducing the voltages required to deplete the holes.

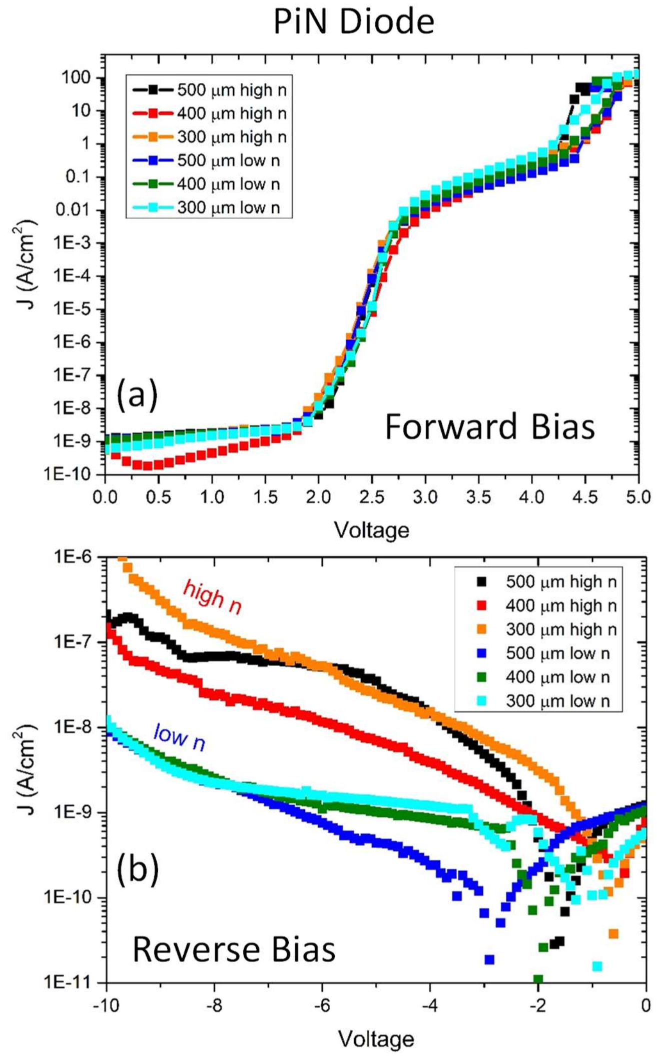

Figure 4. Forward (a) and reverse (b) bias I-V curves of PiN diodes on type II-a wafers both on and off the features characterized by high carrier concentration (n) in Raman maps.

Sixteen devices in a 4x4 grid were placed with the corner devices centered on "high n" regions. A Raman map of the region is shown in figure 5a indicates the devices at the corners of the grid are near the high crystal stress points indicated in figure 2. The reverse leakage current at -10 V is shown in figure 5b as well as the revers bias plots in figure

4b, and it indicates that devices on crystal stress points consistently increase the reverse leakage current of fabricated PiN diodes. We hypothesize these differences are due to the electric field bending in the regions were the defect density is non uniform.

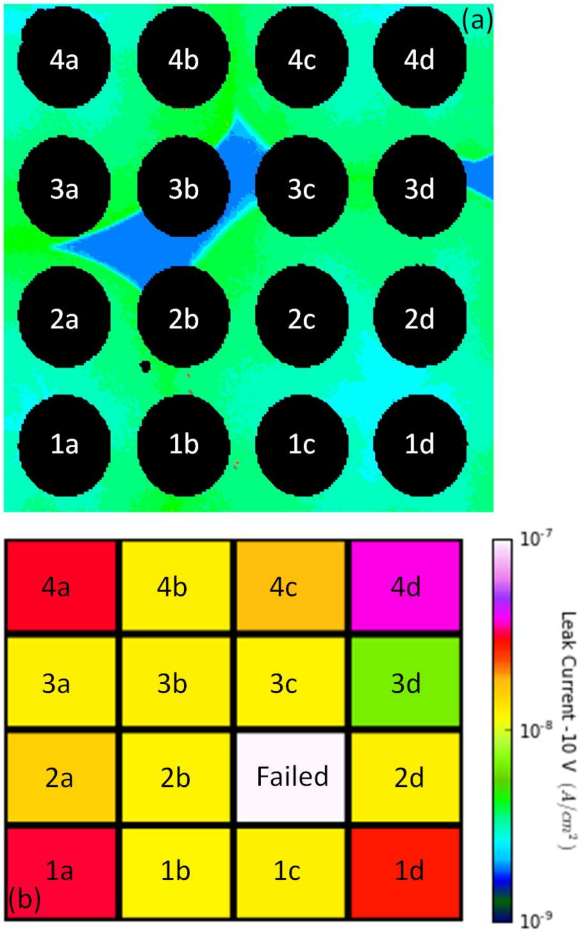

Figure 5. (a) Raman map of sixteen 200 μm PiN diodes on 4x4 grid of a type II-a sample with the corners near regions of high crystal stress is shown. The metal regions shielded by the Raman laser, there were output as black circles. (b) A map of the reverse leakage current at 10 V.

Conclusion

Three wafers obtained from the same vendor were mapped with several long-range optical techniques, and it was determined that some samples have inhomogeneities that can be measured by calculating the carrier concentration using the A_1 peak in Raman spectra. Some of the wafers had homogenates that occur in regular patters. By fabricating devices on and off the regions with high crystal stress (red regions in figure 2b.) we discovered that the defects in the stressed regions likely propagate into the p-layer of PiN diodes. The created defects are likely n-type thus reducing the voltages required to deplete the p-layer. This is supported by the consistent performance of Schottky diodes fabricated on similar samples with the p-layer absent. Our results suggest that devices could be fabricated on the less-expensive type II wafers with the same quality and consistency if regions of high crystal stress are avoided.

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