ONR Short Pulse Research, Evaluation, and non-SWaP Demonstration for C-sUAS Study (OSPRES): Final Technical Report

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14. ABSTRACT

This final technical report covers the OSPRES Grant program, developed to execute high-risk, high-payoff efforts that address elementary gaps to achieving a modular, scalable & electronically steerable high power microwave (HPM) based defense system for the counter UAS mission, with focus on the short-pulse high-average-power space, as well as the responsivity of the target to RF stimuli, while educating the next generation of pulsed power scientists/engineers. The scope spans HPM engagement modeling & simulation, RF coupling, source system/sub-system development (prime power, optical/electrical switches, lasers, pulse forming networks, antenna design & thermal management).

15. SUBJECT TERMS

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2 ADMINISTRATIVE

2.1. Program Overview and Executive Summary

Objective

The technical objective of the ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for C-sUAS Study (OSPRES) Grant program is to execute high-risk, high-payoff efforts that mitigate, fill, or rectify one or more grand challenges or elementary gaps needed to achieve a modular, scalable, and electronically steerable high power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) mission, with focus on the short-pulse high-average power space, as well as the target and its responsivity to radiofrequency stimuli. A parallel objective is to educate the next generation of pulsed power and defense-minded scientists, engineers, and innovators.

Small unmanned aerial systems (sUAS) continue to present an increasing asymmetric threat, from intelligence capture to payload transfer to kinetic airspace nuisance. This problem is considered a grand challenge begging for a comprehensive study of present- and future-art countermeasures, to identify the most optimal (including policy acceptable engagement) means of mitigating the sUAS threat with extrapolation to practical range, cost, delivery, and integration. Solution categories include kinetic and non-kinetic tools; of the non-kinetic tools, the main classes are high energy laser (HEL) and high power microwave (HPM) weapons. Within the HPM space are long- and short-pulse, high-peak and high-average power technologies; short-pulse and high-average power is an important and relatively unexplored space, and the focus of this effort.

The OSPRES Grant program represents the more fundamental high-risk, high-payoff complement to the applied OSPRES Contract program (N00014-18-C-1017). The goal—represented in this final grant report—is to develop capabilities that are published in the peer-reviewed literature, protected as intellectual property, and/or transitioned to the OSPRES Contract effort and beyond for integration with other DoD needs or dual-commercial-use in a service program office. The program is organized as a series of clearly defined sub-projects addressing different challenges or gaps within the overall mission-space. We take a fail-fast philosophy: if a technology/concept is not clearly progressing toward defined targets/milestones, it will be canceled, and a new approach investigated, or a new gap/deficiency within the program scope addressed. Exceptions include projects which form the basis for student theses or dissertations. All efforts should be fundamental and publically releasable in nature when taken individually. This report has been reviewed for operational security, compilation, proprietary and pre-decisional information concerns.

The OSPRES Grant program is broken into sub-areas focusing on HPM engagement modeling and simulation, RF coupling mechanisms, and HPM source system/sub-system development. The latter is divided into further sub-areas including prime power, semiconductor-based switches (photoconductive and non-phototriggered), lasers and optics, pulse forming networks (PFN), thermal management, and antenna design. An overview of the sub-projects is provided in Section 2.2.

Technical Accomplishments

Preliminary work on UAS engagement modeling and simulation was performed with the objective to develop the framework and algorithms required for effective weapons target assignment optimization for both aerial- and ground-based weapons during hostile unmanned aerial threat engagements. However, due to its applied and sensitive nature, this work was transitioned to the PTERA Contract fairly rapidly. Please see the May–Dec 2021 MSRs and the PTERA Contract for further details.

Early work on the OSPRES Grant program focused on fundamental unclassified RF effects studies, which were applied or transitioned to the OSPRES Contract. A substantial RF Coupling sub-effort was pursued to quantify the effect of different enclosures on current induction to the wires and electronics typically used in UASs. We have developed a fast full-wave tool based on characteristic mode analysis that allows one to study the effect of the metallic enclosure on shielding effectiveness. We have created complete and simplified equivalent circuit UAS models, and have demonstrated that the simplified model can accurately model the response of the actual UAS system with significant savings in computational time. This work represents a fundamental advance in the field, and this project was transitioned to the DARPA WARDEN program.

Toward a more efficient power conditioning scheme for high-power microwave generation, we have developed a custom high-voltage switch that can serve as an alternative to large, expensive, and non-US-based commercial BEHLKE switches. We have designed, built, and tested a 10 kV rated HV two-module switch from inexpensive COTS MOSFETS coupled with a 10 kV rated isolated gate driver, which has been successfully tested up to a DC supply voltage of 6 kV at a switching frequency up to 15 kHz. This work terminated at a low-TRL and needs to be tested and ruggedized to meet the MIL-STD 810H to be a direct BEHLKE competitor.

Early work on the OSPRES Grant was also focused on fundamental photoconductive semiconductor switch (PCSS) development, to complement the more applied work executed on the OSPRES Contract effort. Toward optimizing Si PCSS devices, we used TCAD to develop optimum top contact geometries, which yielded a predicted ~30% laser energy reduction with optimized 350 μm spacing. More generally, toward evaluating novel PCSS devices against criteria of more direct value, we developed a figure of merit (FOM) for evaluating semiconductor materials for photoconductive switching applications, building off historical work on electrical switch FOMs (e.g., Baliga FOM). Additionally, efforts were made to investigate GaN as a potential PCSS candidate, including *ab initio* simulations, theoretical device design, and empirical testing. Although progress was made, we determined that the cost-to-benefit ratio for investing resources in GaN PCSS was minimal, and chose to refocuse. Further details are located in the sub-project summary reports compiled below.

Related to the PCSS project, was a fiber laser effort with the goal of reducing by half the cost of pico-second lasers (of average powers up to 120 W). A secondary goal was to increase the operating power of this class of lasers as high as possible. We accomplished

the goals within fiber laser amplifier embodiments (fed by a seed laser diode) in ways that also reduce the amplified spontaneous emission (ASE) noise. Specifically, we found that a pre-burst pumping scheme can reduce the cost of a fiber laser amplifier by a factor of 40 and that gain saturation can be maintained in amplifier stages to suppress the overall ASE by 5,000 (for an overall power gain of 8 million). Nonlinearities limit laser power in circular core fiber amplifiers. We increase the power by over two orders of magnitude by utilizing a tubular core, wherein symmetry breaking causes preferential nonlinear scattering to the inside of the tube, where it accumulates as an air-core mode. These permit a peak power of 10 GW, which enables the triggering of an entire array of up to 100 PCSS via a single laser/amplifier source, thereby eliminating the optical timing jitter constraint.

Additionally, a wide bandgap PCSS-enabled multi-stage laser diode array (LDA) driver was proposed to overcome the size, weight, and cost limitations of conventional laser systems. An initial feasibility study based on Jenoptik's vertical diode stack indicated a need for >100 A currents with sub-ns risetimes, which requires a lock-on conduction in the PCSS with a gain factor $10^{2.6}$ at <50 V bias. However, our attempts with in-house testing to show lock-on conduction in optical switches such as GaN-PCSS, Si-PCSS, and optodiodes were unsuccessful. Due to the unavailability of custom-made GaN-PCSSs and lack of promising results in finding an alternative switch technology, the LDA driver effort was not pursued further.

In the latter half of the OSPRES Grant effort, focus shifted to non-phototriggered ultrafast opening switches, which can avoid the need for high average power (>30 W) laser subsystems per module. Specifically, inductive energy storage and release pulse generators utilizing the ultra-short turn-off transients of drift-step-recovery diodes (DSRDs) were identified as a strong candidate for our target of generating short-rise-time (≤1 ns), high pulse repetition frequency (PRF) (~100 kHZ), high voltage (≥10 kV peak output voltage) pulses, within a small form factor (< 1 L). We pursued several directions: optimizing DSRD devices via simulation and testing, improving diode devices by updating manufacturing processes, and optimizing DSRD pulser circuit design with theory and empirical testing. TCAD was used to determine the optimum diode doping profile, which was found to be exponential with a minimum doping density of $5 \times 10^{13}/cm^3$ and the junction placed near the middle of the device. SPICE models were additionally developed that were able to closely match experimental output, and were used to optimize the pulser for 10 kV peak load voltage. We have modernized drift-step recovery diode (DSRD) manufacturing, moving beyond 60-year-old technology, by using state-of-the-art (SOTA) semiconductor processing techniques to ultimately improve DSRD performance and reliability. A new process has been designed that includes graded epitaxy doping, intermetallic bonding for stacking, anisotropic etch side termination, stain etch side passivation, and selective-deposition-based metallization. After testing and optimization of each step, the fabricated DSRDs were tested and demonstrated better performance than competitor devices. Patent applications on our novel process integration scheme have been submitted to the USPTO. Toward maximizing power output efficiency, we

developed a physics-based circuit model, which was used to systematically optimize pulser performance. Based on this optimization, we were able to demonstrate 4.6 kV output voltage using a single 7-DSRD-stack pulser driven by a single MOSFET with 120 V prime supply. Then, using a MOSFET module and three 7-DSRD-stacks, we were able to achieve a maximum peak voltage of 9.2 kV with a 20–90% risetime of 5 ns using a prime source of 140 V, close to the output voltage target and falling somewhat short of the rise-time target, with PRF measurements still to be determined. Overall, work on the OSPRES Grant cumulated in substantial advancement of DSRD-based pulser technology, and this was transitioned to the PTERA program for further optimization and testing.

Various nonlinear transmission line (NLTL) technologies were investigated to improve the SWAP-C metrics of pulse forming networks (PFNs), including positive feedback, gyromagnetic, and multiferroic NLTLs. We ultimately focused on diode-based nonlinear transmission lines (D-NLTSs) as the positive feedback systems were limited to 100 kW peak power and the multiferroic materials needed to improve on the state-of-the-art in NLTLs are five to ten years away. Some of the challenges faced at the outset included immature and inaccurate design processes/simulation capabilities at high frequencies, a dynamic characteristic impedance that makes signal injection/extraction inefficient, and demonstrated frequency and power generation that fall short of the requirements of directed energy weapon systems. We made progress on each of the above fronts, respectively, by developing clear design metrics ranging from component selection to device fabrication, effectively using bipolar excitation on a DC-biased D-NLTL, and building D-NLTLs with high-voltage epoxy diodes that can handle signal amplitudes in the single to tens of kV. Our studies have shown D-NLTL networks with demonstrated frequency generation in the upper VHF (30–300 MHz) to UHF (0.3–1 GHz) ranges, with our highest recorded frequency generation of 1.58 GHz at MW powers. With auto-tunable inductors and a better handle on the dynamic impedance, the D-NLTL effort was transitioned to the OSPRES Contract and a new program (PTERA) which continues to see center frequency tunability and very high volumetric power density performance at conversion efficiencies that are a factor of four or greater compared with the best gyromagnetic NLTL systems tested.

A multifrequency generator with chirp-capability was implemented to address the limitations of conventional RF pulsers in terms of form factor and waveform tunability. Two versions of these frozen-wave generators (FWGs) were implemented with: (i) coax-based distributed element transmission lines (DETLs) and (ii) lumped-element-based transmission lines (LETLs), both driven by SiC MOSFETs. While chirp capability was demonstrated with both (i) and (ii), dynamic tunability was demonstrated only on the LETL-based generator. Furthermore, the LETL-based generator demonstrated >80% reduction in size and 60% reduction in weight compared with the DETL-based generator. However, the generated frequencies were limited to <100 MHz due to the rise-time and fall-time limitations of the SiC MOSFET, which are on the order of 10s of ns. A solid-state switch analogous to photoconductive solid-state switches (PCSSs) capable of sub-ns t_{rise}

with low jitter and compact trigger mechanism would greatly benefit the solid-state LETL topology of the FWG.

Magnetic pulse compression (MPC) and time-reversal based pulse compression (TR-PC) were evaluated, as an alternative to power combining with solid-state amplifiers (SSAs), to increase the available output power (P_{out}) in a high power microwave (HPM) system within SWAP-C2 requirements. The MPC was shown to theoretically provide a 17 dB increase in the instantaneous P_{out}, up to a few hundred MHz. The achievable gain is strongly dependent on the magnetic core material properties. The restrictions imposed by available magnetic materials and properties required for high-frequency operation were documented. A material development proposal based on MPC requirements was prepared with KRI. The initial study of TR-PC suggests that gain is achievable with pulsed power operation; the feasibility study of TR-PC – SSA integration is on-going with NRL.

Next-generation thermal management systems (TMSs) were investigated to provide compact integrated device cooling, with the target of dissipating up to 1 kW/cm^2 of heat and maintaining active device temperature below 80 °C. A jet impingement TMS (JI-TMS) was designed, modeled with computational fluid dynamics (CFD), and prototyped and experimentally tested. The JI-TMS was able to maintain device temperature at 57.5 °C (54.7 °C simulated) at 100 W and 98.2 °C (99.0 °C simulated) at 200 W. Replacing the silicone heat transfer fluid with a custom nanofluid yielded a further ~15% decrease in temperature. However, due to the high pressure drop in this design, it was determined to be unsuitable for the 1 kW heat removal target, and focus shifted to an ultra-compact TMS (UC-TMS) model. This new design yielded an average surface temperature of 74 °C with deionized water and 37 °C with silicone fluid via simulation, an improved performance over the JI-TMS; however experimental prototyping needs to be completed and pressure changes investigated.

The objective of the antenna design thrust was to determine the extent to which the physical aperture size of an antenna array can be reduced while maintaining peak power density, bandwidth, and beam steerability, over the UHF range (0.3–1 GHz)), compared with present art HPM-capable antenna arrays. First, a design technique for wideband (≥35% bandwidth), high fidelity (>90%), microstrip electrically small antennas, with improved power handling capabilities (~5 kW), at UHF (MHz) to microwave (GHz) operating frequency ranges was developed and experimentally validated. Systematic characterization of planar microstrip phased arrays of various aperture areas and lattice arrangements showed ~46% aperture area reduction without significant degradation in boresight gain (<2 dBi reduction) and beam-steerability (~10°).

Second, we performed a tradespace analysis on multiple ultra-wideband (UWB) single-element antennas and downselected the Shark, Koshelev, and Fractal antennas, with more detailed investigations performed on each. The Shark antenna was a promising candidate for achieving UWB radiation with a high transient gain due to its unique truncated bicone shape, and we set out to uncover design strategies for improving this over the SOTA. Systematic studies revealed that cone height (h) and distance-to-

backplane (d) parameters most heavily influenced bandwidth and gain; however, after parametrization and optimization, improvements in transient gain were not significant enough to continue pursuing this antenna design. The Koshelev antenna was capable of handling GWs of input power, however, lacked bandwidth and high transient gain values. After thorough tradespace studies of single elements and antenna arrays, an optimized Koshelev 4x4 antenna array was found to be 22% smaller while exhibiting 1.4× higher transient gain (therefore higher power density), 24% better aperture efficiency, and the same bandwidth % (900 MHz +/- 100 MHz), but with a ~5° loss in beam-steerability as compared to the state-of-the-art balanced antipodal Vivaldi antenna. Measured results from our Koshelev element prototype agreed well with the simulation results. The Fractal antenna is known for its high fidelity and capability to achieve an UWB response in a small aperture area thanks to its complex and non-uniform patch shapes. Compared to the original Fractal antenna array, our optimized Fractal antenna array achieved 20% more bandwidth without increasing the physical aperture area, and a wide-steering (+/- 60°) was maintained. However, the physical size of the Fractal antenna is not big enough to achieve the desired power density levels. A spin-off effort from the tradespace analysis of the Fractal antenna array focused on developing a machine-learning (ML) based optimization algorithm and associated graphical user interface for antenna metrics prediction. Application of the ML algorithm to a fractal antenna yielded a 9% increase in bandwidth and 6% reduction in aperture area with >90% less computational time than conventional optimization.

Reporting

Results from this work were reported in monthly status reports (MSRs) submitted to ONR. These reports were compiled annually, and are available on DTIC as part of Annual Reports. Biannual technical reviews/exchanges were held in a range of formats including on-site, virtual, and externally in conjunction with the DEPS meeting. Abstracts and presentations for these have been compiled, and are available on DTIC. Please see Table 1 for a list of all reports available on DTIC. Final summary reports for a majority of the OSPRES Grant sub-projects are compiled herein, along with presentations from the final OSPRES Program Review (held November 2 2022 at UMKC).

We have found that adhering to a consistent reporting template (problem statement; tasks breakdown and status; new progress; technical results; summary; etc) helped maintain clarity and continuity in reporting from the multiple sub-project leads, as well as keep projects on track; however we continue to explore options for finding the right balance between clarity and reporting workload/length, with a mixture of shorter monthly and longer quarterly reports being one option. Further, the collection of more comprehensive summary reports upon suspension/transfer/completion of sub-projects was important in archiving knowledge. The agility to start and stop sub-projects was useful in maintaining nimbleness and efficiency; and if anything we would recommend evaluating, summarizing, and breaking off certain sub-projects sooner, especially those which ended up diverging from the initial objective. Biannual review and technical exchanges were imperative for soliciting feedback from collaborators, external experts, and stakeholders,

and the virtual option is a nice complement to in-person meetings to keep costs and resources down, especially if this means being able to keep up a biannual frequency.

Table 1. Summary of OSPRES Reports on DTIC with accession numbers. Note that some of the Biannual Review packages combined both Grant and Contract work.

Report	DTIC Accession Number	Distribution
Annual Report 2018 (Oct 2017–Sept 2018)	AD1065124	A
Annual Report 2019 (Oct 2018–Sept 2019)	AD1157712	A
Annual Report 2020 (Oct 2019–Sept 2020)	AD1192322	A
Annual Report 2021 (Oct 2020–Sept 2021)	AD1192323	A
Annual Report 2022 (Oct 2021–Sept 2022)	AD1192324	A
Binnual Review Spring 2018	AD1122640	D
Biannual Review Fall 2018	AD1157956	C
Biannual Review Spring 2019	AD1122782	D
Biannual Review Fall 2019	AD1121767	C
Biannual Review Fall 2020 (Contract only)	AD1122712	D
Biannual Review Fall 2020 (Grant only)	AD1121741	A
Biannual Review Spring 2021	AD1132980	A
Biannual Review Fall 2021	AD1192321	A

Outputs

Outputs from the OSPRES program, including both the OSPRES Grant (POP = September 30 2017 – September 29 2022) and OSPRES Contract (POP = March 7 2018 – March 7 2023) include, at the time of this final report:

- 34 students graduated (15 BS, 12 MS, and 7 PhD), and ~10 more with degrees in progress;
- 13 peer-reviewed journal publications, 5 journal publications submitted/under revision, and at least 10 manuscripts in preparation;
- 45 conference publications;
- 53 conference presentations;
- 10 theses and dissertations, with several more forthcoming;
- 14 IP disclosures
- 3 provisional patent applications, 2 non-provisional patent applications, and 1 issued patent.

A full list of outputs can be found in Section 4.

2.2. Sub-Project Overview: Timeline and Status

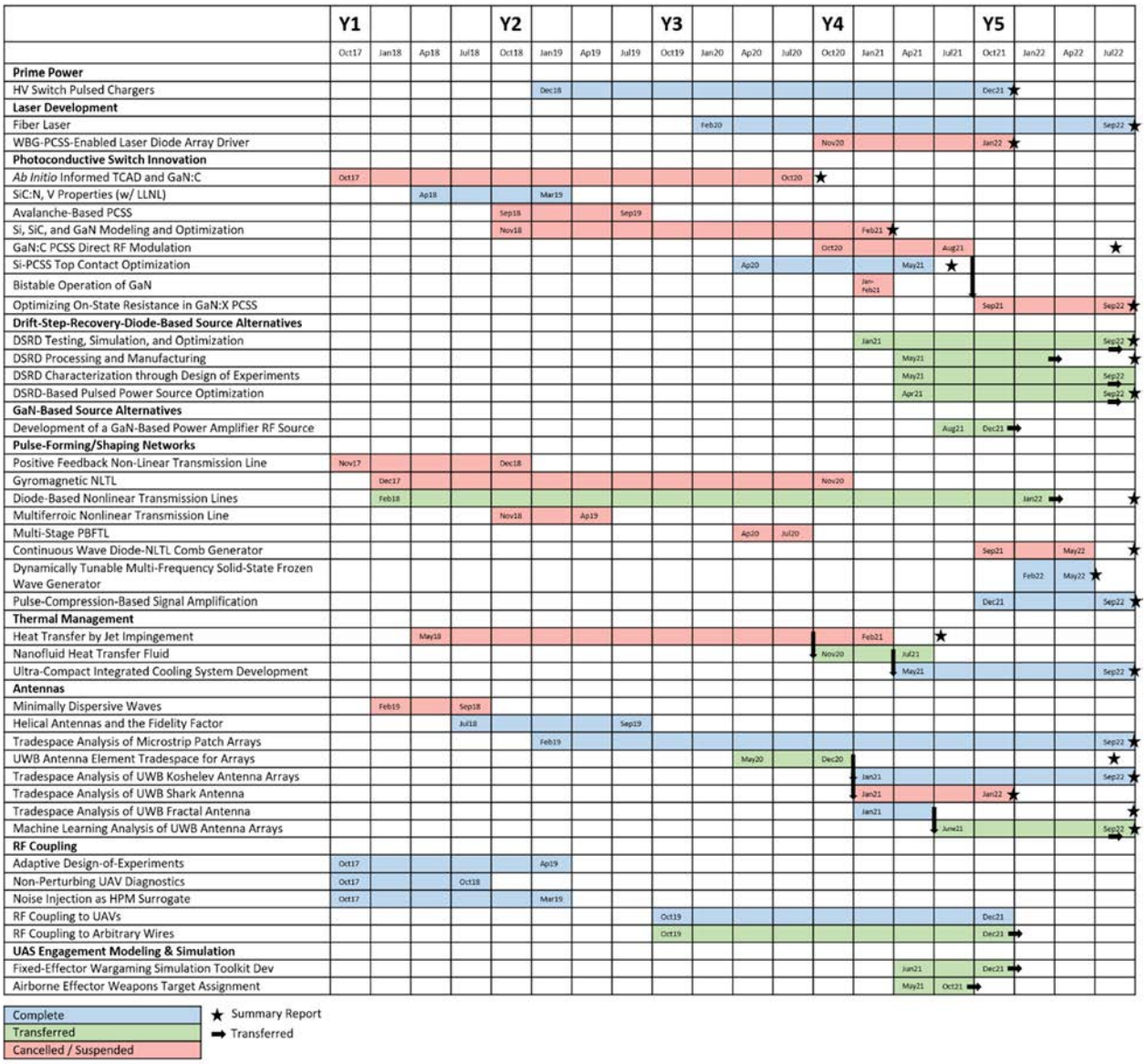


Chart 1. OSPRES Grant sub-projects, timelines, and status.

Summary Reports	**Date**
Ab Initio Informed TCAD and GaN:C	October 2020
Si, SiC and GaN Modeling and Evaluation	February 2021
Jet Impingement Thermal Management System	July 2021
Si-PCSS Top Contact Optimization	August 2021
A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Architecture for Pulsed Power Applications	December 2021
Wide-Band-Gap PCSS-Enabled Laser Diode Array Driver	January 2022
Tradespace Analysis of UWB Shark Antenna	January 2022
Dynamically Tunable Multi-Frequency Solid-State Frozen Wave Generator	May 2022
Tradespace Analysis of Ultra-Wide-Band Antenna Elements	August 2022
Direct RF Modulation Using GaN:C	August 2022
Fiber Lasers and Amplifiers	January 2023
Characterizing and Optimizing On-State Resistance in GaN:X PCSS	January 2023
Drift-Step-Recovery Diode (DSRD) Testing, Simulation, and Optimization	January 2023
Pioneering Drift-Step-Recovery-Diode (DSRD) Processing and Manufacturing	January 2023
DSRD-Based Sub-Nanosecond Pulse Power Source Optimization	January 2023
Diode-Based Nonlinear Transmission Lines	January 2023
Continuous Wave Diode-NLTL Comb Generator	January 2023
Pulse-Compression-Based Signal Amplification	January 2023
Development of Jet Impingement and Ultra-Compact Thermal Management Systems	January 2023
Tradespace Analysis of an Array of Electrically Small Antennas	January 2023
Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna	January 2023
Tradespace Analysis of Ultra-Wide-Band (UWB) Fractal Antenna	January 2023
Machine Learning Analysis of Ultra-Wide-Band (UWB) Antenna Arrays	January 2023
Transfers	
UAS Engagement Modeling & Simulation: Airborne Effector Weapons Target Assignment (PTERA Contract)	October 2021
RF Coupling to Arbitrary Wires (DARPA WARDEN)	December 2021
UAS Engagement Modeling & Simulation: Fixed-Effector Wargaming Simulation Toolkit Development (PTERA Contract)	December 2021
Development of a GaN-Based Power Amplifier RF Source (PTERA Contract)	December 2021
Diode-Based Nonlinear Transmission Lines (OSPRES Contract/PTERA)	
DSRD Testing, Simulation, and Optimization (PTERA)	September 2022
DSRD-Based Pulsed Power Source Optimization (PTERA Grant)	September 2022
Machine Learning Inspired Tradespace Analysis of UWB Antenna Arrays (PTERA Grant)	September 2022

Chart 2. List of OSPRES Grant summary reports available with original publication dates as well as key sub-project transfers. These are compiled in Section 3 of this report.

3 SUMMARY REPORTS

3.1 A Scalable Multilevel Modular 10 kV Silicon Carbide MOSFET Architecture for Pulsed Power Applications

(Faisal Khan; Originally published in the December 2021 MSR)

3.1.1 Executive Summary

Within the scope of this project, the MIDE team has designed and developed multiple versions of a custom HV switch that can function as an inexpensive alternative to the commercial BEHLKE switches in terms of performance, cost and availability. To this end, the team has developed a modular series-connected SiC MOSFET architecture and fabricated an HV switch based on this topology powered by a custom isolated gate driver and precision voltage balancing in the 10-kV and 1-kV/ns class. The proposed voltage balancing method achieves <1.1% voltage mismatch under steady-state and switching transitions. Series connection of MOSFETs can mask the underlying limitation of voltage blocking capability of a single device and potentially attain ultra-high voltage blocking capability. Each module of the proposed HV switch consists of four series-connected 1.7 kV rated SiC MOSFETs, yielding a breakdown voltage of 6.8 kV, and driven by a single custom 10 kV rated isolated gate driver. The proposed HV switch consists of two identical modules, thereby rated for a theoretical voltage blocking limit of 13.6 kV. One gate driver per module, a limited number of passive components (e.g., coupling capacitors, resistors, etc.) per module lead to low-cost fabrication and simpler operation of this HV switch. The modularity of the proposed HV switch introduces a unique capability of scaling up the voltage rating by stacking modules to meet potential application requirements without a complete design overhaul. Simulation and experimental results demonstrate excellent voltage balancing among the individual MOSFETs of each module during switching transients and steady states. A maximum voltage imbalance of <80 V was recorded among the individual MOSFETs in the HV switch at a supply voltage of 6 kV and a switching frequency of 15 kHz during the first run. The switch has been eventually tested at 10 kV and 1 kHz switching frequency to test the voltage withstanding capability.

3.1.2 Objective

Primary Problem: Commercially available high-voltage solid-state switches made by BEHLKE are the best in SWaP-cooling, but are expensive, have long lead times (2–3 months), and are made outside of the US. For the Navy afloat mission to be successful, we need a sustainable supply of US-manufactured switches at a much lower cost.

Solution Space: Design and demonstrate modular high-voltage (~10 kV) and fast (repetition frequency = 100 kHz) solid-state switches using a combination of series- and parallel-connected commercially available inexpensive discrete MOSFETs and custom high-voltage (~10 kV) isolated gate drivers.

Sub-Problem: Voltage balancing among the series-connected MOSFETs, minimization of gate signal delays, cooling of the individual MOSFETs, balancing resistors, high-voltage isolation required for the power supplies, and the controlling pulse width modulated (PWM) signal as well as differential voltage feedback measurement across

individual MOSFETs. A gate driver capable of providing sufficient galvanic isolation for the power supply and gate-driver signal of the (high-side) driver IC is required to drive the HV switch. In addition, the high switching speed of the SiC MOSFETs in the HV switch module leads to high dV/dt, and introduces considerable common-mode (CM) current circulating the gate driver and control circuit, thereby posing a potential risk to the normal operation of the HV switch. A low coupling capacitance of the gate driver power supply can minimize this CM current. To this end, a custom gate driver with 10 kV isolation and low coupling capacitance (< 20 pF) is designed and developed to drive the modular HV switch.

Deficiency in the SOTA:

1. BEHLKE-made switches are expensive. For instance, a single HTS-151-30 switch costs around $5,000.
2. BEHLKE switches along with direct liquid cooling units occupy a considerable amount of space. For instance, an HTS-151-30 switch from BEHLKE has a footprint of approximately 225*85*75 mm without considering the liquid cooling system. Some key parameters of this switch are as follows.
    (a) Maximum operating voltage = 15 kV
    (b) Maximum continuous load current = 2.52 A (without cooling), 30 A (with liquid cooling)
    (c) Maximum turn-ON peak current = 300 A (pulse width = 200 μs, duty cycle <1%)
    (d) Turn-ON resistance = 1.3 Ω
3. Once the switching frequency is greater than 10 kHz, a liquid cooling system is required to operate the BEHLKE switch.
4. Without liquid cooling, the maximum continuous power dissipation (P_{cont}) of the BEHLKE switch is limited (e.g., for HTS-151-30, P_{cont} is 10 W without liquid cooling).
5. At a higher switching frequency (>20 kHz), the BEHLKE switch requires multiple ancillary DC power supplies, i.e., 5, 15, and 60 V.
6. The switches made by BEHLKE cannot be reconfigured to withstand a higher voltage exceeding their recommended rating. BEHLKE offers separate products to operate them at higher voltage/currents.

3.1.3 Technical Background

With the rapid advancement of wide-bandgap (WBG) semiconductor devices, applications of power electronics have increased manyfold. WBG material (e.g., SiC, GaN) based semiconductor devices (e.g., MOSFET, IGBT, etc.) undeniably edges the traditional Si-based semiconductor devices in some key performance metrics including but not limited to dielectric field strength, breakdown voltage, thermal reliability at high temperature, form factor [1]. Low conduction loss (due to low ON-resistance), low switching loss (due to low gate charge) of WBG devices enable higher switching speed,

and lead to a diminished requirement of thermal management compared to Si devices, thereby increasing the power density of an entire system reliant on semiconductor devices. The typical junction temperature of SiC-based devices is close to 200 °C which is approximately 50 °C higher than the typical junction temperature of Si-based devices [2]. This property coupled with excellent thermal conductivity allows the SiC devices to reliably operate at a higher temperature without introducing significant performance de-rating as opposed to the Si devices.

MOSFETs, in general, are inherently faster compared to other types of semiconductor devices (e.g., IGBT, thyristor, etc.). Therefore, WBG MOSFETs are predominantly chosen in high-voltage and high-speed power electronics applications, such as high-voltage pulse generator, electric vehicle powertrain, industrial motor drives, X-ray machines, pulsed power system, etc over other switch types. Lower switching loss and lower ON-resistance of the GaN MOSFETs notwithstanding, the maximum breakdown voltage (900 V) of the commercial-off-the-shelf (COTS) GaNFETs is lower than that of the COTS SiC MOSFET (3300 V) [3], [4]. Therefore, SiC MOSFETs are preferable in high-voltage and high-speed power electronics applications as an alternative to Si devices.

Recent advancement in SiC technology is mirrored in the gradually increasing blocking voltage capability of COTS SiC MOSFETs as evidenced by the new generation of commercially available SiC MOSFETs with a voltage breakdown rating of 3.3 kV. Testing of some of the high-voltage (10-15 kV rated) SiC modules has been demonstrated in select research laboratories. [5], [6]. However, commercialization of these modules seemingly not forthcoming due to excessive manufacturing cost and design complexities. Series connection of multiple low-cost COTS SiC MOSFETs or multilevel converter topologies is two intriguing approaches to attain higher voltage blocking capability. Notwithstanding the considerable advantages of the multilevel converter topologies in terms of low common-mode voltage, low dv/dt stress, and radiated electromagnetic interference to a lesser extent compared to the series-connected MOSFETs [7]–[9], features such as lesser cost, relatively simpler construction, higher efficiency related to the series-connected MOSFET tip the scale in favor of this approach.

Series connection of multiple low-cost COTS SiC MOSFETs is an intriguing cost-effective solution to the increasing demand for semiconductor devices with a high voltage blocking capability and high-speed compatibility. That being said, ensuring equal voltage stress across the MOSFETs in a series stack during the turn-OFF period (steady-state) and switching transients (dynamic state) is a major design challenge for researchers in this field.

Parameter variation of the switching devices, unsynchronized gate drive signals, non-optimized trace layout can lead to unequal voltage exposure across the series-connected MOSFETs in a stack. The unbalanced voltage distribution among the series-connected switches can subject to single or multiple switches to overvoltage stress beyond their rated values resulting in the failure of these switches. This event can subsequently lead

to cascaded failures of all switches in a series stack, thereby leading to complete failure of the device which is catastrophic. To that end, mitigating the voltage imbalance issues pertaining to the series-connected switch is a major design consideration for the researchers working in this field.

Steady-state voltage balancing can be attained by paralleling balancing resistors across each switch connected in series [1], [10]–[23]. However, there is a tradeoff between the level of voltage imbalance at steady-state and losses due to leakage current [20]. As opposed to the relatively simpler design process of voltage balancing during the steady-state, a more sophisticated approach is required to address the dynamic voltage balancing issues. Researchers, working in this field, have proposed a number of approaches as of now to address this issue with a certain amount of success. The techniques proposed to ensure voltage balancing during switching transients can be classified into two major categories, namely- load-side techniques [24]–[27], and gate-side techniques [28]–[32].

The load-side technique is largely reliant on the utilization of passive snubbers, which are among the simplest forms of voltage balancing schemes. In this scheme, snubber capacitors coupled with snubber resistors (RC snubber) and/or diodes (RCD snubber), are connected in parallel with individual power switches. The capacitances of the snubber capacitors are required to be at least five to ten times the output capacitances of the semiconductor switches [24] to effectively control the dynamic voltage imbalance at the expense of the increased amount of snubber power loss and extended commutation time of the switches. In [25], a RCD snubber was introduced in the dynamic voltage balancing scheme for a series-connected HV switch made from two 1.7 kV rated MOSFETs. A RC snubber was used in [27] to minimize the dynamic voltage imbalance of a developmental series-stacked HV switch. To address the fundamental problem of high snubber losses associated with a snubber scheme, a strategy has been proposed in [26] that involves the partial discharge of snubber capacitors during a switching cycle leading to reduced reset current surge and reduced power loss. However, one onboard power supply per switch is required in this proposed scheme, thereby increasing the footprint, and cost of the HV switch.

The active gate control method can be a feasible solution for the dynamic voltage balancing problems among the semiconductor switches in a series stack. This method involves manipulating the dynamic of operation of the switches in their active region and capitalizing on the relationship between the levels of the gate drive signal and the switching transient of the devices. Active voltage clamping circuits proposed in [28], [33], and auxiliary circuits proposed in [29], [30] based on active gate control mechanism aim at controlling the dynamic voltage imbalance in a series stack of switches by feeding additional charges back to the gate terminal to marginally turn the switches ON at the onset of a voltage overshoot event. More sophisticated active gate control methods are demonstrated in [31], [32], [34], where feedback control is employed in the gate-drive loop to regulate the slew rate (dv/dt) of the devices connected in series with respect to carefully defined reference signals to control the voltage overshoot during switching transients.

Another way to minimize voltage overshoot, thereby voltage imbalance in a series stack of switches caused by asynchronous gate signal delays during switching transients is to introduce controlled delays in the gate drive signals [12], [13]. The ingenuity of this approach lies in the fact that the switching speed of the HV switch remains the same while particular gate signals are slightly delayed by a precise amount to counteract the voltage overshoot pertaining to those switches. However, to ensure cycle-by-cycle control over the entire switch, feedback circuits and associated A/D conversion circuits are required in these methods [12], [18], [35], [36]. A considerable amount of time delay may incur on top of the feedback circuitry-controlled gate signal delays due to the delay in sensing and prolonged response time of the A/D conversion circuits. This may curb the high-speed switching capability of SiC MOSFETs, thereby nullifying the advantages associated with WBG devices, and leading to excessive voltage imbalance during initial switching cycles that put the entire switch at risk of a cascaded failure. A modified gate delay control method using a delay line IC to increase the resolution of the delay control step to 150 ps has been reported in [18]. This method allows the SiC MOSFETs to retain their switching capability at the rated maximum operating frequency. However, this method does not account for the problem of voltage imbalance during the initial switching cycles encountered in similar aforementioned works. To solve this problem, a voltage balancing technique under steady-state and start-up conditions based on digital time delay circuit is proposed in [37]. This technique features the capability of updating the initial delay time to account for the voltage imbalance during the startup of the HV switch. However, parameter fluctuations of the switching devices due to process variation during the manufacturing process can lead to the variation of the initial delay time. In addition, the auxiliary circuits associated with generating the delays in gate signal compound the overall cost and complexity of the entire HV switch. In [38]–[40], authors introduced a new wrinkle to the dynamic voltage balancing schemes in the form of adaptive gate resistance for a specific period during the turn-ON or turn-OFF time of the switch. However, attaining the required amount of change in gate resistance with precision timing is of utmost importance to ensure optimal voltage balancing, which is relatively complex to accomplish, and costly to implement. In [14], a voltage balancing scheme incorporating a gate-balancing core is introduced to synchronize the gate drive signals for all the series-connected power devices. However, the magnetic core increases the footprint of the device, and the margin for error in core design is slim, thereby compromising its practical implementation feasibility. An active voltage control technique incorporating a current source at the gate control side of the low-side switch is proposed in [17]. This technique is capable of ensuring voltage balancing during switching transients for the low-side switch only.

Capacitive coupling-based series-connected switches employ a single gate driver to drive an entire switch stack aided by a few coupling components [1], [19]–[21], [41]. As opposed to the active gate control-based voltage balancing methods, the switches in a series stack in the capacitive coupling method do not require individual gate drives, resulting in a more compact footprint and reduced manufacturing/fabrication cost. In [1], the capacitive coupling method is used to control dynamic voltage balancing among series-connected

MOSFETs. However, the design of the proposed HV switch is relevant for only two stages. A quasi-active gate control-based capacitive coupling method was proposed in [21] featuring a single gate driver. During the turn-OFF period, the gate-source voltage of the upper device of the series stack remains close to the threshold limit, thereby posing a risk of false turn-ON. Therefore, reliability and scalability issues plague this technique and compromise its implementation feasibility in practical applications. A two-stage GaN MOSFET-based HV switch featuring a capacitive coupling method is proposed in [41]. Unfortunately, the scalability of this method in terms of a higher number of stages requires experimental validation. In contrast with the passive snubber-based and active gate control-based dynamic voltage balancing techniques, the capacitive coupling-based technique offers superior response speed, simpler circuit operation, and reduced fabrication cost. That being said, ensuring steady voltage balancing with higher number of stages and higher operating voltage remains an area of continuous improvement in HV switch design.

The unavailability of standard isolated gate drivers at high-voltage levels (>5.7 kV) is another major design challenge in experimentally validating the efficiency of the designs of HV switches (as high-side switches) at high (>5.7 kV) voltage levels. Standard COTS isolated gate driver ICs along with standard isolated power supplies for the gate driver ICs lack adequate ruggedness to handle high dv/dt stress typically associated with SiC MOSFETs. To that end, developing a custom gate driver equipped with adequate voltage isolation for the power supplies and the control signal for the gate driver IC is of equal importance as designing a HV switch.

In this report, a capacitive coupling-based modular series-connected HV SiC switch design with excellent voltage balancing has been documented. The proposed method takes advantage of the modular approach to offer scalability to cater to high-voltage applications without the need for a complete redesign and rebuild. The modularity requires the passive components (e.g., capacitors, diodes) in a module to be able to only withstand the voltage across that module instead of the entire HV switch, thereby reducing the voltage stress across those passive components. This eliminates the requirement of stacking many of those passive components in series leading to a compact footprint. A custom HV isolated gate driver with high (≈ 10 kV) galvanic isolation for the power supplies of the driver IC and optical fiber aided isolation for the control signal has been designed and developed to drive the modules of the proposed HV switch. Each module of the HV switch, therefore, consists of one custom isolated gate driver that drives four SiC MOSFETs connected in series coupled with coupling capacitors, diodes, and snubber circuits. The simulation and experimental results are in close agreements regarding voltage balancing among the series-connected 1.7 kV rated SiC MOSFETs in each module during both steady and dynamic states up to a DC supply voltage of 6 kV and a switching frequency up to 15 kHz.

3.1.4 Tasks, Milestones, and Status

1. Design a surface-mount MOSFET-based four-stage switch (6.8 kV rated) and control it using the in-house gate driver, then test its voltage-withstanding ability with a DC supply voltage up to 4–5 kV and evaluate the effectiveness of the thermal management at its current state / DEC 2020 / Completed.

2. Design and develop a modular HV switch (~10 kV rated) using the concept of the tested four-stage high-voltage switch module and an in-house modular gate driver to drive the modular switch /JAN–FEB 2021 / Completed.

3. Test the voltage withstanding ability of the modular HV switch with a DC supply voltage up to 10 kV and switching frequency up to 50 kHz using a resistive load (5–10 kΩ) and evaluate the effectiveness of the thermal management at its current state / FEB–SEP 2021 / Completed.

Details: *Achieving the necessary 10 kV breakdown voltage was a challenge in our previous version of the HV switch. Although the previous version was designed for 10 kV or higher, the gate driver circuit suffered from voltage breakdown on the PCB. We have identified the problem, and it was caused due to narrow spacing between two traces carrying a voltage gradient equal to the high-voltage (HV) supply. Since we experienced this failure, we have redesigned the PCB and used a new optical fiber TX-RX assembly to eliminate this problem.*

4. Test the isolation capability and evaluate the synchronization accuracy of the gate drive signal generated from the modular in-house gate driver / FEB–SEP 2021 / Completed.

Details: *A second test was conducted at a lower voltage using a different loading condition. The load was a series combination of a 200 kΩ resistor and a 9.6 kΩ resistor. Therefore, this combination worked as a voltage divider, and we measured the voltage across the 9.6kΩ resistor. The divider ratio was 21.833:1.*

5. Encapsulate the gate driver board with potting material with a high (~15–20 kV) breakdown voltage rating to prevent possible flashover/arcing in between the HV switch and this board / MAR–SEP 2021 / Ongoing.

Details: *The entire circuit assembly including the driver PCB was immersed in di-electric oil to prevent any unwanted arcing through air, although the final design will use some sort of potting materials for packaging ease. This technique not only resolves the arcing issue, but it also improves the thermal distribution of the system. A complete system has been tested at 10KV, and it successfully withstands this voltage. A repetition rate of 1 kHz is used during testing. The load impedance was 300 kΩ.*

6. Design and fabricate a compact power conditioner circuit based on a 12 kV rated SiC switch made by BEHLKE (HTS 121-15) / APR–MAY 2021 / Completed.

7. Test this modular HV switch coupled with a Si PCSS device up to a DC supply voltage of 5–6 kV and a switching frequency of 50 kHz / SEP 2021/Ongoing.

8. Design and develop a 20 kV rated modular (two modules, each with four MOSFETs) HV switch based on the design concept of the 10 kV rated modular switch using 3.3 kV rated SiC MOSFETs (new product made by GeneSiC Semi) / Ongoing.

9. Design and develop a 20 kV rated modular gate driver based on a WPT based planar transformer topology to ensure adequate galvanic isolation (~30–40 kV) for the power supplies of the gate driver / Ongoing.

3.1.5 Methods and Approach

3.1.5.1 Architecture details

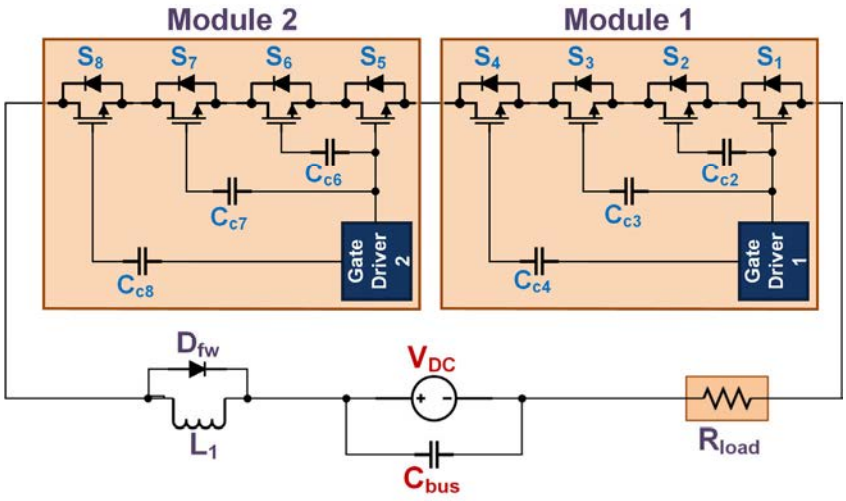


Figure 1. Schematic of the proposed modular HV switch.

The schematic of the proposed modular switch using series-connected SiC MOSFETs is shown in Figure 1. Two identical modules comprise the HV switch, and each module consists of four series-connected MOSFETs. Aside from the SiC switches (S_i, i= 1, 2…..8), the circuit of the HV switch contains coupling capacitors, C_{ci} (i=2, 3, 4, 6, 7, 8), snubber capacitors, C_{si} (i=1, 2…8), zener diodes, Z_{ia} and Z_{ib} (i=1, 2….8), gate resistors, R_{gi} (i=1, 2….8), ferrite bead, FB_i (i=1, 2….8), balancing resistors, R_{si} (i=1, 2…..8), gate-loop diodes, D_{ci} (i=2, 3, 4, 6, 7, 8), inductor L_1 and a freewheeling diode, D_{fw}. A DC bus capacitor bank, C_{bus} is connected across the entire switch, and incorporated in the fabricated HV switch prototype to reduce parasitic inductance stemming from additional wire-board connections. Two custom HV gate drivers are connected across the gate-source terminals of the rightmost MOSFETs (S_1, S_5) in each module. These MOSFETs are coined as the master MOSFETs throughout the rest of the paper for the ease of narration. The rest of the MOSFETs are termed slave MOSFETs and are mentioned as such throughout the rest of the paper as well. A detailed schematic diagram of a single module is illustrated in Figure 2.

3.1.5.2 Key Parameter Selection

A. Selection Criteria of Balancing Resistors

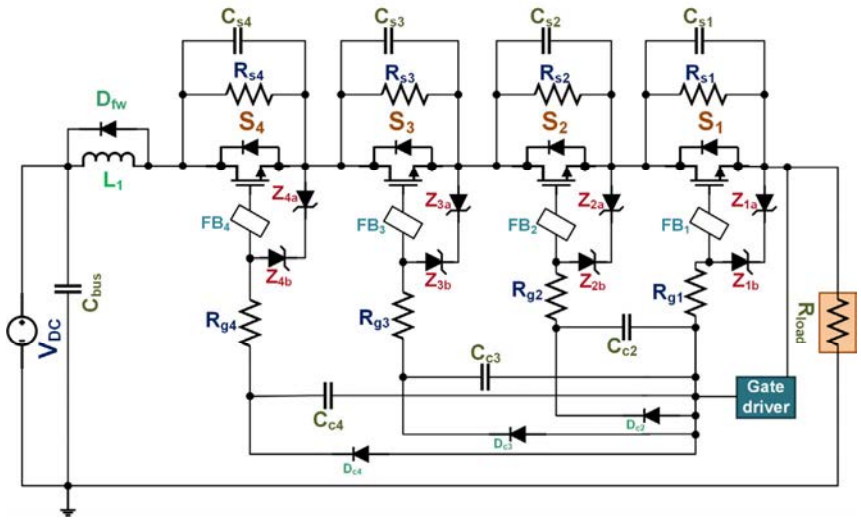


Figure 2. Schematic of a single module of the HV switch.

During the steady-state, the modular switch as a whole is subjected to the entire DC bus voltage. Two mechanisms primarily govern the degree of voltage imbalance among the series-connected MOSFETs in the series stack. Unequal leakage currents pertaining to the manufacturing process variations of the MOSFETs in the modular switch act as the salient instigator of the voltage imbalance during the steady-state. On top of that, probable voltage imbalance a mong the drain-source voltages of the series-connected MOSFETs at the end of the turn-OFF transition stage may carry over to the ensuing steady-state. Resistors can be connected in parallel to the drain-source terminals of the series-connected MOSFETs to minimize the aforementioned voltage imbalance issue associated with the steady-state. The selection of these resistors (R_{si}, i= 1, 2….8), termed as balancing resistors, is a trade-off between power dissipation and the level of voltage imbalance during the steady-state. The value of the balancing resistors required to ensure a steady-state voltage imbalance ratio below 10% can be determined from the following equation [1].

$$R_{\mathrm{si}} < \frac{V_{\mathrm{DC}}}{10 I_{\mathrm{DSS(max)}}}, i = 1, 2 \ldots \ldots 8 \qquad (1)$$

Where I_{DSS} is the leakage current at V_{GS} = 0, and V_{DC} is the supply voltage. Lower R_s leads to a reduced level of voltage imbalance at the expense of higher static power dissipation. In practice, resistors are chosen to have values that are one magnitude less than the equivalent OFF-state resistance of the MOSFETs to direct the leakage current passing through them instead of the MOSFETs.

B. Selection Criteria of Coupling Capacitances

The influence of the coupling capacitors on the dynamics of the switching transient of the individual MOSFETs of the proposed modular switch is pronounced. The gate-source capacitances of the slave MOSFETs are charged and discharged by the discharging and charging of the coupling capacitors respectively. This implies that the amount of gate

charge required to completely turn the slave MOSFETs ON and OFF are solely provided by these coupling capacitors. To that end, the stored charge in the coupling capacitors during the turn-OFF period should be greater than the total gate charges (Q_{gi}, i= 2, 3, 4, 6, 7, 8) of the slave MOSFETs.

In the proposed architecture, the coupling capacitor associated with the slave MOSFET located farthest from the master MOSFET in each module experiences the maximum voltage stress which does not exceed a level of $3V_{DC}/8$ thanks to the modularity of the proposed switch. The voltage level experienced by C_{c2}, C_{c6} is $V_{DC}/8$, and in the case of C_{c3}, C_{c7} it is $2V_{DC}/8$. The required capacitance values should satisfy the following equation.

$$C_{ci} > \frac{Q_{gi}}{(i-1) * V_{DC}/8}, i = 2,3,4 \qquad (2)$$

$$C_{cj} > \frac{Q_{gj}}{(j-5) * V_{DC}/8}, j = 6,7,8 \qquad (3)$$

The typical value of the gate charge (Q_g) of the used MOSFET is 13 nC under a DC bus voltage of 1.2 kV and a load current of 2 A. From equations (2) and (3), the minimum value required for the coupling capacitors at 6 kV can be determined as 5.7 pF, 8.7 pF, and 17.3 pF. The proposed modular switch includes coupling capacitors with values 7 pF, 10 pF, and 21 pF, thereby closely approximating the theoretical values.

C. Selection Criteria of Gate Resistors

SiC MOSFETs have superior switching speed compared to their Si counterparts, reaching a slew rate as high as 50V/ns [42]. However, the extremely high slew rate in addition to the package and circuit stray inductances can lead to voltage overshoot ($L*di/dt$) and subsequent ringing [43], [44]. A compactly designed PCB can contribute significantly to the reduction of stray inductance, thereby mitigating the aforementioned problem to a great extent. That said, minimum creepage and clearance requirements for safe high-voltage operation can inhibit the ability of the circuit designer to optimize the PCB footprint. An alternative solution can come in the form of sufficiently large gate resistors at the expense of increased loss. In our proposed design, we have incorporated 15 Ω gate resistors as a tradeoff between the level of gate ringing and additional loss.

D. Selection Criteria of Snubber Capacitors

Snubber capacitors (C_{si}, i= 1, 2…..8) connected across the drain-source terminals of the series-connected MOSFETs, minimizes the mismatch in slew rates (dV_{dsi}/dt, i= 1, 2,…..8) during switching transients. Unlike traditional snubber capacitors, small valued (in the range of picofarads) capacitors are connected across the drain-source terminals of individual MOSFETs. Snubber capacitors with large values prolong the turn-OFF transition of the individual MOSFETs, thereby increasing the switching loss. Conversely, the absence of snubber capacitors curtails the transition time during the turn-OFF period of the switch at the expense of too big of a mismatch between the slew rates of the

individual MOSFETs that can potentially lead to voltage imbalance of excessive proportions. To that end, a tradeoff is required during the selection of the snubber capacitor values. In the fabricated HV switch prototype, 100 pF ceramic capacitors have been used as snubber capacitors.

E. Selection Criteria of Ferrite Bead

Mitigation of voltage overshoot, electromagnetic interference (EMI) associated with the ultrafast switching characteristic (i.e., high *di/dt*, high *dv/dt*) of the SiC devices is of paramount importance in any high-voltage application [44], [45]. Ferrite bead can assist gate resistors to further minimize the aforementioned issues related to ultrafast switching of the SiC devices [45]. Ferrite bead, in essence, mimics the performance of an RF choke, thereby incorporating high resistance (hundreds to thousands of ohms) in the gate loop at relatively high frequency (tens to hundreds of MHz). However, it barely impacts the circuit's operation at low frequency (tens to hundreds of kHz). Therefore, a carefully selected ferrite bead that offers high impedance at the frequency of interest (ringing frequency) can drastically elevate the performance of the SiC switch. We have incorporated SMD ferrite beads with 2 kΩ resistance at 30 MHz in the gate loop circuits of the series-connected MOSFETs.

3.1.5.3 Design Details of a Custom HV Isolated Gate Driver

The modular 10 kV rated HV switch proposed by the authors in this report requires two isolated HV gate drivers, one for each module of the HV switch. The required isolation rating of each gate driver is at least 10 kV to ensure reliable operation of the HV switch. However, commercial-off-the-shelf (COTS) gate driver modules have isolation ratings as high as 5.7 kV [46], [47]. This rating implies that COTS gate driver modules are not equipped to drive a HV switch with a voltage rating greater than 5.7 kV. Prior studies on HV isolated gate drivers showcased designs based on some experimental switch modules (e.g., CPM3-10000-0350, XHV-9, XHV-7 developed by CREE) [48]–[51]. However, none of the gate driver designs has been realized as a commercial high-voltage isolated gate driver solution as of now. To this end, the authors have proposed and developed a working prototype of a modular (two modules) high-voltage (10 kV rated) isolated gate driver ensuring synchronization of the gate signals for the two modules of the proposed HV switch. Two levels of isolation are needed to be incorporated in the HV isolated gate driver design, namely, i) isolation of the control/PWM signal, and ii) isolation of the power supplies of the gate driver IC. Control signals (e.g., signals for pulse width modulation, overcurrent protection, temperature sensing, etc.) can be isolated by means of optocouplers [52], coreless transformers [53], classical transformers [54], optical fibers [55], etc. Optical fiber is the preferred choice in most cases to provide isolation for the control signals thanks to its superior immunity to noise coupled with high galvanic isolation capability.

Isolation required for the power supplies of the gate driver IC needs to satisfy two basic requirements- i) adequate high-voltage isolation, and ii) low coupling capacitance. The high voltage isolation barrier safeguards the primary side of the power supply from

disruptive ground loops, potential dielectric breakdown casualties caused by high voltage surges, and protects human operators at the control side from deadly electric hazards [56]. Low coupling capacitance (C_{iso}) minimizes the coupling of common-mode current (i_{CM}) from the power side to the control side caused by high *dv/dt* during switching transients of SiC MOSFETs and ensure reliable operation of the gate driver. Equation (4) underscores the influence of the coupling capacitance (C_{iso}) of the gate driver and the slew rate (*dv/dt*) of the SiC MOSFET on the common-mode current.

$$i_{CM} = C_{iso} \frac{dv}{dt} \tag{4}$$

Air core or tape-insulated transformers [48], [50], [57]–[59] with discrete windings, or PCB windings [49], [60], inductive power transfer (IPT) coils [61]–[64], optical fibers [51] are the basis of some of the methods proposed in the literature to isolate the power supplies of the gate driver IC. However, a majority of these approaches (e.g., transformer, IPT, etc.) lead to a large footprint whereas the optical fiber-based approach requires a bulky and expensive laser system, thereby compromising the feasibility of this approach.

A single module of the proposed 10 kV rated gate driver features three compact (≈ 1 sq. inch) 10 kV rated isolated DC-DC converters to provide galvanic isolation for the power supplies of the gate driver IC [65]. These converters, having a power rating of 6 W, can operate at an input voltage ranging from 24 V to 36 V, and capable of producing a regulated output. A 5.7 kV_{RMS} rated reinforced isolated gate driver IC with 2.5 A sourcing and 5 A sinking current capability, has been selected for the proposed gate driver module. The selected gate driver IC has a dedicated pin (V_{EE2}) for ease of application of bipolar supply that facilitates the supply of recommended negative voltage required to ensure reliable turn OFF of SiC MOSFET. An optical fiber link has been designed and developed using transmitters, receivers, and optical fiber that belong to the HFBR-0500Z series. The optical fiber link supports a data transmission rate of 5 MBd and can handle a breakdown voltage rating of 500 V/mm [66]. A DC supply voltage of 24 V powers the gate driver board. Three isolated DC-DC converters yield three voltage rails of +24 V, +5 V, and -5V respectively. The +5 V rail powers the input side of the gate driver IC as well as the receiver of the optical fiber link. A linear regulator (LM1086) scales down the +24 V rail to a regulated +20 V rail. The +20 V rail and the -5 V rails are connected to the output side of the gate driver IC to generate the recommended voltage levels (+20 V, -5 V) required for reliable switching of the SiC MOSFETs. Another linear regulator (LM1086) is incorporated in the design to generate a steady +5 V rail from the primary DC supply that

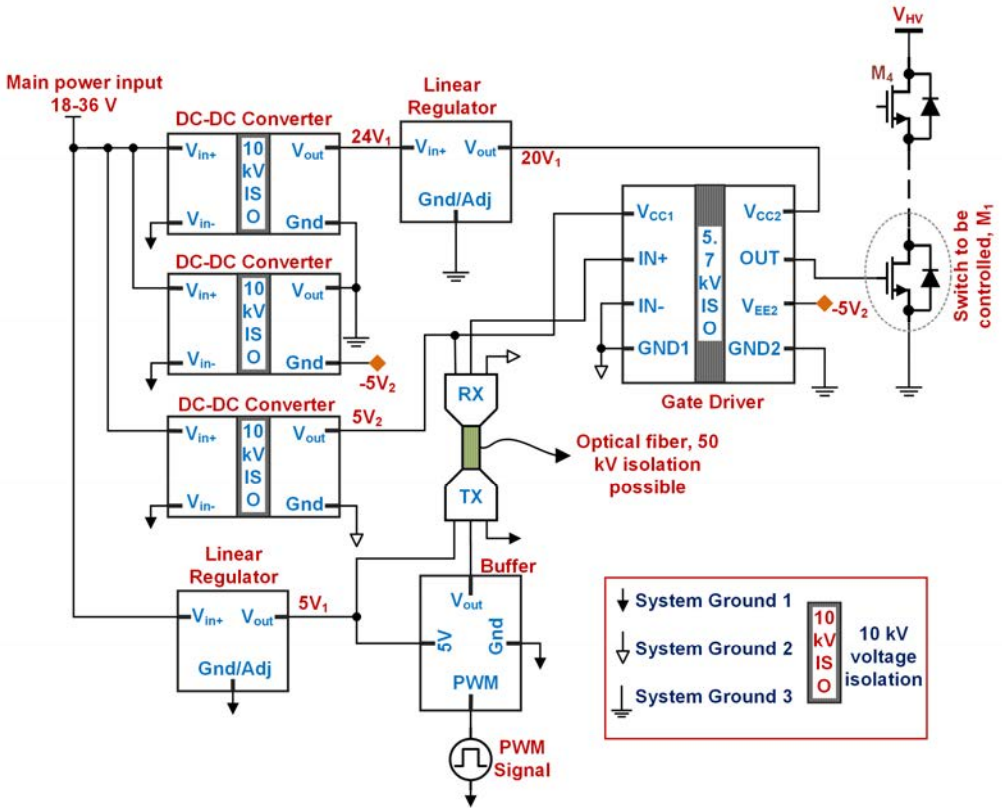


Figure 3. Schematic of a single module of the proposed gate driver.

is used to power the transmitter of the optical fiber link. The entire setup is shown in Figure 3.

The modular gate driver has six isolated DC-DC converters, three for each module as in the single module. However, both modules share the same input DC supply and a single buffer IC (SN75451) with dual outputs feeding identical PWM signals to two transmitters equally distanced from the buffer IC. The rest of the circuit designs of the two gate driver modules are quite identical, thereby eliminating the possibility of performance variation of the gate driver modules as much as possible. One of the major design concerns of a multi-output gate driver is ensuring synchronization of the gate drive signals. To that end, two gate driver ICs, one for each module, are placed equally apart from the receivers of two fiber-optic links in the PCB design. Board-to-board connectors are used to connect the modular gate driver board to the modular HV switch to reduce parasitic inductance in the gate drive loop as well as providing mechanical rigidity to the assembly of the HV gate driver and the HV switch. The traces from the output signals pins of the gate driver ICs to the board-to-board connectors are kept short and of equal length to ensure synchronization of the gate signals as well as further minimization of parasitic inductances

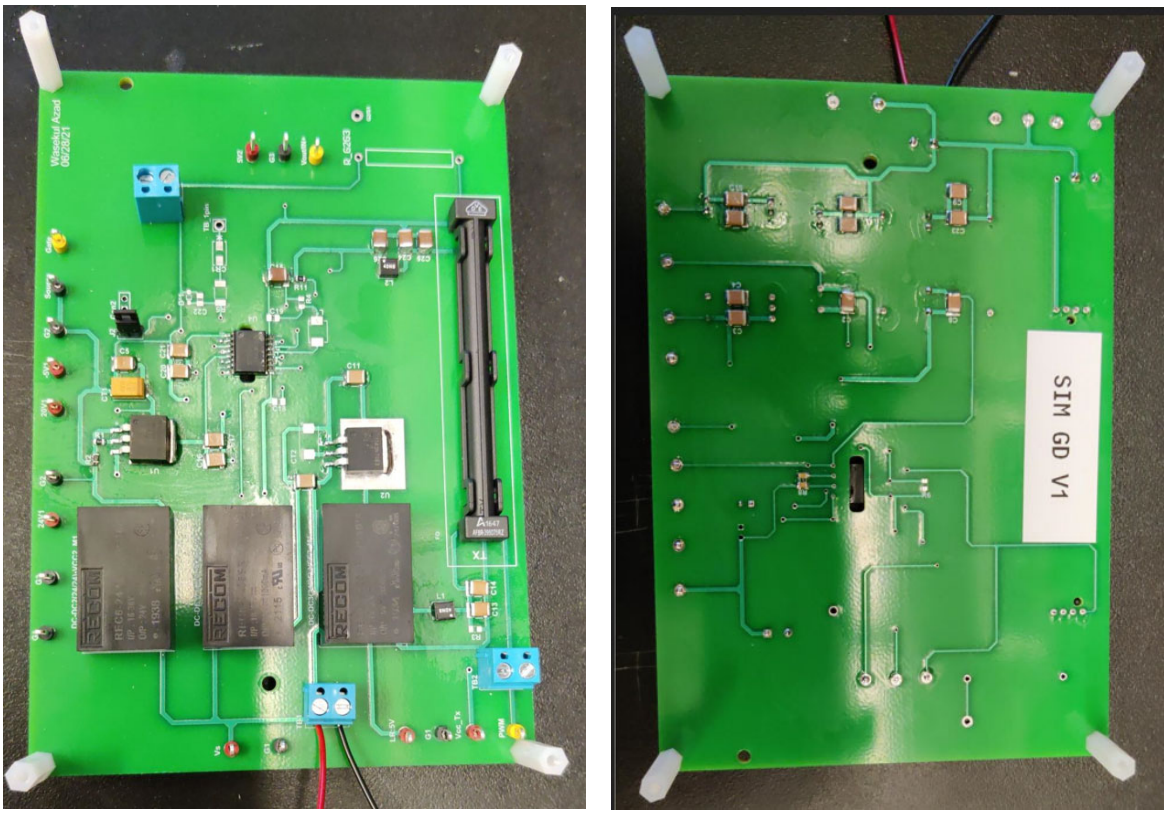


Figure 4. Actual photograph of the modified gate driver circuit showing the integrated optical link (TX) on the left figure.

in the gate loop of the modules of the HV switch. The schematic of a single module of the

modular HV gate driver and the fabricated modular HV gate driver board are shown in Figure 4.

The new MOSFET board shown in Figure 5 has two modules, and has the following +5V, -5V,24V,20V buses, and they all were tested stable and withing tolerance. Total Input current = 100mA. The signal integrity and rise/fall behavior of the new driver board have been shown in Figures 10 and 11.

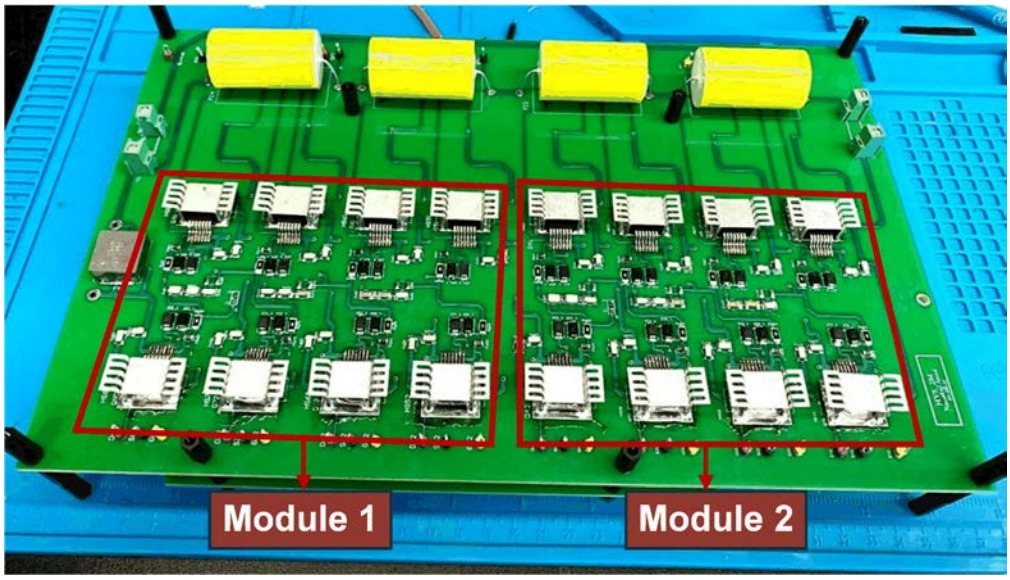


Figure 5. Fabricated prototype of the proposed 10 kV modular switch.

3.1.6 Results and Discussion

Phase I: A 6.8 kV rated four-stage surface-mount MOSFET developed in-house was successfully tested up to a DC supply voltage of 4 kV and at a switching frequency up to 20 kHz with a 3.2 kΩ resistive load. The proposed voltage balancing method achieves <1.1% voltage mismatch under steady-state and switching transitions. The proposed modular HV switch coupled with the custom in-house HV isolated gate driver was tested using a DC supply voltage up to 6 kV and at a repetition frequency up to 15 kHz using the 9.6 kΩ resistive load. Experimental results show reliable turn-ON and turn-OFF characteristics of the entire HV switch under the specified operating condition. The voltages measured across the drain-source terminals of the MOSFETs in a single module are shown in Figure 6 (VDC = 5 kV, $f$sw = 40 kHz, duty cycle = 50%). A maximum voltage imbalance close to 50 V was recorded among the drain-source voltages of the series-connected MOSFETs in a single module that experienced a DC voltage stress of 2.5 kV, thereby validating the effectiveness of the proposed voltage-balancing scheme. To test the entire switch at a higher voltage level, the voltage across the 9.6 kΩ load at a supply voltage of 6 kV and a repetition frequency of 10 kHz was measured and shown in Figure 7. The measured voltages across the drain-source terminals of the series-connected MOSFETs from both of the modules are depicted in Figure 8. In this configuration, each module experienced a maximum voltage stress close to 3 kV. A maximum voltage

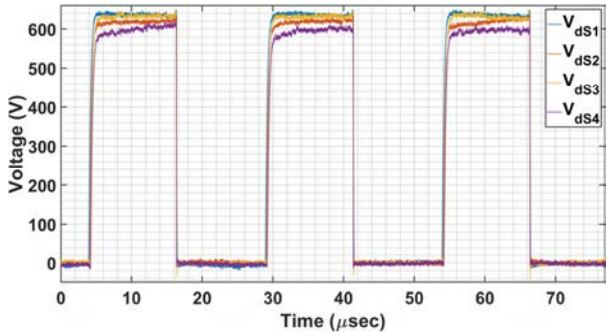


Figure 6. Experimental drain-source voltages measured across the individual MOSFETs in a single module (V_{DC}= 5 kV).

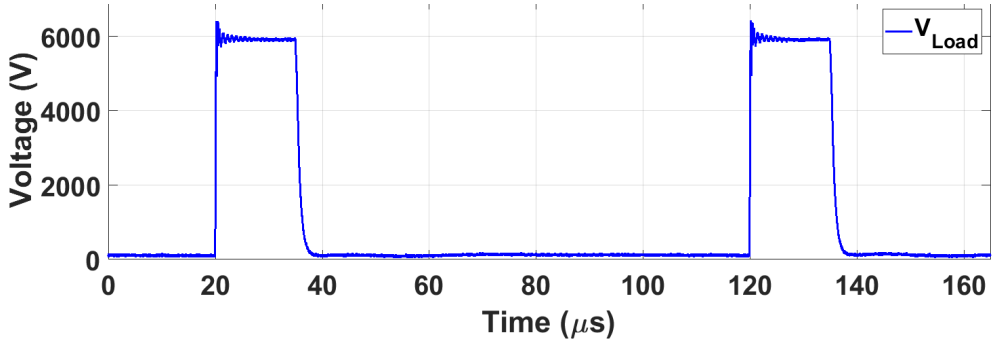


Figure 7. Voltage measured across the 9.6 kΩ resistive load (V_{DC}= 6 kV) to test the 10 kV switch.

imbalance close to 80 V was recorded among the drain-source voltages, which is negligible compared to the breakdown voltage rating of an individual MOSFET. The experimental results are in close agreement with the simulation results regarding voltage balancing among the series-connected 1.7 kV rated SiC MOSFETs in each module during both steady and dynamic states up to a DC supply voltage of 6 kV and a switching frequency up to 15 kHz.

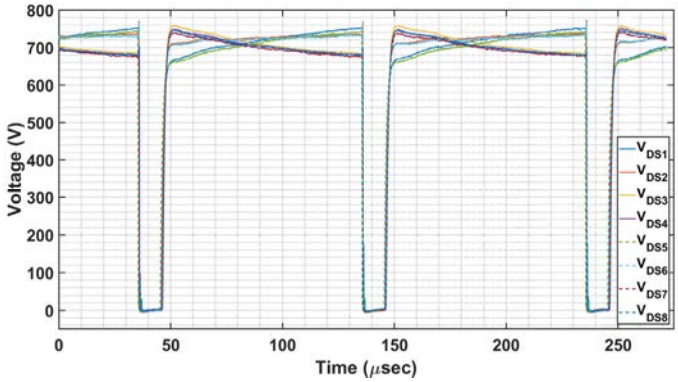
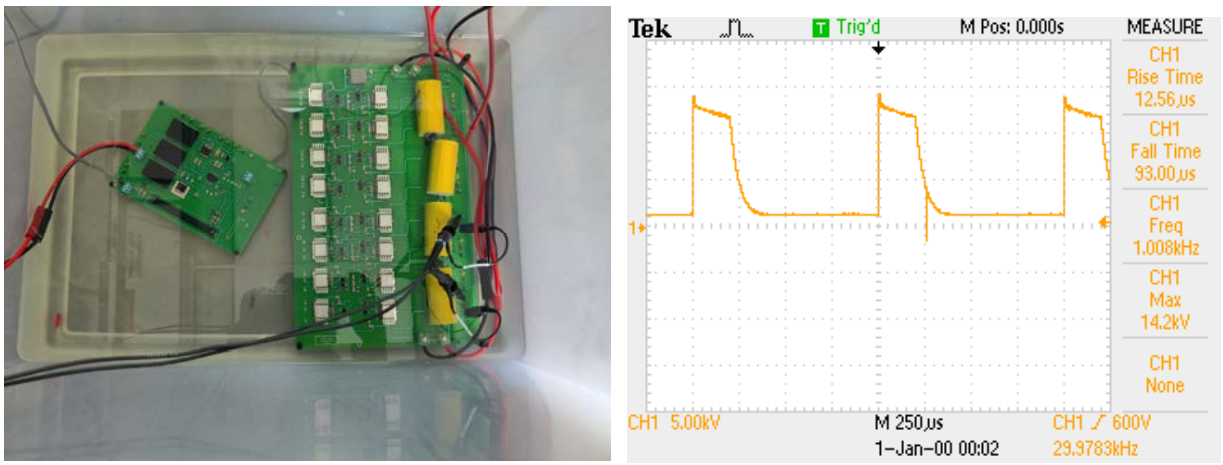


Figure 8. Experimental drain-source voltages measured across the individual MOSFETs in the entire HV switch (V_{DC}= 5 kV).

The lowest rise time was measured as 41 ns associated with the slave MOSFETs (S_4, S_8) located farthest from the master MOSFET in each module. The highest rise time belonged to the master MOSFETs (S_1, S_5) in each module, and recorded as 52 ns. The rise time of the HV switch can be approximated by the highest rise time associated with the series-connected MOSFETs. That being said, the recorded rise time of the proposed modular HV switch is still considerably lower compared to the COTS switches with similar voltage ratings.

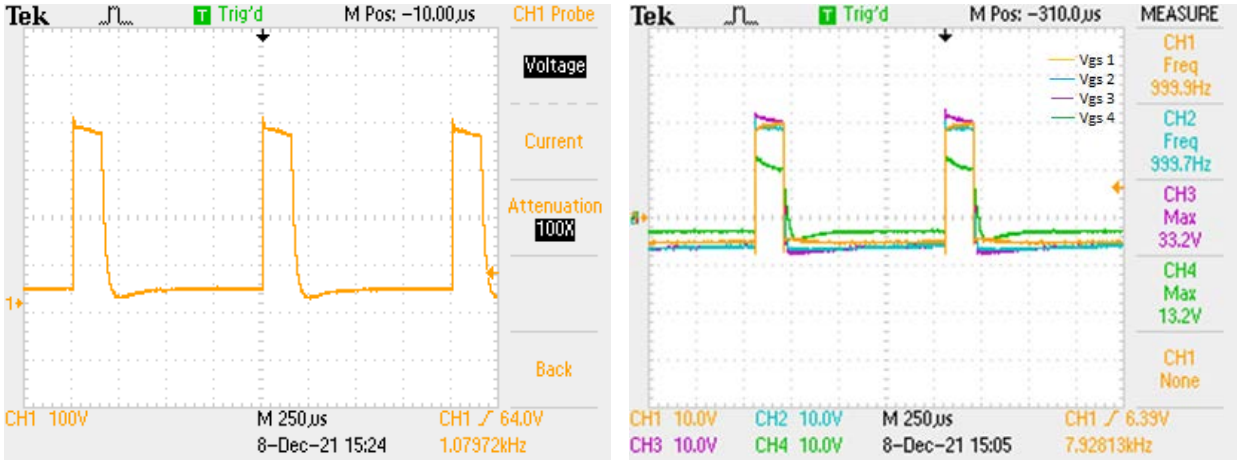
Phase II: A modular (two modules) 10 kV rated HV switch has been designed and a prototype has been developed using 1.7 kV rated SMD MOSFETs (C2M1000170J). An in-house 10 kV rated HV gate driver has been designed and incorporated with the HV switch to drive it (Figure 9). A manuscript on the HV switch and the custom isolated gate driver has been submitted to IEEE Transaction on Power Electronics. An insulating naphthenic dielectric oil has been acquired that meets the ASTM D-3487 specification. With the use of this dielectric oil, altered component placement and new TX-RX optical module, the newly designed gate driver and MOSFET PCB can safely withstand 10KV. At present, the prototype runs at Fsw = 1 kHz, d = 15%, V_{DC} = 10KV, and R_{load} = 300 kΩ. We are yet to test the circuit at 50 kHz switching to complete milestone 1.4.3. We need to test the circuit at much higher load current (load impedance = 5–10 kΩ), and we plan to do so in January. Our present setup especially the HV power supply limits us to test the circuit at significantly smaller load current.

At 10 kV, the gate driver circuit operates flawlessly, and the gate-source signals have the necessary integrity to avoid malfunctions. Results are shown in Figures 10 and 11.



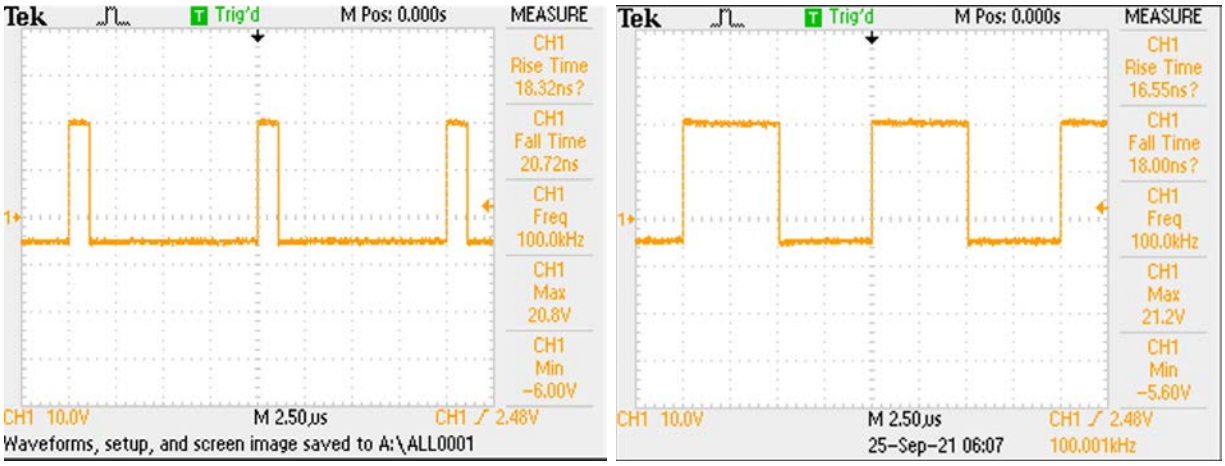
(a) (b)

Figure 9. (a) The modified 10 kV switching module (right) and the gate driver board (left) are immersed in dielectric oil, (b) switching characteristics of the module using a voltage divider probe. The output voltage swing is 10 kV (5 kV/division).



(b) **(b)**

Figure 10. (a) Voltage across the load, the voltage swing was 7.64 kV (b) Gate to source voltages of the four MOSFETs used in a module.



(a) (b)

Figure 11. Modified gate driver output (a) at f = 100 kHz, D = 50%, no load, (b) at f = 100 kHz, D = 10%, no load.

The entire circuit assembly including the driver PCB was immersed in naphthenic dielectric oil to prevent any unwanted arcing through air, although the final design will use some sort of potting materials for packaging ease. The system has been tested up to 10 kV, and we are yet to test the oil's dielectric strength at 20 kV.

3.1.7 Summary and Recommendations

In this report, a 10 kV rated multilevel modular high-voltage switch architecture based on capacitive coupling technique and associated voltage balancing scheme have been presented, and the concept has been verified through simulation and experimental results. The intricacies of the voltage balancing mechanism during switching transients

and steady-state have been explained in a simplified manner. Criteria for critical parameter selection pertaining to the modular HV switch have been discussed with necessary details. The design of a custom high-voltage (10 kV rated) isolated gate driver to drive the modular HV switch has been outlined in this report as well. The modular HV switch coupled with the custom isolated gate driver has been tested at a supply voltage up to 10 kV and at a switching frequency up to 15 kHz in a high-side configuration with a resistive load. A maximum voltage imbalance <80 V has been recorded which is negligible compared to the breakdown voltage rating of a single MOSFET. In addition, the gate drive signals originated from the modular HV isolated gate driver exhibit little to no synchronization delay. Simulation and experimental results validate the modular approach of the proposed HV switch, thereby ushering in an intriguing way to scale up the voltage rating of an HV switch without requiring complete redesign and reconstruction.

3.1.8 Outputs

Graduating student: Dr. Wasekul Azad, July 2021

Conference papers:

(1) A. N. M. Azad, S. Roy, A. Caruso and F. H. Khan, “A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuits,” 2021 IEEE Kansas Power and Energy Conference (KPEC)

(2) A. N. M. Azad, S. Roy and F. H. Khan, "A Single Gate Driver-Based Four-Stage High-Voltage SiC Switch Having Dynamic Voltage Balancing Capability," 2021 IEEE Applied Power Electronics Conference and Exposition (APEC).

Journal article:

A Custom High-Voltage Isolated Gate Driver Circuit Combined With Coupling, and Snubber Circuits for a Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Module, submitted to IEEE Transactions on Power Electronics

Invention disclosure:

An invention disclosure with the title “A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuits” has been filed by UM Technology Commercialization to protect the technology.

3.1.9 References

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3.2 Fiber Lasers and Amplifiers

(Scott Shepard)

3.2.1 Executive Summary

The primary goal of this project was to: reduce by half the cost of pico-second lasers that deliver hundreds of μJ per pulse, at pulse repetition rates on the order of hundreds of kHz (resulting in average powers up to 120 W and peak powers up to 100 MW). A secondary goal was to increase the operating power of this class of lasers to as high as possible. Via innovative design, as validated by simulation and calculation, we accomplished the goals within fiber laser amplifier embodiments (fed by a seed laser diode) in ways that also reduce the amplified spontaneous emission (ASE) noise.

Specifically, we found that a pre-burst pumping scheme can reduce the cost of a fiber laser amplifier by a factor of 40 (for a 2.5% duty cycle burst profile) and gain saturation can be used to design amplifier stages that suppress the overall ASE by 5,000 (for an overall power gain of 8 million). Laser/amplifier system cost can also be reduced (independent of burst duty cycle) by increasing the operating power.

Nonlinearities limit laser power in circular core fiber amplifiers. We increase the power by over two orders of magnitude by utilizing a tubular core; wherein symmetry breaking causes preferential nonlinear scattering to the inside of the tube, where it accumulates as an air-core mode. These permit a peak power of 10 GW, which enables the triggering of an entire array of up to 100 PCSS via a single laser/amplifier source, thereby eliminating the optical timing jitter constraint.

3.2.2 Objective

Primary Problem: High-average-power 1064-nm picosecond lasers are too large (over 1100 cm^3/W) and too expensive (over \$1000/μJ per pulse) for PCSS (photoconductive semiconductor switch) embodiments of HPM-based defense systems. For example, a laser of this class might occupy a volume of 1 m x 30 cm x 30 cm = 90,000 cm^3 and provide an average power of 50 W (thus, 1800 cm^3/W). Costs in this class range from \$100K to \$300K to drive our Si-PCSS applications.

Solution Space: Optically pumped ytterbium-doped optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight, and small-volume solution (with respect to traditional fiber and traditional free-space laser designs). Moreover, our novel optical amplifier tubes, might operate at far higher power levels (over 1000 times greater), thus driving an entire array of PCSS with a single amplifier – thereby reducing system costs and eliminating the optical pulse-to-pulse jitter constraints.

State-of-the-Art (SOTA): Free-space NdYAG lasers or Ytterbium-doped fiber amplifiers optimized for LIDAR, cutting, and other applications.

Deficiency in the SOTA: Optical pump power system costs (in either free-space or fiber lasers) are prohibitive for the PCSS applications until reduced by a factor of at least two.

Solution Proposed: Fiber lasers permit a pre-burst optical pumping technique (wherein we pump at a lower level over a longer time), which can reduce pumping costs by a factor of at least ten. To address the ASE and nonlinear impairments, we are pursuing the use of gain saturation and a staged design of different fiber diameters. We also apply these techniques to fiber amplifiers that incorporate our power amplifier tube in the final stage. The inclusion of our novel tubular-core power amplifier stage should permit a single final laser amplifier stage to trigger an array of several PCSS (eliminating optical timing jitter).

Relevance to OSPRES Grant Objective: The enhancement in SWaP-C^2 for the laser system enables PCSS systems for viable deployment via: a factor of 40 in pumping cost reduction of each laser; and a factor of *N* in system cost reductions as a single laser could drive *N* (up to 100) PCSS in an array, while also eliminating the optical jitter constraint.

3.2.3 Technical Background

Optical pump power system costs account for over 50% of the budget for each laser (in this class, for optical fiber as well as normal/free-space embodiments). For example, a laser in this class might deliver $240\ \mu J/pulse$ at a pulse rep-rate of 500 KHz, resulting in an average power, P_{ave}, of 120 W. We found that the cost of pumping such a laser (just to create the required population inversion) scales as c = 1.44 P_{ave} (with c in thousands of $ and P_{ave} in Watts) independently of how P_{ave} is shared between pulse energy and pulse rep-rate, as depicted in Figure 1. The 120 W benchmark system thus requires $172,800 in pump power cost.

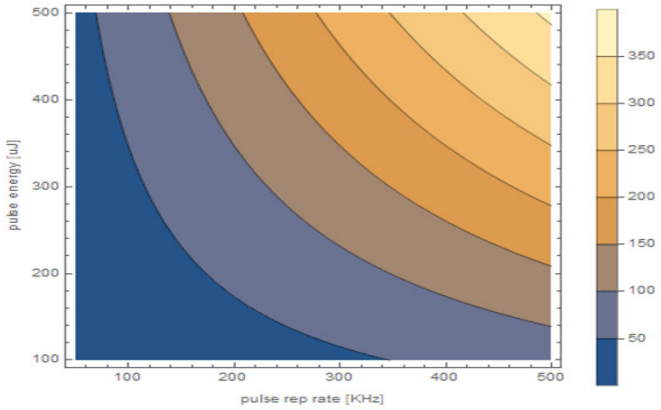


Figure 1. Pumping costs proportional to P_{ave} = (pulse energy) (pulse rep-rate).

In a normal/free-space laser the pump power is on when the output power is comprised of a burst of pulses and the pump power is turned off (or deflected) during the longer times of no output between bursts (otherwise, pumping during the “off times” would generate too much amplified spontaneous emission (ASE) noise).

In a fiber laser/amplifier however we might be able to pump during these “off times” in a “pre-burst pumping scheme,” as depicted in Figure 2, if we can limit the growth of the ASE within that time and if the media can store the pump energy on that time scale.

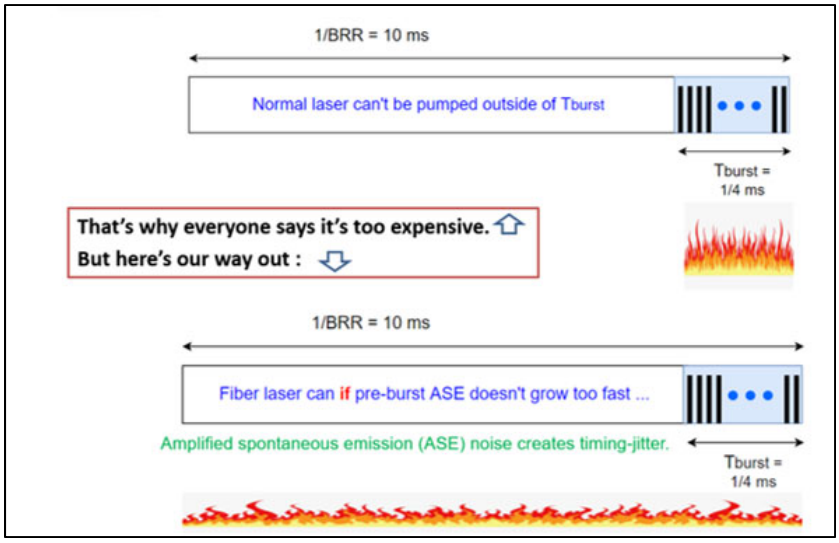


Figure 2. Strategy for pre-burst pumping cost reduction in fiber amplifier.

We utilize several models and simulation packages, including a saturable gain model (based on simplifications of a four-level atomic system [1], which incorporates a quantum field [2] containing the zero-point fluctuations which create the ASE). Fiber nonlinearities are included in other models (and simulations of the intensity dependent index of refraction inherent in glass fiber, or any Kerr media, which generates self-focusing). The simple saturable gain equations, shown in Figure 3, are nonlinear (although they do not include the "fiber nonlinearities") and contain one unconditionally stable critical point to which the gain, g, and output power, P, converge (when the gain saturates) as exemplified in Figure 3. We utilize gain saturation to suppress the ASE growth in various devices.

$$\frac{d}{dt}g = -\frac{g-g_0}{\tau_L} - \frac{gP}{E_{sat}}$$

$$\frac{d}{dt}P = -\frac{1}{\tau_p}P + \frac{2g}{T_R}(P + P_{vac})$$

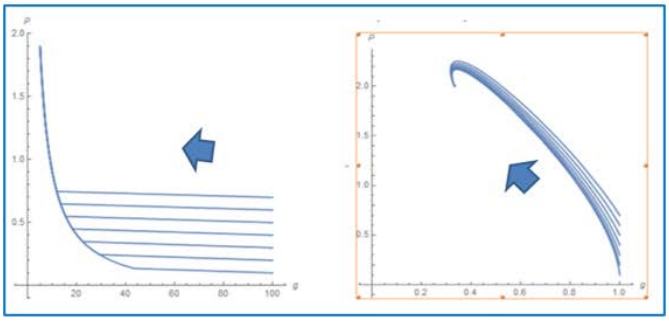


Figure 3. Nonlinear gain saturation model and examples of critical point convergence.

The fiber nonlinearities limit the power levels of optical fiber amplifiers via self-focusing, which expels energy from the glass waveguides. This nonlinear scattering limits the energy in circular and rectangular core [3] fiber; but a tubular geometry can collect such into a hollow-core mode in air. Figure 4 illustrates the underlying mechanisms. We form optical power amplifiers from simple glass tubes (doped in a rare Earth ion such as Erbium

or Ytterbium) which are filled with air (or other materials). The curved surface breaks the symmetry such that a spot input to the edge of the tube, as in Figure 4 a), preferentially scatters to the inside of the tube, as in Figure 4 b), where it is trapped as it feeds otherwise lost energy into a hollow-core propagating mode, as in Figure 4 c).

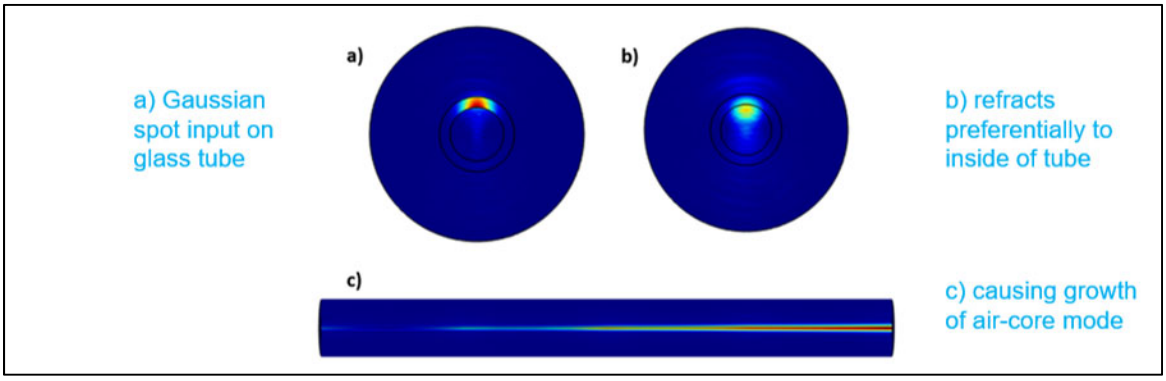


Figure 4. Operating principle of a high-power optical amplifier tube.

3.2.4 Tasks, Milestones, and Status

(A) Devise a pre-burst optical pumping scheme by which we can reduce the costs of the laser by a factor of two or more and calculate the resulting increase in ASE. / FEB–JUL 2020 / Completed.

(B) Reduce the ASE via gain saturation. / Oct 2020 / Completed.

(C) Design saturable gain devices which avoid nonlinear damage. / Completed.

(D) Calculate and ensure that timing jitter remains less than +/-15 ps with a probability greater than 0.9. / Completed.

(E) Demonstrate a cost-reduced fiber laser: the level of success to be quantified via the amount of ASE growth per duration of a pre-burst pumping interval. Growth of 100 uw over 6 ms (the limit in theory) would be considered outstanding. / August 2022. / Sunset due to damage of fiber from outside our group.

(F) Design a new type of higher power, tubular core fiber amplifier. / May–August 2022. / Completed.

(F1) Apply one high-power tubular amplifier to a system comprised of an array of several (say N) PCSS (for example: N=12 in a 3x4 array (or 4x4 array with corners omitted) N=16 in a 4x4 array, etc.), thereby eliminating jitter constraints and reducing laser system cost by more than a factor of 100 (independent of burst profile). / August 2022. / Completed.

(F2) Design a high power, multiple tube optical amplifier and determine if it permits advantages for power handling or beam profile. / August 2022 / Completed.

(G1) Design a beam shaping, optical power combiner using a cladding of 6 tubes. / June 2022 / Completed.

(G2) Design a beam shaping, optical power combiner using a cladding of 6 tubes surrounding one inner tube. / July 2022 / Completed.

(G3) Develop spectral combiners based on multiple-tube waveguides and compare to existing PCF (photonic crystal fiber) technologies. / August 2022 / Completed.

3.2.5 Methods and Approach

Methods involved primarily calculations and simulations (although some experiments were performed, a scaled demo was not achieved due to accidental damage to fiber). The calculations mainly consisted of utilizing Mathematica for symbolic analysis and to numerically solve the nonlinear differential equations which corresponded to a carefully chosen model of rate equations for atomic and photonic transitions. The calculations were used to assess the noise and gain saturation properties of the amplifiers. The model covered the fundamental physics of fiber amplifiers (including the quantum optics aspects, which properly describe the ASE) without getting bogged down in the computational complexities of fiber modes and propagation aspects. Simulations then were used to bring in the propagational complexities as well as the fiber nonlinearities which arise in a Kerr media, such as glass. The simulations utilized COMSOL Multiphysics, and these full-wave solvers were applied to fiber core and cladding of circular, rectangular and tubular geometries – to asses and to discover how to utilize the nonlinear scattering.

To achieve our pump power cost reduction, our approach was to see if we can “pump low and slow” by extending the pump times into the pre-burst times without incurring excessive growth of ASE. We set a 100 μW limit on the ASE, since this would increase the heat on the PCSS by 10% due to leakage current.

High gain designs (of over 10^6) would put us over that thermal-ASE limit by 3 orders of magnitude according to *linear* gain theory (even if just pumping during the burst). Thus, we use *nonlinear* gain saturation to quench the ASE by moving the critical point close to the operating point at each stage of amplification.

High power optical amplifier tubes boost the operating point via thermal effects (from increased surface area but also via carrying some energy in the hollow-core) and via nonlinear effects (scattering of energy that would otherwise be lost is collected into the hollow-core).

3.2.6 Results and Discussion

- Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with pre-burst ASE power levels below the heating level tolerance of 100 mW.

The details for a specific burst profile are presented in Figure 5. By pumping over the entire 10 ms between bursts (instead of only during the 1/4 ms burst) we drop the pump power, hence the pump power costs, by 40. Further details, e.g., tables of ASE growth vs pre-burst time, can be found in the JUN2020 MSR.

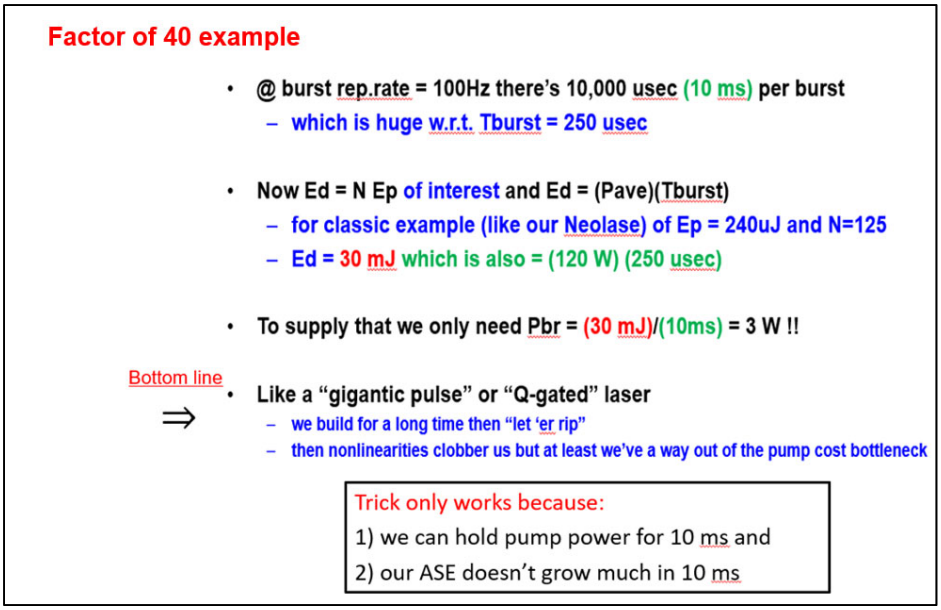


Figure 5. Numeric example of pre-bust pumping cost reduction scheme.

- For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our heating level spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000.

This was accomplished via a staged design in which the operating point, P_{out}, is kept close to the critical point, P_{cp}, so that each stage is nonlinear. Figure 6 exemplifies the approach in a 3-stage design in which even the preamp is kept in the nonlinear realm of operation due to small core diameter d. As the power level in each stage increases – so also must d (in order to stay above the thermal damage threshold). Further details can be found in the SEP2020 MSR.

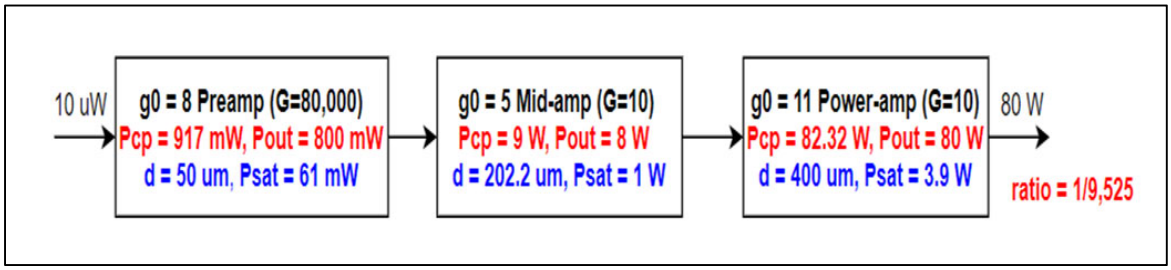


Figure 6. Example of a 3-stage amplifier which suppresses the ASE by 9525.

- We made (to our knowledge) the first observation of self-focusing effects that are not determined by beam power alone. We found instead that these can also be controlled via the geometric factors within a waveguide (such as fiber core diameter).

- We made (to our knowledge) the first observation that a mode exists in the air within a simple glass tube into which we can couple energy from the mode in the glass. Thus, an amplifier (in the doped and pumped glass) can operate at higher powers.

The symmetry breaking of the scattering from self-focusing in a curved waveguide was shown to enable such. This enables thermal advantages along with those resulting from a simple matter of scale as shown in Figure 7.

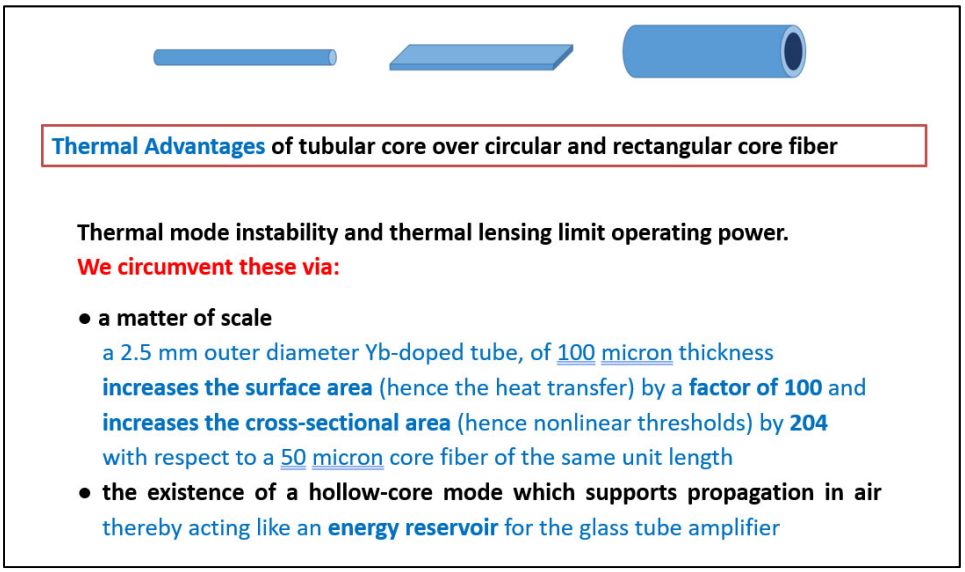


Figure 7. Thermal advantages for a tubular core fiber amplifier.

In Figure 8 “cladding” refers to the glass tube and “core” refers to its hollow (air) core. In the simulations we can artificially turn the Kerr nonlinearity off by setting $\gamma = 0$. Thus, in part a) we see that the power out of the glass/cladding (where it is launched) is reduced when $\gamma \neq 0$, as self-focusing refracts energy out of the glass. In Figure 8 b) however, we see that 96% of the dispelled energy gets trapped in the core/air. Further details can be found in the MAY, JUNE and JULY2021 MSRs.

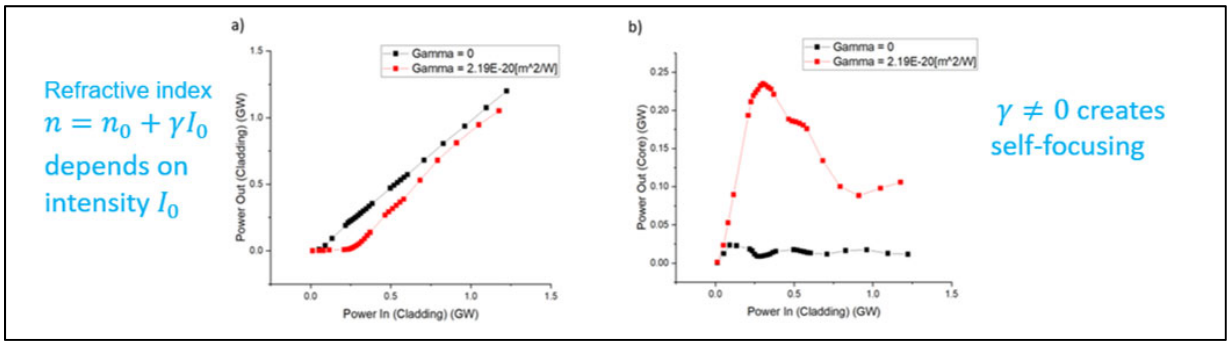


Figure 8. Nonlinear scattering advantages for a tubular core fiber amplifier.

- Advancements in the very high-power operating point (tens of GW) of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) were shown to permit a single laser to trigger an array of several (up to 100) Si-PCSS – reducing the laser system cost and eliminating the optical timing jitter constraint.

In Figure 9 we demonstrate what this would look like for a 37 element array (or a 12 element array, driven by 3 passive power delivery fibers each). Extensive simulation optimized output beam profiles. It is important to note that one device can cover both DoD applications of HPM and HEL (high power microwave and high energy laser) by simply changing the operating power point to adjust the output beam profile from almost uniform to almost Gaussian (respectively). Further details can be found in the AUG2021 MSR.

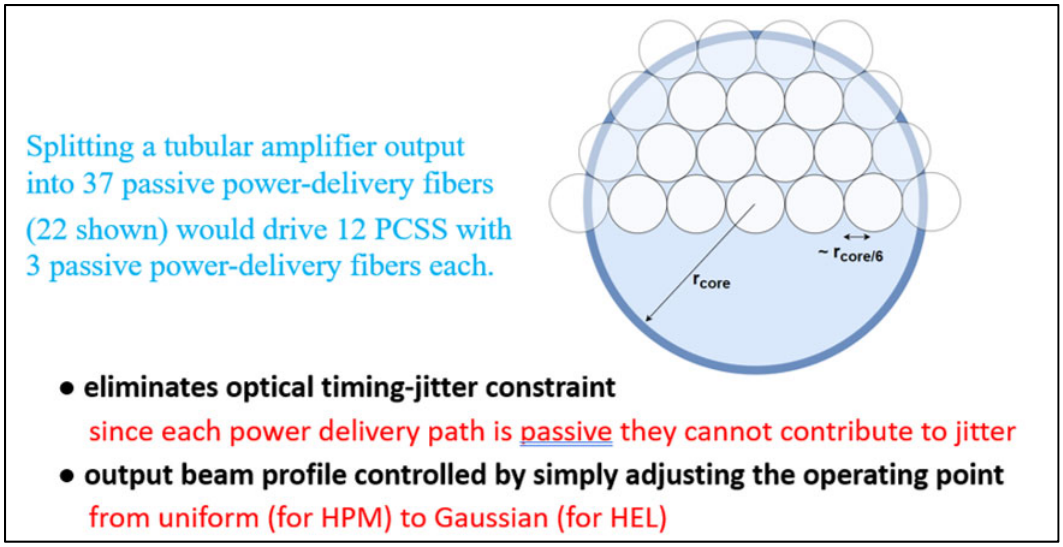


Figure 9. GW peak power levels and uniform beam profiles enable a single laser triggering of an array of PCSS elements.

- We calculated SWaPC improvement examples for the use of a single optical power tube to drive an array of PCSS (relative to a normal free-space implementation of the laser system) finding a cost reduction factor (for a 100 element array) of 83 at reduction in size by a factor of 290. For a 12 element array these improvement factors are 21 and 35. Further details can be found in the DEC2021 MSR.
- Complicated entrance optics for the tubular amplifiers greatly simplified by passively splitting a single source into a 4 “spots” to illuminate the wall of the tube. Found that with 4 spots of radial polarization we can still achieve GW core and 10 GW cladding power levels. Further details can be found in the JAN2022 MSR.
- Power combiners are important components in high-power fiber laser systems and to that application we leveraged our power tube technology; again using a 4 spot input (now with each spot coming from a different laser). We simulated four categories of input polarization and phasing combinations; and found that the

"radial" case (each spot in phase with radial directed polarization) maximizes power transfer into the core. The "phi polarized" case (in which the polarization of each spot is in the direction of increasing angle – tracing out a circle, i.e., to the right on top, down on right, left on bottom, and up on left); minimized power transfer into the core, while confining it primarily inside the cladding. Further details can be found in the MAR2022 MSR.

- Combiners comprised of 6 or 7 tubes lining the walls of an outer tube resulted in our best-yet Gaussian beam profiles (M2 < 1.13) by exploiting a new type of hollow-core resonance which ensues at operating power just beyond the breakpoint (and thus comes at a cost of a 3 dB reduction of cladding power). Further details can be found in the APR2022 MSR.
- By extending the length of the waveguides in our simulations we have revealed new physics, including the surprising creation of high intensity surface waves at the air/glass interfaces. These strikingly narrow spikes or pencil beams could be exploited in Directed Energy systems due to their highly localized nature. These are special waves which "hug" the material interface (rather than reflect from it) as do so-called "creeping waves" which have been observed previously, but such require conductivity. To our knowledge this is the first prediction that something similar can happen at a non-conducting dielectric interface. Such effects must be readily transferrable to RF radiators as well because they exist even in the case of the absence of a Kerr nonlinearity. Metallic tubes could generate creeping waves at RF but surface waves from glass would improve the SWaP. Further details can be found in the JUN2022 MSR.

3.2.7 Summary and Recommendations

A pre-burst pumping scheme can reduce the cost of a fiber laser amplifier by a factor of 40, and gain saturation can be used to design amplifier stages that suppress the overall ASE by over 5,000 (for an overall power gain of 8 million).

Laser/amplifier system cost can also be reduced (independent of burst duty cycle) by increasing the operating power. Fiber nonlinearities limit laser operating power such that fiber amplifiers with cores of standard circular cross-section have reached a fundamental limit. Rectangular/ribbon amplifiers have been considered, but we find that we can increase the power by over two orders of magnitude by utilizing a tubular core geometry – wherein the symmetry breaking causes preferential nonlinear scattering to the inside of the tube, where it is trapped and accumulates as an air-core mode. These permit peak powers of 10 GW, which enables the triggering of all (up to 100) of the Si-PCSS elements within an array via a single laser/amplifier source (thereby eliminating the optical timing jitter constraint).

Recommendations for spin-off technology

Power combiners are important components in high-power fiber laser systems and to that application we have shown how one can leverage our power tube technology via tubes within tubes (which are mode-coupled) and/or spectral combiners.

Therein water in a glass tube outperforms commercially available photonic crystal fiber (with a 90% transmission bandwidth of 300nm, in comparison to 80 nm, at a length of 2 meters).

Our understanding of how arrays of mode-coupled tubes can yield photonic resonances at optical frequencies maps into similar effects realizable at RF (600 MHz to 6 GHz). Thus, much of this work is being transitioned into PTERA objectives for the design of novel reconfigurable patch and horn antennas.

3.2.8 Outputs

S. R. Shepard and H. A. Thompson, “Self-focusing in Guided and Un-guided Media,” presented at the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, 2021.

Presentations at: DE-CDEW Program Review (2022); NRL virtual meeting (2022); LLNL virtual meeting (2021).

Invention Disclosures:

Shepard, “A Low Noise Optical Amplifier,” 21UMK007, 14SEPT2020.

Shepard, “A Novel Optical Fiber Amplifier,” 20UMK012, 02JUN2020.

3.2.9 References

[1] A. Yariv, “An Introduction to Optical Electronics,” second edition, Holt, Rinehart and Winston, N.Y, N.Y. (1976).

[2] E. Desurvire, “Erbium Doped Fiber Amplifiers, Principles and Applications” Wiley, ISBN: 978-0-471-26434-7 (2002).

3.3 Wide-band-gap PCSS-Enabled Laser Diode Array Driver

(John Bhamidipati; Originally published in the January 2022 MSR)

3.3.1 Executive Summary

A multi-stage wide bandgap (WBG) photoconductive semiconductor switch (PCSS) enabled laser diode array (LDA) driver was proposed in an effort to overcome the size, weight, and cost drawbacks of conventional laser systems used in high power microwave (HPM) systems. This involves an LDA enabled by an avalanche PCSS driven by a low power laser diode, which in turn drives the source driver for HPM generation, as shown in Figure 1. The primary goal of this effort is to retrofit a PCSS exhibiting persistent photoconductivity to function as a seed laser diode driven lock-on/avalanche switch [1] [2] to drive a high-power laser diode array (LDA) at ns–sub-μs transients.

An initial feasibility study was performed to determine the output pulse requirements of the enabling switch (PCSS) based on Jenoptik's actively cooled quasi continuous wave (QCW) vertical laser diode stack, which indicated the need for mΩ order on-state resistance, sub-ns risetimes and ~120 A output current. These pulse characteristics require lock-on conduction in the PCSS at <50 V bias, requiring a gain factor of ~$10^{2.6}$ when illuminated with ~1 μJ/pulse optical energy, raising a need for PCSSs made from direct bandgap materials like GaN and GaAs.

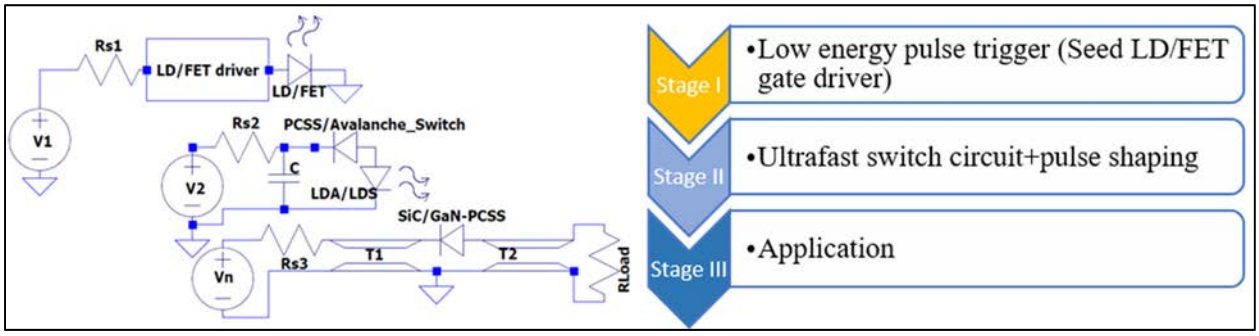


Figure 1. (a) Schematic of the proposed work and (b) flow diagram showing three implementation stages: (i) optical/electrical trigger, (ii) current gain and (iii) application.

Despite the published literature on GaN-PCSS lock-on conduction by Hirsch et al. [1] at Sandia National Lab (SNL), our in-house attempts to replicate the lock-on conduction using NRL fabricated lateral carbon doped GaN-PCSS were unsuccessful. The carbon doped PCSSs tested in-house may be structurally different compared with SNL-made GaN-PCSSs, leading to the discrepancy in results. To understand the material characteristics potentially contributing to lock-on conduction, carbon-doped GaN properties need to be studied computationally. [3] [4] Due to the unavailability of custom-made GaN-PCSSs, alternate PCSS technologies such as custom-made Si-PCSSs and

Si optodiodes by voltage multipliers inc. (VMI), and electrically triggered switches like GaNFETs and avalanche transistors (ATs) with the capability to demonstrate avalanche conduction, have been evaluated to experimentally demonstrate the pulse characteristics indicated by the feasibility study. Though the VMI optodiodes demonstrated ~400 ps rise times when illuminated with pulse energies between 20 µJ and 150 µJ/pulse, the on-state resistance was found to be on the order of 2.3–6.1 Ω, which is three orders of magnitude higher than the target metric. The Si-PCSS, along the same lines, failed to demonstrate the required on-state resistance when illuminated with pulse energies <100 µJ, rendering them inadequate for replacing GaN-PCSSs. The electrically triggered avalanche transistors rated for 60 A peak currents with 80 V hold-off are highly susceptible to device failure due to thermal runaway owing to their packaging and <150°C safe operating temperature. Furthermore, the requirement of 120 A by the LDA requires paralleling the ATs with capacitive coupling, increasing the chances of device failure.

To better understand the lock-on conduction in GaN-PCSS, a comprehensive study needs to be done to understand the effects of carbon/iron doping levels and distribution, crystal defect types, their energy levels, and concentration/densities on transient photocarrier generation, mobility, scattering, and recombination, requiring a dedicated personnel and computational resources with a slim chance of success. Due to the unavailability of GaN-PCSSs and lack of promising results in finding an alternative switch technology, keeping the program's immediate needs in mind, the LDA driver effort will not be pursued any further. However, a subset of this section constituting a solid-state switch enabled compact multifrequency generator referred to as a frozen wave generator will be pursued further and will be reported as a stand-alone section beginning FEB2022.

3.3.2 Objective

Demonstrate a modular multi-stage laser diode array (LDA) driver enabled by a seed-laser-diode-driven avalanche WBG-PCSS that is compact (~1.1 cu-ft), lightweight (~10–12 lbs.) and inexpensive (< $15,000) to be implemented as a potential alternative for the conventional optical trigger (laser) subsystem that enables PCSS-driven HPM-based defense systems and helps overcome the SOTA SWaP-C^2 limitations imposed by the laser's driver and auxiliary subsystems like amplifiers, optics and thermal management system (TMS).

3.3.3 Technical Background

High power microwave (HPM) generation primarily refers to the production of high peak power bursts of coherent narrow-to-ultrawideband electromagnetic waves spanning the frequency range of approximately 30 MHz to 100 GHz. [5][6] The technology used to generate such radiation is often based on pulsed power, [7] although more traditional modulator-based drivers are used as well, particularly at the higher frequencies where continuous wave (CW) operation can be supported for time scales of tens-of-minutes. The term high average-power microwaves implies a long pulse duration, high-repetition rate or continuous beam (referred to as "CW") sources, exemplified by vacuum tube based devices such as klystrons and magnetrons whereas high-peak power microwaves

implies a short pulse duration, a low-repetition rate, or ‘single shot’ sources, exemplified by devices such as the magnetically insulated line oscillator (MILO), capable of pulse widths under 200 ns. [6][7]

Despite successful implementation of vacuum-tube-based sources in HPM generation, the application trade-space was limited due to the complexity in the construction of source drivers, their ~μs jitter, narrow bandwidth, and high failure rates. [8] Advancements in science and technology have enabled unceasing expansion in pulsed-power application trade space with applications like ground penetration radar, wide band communications, high energy linear colliders, power beaming, counter electronics,[8] and other significant civilian and military applications with a need for ultra-wide bandwidth and miniaturization alongside waveform tunability and enhanced reliability. [9] These requirements have rendered the conventional source drivers antiquated, prompting the need to seek alternatives in unconventional sources, including solid-state device technologies like electrically stimulated silicon-based drift step recovery diodes (DSRDs), switching diodes and avalanche transistors, and optically stimulated photoconductive semiconductor switch (PCSS) technologies made of Si and GaAs. [9][1] PCSSs are capable of providing electrical isolation and exhibiting sub-ns turn-on characteristics following the pulse characteristics of the incident optical pulse trigger, enabling operation at high pulse repetition rates (PRRs).

Thus far, implementation of linear and lock-on mode PCSS in pulsed power systems has been successfully demonstrated at multiple kilovolts through relatively mature narrow bandgap (NBG) semiconductors like Si and GaAs. [9][10] Wide bandgap (WBG) semiconductors like 4H-SiC and 3C-GaN, despite being relatively immature in terms of fabrication techniques, have demonstrated linear photoconductivity at ones-of-kilovolts. [9][11]

However, acute optical pulse energy requirements for linear mode PCSS actuation[12][13] have brought forth a need for high average power femtosecond–picosecond lasers with an additional need for ancillary driver control and cooling systems. Despite meeting the system needs, these high average power laser systems return a degraded SWaP-C^2 (size, weight, power, cost and cooling) index due to their cost and volume constraints with a majority of it being contributed by its driver and control subsystem. This limits the application trade space to systems with abundance in financial capital, real-estate, and payload capacity. Industrial state-of-the-art (SOTA) master oscillator power amplifier (MOPA) based 1064 nm picosecond lasers for PCSS-driven HPM-based defense systems are bulky (>5000 cm^3/W), heavy (~125 lbs.) and expensive (~$120,000) with an additional need for second and third harmonic generation optics to trigger WBG solids (GaN/SiC). For reference, a laser in this class would occupy a volume of ~10 cu-ft (2.83 x 10^5 cm^3) and provide an average power of 50 W, thus resulting in 5.67 x 10^3 cm^3/W.

3.3.4 Tasks, Milestones, and Status

(A) Perform initial feasibility study for the cascaded multi-stage optical amplifier design and determine functional requirements for the laser diodes (arrays) and source driver [DEC–JAN 2020 / completed].

  a) Determine the functional requirements of the enabling switch based on Jenoptik 1080 W QCW laser diode stack [JAN 2020 / completed]

(B) Complete initial stage experimental implementation of the PCSS-based driver and demonstrate positive current gain using GaN-PCSS, triggered with a 404 nm laser diode. [DEC 2021–JAN 2022 / incomplete].

  a) Demonstrate lock-on conduction at <50V bias in GaN-PCSS with switch gaps 50 –100 μm. [DEC 2022 / incomplete]

  b) Evaluate switch response when excited with 355 nm, 375 nm, and 404 nm laser diodes to understand the device performance when excited intrinsically and extrinsically. [JAN 2022 / incomplete]

(C) In addition to (B), investigate potential alternatives to GaN-PCSS in both PCSS and non-PCSS domains. [NOV–DEC 2021 / completed].

  a) Evaluate Si-PCSS, and Si optodiodes from voltage multipliers inc., to verify the lock-on conduction at <200 volts with <50μJ/pulse optical illumination.

  b) Evaluate avalanche transistors rated for 80 V to verify the peak output current and reliability when used at >100 kHz PRR.

(D) Define performance metrics for PCSS-based driver and complete numerical calculations for required output current at each stage and corresponding PCSS (GaN/GaAs) operating voltages in light of electric fields required for lock-on/avalanche mode, establish real-time implementation timeline, cost estimates, jitter limitation, and explore ways to protect LDA from PCSS ringing. [MAR 2021 / partially complete / revisit after completing (B)].

(E) Proof of concept testing of the two-stage PCSS-enabled driver system with a 50 Ω load at 1 kHz pulse repetition rate (PRR) [NOV–DEC 2021 / incomplete].

(F) Working prototype demonstration at ~MHz PRR with laser diode array/stack and ancillary optics based on HPM source driver needs including thermal management system (TMS). [JAN–FEB 2022 / suspended].

3.3.5 Methods and Approach

Initial efforts started as a survey of the existing laser technologies and laser drivers to establish the SOTA limitations in the current market. Based on the market research, a need for a compact optical source was established. The first priority of this effort was to demonstrate a low cost, compact and lightweight driver for the lasers and/or laser diode arrays.

To accomplish this, a multi-stage approach has been proposed, where the first stage includes a low power laser diode driven by a compact driver, exciting a PCSS in the second stage in lock-on/avalanche mode, as shown in Figure 1. The need for avalanche

mode has been determined in the initial feasibility study. The avalanched PCSS enables an laser diode array (LDA), which in turn excites the source driver in the HPM generation system. The wavelength of LDA is determined based on the source driver material.

Two distinct approaches have been implemented for this work: (i) retrofit a PCSS exhibiting persistent photoconductivity [10] to function as a seed laser diode (SLD) driven lock-on/avalanche switch [9] to drive a high-power laser diode array (LDA) at sub-μs–ns transients, and (ii) investigate the possibility of driving the LDA using electrically triggered switches like GaNFETs and avalanche transistors (ATs) with minimal jitter instead of PCSS to obtain similar results experimentally. [11]

The testing of GaN-PCSS to demonstrate lock-on conduction was performed in-house to replicate the published work of SNL using a capacitive circuit as shown in Figure 2

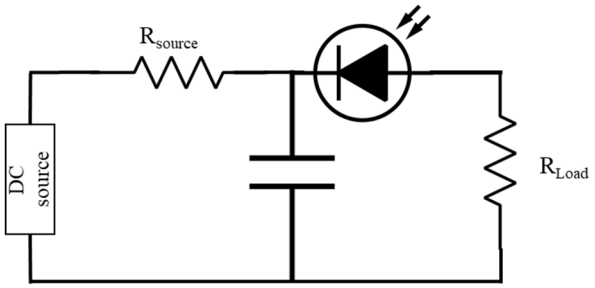


Figure 2. Operational circuit for GaN-PCSS testing.

On the other hand, the experimental evaluation of alternative PCSS technologies like custom-made Si-PCSS and VMI Si-optodiodes has been performed on 4.4 Ω stripline with 2.5 ns charge and 5 ns discharge lengths, triggered with 70 ps FWHM optical pulse with energies between 20 and 200 μJ. The expectation is to potentially demonstrate avalanche switching with optical energies <20 μJ at <50 V bias.

The evaluation of electrically triggering switch technologies like avalanche transistors has been performed to replicate Marx generator operation to demonstrate high current outputs with multiple kHz repetition rates.

3.3.6 Results and Discussion

The state-of-the-art COTS laser driver specifications and limitations have been comprehensively studied, and working backwards from the LDA requirements, the target performance metrics of the enabling switch have been determined in terms of output current (>120-A), pulse repetition rate (>1-MHz), transient response (<200-ps risetime and <1-ns pulse width), and volume (<0.75 cu-ft). A preliminary feasibility study has signified the need for lock-on conduction mode with ~$10^{2.6}$ gain factor to drive at >1-MHz pulse repetition rate while limiting the amplification stages to 2. Inducing lock-on operation at low electric fields (~3–3.5 kV/cm) potentially reduces the risk of high jitter at ~MHz order pulse repetition rates (PRR) and negative currents due to ringing during recovery,

which could otherwise damage the optical source (LDA). 72 mΩ on-state resistance (calculated) while operating PCSS in lock-on mode at low voltages (50-µm device at ~17.5 V bias) reduces the power dissipation (0.08 µJ/pulse), resulting in reduced cooling system requirements, retaining the expected SWaP-C^2 factor. This approach can potentially reduce the monetary costs to 10–12% of the conventional laser system, while achieving the expected goal of miniaturizing the optical subsystem by 90%.

To demonstrate the lock-on conduction mode in carbon-doped GaN-PCSS by replicating the published literature, [1] testing was performed in-house. Per the literature, the GaN-PCSS is expected to switch in lock-on mode at electric fields ~3–3.5kV/cm. However, our in-house experimental results have shown a strictly linear response of GaN-PCSS up to 18 kV/cm electric fields when triggered using 355 nm and 404 nm wavelengths. The attempts to demonstrate lock-on mode have been unsuccessful with the devices on-hand.

To find an alternative to the GaN-PCSS, we evaluated PCSS technologies like custom-made Si-PCSSs and commercial-of-the-shelf Si optodiodes (SKU: OZ150SG) rated for 15-kV procured from Voltage Multipliers Inc. The testing has been performed on a 4.4-Ω microstrip to verify the device ability to demonstrate <200-ps t_{rise} and <75-mΩ R_{on} while pushing >100-A current when excited with a 70-ps FWHM laser pulse. An optical energy sweep test was performed, keeping the charge voltage and laser spaciotemporal profile the same. The results from the test are reported below in Table 1.

Table 1. Results from Si optodiode pulse testing performed at 200-V charge voltage with a 70-ps FWHM optical pulse illumination and varied optical pulse energies.

Pulse energy (µJ)	Charge/bias voltage (V)	Output voltage (V)	Rise time (ps)	Fall time (ns)	On-state resistance (Ω)
200	200	96	428	4.845	0.143
103	200	66	368.56	4.652	2.266
47	200	55	360.65	4.3	3.6
21	200	42	329.46	3.9	6.076

The best result in terms of on-state resistance (0.143-Ω) was observed at 200-µJ illumination while t_{rise} (329.4-ps) was observed when illuminated with 21-µJ optical energy. Nonetheless, the obtained results failed to satisfy the metrics (R_{on} = 0.072-Ω and t_{rise} < 200-ps) determined by the feasibility study, rendering the Si-PCSS and VMI optodiodes infeasible for implementation as an alternative to GaN-PCSS.

Alongside the photo switches, electrically triggered switches like avalanche transistors have been evaluated against the established performance metrics to work in Marx-generator-style avalanche circuit. Though the transistors are rated for 60 A peak currents with 80 V hold-off, the ATs are highly susceptible to device failure due to thermal runaway

owing to their packaging and <150°C safe operating temperature and cannot be used even at a few kHz PRR. Furthermore, the requirement of 120 A by the LDA requires paralleling the ATs with capacitive coupling, increasing the chances of device failure.

3.3.7 Summary and Recommendations

PCSS and non-PCSS switch technologies capable of avalanche conduction have been evaluated against the pulse requirements for a LDA enabling switch. While GaN-PCSS with a direct bandgap has a potential to demonstrate lock-on/avalanche conduction, the limited device availability and fabrication customization has restricted the extent of evaluation. A comprehensive computational study to understand the compensation effects of sub-bandgap states on the photoresponsivity of carbon-doped GaN is recommended to understand mid-gap optical excitation that would potentially contribute to lock-on conduction. Though avalanche transistors failed to meet the design requirements, there are potential candidates in electrically triggered switch technologies like drift step recovery diodes (DSRDs) and silicon avalanche shapers capable of meeting the pulse requirements. However, these bring forth a trade of in terms of jitter (>50 ns) and implementing these devices requires additional effort to compensate it.

3.3.8 Outputs

IP disclosures

J. Bhamidipati, E. R. Myers, and A. N. Caruso “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources”, 21UMK009, 04NOV2020

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3.4 *Ab Initio* Informed TCAD and GaN:C

(Paul Rulis; Originally published in the October 2020 MSR)

What follows is a condensed summary of the sub-group motivation, activity, current results, and suggestions for future work as opposed to a chronological review of reports.

The material properties of gallium nitride (GaN) suggest that, in principle, GaN is well-suited for use in high voltage photo-conductive semiconductor switches (PCSS). The ongoing challenge is to turn the “in principle” performance of GaN into practical performance in device-scale systems. From the literature, progress has been made regarding the fabrication and development of high-quality bulk GaN substrates with the inclusion of dopants to obtain GaN buffer layers with high resistivity. For example, C and Fe are used as dopants to create deep acceptor states to compensate for residual donors in GaN buffer layers. [1,2]

Unfortunately, experimental device design and optimization is usually time-consuming and expensive. In response, the method of Technology Computer-Aided Design (TCAD) for simulating device properties had been widely demonstrated as a powerful tool for rapid design of electronic devices. TCAD simulations combine device geometries and the known electronic properties of the device materials under different conditions (e.g., dopant types, concentrations, and profiles) to produce reliable simulations of device performance. The main input ingredient for TCAD simulation of an arbitrary material is an array of material parameters that describe key electronic response properties. For many common electronic materials (e.g., Si) these parameters are well-known due to decades of experimental and theoretical work. Unfortunately, for relatively new materials such as doped GaN the collection of parameters under different conditions is much less well known. [3] Indeed, there are only a few experiment details about doped GaN that can fulfil the list needed for accurate TCAD device-scale electronics simulation. Therefore, it is necessary to turn to computational and *ab initio* methods to obtain material parameters for use in TCAD simulations.

Such an approach has been demonstrated already for intrinsic GaN among other materials. [4–7] Figure 1 illustrates one proposed organizational flowchart for accumulating the necessary input for a device-scale simulation driven in large part by accumulation of *ab initio* data. In this approach, not all of the data is obtained from a purely *ab initio* approach and empirical and classical molecular dynamics computational methods are used to help check and inform the *ab initio* results. Building a customized approach for doped GaN completely from scratch is well beyond the remit of the sub-effort and would require a much larger and more dedicated effort. However, fortunately, alternative approaches are available that leverage existing technologies (e.g., the Silvaco TCAD application) to enable the development of informed understanding of the device-scale electronic and transport properties of novel doped semiconductors with little if any input from sources beyond *ab initio* calculation.

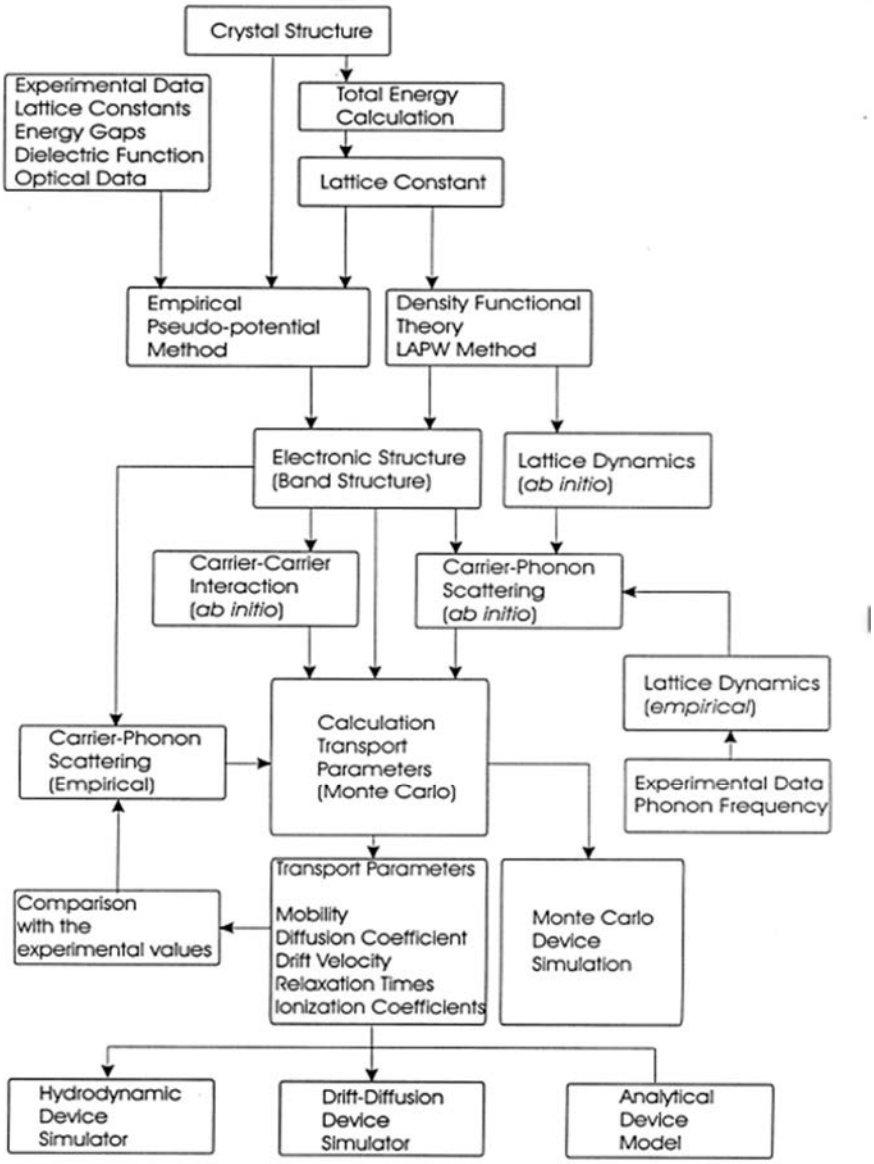


Figure 1. From reference [6]. One proposed method for accumulating the material parameters required for *ab initio* driven simulation of device-scale electronic transport.

As a proposed practical implementation of the flow diagram in Figure 1, intended for the specific input needs of Silvaco TCAD, we brought together the collection of *ab initio* tools shown in Figure 2.

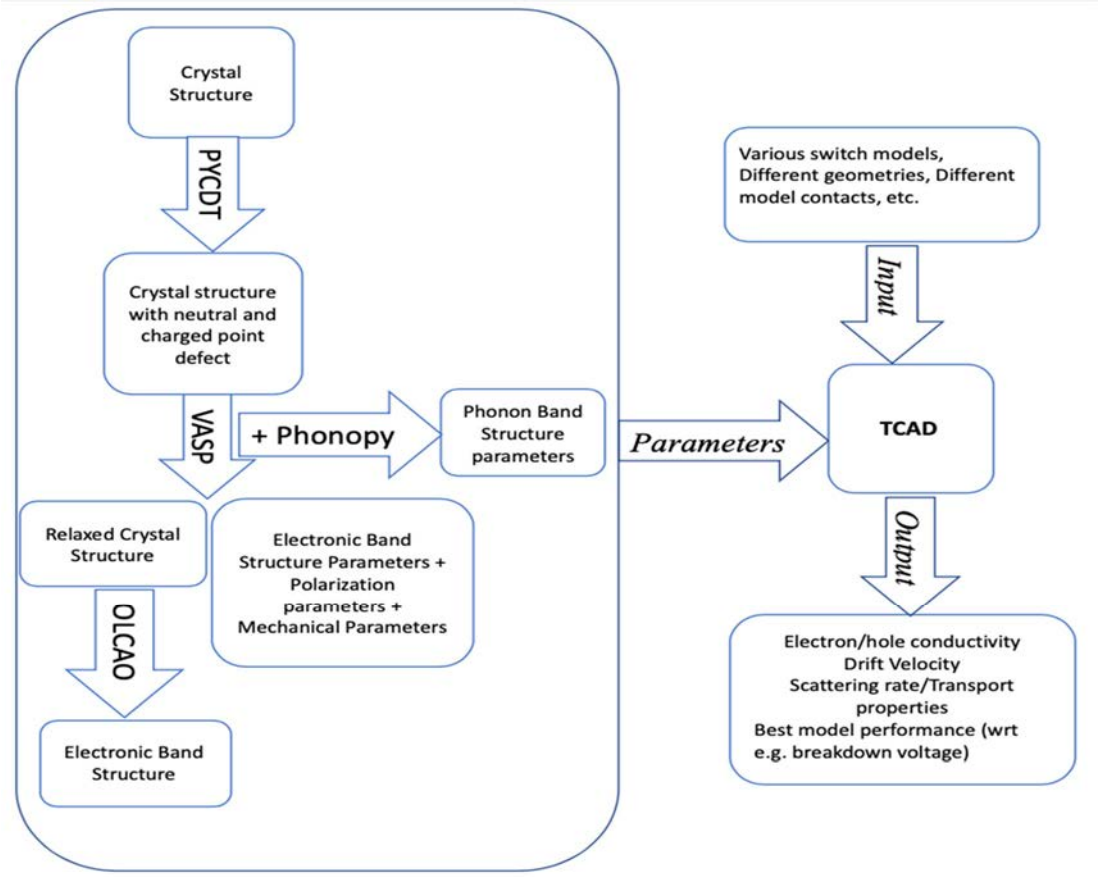


Figure 2. Flow diagram of programs for computing TCAD parameters.

The PyCDT program [8,9] (Python Charge Defect Toolkit) was used to produce models of crystalline GaN with either a C or Fe dopant atom. PyCDT was used instead of manual dopant insertion so that we would have an optimized cell size with limited dopant-dopant interaction, especially for scenarios with non-neutral (charged) dopant atoms. The charge neutral models that were generated are shown in Figure 3.

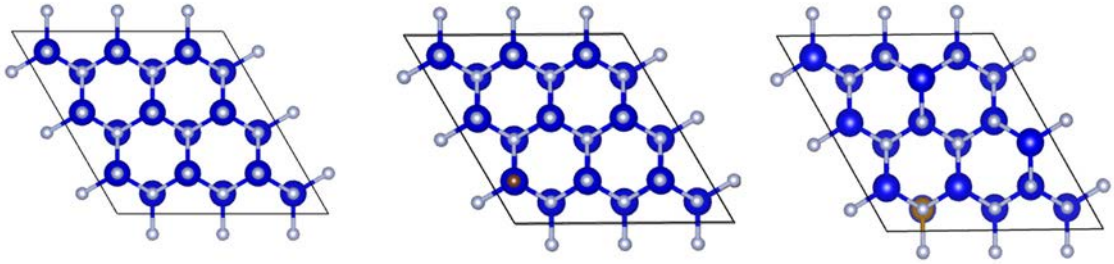


Figure 3. GaN models. Left crystalline GaN, center GaN:C, right GaN:Fe.

The resultant models were subsequently used for computation of the electronic band structure using VASP with a hybrid density functional that includes exact Hartree-Fock exchange [10–12], (a rather computationally intensive calculation for a supercell model). The use of a hybrid density functional is required to be able to obtain a correct band gap. The mixing parameter between the traditional exchange-correlation term and the exact Hartree-Fock exchange was determined for crystalline GaN through iterative trial and error to match the known experimentally determined value. From the relaxed crystal structure for GaN the band structure, band gap, electron/hole effective mass, mobility, polarization parameters, mechanical parameters, dielectric function, and dopant/defect states for GaN were obtained. Those results have been tabulated into Tables 1 and 2. The same mixing parameter could be used for future GaN:C and GaN:Fe calculations, where no experimental value is known. Doped materials require significantly more computational effort because they must be modeled with a supercell approach. Therefore, only some GaN:C and GaN:Fe calculations have been completed to date. Additionally, the shear deformation potentials are currently being calculated but they are also a fairly time consuming type of calculation.

Table 1. Calculated parameters for GaN in comparison to published values along with syntax label used in Silvaco TCAD.

Parameter	Symbol	Syntax	Units	**GaN (**published**)**	**GaN** (This work)	**GaN-C**	**GaN-Fe**
Electron eff. mass (*z*)	m_{cz}	MZZ	m_0	0.20 [13–15]	0.24		
Electron eff. mass (*t*)	m_{ct}	MTT	m_0	{0.18, 20} [13–15]	0.23		
Hole eff. mass param.	A1	A1		{-6.56 , -7.24} [13–15]	-6.92		
Hole eff. mass param.	A2	A2		{-0.91, -0.51} [13–15]	-0.674		
Hole eff. mass param.	A3	A3		{5.65 , 6.72} [13–15]	6.02		
Hole eff. mass param.	A4	A4		{-2.83, -3.36} [13–15]	-2.476		
Hole eff. mass param.	A5	A5		{-3.13 , -3.35} [13–15]	-3.21		
Hole eff. mass param.	A6	A6		{-4.86, -4.72} [13–15]	-4.67		
Valence band reference	Ev_0		eV	-2.64 [13–15]	-2.651		
Direct band gap (300K)	$E_g(300)$		eV	{3.44 , 3.42, 3.507,1.74, {3.51, 2.12}, 3.24 [13–15]	2.97		
Spin-orbit split energy	D1	DELTA1	eV	{0.021, 0.019, 0.016} [13–15]	0.020		

Crystal-field split energy	D2	DELTA2	eV	{0.01618, 0.01413, 0.01213} [13–15]	0.01015		
Lattice constant	a_0	ALATTICE	Å	3.190, 3.155, {3.215, 3.182}, 3.197 [13–15]	3.189	3.191	3.194
Elastic constant	C_{33}	C_{33}	GPa	{392, 398, 224}, 354 [13–15]	346.623	338.426	321.574
Elastic constant	C_{13}	C_{13}	GPa	{100, 106, 92}, 68, exp=70 [13–15]	73.369	75.681	62.212
Hydrostatic deformation potential	ac	AC	eV	-4.08 [13–15]			
Shear deform. potential Exp(range)= -9.6 to -3.1	D1	D1	eV	{-0.89, -3.0, 0.7}[1], {-4.9, -5.81, -5.33} [13–15]			
Shear deform. potential Exp(range)= -11.8 to -8.1	D2	D2	eV	4.27, 3.6, 2.1[1],{-11.3,-8.92,-8.84} [13–15]			
Shear deform. potential Exp(range)= 1.4 to 8.2	D3	D3	eV	5.18, 8.82, 1.4 [13–15],{8.2, 5.47, 5.8} [13–15]			
Shear deform. potential Exp(range)= -4.1 to -0.7	D4	D4	eV	-2.59, -4.41, 0.7 [13–15], {4.10, -2.98, -3.09} [13–15]			
Polar optical phonon energy	---------	--------	(meV)				
Acoustic optical phonon energy	---------	--------	V				
Dielectric function		dielectric		9.7, 8.9, 10.4,9.4, 9.5 [13–15]	10.5	10.01	14.185

Table 2. Polarization parameters for GaN (C/m^2).

Parameter	**GaN (**published**)**	**GaN**	**GaN-C**	**GaN-Fe**
Spontaneous polarization	-0.034, -0.029 [13–15]			
Piezoelectric constant (z) (e_{33})	0.73, 1.27, 0.67 [13–15]	0.88	0.47	- 0.517
Piezoelectric constant (x,z) (e_{31})	{-0.49,-0.35, -0.34 }, -0.37, -0.22 [13–15]	-0.27	-0.25	- 0.52

The parameters for pure GaN are already incorporated into Silvaco TCAD and so certain TCAD simulations can already be computed such as the breakdown voltage. Computed results are compared to experimental results in Figure 4. Once the ability to compute all

of the parameters for GaN has been demonstrated then the same methodologies will be applied to compute the parameters for GaN:C and GaN:Fe followed by the same type of TCAD simulations.

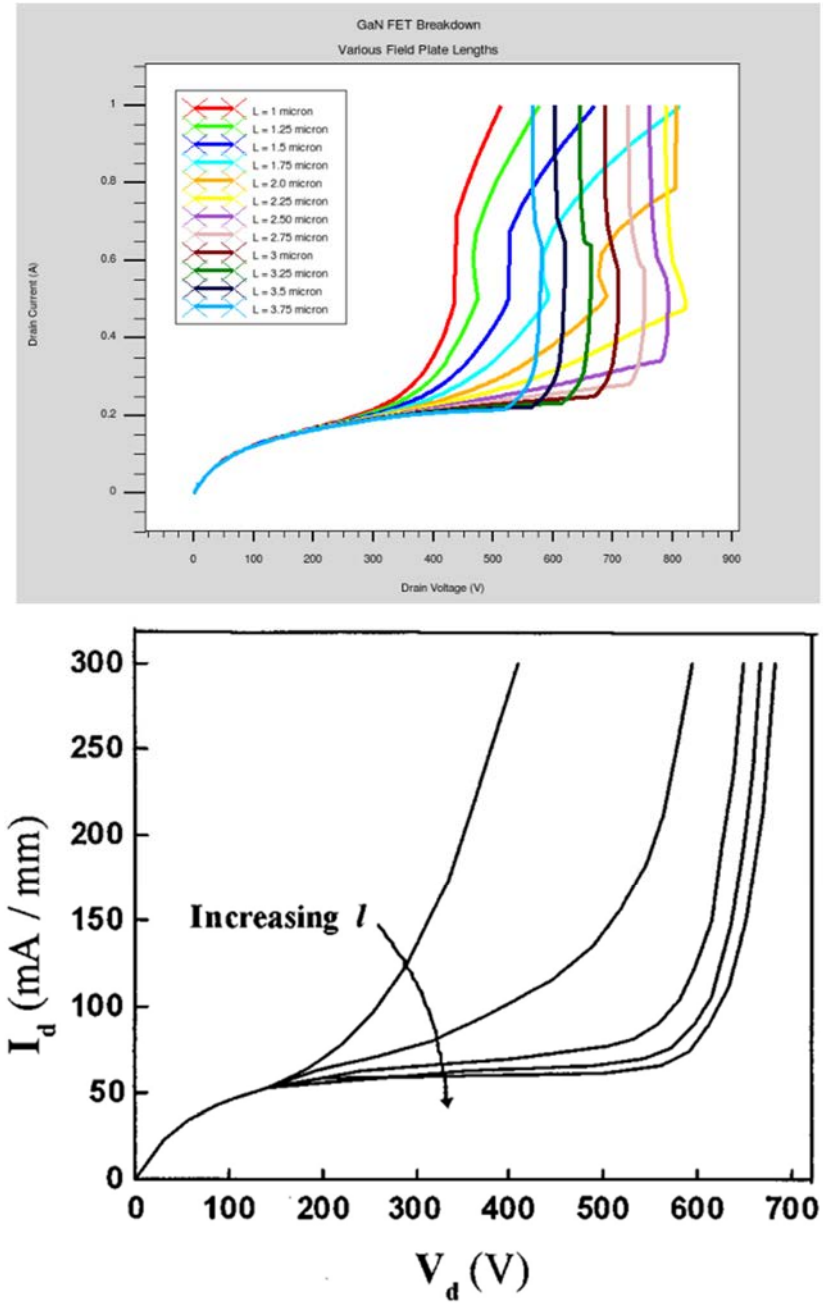


Figure 4. TCAD simulation of breakdown voltage for crystalline GaN compared to experimental data from reference [16].

Additional results were also obtained during the effort leading up to and supporting the progress toward understanding and then computing the parameters in the previously discussed tables. For the sake of brevity those results are not presented here and are instead left within the regular monthly status reports. However, in the most recent months an interest has been developed to understand the role that defects (point and extended) play in the device-scale properties of doped GaN. The complicated defect structure of GaN is shown in Figure 5 from reference [17].

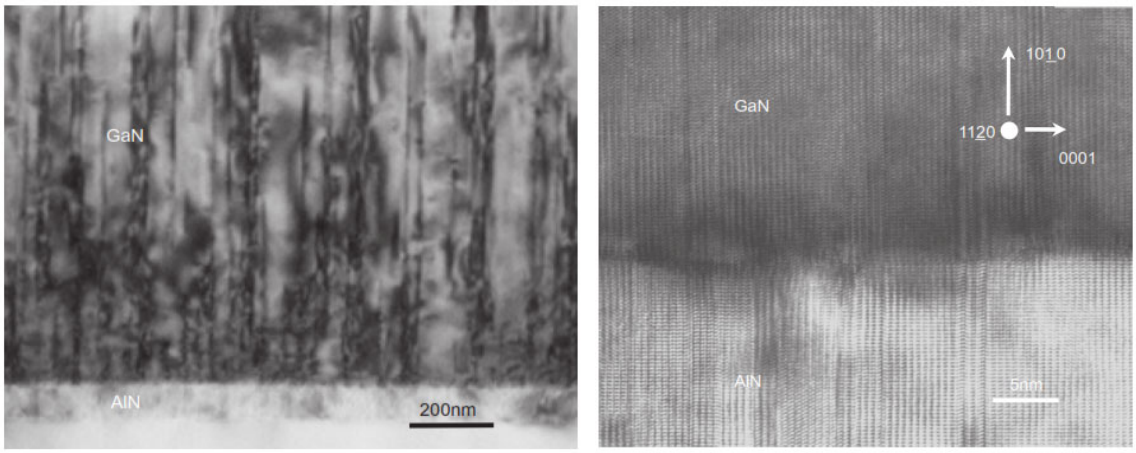


Figure 5. HRTEM images of GaN on an AlN substrate [17]. Extended dislocation defects and interfacial structures are clearly visible.

Regarding the point defects, work was performed to compute preliminary characterizations of the defect structures in GaN:C. The first point of interest was the x-ray absorption near edge structure (XANES) spectra of C-1s orbitals in GaN:C, shown in Figure 6. Although PyCDT was used to evaluate the most likely position for a C point defect, confirmation via experiment would be helpful. The XANES spectra is usually a unique fingerprint of the local atomic environment of the target atom. Therefore, the computed and a measured XANES spectra may be directly compared to definitively identify the most probable C atom position(s) in the crystal cell.

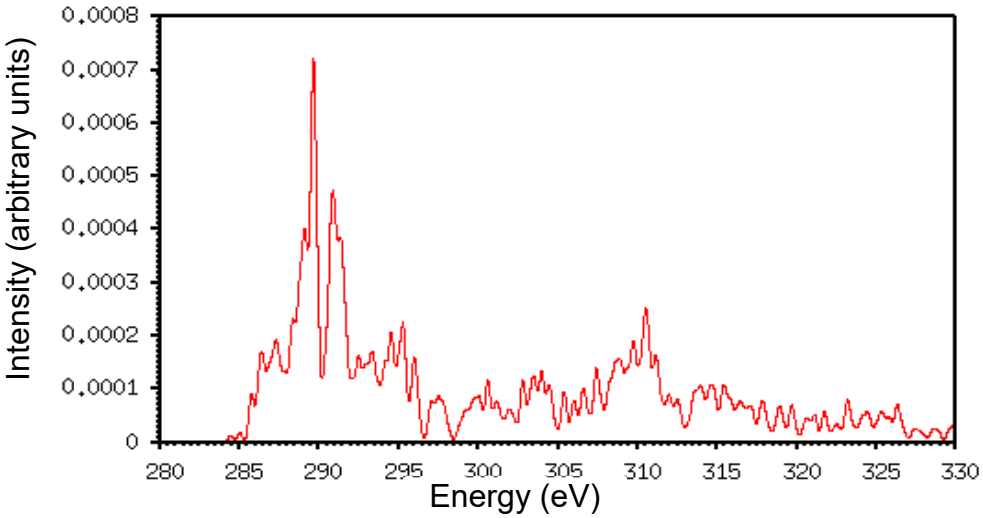


Figure 6. Computed XANES spectrum of C-1s dopant in GaN using the OLCAO method [18].

Beyond the point defects that depend on the dopant choice and concentration, it is expected that extended defects in GaN likely play a crucial role in governing the electronic properties of GaN. However, modeling the extended defects and understanding their collective impact on the bulk properties of GaN under extremely high fields presents a challenging multi-scale problem for which there is limited prior work and for which there are important potential gains in theoretical and practical knowledge.

In summary, the study of doped GaN via *ab initio* methods for the purpose of informing TCAD-level simulations has made significant progress. A methodology has been developed and executed on for crystalline GaN, mostly to the point of completion. The same method is likely to be applicable to GaN:C and GaN:Fe, enabling Silvaco TCAD simulations of device-scale systems with doped GaN. The precise nature of the point defects is accessible and could be confirmed via comparison between computed and experimentally obtained XANES spectra. As the collection of material parameters for point defect containing GaN is nearing completion, the stage is set for potential future exploration of extended defect structures in GaN. Such an effort would require substantial dedicated student time and faculty oversight which is presently outside of the scope of the current broader effort.

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3.5 Si-, SiC, and GaN Modeling and Evaluation

(John Bhamidipati; Originally published in the February 2021 MSR)

3.5.1 Executive Summary

High-power ultrafast switching fundamentals and switching technologies have been comprehensively studied in the context of optically and electrically stimulated switching technologies and pulse forming networks (PFNs), and factors inhibiting the transient response (rise-time, fall-time, etc.) and device lifetime have been identified for further study. Existing power electronics based figures of merit (FoM) proposed by Baliga, Johnson, Keyes, Kim, Shigekane, Wang, Huang, and Shenai over a period of 40 years have been comprehensively studied, and a need for new FoM based on photoconductive semiconductor switches (PCSSs) for pulsed power applications has been identified. A FoM has been derived for material-level evaluation of high-power linear-mode PCSSs in a capacitive circuit based on a power dissipation model for adiabatic and non-adiabatic heating cases, which has been submitted to the IEEE T-ED journal for publication (currently under revision).

Building upon the material-level evaluation of photoconductive solids, the effort has been extended to include device evaluation to compare the performance of Si-, SiC- and GaN-PCSSs. Si-PCSS carrier lifetime control techniques like Au-diffusion, Pt-diffusion, and electron-beam irradiation have been studied, and selective crystal damage with proton irradiation has been proposed as an alternative with two orders of magnitude lower leakage current due to selective localization and better lifetime control (faster recovery) due to larger trap cross-section. These results have been demonstrated through TCAD simulations, but not empirically verified. Non-isothermal simulations have been performed to study heat dissipation trends in Si-PCSS, but the results were inconclusive with 2D models. The heat dissipation trends need to be studied in 3D models to accurately quantify the heat dissipation and temperature rise rates in pulsed mode operation.

Lateral- and vertical- geometries of GaN- and 4H-SiC PCSS have been simulated and intrinsic carrier generation at optical wavelengths of 355-, 365-, 385- and 532-nm have been studied. A comprehensive study needs to be done to better understand the effects of device geometry, doping levels and distribution, crystal defect types, defect energy levels, and concentration/densities on transient photocarrier generation, mobility, scattering, and recombination, requiring enormous number of man-hours and computational time. However, keeping the program’s immediate needs in mind, this effort is being deprioritized and suspended for the time being.

3.5.2 Objective

To evaluate semi-conducting/insulating solids and device technologies through performance-based, application-specific figure(s) of merit (FoM) for high power photoconductive ultrafast switches and circuit topologies for linear/lock-on/avalanche modes of operation based on switching frequency, power dissipation, and cooling needs.

This effort also aims to explore possibilities of pushing the state-of-the-art limitations of each technology through novel fabrication techniques and recommend coherent SwaP-C^2 compliant solution through a near-ideal combination of PCSS driver and pulse forming networks (PFNs) for a pulsed-power system to achieve high power conversion efficiency with minimal spatial and capital footprint.

This involves evaluation of semiconducting/semi-insulating solids in the context of photo-stimulated switching technologies to determine an optimal source driver material to achieve tens-of-kV switching at near-zero jitter, sub-nanosecond rise-time, sub-unity Ω impedance, and nanosecond-order recovery, yielding GHz order bandwidth with enhanced reliability. This involves a comprehensive study of the effects of device geometry, doping levels and distribution, crystal defect types, defect energy levels, and concentration/densities on transient photocarrier generation, mobility, scattering, and recombination.

3.5.3 Technical Background

High-power microwave (HPM) generation primarily pertains to the generation of high peak power bursts of narrowband electromagnetic radiation based on pulsed power, spanning the frequency range of approximately 1 to 100 GHz.[1] The ideal driver waveform would be an impulse generator—in other words, a high voltage spike with picosecond-order rise-time, operated at high repetition rate.[1] For decades, conventional pulsed power systems have primarily implemented vacuum-tube based klystrons, magnetrons, ignitrons, and spark gaps as sources by converting electron beam kinetic energy into electromagnetic radiation for HPM generation.[2] Despite the successful implementation in HPM systems, source drivers were limited by size, complexity, ~μs jitter, tunability, and failure rates, fostering research for alternative solutions in solid-state electronics using photoconductive switches.[3]

Nevertheless, the efforts have been constricted to relatively narrow bandgap (NBG) semiconductors Si and GaAs with <150°C safe operational temperatures, implemented in a pulse forming network. Continuously evolving application trade-space in the realm of pulsed power applications, advancement in the material science research, and commercialization of semi-conducting/insulating materials have given scope to novel materials like GaN, SiC, BN, AlN, Ga_2O_3, and diamond, capable of photo- and electro-conductivity to implement high power opening and closing switches.[4] Their unique properties including, but not limited to, thermal conductivity, electron saturation velocity and electric field breakdown translate into higher operating voltages on the order of tens-of-kV, operating temperatures (>150ºC), and pulse repetition frequencies (PRF) of hundreds-of-kHz making them superior to Si in high power ultrafast switching.[4] A near-ideal ultra-wide-band (UWB) HPM source driver is expected to have ~mΩ-cm and ~MΩ-cm on- and off-state resistivity, respectively, with minimal stray capacitance and inductance (from switch-leads, geometry, and p-n junction), high PRF (~500 kHz) and picosecond-order rise- and fall-time. [6]

Each of these expectations is influenced by a combination of material, device, and circuit parameters, including, but not limited, to geometry, conductivity (electro/photo), field, carrier generation, mobility, scattering, and recombination, parasitics, surface termination, thermal radiation coefficient, conductivity, carrier lifetime, and surface area. Historically, the solid-state HPM sources have been demonstrated using Si, GaAs and SiC,[5] but SiC has not been extensively studied in comparison with other solids.

To effectively navigate this high-degree-of-freedom optimization, a figure of merit (FoM) can be used to screen and compare material capabilities quantitatively before attempting expensive empirical development campaigns. Johnson,[7] Keyes,[8] and Baliga[9] originally proposed figures of merit that enabled gross comparison of semiconductor materials for power electronics applications. Kim,[10] Wang,[11] Huang,[12] Shigekane,[13] and Shenai[14] have extended the effort to accommodate increased peak power density, average power density, operational frequency, heat removal, and the device-level implications of back-end processes, respectively.[14] While these FoM have been broadly successful, they are built for gate-based junction transistors and fall short in evaluating optically-stimulated photoconductive semiconductor switch (PCSS) technology where carrier generation and operational cutoff frequencies are limited by inherent material characteristics, device geometries, and incident spatiotemporal optical pulse intensity, raising a need for a PCSS-based FoM.

The results from this project contribute to implementing solid-state source drivers for HPM generation and many other pulsed-power applications. This is achieved by quantitatively screening and comparing the source-driver material and device technology capabilities in conjunction with pulse forming networks for a given application requirement before attempting expensive empirical implementation. Furthermore, this research explores novel fabrication techniques for parameter tailoring and post processing techniques that potentially contribute to push the theoretical performance limitations of the photoconductive devices. With the anticipated result of this effort, the multifaceted application-specific SWaP-C^2 compliant HPM source driver development can be completed with device design using the optimal semi-conducting/insulating solid and switching technology.

3.5.4 Tasks, Milestones, and Status

3.5.4.1 High Power Ultrafast Switch Fundamentals

i. Explore switching technologies capable of high-power ultrafast switching in optical- and electrical-actuation domains and study the micro and macro properties of semiconductors inhibiting switches' transient response and performance. *[DEC 2018 / completed]*

ii. Survey novel switching technologies (diodes, transistors and 2DEG-based switches) for down-selection in fast-rise pulsed power applications, study semiconductor(s) capable of implementation and refine performance metrics with quantitative reasoning *[FEB-MAR 2019 / completed]*

iii. Review existing power electronics figure(s) of merit (FoM)[7-14] to verify their suitability for evaluating optically triggered switches (PCSSs). *[APR 2019 / completed]*

3.5.4.2 Figure of Merit

iv. Recognize deficiencies in the existing FoM and derive a new FoM to address the deficit areas in light of the fundamental physics essential for high power linear-mode PCSS operation. *[JUN 2019 / completed]*

v. Explore tunable pulse forming networks (PFNs) with high efficiency suitable for high power ultrafast switching *[JUN 2019 / partially completed, expected to be done along with device-level evaluation]*

vi. Refine linear-mode PCSS FoM for on- and switching-states using power dissipation model (PDM) *[AUG 2019 / completed]*

vii. Quantitatively analyze the derived power loss equations for switching stages of the devices for Si, SiC, GaN, and diamond with varied geometry and illumination conditions as next step to defining figure of merit for PCSS without PFN *[OCT 2019 / completed]*

viii. Numerical analysis for turn-on and turn-off power loss equations to quantify the switching losses and combine with thermal conductivity for material FoM *[JAN-FEB 2020 / completed]*

ix. Refine numerical analysis for a generalized operational scenario across the photoconductive solids for on- and switching-states for adiabatic and non-adiabatic heating *[MAR 2020 / completed / Linear-PCSS FoM derived]*

x. Complete cost-effectiveness analysis to determine optimal material for PCSS implementation in a given application using material FoM in comparison with SWaP-C^2 requirements and complete drafting the manuscript 'Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches' *[APR-MAY 2020 / completed / manuscript submitted for journal publication]*

3.5.4.3 Device-Level Evaluation (Si-, SiC-, and GaN-PCSS)

xi. Evaluate Si-PCSS performance as a function of temperature by studying temperature dependence of band parameters and carrier dynamics (generation, transport, velocity saturation and recombination) through TCAD simulations. *[APR 2020 / completed]*

xii. Study photo-illuminated recovery of a 2-D, 1000×500-μm Si-PCSS device with a p-i-n doping profile (p^+,n^-,n^+) = (10^{19},10^{12},10^{19}) and a 500-μm optical window to map recovery time as a function of defect/trap type, density, level and cross sectional area. *[APR-MAY 2020 / completed]*

xiii. Study and compare the effects of defect-inducing fabrication processes/techniques such as gold (Au) diffusion and platinum (Pt) diffusion and compare with electron-beam irradiation on Si-PCSS recovery (carrier lifetime control). *[MAY-JUN 2020 / completed]*

xiv. Study the effects of proton-irradiation and γ-irradiation on carrier lifetime control and compare the study with electron-beam irradiation. *[JUL-AUG 2020 / completed]*

xv. Simulate different defect localization profiles, and complete numerical calculations for proton-irradiation dosage (fluence rates) and beam acceleration voltages (for penetration depth) using SRIM and TRIM models to experimentally verify the simulation results obtained in (xiv) *[SEP-OCT 2020]*

xvi. Experimentally validate the obtained simulation results for proton-irradiation induced defect profiles *[OCT 2020 / on hold – could not find a reasonable accelerator for proton-irradiation]*

xvii. Simulate and study 4H-SiC PCSS optical absorption profile and carrier generation at 265-, 355-, 385- and 532-nm incident wavelengths for optical energies between 250-μJ and 2.5-mJ at varied voltage bias (3–10kV) *[JAN 2021 / incomplete].*

xviii. Perform Si-PCSS non-isothermal simulations to quantify heat dissipation and temperature rise per pulse due to joule heating, generation-recombination, and Peltier-Thomson effect. *[SEP 2020 / results inconclusive]*

xix. Study optical and electrical performance of P-N doped and undoped semi-insulating vanadium compensated SiC-PCSS including optical absorption profile characterization, geometric (vertical and lateral) and doping profile optimization, and their effects on carrier dynamics. *[OCT-NOV 2020 / partially complete]*

xx. Simulate 3D Si-PCSS models at varied defect density and localization and optical energy to quantify their effects on power throughput, output pulse width, heat dissipation and temperature rise. *[DEC-2020 / incomplete]*

xxi. Complete parametric study of SiC-PCSS including rise- and recovery-time optimization simulations for varied vanadium and nitrogen concentrations, and high voltage transient response study for varied geometry, optical trigger, contact design, and illumination area *[Jan-Feb 2021 / incomplete]*

xxii. Model carbon- and iron-compensated GaN-PCSS with vertical and lateral geometries to simulate transient response, including rise- and fall-time, voltage hold-off, and peak- and average powers for performance evaluation against Si- and SiC-PCSS models. *[MAR 2021 / suspended]*

xxiii. Model carbon-compensated GaN-PCSS with vertical and lateral geometries, varied contact layers, carrier dynamics (generation, transport, and recombination) and circuit topologies to verify operational mode and current gain; then, calculate reduction in optical requirements in contrast with linear mode. *[MAR-APR 2021 / partially complete, on hold]*

xxiv. Evaluate the doping profiles, contact layering, and patterning for SiC-PCSS and explore suitable fabrication techniques to achieve desired optimal doping profile using TCAD-Athena. *[FEB-MAR 2021 / suspended]*

xxv. Evaluate the doping profiles, contact layering, and patterning for SiC-PCSS and explore suitable fabrication techniques to achieve desired optimal doping profile using TCAD-Athena. *[APR 2021 / suspended]*

xxvi. Complete parametric study of SiC-PCSS including rise and recovery time optimization simulations for varied vanadium and nitrogen concentrations, and high voltage transient response study for varied geometry, optical trigger, contact design, and illumination area. *[MAR-APR 2021 / suspended]*

3.5.5 Methods and Approach

Evaluation efforts started as a survey/exploration of optically (e.g. PCSSs) and non-optically stimulated (e.g. MOSFETs, IMPATT diodes, HEMTs, etc.) high power ultrafast switching technologies that may enable breakthroughs in solid-state source-enabled microwave generation. The first priority of this effort was exploring the factors (micro and macro) that inhibit the transient response and limit the performance of both PCSS and non-optically stimulated devices. Micro- and macro- switch properties that influence performance irrespective of the stimulation mechanism and some properties exclusive to PCSS have been identified and switching technologies suitable for the application (HPM generation) criteria have been down-selected. During this process, we came across multiple figure(s) of merit proposed by researchers [7-14] over time that have classified semi-conducting/insulating solids through the lens of electrically actuated switching technologies such as JFETs and MOSFETs, but not PCSSs. After a comprehensive review of figures of merit, a need for evaluation of the semi-conducting/insulating materials in the context of optical pulse stimulation was recognized.

This involved a two-stage evaluation: (i) standalone material-level evaluation by deriving a FoM for linear-mode PCSS operation, followed by (ii) device-level evaluation based on the results from (i) along with pulse forming networks.

Taking fundamental PCSS operational parameters into account, material-level evaluation across photoconductive solids has been implemented using a power dissipation model for on- and switching-states. From the material-level evaluation results, Si, 4H-SiC and 3C-GaN are considered as viable candidates for PCSS device-level evaluation based on their performance and manufacturing maturity.

Long carrier lifetimes have been identified as a limiting factor in Si-PCSS, resulting in increased heat dissipation and limited pulse repetition rates (PRR). Historically, fabricated Si devices are processed through Au-diffusion, Pt-diffusion, and electron-beam irradiation to generate sub-band traps for lifetime control, but with high leakage current across all of the techniques. Localized proton-irradiation defect profiles have been simulated and studied to demonstrate better carrier lifetime control at reduced leakage current. However, experimental verification has not been performed due to unavailability of a beam accelerator with required beam energy.

Initial studies on fundamental photoconductivity parameters like absorption, photoresponsivity, and doping profiles of SiC- and GaN-PCSSs have been studied for vertical and lateral geometries. However, in the interest of the program’s more pressing needs, this project is being deprioritized and suspended for the time being. As time permits, this subproject may be revisited in the future.

3.5.6 Results and Discussion

3.5.6.1 Material-Level Evaluation

Based on the macro and micro properties influencing semiconductor switch performance, the material-level evaluation for photoconductive solids has been performed by deriving a new linear PCSS figure of merit (FoM). The macro and micro properties taken into account are listed in Table 1 (A & B) below.

Table 1. (A) Macro and micro properties influencing semiconductor switch performance, **(B)** Macro and micro properties affecting PCSSs specifically.

General Semiconductor Properties	
Macro Properties	**Micro Properties**
Rise-time	Carrier generation
Hold-off voltage	Carrier recombination
Heating	Traps/crystal defects
Recovery	Scattering
Conductance	Dopants
Impedance	Carrier transport
Dark current	Drift and diffusion
Contacts	Injection inefficiency
Geometry	

PCSS Specific Properties	
Macro properties	**Micro Properties**
Incident energy	Absorption
Wavelength	Phonon assist vs. direct transition
Contact geometry	Sub bandgap states
AR coatings	

A FoM based on material power handling and capacity to resist temperature rise, based on fundamental parameter tuning has been derived through a power dissipation model (PDM). A PDM evaluates switching (turn-on and turn-off) and on-states to calculate power-dissipation rates across the photoconductive materials; the rates are then employed to calculate trends of temperature rise for adiabatic and non-adiabatic heating in the materials. It should be noted that PCSS conductance is contingent on photon absorption and breaks the tradeoff between V_{BD} and R_{ON} in electrically triggered devices. Figure 1 shows a spider chart that represents the numerical material parameters used in this analysis.

Figure 2 highlights the tradeoff between carrier lifetime and required optical power at 1Ω on-state resistance across photoconductive solids using Equation 1 below, for an assumed 100% photoabsorption efficiency and the material thickness optimal for a 10 kV device. The wavelength is chosen with respect to the solid's bandgap. For any given carrier lifetime, silicon is found to require the greatest optical power of all the considered solids, followed by GaAs. BN requires the least, as presented.

$$P = \frac{L^2 h\vartheta}{q\tau\mu_{\mathrm{T}} R_{\mathrm{on}}} \qquad \textit{(Eq. 1)}$$

Where P is required optical power, $h\vartheta$ is incident photon energy, L is device thickness $\left(L = \frac{10^4}{E_C}\right)$, E_C is the solid's critical field, μ_T is the mobility of holes and electrons, τ is the carrier lifetime, and R_{on} is on-state resistance.

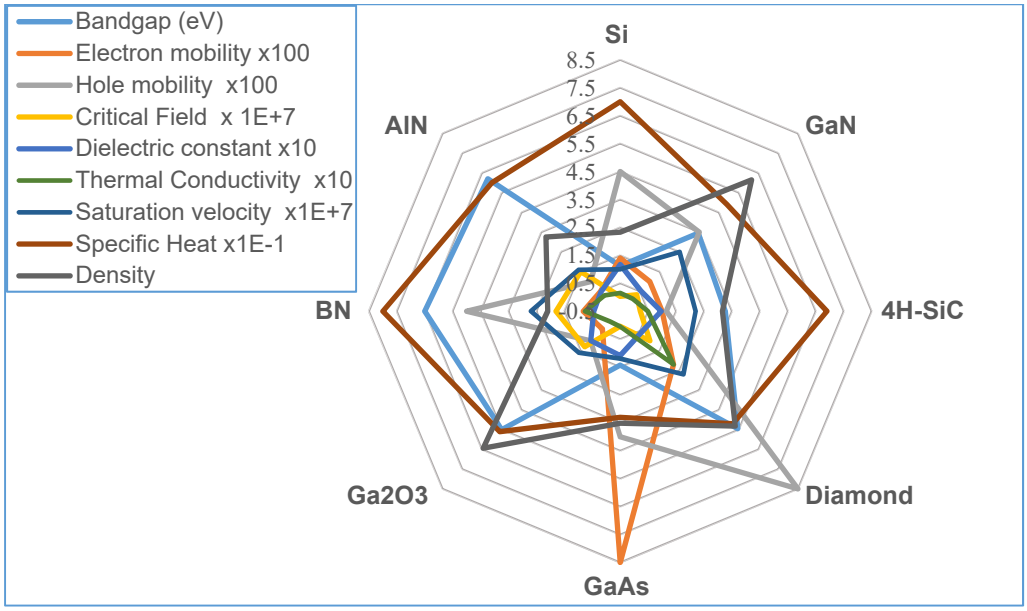


Figure 1. Spider chart showing electrical and thermal properties used to calculate power dissipation and high-power figure of merit.

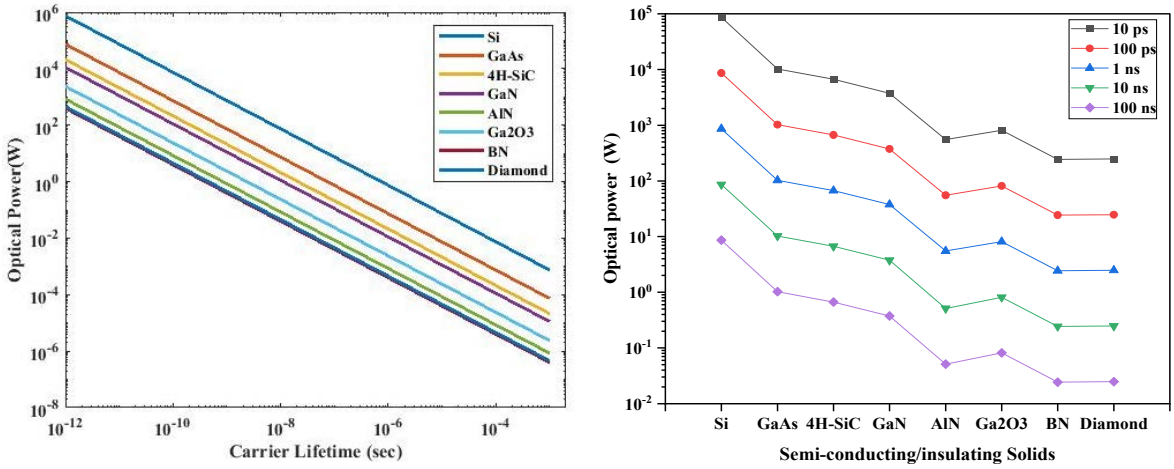


Figure 2. (Left) Tradeoff between carrier lifetime and required optical power across photoconductive materials and **(Right)** optical power requirement trends across photoconductive solids at different carrier lifetimes.

On-State Linear PCSS FoM

The on-state linear PCSS FoM facilitates the material evaluation of PCSS in systems driven at ~kHz PRR and tens-to-hundreds of μs pulse-width with negligible switching losses. Based on Equation 2 and the material parameters reported in Table 1, Figure 3 returns 4H-SiC as the highest rated WBG material (200 times superior to silicon), and diamond as the highest for an UWBG material (24,000 times superior to silicon) operated in linear mode.

$$\textit{On-state FOM} = \frac{E_C^2 E_g \eta \mu t_r k_{th}}{h\nu} \qquad \textit{(Eq 2)}$$

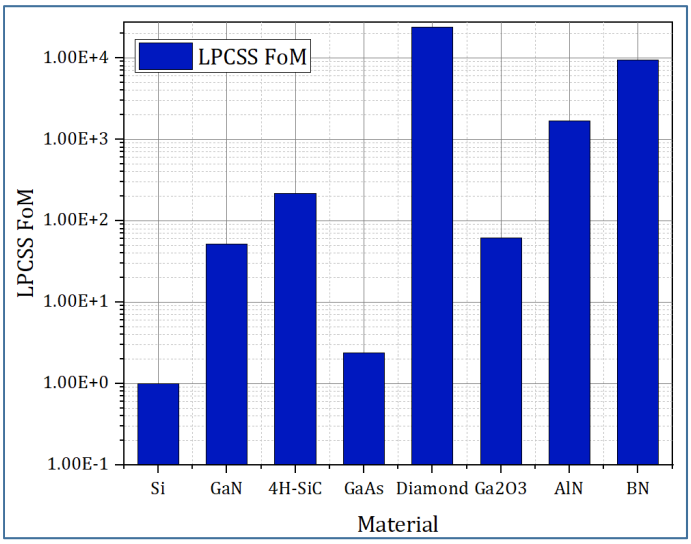


Figure 3. Comparison of the on-state L-PCSS FoM across photoconductive materials, normalized to silicon in the limit of kHz PRR, hundreds of μs pulse width and low loss assumed.

Switching FoM

Power dissipation equations during turn-on and turn-off (shown in Equations 3 and 4 below) have been derived using a PDM across photoconductive solids based on Nunnally's photoconductivity equations [15]

$$P_{turn\text{-}on} = \frac{\mu_T E_c^2 l^3}{R_L \mu_T I_0} \int_{t_0}^{t_1} \frac{\left(1 - e^{\frac{-t}{T_{net}}}\right)}{e^{-2.77*\frac{t}{\tau_p}\left[2 + R_L q\, \mu_T \frac{I_0}{E_\lambda L} T_{net}\right] - 2R_L\, q \mu_T \frac{I_0}{E_\lambda L} T_{net}\left[e^{-5.54\left(\frac{t}{\tau_p}\right)^2 - \frac{t}{\tau_p}}\right]}} dt \qquad \textit{(Eq 3.)}$$

$$\textit{and } P_{turn\text{-}off} = I_0 T_{net} q\, \mu_T E_c^2 L^3 \int_{t_2}^{t_3} \frac{e^{-2.77\left(\frac{t}{\tau_p}\right)^2 - \frac{-t}{T_{net}}}}{\left\{E_\lambda^3 + 2R_L q\, \mu_T I_0 T_{net}\; e^{\left[-2.77\left(\frac{t}{\tau_p}\right)^2 - \frac{-t}{T_{net(on)}}\right]}\right\}} dt \qquad \textit{(Eq 4.)}$$

where the limits t_0 and t_1 signify turn-on transition time limits, while t_2 and t_3 pertain to the turn-off transition. $I = I_0 e^{-4ln2\left(\frac{t}{\tau_p}\right)^2}$ is the temporal Gaussian light pulse with peak optical intensity I_0, $n(t)$ is the carrier generation function, E_c is the operational electric field, L is the thickness of the device (carrier path length/switch gap), d, w are the length and width of the solid, hv is the incident photon energy, R_{on} is on-state resistance, R_L is load resistance, q is the charge of the electron , μ_T is the mobility of holes and electrons, t_r is the inherent device-recombination time, t_T is the transit time of carriers given by $t_T = \frac{L}{\mu_T E_c}$, $T_{net} = \frac{t_r * t_T}{(t_r + t_T)}$, $T_{net}(on) = t_T$, and τ_p is the FWHM of the optical pulse.

Calculations were done assuming a monochromatic temporal-Gaussian pulse chosen with bandgap-dependent wavelength for each photoconductive solid to facilitate 100% quantum efficiency. FWHM τ_p = 2 ns and pulse intensity capable of generating 10^{17} photoelectron and photo-hole pairs per pulse have been considered with an assumed 100% absorption and 100% contact injection efficiency to alter device resistance from GΩ to mΩ order at 30kV/mm electric field, adequate to trigger saturation velocity in charge carriers across all materials with a 50 Ω load resistance. Figure 4 (left) shows the temperature rise-rate across the photoconductive solids for adiabatic and non-adiabatic operation and Figure 4 (right) shows the respective figure of merit numbers for the same.

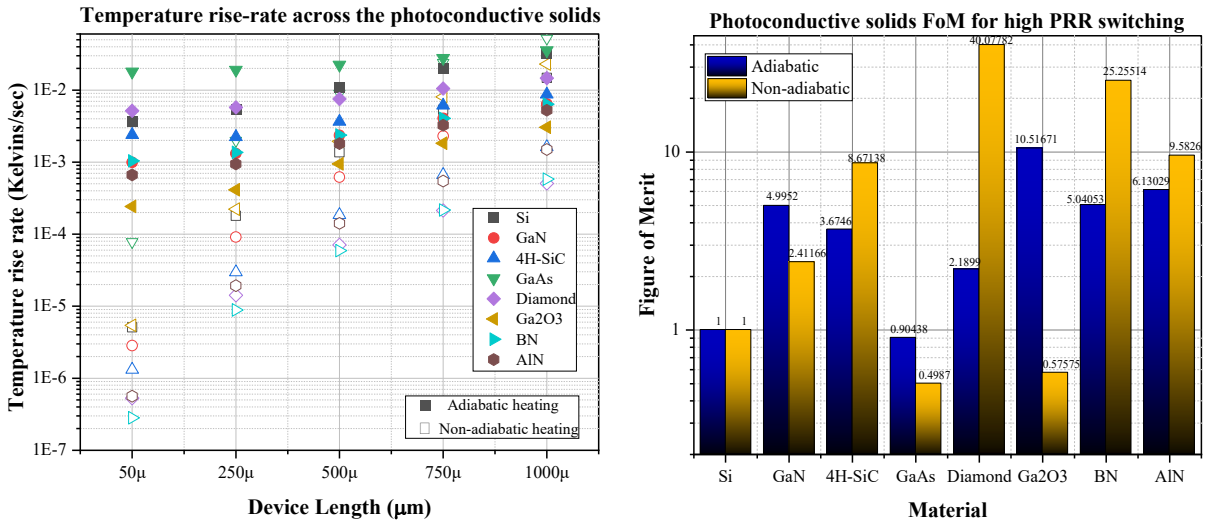


Figure 4. (Left) Temperature-rise rate (Kelvin/sec) across materials at 50 kHz PRF and 30kV/mm electric field at 50 µm, 250 µm, 500 µm, 750 µm, and 1000 µm carrier path lengths for adiabatic and non-adiabatic heating; and (**Right)** Switching-mode linear PCSS FoM normalized to Si for adiabatic (blue) and non-adiabatic (yellow) heating across NBG, WBG, and UWBG photoconductive materials switched at 50 kHz PRR.

UWBG-material Ga_2O_3 is found to perform five times better than diamond for adiabatic heating, owing to its specific heat constant; under non-adiabatic heating, however, diamond's thermal conductivity recompenses for incurred losses (~80 times Ga_2O_3), resulting in a ~10^{-6} temperature rise rate for high-PRR operation. However, based on the device fabrication maturity, Si-, SiC-, and GaN- device technologies have been selected for device-level evaluation.

3.5.6.2 PCSS Device-Level Study (Si-, SiC-, and GaN-PCSS Evaluation)

Si-PCSS

Au-diffusion, Pt-diffusion, e-beam irradiation,[17] and proton irradiation[18] effects on the carrier lifetime of silicon have been studied. While Au- and Pt-diffusion have drawbacks in the fabrication process, electron irradiation is a widely followed post-processing technique that creates uniform defects across the crystal. However, it results in increased leakage current (dark current) across the device due to distributed defects across the device, contributing to heat dissipation and affecting device lifetime. Simulations have shown faster recovery with localized defect profiles caused by proton-irradiation and at 3 orders of magnitude lower leakage currents as shown in Figure 5. Figure 6 shows a simulated proton irradiation defect profile and photo illuminated recovery comparison between electron irradiation and proton irradiation at different dominant trap levels. The defect penetration depth and distribution parameters have been calculated using SRIM (Stopping and Range of Ions in Matter) and TRIM (Transport of Ions in Matter) models.[19]
Note: dominant trap-levels depend upon the anneal and operational temperatures.

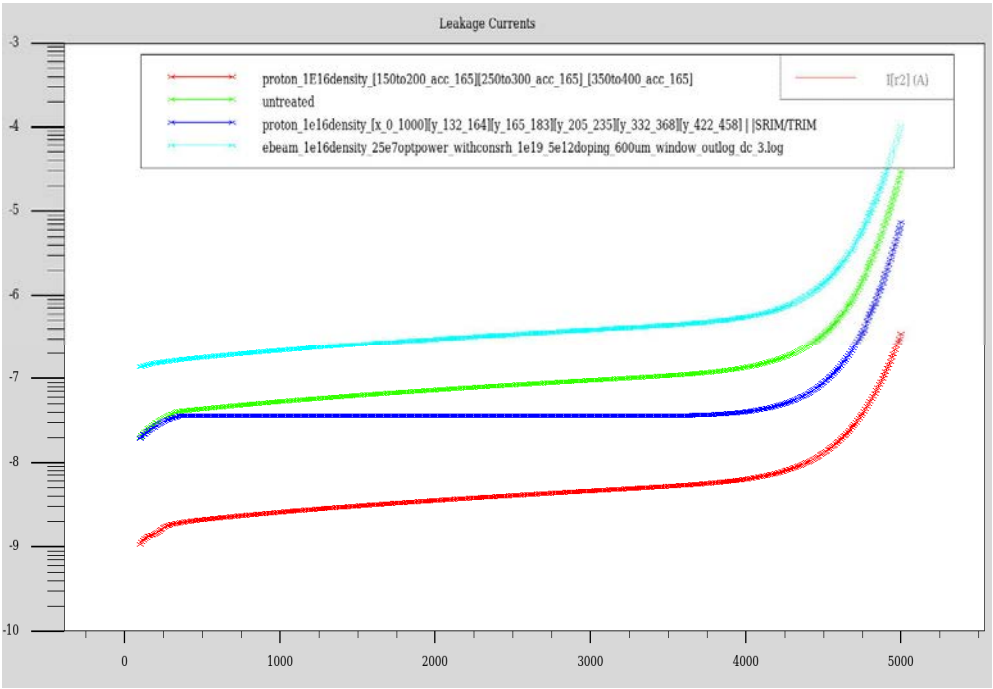


Figure 5. Leakage current trends across Si-PCSS with defect densities of 1E16 cm^{-3} when treated with proton irradiation: profile I (red), unirradiated (green), proton irradiation; profile II (navy) and electron irradiation (aqua).

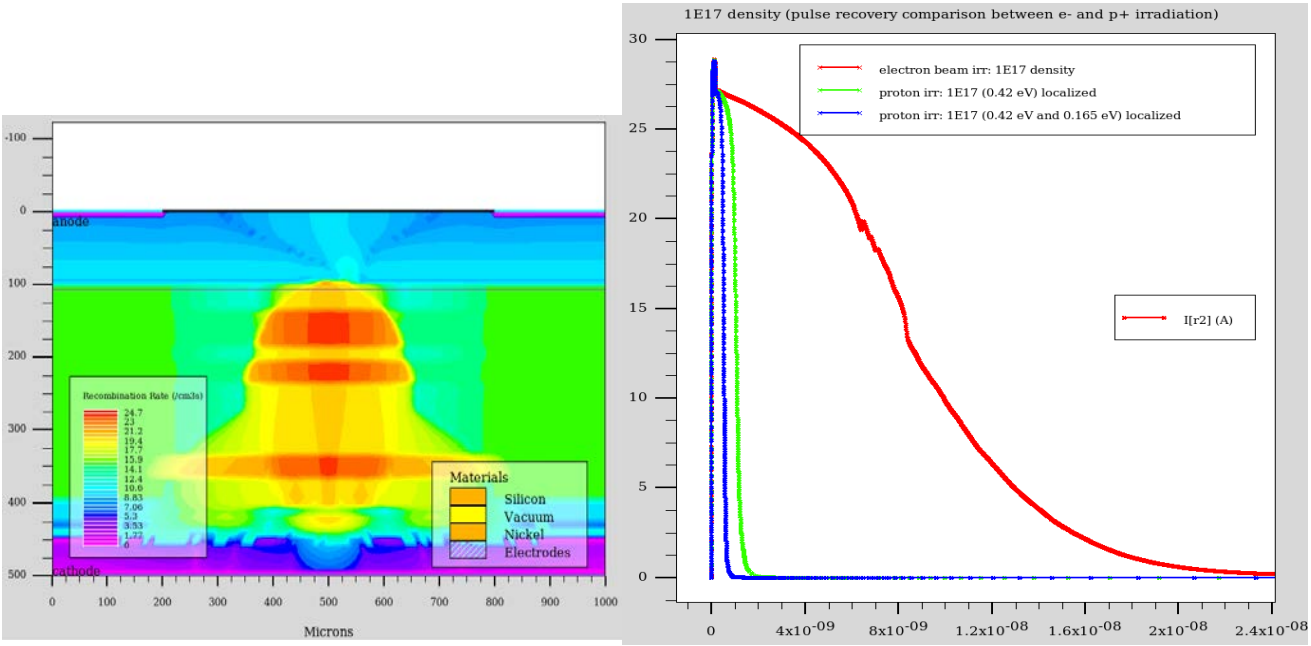


Figure 6. (Left) Simulation result showing localized defect densities (in red) induced in Si-PCSS through proton irradiation; **(Right)** Photo-illuminated recovery comparison between electron irradiation (red) with dominant trap-level E_t = Ec–0.41 eV and proton irradiation with different dominant trap-levels E_c–0.42 and Ec–0.165 and E_c–0.42 eV (two dominant levels) at 1E17 cm^{-3} defect density.

SiC- and GaN-PCSS

Detailed study of intrinsic and extrinsic SiC- and GaN-PCSS optical properties in lateral and vertical geometries, along with PFN-based analysis and non-isothermal power dissipation analysis of Si-PCSS simulations have not been completed. Unfortunately, a detailed study is time-consuming and computationally expensive. The time-consuming nature of this simulation study alongside more immediate needs of the program have led to deprioritizing and suspending this project for the time being.

3.5.7 Summary and Recommendations

High-power ultrafast switching fundamentals and technologies have been comprehensively studied in the context of HPM source drivers. A new figure of merit based on PCSSs has been derived and results have been submitted for a journal publication. This figure of merit can be extended in the future to include PFN- and device-based evaluation.

Via TCAD simulations, Si-PCSS recovery optimization has been studied and a potential solution has been proposed with better carrier lifetime control (1–2 ns vs. 16 ns recovery, from Figure 6) at two orders of magnitude lower leakage current compared with Au-

diffusion, Pt-diffusion, and electron beam irradiation. However, an experimental validation of proton-irradiation-induced carrier lifetime control is recommended as it would prove to be a huge asset in enhancing the average power throughput while reducing the cooling requirements of PCSSs. A heat dissipation study via 3D device modeling needs to be conducted to estimate the cooling requirements for different operational conditions.

A comprehensive study of SiC- and GaN-PCSS photoconductive parameters in conjunction with pulse forming networks has to be completed. A study of C- and Fe-compensation effects on GaN-PCSS photoresponsivity is recommended to understand mid-gap optical excitation and for bistable operation.

3.5.8 Outputs

3.5.8.1 Journal Articles

John Keerthi Paul Bhamidipati, Eliot R. Myers, Adam M. Conway, Lars F. Voss, and Anthony N. Caruso, “Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches,” *IEEE Transactions on Electronic Devices*, Under Revision, **2020**.

3.5.8.2 IP disclosures

Bhamidipati, “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources”, 21UMK009, 04NOV2020

3.5.9 References

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3.6 Direct RF Modulation Using GaN:C

(Heather Thompson; Originally published in the August 2022 MSR)

3.6.1 Executive Summary

Silicon (Si) is commonly used in RF pulse generation systems utilizing photoconductive semi-conductor switches (PCSS) due to its technological maturity, availability, and low cost; however, as applications require more extreme operating ranges, it becomes necessary to consider other materials. Gallium nitride (GaN) is a wide-bandgap semiconductor (~3.4 eV) with material characteristics allowing for higher operating voltage, frequency, and temperature. The fast recombination of GaN also allows for direct modulation of the output pulse by altering the photon source characteristics (i.e., pulse-width, rise-time, etc.), which also eliminates the need for pulse forming transmission lines that can be ones-of-feet long and allows for PCSS operation using a small PCB. Towards proving proof-of-concept, two different PCB were set up to allow for unipolar and bipolar modulation and optical delay system setup to provide various time delays between pulses. Unipolar modulation was successfully demonstrated at >2 kV, with higher voltages being unobtainable due to surface flashover between the PCSS contacts. Bipolar modulation was achieved at low voltages by adding a second PCSS, operating with negative bias, showing proof-of-concept for direct RF modulation using GaN:C PCSS. Further testing using a picosecond laser with quicker rise-time and 70 ps pulse-width was not achievable as the resulting usable laser energy, after conversion to 355 nm, did not allow for a low enough on-state resistance in GaN PCSS. Work was subsequently stopped as focus shifted to other OSPRES projects.

3.6.2 Objective

Primary Problem: Need for a more compact, cost-effective RF pulse generation system for Navy afloat missions on smaller vessels and vehicles.

Solution Space: Improve efficiency and reduce necessary material, size, and thermal requirements by utilizing gallium nitride (GaN) in photoconductive semiconductor switches (PCSS) through exploitation of its material properties, which can theoretically allow for higher operating voltages, frequencies, and temperatures, while also eliminating the need for pulse-shaping transmission lines through direct RF modulation using the laser/photon source driving the PCSS.

Sub-Problem: Lack of maturity in compensated gallium nitride semiconductor (i.e., GaN:X with X=C,Fe) PCSS manufacturing, development, and optimization.

State-of-the-art (SOTA):

Silicon-based technologies:

(1) Theoretical breakdown of 0.3 MW/cm limiting operating voltage leading to larger devices—contributing to increased overall system size—to reach >10 kV operating voltage.

(2) For minimizing on-state resistance and maximizing efficiency, ~100 μJ optical pulses per 4 MW of peak power, increasing the size of laser necessary for device triggering.

(3) Ones-of-μs recovery time, limits quick device turn on and high pulse-repetition rate operation and leads to increased device heating and increased cooling requirements.

(4) Operating temperature of <160 °C leading to increased cooling requirements.

Solution Proposed:

Replacing Si with GaN:C:

(1) Theoretical breakdown of 3 MV/cm allowing for higher operating voltage per device area allowing for smaller devices at similar operating parameters as Si.

(2) Fast recombination time allows for output pulse modulation determined by the incident laser characteristics (rise-time, pulse width, etc.), allowing for direct RF modulation eliminating the need for bulky pulse-forming transmission lines (~3 ft long).

(3) Incident optical energy of ~20 μJ needed for peak power operation at >3 MW, reducing the size of laser.

(4) Theoretical operating temperature of ~500°C (limited by circuit components and materials) reducing system cooling needs and allowing for operation in harsh environments.

Relevance to OSPRES Grant Objective: Reduction in size and cost for cooling system, removal of a pulse-shaping system, and decrease in material cost, leading to enhanced SWaP-C^2 capability with greater modularity and scalability.

Risks, Payoffs, and Challenges: Due to manufacturing limitations, GaN PCSS devices tend to be limited to lateral geometries (both contacts on the top side of the device), limiting operating voltage due to current crowding and surface flashover. The recovery time (ones-to-tens-of-ns) may lead to device heating and increased DC content when generating RF content with a period on the same order as the recovery time.

3.6.3 Technical Background

RF generation using PCSS devices is commonly done with silicon (Si) due to its technological maturity and low material cost, but its narrow bandgap and material characteristics cause deficiencies in performance that can be overcome by using a wide-bandgap material such as gallium nitride (GaN). The bandgap (~3.4 eV) of GaN, along with its higher electric field breakdown, faster saturation electron velocity, and drift-velocity (Figure 1), allow for operation at higher operating voltages, frequencies, and temperatures, leading to an overall system with a reduced form factor and increased SWAP-C^2 capabilities [1].

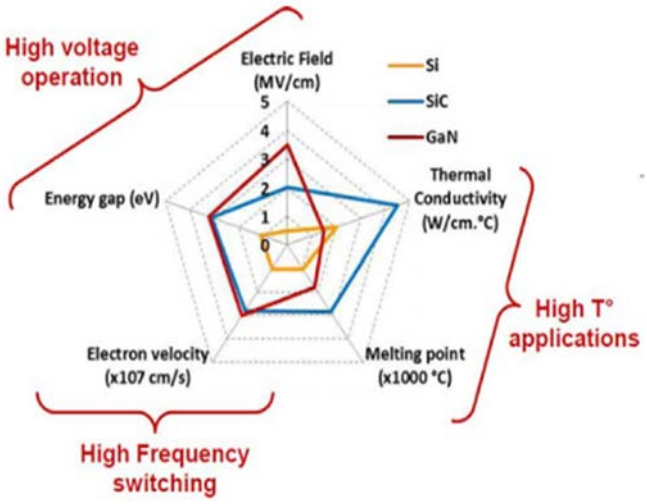


Figure 1. Comparison of Si, SiC, and GaN material properties [1].

The fast recombination in GaN allows for output pulse—thus frequency content—determination based on the characteristics of the incident light source (Figure 2). Utilizing the quick recombination time allows for GaN:C-based PCSS to be used as a frequency agile RF source by altering the incident laser rise-time, pulse-width, pulse repetition rate, and delay time towards eliminating the bulky pulse-forming transmission lines required in Si-based PCSS systems.

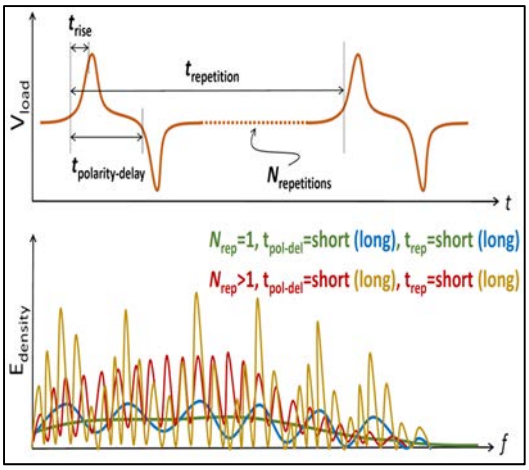


Figure 2. Diagram demonstrating possible ways of direct RF modulation of GaN:C.

Gallium arsenide (GaAs) is another commonly used narrow-bandgap material that is readily available, but unlike Si, has a direct bandgap and faster recombination time, allowing for laser characteristics to again dictate the output pulse achieved using PCSS. Direct RF modulation has been demonstrated using GaAs PCSSs by Stoudt et al [2], and

they were able to show that a frequency agile RF source was possible, as shown in Figure 3, at ones-of-GHz operation. This work served as the inspiration for using GaN as a frequency agile RF source through direct modulation.

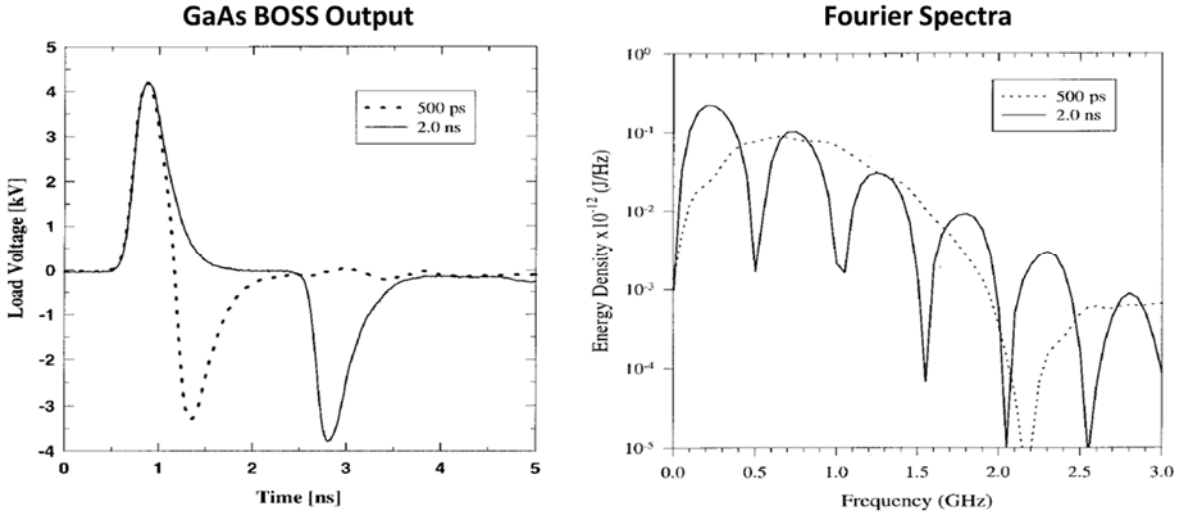


Figure 3. (Left) Plot of GaAs BOSS output utilizing bipolar modulation output for direct RF modulation. (Right) The Fourier spectra resulting from the GaAs PCSS output.

3.6.4 Tasks, Milestones, and Status

(A) **Dec 2020** Demonstrate GaN:C PCSS high-voltage operation (ones-of-kV to start) using pulse charger obtained from the HV switch development team. [Complete]

(B) **Jan 2021** Demonstrate RF unipolar modulation in the 1–2 GHz regime and up to 2 kV operating voltage with current PCB setup and the automated optical delay system. [Complete – up to >1 kV]

(C) **March 2021** Demonstrate RF bipolar modulation using two GaN:C devices, along with a positive and negative power source, based on the pulse-switch-out-generator-based circuit and setup with the automated optical delay system. [Complete – at low voltage only]

(D) **April 2021** Move test setup and show higher center frequency content and repetition frequency of unipolar and bipolar modulation using the neoLASE (70 ps) laser versus the wedge (~1.5 ns) laser. [Complete – neoLASE had insufficient laser energy after converting to 355 nm to allow for minimal on-state resistance in GaN PCSS]

(E) **May 2021** Complete study of recovery for differing gap lengths, incident energies, and operating voltages and find solutions to reduce the recovery time. [Incomplete as efforts were focused on other OSPRES projects.]

3.6.5 Methods and Approach

Due to the wide bandgap of GaN, incident UVA light is necessary for device activation, and therefore converting the existing IR source to UV using second- and triple-harmonic

generation (SHG/THG) is necessary (Figure 4). To manipulate the output, a free-space optical delay is set up to be adjustable, enabling the control of timing between pulses for manipulation of RF frequency output and allowing for frequency agility. Towards maintaining a small form-factor, a PCB is used to connect two PCSSs to a positive and negative power source and pulse charger, allowing for bipolar modulation (Figure 5). The outputs are then measured using an oscilloscope and plotted using Origin.

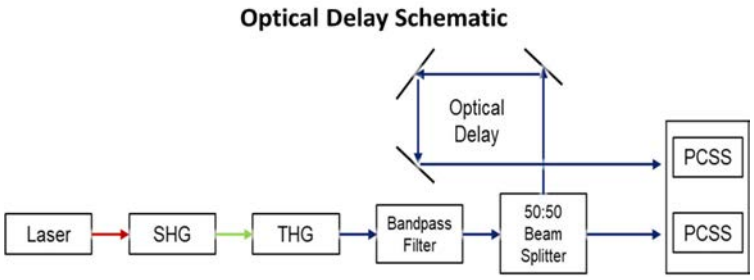


Figure 4. Optical delay schematic for bipolar RF modulation using GaN:C PCSS.

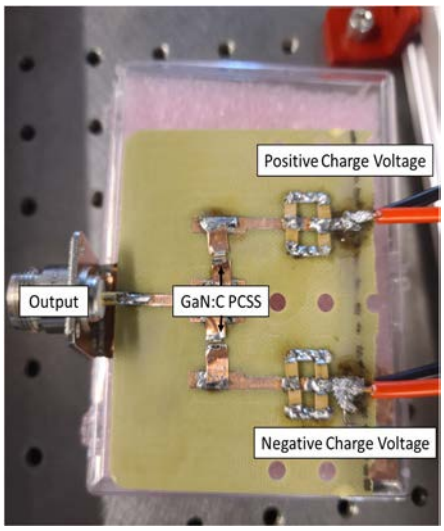


Figure 5. PCB layout for bipolar direct modulation using GaN:C PCSS.

3.6.6 Results and Discussion

Unipolar modulation using one GaN:C PCSS with free-space optical delay was demonstrated at <2 kV using a wedge laser (~1 ns rise-time). It is expected that adding a second GaN:C PCSS, operating using negative bias, and adjusting the timing between the two pulses, will result in a decrease of non-radiating DC content and allow for frequencies in the hundreds of MHz to ones of GHz to be achievable. The attained unipolar output is shown on the top left in Figure 6, with the expected bipolar output and bipolar FFT output shown in the same figure, with resulting frequencies in the hundreds-of-MHz range. Results at higher voltages were not achieved due to flashover occurring

across the contacts of the GaN PCSSs even when using encapsulating material, Sylgard 184, as air bubbles in the Sylgard, after vacuum curing, allowed for arcing between the contacts.

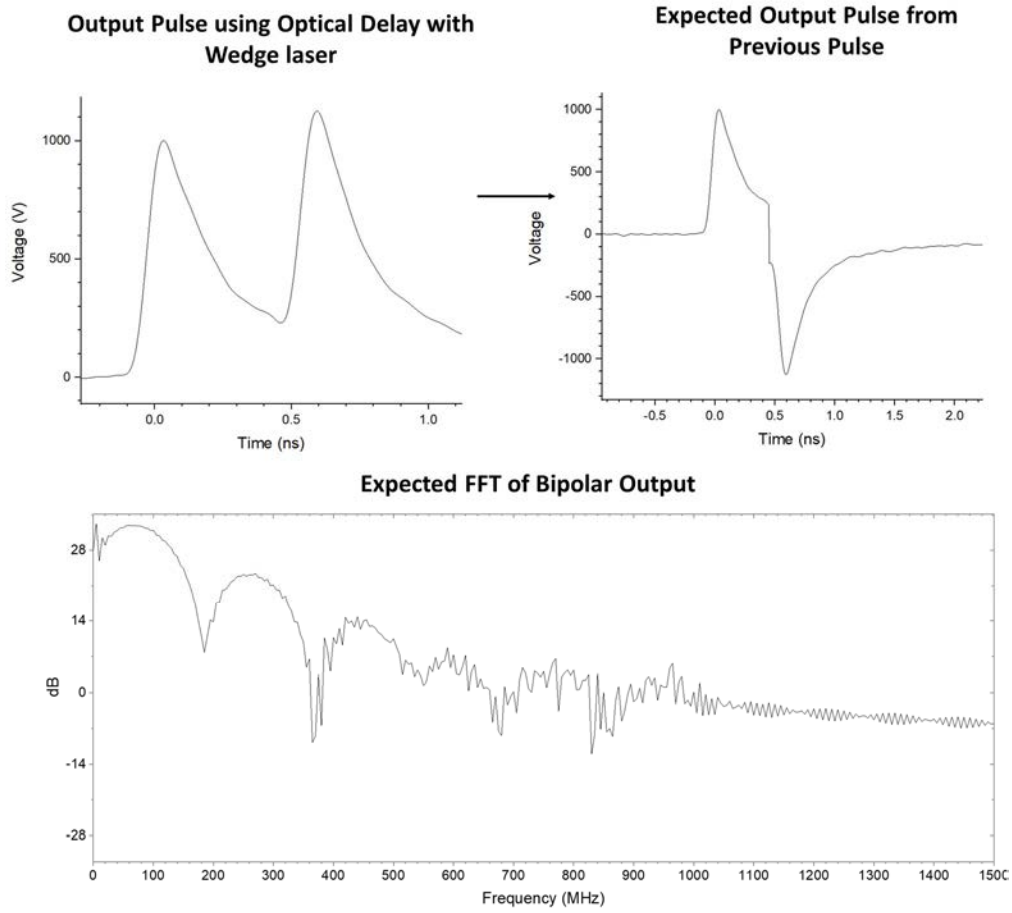


Figure 6. (Top Right) Unipolar modulation output using GaN:C PCSS. (Top Left) Expected bipolar output using GaN:C PCSS, determined from unipolar modulation results. (Bottom) Expected Fourier spectra of bipolar output using GaN:C PCSS for direct RF modulation.

Bipolar output was achieved at low voltage (~10 V) as a proof-of-concept for the PCB/direct modulation using two GaN devices. To achieve higher voltages and power, a different power supply is required. The resulting bipolar pulse is shown in Figure 7.

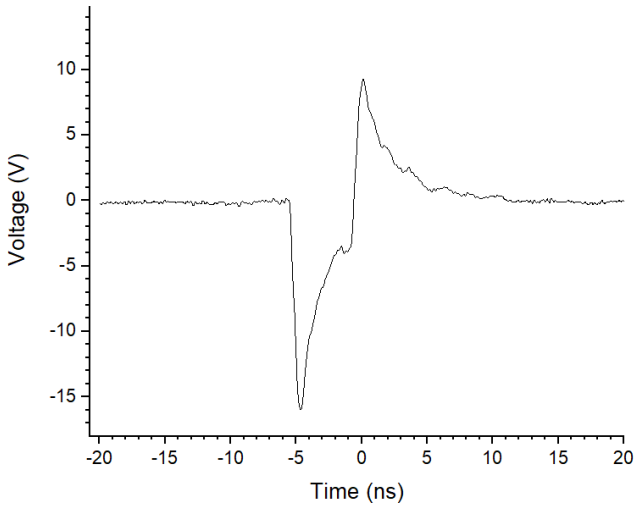


Figure 7. Bipolar output using GaN:C PCSS at low voltage for proof-of-concept towards direct bipolar RF generation.

To allow for higher frequency content, bipolar modulation using the neoLASE laser (70 ps vs ~1 ns pulse-width) was planned because of this photon source offering a quicker rise time. The optical delay and SHG/THG setups were moved to work with this laser and conversion to 355 nm was successful; however, only ~6 μJ of energy was left after conversion, which then needed to be split approximately in half for the free-space optical delay. Because of this small usable energy, there was not enough laser power to reach low enough on-state resistance to demonstrate outputs using quicker rise-time and pulse-width. To overcome this challenge, a different laser with similar rise-time and pulse-width but higher laser energy would need to be sourced. Further testing ceased as efforts were put towards other OSPRES projects.

3.6.7 Summary and Recommendations

GaN is a promising material for RF generation systems offering higher operating voltage, power, and temperature while maintaining or reducing the system form-factor over Si. The fast recombination time of GaN also allows for direct output modulation using the incident photon source activating the PCSS, negating the need for bulky pulse-forming transmission lines and allowing for device operation using a small PCB. Unipolar operation was demonstrated at >2 kV, with higher voltage results not being obtained due to flashover between the contacts. Bipolar modulation was shown at 10 V as a proof-of-concept, but higher voltage operation not demonstrated due to lack of needed power supply allowing for higher negative bias operation. Further results using the neoLASE, which offers a quicker rise-time and pulse-width, for higher output frequency output was not achieved as there was insufficient usable energy once this laser was converted to 355 nm using SHG/THG, thus low enough on-state resistance was not achieved in GaN PCSS using this laser. Further work was stopped due to efforts being placed towards

other OSPRES projects. Future success using GaN:C PCSS would benefit from a comprehensive study of minimizing on-state resistance to allow for devices with wider gap lengths and/or device type (lateral vs. vertical) towards eliminating arcing between contacts at >2 kV operation. Studies should include allowing operation using a higher incident wavelength (405 or 532 nm) and less incident energy (number of incident photons) to reduce incident photon source cost and size.

3.6.8 References

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[2] Stoudt, D. C., Richardson, M. A., & Peterkin, F. E. (1997). Bistable optically controlled semiconductor switches in a frequency-agile RF source. IEEE Transactions on Plasma Science, 25(2), 131–137. https://doi.org/10.1109/27.602483

3.7 Si-PCSS Top Contact Optimization

(Jay Eifler; Originally published in the August 2021 MSR)

3.7.1 Executive Summary

The silicon photoconductive semiconductor switch (Si-PCSS) requires a high energy laser to trigger the closing of the switch, with 1064-nm lasers being widely available and less expensive than other lasers. But high-average-power 1064-nm picosecond class lasers are too large and monetarily expensive for Navy afloat missions. To reduce laser size and cost, a redesign of the Si-PCSS top contact geometry has been completed using TCAD solutions to allow more efficient use of laser energy. The top contact geometry optimization is for a fixed 10-μm metal line width and for determining the best spacing between the metal lines (see Figure 1). A doping-dependent free carrier absorption photogeneration model is also employed to account for the laser illumination passing through the p-side anode contact first to reach the intrinsic region of the Si-PCSS and improves the simulation accuracy. Simulations have shown a 30% maximum possible percent laser energy reduction is possible when using the optimal 350-μm laser windowing spacing. Experiments with a small number of devices have shown a qualitative percent laser energy reduction when using optimal spacings. Further experimental data from a larger number of devices (due to device variability) is recommended to confirm simulation results of the possible percent laser energy reduction for the OSPRES mission.

3.7.2 Objective

High-average-power 1064-nm picosecond class lasers, necessary for activating silicon photoconductive semiconductor switches (Si-PCSS), are too large (1100 cm^3/W) and monetarily expensive ($1000/μJ*pulse) for the Navy afloat missions. For example, a laser of this class might occupy a volume of 1-m x 30-cm x 30-cm = 90,000-cm^3 and provide an average power of 50-W (thus, 1800-cm^3/W). A lab laser might cost $100,000 and deliver 100 μJ of laser energy to the Si-PCSS through fiber with 50% energy losses. By altering only Si-PCSS device parameters, one can enable both a laser size and cost reduction. Specifically, the laser energy required by the Si-PCSS can be reduced by altering the Si-PCSS top contact laser windowing spacing.

Si-PCSS top contact pattern designs are not known to have been published in detail. In-house patterns have used only an outer ring for the contact (resulting in high on-state resistance) and were improved by metallizing across the ring with filaments (to reduce current density high-points), similar to solar cell top contact designs. The Si-PCSS laser windowing spacings used were 10- and 20-μm, with 20-μm spacings achieving sufficiently low sub-ohm on-state resistance using in-house laser energy of ~100-μJ delivered to the Si-PCSS. However, there is no justification for 20-μm spacing being optimal for producing low sub-ohm on-state resistance with the least required laser energy. The solution is to optimize the OSPRES Si-PCSS top contact patterns using TCAD to meet reduced laser energy over a range of possible on-state resistances. Optimized top contact patterns

require less laser energy, which enhances SWaP-C^2 for the laser system needed to drive the Si-PCSS.

3.7.3 Technical Background

Solar cells and photoconductive semiconductor switches (PCSS) both rely on metal contacts at the anode and cathode of the device (a diode) for electrical connection to outer circuits and both require an aperture in the anode electrode (or transparent electrodes) to allow light to enter the semiconducting material (here we are concerned with silicon). This top contact electrode has a metal geometry design that can be optimized for some specific application/performance metrics(s) by altering the geometry, referred to as geometric optimization (as opposed to topology optimization) [1]. Topology optimization (a mathematical method) has been applied to many multiphysics problems and does not require predefined configurations and can obtain any shape within the design space, for example leaf shaped solar cell contact designs. Solar cell top contact designs are optimized for the larger size of the solar cell/module and often for absorbing sunlight and comprise the bulk of top contact design in the literature [2-10]. PCSS are equivalent to a small solar cell in size and mostly use laser light. Due to the smaller size of the PCSS, the regular metal grid design (see Figures 1 and 2) without fingers suffices. We have also explored and fabricated the fingered grid of Figure 2 but have not optimized the design and it has not been compared to the regular grid designs (except, see Figure 8 for fishbone data).

The Si-PCSS studied in this report are 1-cm x 1-cm devices that are 1300-μm thick. The actual simulation model is 0.8-cm in width and is a 2D model (3D model with 1-μm thickness) that has a multiplicative length of 0.8-cm and is 1300-μm thick. Initial TCAD simulations used a 500-μm thick device for faster compute times. The results are meant to be applied to 7-cm x 0.5-cm devices which are too large to simulate in TCAD, but 1-cm x 1-cm devices have also been fabricated (see Figure 9) and are very close to the TCAD simulation model (0.8-cm x multiplicative 0.8-cm).

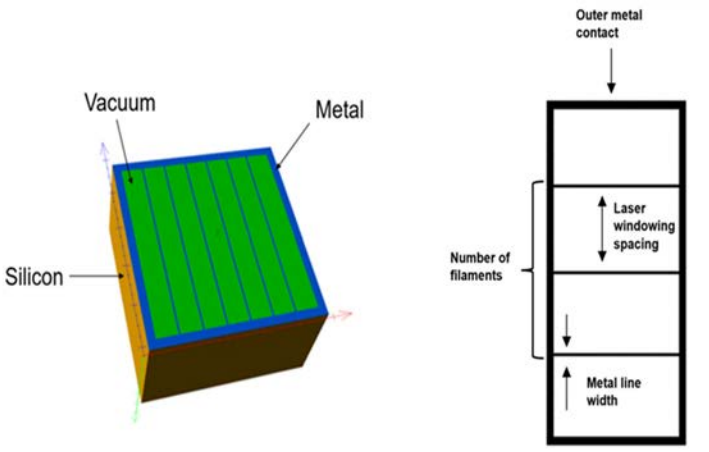


Figure 1. (Left) 3D mock-up of Si-PCSS with top contact pattern (blue). (Right) Top contact as 2D pattern from above/below showing laser windowing spacing between metal filament(s) of some metal line width (metal line width is 10 μm due to cost of manufacturing finer metal line widths.

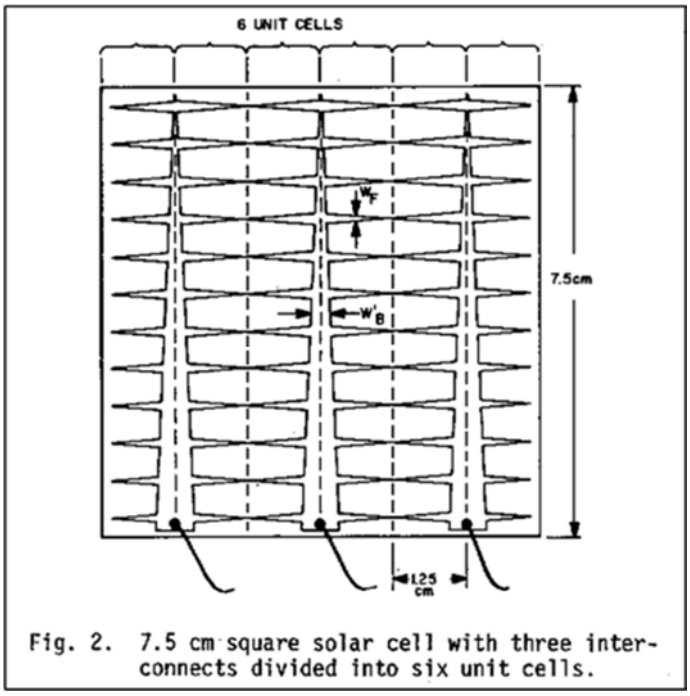


Figure 2. Regular grid design with tapering and fingers with tapering [7].

It is also well known that a grid of crossed metal filaments is less efficient than a regular grid (regular grid is shown in Figure 1 at right). Choosing a regular grid as the basic top contact design leaves primarily the metal line width and laser windowing spacing as the geometric optimization parameters. (Other considerations can be made for the ends of the model—the extreme edges of the device where often the spacing is increased or

filaments curved near the ends to improve performance—but we have not studied this effect.) The outer metal ring is made thicker (1-mm) for solderability. Solar cell top contact metal line optimization methods have been explored [8] showing that solar cell performance can be increased with narrower metal line widths. While metallization techniques have made finer metal dot resolution more cheaply available, cost effective metallization limits the metal line width to no less than 10-μm. The question then is what is the optimal spacing.

The simplest method of optimizing the spacing is increasing the width to allow more light in and therefore photogeneration of charge carriers in the silicon of the device. However, the current must travel to the metallization through the top-layer of the highly doped silicon. As the spacing widens to allow more light in, the current must travel further through the resistive top-layer. Ultimately there is a balance that is made between photogeneration and resistive losses [7]. For the PCSS in a simple pulse forming network (see Figure 3), the on-state resistance (R_{on}) is the measure of the efficiency with respect to the load resistance. Therefore, we use R_{on} to optimize the spacing for the PCSS (solar cells have different methods of determining efficiency and for optimizing top contact spacing).

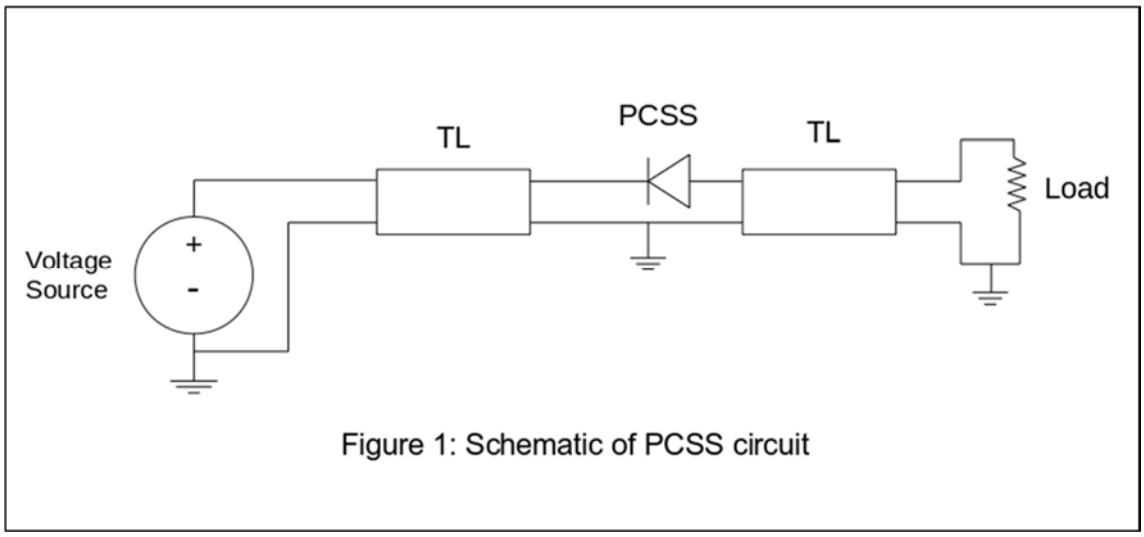


Figure 3. Circuit schematic of the experimental on-state resistance test setup used for TCAD circuit simulation.

While various theoretical methods exist to calculate an optimal spacing [8,9], TCAD allows for a more detailed description of the device and modeling of the semiconductor device physics. Initial TCAD test simulations immediately showed the existence of an optimal spacing considering only R_{on}. Further TCAD simulations for fuller sized device models matched closely to the actual PCSS devices including doping-dependent free carrier absorption of laser light were carried out. The simulations were analyzed to determine the percent laser energy reduction vs window spacing and the optimal spacing producing the maximum amount of laser energy reduction.

The p-side doping of the Si-PCSS was originally chosen to allow more light to pass through and be absorbed in the intrinsic region of the device while balancing this concern with the higher p-side doping needed for an ohmic contact. In optimizing the top contact window spacing, a doping-dependent free carrier absorption method was needed in TCAD for the correct photogeneration and correct estimation of the required laser energy. A custom photogeneration model was developed considering doping dependent free carrier absorption in silicon [13-16].

3.7.4 Tasks, Milestones, and Status

(A) Perform literature review of solar cell top contact design / JUL 2020 / Solar cell top contact design useful for PCSS and theoretical methods best implemented in SPICE for the optimal metal line width and spacing.

The literature review provided understanding of the applicability and methods of solar cell top contact design to the PCSS. From this study, the metal line width was found to improve performance the narrower it can be made. Also, in practice, the optimal spacing is what is needed. The theoretical methods, implemented through SPICE circuit simulation, provided the best method but are unavailable for PCSS or are difficult to self-implement.

(B) Determine if an optimal spacing based on on-state resistance exists with TCAD simulation / JUL 2020 / Milestone: TCAD successfully simulated the existence of an optimal spacing.

The earliest TCAD simulations performed for top contact optimization began to show the existence of optimal spacing, but it was not understood this should be examined until the literature review of solar cells. Further TCAD simulation conclusively showed the existence of the optimal spacing using on-state resistance as the performance metric for PCSSs.

(C) Develop doping-dependent free carrier absorption (DDFA) model for photogeneration in TCAD / 21 AUG 2020 / Milestone: TCAD DDFA modeled significant ~10% required laser energy increase.

Doping-dependent free carrier absorption (DDFA) was improved by refining the meshing used in TCAD simulations to produce no photogeneration underneath the top contact filaments. The top contact filaments are 10-μm wide and the mesh had to be refined to at least 5-μm with finer meshing down to 1-μm producing better results. Next, the TCAD model was implemented for 1-cm^2 area device models as opposed to earlier 1-mm^2 models. DDFA raised the required laser energy for an on-state resistance by 10%, showing it was non-negligible.

(D) Run parameter space study for 1300-μm thick Si-PCSS with DDFA / 12 NOV 2020 / Milestone: ~30% laser energy reduction;

Experimental on-state resistance versus laser energy results were almost exclusively conducted on 1300-μm thick Si-PCSS while TCAD simulations initially made use of thinner devices to reduce mesh points and save computational time. A new DDFA TCAD study has being completed for percent laser energy reduction vs spacing by first producing on-state resistance vs laser energy curves with a comparison to experimental data for 1300-μm devices. The inclusion of the DDFA photogeneration model greatly increased simulation time for the larger models. Due to mesh point limitations of a 1300-μm thick, 0.8-cm wide 2D device model was used. Simulation results indicate that a laser energy reduction of up to 30% is possible and needs experimental verification.

(E) Fabricate top contacts and test on-state resistance vs incident laser energy / 15 DEC 2020 to fabricate / Top contacts metallized / Milestone: FEB 2021 delivery of new top contacted Si-PCSS. MAR 2021 new top contacted Si-PCSS tested.

(F) TCAD determination of Si-PCSS variability in optimized top contacts dependent on p-doping profile peak concentration and doping depth for boron and aluminum. More accurate determination of optimal spacing in laser windowing of top contacts and switch geometry dependence for general applicability of optimal top contact. / DEC 2020 / P-doping not found to effect optimal spacing. Finer determination on optimal spacing and geometry dependence of optimal spacing not completed.

P-doping was not found to significantly alter the optimal spacing. More accurate determination of the optimal spacing finer than 350-μm was never attempted but would help in distinguishing smaller shifts and trends in the optimal spacing varying with doping, applied voltage and laser energy. Additional simulations over a range of device sizes were not attempted to determine a scaling law for the results to larger devices (7-cm length scale).

3.7.5 Methods and Approach

Purely theoretical methods for solar cells were first consulted [7,8] in how to design and optimize PCSS top contacts. The theoretical approach suggested the regular metal grid design optimized for spacing was best, especially for smaller cells such as the PCSS. Theoretical methods are best realized in SPICE circuit simulation and methods exist to model full scale PCSS in detail but require manual development of the computer tools and are at the edge of computational feasibility [11,12]. Ready tools exist in TCAD for superior physical modeling, but for smaller scale PCSS models [3]. The approach then is to model a sufficiently large PCSS in TCAD for which the optimal spacing (considering a minimum 10-μm metal line width) will hold for both the smaller sized TCAD PCSS device models (0.8-cm width) and the actual full scale PCSS device (1-cm width). These two device sizes are nearly the same. The results of the 1-cm TCAD and experiments are then used for 7-cm width PCSS.

The window spacings studied for the TCAD simulations to determine the existence of an optimal spacing due to a lowest R_{on} were over a wide range as seen in Figure 4 and ranged from 10-μm to the full size of the device (no metal filaments) with a greater density of the studied spacings for smaller spacings. Later simulations for the percent laser

energy reduction possible used 20-, 40-, 60-, 100-, 200- and 350-μm window spacings. The spacings larger than 350-μm were not studied since smaller spacings are thought to reduce the current density and heating, while larger spacings are useful when less metal is important for either cost or reflection of light back to the optics and the optical fiber. The computational cost of the simulations were also reduced by studying spacings less than or equal to the optimal spacing (note the earlier TCAD R_{on} vs spacing study for the existence of an optimal spacing less accurately determined the optimal spacing to be around 400-μm).

One factor of concern is the absorption of laser light (at 1064-nm in silicon) in the p-doped anode side of the PCSS since the light must first travel through the p-doped anode to the low n-doped intrinsic region. To account for additional doping-dependent free carrier absorption of 1064-nm in silicon, C programming code within TCAD function templates for photogeneration was modified. Other factors that could affect the R_{on} for various laser energies included area effects, reflectivity at the surface, and Gaussian vs uniform laser spatial profile (only uniform studied).

TCAD simulations determined that small enough width (and therefore area) devices had a different optimal spacing than for sufficiently wide devices for which the optimal spacing no longer changed (also implies the applicability of the 1-cm simulation results to the 7-cm devices). The change in optimal spacing is in part due to the smaller number of possible metal filaments for a small width device (less than one hundred as opposed to several hundred metal filaments). The reflectivity of the TCAD model was matched to the R_{on} experimental testing conditions where the silicon surface (covered with an anti-reflective coating) is exposed to air directly, as opposed to being covered additionally with Silgard and plastic covering. There can be some experimental error on the reflectivity due to cleaning and finger smudges on the laser window.

A series of TCAD simulations in a 2D parameter study were performed. The 2D parameter study consisted of varying both laser energy delivered to the switch and window spacing. The simulations were performed isothermally at 300-K. The PCSS were simulated within a TL-circuit or simple pulse forming line (see Figure 3) closely resembling the actual experimental R_{on} test setup. R_{on} values from simulation were tabulated vs laser energy (figures in the Results and Discussion Section). These data were fit to power law functions, as R_{on} is known experimentally to be inversely proportional to the incident laser energy (rather than a purely linear interpolation of the data). From here, laser energy differences between different window spacings at a fixed R_{on} were collected relative to the 20-μm window spacing originally used. A percent laser energy reduction (E_{per}) vs R_{on} can then be tabulated:

$$E_{per} = \frac{E_{20} - E_{wid}}{E_{20}} * 100\%$$

where E_{20} is the baseline required laser energy for devices with a window spacing of 20-μm and E_{wid} is the wider window laser energy. Owing to the relatively flat or constant

percent laser energy reduction per R_{on}, percent laser energy reduction vs spacing can be obtained.

3.7.6 Results and Discussion

Simulations

The first TCAD simulations were focused on verifying the existence of an optimal spacing based on R_{on} and not laser energy reduction. Subsequent TCAD simulations for laser energy reduction used a much lesser number of spacings and a greater number of laser energies. In Figure 4, spacings from 10-μm to the entire possible 8000-μm wide window (no metal filaments) are shown for the 1-cm device with 1-mm outer electrode. From about 100-μm to 1600-μm, R_{on} remains relatively low but outside these boundaries rises. For lower spacings the R_{on} rise is due to increasingly less laser light creating photogenerated carriers for conduction. For higher spacings the R_{on} rise is due to the increasing distance carriers must travel in the more highly conductive top-layer of silicon before reaching metal. It is thought that lower R_{on} should also result in better thermal management, but thermal studies are required. The optimal spacing is the spacing with the lowest R_{on} and was at 400-μm for this study (later studies refined the determination of the optimal spacing to 350-μm). Also, the optimal spacing is seen not to vary with increasing laser energy as R_{on} rises. Optimal spacing was also found (in other studies) to not vary much with p-side doping concentration or reverse-bias TL charge-side voltage.

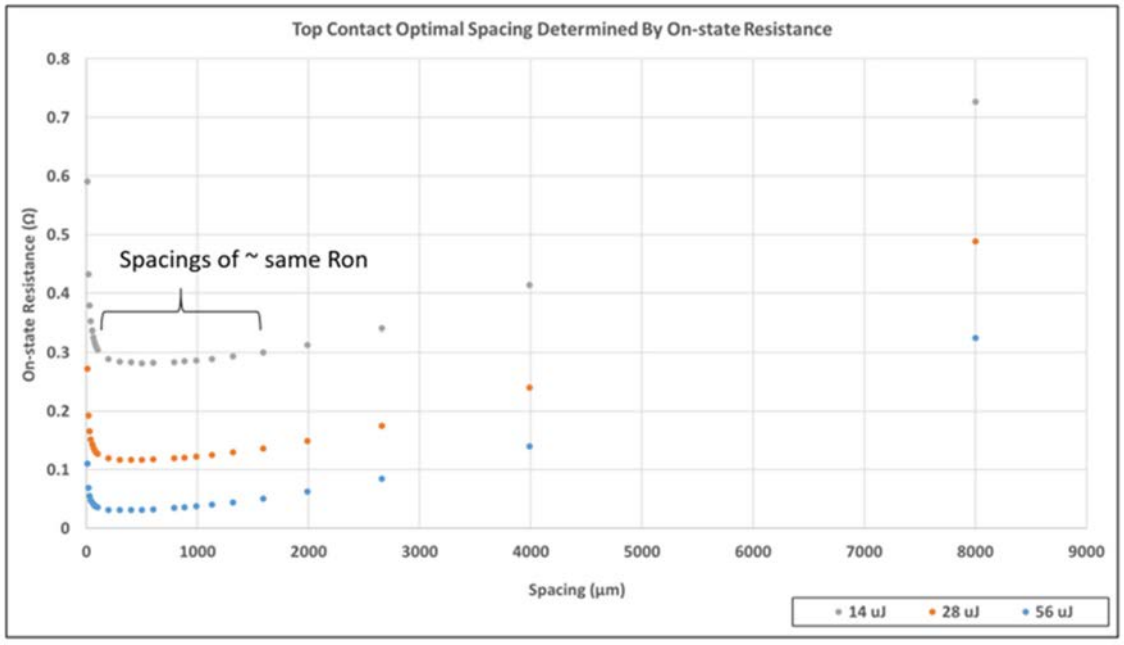


Figure 4. Window spacings show region of minimal on-state resistance (R_{on}) outside of which R_{on} increases dramatically.

A set of TCAD simulations were carried out with the goal of comparison to earlier experiments and a later set of planned experimental measurements using the R_{on} testing setup. A doping-dependent free carrier absorption (DDFA) model was added to the TCAD photogeneration model to account for absorption due to the highly doped p-side through which the laser light must travel to reach the thick intrinsic region of the Si-PCSS. Also, the reflectivity for the anti-reflective coating, silicon and air was added to the model to replicate test conditions. The data was visualized in the conventional R_{on} vs laser energy plots as in Figure 5. These additions to the modeling reduced the error between simulation and experiment.

The experimental data (exp) is seen to be within the ± 0.2-Ω error estimated for the R_{on} measurement when compared to the simulation results. Device variability plays a bigger role and must be averaged over enough devices to compare to experiment and simulation (for example see Figure 8). From the simulation curves, a power law is fit and the data points interpolated to more accurately estimate the laser energy difference between two spacing curves at a fixed R_{on} (due to the small number of simulation datapoints). The original spacing of 20-μm is used as reference to indicate improvement, as it happened the 20-μm spacing was not very optimal. A percent laser energy reduction curve vs R_{on} can then be tabulated as seen in Figure 6.

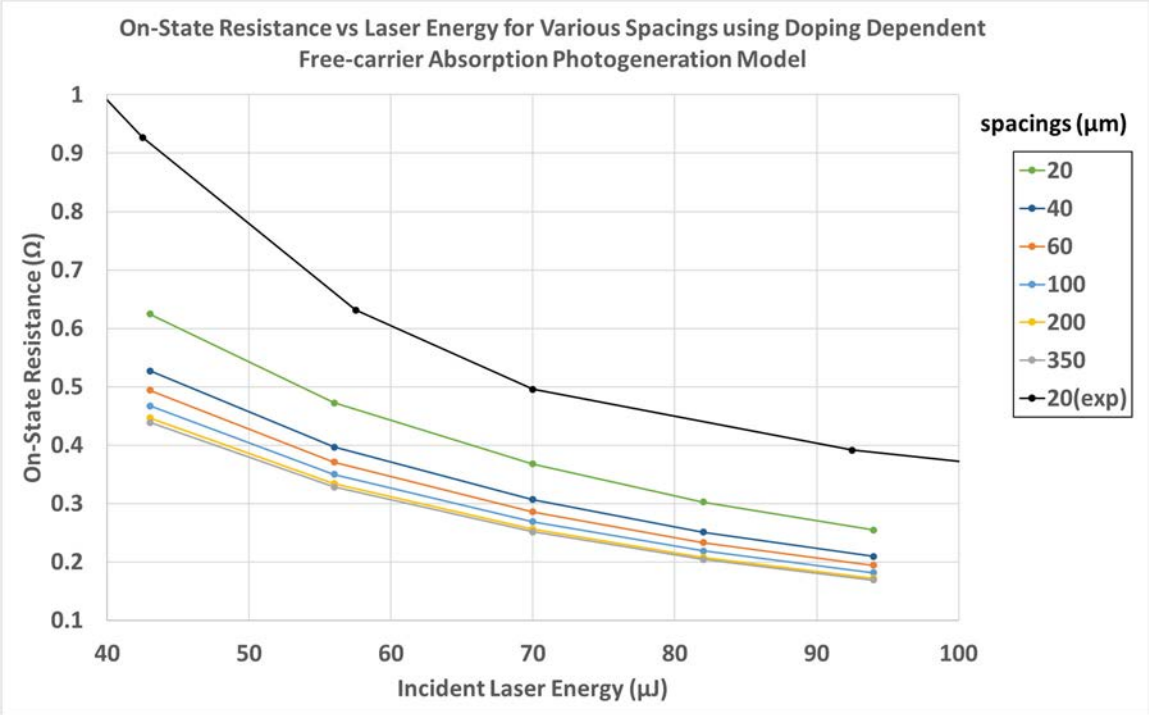


Figure 5. TCAD simulation results reproducing conventional on-state resistance vs laser energy curves as seen in experiment. (Black, top) exp line is for 20-μm spacing and is an experiment result.

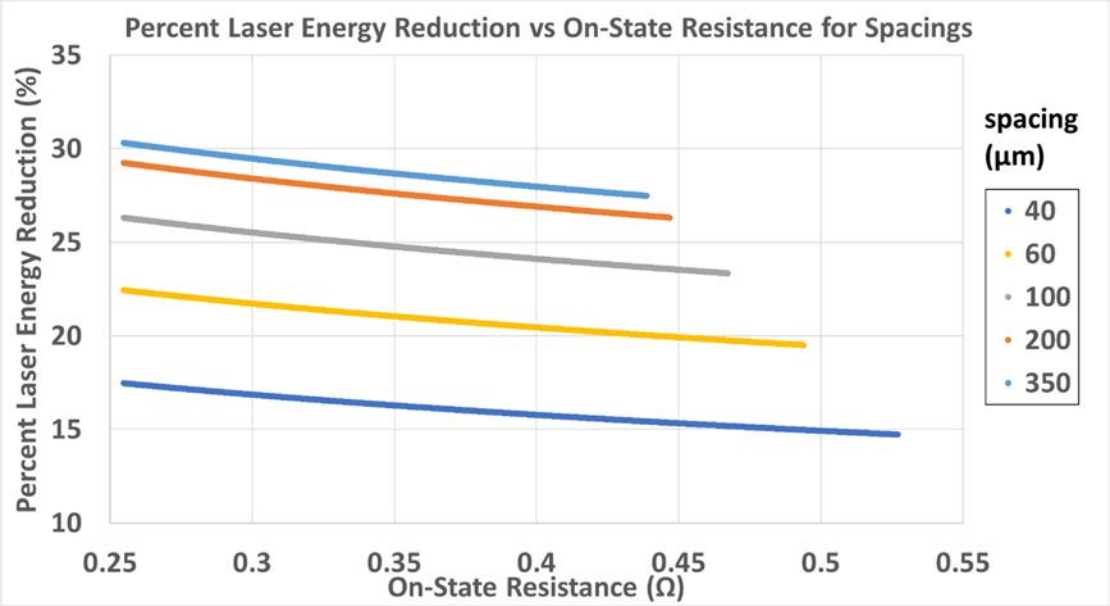


Figure 6. Percent laser energy reduction vs on-state resistance. The percent laser energy reduction across the on-state resistances tested (and laser energies used) is relatively flat or constant.

Since the percent laser energy reduction is nearly flat or constant over the range of R_{on} (and therefore laser energies) simulated, the average percent laser energy reduction can be plotted against the spacing, as in Figure 7.

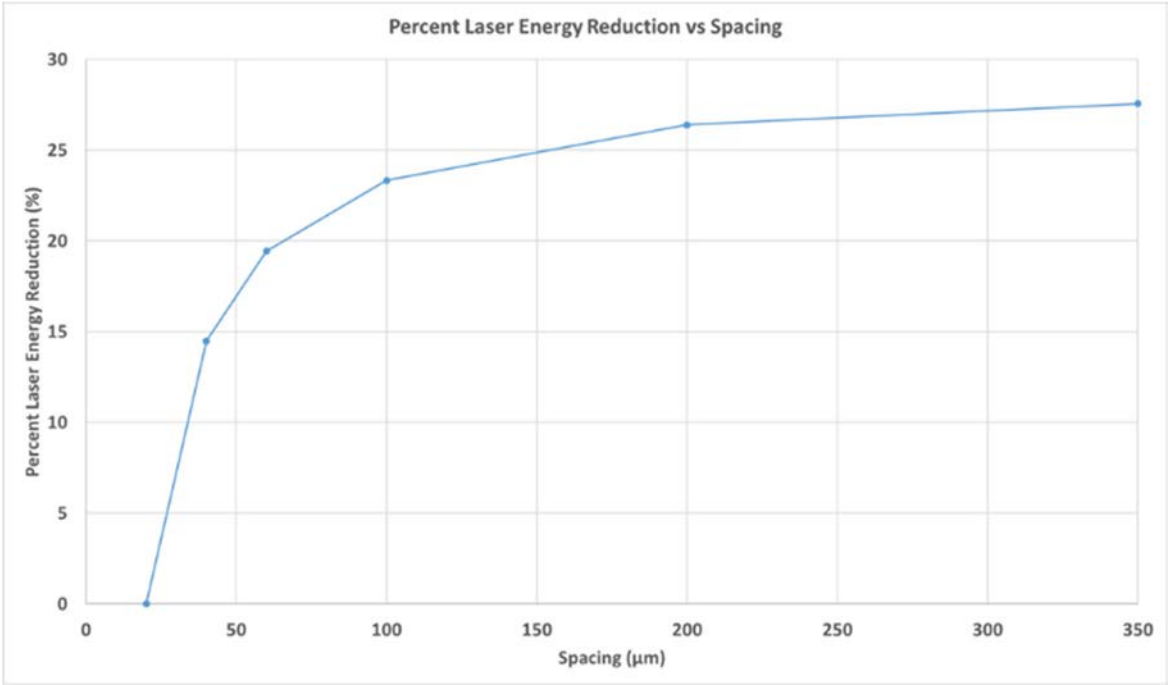


Figure 7. Percent laser energy reduction vs spacing curve shows 20-µm reference spacing with a zero percent laser energy reduction and the optimal 350-µm spacing with the maximum

possible laser energy reduction (and minimum on-state resistance). Beyond 350-μm the percent laser energy reduction again reduces below the maximum possible.

The 20-μm spacing is assigned zero percent laser energy reduction as the reference spacing. After the 350-μm spacing, the percent laser energy reduction will decrease (see Figure 4) and 350-μm is the minimum R_{on} and maximum possible percent laser energy reduction spacing to the degree of accuracy of the simulated data test points (the optimal spacing could be slightly higher or lower). There are especially large gains in percent laser energy reduction in increasing the spacing from the original and reference spacing of 20-μm to 100-μm spacing (where R_{on} is approximately as low as it gets). From this simulation data, spacings between 100-μm and 350-μm can be considered as optimal with 350-μm having the maximum possible percent laser energy reduction and lowest possible R_{on}.

Experiments

Based on TCAD simulations, 2 wafers of Si-PCSS with variable window spacing were fabricated by Semiconductor Power Technologies (SPT). The metallization method itself is relatively cheap and fast. Table 1 shows the number of devices of each spacing for 1-cm and 7-cm devices from 2 wafers. Dicing damage on the 2 wafers resulted in only one 7-cm Si-PCSS being testable and fourteen 1-cm Si-PCSS. All the 1-cm devices showed higher resistance than expected which may have been due to dicing damage.

Table 1. Si-PCSS variable window devices fabricated by SPT.

Wafer spacing/devices	Spacings (μm) and number of devices fabricated per spacing						Total devices per wafer
1 cm spacings	20 μm	40 μm	60 μm	100 μm	200 μm	350 μm	
1 cm devices per spacing	6 devices	6 devices	6 devices	6 devices	6 devices	6 devices	36 devices
7 cm spacings	-	-	60 μm	-	-	350 μm	
7 cm devices per spacing	-	-	5 devices	-	-	5 devices	10 devices

Si-PCSS prior to this report were measured for their R_{on} vs laser energy curves and were all 7-cm devices. In Figure 8 the data for eight 7-cm devices are shown and all have 10-μm metal line width and 20-μm window spacing and are shown as open square symbols and are from an earlier study. A tenth new 7-cm device from this study is shown with black triangles which has a 350-μm window spacing. All the eight 7-cm devices (prior to this study) are fit to a power law as a dashed dark blue line (Power in the figure key) which can be compared to the new single 7-cm, 350-μm window spacing result (magnified in the top right figure inset where the black circle shows the laser energy difference at a fixed R_{on}). In the inset or larger figure can be seen the 20-μJ laser energy difference at ~0.8-Ω R_{on}. With only one device the results could be fortuitous due to device variability, but are encouraging. Note, the single surviving 7-cm device from this study was badly damaged from dicing but did have R_{on} within the previously tested 7-cm as seen in Figure

8, however the new 1-cm devices (Figure 9) had higher R_{on} than previously tested 1-cm devices (no data provided but within earlier grant reports).

In Figure 9 the experimental data between 50-µJ and 100-µJ of laser energy are shown. The open symbols can be seen to occupy mostly the lower R_{on} values obtained across the laser energies tested. By grouping the results into 100-µm and greater and less than 100-µm spacing, the R_{on} vs laser energy curves of the two groups can be compared, see Figure 10.

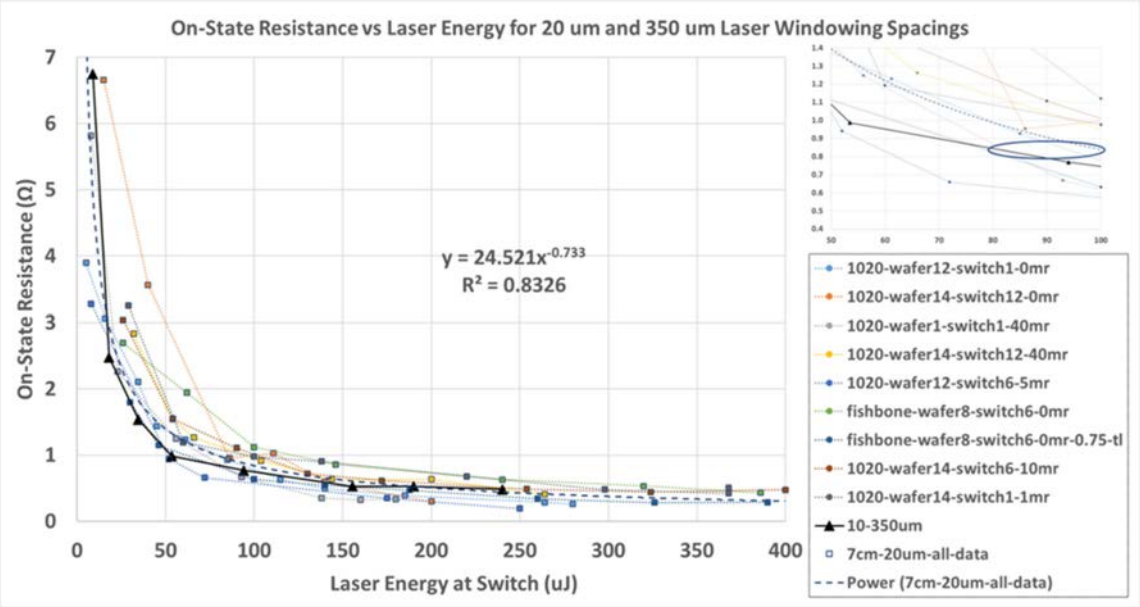


Figure 8. On-state resistance vs laser energy incident at switch for eight 7-cm, 20-µm window Si-PCSS and a single 7-cm, 350-µm Si-PCSS (large black triangles). Half of the 20-µm curves are nearly the same as the 350-µm curve. The dashed dark blue line is the power law fit to the 20-µm data. The inset is a magnification of the region comparing laser energy used at ~0.8-Ω on-state resistance between the 350-µm device and the 20-µm data. The circled region in the inset shows the 20-µJ laser energy reduction.

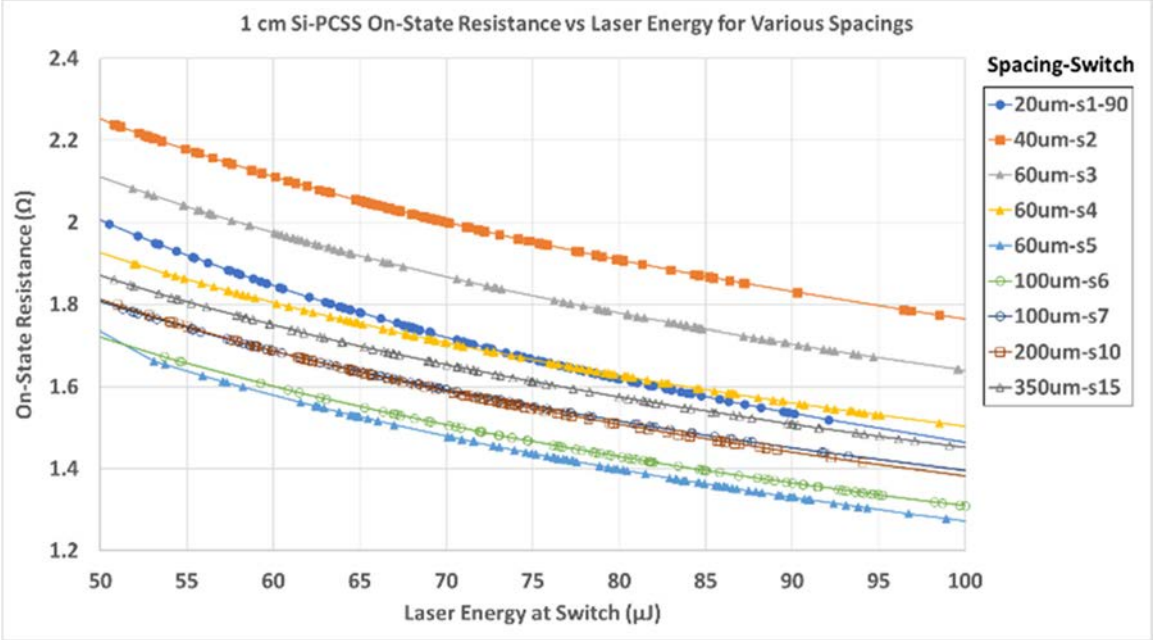


Figure 9. Experimental on-state resistance vs laser energy curves for SPT variable window Si-PCSS.

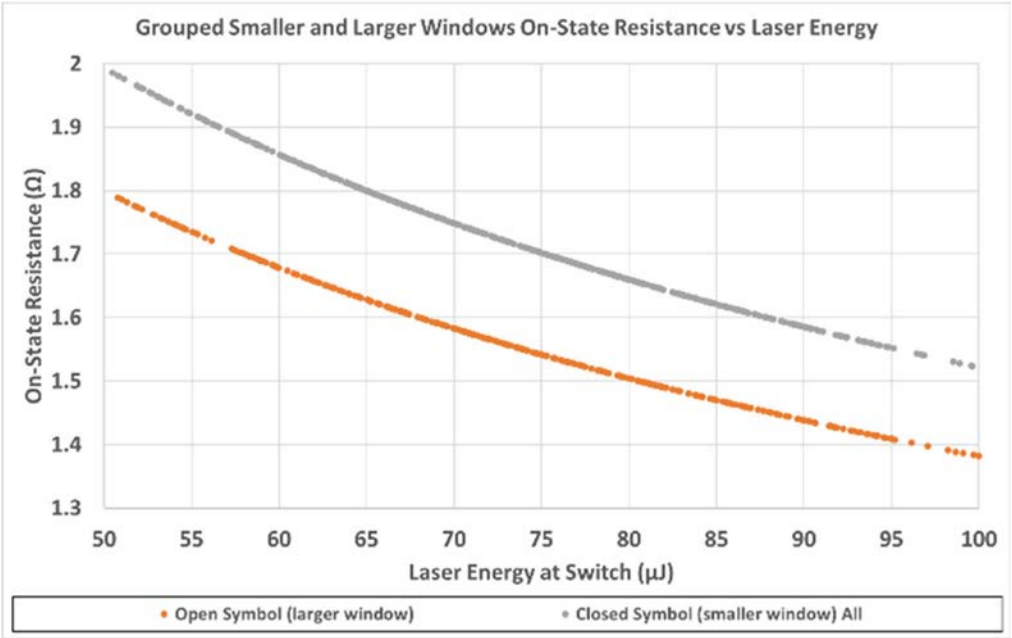


Figure 10. On-state resistance vs laser energy curve with the less than 100-μm window spacing results (gray) and 100-μm and greater results (orange) averaged together. A 22% laser energy reduction can be seen in the graph between the 100-μJ (gray) data point and the (orange) datapoint at the same on-state resistance (at ~1.52-Ω).

A 22% laser energy reduction can be deduced from the graph of the two groups which is over-estimated due to the device variability and low number of devices experimentally tested. The analysis of the experimental data provides a qualitative result of a significant percent laser energy reduction for devices that have approximately optimal R_{on} (100-µm to 350-µm spacing). Stronger experimental data would yield useful information for publication and inhouse device performance. A study of 2 or more wafers of 1-cm devices, where dicing damage does not occur will likely yield lower R_{on} devices, and a larger number of good devices. And should produce stronger data confirming or not the simulated R_{on} vs laser energy, percent laser energy reduction vs spacing, and the optimal spacing for maximal percent laser energy reduction. The experimental and simulation data were not comparable on an absolute scale due to a higher than usual R_{on} for the actual 1-cm devices that received dicing damage, but the relative trend of larger windows having greater percent laser energy reduction held between simulation and experiment.

3.7.7 Summary and Recommendations

A laser is necessary to trigger the closing of the Si-PCSS but requires a high laser energy which leads to higher costs and sizes of the laser system. To reduce the required laser energy, purely theoretical and SPICE methods were first explored for Si-PCSS top contact optimization, which led to exploring TCAD simulations to test for an optimal on-state resistance. After showing an optimal on-state resistance existed using TCAD simulation, more complete top contact window spacing and laser energy studies were performed with a doping-dependent free carrier absorption model being added to the photogeneration model to improve the accuracy of the results. Further simulations with more realistic device sizes were executed and a percent laser energy reduction versus top contact window spacing was tabulated. TCAD simulation results showed a possible maximum ~30% laser energy reduction when using the optimal 350-µm spacing. Experimental results confirmed a qualitative effect of increased laser energy reduction with more optimal spacings. More and better devices will be needed to verify conclusively the simulation results with experimental data. It is recommended to fabricate and test another 2 wafers of 1-cm Si-PCSS with variable window spacing to experimentally confirm the TCAD optimal spacing and percent laser energy reduction.

3.7.8 Outputs

Photoconductive Contact Pattern for Enhanced Charge Collection, July 8, 2020, IP disclosure.

3.7.9 References

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3.8 Characterizing and Optimizing On-State Resistance in GaN:X PCSS

(Heather Thompson)

3.8.1 Executive Summary

Towards cUAV defense on navy vessels and vehicles, there is a need for compact, cost-effective RF pulse generation systems. Such systems typically utilize silicon (Si) or gallium arsenide (GaAs) photoconductive semiconductor switches (PCSS) due to their low cost and material maturity, but as applications require more extreme operating ranges, their limitations are becoming increasingly apparent. Gallium nitride (GaN) is a wide-bandgap (~3.4 eV) semiconductor with material characteristics allowing for higher operating voltage, frequency, and temperature. However, an important problem to solve is minimizing conduction losses in order to maximize efficiency and reduce thermal issues when using compensated, semi-insulating GaN:X at <1 Ω on-state resistance. To achieve this, the material, device, and system levels must be considered, as these all factor into on-state resistance, resulting in several variables that must be altered toward optimization. To reduce the number of iterations studied, a literature review was conducted to determine certain “fixed” constraints: operating mode, photogeneration mode, and overall device type. It was concluded that linear operating mode would be used due to minimal jitter operation and increased device lifetime, intrinsic activation due to increased optical efficiency, and lateral devices because of the intrinsic mode constraint. Future iterations will also include nanostructure topology to increase the active volume in the device, so as to overcome on-state resistance minimization limitations caused by the shallow absorption depth of the photon source.

On-state resistance measurements collected at UMKC focused on wavelength and incident laser energy (number of photons) due to the ease of manipulating these variables with a limited number of available devices. It was shown that at wavelengths over 370 nm, there is an exponential increase in on-state resistance for all gap lengths tested (20–1000 μm); therefore, using a cheaper, easier to source laser at higher wavelengths is not a viable option. As a function of incident energy, on-state resistance reached ~1 Ω at approximately 20 μJ for a device with 500 μm gap length, thus energies above this level do not generate excess carriers and instead contribute to device heating, so it is not beneficial to source more costly, powerful lasers unless a wider gap length is needed for high power operation and to prevent surface flash over between contacts. Current work is focused on simulations being performed using TCAD and COMSOL, with initial results being compared to experimental results to determine simulation validity. Once determined valid, simulations will be used to conduct parametric sweeps of variable material, device, and system level alterations towards minimizing on-state resistance and increasing efficiency without the need for several iterations of physical GaN PCSS devices.

3.8.2 Objective

Traditionally, RF generation using photoconductive semiconductor switches (PCSS) relies on materials such as silicon (Si) or gallium arsenide (GaAs) due to their availability and low cost; however, as these applications begin to require higher operating frequencies, powers, and temperatures, with the same or reduced system form-factor, the theoretical operating limits of these materials are being reached. Current PCSS-based RF generation systems can achieve MW-range output power, ones-of-gigawatts frequency content, and electrical efficiency of ~60%, but require increased laser energies and device sizes to reach this efficiency and necessary operating power. An alternative material for this purpose is gallium nitride (GaN). Its 3.4 eV bandgap, 1000 cm^2/Vs electron mobility, and thermal properties could enable pulsed-power applications requiring up to 5 MV/cm critical field, high-frequency operation, and high operating temperatures, respectively.

A key challenge with using GaN-based PCSS systems involves minimizing conduction losses, maximizing efficiency, and reducing thermal issues in compensated, semi-insulating GaN:X (i.e., GaN:X with X=C, Fe,…) to achieve <1Ω on-state resistance by optimizing modifiable parameters of GaN:X at the material, device, and system levels, while still maintaining quick switch turn-off time and low turn-off losses. Towards this goal, simulations and available experimental results, from both the literature and collected results at UMKC, will be used in determining the optimal GaN:X PCSS device characteristics.

Relevance to OSPRES Grant Objective: Increase efficiency of Navy cUAV PCSS-based systems through exploiting the material properties of GaN and optimizing GaN PCSS by minimizing on-state resistance and conduction losses, leading to enhanced SWaP-C^2 capability with greater modularity and scalability.

***Challenges*:** The high cost of material leads to a limited number of devices available for experimental testing and analysis, requiring most of the optimization studies to be performed using simulation software (COMSOL and TCAD).

***Risks*:** Simulation results may differ from experimental results for certain PCSS parameters due to particular photogeneration and recombination parameters not being included in models along with non-ideal, real-world experiments requiring additions such as encapsulation material or other changes not fully addressed in simulation.

3.8.3 Technical Background

On-state resistance is a major contributor to losses and decreased efficiency in GaN-based PCSSs, and this can be mitigated by optimizing certain material, device, and system level parameters towards its minimization. By defining the parameters affecting on-state resistance, how they are correlated to one another, and the degree to which they can be easily manipulated, GaN-based PCSS devices can be used to reduce the size

and cost of RF generation systems along with providing increased power, frequency, and temperature capabilities.

By identifying the operating mode and photogeneration method to be used, the number of possible parameters considered for optimization is reduced. Two modes of operation are possible for GaN PCSS: linear (one carrier generated per absorbed photon) and non-linear (impact ionization utilized to generate multiple carriers per absorbed photon). While a non-linear mode could offer reduced laser energy needs and increased responsivity, linear operation is preferred due to decreased jitter and increased device lifespan and is the focus of this work [1]. Photogeneration methods available for GaN PCSS are intrinsic—relying on incident photons at or above the bandgap energy to move electrons to the conduction band—and extrinsic—exploiting mid-gap impurities and defects that can be activated using below bandgap photon energy—but intrinsic operation offers lower on-state resistance due to higher quantum and optical efficiency. However, due to the shallow absorption depth in intrinsic operation, the study is restricted to lateral devices [2].

Many material characteristics are determined by their inherent material properties and cannot be manipulated, so we further reduce parameters of this study to those which can be changed during the manufacturing process. The first material alteration considered is the carbon doping concentration in GaN, which can be altered during the growth process by varying the growth temperature, pressure, and ratio of precursors, however must stay within a certain range to maintain semi-insulating material properties instead of n- or p-type properties [3]. The second material characteristic considered is the type and quality of the substrate. Typically, Si or GaAs is used because they are inexpensive, but the use of SiC or GaN can reduce defects caused by dislocations and strains from lattice and thermal mismatch between the substrate and GaN, which can lead to device failure.

Device level parameters will encompass device contact type and geometry as these can greatly affect the responsivity and power handling capabilities of these devices by changing the amount of the device surface covered by contact material and the gap length between contacts, respectively. Additional device changes include the addition of a nanostructure wall array of “nano-fins” based on work done by Liu et al. (2021) using GaAs PCSSs. This work sought to overcome limited active device volume restricting the minimization of on-state resistance due to the shallow absorption depth of incident photons (~0.14 μm at 532 nm incident photon wavelength for GaAs). By adding a nanostructure wall array of “nano-fins” in the gap length of the device (Figure 1), or 3D grooves in the surface that are less than one half of the size of the incident photon wavelength to avoid scattering, photon absorption occurs on the top and side surfaces of these fins, essentially increasing the active area cross section and improving photocurrent while reducing trigger fluence (incident energy per area needed for device activation). Shown in Figure 2, photocurrent in linear mode operation was increased from 1.9 μA to 106 μA for a trigger fluence of 3.8 mW/cm^2 with the addition of these fins [4].

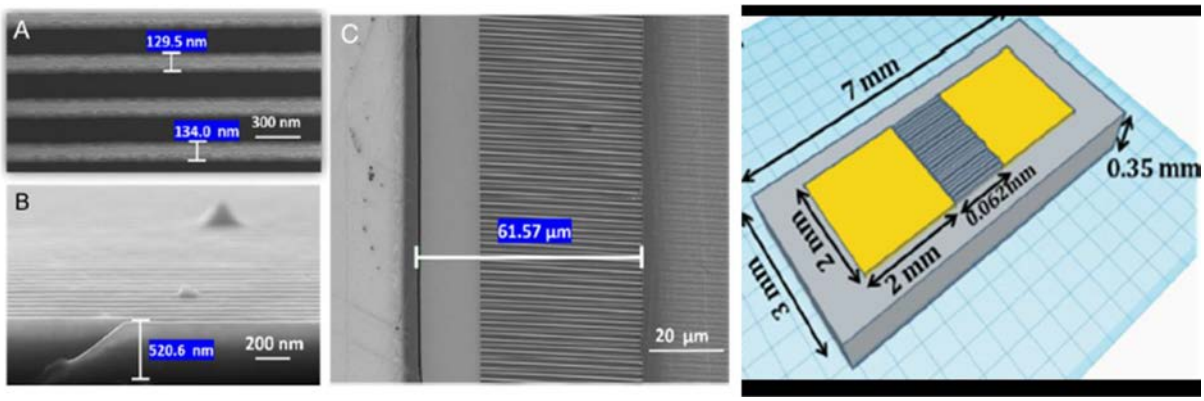


Figure 1. (Left) SEM images of nanostructure wall array on GaAs PCSS for increasing effective penetration depth and active volume to reduce on-state resistance with (A) being the top view, (B) the side view, and (C) a zoomed-out image of the nano-wall array. (Right) Illustration of GaAs PCSS device geometry with nanostructure wall array placement seen in the gap length of the device [4].

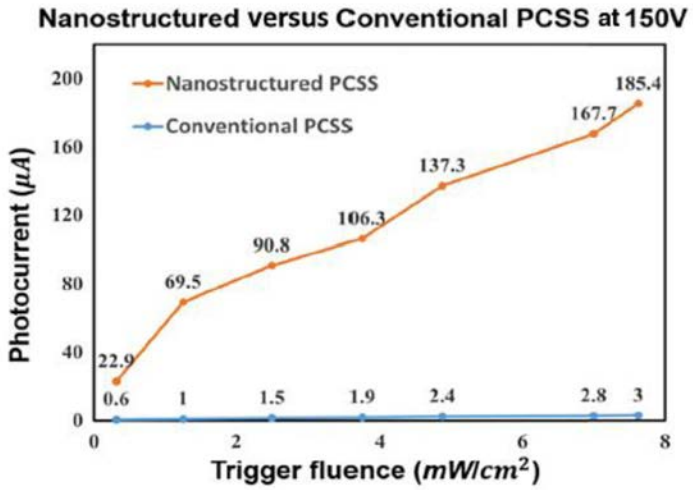


Figure 2. Photocurrent as a function of incident trigger fluence (energy per area) for a conventional and nanostructured GaAs PCSS showing the increase in photocurrent generated using the nanostructure addition to the devices [4].

System level parameters include the operating circuit and incident photon source, which add additional cost and size to the overall system depending on the source used. For the laser, the wavelength, energy (number of photons), operating frequency, and pulse width will be considered as these all affect efficiency and on-state resistance. An additional consideration towards minimizing on-state resistance without adding to incident laser energy, and costs, is the energy density and spot shape of the laser, which can be modified by keeping the laser energy and pulse width constant to maintain a steady average power. In the study mentioned in Zhang (2015), GaAs PCSS devices were used with an incident energy of 1 µJ and pulse width of 300 ns to obtain an average laser power of 33.3 W for varying spot shapes and energy densities as shown in Figure 3. It was found

that the more focused shape, with the highest energy density, achieved the lowest on-state resistance (Figure 4) [5]. This finding shows that using additional optics to spread out the incident laser spot size to the entire active area may increase the on-state resistance of the device compared to using a focused, smaller spot size.

Table 1. Performance details of laser pulses.

spot shape	Size(mm^2)	Energy density($uJ.mm^{-2}$)
scattered	16.24	0.06
Long-striped	9.975	0.1
focused	0.5027	1.99

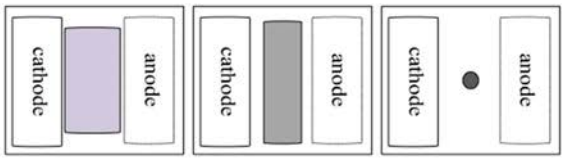


Figure 4. (Left) Incident laser characteristics for incident laser power of 33.3 W with varying spot shapes and energy densities incident on the GaAs PCSS. (Right) Illustration of the various spot shapes used in the GaAs PCSS study.

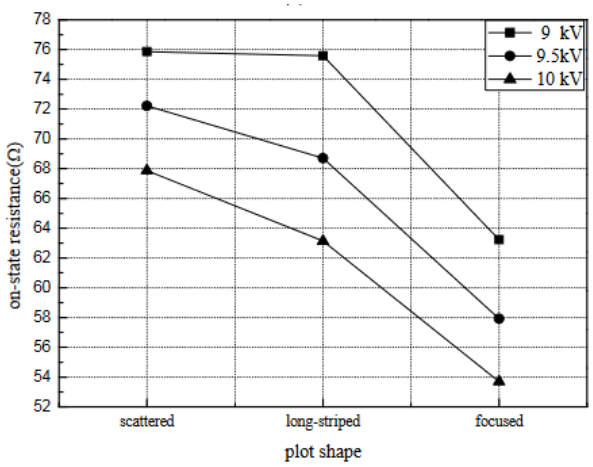


Figure 4. On-state resistance results from using different laser spot shapes and energy densities.

3.8.4 Methods and Approach

Towards determining the optimal GaN PCSS parameters to maximize efficiency, on-state resistance was calculated from output voltage versus charge voltage measurements collected at UMKC focusing on changes in on-state resistance due to altering incident wavelength, incident energy, and device gap length.

3.8.5 Results and Discussion

A literature review was conducted to parse out the parameters affecting on-state resistance in GaN PCSS (Figure 5), and these were narrowed down to those changeable within the material, device, or system levels of a GaN-based PCSS RF generation system. This review also allowed for constraining operating and photogeneration modes to linear mode due to increased device lifetime and minimal jitter, and intrinsic mode due to increased optical efficiency, respectively; however, the constraint of intrinsic mode also limits the device type to lateral PCSS.

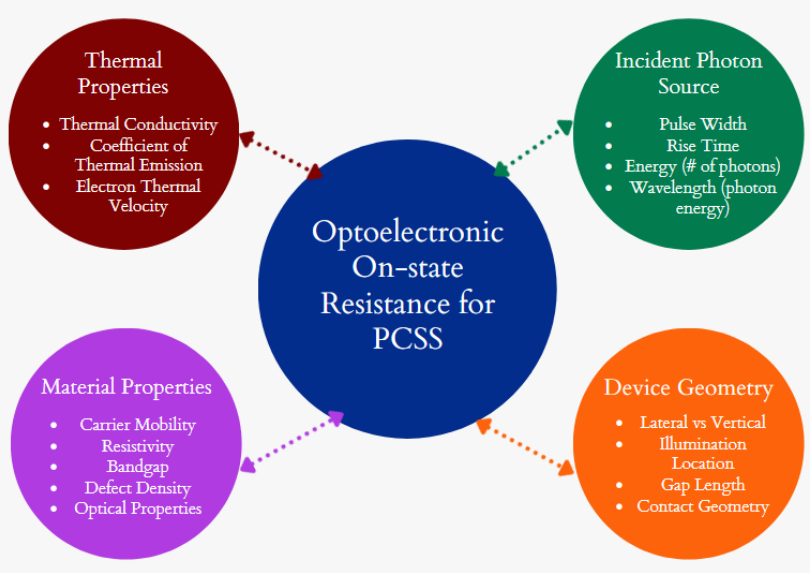


Figure 5. GaN PCSS on-state resistance parameters for Gan PCSS.

At UMKC, experimental data measuring output voltage versus charge voltage was collected and used to calculate on-state resistance. This data primarily focused on changes in on-state resistance as a function of wavelength and incident energy (number of photons) of the incident photon source, as these were the easiest parameters to change without having a variety of devices on hand with differing material properties. Wavelength-dependent on-state resistance was calculated from measurements taken using devices with variable gap lengths (from 20 μm up to 1000 μm) as shown in Figure 6. It was found that with increased gap length, the operating voltage can be increased due to the reduced chance of surface flashover between contacts, but the required incident energy needed to minimize on-state resistance also increases with gap length. On-state resistance at ~1 Ω was not achieved for gap lengths above 20 μm due to the energy of the incident laser not being sufficiently high. At wavelengths over 370 nm, there was an exponential increase in on-state resistance for all gap lengths, showing that photon sources at and above this wavelength, which are typically easier and cheaper to source, are not viable options.

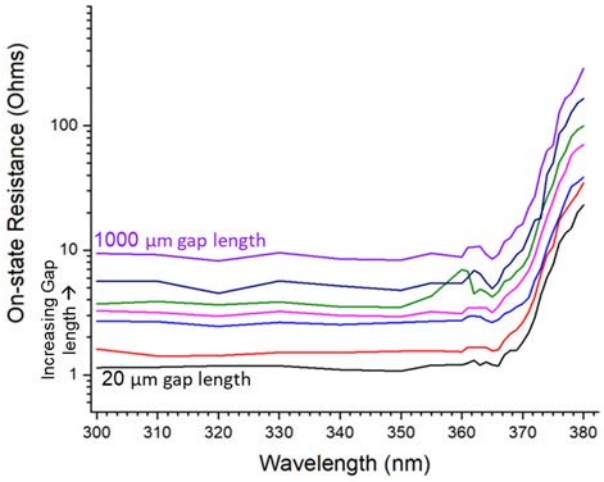


Figure 6. On-state resistance as a function of wavelength for GaN PCSS with different gap lengths.

Using a 500 μm gap length GaN PCSS, on-state resistance as a function of incident energy was also calculated from experimental results, as laser energy is a huge portion of the laser cost. It was shown that on-state resistance, with this gap length, is ~1 Ω at approximately 20 μJ, meaning that energies above this level do not generate excess carriers in the device but instead contribute to device heating.

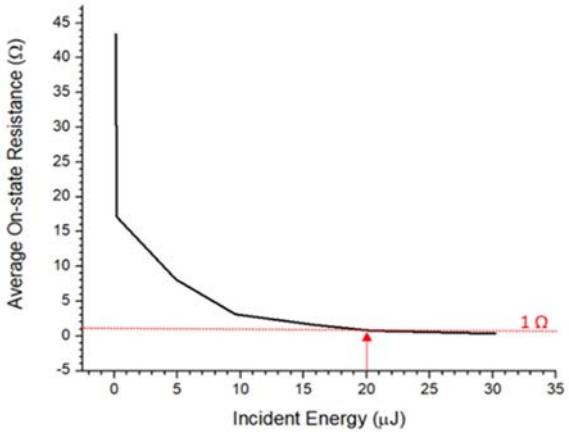


Figure 1. Average on-state resistance as a function of incident energy using a 500 μm gap length GaN PCSS.

Simulation results in TCAD and/or COMSOL are being compared to experimental results collected at UMKC to determine simulation validity and any alterations necessary to obtain accurate simulation results towards optimizing GaN PCSS for minimizing on-state resistance.

3.8.6 Summary

Literature review completed towards determining constraints and changeable parameters to optimize on-state resistance in GaN PCSS, leading to a material option that provides improved efficiency and SWAP-C2 capabilities for a PCSS-based RF generation system.

Constraints:

- Linear mode due to minimal jitter operation and increased device lifetime.
- Intrinsic activation because of increased optical efficiency over extrinsic activation.
- Limited to lateral devices resulting from intrinsic mode constraint.

Changeable Parameters:

- Material and growth characteristics: doping concentration, substrate type and quality
- Device geometry: gap length, device area, interdigitated vs traditional linear, etc.
- Laser characteristics: incident wavelength, incident power (number of photons), energy density, and spot shape/size.
- Nano-structure topology: increasing active volume in the device to overcome on-state resistance minimization limitations due to shallow absorption depth of the photon source through utilizing an array of fins <1/2 the incident wavelength, to prevent scattering. This allows for improving optical efficiency without increasing the incident laser energy (number of photons) thus preventing increased laser costs and size. A similar study using GaAs PCSS devices showed an increase in photocurrent from 1.9 μA to 106 μA for a trigger fluence of 3.8 mW/cm^2 [4].

A working GaN PCSS model was created using both COMSOL Multiphysics and Silvaco TCAD to allow for ongoing parametric studies towards minimizing on-state resistance in GaN PCSS without the need for manufacturing several iterations of devices.

3.8.7 References

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3.9 Drift-Step-Recovery Diode Testing, Simulation, and Optimization

(Jay Eifler)

3.9.1 Executive Summary

Drift-step-recovery diodes (DSRD) and DSRD-based high-voltage pulse generators are competitive with photoconductive solid-state switches (PCSS) and PCSS-based systems as they do not require a laser, reducing system size and cost, while maintaining the high peak power and fast risetimes required for countering unmanned-aircraft systems (cUAS). To design and optimize DSRD and DSRD-based pulsers, accurate DSRD modeling is required. DSRD have been modeled with Silvaco TCAD simulations to optimize the DSRD doping profile for fast risetimes with a maximum of peak power. A DSRD SPICE model has been developed based on the standard diode model and in-house current–voltage (IV), capacitance–voltage (CV), reverse recovery test (RRT) and reverse breakdown measurements. The DSRD SPICE model has been successfully used to optimize DSRD-based pulser designs within LTspice simulation to achieve ~10 kV peak load voltage.

3.9.2 Objective

The main objective of this program is to optimize the DSRD device and pulser for maximum peak power while maintaining characteristic ns-order risetimes. DSRD-based pulsers are competitive with PCSS-based systems with the benefit of not requiring a laser, which reduces the cost and size of the pulser system. Other requirements are for low-jitter, cooling, and additional pulse sharpening. Using TCAD simulations, the DSRD doping profile, geometry, and lifetime killing defects can be optimized for DSRD peak performance. SPICE simulations require a DSRD SPICE model and can be used to optimize the DSRD-based pulser. The development of a DSRD SPICE model within LTspice for peak pulser performance and TCAD optimization of the DSRD doping profile is the approach for satisfying the peak power and risetime objectives. DSRD are characterized using the IV, CV, reverse recovery testing (RRT), and reverse breakdown measurements for determining key performance indicators for pulser experiments and developing fit parameters for the LTspice standard diode DSRD model.

3.9.3 Technical Background

The optimization of the DSRD, most importantly the diode geometry, doping profile, and defects, is largely based on the peak load voltage and risetime produced within a DSRD-based pulser. Also considered are the voltage riserate, pre-pulse height, diode breakdown effects, and DSRD forward and reverse pumping currents. In addition, the voltages and currents of various components (capacitors and inductors) within the DSRD pulser can also be used to assess the operation and performance of the DSRD within the pulser.

The DSRD-based pulser is less costly and more compact due to not requiring a laser but requires some additional pulse sharpening at the output to achieve sub-ns risetimes. The

cooling required for a DSRD-based pulser is comparable to other pulsed power systems. Pulse sharpening at the load can be accomplished by using either a silicon avalanche shaping diode (SAS) or a diode non-linear transmission line (DNLTL), especially when achieving higher voltage riserates possible with correctly driven stacked DSRD. Low-jitter of the system will be required to combine in the far-field when operating DSRD-based pulsers as part of an antenna array.

TCAD [4] is the only simulation method available to consider the doping profile and its effects on DSRD performance. In addition, TCAD also allows to define the diode geometry along with any defects in its simulation model. However, TCAD has one limitation in modeling heat transfer in stacked DSRD. Only unstacked DSRD can be studied for their temperature. Compared to SPICE, the device models in TCAD are much improved, but manufacturer SPICE models for devices (MOSFETS, gate drivers) cannot be included within TCAD.

SPICE is used to design and optimize DSRD-based pulsers along with theory and experiment because manufacturer device models are only available in SPICE simulators, but not in TCAD. Otherwise, device modeling in TCAD and SPICE are principally the same with SPICE models being simpler and more computationally low profile or compact. The SPICE device models are not as physically based as the TCAD models and rely on fitting experimental IV, CV, RRT, and reverse breakdown testing curves. Since DSRD is a power diode, it is modeled as a diode in SPICE. There are a number of SPICE diode models (standard, Philips, HiSIM, CMC, etc.) that share some modeling equations, but they differ in modeling details [5]. For this project, the standard diode model [2] has been chosen since it is included in almost all circuit simulators, for example in LTspice [1]. SPICE simulation allows the probing of voltages at different circuit nodes and currents through circuit elements which are not easily measurable together in experiments, and supplements what can be probed in the pulser with an oscilloscope. In SPICE, the circuit components can be swept for optimal values and device models can be altered to assess the effect on circuit-level performance as well.

The experimental IV, CV, RRT, and reverse breakdown data can be correlated to the experimental pulser results to predict and track which DSRD will perform the best in pulse testing. For example, the key performance indicators (KPI) of breakdown voltage and series resistance (as derived from the linear region of the forward IV), have been used to select best performing DSRD within the pulser.

3.9.4 Tasks, Milestones, and Status

(A) Milestone – Develop DSRD SPICE model within LTspice, fitting with IV/CV/RRT experimental tests

1. Develop accurate forward IV, reverse CV and reverse recovery testing (RRT) modeling in LTspice standard diode model; **Completed**.
2. Develop reverse IV and forward CV modeling and parameters in LTspice standard diode models; **Discontinued**.

(B) Milestone – Develop automated fitting procedures for developed LTspice DSRD models; **Completed**.
1. Improve speed/accuracy/size of brute force fitting methods for LTspice; **Completed**.
2. Python fitting tools to speed fitting; **Discontinued**.

(C) Milestone – Complete LTspice parameterization of the standard diode model for DSRD inventory (legacy, EG, Gen2); **Completed**.

(D) Milestone – Collect DSRD forward IV characterization curves for 2450 and new 371 semiconductor analyzer measurement data (forward IV and breakdown); **Completed**.

(E) Milestone – Determine optimal DSRD doping profiles for best pulser performance within TCAD; **Completed**.

3.9.5 Methods and Approach

3.9.5.1 DSRD Modeling and Circuit Simulation

For DSRD and DSRD-based circuit simulations, we used either Silvaco TCAD and the LTspice circuit simulator. TCAD allows the modeling of the most realistic semiconductor device models with some details of the device geometry, doping profile, and defects, along with modeling equations for device breakdown, carrier mobility, and carrier lifetime. SPICE device models, when available (usually from the device manufacturer), allow for fitting of experimental characterization curves and provide a reasonably accurate device model for circuit simulation. Thus, our approach has been to optimize the DSRD doping profile in TCAD, obtain the optimized DSRDs from manufacturers (collaborators), characterize them, and develop DSRD SPICE models by fitting the experimental characterization curves within LTspice. LTspice is freely available and a greater number of circuit designers can use the LTspice DSRD model when compared to commercial circuit simulators (PSPICE, HSPICE, SmartSpice, and Saber). For the DSRD SPICE model, we used the standard diode model provided within LTspice. Even though the LTspice models cannot capture all the DSRD operation (as in TCAD), the LTspice DSRD model has been used to successfully optimize the pulser designs. The SPICE models are then used for the DSRD-based pulser circuit simulation. Since much of the circuit details are captured well in LTspice simulation, along with the properly fitted standard diode model as DSRD model, qualitative details about the pulser and DSRD operation are preserved and the DSRD model is useful as a design tool.

3.9.5.2 Diode Characterization

The DSRDs were characterized as diodes using the IV, CV, RRT, and reverse breakdown measurements and then are tested in a separate DSRD-based pulser. The forward IV measurements were performed using a Keithley 2450 sourcemeter [7] in a 4-wire

measurement mode to measure high current and low resistance. However, the measurements with the Keithley 2450 were limited to 100 mA due to heating effects. To measure higher current up to 100 A, we used a Tektronik 371 curve tracer [8], which uses short pulses to reduce the temperature effects. To assist in the IV measurement, we made a custom IV fixture, which used a pressurizing screw to fasten the DSRD between copper foils in the 4-wire setup. For low current reverse IV measurement, we used a Keithley 6485 picoammeter [6], which also allowed for low reverse breakdown voltage (<200 V) measurement. For higher breakdown (up to 3000 V), we used the Tektronik 371 curve tracer, and the measurements were usually stopped at a reverse current value of 1 mA. We used an Agilent 4294A precision impedance analyzer [9] along with an Agilent16451B material test fixture to perform the forward and reverse CV measurements (up to 40 V in reverse bias). For reverse recovery testing (RRT), we used Avetech AVR-EB4-B pulse generator [10] with a diode recovery testing setup.

3.9.6 Results and Discussion

3.9.6.1 DSRD Doping Profile Optimization

We optimized the DSRD doping profile and geometry in TCAD simulation for optimal pulser performance in terms of peak load voltage and risetime. The output voltage riserate, prepulse, device breakdown, and maximum reverse DSRD current were also considered. However, we did not explicitly model or use the defects in the DSRD design. The device was modeled in 2D as a 1D device and therefore only thickness and area of the device were accounted for. Diode stacking was modeled directly by stacking the DSRD in series within the simulation (but as separate TCAD devices).

The first step in using the TCAD DSRD model is to have an accurate model. We used the Selberherr breakdown model [4] and a carrier–carrier scattering model for high-power forward-biased devices. The Selberherr model, however, does not cover dynamic breakdown, which requires very high voltage riserates (>10^{12} V/s). The Selberherr TCAD breakdown model has successfully predicted the IMPATT-style oscillations that occur on the pulse top due to breakdown. The carrier–carrier scattering model for mobility improved the simulations only slightly, while the breakdown model was critical to determining peak load voltage and risetime limitations.

The TCAD simulations are computationally expensive and only a limited number of simulations could be performed. Some earlier studies attempted to solve for the optimal stack height and area, but due to the large number of simulations, only the doping profile was optimized. Figure 1 shows a typical p-π-n DSRD doping profile [9] along with the geometric aspects of the DSRD. The doping profiles were varied in terms of maximum doping of the p- and n-sides, the minimum doping of the base, the basewidth, and the junction placement. In addition, the functional shape or gradient of the doping profile was also studied.

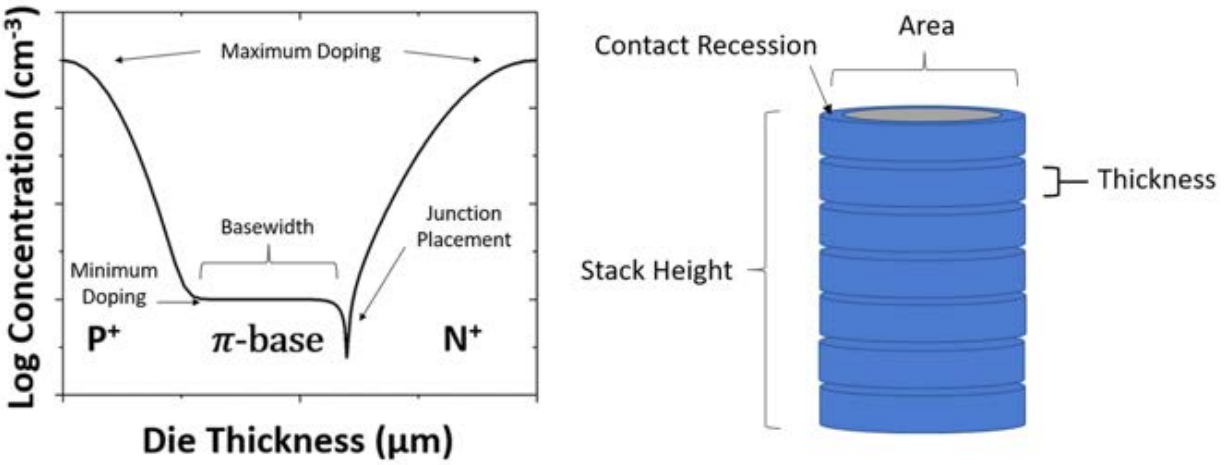


Figure 1. DSRD typical p-π-n doping profile and DSRD geometric aspects.

The first TCAD DSRD doping profile study compared doping profiles of different functional shapes: linear, exponential, gaussian and error function. Dopant diffusion creates either gaussian or error function shaped doping profiles, while epitaxy can achieve linear (or abrupt) or exponential doping profiles. In our simulation, the exponential doping profiles performed the best overall in terms of peak load voltage, risetime, voltage riserate, prepulse height and maximum DSRD reverse current and were selected for epitaxy design.

Once the doping profile was selected, the first doping parameter study varied junction placement, minimum doping and basewidth. The dependency of junction placement was not as great as initially thought and less emphasis on this was placed subsequently. However, the best junction place was at 95 µm from the N^+ edge in a 200 µm device. From the study of peak voltage vs. risetime data, we found the lowest risetime of ~1.2 ns for a doping density of 5×10^{13} dopant atoms/cm^3 and no or basewidth (Figure 2). Similarly, the highest peak voltage was obtained for a doping density of 10^{12} dopant atoms/cm^3 and a 5 µm basewidth. This showed that the basewidth should be as narrow as possible unless higher peak load voltages and longer risetimes are desirable. The peak doping can be lower than 1×10^{19} dopant atoms/cm^3 (but higher than 1×10^{18} dopant atoms/cm^3 due to ohmic contacts requirements). We found that a lower p-side than n-side is optimal. We also found that the minimum doping of the pn junction and/or basewidth should be 5×10^{13}-1×10^{14} dopant atoms/cm^3 for optimal performance for the exponential profile created with layered epitaxy.

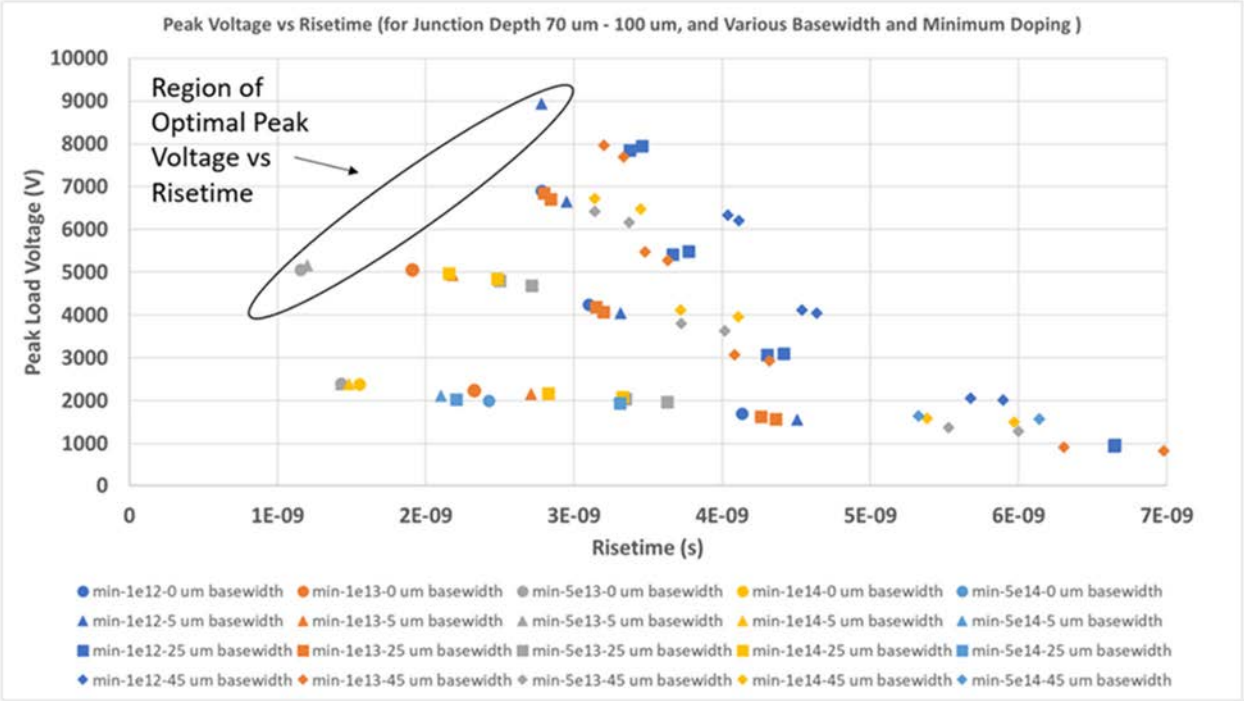


Figure 2. Peak load voltage vs risetime for TCAD simulations without breakdown. The junction placement results are only for 70 µm-100 µm. The region of optimal peak voltage and risetime is circled.

We performed a second set of TCAD doping parameter studies for two reasons. The first was that the epitaxy manufacturer had placed limits on the doping depth and doping gradient that could be manufactured and these doping profiles were now of greater interest. The second was to improve the simulation circuit used by including a voltage source and MOSFET using a voltage-controlled variable resistance switch. The DSRD device thickness was 170 µm for the second doping parameter study due to the limitations of the manufacturer. However, the second optimization study also resulted in the same doping profile even with the differences in simulation circuit and manufacturer limits on the doping profiles that can be created (see the June 2021 MSR).

3.9.6.2 DSRD Characterization

DSRDs were characterized using the IV, CV, RRT, and reverse breakdown measurements. From the forward IV measurement, the voltage drops at a current of 50 A were recorded as one of the key performance indicators because this voltage drop reduces the available prime supply voltage for the forward pumping current calculation. Similarly, the on-state resistance of the diodes were obtained by fitting the linear region of the forward IV curve, mostly above 50 A. The reverse recovery test (RRT) was not adequate in characterizing the pulser performance, because the pulsers are designed to run at much higher current and voltages and at faster switching times than in the RRT measurements. However, the RRT measurements were successful in measuring the

charge storage times under the conditions possible in the Avtech pulser. The key performance indicators (KPI) extracted from the diode characterization measurements were presented in the SEP2022 MSR. Among these, the forward voltage drop at 50 A, on-state resistance, and the breakdown voltage of the diodes were used to successfully select top performing EG-series diodes within pulser tests and helped to achieve the 9 kV-10 kV peak load voltages obtained in the pulser. In Table 1 and Table 2 are shown the best performing DSRD for the EG and Gen2 series based on breakdown voltage, forward voltage drop at 50 A and series resistance for pulser performance. The EG-series DSRD were selected and tested in the pulser and obtained the highest peak load voltage of the time at 9.2 kV. The breakdown was not reached in pulser testing and so the conductivity of the diode based on forward voltage drop and series resistance determined the best performing DSRD. Low breakdown devices were excluded from the testing by selecting the top performers as well.

Table 1. Key performance indicators of the best performing EG series DSRD.

Diode	Forward Voltage Drop at 50 A (V)	On-State Resistance (Ω)	Breakdown Voltage (V)	Reverse Current At 200 V (μA)	Zero-Bias Junction Capacitance (pF)	Reverse Capacitance At 35 V (pF)	Maximum Forward Capacitance (pF)	Maximum Forward Capacitance Voltage (V)
EG1568	14.73	0.082	3100	0.51	640.72	322.91	9769.77	3.43
EG1572	16.75	0.088	3100	0.78	641.28	314.96	39529.54	4.10
EG1573	15.38	0.090	3100	1.73	637.10	334.63	11199.25	3.43
EG1613	16.40	0.118	3100	0.78	642.75	292.28	5649.65	2.98

Table 2. Key performance indicators of the best performing SPT Gen2 series DSRD.

Diode	Forward Voltage Drop At 50 A (V)	On-State Resistance (Ω)	Breakdown Voltage (V)	Average Reverse Current At 200 V (μA)	Zero-Bias Junction Capacitance (pF)	Reverse Capacitance At 10 V (pF)	Maximum Forward Capacitance (pF)	Maximum Forward Capacitance Voltage (V)
gen2.1-d3-1	1.25	0.008	490	63.00	1426.36	561.56	5311.02	0.40
gen2.1-d4-2	1.27	0.008	567	294.45	1470.40	564.62	2707.21	0.30
gen2.1-x-1	1.23	0.007	585					
gen2.1-x-3	1.41	0.009	571					
gen2.2-d12	1.196	0.008	395	126.71	1485.72	558.86	8211.75	0.34
gen2.2-d13	1.257	0.009	552	5.28	81.73	81.68	81.74	0.45

3.9.6.3 LTspice DSRD Model

For DSRD modeling, we used the standard ‘Berkeley’ diode model [2,3] available within LTspice which improves upon simple time-dependent variable resistance models often used for modeling switches. The standard diode model has several parameters: IS, N, IKF, RS, CJO, VJ, and M [2] which are fit to the experimental data through a brute-force comparison with the simulated IV and CV curve. Here, IS is the saturation current

parameter but is not often set to the physically measurable saturation current. N is the emission coefficient where 1 is for ideal diodes and 2 is for recombination dominated diodes. IKF is the forward knee current due to high-level injection. RS is the series resistance and represents an actual series resistance within the equivalent circuit of the diode model. CJO is the zero-bias junction capacitance in the standard diode model and can be set to the experimental value. VJ is the junction potential for use in the capacitance equation and is set to the default 0.75 V. M is the grading coefficient and relates to the gradient of the doping profile. The parameters IS, N, IKF, and RS are obtained by fitting the forward IV measurement data whereas CJO, VJ, and M are obtained by fitting the reverse CV measurement data. The reverse IV and forward CV data are not often used in diode modeling because either they do not contribute significantly to diode performance or they introduce complexity and unreliability [9] in diode modeling.

The standard diode model, however, does not contain a diode recovery model, which is critically important in simulating the diode turn-off transient in DSRD-based pulser. Therefore, a transit time parameter of the forward CV model is re-assigned for recovery time modeling as is the standard engineering practice within the standard diode model. The transit time (TT) parameter is fit to the reverse recovery test (RRT) data and later adjusted to match pulser results. Apart from the parameters in the standard model, the breakdown voltage (BV) parameter is set to the experimental static breakdown voltage.

We had a large collection of DSRD. Some of been acquired through a third part manufacturer and others manufactured by Semiconductor Power Technologies (SPT). The measurements of the EG series (third-party) and Gen2 series (SPT) DSRD inventory have been fit within the LTspice standard diode model. Earlier models used the 6485 picoammeter data but later models used both the Keithley 2450 and Tektronik 371 experimental forward IV data. A large set of experimental and fit data were presented in SEPT2022 MSR.

With the diode parameters set into the standard diode model, we tested the DSRD models in a variety of circuits. These results of the DSRD parameters allowed device-specific modeling of DSRD within the pulser circuits for the optimization of both the DSRD and the pulser circuit together. Within the pulser circuit, the transit time (TT) parameter was adjusted to match either the peak load voltage or risetime since matching both was rarely possible in LTspice using the standard diode model. Generally, the behavior of the pulser circuit over trigger duration and prime voltage sweeps were not captured well in LTspice simulations. However, much of the circuit behavior was captured qualitatively and for that reason the DSRD LTspice models and pulser simulations were still useful in designing and optimizing DSRD-based pulsers for a target pulse output voltage of 10 kV. The LTspice simulations allowed probing of voltages and currents, that were not possible in experiment, and allowed easy adjustment of capacitor, inductor, and resistor values for optimal behavior even if the simulations were ‘only so accurate.’ From LTspice simulations using device-specific diode parameters, optimizations of the pulser circuit (for inductor and capacitor component values) were performed that resulted in maximum peak load voltage of 9 kV–10 kV for the first time.

3.9.7 Summary and Recommendations

The DSRD doping profile was optimized in TCAD simulation, resulting in an exponential doping profile, with no base region, junction placement in the middle of the device, maximum doping of 1×10^{19} dopant atoms/cm^3 and a minimum doping of 5×10^{13} dopant atoms/cm^3. The optimal doping profile produced the best peak load voltage, risetime, voltage riserate, lowest prepulse height and highest maximum DSRD reverse current within TCAD simulation. An LTspice DSRD SPICE model was developed from the standard diode model and fit to experimental IV, CV, and RRT curves. The DSRD SPICE model was subsequently used to optimize the DSRD-based pulser for 10 kV peak load voltage within LTspice simulation in conjunction to the working principle of the 1x1 DSRD pulser.

3.9.8 References

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3.10 Pioneering Drift-Step-Recovery Diode Processing and Manufacturing

(Alex Usenko)

3.10.1 Executive Summary

We have modernized drift-step recovery diode (DSRD) manufacturing by using state-of-the-art (SOTA) semiconductor processing techniques. We have moved beyond 60-year-old commercial processing technology to ultimately improve DSRD performance and reliability. A new process has been designed and tested that includes graded epitaxy doping, intermetallic bonding for stacking, anisotropic etch side termination, stain etch side passivation, and selective-deposition-based metallization. A Gen2 batch of DSRDs was finished and 21-die stacked devices submitted to the pulse performance testing team at UMKC, which demonstrated better performance than competitor DSRDs. A Gen3 lot is partially complete. A new process integration scheme has been developed for Gen3 DSRDs, and a patent application submitted to USPTO.

3.10.2 Objective

Primary Problem: DSRDs have not increased in performance since the 1960's due to reliance on deep diffusion manufacturing. Their voltage-to-risetime, dV/dt, remains about 10^{12} V/s. To achieve the 10^{13} V/s (10 kV/ns) voltage-to-risetime required by an all-solid-state HPM pulse generator in support of the Naval afloat mission, improving DSRD manufacturing techniques is critical.

Solution Space: Leverage applicable concepts from the mainstream silicon chipmaking industry and apply new manufacturing methods to DSRD processing.

Sub-Problem 1: Diode silicon surface termination/passivation: The SOTA uses diode termination by a vertical wall, resulting in low breakdown voltage due to limitations by surface breakdown. To increase the diode breakdown voltage to closer to that of the bulk silicon breakdown voltage value, the vertical side wall design must be avoided.

Sub-Problem 2: Stacking of DSRD dies: The SOTA is based on eutectic soldering of diode dies into a stack, which limits the stack lifetime to below 10^{12} pulses. Also, the SOTA did not apply the methodology of stacking wafers first, then cutting into dies. Switching to wafer level stacking will decrease the number of stacking operations by more than 100x.

Sub-Problem 3: Packaging of stacked dies: The SOTA uses bare stacked DSRDs. Mounting the bare stack into a press-pack, stud or power module type package will improve long-term stability, such that the stack will survive a much higher number of pulses before it burns out.

3.10.3 Technical Background

State-of-the-Art (SOTA): In a recently published paper (2022),[1] the Russian St. Petersburg team at the Ioffe institute reported achieving a peak current density of 5 kA/cm^2 with a rise time of the output pulse front of ~2.3 ns, and a peak voltage across the load of 900 V (i.e., the peak switching power is 4.5×10^6 W/cm^2). The St. Petersburg

team utilized deep diffusion technology. A competing team at Ekaterinburg, Russia,[2] reports similar pulse performance. Both teams use outdated deep diffusion technology. As one can see, there has not been any significant improvement in DSRD pulse performance since the pioneering work done in 1960.[3]

Deficiency in the SOTA: First, no DSRDs have been manufactured using epitaxy technology with doping profile optimization. Second, no DSRD processing method exists that integrates side passivation with silicon dioxide. Finally, an acceptable DSRD stacking process has yet to be developed.

Solution Proposed: Manufacture DSRDs within the continental United States using an epitaxial growth process leveraging the optimal characteristics (e.g., doping profile, carrier concentration) determined through the work performed by our simulation sub-team and through working with industry partners at Semiconductor Power Technologies (SPT), Livermore Semiconductor Research Laboratories (LSRL), and Lawrence Livermore National Laboratory (LLNL – Voss Group).

Relevance to OSPRES Grant Objective: DSRD manufacturing technology is a major building block of short-pulse high-peak-power defense systems. Our new disruptive process flow for DSRDs enables not only manufacturing of DSRDs at scale, but within the continental United States (CONUS). In doing so we will redefine the SOTA by producing optimal DSRDs. DSRDs will be used within best-in-class HPM pulse generators as part of more advanced defense systems within the Navy arsenal.

Risks: As the process of producing DSRDs using epitaxial growth with doping profile design is novel, uncharted territory, there is inherent risk to its success. Additionally, post-processing methods based on the discussions provided in the ***Sub-Problems*** section are not well-established.

Payoffs: Replacing traditional deep diffusion technology with a new process integration scheme would allow better DSRD pulse performance. Electrical breakdown voltage is expected to increase, rise time on a load is expected to decrease, reliability and service time are also expected to increase.

3.10.4 Tasks, Milestones, and Status

(A) Milestone – Produce epitaxial DSRDs that contain optimal exponential doping profiles and carrier concentrations.

1. Task – Design of experiment on 25 wafers through negotiations with vendors / *MAY–JUL21* / Completed.
2. Task – Perform DSRD stack epitaxy on 13 wafers at SVM Inc., and 25 wafers at LSRL / *JUN–AUG21* / Completed.
3. Develop process integration scheme that uses epitaxy instead of deep diffusion / *JUL–OCT21* / Completed.
4. Compare traditional DSRD technology and suggested integration scheme. List disadvantages of traditional processes and define potential advantages of new processes / MAY–NOV21 / Completed.

5. Run Gen2 and Gen3 lots. Gen2 is on wafers with epi from SVM, Inc., Gen3 is on wafers with epi from LSRL. Gen2 uses the same BEOL as Gen1. Run BEOL of Gen3 – using our new patented processing scheme – Si_3N_4 masking, TMAH etch, oxidation, selective electroless metal deposition, wafer bonding, sawing into diode stacks / Completed.

(B) Milestone – Develop diode separation technique while keeping wafer integrity.

1. Design lithography masks for short loop experiment, submit order to vendor. / MAR–APR21 / Completed.
2. Design short loop experiment for V-groove etching for diode separation. / MAR–APR21 / Completed.
3. Run short loop experiment for the diode separation by anisotropic etch; analyze results / MAY–OCT21 / Completed.
4. Based on results of previous short loop run, adjust equipment, and process recipes to achieve sufficient etch uniformity across the wafer. Run on updated equipment and recipe to prove etch uniformity. / Completed.
5. Design lithography masks for epi DSRD run; submit order to vendor. / Completed.
6. Run Gen3 lot through V-groove etch step, transfer lot to next process step. / Completed.

(C) Develop Ohmic contact deposition technique integrable with epitaxy, diode side termination/passivation, and wafer bonding steps.

1. Design short loop experiment to determine technical feasibility of selective electroless deposition of metal stack as a method of Ohmic contact forming in the DSRD process integration scheme. / OCT21 / Completed.
2. Determine vendor from which to order electroless deposition kits; obtain quotes, order, receive the kits. / OCT21 / Completed.
3. Run short loop experiment – nickel-copper-tin stack electroless deposition on a blanket wafer. Analyze results. / DEC21 / Completed.
4. Develop process recipe for the metal stack deposition to use in Gen3 DSRD lot manufacturing / Completed.
5. Run the selective metallization step on Gen3 lot; transfer the lot to next processing step. / Completed.

(D) Develop wafer stack bonding technique integrable with the rest of Gen3 process flow.

1. Design short loop experiment for bonding 2 blanket wafers with Ni-Cu-Sn layers by solid–liquid interdiffusion. / SEP21 / Completed.
2. Run 2-wafers short loop experiment. Analyze results. / Completed.
3. Test technical feasibility of multiple wafer bonding by bonding 10-wafer stack / Completed.
4. Upon proof of technical feasibility of 10-wafer stacking, develop process recipe to use for processing of Gen3 DSRD lot / Completed.

5. Run wafer bonding step on Gen3 lot, transfer the lot to next processing step. / Completed.

(E) Develop wafer stack sawing technique into DSRD stacks, integrable with the rest of Gen3 process flow / Completed.

1. Design sawing process using Disco saw available at Semiconductor Power Technologies for cutting 10-wafer stack / Completed.
2. Develop process recipe for Disco saw tool to use for Gen3 lot. / Completed.

(F) Develop diode side passivation process integrable with the rest of DSRD process flow.

1. Test compatibility of thermal oxidation for the diode side passivation with preceding anisotropic etch step / Completed.
2. Alternative diode side passivation process: design short loop experiment on room temperature oxidation by forming porous Si film and oxidizing the porous film / APR–OCT21 / Completed
3. Run part of Gen3 lot using the oxidized porous Si as diode side passivation / Completed.
4. Run part of Gen3 lot using the oxidized porous Si as diode side passivation / Completed.

(G) Develop a DSRD process based on out-diffusion (opposite to traditional in-diffusion process).

3.10.5 Approach

Silicon power devices such as diodes, MOSFETs, and IGBTs currently account for roughly 90% of the entire power device market, leaving only 10% to wide band gap (WBG) semiconductors including silicon carbide and gallium nitride. While nearly all research and development activities are concentrated on the WBG semiconductors, the lack of R&D in silicon power devices has left them nearly unchanged for the past 20 years. This is especially true for pulsed Si devices, which still rely on 60-year-old technology. Meanwhile, mainstream silicon integrated circuit technology has progressed dramatically in the last two decades, with feature sizes shrinking from submicron to 3 nm. Over the course of this project, we have shown promising examples of applying new technologies, initially developed in mainstream silicon technology, MEMS, photonics, and 3D packaging, to silicon power device technology. This will keep silicon devices, including pulsed power ones, as strong competitors to the WBG devices for many years to come.

3.10.6 Results and Discussion

A new process flow for manufacturing DSRDs has been developed. Two patent applications [1], [2] have been filed with USPTO to establish our intellectual property on this new integration scheme. A simplified process flow schematic is shown in Figure 1.

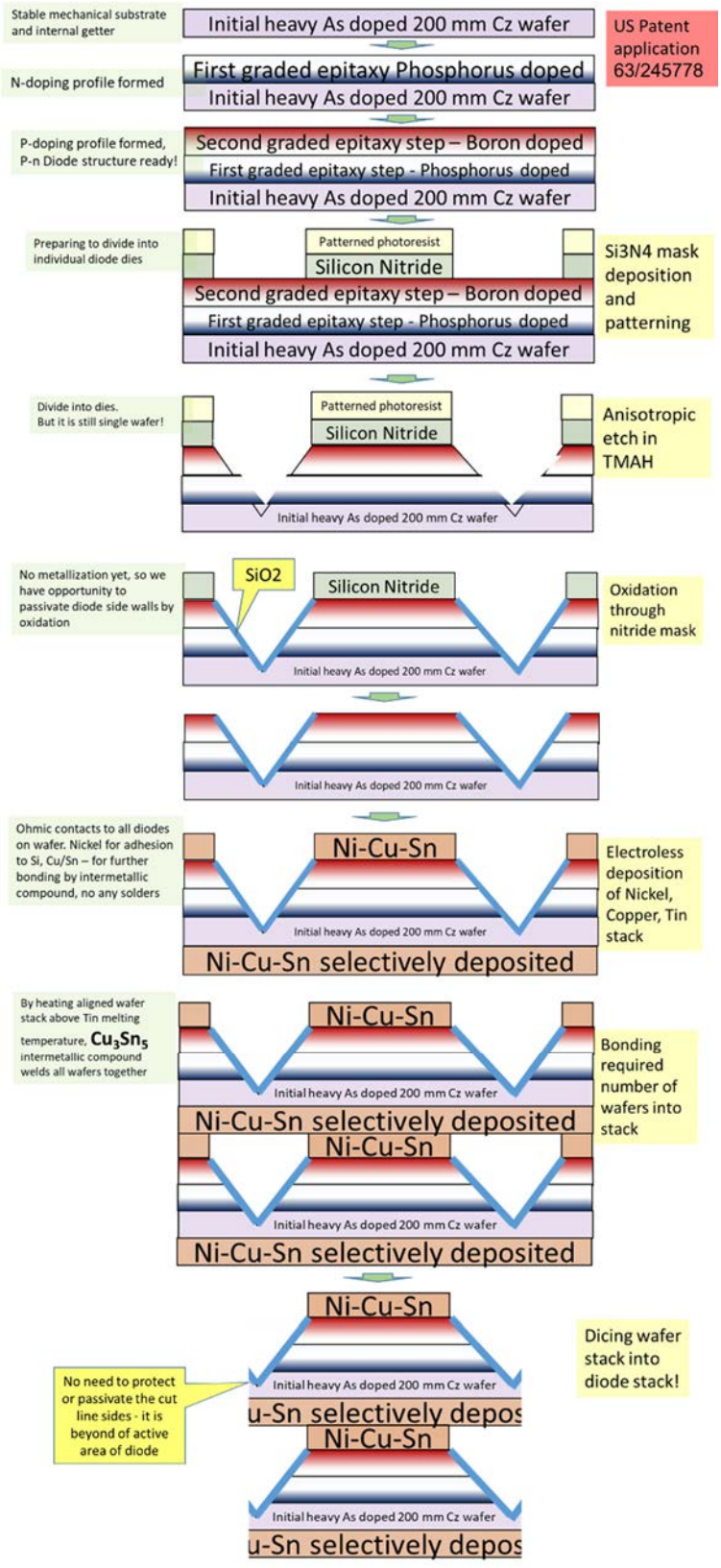


Figure 1. Schematic DSRD process flow.

Individual process steps of the flow have been developed. Results for several of these steps have been presented at conferences: on diode side passivation step [3], on selective metal deposition for device contacts [4], on graded epitaxy [5], on die singulation by anisotropic etching [6], on wafer level stacking [7], on diode passivation by porous Si obtained by stain etch [8].

[1] S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same,” *US Patent Application 17/855735* filed 06/30/2022.

[2] S. Bellinger, A. Caruso, A. Usenko, “Stacked Diode with Side Passivation and Method of Making the Same,” *US Patent Application 17/946022* filed 09/15/2022.

[3] A. Usenko, A. Caruso, S. Bellinger, S. Dhungana, R. Allen, “Improved Manufacturing Process for High Voltage Pulse Diodes,” *Proceedings of The IEEE International Power Modulator and High Voltage Conference*, Knoxville, TN, June 19-23, 2022.

[4] A. Usenko, S. Dhungana, A. N. Caruso and S. L. Bellinger, “Electroless Nickel Plating for Ohmic Contacts to Silicon Power Devices,” *Abstracts of 242nd Electrochemical Society Meeting*, Atlanta, GA, October 9-13, 2022 [doi].

[5] A. Usenko, A. Caruso, S. Bellinger, S. Dhungana, R. Allen, “Adopting Processes from Mainstream Silicon Technology to Discrete Power Devices Technology,” *2nd Annual Workshop on Solid State Devices and Applications for Directed Energy at GE Research* in Niskayuna, NY, October 26-28, 2022.

[6] S. Bellinger, A. Caruso, A. Usenko, “New Paradigm on Making Semiconductor Opening Switches for Pulsed Power,” *oral presentation at the 2021 23th IEEE Pulsed Power Conference*, Denver, CO, December 12-16, 2021.

[7] S. Bellinger, A. Caruso, A. Usenko, “Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme,” *oral (online) presentation at the 240th Electrochemical Society Meeting*, Orlando, FL, October 10-14, 2021 [doi].

[8] A. Usenko, J. Eifler, S. Roy, G. Bhattarai, M. Hyde, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “New Paradigm in Fabrication of Semiconductor Opening Switches for Pulsed Power,” *Directed Energy Systems Symposium*, Washington, DC, October 25-29 2021.

3.10.7 Summary and Recommendations

DSRDs are the major components required for high power microwave (HPM) based defense system for the counter unmanned aerial system (cUAS) OSPRES mission. Toward this goal, we have developed a novel process flow and have manufactured DSRDs that exceeded the existing performance of devices of this type. We recognized that other teams in the US and other countries that develop DSRDs are either using 60-year-old technology or using new materials with immature technology. The 60-year-old technology—deep diffusion into thinned silicon wafers—has already exhausted all performance improvement options. An example of an immature technology is making DSRDs on diamond—lab scale devices have been demonstrated, but it will take too long to develop a process for volume scale manufacturing. We use mature silicon technology, but have replaced almost all process steps by newer more advanced processes: for the doping step we have replaced deep diffusion by graded epitaxy; for wafer separation into dies we have replaced mechanical sawing by anisotropic etch; for device edge

passivation we have replaced the polyimide coating by growing porous a silicon layer; for forming Ohmic contacts we have replaced blanket metal deposition by selective electroless plating; and for the stacking step we have replaced solder bonding by solid-liquid interdiffusion bonding.

We have also experimentally proven that each of the new process steps we have chosen for our DSRD process integration scheme works toward improvement of pulsed performance of the final DSRD devices.

As the major goal of this OSPRES sub-project, developing a new disruptive manufacturing process for DSRDs, has been successfully achieved, project termination is reasonable. However, our efforts open a wide range of possibilities for further improvements, including the optimization of each individual new process step, toward improving the pulsed performance of DSRD devices.

3.10.8 Outputs

Patent applications and conference publications and presentations are listed as references [1] – [8] in the Results and Discussion section.

3.10.9 References

[1] Lyublinsky, A.G., Kardo-Sysoev, A.F., Cherenev, M.N. and Vexler, M.I., 2022. Influence of DSRD Operation Cycle on the Output Pulse Parameters. *IEEE Transactions on Power Electronics*, 37(6), pp.6271-6274.

[2] Rukin, S. N. "Pulsed power technology based on semiconductor opening switches: A review." *Review of Scientific Instruments* 91, no. 1 (2020): 011501

[3] Boff, A., J. Moll, and R. Shen. "A new high-speed effect in solid-state diodes." in *1960 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, vol. 3, pp. 50-51. IEEE, 1960.

3.11 DSRD-Based Sub-Nanosecond Pulse Power Source Optimization

(Gyanendra Bhattarai)

3.11.1 Executive Summary

This sub-project started with an objective of developing an ultra-compact (≤1L ≤5 lbs.) solid-state pulse generator for high-power microwave (HPM) generation using drift-step-recovery-diodes (DSRD) capable of producing ≥10 kV peak output voltage across a 50 Ω load with a risetime of ≤1 ns and a pulse repetition frequency (PRF) of ≥1 kHz using ≤200V prime power. DSRDs are not available to purchase within the United States. Thus, we collaborated with diode manufacturers to manufacture DSRDs by providing them with optimum diode doping profiles. For those diodes, we developed SPICE models for circuit simulation using TCAD and LT-Spice. To obtain a maximum output voltage using minimum prime power, we developed a physics-based circuit working principle and used it to design a systematic optimization scheme for the pulser circuit. Using the optimization, we were able to demonstrate 4.6 kV output voltage using a 7-stack DSRD diode and 120 V prime supply from a single stack DSRD pulser driven by a single MOSFET. To achieve 10 kV output voltage, we developed a MOSFET module containing four MOSFETs in parallel and a MOSFET driver circuit that enabled pumping ~2 kA of current through the MOSFET module. Using the MOSFET module, we were able to achieve a maximum peak voltage of 9.2 kV with a 20–90% risetime of 5 ns using a prime source of 140 V from a pulser containing 21 diodes. Increasing the output voltage further was not possible due to the MOSFET's open-circuit voltage limit of 1500 V. However, with the availability of higher-voltage MOSFETs or by stacking multiple MOSFETs in series and in parallel, even higher voltage can be obtained from a single-stage pulser containing an increasing number of diodes in series. We also identified that the output voltage can be increased by stacking single stack pulsers in parallel. Although we were close to our target on output voltage, we could not achieve the pulse risetime, which is mainly a function of DSRD recovery rate, with improved shorter recovery diodes required. PRF and efficiency studies of the best pulser were not completed due to time limitations, and these tasks were transitioned to the PTERA program.

3.11.2 Objective

Inductive energy storage (IES) and release pulse generators utilizing the ultra-short turn-off transients of drift-step-recovery diodes (DSRDs) are now considered among some of the strongest contenders for ultra-portable all-solid-state high-power microwave (HPM) systems. Their high-voltage output can be fed into sub-nanosecond solid-state pulse sharpeners (SAS, D-NLTL, etc.) to achieve ultra-short high-voltage (100's of kV) pulses and can remove the need for photo-triggered switches and their laser sub-systems, reducing overall cost, volume, and weight and rendering them suitable for Navy afloat missions.

While DSRD-based pulsers can theoretically achieve the targeted 1's of GW in 1's of ns, their circuits are not topologically optimized to achieve high voltage gain (peak pulse

voltage/prime source voltage), thus requiring large and heavy, high-voltage (multiple kV) prime power supplies to achieve the target output. They also require liquid-based cooling systems to dissipate the excess heat they generate during operation, which further adds weight and volume. Available literature on IES pulse generators[1]–[3] only describes a few circuit configurations, and there is a lack of comprehensive investigation of circuit topologies and optimization to achieve maximum gain and efficiency and reduce thermal load. Currently available air-cooled DSRD-based pulsers[4] under ~0.01-m^3 and ~2-kg are limited to <20 kV, 1–2 ns risetime, and <4 ns FWHM across a 50 Ω load with a PRF of <15 kHz in burst mode. Additionally, these pulsers are expensive and are not available within the United States.

DSRDs are not available domestically yet as COTS components, but rather manufactured in small-batch quantities, with statistically significant variations in their performance parameters. In addition, standard SPICE models for these devices are not available and custom-developed SPICE models of these diodes may not be accurate enough to simulate realistic circuits due to unknown device properties and limitations such as carrier distribution, carrier lifetime, breakdown field, and maximum safe current during high-voltage transients. In this context, the objective of this research work is to systematically develop optimum circuit topology to maximize the peak output voltage, peak power, and volumetric power density of DSRD-based HPM systems, to minimize the heat loss to be able to air cool by increasing energy efficiency through optimization of circuit elements without sacrificing the desired nanosecond risetime of the pulses generated, and to fabricate pulse generators with output reaching or exceeding current state-of-the-art portable sources. Additionally, the objective of the study is to provide necessary feedback to the US-based diode manufacturers to develop next-gen diode manufacturing technologies based on physics-based circuit theory, simulation, and experimental results.

3.11.3 Technical Background

Inductive energy storage (IES) and release systems have been used in very-high voltage production for a long time [ref]. In such systems, a large amount of energy is stored in an inductor during a short period of large current and then the current path is abruptly broken, establishing a very large voltage across the inductor

$$V_L = -L\frac{dI}{dt} \tag{1}$$

Historically, switches like exploding wires were used to achieve the short turn off transients (large dI/dt). However, an exploding wire is limited to single pulse generation because of the need to replace it and high pulse repetition frequency (PRF) is impossible. The invention of the drift-step-recovery-diode (DSRD)—a semiconductor opening switch (SOS)—in 1981 opened a new era of DSRD-based IES pulse generators; however, DSRD manufacturing capability remained within Russia for a long time. Even today, DSRDs are not available to purchase within the United States as COTS devices, and thus the research and development of DSRD-based high-voltage pulse generators is still in an early stage. There is limited literature available aimed at pulser circuit design, and that

which is available does not provide enough information on the circuit operation physics, which is critical for exploiting diode characteristics to achieve the maximum voltage and power output from the pulse generators.

The most advanced DSRD-IES pulse generators are still located within Russia, and pulsers capable of producing 400 kV pulse amplitudes across a 100 Ω load with a PRF of up to 4 MHz have been developed by IOFFE in Russia[5]; however, these are very large in size and weight (≥1-m^3, ≥300-kg) due to their large prime power supplies and cooling requirements. Small and light-weight sub-nanosecond pulse generators (~0.01-m^3, ~2-kg), which are available to purchase from MegaImpulse, however, are only able to achieve <7-kV across a 50 Ω load and are very expensive.

3.11.3.1 DSRD-Based IES Pulser: Working Principle

A DSRD is simply a diode which allows a large forward current through it with very small ON-state resistance but acts as an insulator in the reverse direction, however, with a distinct feature that when it is reverse biased immediately after a short period of forward current, it conducts for a short time in the reverse direction and turns off very sharply, thus acting as an ultra-fast opening switch, as shown in Figure 1. This ultra-fast recovery is due to the extraction of injected free charge carriers, and this recovery feature can be used to produce ultra-short high-voltage pulses using an inductive energy storage and release system (IESR).

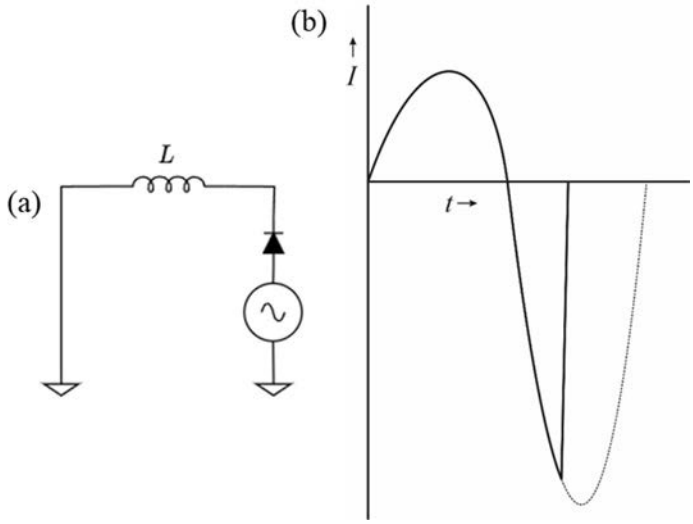


Figure 1. (a) A DSRD in series with an inductor and an asymmetric oscillating biasing source, and (b) the expected current characteristics through the DSRD. The dotted curve represents current profile in absence of the DSRD.

When a DSRD connected in series with an inductor [Figure 1(a)] is forward biased for a short period of time and is reversed biased immediately, the diode conducts for a short period of time and achieves a peak reverse current $I_{0,\mathrm{rev}}$. As the diode snaps sharply causing a rapid drop in current, a large voltage is developed across the inductor. If a load

resistor (R) is connected in parallel to the DSRD, the energy stored in the inductor during the reverse current is transferred to the load. In an ideal case with infinitesimal recovery time ($dI/dt \rightarrow \infty$), the voltage across the load is given by

$$V_{out} = I_{0,\mathrm{rev}} R \tag{2}$$

where $I_{0,\mathrm{rev}}$ is the magnitude of the peak reverse current through the DSRD [Figure 1(b)]. However, in a real case with finite recovery time (finite dI/dt), the output voltage is given by Equation (1). Equation (2) shows that, to achieve >20 kV output across a 50 Ω load, a peak reverse current of >400 A is required with ideal recovery ($dI/dt \rightarrow \infty$). For real DSRDs, a larger current is required as a significant fraction of energy is dissipated in the diode as heat during the finite time of current cut-off. Thus, it is critical to achieve as much large reverse current as possible to increase the output voltage, which is the main goal in DSRD-based pulser design.

Within the linear charge transport regime, the reverse current (or the carrier extraction current) in the DSRD depends on the applied reverse bias (V), the amount of available free charge (Q) in the diode, and the thickness (d) of the active region of the diode given as

$$I_{0,\mathrm{rev}} = Q \frac{\mu V}{d^2} \tag{3}$$

From which, we see that the reverse peak current in a DSRD can be increased by increasing the injected charge and the applied reverse bias. For a DSRD, the amount of free charge available for extraction during the reverse biasing depends on the amount of charge injected into the diode during forward pumping and can be written as

$$Q = \int_0^{T_{\mathrm{pump}}} I_F(t)\, dt \tag{4}$$

Here, we assume that the effect of carrier recombination is negligible as carrier lifetime in DSRDs is very long compared to the forward pumping time T_{pump}. Due to the finite ON-state resistance (R_s) of the diode/diode stack, the maximum forward current is limited by the forward voltage as

$$I_{\mathrm{F,MAX}} = \frac{V_{\mathrm{forward}}}{R_s} \tag{5}$$

Because of limitations in pumping time and prime source voltage, the only way to increase the peak reverse current is to design a circuit which generates a short forward pulse followed by a large reverse bias, however, using a minimum prime supply voltage to achieve a target form factor.

3.11.3.2 Solution Space

We know now that the DSRD pulser design should be aimed to increase the forward and reverse pumping current to increase the output voltage. However, it is equally important to design a circuit that results in the shortest possible pulse risetime, which is a

complicated function of diode recovery time, circuit inductance, and capacitance. At the diode level, the forward current can be increased by lowering the ON-state resistance (using optimum doping profile, larger cross-section area, conductive bonding for diode stacking etc.) and the reverse breakdown voltage can be increased by using advanced diode manufacturing process. Similarly, the pulse risetime, which is controlled by the diode recovery time, can also be reduced by using an optimum DSRD doping profile, which requires a comprehensive research effort as well. At the circuit level, output voltage and pulse width can be tuned by a systematic analysis of the pulser circuit using increasing number of diodes in series (for higher breakdown voltage), number of parallel branches of diode stacks (for larger diode current), and optimization of the other circuit elements. Thus, we proposed to tackle the problem using the following approaches:

A. Develop and optimize DSRD doping profile for larger current, higher breakdown voltage, and shortest diode recovery time and coordinate with diode manufacturer.
B. Characterize the DSRD diodes using standard diode characterization techniques such as current–voltage, capacitance–voltage, and reverse recovery measurements, as well as pulser performance.
C. Develop SPICE models for the diodes to use in pulser simulations.
D. Design pulser circuits, develop circuit theory, perform simulation, and optimize the circuit elements using developed circuit theory and coordinate with diode manufacturer for diode requirements.
E. Design pulser circuit board within the volume and weight limitation, select and/or fabricate components, and perform diode testing to demonstrate target performance.

The first three tasks are covered in detail in Drift-Step Recovery Diode Testing, Simulation, and Optimization Summary Report. Here, we will only describe the remaining last two tasks.

3.11.3.3 Proposed Solution: MOSFET-Driven DSRD-based Pulse Generator

As we are working on an all-solid-state solution for a DSRD-based pulser, our simple pulser circuit consists of two MOSFET-driven LC oscillating circuit loops for both forward and reverse pumping stages of the pulser. While forward pumping is easily achieved by simply discharging a capacitor through the diode and inductor, obtaining a large reverse voltage ($\gg V_{prime}$) immediately after the forward pumping is critical to achieve a large peak reverse current and short diode turn-off time. The simplest solution to achieve a large reverse voltage is to use the fast turn-off transient of the MOSFET, which induces a large voltage across another inductor, and feed that voltage for reverse pumping. A simplified circuit diagram of the proposed circuit is shown in Figure 2. However, we also plan to study different circuit topologies to achieve similar circuit action and select the best one based on obtained performance.

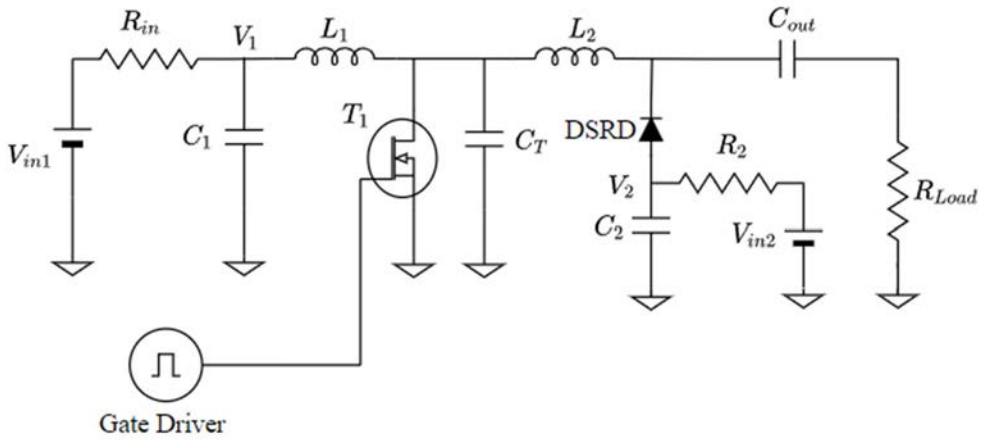


Figure 2. A schematic of a MOSFET-driven DSRD-based pulsed power circuit.

In the circuit, the forward pumping is achieved by turning the MOSFET (T_1) on so that the capacitor C_2 discharges through the inductor L_2 to ground. At the same time, the capacitor C_1 discharges through the inductor L_1 to ground establishing a large current. When the MOSFET is turned off, a large voltage is developed across the MOSFET, which then reverse biases the DSRD and sets up a large reverse current and drives the DSRD to snap OFF, eventually producing a large output voltage across the load. The challenges to fabricate an optimized pulser are then:

a. Optimizing the forward pumping time and MOSFET turn-on time.
b. Optimizing the inductors and capacitors to achieve the maximum possible reverse bias voltage, which is limited by the safe open-circuit voltage of the MOSFET.
c. Optimizing the number of diodes in a stack and the number of such diode stacks in parallel to increase both the reverse breakdown voltage and forward pumping current.
d. Selecting MOSFETs with large short-circuit current, large open-circuit voltage and optimum turn-off time, stacking them to increase current, and developing MOSFET driver circuit.

In this project, we propose to solve these problems by developing a physics-based circuit theory for the pulser, optimizing the circuit elements using theory, and further optimizing the circuit using SPICE simulation using the diode models developed from their experimental characterization. Further, we will develop theory for series and parallel stacking of pulsers to see if the output voltage can be increased further beyond that which is achievable by a single stack pulser.

3.11.4 Tasks, Milestones, and Status

To address the primary problem and achieve the solution proposed, two major efforts for this work are distinguished: (1) Develop a physics-based working principle (circuit theory) for the proposed pulser circuit and develop a circuit optimization algorithm using SPICE simulation, and (2) fabricate and test a pulser circuit using multiple combination of diodes

and iterate through multiple inductor and capacitor combination (beyond the optimized values from the simulation).

Milestones for the first effort, and tasks to achieve them along with a timeline to do so, are as follows:

(A) Milestone – Develop working principle / circuit theory of DSRD pulse generator to facilitate optimization of 1×1 pulse generator [***Completed JAN22***]

(B) Milestone – Develop circuit optimization algorithm based on the theory developed on Milestone (A) [***Completed JAN22***]

(C) Milestone – Extend the theory developed in Milestone A to facilitate optimization of M×N pulse generator [***Partially completed, Transitioned to PTERA***].

Milestones for the second effort, and tasks to achieve them along with a timeline to do so, are as follows:

(D) Milestone – Construct/demonstrate a single stage pulse generator prototype capable of producing ≥ 5-kV peak voltage, with nanosecond risetime based on the theory developed [***Completed FEB 22***].

1. Task – Develop the pulser circuit to include electrically optimal (not mechanical) layout considerations and components within Altium [***Completed DEC21***];
2. Task – Simulate and optimize the pulser circuit based on the developed theory and optimization algorithm [***Completed FEB22***];
3. Task – Fabricate/populate the pulser circuit board and evaluate single-pulse performance output in terms of peak voltage amplitude, risetime, and FWHM [***Completed FEB22***];
4. Task – Process and analyze waveform data acquired, compare to LTSPICE simulations, and provide results to TCAD simulation team [***Completed FEB22***].

(E) Milestone – Construct/demonstrate a single-stage/multi-stage pulse generator prototype capable of producing ≥10-kV peak voltage, ≥2-MW peak-power, [***Completed SEPT22***].

1. Task – Work with TCAD simulation team (see Section 3.6) and diode manufacturing team to revise/update diode manufacturing and stacking process for improving diode properties required for target output voltage [***Completed APR22***];
2. Task – Simulate and optimize the pulser circuit with increased number of MOSFETs and diodes (in series) to increase the MOSFET current and to achieve >10 kV output voltage, [***Completed APR22***];
3. Task – Design, fabricate, and evaluate the performance of a parallel combination of MOSFETs to increase current handling capability [***Completed JUL22***]

4. Task – Fabricate/populate the pulser circuit board and evaluate single-pulse performance output in terms of peak voltage amplitude, risetime, and FWHM [***Completed JUL22***]
5. Task – Perform PRF study, ranging from 100-Hz to 100-kHz, to evaluate the PRF handling capabilities of the pulse generator and standard deviation of the pulse output [***Transitioned to PTERA***];

(F) Milestone – Construct/demonstrate a M×N SOS pulse generator prototype capable of producing $\geq$20-kV peak voltage, $\leq$1-ns risetime, $\leq$2-ns FWHM, $\geq$8-MW peak-power, $\geq$1-kHz PRF, and $\geq 2\sigma_{V_{peak}}$, which operates in continuous-burst mode as a viable candidate for OSPRES contract source alternative [***Transitioned to PTERA***].

3.11.5 Methods and Approach

Theory, simulation, and optimization: To tackle the problem effectively, we first had to develop the working theory of the pulser circuit and verify this through simulation. For circuit simulation, we used LT-Spice simulation software and custom-developed SPICE models for DSRDs based on their in-house characterization. We developed an optimization algorithm based on the working theory that systematically varied the circuit parameters (inductances, capacitances, pumping time, and trigger length) to obtain the highest possible output voltage using the smallest possible prime supply voltage.

Circuit design and fabrication: We used Altium for the pulser circuit board design to minimize the overall volume while maintaining enough space for air cooling. The designed circuit boards were then ordered. The circuit elements were populated in our lab using reflow oven and hand soldering.

Inductor construction and characterization: To fabricate inductors of desired inductance, we used an open-source application, Coil64[6], which gives the inductance, series resistance, self-capacitance, and self-resonance frequency of an inductor. We also developed a Python script to calculate the inductance of the inductors based on their geometries. We used an Agilent 4294A impedance analyzer to characterize the inductors using impedance analysis.

Pulser Testing: We tested the pulser circuit performance in our high-voltage laboratory, which is equipped with all required instrumentation. We used a Keysight 2450 sourcemeter as a prime source supply, Keysight 33509B TrueForm waveform generator for input trigger, a Tektronix MSO64 Series 6 25Gs/sec 4-GHz oscilloscope to measure the output waveform, high-voltage probes for measuring high voltage outputs (such as MOSFET voltage), and Bart attenuators to attenuate the pulser output voltage before feeding it into the oscilloscope input terminal.

3.11.6 Results and Discussion

3.11.6.1 Theory Development, Simulation, and Circuit Optimization

A simplified theory of operation for the proposed DSRD-based pulser circuit has been developed and was presented in the DEC21 MSR. From the theory, we were able to

approximate the optimum range of the trigger length ($\pi\sqrt{L_2C_2} \leq T_{\mathrm{ON}} \leq 1.5\pi\sqrt{L_2C_2}$), which helped to reduce the simulation time significantly to obtain the optimum circuit components and trigger length. We were also able to approximate the minimum value of L_1C_1 product ($L_1C_1 \geq 4T_{\mathrm{ON}}^2$) to obtain the maximum possible reverse voltage for a set value of prime voltage that is required for increasing the peak extraction (reverse) current. Although the theory could be used to optimize the circuit components for the ideal case, because of the limitations imposed by the MOSFET and DSRD breakdown voltage, we needed to develop an optimization scheme to be used within LT-Spice simulations. We developed a complete circuit optimization algorithm, which maximizes the output voltage with minimum prime supply voltage possible. This is achieved by setting a small injected charge (Q_{inj}) and a short pumping time (t_{pump}). Once these are defined, we set other circuit parameters as

$$L_2 = 2\frac{V_{\mathrm{in2}}}{Q_{\mathrm{inj}}}\left(\frac{t_{\mathrm{pump}}}{\pi}\right)^2; \qquad C_2 = \frac{Q_{\mathrm{inj}}}{2\,V_{\mathrm{in2}}} \tag{6}$$

As we already mentioned that C_1 can be chosen to be any large value, the only unknown circuit elements are then inductor L_1 and the trigger length T_{ON}. The optimization is then obtained by iterating the simulation for different values of L_1 and trigger length and repeating the same procedure by increasing the injected charge until the target output is achieved. Although, the iterative process is still long, the working theory reduced the simulation time significantly by reducing the optimization parameters.

3.11.6.2 MOSFET Stacking and Driver Circuit

We observed from our simulation optimization that the MOSFET current required for pulser circuits optimized for >5 kV is quite high (>400 A), for which a single MOSFET is not able to provide the necessary currents due to their limitations. Thus, it was essential to develop MOSFET modules with several MOSFETs in parallel to increase the current handling capability. However, with parallel MOSFETs, we faced frequent driver IC burnout. Thus, we designed a modular MOSFET driver circuit with a totem-pole BJT pair, as shown in Figure 3. The designed driver circuit is now able to handle a maximum current of 2 kA. The detail of the circuit and design has been reported in the APR22 MSR.

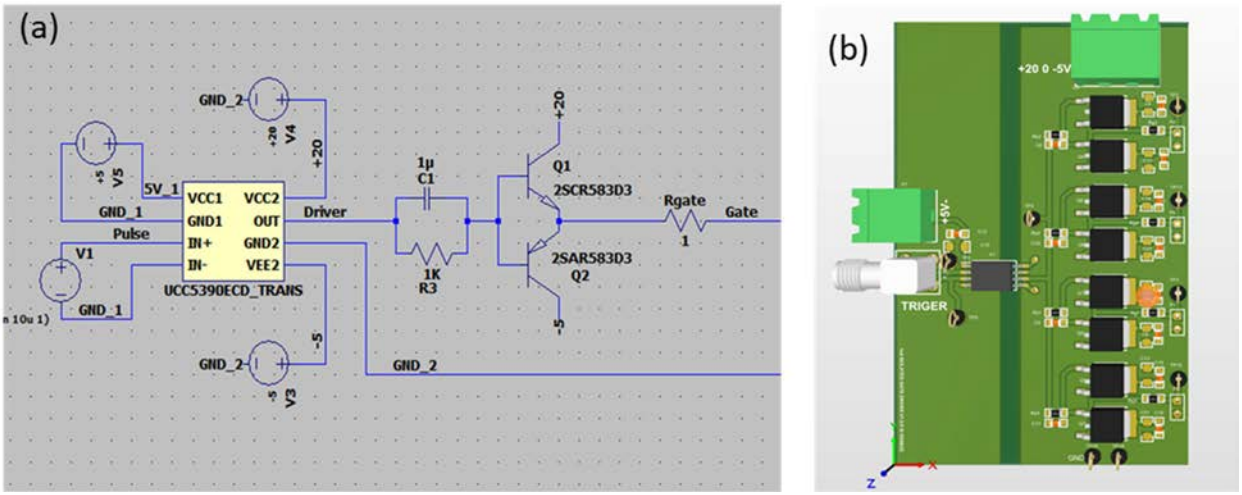


Figure 3. (a) A modular gate driver circuit schematic and (b) the designed PCB layout of the circuit.

3.11.6.3 Pulser Performance Testing

To test the validity of the working principle we developed, we optimized a single-stage pulser using four 7-stack diodes from the EG series for a target output voltage of 14 kV, and we obtained the following circuit components.

$$V_{\text{in1}} = V_{\text{in2}} = 120\ \text{V},\ R_{\text{in}} = 100\ \Omega,\ L_1 = 265\ \text{nH},\ C_1 = 45\ \mu\text{F},\ L_2 = 330\ \text{nH}$$

$$C_2 = 250\ \text{nF},\ C_{\text{s}} = 15\ \text{nF},\ C_{\text{out}} = 15\ \text{nF},\ R_2 = 1.2\ \text{k}\Omega,\ T_{\text{ON}} = 1.1\ \mu\text{s}$$

We populated the pulser circuit and tested its performance for a different combination of the diodes. A summary of the outputs obtained using different EG-series diode stacks is given in Table 1.

Table 1. Experimental outputs of different pulsers implementing different EG series diodes.

	Optimum Trigger length (ns)	Peak Voltage (kV)	Peak Power (kW)	Total Energy (mJ)	Rise Time (ns)	Fall Time (ns)	FWHM (ns)
7-stack (EG1605)	1000	4.6	415.9	6.43	6.3	59.8	18.2
7-stack (EG1606)	1000	4.5	406.8	6.06	9.4	65.4	19.1
14-stack (EG1605-1606)	800	6.1	736.9	4.96	6.8	14.8	8.5
21-stack (EG1605-1607)	700	5.0	492.0	3.53	14.3	16.4	8.8
21-stack (EG1607-1609)	900	4.0	325.6	4.43	30.6	59.0	20.6
28-stack (EG1571-1574)	700	6.7	905.2	5.04	9.6	18.9	6.9
28-stack (EG1605-1608)	600	2.9	168.2	2.15	28.9	30.7	17.8

From Table 1, we clearly see that the expected output for 28-stack diodes does not match with the simulated output, which we believe is mainly due to the inaccurate SPICE models developed for the DSRDs as individual dies differ significantly in their characteristics (see the DSRD Testing, Simulation, and Optimization Summary Report) and a single SPICE model cannot represent all the dies in a stack. Another reason for mismatch between the simulation and experiment could be the difference between the expected inductance of custom-built inductors and their real values in experiments.

Although the experimental result for 28-stack diodes were off from the expectation, we obtained 6.1 kV from a pulser using two 7-stack diodes, which is close to the expected output (7 kV) and met our target of 5 kV output. Another important result obtained from the 7-stack measurement is that we did not observe a breakdown effect below 4.6 kV (Figure 4), from which, we estimated a breakdown voltage of ≥670 V/die, an important diode parameter for designing new pulser circuit.

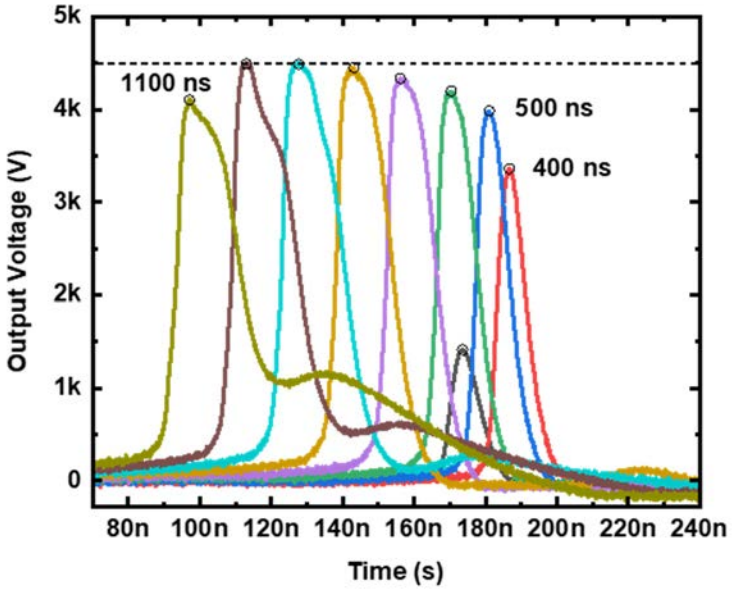


Figure 4. Pulser output using 7-stack EG1606 diode for different trigger lengths.

Figure 4 also shows an important result that increasing the trigger length beyond an optimum value results in lower output voltage, which verifies our prediction based on the working theory developed.

As we hypothesized that the incorrect values of the custom-built inductors could be the reason behind the mismatch between simulation and experiments, we planned to comprehensively characterize the inductors. Initially, we used Coil64[6], an open-source application, to design and construct the inductors using a wire of known diameter. The application also estimates the series resistance, self-capacitance, and self-resonance frequency of the inductor. However, we later realized that the program does not consider the frequency dependence of the equivalent circuit parameters for the inductors, which is a major source of error for a circuit working in the MHz range. Thus, we developed another

Python script to approximate the inductance. The inductors were then characterized using an Agilent 4294A impedance analyzer to compare the results with the theoretical approximation. With the new calculations, we were able to estimate the inductance of the custom-built inductors within a ±10% error margin.

Moving forward, we optimized a pulser circuit using three 7-stack diodes from the EG series with a target output voltage of 10 kV using a prime supply voltage of 120 V and trigger length of 500 ns. Theoretically, a 21-stack diode should be able to produce an output of >14 kV based our measured reverse breakdown voltage. However, we were only able to achieve a maximum output voltage of 9.2 kV (Figure 5) with a 10–90% risetime of 9 ns (20–90% risetime of 5 ns) for a prime source of 140 V and a trigger length of 750 ns. This is the highest peak voltage output and the highest linear voltage gain ($V_{out}/V_{prime} = 65$) obtained with a single 1×1 DSRD pulser fabricated in this study.. However, there are still discrepancies between the simulated and experimental result, which might be because of inaccuracies in diode parameters used in the SPICE simulation model.

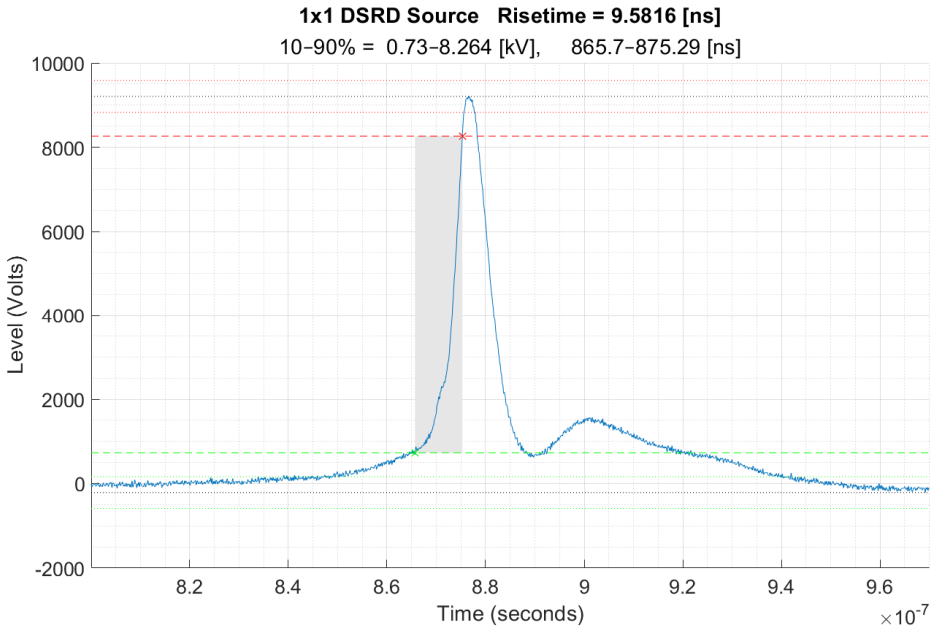


Figure 5. Output voltage pulse from a 1×1 DSRD pulser using EG1571, EG1572, and EG1573 7-stack diodes designed to produce 10 kV output.

3.11.7 Summary and Recommendations

This project of developing an all-solid-state ultra-short high-voltage pulse generator using drift-step-recovery diodes (DSRDs) started in Apr 2021 by targeting an ultralightweight alternative to large and heavy high-power microwave systems, which traditionally use

photo-triggered switches and spark gaps, to meet the SWAP-C targets of the OSPRES mission. Because DSRDs are not commercially available within the United States, we started our project by collaborating with a couple of diode manufacturers to fabricate DSRDs by providing them with optimum diode doping profile to achieve the highest peak voltage and the shortest risetime. After we obtained the diodes, we characterized them using standard diode characterization methods and developed SPICE models to be used in pulser simulations (see DSRD Testing, Simulation, and Optimization Summary Report). For the DSRD-based pulser, we chose a simple MOSFET-driven circuit as shown in Figure 2. The circuit provides a short forward current through the diode when the MOSFET is ON and a large reverse bias when the MOSFET is turned off, which drives the diode in sharp recovery mode, inducing a large output voltage pulse. Although identical and similar circuits are being used in DSRD-based pulsers by several authors, we did not find any theoretical basis for their circuit optimization. Thus, we developed a physics-based circuit working principle and utilized it to develop a systematic circuit optimization scheme to get the highest possible pulsed output voltage using a minimum input voltage supply. Using the theory and optimization algorithm, we simulated, optimized, and experimentally demonstrated many pulsers using diode stacks with varying diode quantity. For a pulser using 7-stack diodes, we measured a maximum peak output voltage of 4.6 kV, suggesting that the diodes have a reverse breakdown voltage of >670 V per die and that a maximum of 14 kV pulse is possible using 21-stack diodes. However, to achieve that, we needed a much larger current through the MOSFET beyond its safe limit (500 A). To increase the current, we developed a driver circuit module to drive a total of four MOSFETS in parallel thereby increasing the MOSFET current limit to 2 kA. Using the parallel MOSFETs and three 7-stack diodes, we were able to achieve a maximum peak voltage of 9.2 kV with a 20–90% risetime of 5 ns using a prime source of 140 V.

Although we developed and implemented our circuit optimization scheme to obtain the largest linear voltage gain of 65 reported, we could not obtain the maximum possible output voltage (14 kV) allowed by the diode reverse breakdown voltage due to the open circuit voltage limitation of the MOSFET modules. With increasing output voltage, the MOSFET voltage increased beyond its safe limit (1500 V), and we observed frequent MOSFET burn out. To increase the output voltage by increasing the number of diodes within the stacks, we recommend two potential strategies: (a) developing a MOSFET module with multiple MOSFETs in series so that they can handle much larger voltage spikes during pulse production, or (b) combining multiple single stack pulsers in parallel to increase the load current and thus output voltage. Additionally, the pulse risetime of the output we obtained did not meet our target (≤1 ns) as it is controlled by the diode recovery property which we cannot modify at the circuit level. With better diodes with shorter recovery time, it is certainly possible to achieve shorter risetime. Due to time limitations, we could not perform PRF studies of the pulser developed, which is very important for the OSPRES mission, and we recommend a comprehensive study of this in the future. There are still inconsistencies between the simulated and experimental output,

and we believe that such inconsistencies are due to imperfect SPICE models of the diodes developed, which can be further improved upon.

3.11.8 Outputs

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3.11.9 References

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3.12 Diode-Based Nonlinear Transmission Lines

(Nicholas Gardner)

3.12.1 Executive Summary

Diode-based nonlinear transmission lines (D-NLTLs) have been investigated as a way to reduce the size, weight, and cost of pulse forming networks (PFNs) for application in Navy afloat missions. D-NLTLs are promising due to their compact design, which uses commercial off-the-shelf components, and their lack of need for auxiliary cooling or external fields for operation. However, D-NLTL networks have not yet been implemented outside of the lab setting due to an inefficient design process, a dynamic characteristic impedance that makes signal injection/extraction challenging, and demonstrated frequency and power generation that fall short of the requirements of directed energy weapon systems. We have made progress on each of the above fronts by developing clear design metrics ranging from component selection to device fabrication, effectively using bipolar excitation on a DC biased D-NLTL, and building D-NLTLs with high voltage epoxy diodes that can handle signal amplitudes in the single to tens of kV. Our studies have shown D-NLTL networks with demonstrated frequency generation in the upper VHF (30–300 MHz) to UHF (0.3–1 GHz) ranges, with our highest recorded frequency generation of 1.58 GHz reaching into the L-band (1–2 GHz).

3.12.2 Objective

The size, weight, and cost of pulse forming/shaping networks (PFNs) need to be reduced and optimized for Navy afloat missions. In an effort to optimize such systems, work focused on developing a diode-based nonlinear transmission line (D-NLTL) as a pulse shaping network for the conversion of energy to the ultra-high frequency (UHF) band (0.3–3 GHz) at single MW peak power. To date D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit as shown in Figure 1. Simulations of lumped element (LE) NLTLs indicate achievable frequencies in the single GHz range. However, simulation/measurement agreement becomes increasingly sensitive to parameters and factors outside of inductive and capacitive element choice alone at frequencies above ~100 MHz. Disparities between measurement and simulation above contribute to a trial by error design process for D-NLTL networks.

To improve simulation/measurement agreement and streamline D-NLTL design processes, diode parameters affecting frequency generation in the context of a NLTL application are identified and characterized via simulation and experiment, for the purposes of setting limits and desired ranges required for UHF generation. Such parameters include, but are not limited to: diode frequency response, diode reverse bias hold-off voltage, diode small signal capacitance, diode chip/package parasitics, and diode relaxation time. The improved understanding of the explored parameters will be used to design and fabricate a D-NLTL capable of GHz center frequency generation at single MW peak powers.



Figure 1. 20 cell D-NLTL of dimensions 1.1 x 23.45 cm constructed with commercial off the shelf components.

3.12.3 Technical Background: D-NLTL Theory

Diode-based nonlinear transmission lines are a ladder network of cascading cells, each with a series inductance provided by a linear inductor and a shunt capacitance provided by the reverse bias P-N junction of a diode as shown in Figure 2.

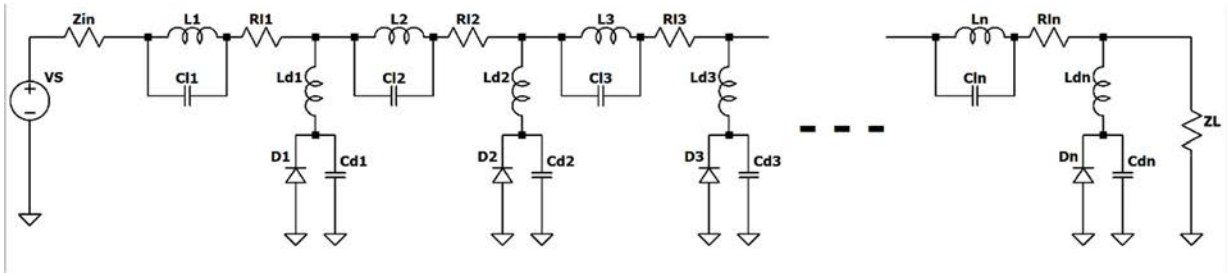


Figure 2. Example of a D-NLTL schematic. Ln and Dn represent the series lumped inductance and shunt reverse bias diode respectively. C_{Ln}, R_{Ln}. L_{Dn}, and C_{Dn} represent sources of loss present in the inductor and diode packages.

As a signal passes through a given cell in a D-NLTL network, the size of the depletion zone will decrease as the amplitude of the pulse increases. When depletion zone size decreases, the permittivity of the semiconductor material decreases with it. Such a relationship between device permittivity produces a nonlinear voltage dependent capacitance similar to that shown in Figure 3 and modeled by Equation 1.

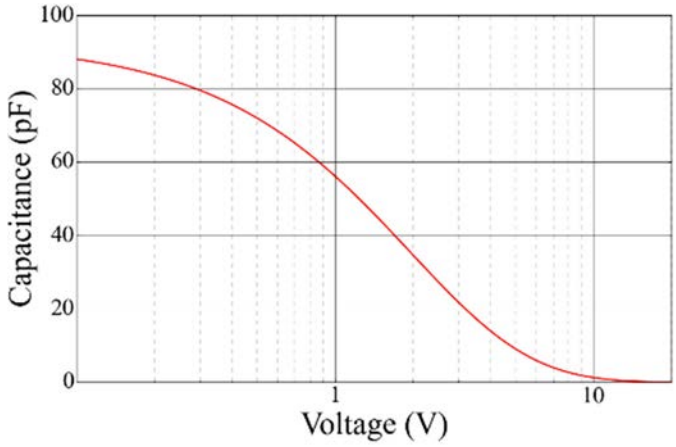


Figure 3. An example characteristic capacitance curve. The curve is for the SMV1702 model diode by Skyworks used in several of the low-voltage D-NLTL studies.

$$C(V) = \frac{C_{j0}}{\left(1 - V/V_j\right)^m} \quad (1)$$

When a signal enters a nonlinear transmission line, variations in network capacitance produced by Equation 1 generate variations in signal propagation rate according to Equation 2.

$$v = \frac{1}{\sqrt{LC(V)}} \quad (2)$$

Equations 1 and 2 produce edge sharpening in the signal wherein high amplitude portions of the signal have a larger group velocity than low amplitude portions of the signal. The amount of rise time reduction (quantified by Equation 3) is critical to determining the behavior of a D-NLTL.

$$\Delta T = n\left(\sqrt{LC_{j0}} - \sqrt{LC(V_{max})}\right) \quad (3)$$

When the excitation rise time ($t_{r,\,in}$) is less than ΔT, the network will operate to only sharpen the rise time of the pulse. However if $t_{r,in}$ is less than ΔT, a shock wave is produced in the network. The rise time of the shock wave is limited by the low pass characteristic provided by a shunt capacitance taking on a value determined by Equations 4 and 5.

$$t_r \sim \frac{1}{f_{bragg}} \quad (4)$$

$$f_{bragg} = \frac{1}{\pi\sqrt{LC_{max}}} \quad (5)$$

A signal is broken into a sequence of soliton waveforms (shown in Figure 4) by a D-NLTL network through production of a shock wave and spatial dispersion provided by the lumped element structure. It is both the production of the minimum rise time and the timing of the soliton peaks that are responsible for increasing frequency content in a signal. The sharpened rise time corresponds to the max or Bragg frequency (f_{Bragg}), and the time between solitons corresponds to the center frequency (f_c).

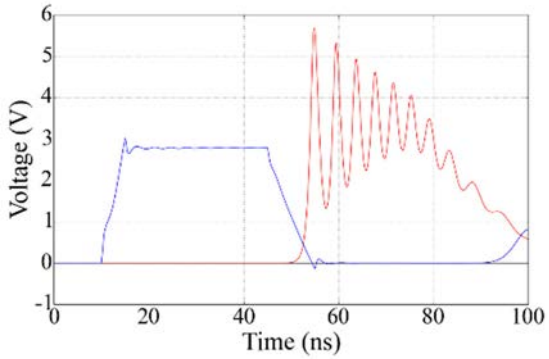


Figure 4. A monopolar square pulse (blue) broken into a sequence of soliton waveforms (red) through a balance of shockwave production from nonlinearity and spatial dispersion from the lumped element structure.

3.12.4 Tasks, Milestones, and Status

(A) Milestone – Construct/demonstrate a prototype capable of UHF generation at low voltages (1–100 V excitation amplitude)

(A1) Break a low-voltage pulse into a sequence of solitons (SEP20)

(A2) Increase frequency generation past 200 MHz (NOV20)

(A3) Write/Submit manuscript on D-NLTL design processes (MAY22)

(B) Milestone – Demonstrate tuning of waveform at low voltages using electrical or mechanical means (Completed with voltage biasing APR21)

(B1) Write/Submit manuscript on LV D-NLTL tuning circuit (Ongoing/In Revision)

(B2) Simulate a HV tunable D-NLTL topology using the K series epoxy diodes (DEC21)

(C) Milestone – Construct/demonstrate a prototype capable of frequency generation above 1 GHz at single MW peak powers (Completed MW peak power but not GHz center frequency – Ongoing)

(C1) Identify diode candidates with a hold-off voltage of several kV and a low signal junction capacitance under 100 pF (Completed JAN21)

(C2) Design/fabricate single diode prototypes (Completed JAN21)

(C3) Perform initial tests using half-barrel pulse source (Completed FEB21)

(C4) Test a prototype using two diodes in series (Completed FEB–MAR21)

(C5) Test lines using Mega Impulse source (Completed MAY21**)**

(C6) Test K50F D-NLTL using PCSS as a source (Completed JUN21)

(C7) Use simulations and tests to refine line for increased frequency generation (Completed JULY21)

(C8) Test lines using PCSS as a source with various cell inductances (Completed JULY**)**

(C9) Test lines using Marx Generator as a source (Completed AUG21)

(C10) Write/Submit manuscript on the GHz MW D-NLTL Prototype (Ongoing/In Revision)

3.12.5 Approach

Disparities between simulation and measurement necessitated that D-NLTL work followed a cyclic approach as shown in Figure 5. First a primary research milestone (i.e., Milestone A, B, or C from the previous Section) would be identified. If a previously built prototype was potentially capable of advancing work on the chosen milestone, results were simulated for that prototype and then measurements were carried out. If there was not a prototype available, then one was designed based on the rules of thumb, constructed, and measurements would be taken. Regardless of advancement of primary milestone, measured results were consistently compared back to simulated results to work towards achievement of a secondary goal of improving a general D-NLTL design process for devices operating in the UHF frequency band.

All investigations had 4 primary measurements used to evaluate whether a given design achieved a desired milestone: Peak power, Center frequency, Efficiency of RF content generation, and Bragg cutoff frequency. Each is shown in Figure 6. Measurements specific to a single milestone are described in greater detail in the next Section.

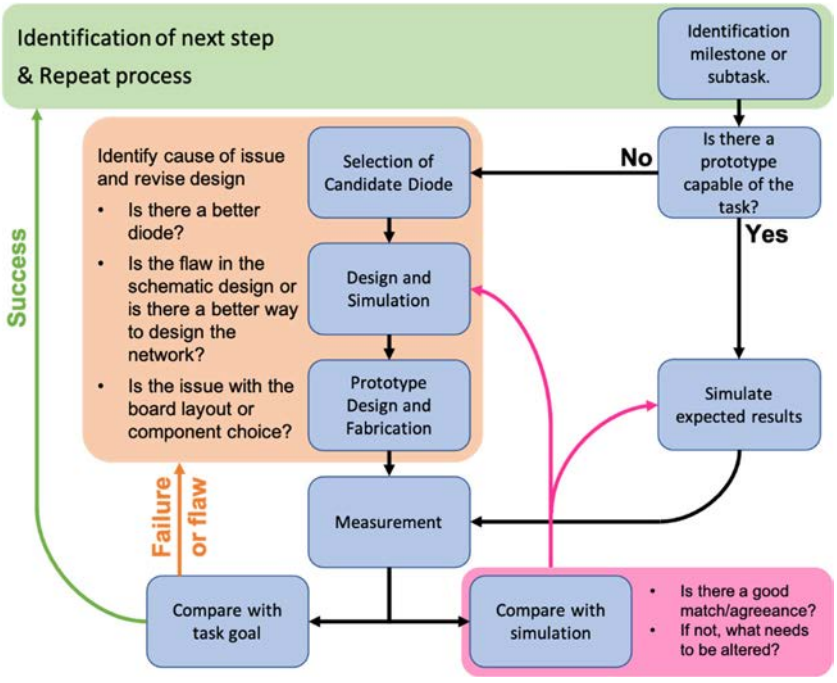


Figure 5. The cyclic process used for D-NLTL research. Research would focus on a primary objective (i.e., Milestone A, B, or C from the previous Section) while using measured results to continuously feedback into and improve the initial simulation and prototype design process to achieve the secondary objective of improving D-NLTL design pathways for high frequency generation.

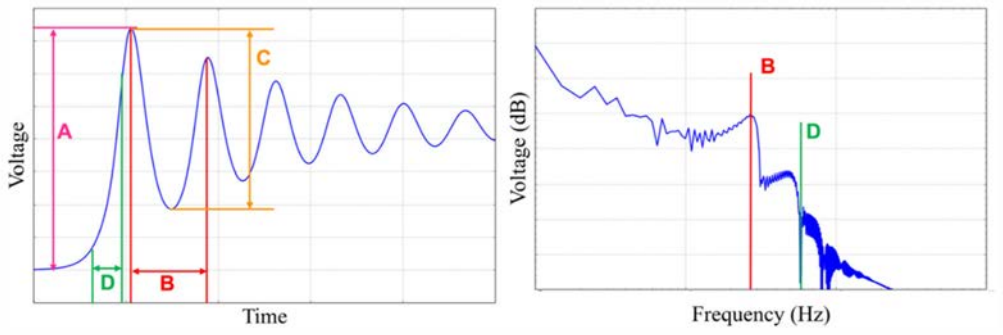


Figure 6. The measurements of interest in D-NLTL work in time and frequency domains. A denotes the peak power, B denotes the center frequency measurements, C denotes the voltage modulation depth, and D denotes the Bragg frequency cutoff.

3.12.6 Results and Discussion

There are three primary milestone results to discuss, each with its own manuscript either in publication or currently in the review process. The first is work on the design process for D-NLTLs intended for operation in the UHF band. The second involves work related to application of a DC bias to D-NLTLs. The third is work done on a D-NLTL capable of generating peak powers on the order of a single MW as well as maximum frequencies on the order of a single GHz.

3.12.6.1 D-NLTL Design Metrics

Prior to OSPRES work on D-NLTL systems, results presented in the literature focused primarily on sub 100 MHz center frequency generation, with most notable works presenting frequency generation in the single to few 10s of MHz [4-7]. When design processes presented in these words were applied to achieve UHF band generation, prototypes failed to produce results close to those from simulations, often failing to demonstrate soliton generation at all. As a solution to the problem, parametric studies were performed on a D-NLTL prototype operating in the VHF (very high frequency, 30-300 MHz) band. The goal of the parametric studies was to determine what design parameters needed to be considered when simulating and constructing D-NLTLs for operating frequencies above 100 MHz. These parametric studies were then used to produce rules of thumb for designing and fabricating D-NLTL prototypes for operation in the upper VHF to UFH frequency bands. Design parameter applicability was demonstrated by fabricating a D-NLTL with a center frequency of 256 MHz and demonstrating a high degree of agreement between simulation and measurement. Results were of high significance as the previously highest reported center frequency by a D-NLTL was 230 MHz [8-9]. Results are summarized below with more detailed results published in AIP advances as “Design Considerations for Diode-Based Nonlinear Transmission Lines” [1]. Table 1 summarizes the trends found in the D-NLTL parameter space studies. Results found were used to produce the following design metrics for D-

NLTLs operating at frequencies above 100 MHz. Table 2 summarizes rules of thumb for device selection and prototype design parameters developed from D-NLTL parameter space trends.

Table 1. Results of parametric studies of D-NLTLs operating in the VHF band.

Parameter	**Result for D-NLTL behavior**
Excitation amplitude	Direct effect on peak amplitude, f_c, f_{Bragg} and η_{RF} with all increasing with excitation amplitude.
Excitation width	Only effected number of solitons generated over the tested range with a soliton generated per 10 ns of FWHM.
Cell inductance	There is a tradeoff between f_c and η_{RF}. Low *L* gives high f_c but if line length is not altered signal VMD drops.
Termination impedance	Reflections of multi-soliton waveforms can be suppressed when the D-NLTL is terminated using Z_{avg} for the network.
Diode CV curve	Frequency generation increases at low C_{j0}, low V_j and high m values corresponding to a sharp *C(V)* curve with a low average capacitance.

Table 2. Rules of thumb for component selection and D-NLTL network design.

Design Parameter	**Guidance**
Cell Inductance L	Should fall in a range of 10–100 nH. Below 10 nH and PCB trace inductance dominates. Above 100 nH necessitates a diode capacitance in the range of PCB stray capacitance.
Diode V_R	Based on potential power production using the equation $P_{max} = V_R^2/50\Omega$. In General, V_R should be large enough to avoid signal clipping.
Diode C_{j0}	Should be low enough to allow for frequency generation above a minimum desired frequency based on $f_{min} = 1/\pi\sqrt{LC_{j0}}$
Diode Saturation	Diode saturation needs to occur within the desired operational range and correspond to a Bragg frequency above desired operation frequencies.
Line Length	Constrain to keep *VMD* close to 50% while attaining desired center frequency.
Diode and Inductor Package Parasitic	Must be included in simulation either from manufacturer specifications or estimated for reliable center frequency predictions

Parameters shown in Table 2 were verified through design of a D-NLTL capable of frequency generation in the upper VHF band. The fabricated D-NLTL consisted of 40 cells each with one SMV1702 model diode from Skyworks Inc and one 22 nH air core inductor. Figure 7 shows waveform results and simulation comparisons. The D-NLTL produced a center frequency of 256 MHz and a f_{bragg} of 446 MHz.

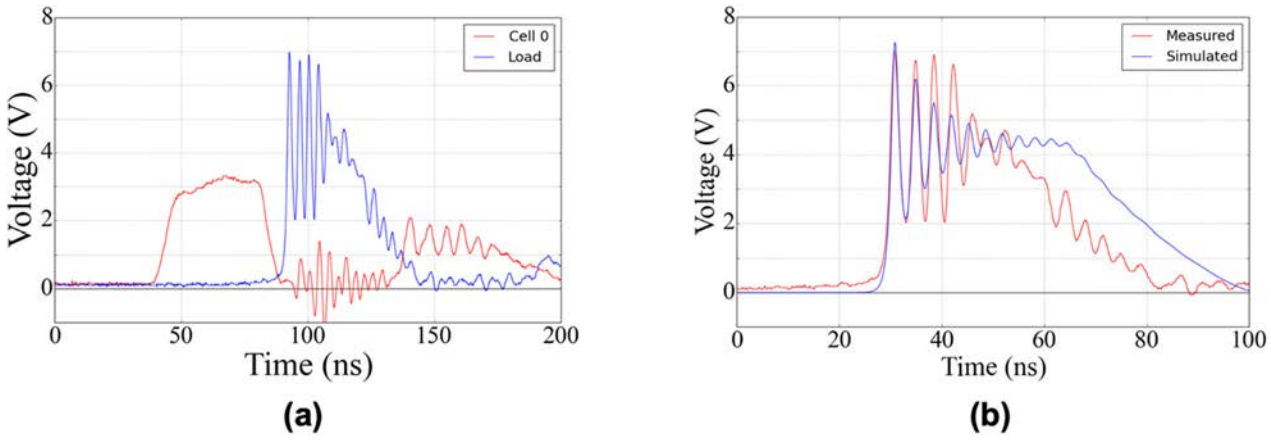


Figure 7. Results from the SMV1702 D-NLTL. (a) Displays waveform measurements taken from prototype testing. (b) Displays a comparison between measured and simulated waveforms for verification.

More details on results can be seen in the following monthly grant reports on D-NLTLs:

- September 2020 – Section 3.4
- October 2020 – Section 3.1
- Fall 2020 Review

3.12.6.2 Electrically Tunable D-NLTL

A major roadblock to D-NLTL implementation in RF systems is a dynamic impedance characteristic to D-NLTLs. The dynamic capacitance responsible for shockwave production and soliton generation also produces a signal-dependent impedance that increases as signal strength increases. OSPRES work on electrical control of diode characteristic capacitance was initially aimed at finding methods of increasing the frequency agility of a D-NLTL system and ended up producing a method of both enabling use of bipolar excitations and reducing negative effects of a dynamic impedance.

An ability to electrically alter D-NLTL characteristics through an application of a DC bias to each diode in the network was presented in publications by two separate groups [10-11]. Work by Kim and co-authors indicated frequency characteristics could be altered by applying a DC bias to each diode and provided a helpful initial design for DC bias application, however the presented work focused only on the cutoff frequencies of the network and not on center frequency or soliton generation [10]. Work by Marsteiner and co-authors indicated a DC bias could allow for use of bipolar excitations, however results were purely simulated using specially designed waveforms [11].

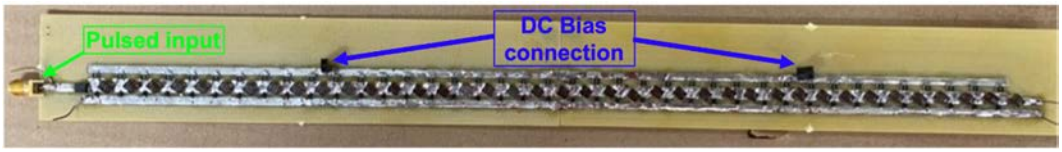


Figure 8. The D-NLTL prototype used for DC biasing investigations.

For our work we attached a DC bias to the anode of each diode through 1 kΩ surface mount resistors in a 40 cell D-NLTL network based on the SMV1702 diode as shown in Figure 8. In the first round of tests the D-NLTL was provided with a 10 V monopolar square excitation while positive and negative polarity DC biases were applied to the network. Increasing magnitude of a positive polarity bias increased generated center frequency, while increasing magnitude of a negative polarity bias decreased generated center frequency. Figure 9 displays examples of waveform responses to the applied bias and Figure 10 displays full results of DC bias effect on center frequency. Of note is a reduced VMD at increased positive DC biases in Figure 9 and a center frequency flattening at the upper range of applied DC biases in Figure 10. Each effect is attributed to flattening of diode CV curves at saturation. At low saturation diode capacitance, characteristics are highly nonlinear and produce desired frequency characteristics, while at saturation, CV characteristics flatten and become less dynamic and less capable at producing high frequency content.

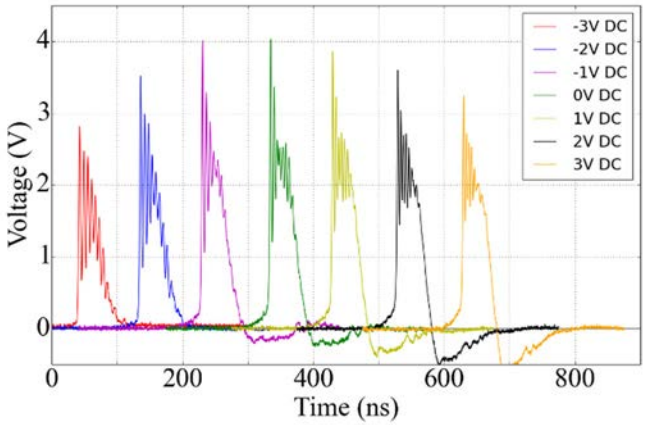


Figure 9. Waveform response to applied DC bias. Waveforms are shifted both temporally and vertically for ease of comparison.

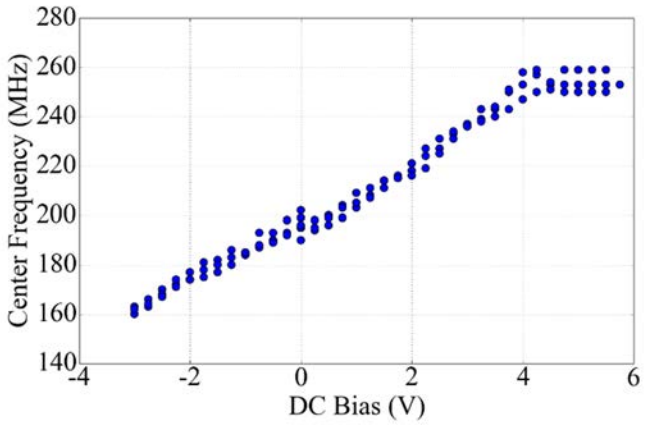


Figure 10. Effect of applied DC bias on generated center frequency.

The next task was to test the results from the manuscript produced by Marksteiner and co-authors to see if a DC bias could allow for use of bipolar excitations outside of simulation. In all cases the applied bias was set to the negative polarity amplitude of the bipolar pulse. A 10 V peak-to-peak 20 MHz sine wave and a 10 V peak-to-peak 8 MHz 20% duty cycle square wave were tested with the network. Waveform results for the study are shown in Figure 11, and center frequency results for an unbiased 10 V square pulse, biased sine wave, and biased square wave are shown in Table 3. In the case of a bipolar square-wave excitation on a DC biased D-NLTL, a 37% increase in center frequency was observed when compared to an unbiased D-NLTL with a 10 V square pulse excitation. The increased center frequency can be attributed to mitigation of impedance mismatch effects at the source-line interface. Since the DC bias is applied after the source-line interface, the actual pulse amplitude affected by the mismatch is ±5 V as opposed to +10 V in the monopolar case. An amplitude of ±5 V causes a smaller swing in D-NLTL impedance, allowing for a smaller fraction of energy to be lost. In the observed results, the amplitude was reduced by ±1 V, when the signal was superimposed on the DC bias the resulting effective pulse amplitude was 8 V, driving each diode to a greater saturation and greater frequency generation. In comparison, the 10 V monopolar pulse would be reduced to an amplitude of 3 V after the source-line interface.

Table 3. Center frequency result comparison for a 10 V monopolar square pulse on an unbiased line, a 10 V peak-to-peak 20 MHz sine wave, and a 10 V peak-to-peak 8 MHz square wave.

	Unbiased Square pulse	Biased 20 MHz Sinusoid	Biased 8 MHz Square wave
Center Frequency	190–200 MHz	214 MHz	263 MHz

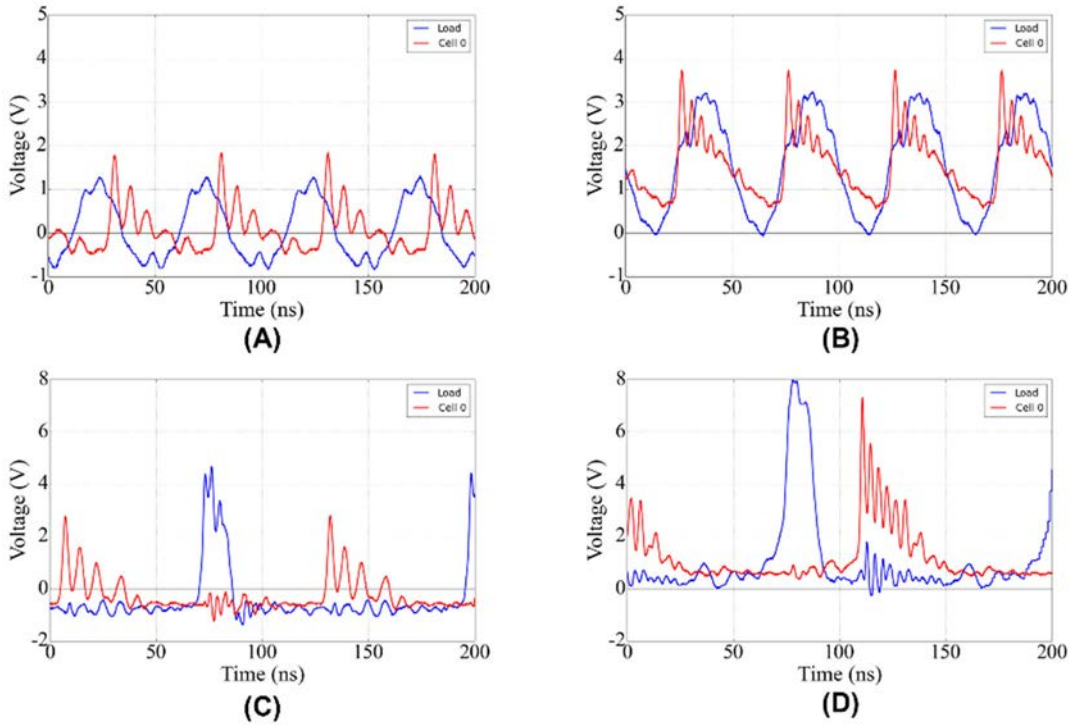


Figure 11. Bipolar excitation waveform results. (A) 10 V peak-to-peak 20 MHz sine wave with no DC bias. (B) 10 V peak-to-peak 20 MHz sine wave with DC bias. (C) 10 V peak-to-peak 8 MHz 20% duty cycle square wave with no DC bias. (D) 10 V peak-to-peak 8 MHz 20% duty cycle square wave with DC bias.

More details on results can be seen in the following monthly grant reports on D-NLTLs:

- February 2021 – Section 3.7
- March 2021 – Section 3.3
- Spring 2021 Review
- June 2021 – Section 5.1

3.12.6.3 GW-GHz D-NLTL

Using design parameters specified in the “D-NLTL Design Metrics” Section, epoxy diodes capable of handling reverse bias potentials of several kV and C(V) curves capable of frequency generation in the upper UFH to L (1–2 GHz) band frequencies. Diodes were produced by Voltage Multipliers inc. and their parameters are shown in Table 4.

Table 4. Device parameters for K50F and K100F model high voltage epoxy diodes from Voltage Multipliers Inc.

Diode	C_{j0} (pF)	V_j (V)	C(1 kV) (pF)
K50F	68.46	5	6.85
K100F	34.76	10	3.48

Prototypes were designed for two purposes:

1) Achieve GHz frequencies and MW peak powers
2) Evaluate if frequency and power output could be reliably increased through series stacks of diodes

Three pulsed sources were used for measurements: one based on a drift step recovery diode (DSRD) circuit, one based on a photoconductive semiconductor switch (PCSS), and a ppm0731 pulser from Mega Impulse (MI). The reasoning for using each source is summarized in Table 5.

Table 5. Motivation behind each pulse source used for D-NLTL excitation.

Source	Reason
DSRD	Highest amplitude source readily available. Capable of providing amplitudes of ~10 kV. Expected to drive each D-NLTL to maximum saturation and therefore max possible frequency generation. Not expected to produce multiple solitons due to narrow pulse width.
PCSS	Square pulse with sufficient width to generate waveforms with multiple solitons. Amplitude would not drive D-NLTL to its limits, but would verify if the D-NLTLs could form multi soliton waveforms as intended.
MI	Rise time and pulse width of MI pulse was far above the theoretical Bragg cutoff frequency of each line. Both lines were expected to greatly attenuate the waveform, demonstrating their low pass characteristic.

Results from each test are shown in Figure 12 and summarized in Table 6. Significant findings included: a Bragg frequency generation in the L-band, peak power production in the single MW range, and a center frequency in the UHF band.

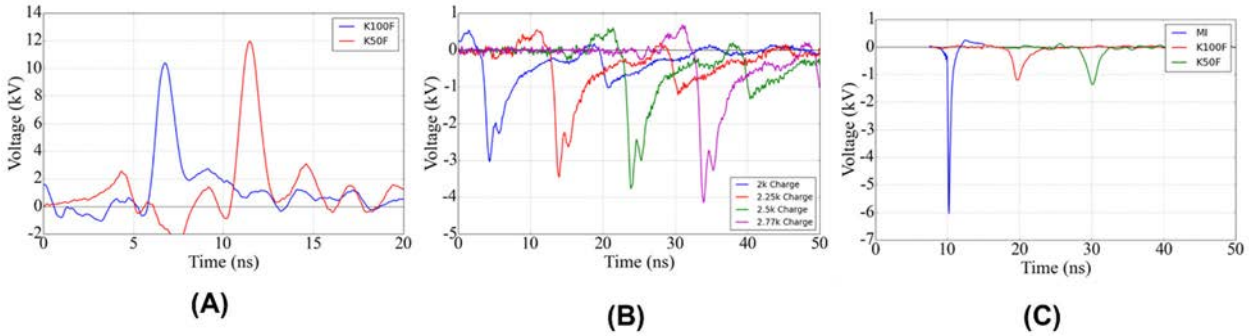


Figure 12. Waveform results from HV D-NLTL studies. (A) DCRD Waveforms for both NLTLs. (B) PCSS waveforms for the K100F D-NLTL. (C) MI waveforms with MI excitation waveform for reference.

Table 6. Frequency and power results for each source with each D-NLTL. Center frequency was only measured when multi-soliton waveforms were produced. Peak powers are calculated for a 50Ω load.

Source	D-NLTL	f_{Bragg}	f_c	P_{peak}
DSRD	K50F	1.44 GHz	--	2.88 MW
	K100F	1.58 GHz	--	2.33 MW
MI	K50F	677 MHz	--	36.9 kW
	K100F	926 MHz	--	29.0 kW
PCSS	K100F	1.19 GHz	756 MHz	342.7 kW

More details on results can be seen in the following monthly grant reports on D-NLTLs:

- February 2021 – Section 3.7
- March 2021 – Section 3.3
- Spring 2021 Review
- May 2021 – Section 3.3
- June 2021 – Section 5.1
- July 2021 – Section 5.1
- August 2021 – Section 5.1
- September 2021 – Section 9.1

3.12.7 Summary and Recommendations

Diode-based nonlinear transmission lines present a possible avenue for the reduction of size, weight, and cost of RF systems when used as a pulse shaping network within a larger system. D-NLTLs have a characteristic lumped element ladder network topology that is compact, makes use of commercially available components, and does not require use of auxiliary cooling systems or external fields for operation. However, implementation of D-NLTLs in real world systems has been held back by inefficient design processes, impedance matching issues, and lack of demonstration of frequency generation above the VHF band or MW peak powers.

In our work we improved D-NLTL design processes for VHF and UHF band applications by providing guidelines for component selection and device fabrication, summarized in Table 2. We demonstrated improvements in matching the dynamic impedance of a D-NLTL through use of a bipolar excitation pulse and DC biasing diodes in the D-NLTL network. Finally, we demonstrated that UHF and L-band frequency generation as well as MW peak power generation is possible with proper diode selection. Further we showed an ability to increase D-NLTL frequency and power generation through series stacks of diodes in each D-NLTL cell. Each of the presented results brings D-NLTL networks closer to achieving the goal of reducing the size, weight, and cost of RF systems.

To further improve D-NLTL applicability, future research paths should focus on: metrics for production of custom diodes, investigation into substrate materials outside of standard FR4 PCB, and demonstration of signal radiation from a D-NLTL system.

3.12.8 Outputs

3.12.8.1 Published/In Press

[1] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “Design Considerations for Diode-Based Nonlinear Transmission Lines,” AIP Advances, 12, 055012, May **202**2 [doi].

3.12.8.2 In Preparation

[2] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “UHF and L-Band Frequency Generation at MW Peak Power using Diode-based Nonlinear Transmission Lines as Pulse Forming Networks,” *Transactions on Plasma Science*, In Preparation, **2023**.

[3] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “Electrically Tunable Diode-Based Nonlinear Transmission Line,” *TBD*, In Preparation, **2023**.

[4] N. Gardner, “Diode-Based Nonlinear Transmission Lines as a High Power Radio Frequency Source,” PhD Dissertation, In Preparation, **2023.**

3.12.9 References

[1] E. G. L. Rangel *et al.*, “The Development of Capacitive Nonlinear Transmission Lines and Its Performance Limits,” *IEEE Int. Pulsed Power Conf.*, vol. 2019-June, 2019, doi: 10.1109/PPPS34859.2019.9009883.

[2] E. G. L. Rangel *et al.*, “The Development of Capacitive Nonlinear Transmission Lines and Its Performance Limits,” *IEEE Int. Pulsed Power Conf.*, vol. 2019-June, 2019, doi: 10.1109/PPPS34859.2019.9009883.

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[4] L. P. S. Neto, J. O. Rossi, J. J. Barroso, E. G. L. Rangel, and E. Schamiloglu, “Improving the voltage modulation depth and RF power generated on Nonlinear Transmission lines,” *2018 IEEE Int. Power Modul. High Volt. Conf. IPMHVC 2018*, pp. 416–420, 2018, doi: 10.1109/IPMHVC.2018.8936795.

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[6] L. R. Raimundi, J. O. Rossi, E. G. L. Rangel, L. C. Silva, and E. Schamiloglu, “High-voltage capacitive nonlinear transmission lines for RF generation based on silicon carbide schottky diodes,” *IEEE Trans. Plasma Sci.*, vol. 47, no. 1, pp. 566–573, 2019, doi: 10.1109/TPS.2018.2873491.

[7] H. Kim, S. J. Ho, M. K. Choi, A. B. Kozyrev, and D. W. Van Der Weide, “Combined left- And right-handed tunable transmission lines with tunable passband and 0° phase shift,” IEEE Trans. Microw. Theory Tech., vol. 54, no. 12, pp. 4178–4183, 2006, doi: 10.1109/TMTT.2006.885884.

[8] Q. R. Marksteiner, B. E. Carlsten, and S. Russellce, “Efficient Generation of RF using a Biased Soliton Generating Nonlinear Transmission Line with a Bipolar Input,” Microw. Opt. Technol. Lett., vol. 52, no. 6, pp. 1411–1413, 2010.

3.13 Continous Wave Diode-NLTL Based Comb Generator

(John Bhamidipati and Nicholas Gardner)

3.13.1 Executive Summary

Diode-based nonlinear transmission lines (D-NLTLs) were investigated to be implemented as SWaP-C optimized pulse shaping solution(s) for RF and microwave sources for navy afloat missions. In this effort, a majority of the focus was placed on continuous wave (CW) excitation of the D-NLTLs to understand and mitigate any limitations of pulsed mode of operation, such as power reflection, standing wave generation, and return power losses at the source–line and line–load interfaces induced by dynamic impedance changes due to varying diode capacitance, which limit practical D-NLTL applications. D-NLTLs were simulated, fabricated, and tested to be implemented as a comb generator by converting continuous wave (CW) signals from low frequency–very high frequency (LF–VHF) bands (0.03 MHz–30 MHz) to the ultra-high frequency (UHF) band (0.3–3 GHz) at ones-of-MW peak power. D-NLTL characteristics in terms of center frequencies, peak power, peak voltages, and harmonic generation were studied as functions of series inductance, diode model(s), and excitation frequency. Although simulation studies revealed frequency generation up to 2 GHz, only up to 0.5 GHz was realized experimentally with up to 100 MHz exciation. At excitation frequencies ≥100 MHz, the D-NLTL operation was found to shift from soliton generation mode to pulse sharpening mode, wherein an output frequency of 1.5 GHz was obtained when tested with a 700 MHz sinusoidal pulse.

Despite experimentally realizing up to 0.5 GHz and ~1.5 GHz output frequencies in D-NLTLs with <50 MHz and 700 MHz CW excitation, respectively, the impedance mismatch issue still remains partially unresolved. A need for a source–line interface with non-standard impedance was identified in order to minimize reflections when connecting the NLTL to the excitation source. This can potentially be achieved by implementing one or more impedance transformer(s) between the source output and NLTL input, which can potentially reduce the impedance mismatch and reduce the power reflection issues in CW mode

3.13.2 Objective

While diode-based nonlinear transmission lines (D-NLTLs) are a promising technology towards optimizing SWaP-C requirements of RF and microwave sources on Navy afloat missions, they present limitations in terms of power reflection, standing wave generation, and return power losses at the source–line and line–load interfaces due to dynamic impedance changes the diodes undergo in pulsed operation mode, limiting practical D-NLTL applications. This goal of this effort was to use a D-NLTL triggered in continuous wave (CW) mode to work as a comb generator by converting CW signals from low frequency–very high frequency (LF–VHF) bands (0.03 MHz–30 MHz) to the ultra-high frequency (UHF) band (0.3–3 GHz) at ones-of-MW peak power. Such an application with reduced dependence on transient changes was expected to decrease impedance

mismatch effects at the source–line and line–load interfaces by continuously oscillating D-NLTL peak impedance between the same two values.

However, the design considerations for COTS high-frequency D-NLTL based comb generators capable of generating up to ~50 GHz frequencies are limited to <1 Watt output powers, which is <0.1% of the power handling capability required for navy afloat missions. Using the metrics associated with low-power comb generators alone to design D-NLTLs capable of generating ~1–2 GHz frequency with capability to handle MW-order peak powers could potentially introduce design errors resulting in frequency/power prediction–measurement discrepancies on the order of a few hundred MHz. This effort is focused on investigating design parameters and demonstrating an ability to reduce the source–line impedance mismatch effect on signal amplitude via CW excitation, first through simulations and then by validating the results experimentally using low voltage (LV) and high voltage (HV) prototypes. A successful demonstration of improvements to impedance matching at the source–line interface using a CW signal measured as a reduction in signal amplitude loss between the source and D-NLTL.

3.13.3 Technical Background

Nonlinear-permittivity-based NLTLs are all-solid-state discrete-element-based networks designed to generate microwave frequency content by breaking excitation pulses into sequences of solitary waves as shown in Figure 1. These can be implemented in civil, military, and medical applications such as pulse compressors, frequency multipliers, phase shifters, counter-electronics, radar, etc., involving pulse forming/shaping networks [1].

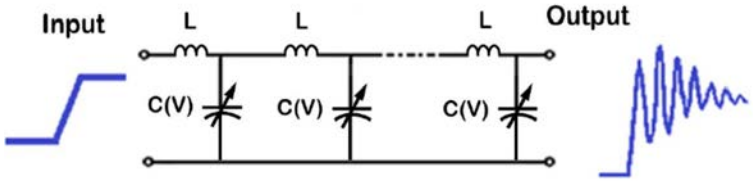


Figure 1. Circuit model of capacitive NLTL, adapted from Lopes Rangel et al.[2]

A discrete-element NLTL consists of a nonlinear dispersive medium where electrical solitons propagate in the form of voltage waves with a constant shape and velocity. Soliton formation occurs due to the balance between the effects of dispersion and nonlinearity. Dispersion arises from the periodic nature of the elements, while the nonlinearity is introduced by nonlinear dielectric materials such as voltage-dependent capacitors and nonlinear ferrimagnetic materials such as current-dependent inductors. Indeed, these types of NLTLs can be categorized as capacitive, inductive, or hybrid lines according to the nonlinear elements used. The solitons in NLTLs can result in (i) edge sharpening and (ii) ultrafast pulse generation via frequency doubling.

Design and fabrication of diode-based NLTLs (D-NLTLs) for a specific frequency and power range is complex. Studies by Aziz [3], Drazin [4] and Infeld [5] aimed at connecting

complex soliton dynamics to network topology, requiring the use of simplified capacitance curves applied to idealized excitation pulses. Furthermore, the nonlinear capacitive reactance provided by a diode introduces a varying impedance, yielding issues with energy injection and extraction at the source–line and line–load interfaces, resulting in decreased D-NLTL efficiency, and in some instances causing complete destruction of the soliton wavefront [6]. Studies by Korteweg [7] and Ricketts[8] have shown some success in achieving a match with the dynamic impedance, but it was limited to a single soliton wavefront similar to those in [9]–[10].

When an input pulse is injected into a dispersive *LC* line, it propagates down the line length with a velocity $v = \frac{1}{\sqrt{LC}}$, where *L* and *C* are the inductance and capacitance per unit length, respectively. If the line is implemented with a nonlinear capacitor whose capacitance decreases with an increase in voltage, the portion of the pulse with higher voltage amplitude will travel faster than the lower amplitude portion of the pulse, which starts to travel before the peak voltage. In this way, the pulse peak catches up with the rising edge, sharpening the pulse front with a very fast rise time, enabling D-NLTLs to enhance the discrete spectral content of a pulse with high volumetric power density by exploiting the nonlinear permittivity of the reverse-biased diodes instead of the variable capacitors.

Commercial-off-the-shelf (COTS) GaAs varactor diode-based monolithic microwave integrated circuit (MMIC) D-NLTL comb generators are capable of operating at input and output frequencies up to 600 MHz and 30 GHz, respectively. However, these comb generators are not capable of handling powers higher than 27 dBm (0.51 W). In-house pulsed D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes (~0.5–0.7 MW peak power) in a light-weight small-footprint circuit. Further D-NLTL network efficiency is hindered by a signal-dependent impedance characteristic to the network, leaving reported efficiencies of RF content generation at 10% or less of incident pulse energy.

3.13.4 Tasks, Milestones, and Status

(A) Demonstrate an ability of a CW excitation signal to reduce the source–line impedance mismatch effect on signal amplitude present in D-NLTLs when compared to pulsed mode operation, first through simulations and then by validating the results experimentally using low voltage (LV) and high voltage (HV) prototypes.

(A1) Show the potential to improve source–line impedance mismatch in simulation (Completed SEP21)

(A2) Experimentally demonstrate a low voltage (LV) and high voltage (HV) prototypes receiving a CW input to quantify and reduce source–line mismatch (Completed SEP21)

(A3) Compare measured results with simulation behavior; comparison of results will be used to further refine D-NLTL simulation techniques (suspended)

(A4) Determine if there are improvements to system behavior if D-NLTL diodes are biased when receiving a CW input (suspended)

(A5) Demonstrate improvements to the source–line impedance mismatch in a LV prototype (Completed FEB22)

(A6) Demonstrate a HV prototype receiving a CW input (Completed NOV21)

(B) Demonstrate UHF – L-band (0.3–2 GHz frequency) generation as functions of excitation frequencies and series inductances via a CW D-NLTL.

(B1) Excitation of K100F and K50F D-NLTLs using a 700 MHz signal from the R&S amplifier to demonstrate harmonic generation/ (Completed NOV21)

(B2) Demonstrate frequency comb (harmonics) generation in K50F D-NLTL with continuous wave VHF excitation (Completed APR22)

(B3) Perform simulation and experimental studies to measure center frequencies and peak voltage output as a function of source–line and line–load impedances (Completed APR22)

(B3) Simulate topologies capable of utilizing a bipolar pulse for CW applications (Suspended)

(C) Demonstrate UHF generation at single MW power levels with a CW D-NLTL (Suspended due to unavailability of impedance transformer designs).

3.13.5 Methods and Approach

D-NLTL networks were first simulated with LTSpice to determine initial network behavior prior to prototype fabrication. Based on the results, three different D-NLTL prototypes consisting of 20–40 L–C pairs (20–40 cells) were designed with SMV1702, K50F, and K100F diodes. In all the prototypes, air core inductors are used as lumped series inductance. These diodes have been selected based on their steep C–V curves.

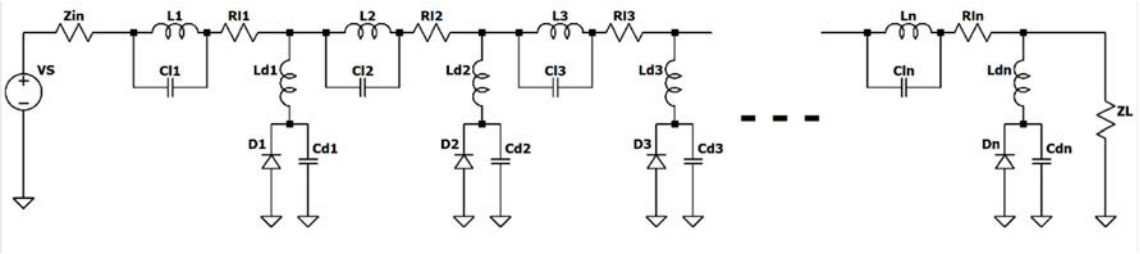


Figure 2. D-NLTL schematic set up for simulation. L_n and D_n represent lumped inductance and diode respectively. C_{ln}, R_{ln}, L_{dn}, and C_{dn} represent losses in the inductor and diode. Z_{in} is the source impedance, and Z_L is the termination impedance.

Figure 2 shows a schematic capture of a D-NLTL circuit in LTSpice. The components labeled C_{ln}, R_{ln}, L_{dn}, and C_{dn} represent sources of losses in the network, Z_{in} represents the impedance mismatch between the D-NLTL and 50 Ω pulse source, and Z_L is the termination impedance. During simulation, transient measurements were collected at the

source, between Z_{in} and L_1, and across Z_L. Iterative simulations altering the series inductance, and source–load and line–load resistances, have been performed to measure the variation in center frequency and peak power as function of each parameter.

Testing was performed with two sources, one of which was in pulsed mode with varying pulse geometry, and the other with a continuous wave (CW) sinusoidal input. Upon performing initial testing and quantifying the impedance mismatch issues in pulsed mode, the testing was extended to include testing with continuous wave excitation using Rohde & Schwarz, and ENI RF pulse amplifiers with 0.7–1.5 GHz and 0.25–150 MHz frequency ranges, respectively, in order to explore potential mitigation solutions. The amplifiers were fed continuous wave sinusoidal input using a Rohde & Schwarz SMB 100A. Figure 3 shows a block diagram of the experimental setup. Each line was first tested with negative polarity excitations produced by the photoconductive semiconductor switch (PCSS) and then with bipolar sinusoidal excitation.

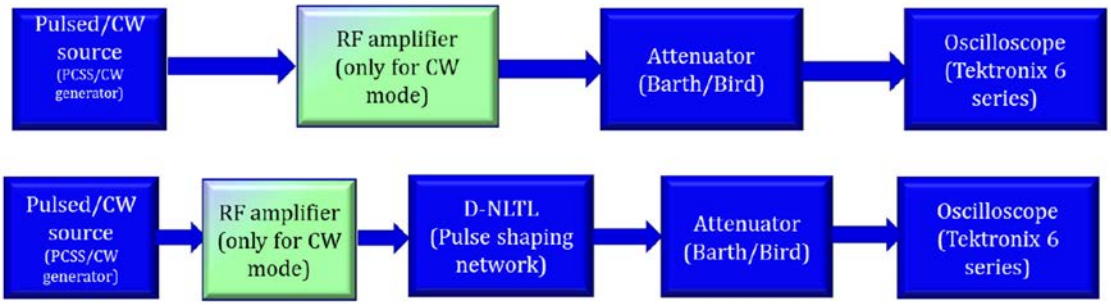


Figure 3. Block diagram of the experimental set up used in each test. (A) Input signal measurement, fed directly from source to the scope via attenuator (B) D-NLTL test setup for measuring D-NLTL characteristics. Appropriate attenuation is used in each case to protect the data collection equipment.

3.13.6 Results and Discussion

Prototypes with K50F diodes were fabricated with two distinct configurations: (i) one diode (1D) per cell and (ii) two diodes (2D) per cell connected back-to-back to increase the break voltage limit. The NLTLs were equipped with 50 Ω n-type connectors on the input and the output ends to facilitate ease of interfacing with the test equipment as shown in Figure 4.

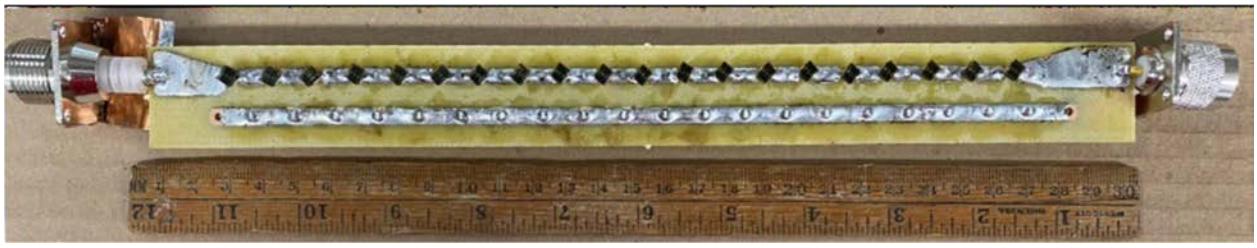


Figure 4. 2D K50F D-NLTL prototype with 50 Ω n-type connectors.

These lines were separately tested using an ENI 3200L RF amplifier capable of 0.25–150 MHz frequencies, for which the excitation input was fed from a Rohde & Schwarz SMB 100A RF pulse generator capable of generating 100 kHz – 20 GHz frequencies. Based on simulation results, the prototypes were tested up to 100 MHz excitation frequencies with 3.3 nH and 6.6 nH series inductors with up to 300 W RF power sourced from an ENI amplifier.

3.13.6.1 K50F D-NLTL with 1 Diode (1D) Configuration:

When tested at 300 V (5 dBm input from 'SMB 100A' fed into ENI 3200 L amplifier with 55 dB gain) peak voltages at frequencies 20–100 MHz with two distinct series inductances 3.3 nH and 6.6 nH, frequencies up to 0.4 GHz have been generated by the D-NLTLs in continuous wave mode. Testing at higher excitation voltages was limited due to the test and probe equipment sensitivity and attenuator limitations. More frequency harmonics were noticed when excited with frequencies between 20–40 MHz. Due to the limitation in *C*(V) curve transition, an increase in excitation frequencies has limited the soliton generation and shifted the NLTL operation to pulse sharpening mode instead of shockwave generation mode. Figure 5 shows the frequency domain diagram of excitation frequencies, while Figures 6 and 7 show the D-NLTL response as a function of excitation frequencies for 3.3 nH and 6.6 nH lines, respectively.

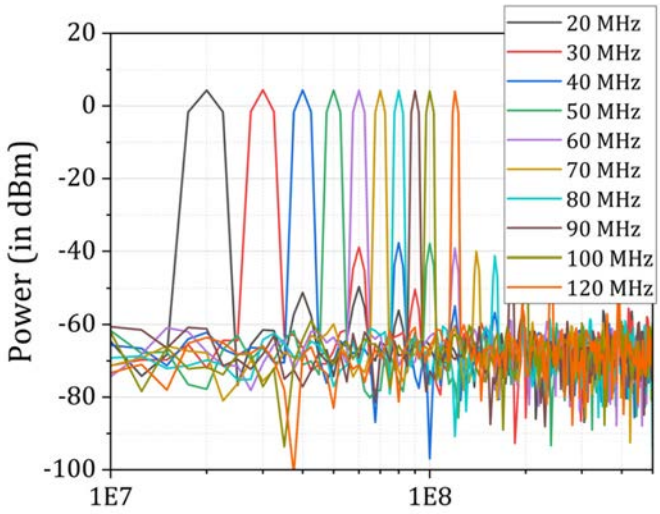


Figure 5 Frequency domain representation of D-NLTL test excitation frequencies.

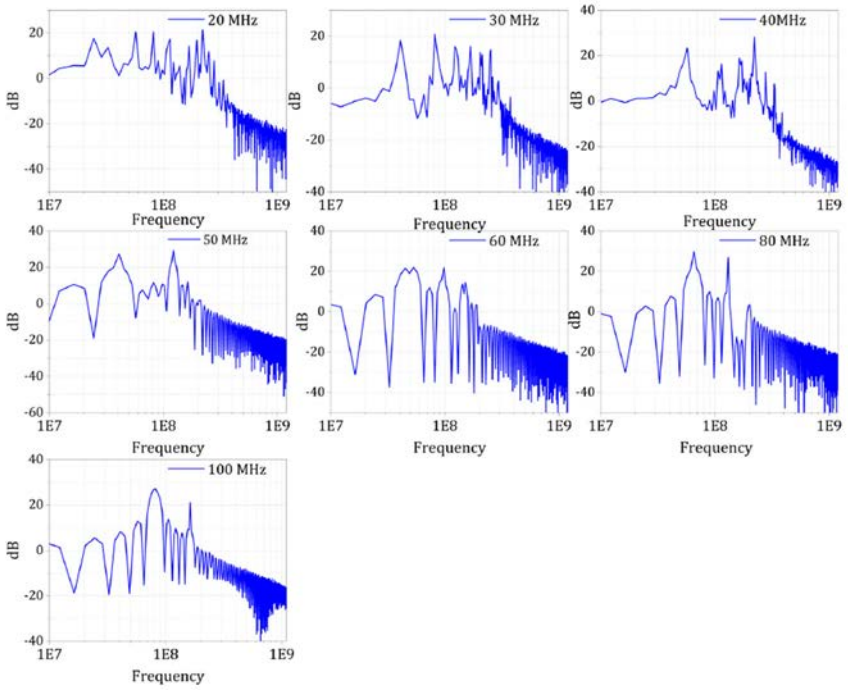


Figure 6 Frequency domain representation for the load characteristics of 1D K50F D-NLTL prototype with 3.3 nH series inductor at excitation frequencies 20–100 MHz.

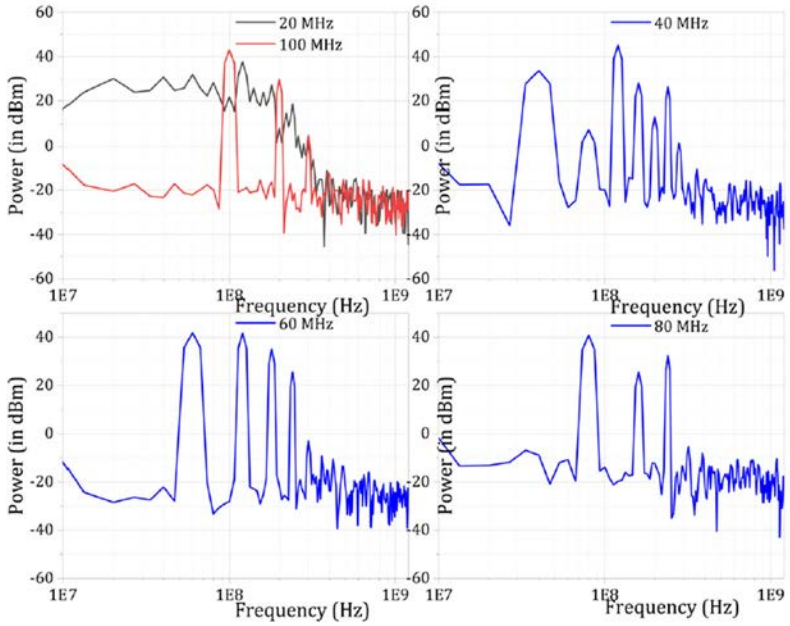


Figure 7. Frequency domain representation for the load characteristics of 1D K50F D-NLTL prototype with 6.6 nH series inductor at excitation frequencies 20–100 MHz.

3.13.6.2 K50F D-NLTL with 2 Diode (2D) Configuration:

In-house testing of a 2D configuration of the K50F D-NLTL yielded similar results as the 1D prototype. The number of solitons generated continued to reduce with an increase in excitation frequency. However, the frequencies and number of harmonics generated in the 2D configuration were noticed to be considerably higher than in the 1D configuration. Though the upper limit of the generated frequencies was 0.4–0.5 GHz, the frequency band spacings were found to be lower in the 2D configuration. The frequency domain representations of the NLTL output are shown in Figure 8

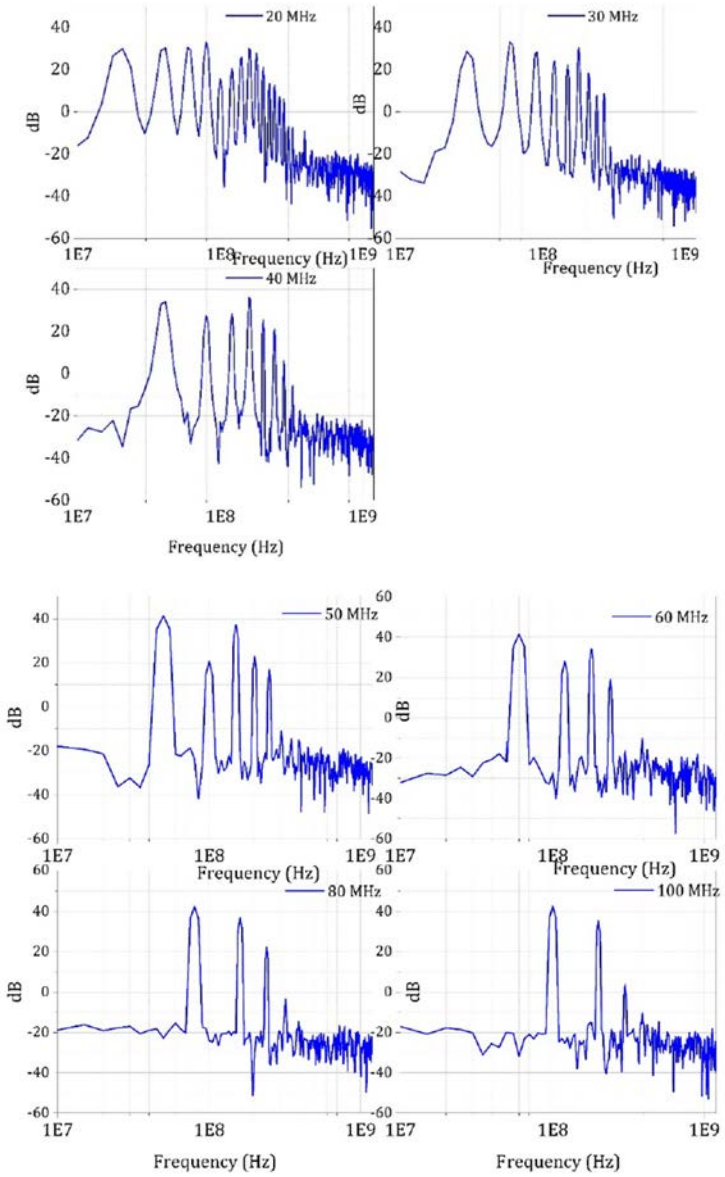


Figure 8. Frequency domain representation for the load characteristics of 2D K50F D-NLTL prototype with 3.3 nH series inductor at excitation frequencies 20–100 MHz.

3.13.6.3 K100F D-NLTL:

Frequency doubling was also observed in the K100F D-NLTL when excited with 700 MHz sinusoidal input at 100 V as shown in Figure 9. Though the efficiency was found to be <7%, output frequencies between 700 MHz and 1.4 GHz have been observed.

Despite the GHz-order frequencies observed in the simulation study, only up to 0.5 GHz frequencies have been demonstrated with <25% efficiency at the load. Power reflection of 45–50% was observed in the RF amplifier at >150 W input power. Simulations showed better peak powers at 3.3 nH inductance impedance matching compared with inductances of 6.6 nH–18 nH. However, when D-NLTL load output was studied as a function of varied source–line and line–load impedances, better voltage peaks were observed with source–line impedance <30 Ω as shown in Figure 10, with 10 Ω showing the best performance.

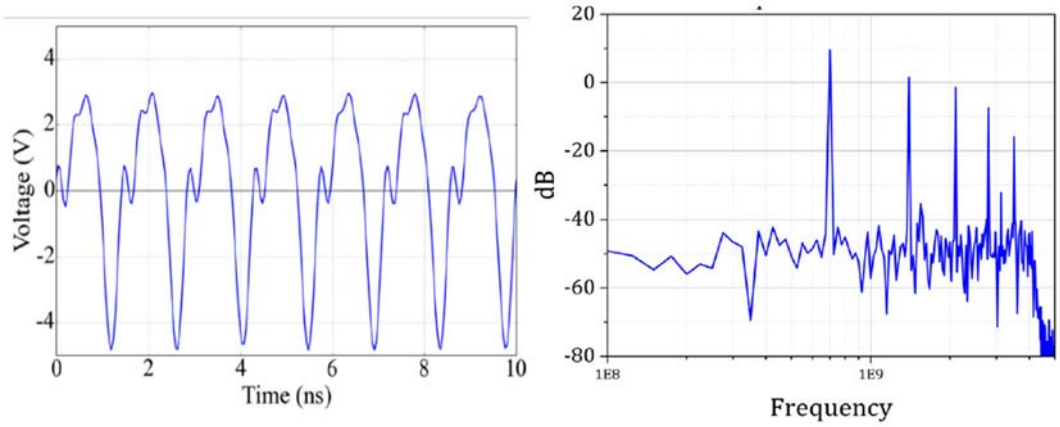


Figure 9. K100F D-NLTL output when excited with 100 V 700 MHz sinusoidal pulse train.

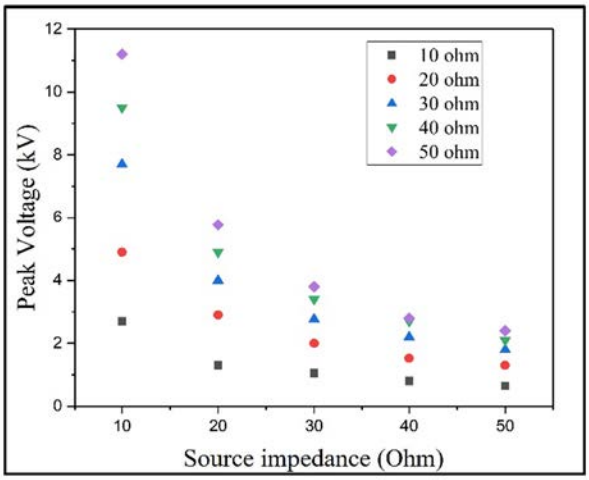


Figure 10. D-NLTL Peak voltage as a function of source–line load–load impedance.

Nevertheless, the NLTLs are typically equipped with 50 Ω connectors to interface with other test equipment. Using a 10 Ω–50 Ω impedance transformer between the n-type connector and the test equipment (pulse source) could be a potential solution to overcome this limitation and improve impedance mismatch at the source–line interface.

3.13.7 Summary and Recommendations

A low voltage (LV) prototype was tested with several CW inputs to observe initial behavior of a D-NLTL with a CW source. Very little improvement on the source–line impedance mismatch was observed for the LV tests.

A high voltage (HV) D-NLTL based on epoxy diodes of model K50F equipped with 50 Ω n-type connectors on source and load ends was tested with sinusoidal excitation with frequencies 20 MHz–100 MHz. Testing was performed using an 'ENI 3200 L' RF amplifier with up to 200 W input power. Output frequencies up to 0.3 GHz were generated with <100 MHz excitation, showing generation of harmonic frequencies. While soliton generation was seen at <100 MHz excitation with ~25% conversion efficiency, a shift in NLTL operation mode was noticed from soliton generation to pulse sharpening (frequency doubling). An inverse relationship was noticed between the number of frequency bands and excitation frequency, implying a need for diodes with steeper C(V) curves. When V_{peak} and f_c were studied computationally as a function of source and load impedances, a highest V_{peak} and f_c were noticed when a combination of 10 Ω and 50 Ω were used at source and load, respectively, while the lowest was noticed with 50 Ω at both the ends. Custom impedance transformer designs are highly recommended to pursue this effort further.

If D-NLTLs are to be implemented to reduce/eliminate the source–line and line–load reflections in CW mode, a 50 Ω to 10 Ω impedance transformer design is recommended to attain impedance matching and to interface the n-type connectors with the NLTL to potentially reduce the impedance mismatch at the load. As the harmonics are a result of rapid capacitance change within the diodes' depletion region, HV diodes with steeper C(V) curves are required to demonstrate higher frequency harmonics.

3.13.8 Outputs

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3.14 Dynamically Tunable Multi-Frequency Solid-State Frozen Wave Generator

(John Bhamidipati)

3.14.1 Executive Summary

An all-solid-state compact multifrequency generator with chirp-capability and dynamic tunability was proposed as an attempt to overcome the limitations of the conventional RF pulsers in terms of form factor, frequency response, waveform tunability, and power conversion efficiency. Historically, frozen wave generators (FWGs), a sub-class of RF pulsers, were studied to address the aforementioned limitations, but their experimental realization implementing sparkgaps and coax-based distributed element transmission lines (DETLs) limited the system weight, reliability, form factor, and frequency tunability. The primary goal of the effort was to replicate the literature-standard coax-based FWG with varied coaxial cable lengths to demonstrate chirped pulse widths and extend the work by replacing the DETL system with lumped-element-based TLs (LETLs) to achieve SWaP optimization. SiC MOSFET-switched FWG prototypes for DETL- and LETL-based FWGs were implemented, where the lumped-element parameters such as inductance and capacitance for LETLs were adapted from the literature-standard DETLs with a velocity factor of 0.66.

Upon demonstrating the LETL-based FWG, the chirp- and dynamic-tuning-capability of an all-solid-state FWG was realized on a 7.5-cm × 30-cm × 3-cm printed circuit board via a 12-segment LETL embodiment. Dynamically tunable pulse trains with 15–24 ns pulse widths (40–80 MHz) were demonstrated with >35% pulse conversion efficiency with $<2\times10^{-4}$ m^3 volume, yielding >80% reduction in volume compared with vacuum-relativistic pulsers, and 60% reduction in weight compared with coax-based FWG system.

However, the transient characteristics of the enabling switch (MOSFET) in terms of t_{rise} and t_{fall} were noticed to be the limiting factors to attain flat-top pulse trains. Furthermore, a need for >11 ns pulse width/delay to be compatible with rated t_{rise} of the MOSFET capped the frequency response of the pulser at <100 MHz. A solid-state switch analogous to photoconductive solid-state switches (PCSSs) capable of sub-ns t_{rise} with low jitter and compact trigger mechanism would greatly benefit the solid-state LETL topology of the FWG.

3.14.2 Objective

Demonstrate a compact single PCB-mount, all-solid-state multifrequency generator capable of DC-to-RF pulse conversion with chirp capability and dynamic (electronic/mechanical) frequency tunability, and 30% or more power conversion efficiency, yielding >75% reduction in form factor compared with conventional microwave pulsers.

3.14.3 Technical Background

A pulse generator or a pulser is either an electronic circuit or a piece of electronic test equipment capable of generating rectangular pulses. Sources capable of generating RF pulses from DC energy find applications in the pulsed power domain for microwave and millimeter-wave pulse generation, plasma physics, radar, time domain metrology, etc. Historically, equipment like vector inversion generators (VIG), quarter wave transmission-line-based oscillators, and lumped-element L-C oscillators have been typically implemented for generating frequencies <500 MHz [2]. The frequency of oscillation for such devices is inversely proportional to the square root of the product of the capacitance (C), and the inductance (L) (frequency $\propto \frac{1}{\sqrt{LC}}$). For frequencies >500 MHz, the capacitance and inductance required for discrete LC oscillators are so small that stray effects tend to dominate and limit the attainable frequency. In the microwave region of the spectrum, devices like vircators, backward wave oscillators, relativistic magnetrons, etc. are used [2]. While VIGs configured as oscillators and lumped-element NLTLs are capable of generating pulses with center frequencies of 500 MHz and 1.2 GHz, respectively, they are limited by <12% efficiency. These pulsers are typically large, making them infeasible to deploy in compact and portable payload spaces. In general, the wave packet generated by these techniques consists of a decaying sinusoid of a few cycles with only one or two of the cycles having high peak power.

A frozen wave generator (FWG) is an alternative technique investigated for years by researchers such as Forcier *et al*.,[1] Gripshover *et al*.,[3] Best *et al*.,[2] Holzman *et al*.,[7] and Weibel *et al.,* [8] to overcome drawbacks in conventional microwave pulse generators by exploiting the ability of this device to generate a square-top, constant-amplitude, multi-cycle waveform of user-defined pulse width, covering tens-of-MHz to sub-THz center frequency range with scalability to MW-order powers in the RF domain.

A classical FWG consists of a linear, multi-switch ensemble of TL segments with alternate segments charged to opposite polarity, constituting a single cycle, as shown in Figure 1. Multiple pairs of segments, each with an enabling switch, are connected in series to generate a stream of RF pulses with a fixed center frequency and a narrow bandwidth. Simultaneous closure of all the switches converts the spatially stored electrostatic charge distribution to dynamic “traveling” waves moving through the line segments in opposite directions toward the load. The length of each TL segment is one-half of the wavelength of the desired radiation. In this arrangement, energy from a power supply is statically stored in alternately charged sections of the transmission lines with constant characteristic impedance Z_0 and requires ‘(n–1)’ switches for ‘n’ segments of TLs to produce ‘n/2’ cycles of RF pulses.

For years, multi-switch embodiments of FWGs have been implemented using coax-based TLs, alternately connected to two equal valued DC power supplies (one positive and one negative) to enable bipolar pulse generation as shown in Figure 1. The primary drawbacks of the initial FWG embodiment are (i) the need for a separate switch between each pair of segments and (ii) their fixed center frequency. With multiple switching

elements regulating the transmission line charge–discharge cycles, a few significant challenges associated with the synchronization need to be addressed to efficiently generate low-jitter RF pulses. These include synchronization of sub-nanosecond switching, external trigger, and sub-nanosecond switch impedance collapse (requires comprehensive characterization of individual switches to match the parameters exactly).

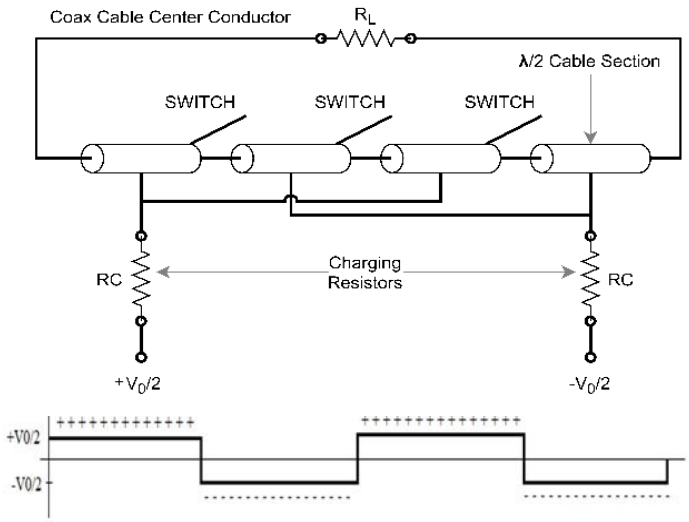


Figure 1. Circuit configuration of a two-cycle FWG (transmission line is replaced by a coaxial cable)

To elude this complexity, Forcier implemented a single-switch-enabled folded FWG topology where alternate coaxial transmission lines charged by a positive power supply are connected to one end of the switch, and the other set of alternate transmission lines charged by a negative power supply are connected to the other end of the switch. However, the center conductor of the coaxial transmission lines remains continuous throughout all the line segments as shown in Figure 2. This folded topology implemented by Best et al. and Forcier et al. offers an additional advantage of reduced switching loss that affects the first half cycle of the output pulse. Despite successful implementation of the folded topology, the use of coaxial cables limited the ability to tune center frequencies dynamically. Furthermore, Best and Forcier implemented modified stab switches and spark gaps, respectively, which were suboptimal due to their switching speeds, jitter, and device lifetime.

Typically, 50 Ω coaxial cables are used to facilitate impedance matching with the load, which is usually a radiating antenna. These cables have a velocity factor (v_f) of 0.66, capable of generating pulse widths of 5.05 ns for every meter of the coaxial cable used. Though this approach reduced the synchronization complexities, the coaxial cables with fixed lengths result in fixed pulse widths, making it infeasible to tune the frequency bands.

However, if the pairs of transmission line segments are varied in length discretely for *n*-segments, at sufficiently high *n*, a chirped output pulse train with smoothly varying $\lambda/2$ in

the time domain and a moderately smooth frequency space can be realized. Forcier et al. have demonstrated this technique using coaxial cables, but the number of pulses realized experimentally was limited to 3 [1], [5]. Furthermore, if the transmission lines are made to be remotely tunable, the center frequency and the bandwidth of the system can be dynamically tuned. FWGs capable of chirped pulse widths and dynamic tunability can potentially broaden the application space of the FWG, making it a one-size-fits-all solution for pulser needs without the use of a vacuum-electron source.

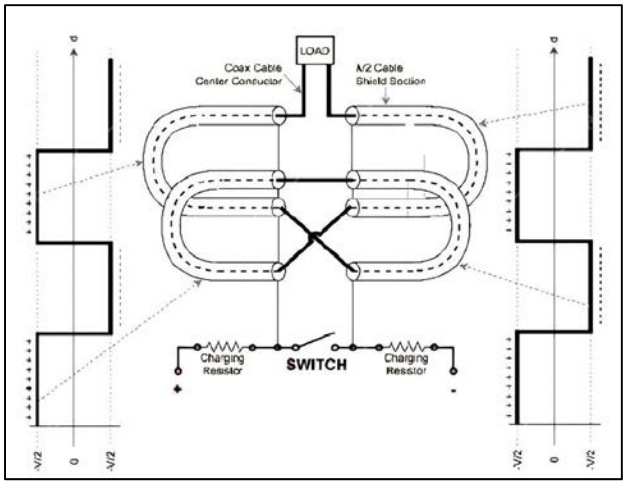


Figure 2. Basic architecture of a folded frozen wave generator.

3.14.4 Tasks, Milestones, and Status

A. Simulate a chirp-capable distributed-element transmission-line-based (DETL) 16-stage frozen wave generator (FWG) with balanced and unbalanced load configurations. [JUN–JUL 2021 / complete]

B. Demonstrate a SiC-MOSFET-powered FWG prototype on a custom-built PCB with Cree/Wolfspeed MOSFET, and 50 Ω coaxial cables and/or microstrip transmission lines capable of generating chirped pulse widths. [JUL–AUG 2021 / complete].

C. Simulate a lumped-element transmission line (LETL) based FWG with up to 12 segments to replicate results from the DETL-FWG simulations. [AUG–SEP 2021 / complete]

D. Demonstrate a modular 4–8 stage SiC-MOSFET enabled FWG with lumped-element-based transmission lines with and without chirp capability. [SEP–OCT 2021 / complete]

E. Design and test a 12-segment, MOSFET-enabled FWG prototype with dynamic pulse width tunability using lumped-element-based transmission lines [NOV–DEC 2021 / complete].

F. Perform root cause analysis to determine the causes for (i) pulse overlap demonstrated by the Gen1 LETL-FWG prototype under unbalanced load configuration, and (ii) consistent reduction in the peak voltage output of the pulse train output. [JAN–FEB 2022 / complete]

G. Demonstrate motorized and/or electronically tunable DETL-FWG prototype with dynamic tunability capable of generating multiple center frequencies. [MAR–APR 2022 / suspended]

3.14.5 Methods and Approach

The DETL and LETL based FWG topologies were implemented computationally and experimentally under balanced and unbalanced load configurations. The literature-standard folded coaxial topology (DETL) reported by Forcier and Best [1–2, 4–5] was realized with Cree/Wolfspeed SiC MOSFET(C2M1000170D) to establish the baseline measurements for the FWG and to calculate inductance and capacitance of the DETLs as a function of coax length. These parameters were used in the lumped-element TLs (LETLs) to mimic the behavior of the DETL-FWG characteristics with a reduced form factor. The design was modified for a 12-segment LETL-FWG to optimize the pulse widths/delays and enable dynamic tunability by including a tunable L-C pair in each LETL. The design specifics are discussed below.

Distributed Element Transmission Line based FWG (DETL-FWG):

A 16-stage, chirp-capable, MOSFET-switched FWG shown in Figure 3 was modeled in LTSpice with two load resistors, R_L and R_T. In simulations, TL segments capable of pulse widths between 0.5–3 ns were used to demonstrate chirp capability from 0.3–2 GHz. FWG performance is studied with two load configurations: (i) balanced (R_L=R_T), and (ii) unbalanced (R_L>> R_T), respectively. Given that the path of traveling waves in (i) and (ii) were distinct, crossover distortion was avoided by implementing a horizontal symmetry of TL segments for the balanced load configuration as shown in Figure 3(a), and a diagonal symmetry for unbalanced load as shown in Figure 3(b). TL segment arrangement can be distinguished by the naming convention.

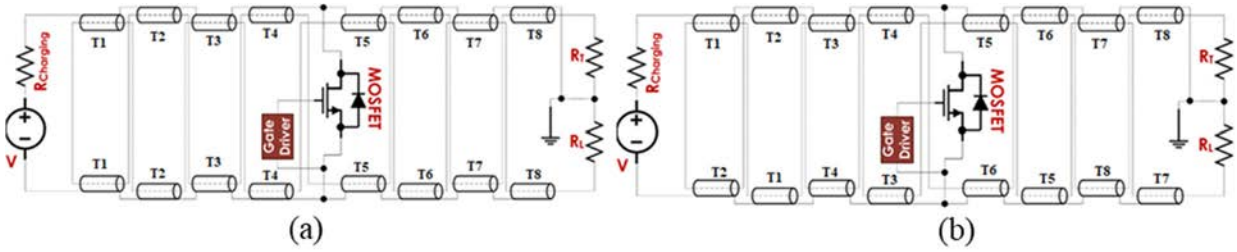


Figure 3. (a) A 16-stage symmetric FWG (R_T=R_L), and (b) an asymmetric FWG (R_T<< R_L), with programmable delay and ON-time.

Experimentally, the DETL-FWG topology was realized through a MOSFET-switched prototype implemented using 50 Ω coax-based TL segments with a 0.66 velocity factor. The MOSFET was rated for 10.5 ns rise-time (t_{rise}), 60 ns fall-time (t_{fall}), 1.7 kV

drain-source voltage, and 1 Ω drain-source on-state resistance (R_{DS}(on)); driven by a Texas Instruments UCC5390Q1 gate driver. The implemented coaxial cable demonstrates 5.05 ns t_{pulse}/t_{delay} per meter. Figure 4**Figure** shows an 8-segment DETL-FWG prototype implementing four coaxial pairs of lengths 5-, 4-, 3- and 1-meters, inducing propagation delays of 25 ns, 20 ns, 15 ns, and 5 ns, respectively.

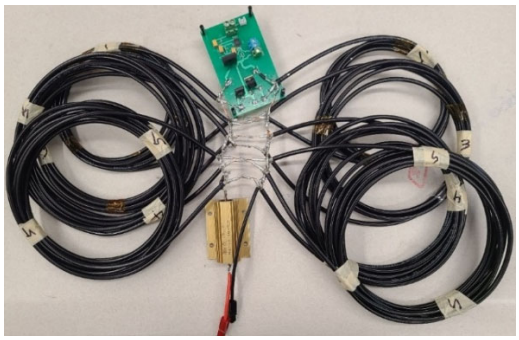


Figure 4. An 8-segment coax-based chirp-capable SiC-MOSFET-driven FWG.

Lumped-Element Transmission Line based FWG (LETL-FWG)

The DETL topologies yield length-dependent, non-tunable pulse widths that subsequently limit the application trade space of the FWGs. In addition, high-power, high-frequency DETLs are bulky and heavy with limited flexibility to minimize the form factor. To address said limitations, LETL-based FWG was designed using lumped-elements, where t_{pulse} and t_{delay} depend on the L and C parameters instead. Each TL segment was equipped with an ensemble of fixed LC cells and one tunable LC cell. Similar to DETL-FWG design, it employs a SiC-MOSFET and a UCC5390Q1 driver. The L and C parameters for each cell were precisely selected to maintain a 50 Ω characteristic impedance in each LETL segment. With L-C combination of 75 nH-30 pF generating 1.5 ns t_{pulse}/t_{delay}, their multiples were selected for LETL cells. The t_{pulse} of each segment can be tuned individually by varying the L and C parameters in the tunable cell(s), which subsequently tunes the center frequency (f_c).

3.14.6 Results and Discussion

A chirp-capable coax-based design was implemented with 4-, and 8-segment TL topologies under balanced and unbalanced load configurations.

A four-segment FWG topology implemented with two coax cables of 4 m each, and the other two of 5 m each demonstrated ~20 and ~25 ns pulse widths, respectively, under balanced and unbalanced load configurations with chirp based on the lengths of the coaxial cables. A center frequency of ~20 MHz was noticed in the unbalanced load configuration for the unipolar pulse train generation with voltage swings between +160 and –220 V, while in the balanced load with bipolar pulse train generation, it was noticed to be ~ 75 MHz with voltage swings between –170 and +170 V as shown in Figure 5. Furthermore, when the number of TL segments is increased to eight with coax pairs of

lengths 5, 4, 3 and 1 m, a significantly lower peak voltage swing was observed alongside ringing towards the tail with frequencies chirping between 15 and 70 MHz were noticed.

With an increase in number of transmission line segments, an increase in pulse overlap and pulse deformation due to deconstructive interference was noticed under unbalanced load conditions, and the load measurements start to deviate from the expected waveform when the number of segments is >8. Significant ringing was observed when 8 and more TL segments were used under balanced load conditions, caused due to the impedance mismatch between the transmission line ensemble and the load.

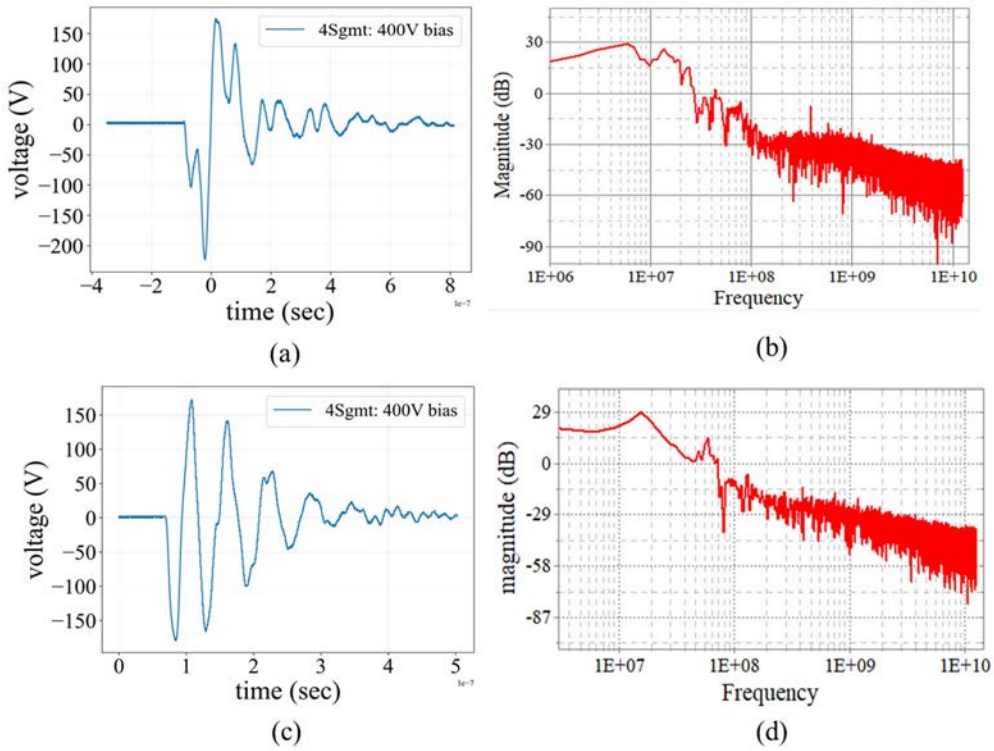


Figure 5. (a) 4-segment FWG load characteristics under unbalanced load, (b) frequency domain representation of (a), (c) 4-segment FWG load characteristics under balanced load, and (d) frequency domain representation of (a).

Extending the literature-standard work, LETL-FWG prototypes were experimentally verified for eight-, and twelve-segment configurations under balanced and unbalanced loads using folded FWG topology with one power supply and switched using a Cree/Wolfspeed C2M1000170D SiC-MOSFET. The LC parameters were selected such that the characteristic impedance of the line is maintained at 50 Ω, while waveform tunability was introduced in the 12-segment FWG prototype by including a mechanically-tunable inductor capacitor pair (highlighted in red) in each transmission line segment as shown in Figure 6.

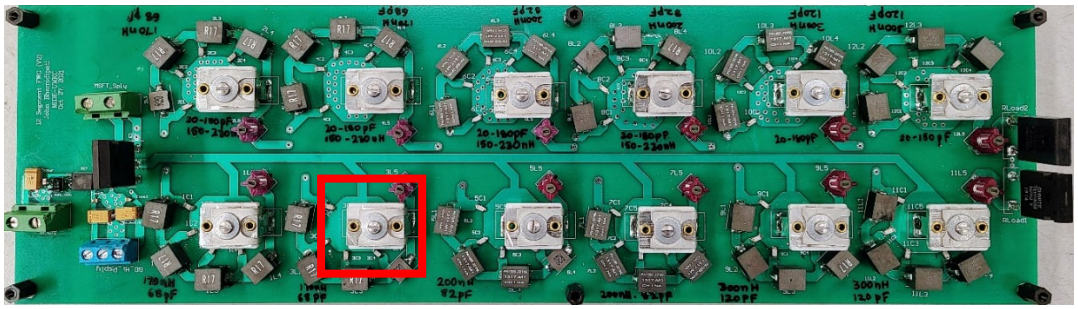


Figure 6. Twelve-segment dynamically-tunable LETL-FWG prototype switched using Cree/Wolfspeed C2M1000170D MOSFET, driven using a Texas Instruments UCC5390Q driver.

In the 8-segment FWG, 4 segments were loaded with 4 cells of 270 nH – 102 pF each and the other 4 were loaded with 4 cells of 150 nH – 62 pF, capable of generating 21 ns and 12 ns pulse width/delay, respectively. When tested at 400 V under unbalanced configuration, issues with pulse overlap were noticed. Though the pulse train in one polarity represented the expected waveform from the simulations, the reflected waveform failed to demonstrate similar properties. A significant pulse-train overlap has been noticed in the unbalanced load configuration. Despite demonstrating the center frequencies >70 MHz, the unbalanced load configuration demonstrated pulse overlap due to the non-aligned charge–discharge cycles of the LETLs, limiting the frequency content of the FWG.

A twelve-segment Gen-I non-chirp-capable prototype (shown in Figure 6), when tested at 400 V bias under balanced load configuration with 4 cells of 300 nH – 120 pF in each segment has shown a consistent temporal waveform in-line with the simulation results. However, a consistent drop in the peak voltages has been observed under balanced load as shown in Figure 7. With an increase in the number of TL segments, the inability of the MOSFET to perform simultaneous switching of all the transmission lines has been elevated, leading to decreased charge time due to delayed opening and prolonged high-charge state due to delayed closing. The placement MOSFET at one end of the FWG was speculated to be the root cause, leading to switching delays.

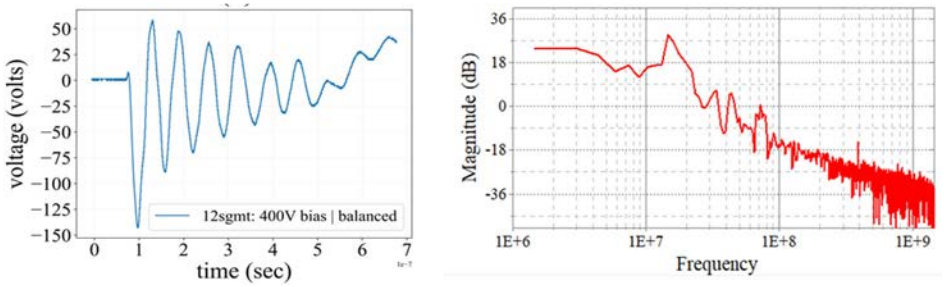


Figure 7. (left) Load characteristics of a 12-segment fixed pulse width LETLs with 4× 300nH-120pF LC ladder cells in each segment, capable of generating 24 ns pulse width, (right) frequency domain representation.

To confirm this speculation, a Gen II 12-segment FWG was designed with modified MOSFET placement as shown in Figure 8 to minimize switching delays. The characteristic impedance of the LC ladder networks was set to 50 Ω and the fixed LC components were selected to generate pulse widths between ~13 and ~24 ns, and additional tunable LC components in each segment add 2 – 5 ns. Anticipated pulse width(s) were measured under balanced (50 Ω and 50 Ω) load configuration as shown in Figure 9.

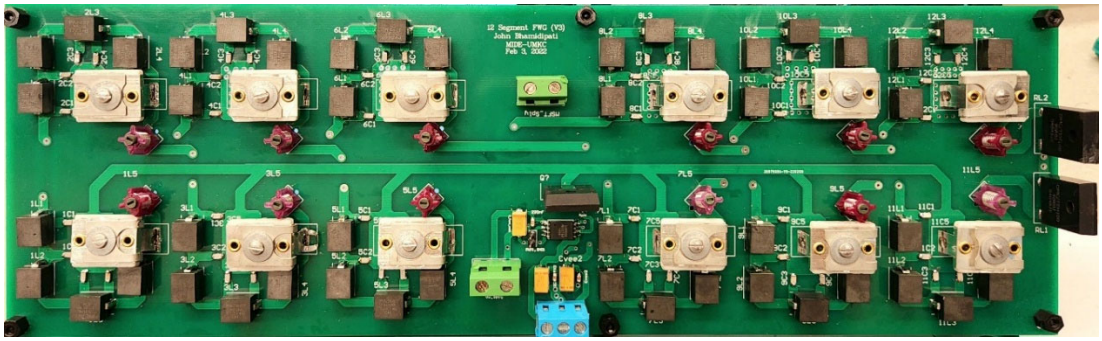


Figure 8. Gen 2 prototype with modified MOSFET and gate driver layout.

Nevertheless, the Gen II prototype with updated MOSFET (results shown in Figure 9) did not show a significant improvement in peak voltage trends of the output wave packet. The rise-time of the MOSFET being ~10.5 ns is determined to be too slow to perform simul-switching of the transmission lines, raising a need for a switch with sub-ns rise-time and ns-order fall-time.

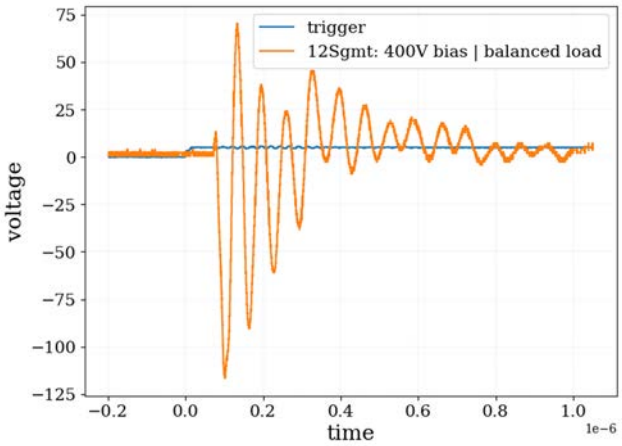


Figure 9. 12-segment balanced load FWG output when the lines are charged to 400 V. Each transmission line segment has been loaded with 4x 300nH-120pF LC ladder cells, capable of generating 24 ns pulse width.

Switches such as PCSSs and drift step recovery diodes (DSRDs) with sub-ns pulse characteristics can be potentially implemented to address this limitation if a compact,

lightweight trigger mechanism is developed. Furthermore, remote tunability can be made possible by including an MCU/ECU controlled tunable L-C pair in each TL segment.

3.14.7 Summary and Recommendations

The chirp- and dynamic-tuning-capability of an all-solid-state FWG was realized on a 7.5-cm × 30-cm × 3-cm printed circuit board via a 12-segment LETL embodiment. Dynamically-tunable pulse trains with 15–24 ns pulse widths (40–80 MHz) were realized with >35% pulse conversion efficiency at $<2\times10^{-4}$ m^3 volume, yielding >80% reduction in volume compared with vacuum-relativistic pulsers. Replacing the DETLs in literature-standard coax-based topology with lumped elements enabled tunability, enhanced robustness, and yielded >60% reduction in size and weight. Transient characteristics of the enabling switch (MOSFET) in terms of t_{rise} and t_{fall} were noticed to be the limiting factors to attain flat-top pulse trains. Furthermore, a need for >11 ns pulse width/delay to be compatible with rated t_{rise} of the MOSFET capped the frequency response of the pulser at <100 MHz. A solid-state switch analogous to PCSS capable of sub-ns t_{rise} with low jitter and compact trigger mechanism would greatly benefit the solid-state LETL topology of the FWG.

3.14.8 Outputs

3.14.8.1 Journal Publications

J. K. P. Bhamidipati, K. C. Durbhakula, and A. N. Caruso, “A Dynamically Tunable Discrete-Element Transmission Line Pulse Generator,” *International Journal of Electronics and Communications*, Submitted March 6 **2022**, Manuscript ID#AEUE-S-22-01270.

3.14.8.2 Dissertation

John Keerthi Paul Bhamidipati, “Pulse Generation, Shaping, and Optimization Solutions for Solid-State-Switch-Enabled High-Power Microwave Generation Systems” PhD Dissertation in Physics and Electrical Engineering, University of Missouri-Kansas City, **2022**.

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3.15 Pulse-Compression-Based Signal Amplification

(Feyza Berber Halmen)

3.15.1 Executive Summary

Magnetic pulse compression (MPC) and time-reversal based pulse compression (TR-PC) were evaluated, as an alternative to power combining with solid-state amplifiers (SSAs), to increase the available output power (P_{out}) in a high power microwave (HPM) system within SWAP-C2 requirements. The MPC was shown to theoretically provide a 17 dB increase in the instantaneous P_{out}, up to a few hundred MHz. The achievable gain is strongly dependent on the magnetic core material properties. The restrictions imposed by available magnetic materials and properties required for high frequency operation were documented. A material development proposal based on MPC requirements was prepared with KRI. The initial study of TR-PC suggests that gain is achievable with pulsed power operation; collaboration with NRL is on-going on feasibility study of TR-PC – SSA integration.

3.15.2 Objective

Solid-state amplifiers, such as gallium-nitride-based high electron mobility transistors (GaN HEMTs), can be used as high power microwave (HPM) sources to achieve the SWAP-C2 performance metrics necessary to support the cUAV Naval afloat mission. However, even the best high-power GaN HEMTs are limited to 2–3 kW of peak power, much lower than the 0.1 to 3 MW pulsed power available from traditional HPM sources such as travelling wave tubes (TWTs). Achieving a power density of 1 W/cm^2 at a distance of 10 m with a high gain (≥ 10 dBi) narrow-band antenna requires an input power increase of two to three orders of magnitude. Power combination methods to achieve an effective radiated power (ERP) at MW scale require 10 s to 100 s of GaN HEMTs, compromising the SWAP-C2 performance.

Pulse compression techniques are used to increase the peak power and lessen the pulse width in HPM applications. Adapting pulse compression at the GaN HEMT or any other SWAP-C2 compatible source output can achieve the required ERP if the gain is ≥10.

Pulse compression is generally used to generate a pulsed output with a high peak output power and a wideband frequency content from a DC or AC (50/60 Hz) high voltage supply, such as in magnetic pulse compression (MPC), or from an impulse, as in time-reversal based pulse compression (TR-PC). The main challenge lies in identifying a pulse compression technique that can be used to amplify a narrowband RF input signal. Some of the circuit elements for common pulse compression techniques, such as the saturable inductors used for energy storage in MPC, exhibit increasingly lossy behavior with high frequency. Another challenge is to determine the operating frequency limits of the suitable pulse compression technique for high-frequency, high-power signals.

Large MPC circuits (>1 m^3, >1000 lbs) have demonstrated peak output power up to a few GWs. Smaller versions (~0.125 m^3, 50 lbs to 100 lbs) can achieve 7.5 MW peak power

[1]. Traditional MPC systems are large, leverage huge transformers, and require liquid coolant such as transformer oil, which leads to undesirable system mass values of ≥1000 lbs. There is no known example of high-frequency signal amplification utilizing MPC.

3.15.3 Technical Background

3.15.3.1 Magnetic Pulse Compression

Magnetic pulse compression (MPC) [2-4] is based on resonant energy transfer and magnetic switching. Figure 1 shows the basic two-stage MPC circuit, its states during operation, and the resulting waveforms. Each stage in the MPC circuit consists of an input and output capacitor with a saturable inductor in between. Once the input capacitor is charged to the desired voltage, the energy is resonantly transferred to the output capacitor. The timing of the resonant energy transfer depends on the LC time constant of the stage and gain is achieved by scaling the resonance time of different stages. The saturable inductor, i.e., the magnetic switch, can be considered as a switch and an inductor in series. However, due to short resonance times and high voltage or current values, generally only the input stage saturable inductor can be replaced with such components.

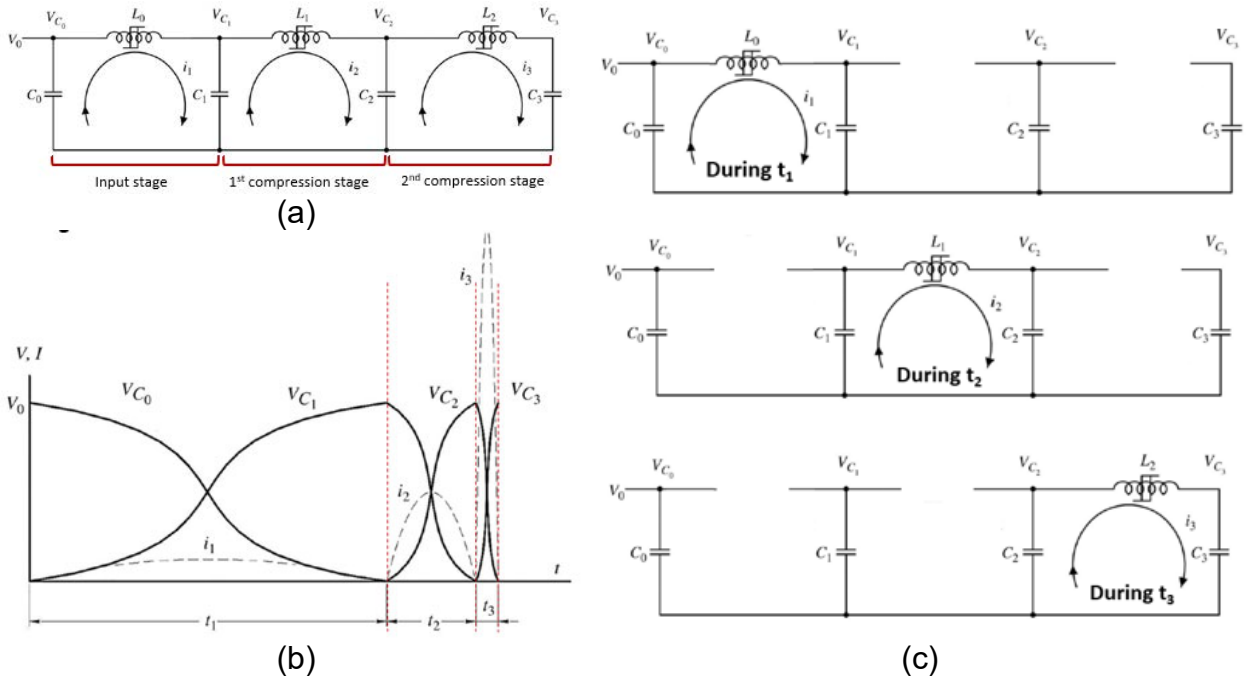


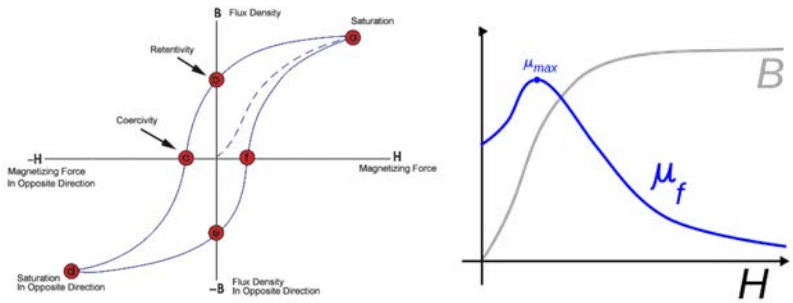
Figure 1. Two-stage MPC circuit (a) schematic, (b) expected waveforms, and (c) ideal states during its operation (adapted from [4]).

The magnetic switch is basically an inductor with a saturable magnetic core, and it utilizes the large impedance change due to magnetic core saturation. A saturable magnetic core exhibits hysteresis in its magnetic flux density (B) in response to an applied magnetizing force (H), as depicted in Figure 2, and its flux density approaches a maximum value, i.e.,

saturates, at high applied fields. As the slope of the B–H curve is the permeability (μ) of the material (B = μH), a saturable magnetic core has two distinct permeability values: its relative permeability (μ_r) is high when it is not saturated but approaches 1 when it is saturated. Given the general equation for inductance:

$$L = \frac{\mu_r \mu_0 N^2 A_e}{l_e}, \tag{1}$$

an inductor constructed from such a material has high impedance determined by its μ_r when it is not saturated, resulting in isolation between stages like an open switch. During saturation it acts like an air core inductor, through which the input capacitor discharges. This behavior results in the circuit states shown in Figure 1(c) during MPC operation.



(a) (b)

Figure 2. (a) Typical B-H curve of a saturable magnetic core and (b) the change in relative permeability (μ_r) with magnetizing force (H) (adapted from [5]).

Assuming only the input stage inductor is saturated, the circuit equation for MPC input stage can be written from KVL as:

$$\frac{1}{C_0}\int i_1(t)dt + L_{0,sat}\frac{di_1(t)}{dt} + \frac{1}{C_1}\int i_1(t)dt = 0 \tag{2}$$

From the initial conditions $i_1(t) = 0$ and $L_{0,sat}\frac{di_1(t)}{dt} = V_0$, the solutions for $i_1(t)$ and $v_{C1}(t)$ are:

$$i_1(t) = \frac{V_0}{L_{0,sat}\omega_0}\sin\omega_0 t \tag{3}$$

$$v_{C1}(t) = \frac{V_0}{C_1 L_{0,sat}\omega_0^2}(1 - \cos\omega_0 t) \tag{4}$$

where ω_0 is defined as:

$$\omega_0 = \sqrt{\frac{1}{L_{0,sat}C_{01}}} = \sqrt{\frac{1}{L_{0,sat}}\left(\frac{1}{C_0} + \frac{1}{C_1}\right)} = \sqrt{\frac{C_0 + C_1}{L_{0,sat}C_0 C_1}} \tag{5}$$

For C_1=C_2=C, the maximum current and maximum voltage at the input stage are:

$$I_{1,max} = V_0\sqrt{C/(2L_{0,sat})} \quad \text{at} \quad t = \pi/2\omega_0 = \pi/2\sqrt{L_{0,sat}C/2} \quad (\text{from } \sin\omega_0 t = 1) \qquad (6)$$

$$V_{c1,max} = V_0 \quad \text{at} \quad t = \pi/\omega_0 = \pi\sqrt{L_{0,sat}C/2} \quad (\text{from } 1 - \cos\omega_0 t = 2) \qquad (7)$$

The same equations are used for the next stage, under the assumption that its saturated inductance is much smaller than the inductance of the preceding and subsequent stages during its operation. This is ensured by using saturable inductor L_n designed to saturate at the time $t = \pi\sqrt{L_{n-1,sat}C_{(n-1)(n)}}$, when the input capacitor C_n is charged to its maximum value. Therefore, smaller saturated inductances are used for subsequent stages, resulting in shorter time constants and higher maximum currents as given by Equations (7) and (6), respectively. Compression gain is defined as the ratio of time constants:

$$G = \frac{t_0}{t_1}\frac{t_1}{t_2}\ldots\frac{t_{n-1}}{t_n} = \frac{t_0}{t_n} = \sqrt{\frac{L_{0,sat}}{L_{n,sat}}} \qquad (7)$$

which reduces to the ratio of number of windings, N_0/N_n, for the same inductor material and geometry. Generally, N = 1 for the last stage to maximize gain. Voltage, instead of current, amplification can be obtained by scaling the capacitors instead of the inductors. However, this is not a preferred method in MPC design due to its low energy transfer efficiency [3,4].

Flux density through an inductor can be altered by flowing current through it or applying voltage to its windings, governed by Ampere's and Faraday's laws, respectively. Given:

$$\varepsilon = -N\frac{d\phi}{dt} \quad \text{and} \quad \phi = B \cdot A_e, \qquad (8)$$

The relation between the applied voltage and the flux density swing is obtained as:

$$\int_0^t V dt = \Delta B \cdot N \cdot A_e \qquad (9)$$

For the saturation of the inductors in the MPC circuit depicted in Figure 1, the flux density should increase to the magnetic material's B_{sat} value during time to saturation, t_{sat}, yielding the saturation condition:

$$\int_0^{t_{sat}} V dt = \langle V_c \rangle \cdot t_{sat} \geq B_{sat} \cdot N \cdot A_e \qquad (10)$$

The total voltage applied to the inductor L_1 at $t_0=\pi/\omega_0$, the time to saturation required for accurate MPC operation, is calculated from (4) and (5) as:

$$\langle V_{c1} \rangle t_0 = \int_0^{\frac{\pi}{\omega_0}} \frac{V_0}{2}(1 - \cos(\omega_0 t)) = \frac{V_0}{2}\frac{\pi}{\omega_0} = \frac{V_0}{2}\pi\sqrt{L_{0,sat}C/2}. \qquad (11)$$

The traditional MPC circuit depicted in Figure 1 only involves unipolar waveforms and the inductors are saturated only in the positive direction. To avoid flux build-up, each inductor

needs to be reset using an external circuitry after their saturation time [6]. This adds extra complexity to the circuit, especially in terms of timing control.

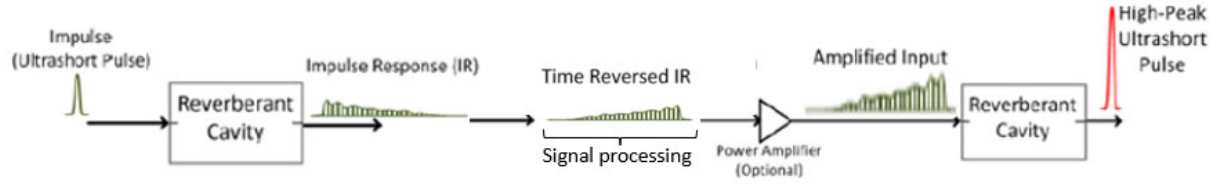
Finally, if the output capacitor is replaced with a resistor in Figure 1(a), the resistive load impedance should match with the pulse forming network characteristic impedance, Z_0, for optimum power transfer:

$$R_L = Z_0 = \sqrt{\frac{L_{2,sat}}{C_2}} \tag{12}$$

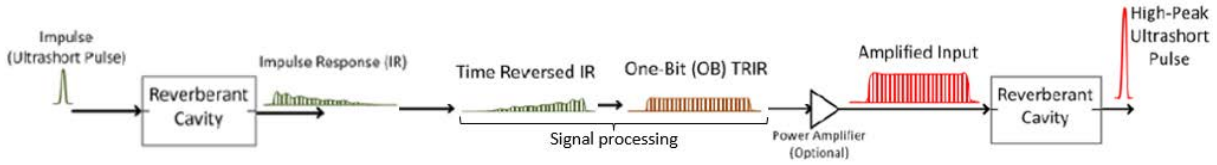
For a matched load, the voltage at the load is halved, $V_0/2$, and the current is reduced to $V_0/2Z_0$., effectively reducing the compression gain and instantaneous power.

3.15.3.2 Time-Reversal Pulse Compression

The time-reversal pulse compression method utilizes a resonant cavity and signal processing to generate a high-peak ultrashort pulse from an impulse [7,8]. Figure 3(a) shows the architecture for the time reversal pulse compression system. An ultrashort pulse is applied to a reverberant cavity, and the recorded impulse response (IR) is time reversed and re-applied to the same cavity. A reconstructed pulse, with higher peak power, is obtained at the output of the cavity. For the impulse response record time T, the reconstructed output pulse is formed at t = T, indicating a time delay determined by the response measurement duration. Signal fidelity is preserved, and phase errors caused by the dispersive cavity environment are corrected by the TR-PC process.



(a)



(b)

Figure 3. Architecture of (a) time reversal pulse compression and (b) one-bit time reversal pulse compression systems (adapted from [7]).

The compression gain of the reverberant cavity is defined as the ratio of cavity output signal peak magnitude to time reversed cavity input signal peak magnitude. The gain is calculated from the time-domain signal values. As only a few dBs of compression gain is available from TR-PC, the process is modified to one-bit time-reversal pulse compression (OBTR-PC), depicted in Figure 3(b) [7,8]. OBTR-PC applies the signum function to the

TR-IR prior to cavity input, effectively increasing the energy per time of the TR signal. The compression gain is increased to over 20 dB with OBTR-PC. However, time sidelobes are created with the OBTR, indicating compromised signal fidelity. The details of the TR-PC methods can be found in the June 2022 MSR.

3.15.4 Tasks, Milestones, and Status

(A) Milestone – Demonstrate 2–3 times increase in peak power and compression gain using magnetic pulse compression (MPC) [PARTIALLY COMPLETE].

1. Subtask – Model saturable inductors in LTSpice for MPC simulations / COMPLETE.
2. Subtask – Simulate traditional MPC circuit in LTSpice / COMPLETE.
3. Subtask – Investigate the operation, design, and pitfalls of MPC circuits / COMPLETE.
4. Subtask – Design and simulate MPC circuit with RF input to evaluate the resulting amplification and frequency content. / PARTIALLY COMPLETE.
5. Subtask – Model the high frequency behavior of MPC circuit / PARTIALLY COMPLETE.
6. Subtask – Investigate alternative solutions for high frequency operation of MPC / COMPLETE.
7. Subtask – Build and test the MPC prototype using bench top power supply / SUSPENDED.

(B) Milestone – Investigate pulse compression methods other than MPC for feasibility / PARTIALLY COMPLETE

1. Subtask – Study time reversal pulse compression to assess its compatibility with GaN-based source. / PARTIALLY COMPLETE.

(C) Milestone – Increase the compression gain available from PC. / SUSPENDED.

(D) Milestone – Build and test SWAP-C2 compatible high-frequency PC prototype with GaN source. / SUSPENDED.

3.15.5 Methods and Approach

3.15.5.1 Magnetic Pulse Compression

A prototype was constructed and tested with readily available components for the initial study of traditional MPC circuits. Then, saturable inductor modeling was investigated and realized in LTSpice to enable simulation of MPC and effects of magnetic core characteristics on MPC operation. Even though MPC circuit equations assume ideal magnetic cores and do not include the effects of core parameters on circuit operation, hysteresis behavior and the B–H curve shape have serious effects on MPC behavior.

Next, MPC circuit and magnetic core considerations for high-frequency operation were investigated. Commercially available magnetic cores were evaluated for high-frequency MPC operation. As the limitations with COTS magnetic cores over 300 MHz became

obvious, alternate materials, such as superparamagnetic materials, were explored. This led to discussions with KRI (Northeastern University) on grain-boundary-engineered magnetoceramic nanocomposites. A proposal to develop a new magnetic core material, tailored for high-frequency MPC operation, was prepared with KRI.

The MPC circuit was altered to accommodate continuous-wave input signals. Proof-of-concept was demonstrated through LTSpice simulations. Note that the high-frequency effects were not built into the saturable inductor model utilized in the simulations due to time constraints and need to be included in any future effort. Efforts to build a prototype at the maximum frequency possible with commercial COTS, i.e., ≤ 200 MHz, were also suspended due to running out of time on the program.

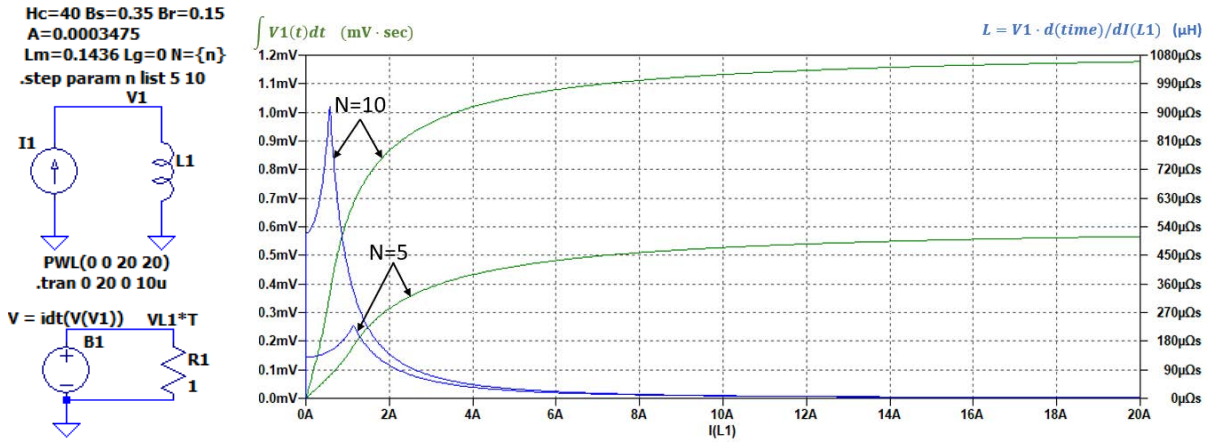
3.15.5.2 Time-Reversal Pulse Compression

The feasibility of the TR-PC methods for signal amplification was evaluated through discussions with collaborators at the Naval Research Lab (NRL). NRL's theoretical and experimental work on TR-PC focuses on different applications. Through biweekly meetings the readily available data were assessed and sometimes re-analyzed for signal amplification viability.

3.15.6 Results and Discussion

3.15.6.1 Magnetic Pulse Compression

Saturable inductors are modeled in simulators using the magnetic core behavioral models. Even though inductor saturation can be approximated with hyperbolic tangent or arctangent functions in LTSpice, a more accurate saturation behavior with hysteresis is obtained using the Chan model [9]. To calculate the upper and lower branches of the major hysteresis loop, the initial magnetization curve, and the minor hysteresis loops, Chan model uses the geometric parameters for the magnetic core and the number of inductor windings, as well as the coercive force H_c, remnant flux density, B_r, and the B-axis intersection of the asymptotic line for saturation flux density, B_s, of the magnetic core, as shown in Figure 4(a).



(a) (b)

Figure 4. (a) LTSpice simulation circuit for saturable inductor with Chan model, and (b) Volt–second product and inductance vs. current for saturable inductors with N = 5 and 10.

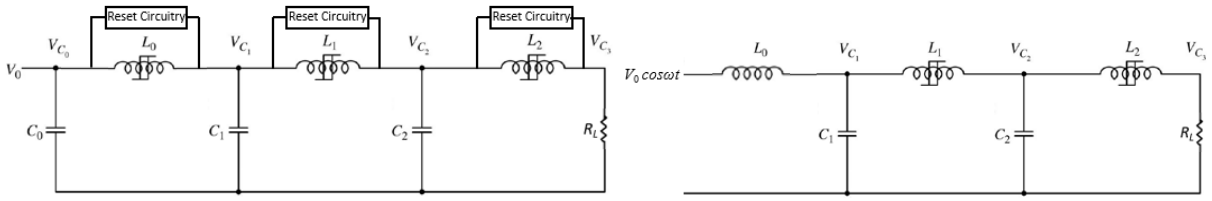
The time integral of the inductor voltage can be obtained using a behavioral voltage source and is plotted against the inductor current in Figure 4(b). This is the inductor equivalent of the magnetic material B–H curve, as explained in the March 2022 MSR. Plotted in the same figure is the change of inductance with applied magnetic field. The MPC operation relies on sharp change of inductor impedance and any gradual change in inductance results in a 'leaky switch' that causes leakage currents to subsequent stages and decrease in available compression gain. Simulations show that a magnetic core with sharp saturation behavior, low H_c, and high B_r is ideal to minimize the MPC leakage currents. Details can be found in MSRs from March and April 2022.

The traditional two-stage MPC and the proposed continuous-wave input MPC are depicted in Figure 5(a) and (b), respectively. Input capacitor is redundant in case of CW input, and the input stage resonance frequency, which affects the time to saturation for L_1, is reduced to $\omega_0 = 1/\sqrt{L_0 C_1}$. Bipolar input signal is preferred for the CW-input MPC to enable inductor saturation in both directions and to avoid reset circuitry. This means that the input signal amplitude and frequency should provide enough flux to saturate the inductor for $\Delta B = 2B_{sat}$. For saturation occurring at half signal period, the time voltage product, VT, required is:

$$\int_0^{\frac{\pi}{\omega}} V_0 \sin \omega t \, dt = 2B_{sat} \cdot N \cdot A_e \quad \Rightarrow \quad V_0 \cdot T = \; 2\pi \cdot B_{sat} \cdot N \cdot A_e \tag{13}$$

This sets the initial restraint on core selection and the maximum achievable compression gain given by Equation (7). B_{sat}, N, and core cross-sectional area, A_e, should all be minimized so that the input voltage to the MPC, coming from an amplifier and limited to several hundred volts for the best commercially available SSA, can saturate the inductors at high frequencies. In order to ease the requirements for inductor winding N, the input

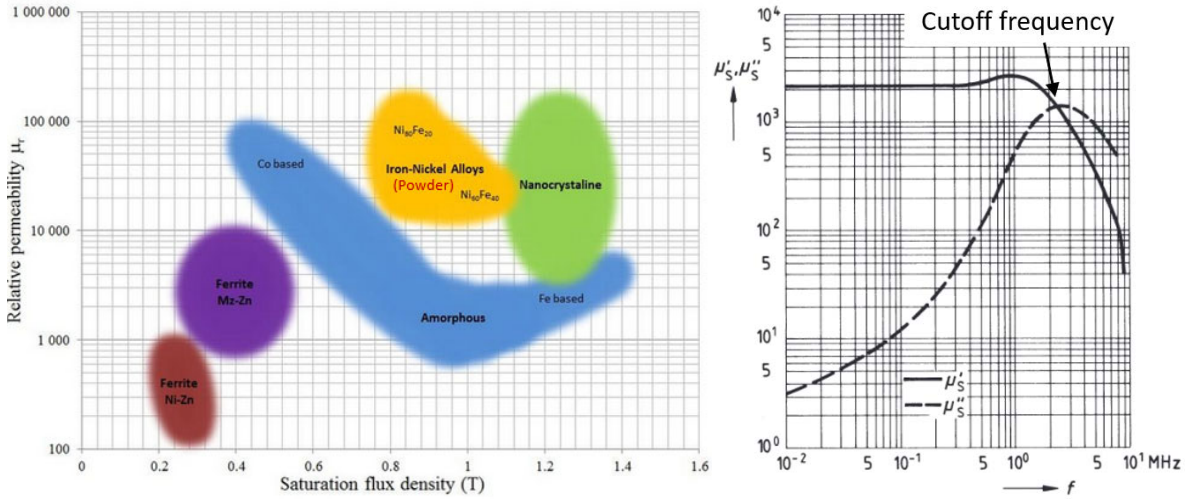
stage of the proposed MPC uses an air-core inductor, instead of a saturable inductor. A compression gain of 16 can easily be obtained with L_0 = 16L, L_1 = 4L, and L_2 = 1L as the first stage inductor with N = 4, instead of the input stage inductor with N = 16, is to be saturated with the input voltage. Inductor ratios can be increased to improve the gain; however, VT product requirements for saturation and additional losses due to winding or increased inductance need to be considered.



(a) (b)

Figure 5. (a) Two-stage MPC with DC input and (b) two-stage MPC for continuous-wave input.

Different magnetic core materials were investigated to determine the most suitable candidates for high-frequency pulse compression, especially considering the low B_{sat} requirement. Commercially available magnetic cores are grouped as 'soft' iron, silicon steel, amorphous, nanocrystalline, powder, and ferrites. Details of COTS magnetic material survey can be found in the February, May, and July MSRs. The relative permeability and B_{sat} for common magnetic cores are given in Figure 6(a). NiZn ferrites have the lowest B_{sat} of ~ 200 mT among COTS magnetic cores [10].



(a) (b)

Figure 6. (a) Relative permeability and B_{sat} for common magnetic core materials [11] and (b) typical magnetic core complex permeability [12].

Figure 7 shows the input voltage required to saturate a magnetic core of A_e = 12.9 mm^2 and N = 4 with different B_{sat} values for input frequencies between 100 kHz and 1 GHz. B_{sat} needs

to be lower than 10 mT for V_{in} required at 1 GHz to be reduced to several hundred volts, a more realistic value for SSA output voltages. Toroids with cross-sectional area of ~1 mm^2 exist; however, toroid dimensions required to fit in the conductor windings need to be considered. Even if such small toroids are used in the design, the B_{sat} requirement is only relaxed by an order of 10. As no magnetic material with B_{sat} < 100 mT is commercially available, MPC cannot be realized at 1 GHz for SSA integration, given the low SSA V_{out}.

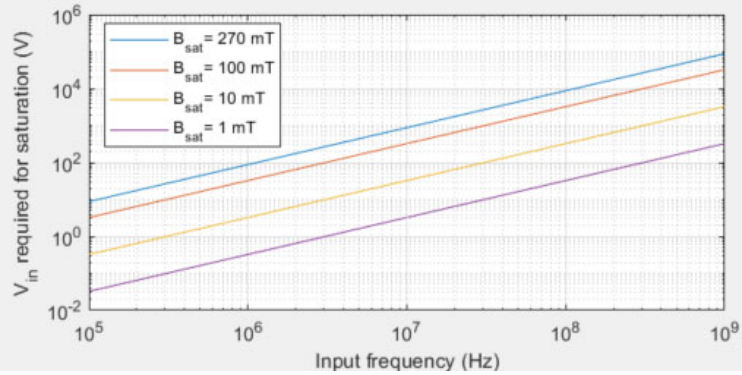


Figure 7. V_{in} required for inductor saturation at different input frequencies for various magnetic core saturation flux densities (A_e = 12.9 mm^2 and N = 4).

Even though NiZn ferrites have the lowest μ_r compared to other cores, as shown in Figure 6(a), they operate at the highest frequencies. This is in accordance with Snoek's law, which dictates inverse proportionality between the cut-off frequency and the initial permeability of a material [13]. Cut-off frequency is related to the complex behavior of permeability and is illustrated in Figure 6(b) for a typical magnetic material. Material μ_r, indicated by the real permeability, drops off to unity and the imaginary permeability, which determines the power loss through the material, increases at the cutoff frequency. The magnetic core cannot be utilized in an MPC circuit beyond its cutoff frequency because it will not provide a large impedance change during saturation and its losses will be too large. The best COTS NiZn core has a cutoff frequency of less than 350 MHz and μ_r of only 7.5 [10]. This core can operate as a magnetic switch only up to 350 MHz and it would be a leaky switch due to its low initial permeability. An MPC circuit that operates over 350 MHz cannot be build due to lack of available magnetic material.

As no suitable commercial material is available for high frequency operation, a typical NiZn core was used in the MPC simulations for proof-of-concept at lower frequencies. The schematic for the designed circuit is given in Figure 8(a), and the general design procedure for a given input frequency is outlined in Figure 8(b). For this design, the MPC capacitors were set to 100 µF and the required input frequency and voltage were calculated. The load resistor is sized at $R_L > Z_0$ to minimize the residual negative voltage at C2. Optimum load match for energy transfer is compromised at the cost of circuit stability; details are included in the July 2022 MSR.

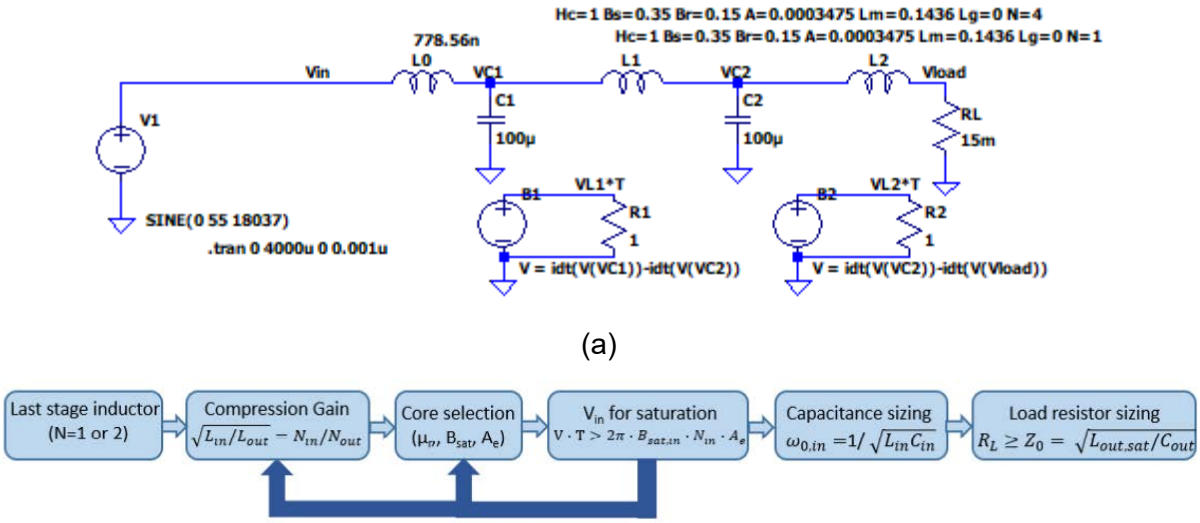
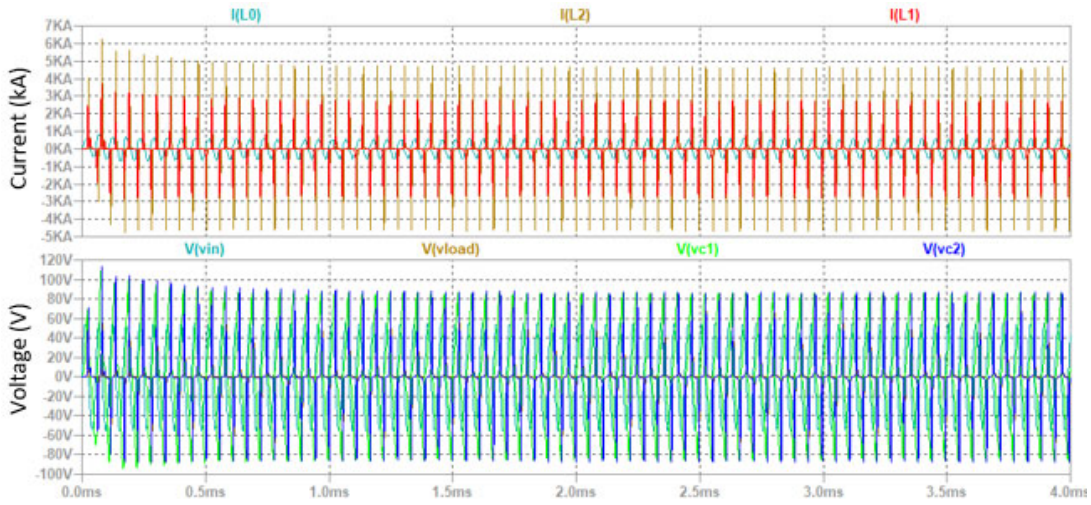
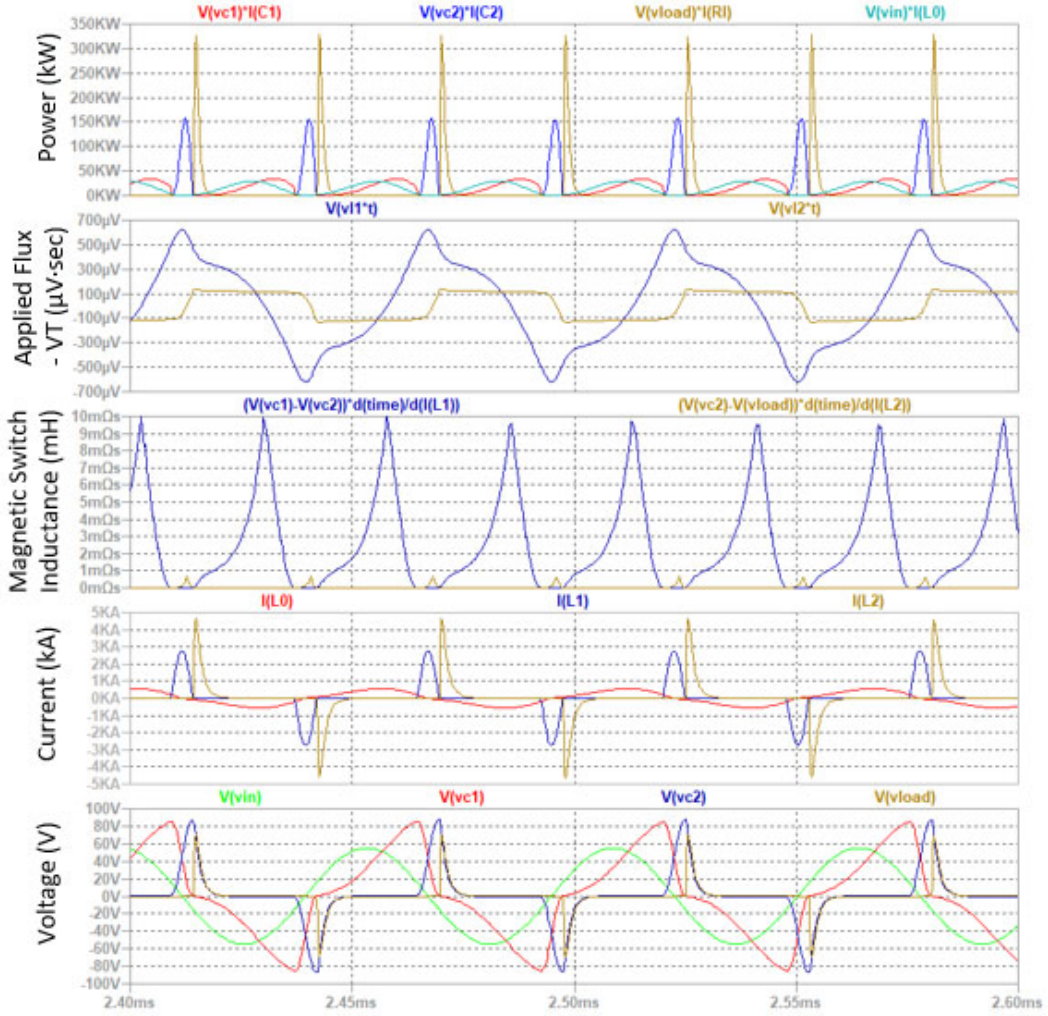


Figure 8. (a) LTSpice schematic for the two-stage MPC with continuous-wave input, and (b) the general design procedure for a given input frequency.

Figure 9(a) shows the voltage and current waveforms at different stages of the two-stage MPC with 55 V input signal at 18 kHz. The operation is stable after initial settling behavior. Details of important waveforms, including the voltage–time product applied to saturable inductors and the corresponding change in their inductance are given in Figure 9(b). Gain is 4 at the first stage, as expected, but is reduced to >2 at the second stage due to $R_L > Z_0$.



(a)



(b)

Figure 9. Two-stage MPC with 55 V, 18 kHz input: a) voltage and current waveforms and (b) detail of voltage, current, magnetic switch inductance, VT product, and power.

Figure 10 shows the voltage, current, and power gain between the input and output terminals of the two-stage MPC. Total power gain of 11 is obtained with current gain of 9 and voltage gain of 1.2. Some of the gain lost to resistive loading is compensated by the peaking at the input stage.

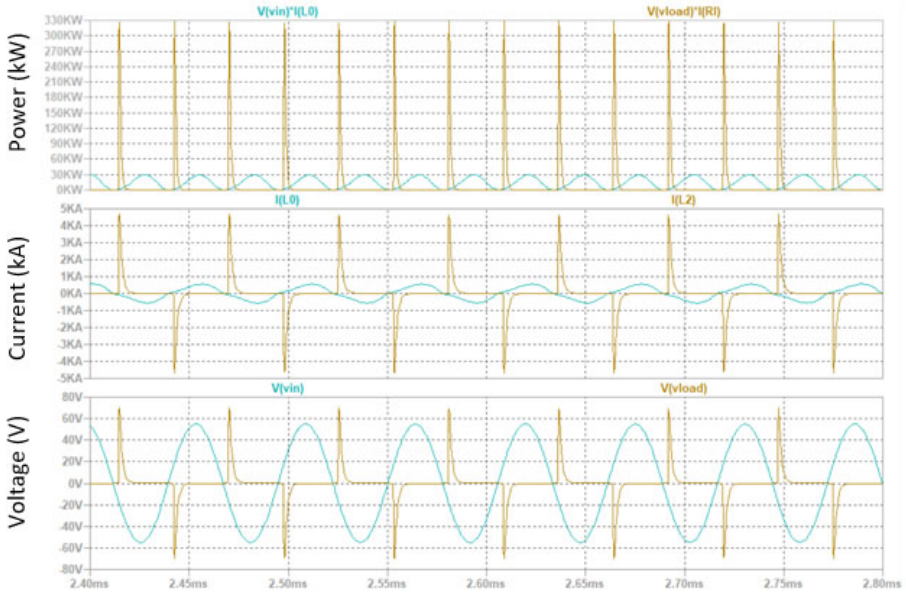


Figure 10. Voltage, current, and power gain of the designed two-stage MPC.

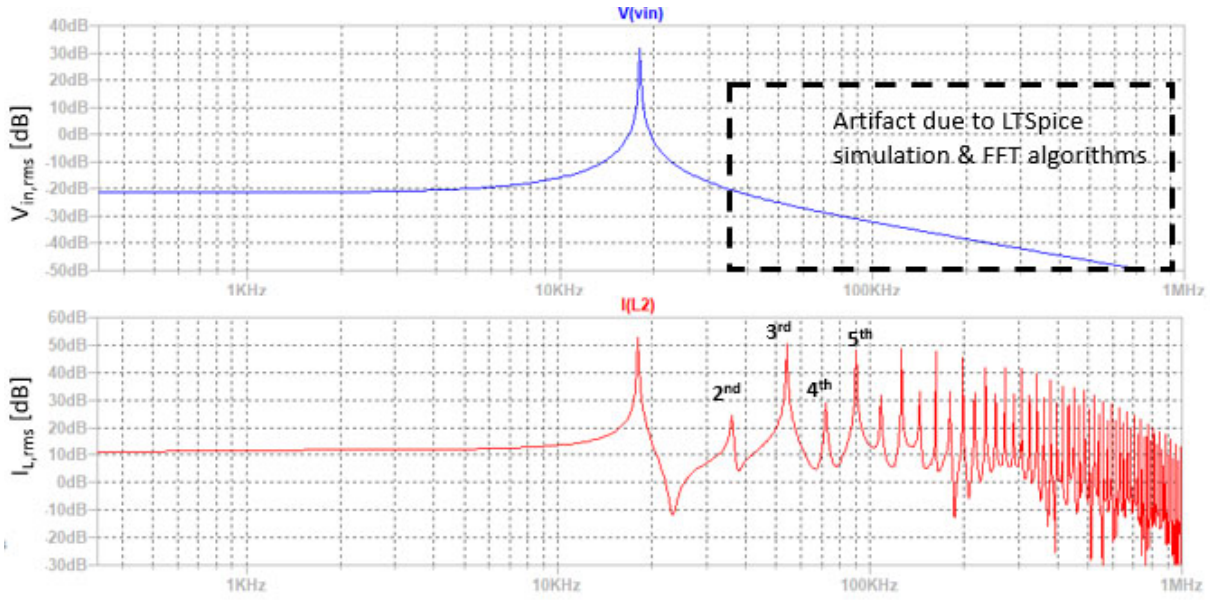


Figure 11. Frequency spectrum for the input sine voltage at 18 kHz and the resulting compressed current at the MPC output.

The signal spectra for input voltage and output current are given in Figure 11, as obtained from LTSpice. There are artifacts in the high-frequency regions due to LTSpice simulation

and FFT algorithms; however, main signal power accuracy is verified with hand calculations and the high-frequency spectral content matches the expected spectrum qualitatively. For the input sinewave of 55 V, rms signal power of 33 dB is expected and observed in the plot. For the compressed output current of 4.5 kA, the expected rms signal power would be 71.6 dB. Given the signal power of <55 dB at 18 kHz, around 18 dB is expected to be lost to harmonic content. Figure 12 depicts the expected spectral content for symmetric compression, with only odd harmonics present. Even harmonics are also present in Figure 11 and are attributed to the asymmetric compression in MPC with unequal rise and fall times. Signal fidelity is severely compromised with MPC.

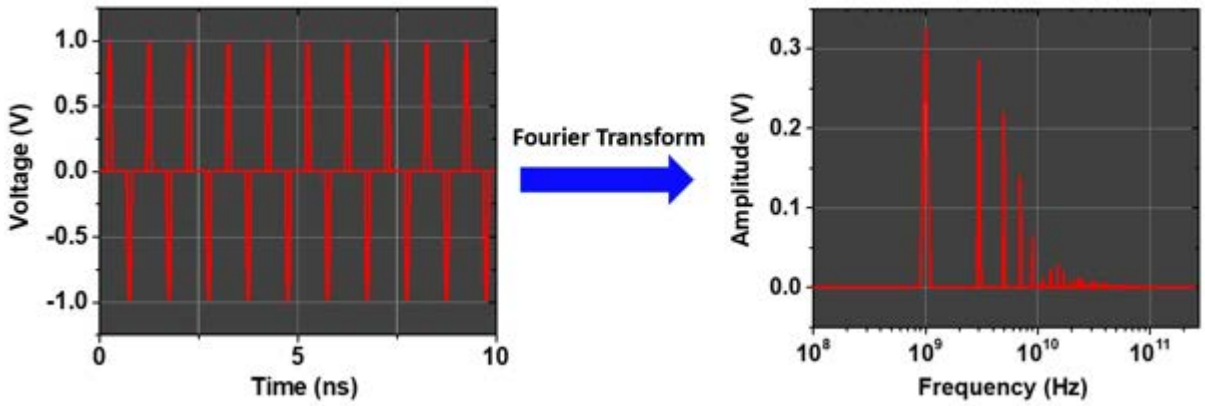


Figure 12. Symmetrically compressed sinewave in time and frequency domain [14].

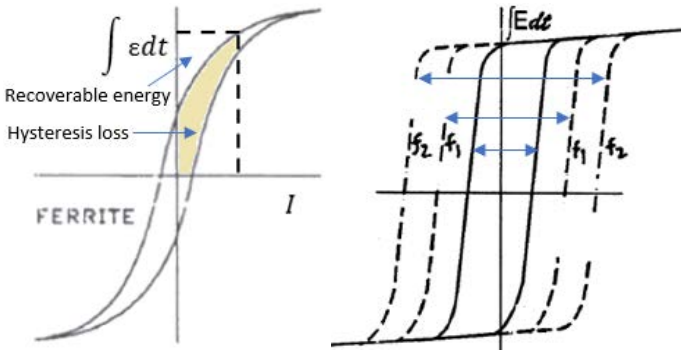
The data from Figure 11 is used in hand calculations to approximate the gain in frequency domain, with and without an MPC at the SSA output. Converting the voltage and current values at 18 kHz from Figure 11 to power by using the appropriate load resistances, i.e., 50 Ω and 15 mΩ, respectively, 18 dB (48 dBm) and 35 dB (65 dBm) are obtained. There is approximately 17 dB gain to be obtained from interfacing the SSA with an MPC system. It is imperative to note that some of the gain will be lost to the impedance matching network between the MPC and the antenna. Parasitic losses related to circuit components are also not included in the current LTSpice simulations and need to be considered.

The main losses in an MPC circuit, that reduce the compression gain, are magnetic switch leakage and inductor losses. Magnetic switch leakage is related to on/off relative permeability and the B–H curve shape of the magnetic core. A magnetic core with high unsaturated μ_r and sharp saturation characteristics is required to minimize the leakage losses. Inductor losses arise from both the winding and the magnetic core. Winding related losses include DC and AC wire resistances, dielectric losses, and, most importantly, the wire capacitance, which appears in parallel with the inductor and results in a self-resonant frequency, above which the inductor acts like a capacitor. Wire material and sizing, number of turns, and winding methods need to be optimized to minimize the winding related losses.

Inductor core material is the major contributor to the MPC losses. The most common core losses are hysteresis, eddy current, and anomalous losses, detailed in the January 2022 MSR. Hysteresis loss, visualized in Figure 13(a), is a general dissipative process in magnetic materials, quantifying the energy lost while moving the operating point. Eddy current losses are due to voltage induced in the core finite resistance, caused by varying magnetic fields. Eddy current losses can be minimized by increasing core resistance and reducing the eddy current loop area, through core processing methods such as lamination. All the remaining losses caused by other mechanisms are called anomalous or residual losses. Legg's equation for total loss provides an insight into the contribution of each loss [15]:

$$\frac{R_C}{\mu L} = aB_m f + cf + ef^2 \tag{14}$$

R_C, L, and μ are the core's effective ac resistance, inductance, and permeability, respectively. The first term is the hysteresis loss, and it increases with the maximum flux density, B_m, of the operation. Hysteresis and anomalous losses are proportional to the operating frequency, whereas the eddy current loss increases with the square of frequency. The frequency dependence of losses results in the widening of core hysteresis loop with increasing frequency as depicted in Figure 13(b).



(a) (b)

Figure 13. (a) Hysteresis loss and (b) change of hysteresis loop with frequency [16].

Legg's Equation is valid at low flux densities. A more accurate loss calculation for sinusoidal excitation at higher flux densities can be obtained through Steinmetz's Equation [17]:

$$P_v = k \cdot f^a \cdot {B_m}^b \tag{15}$$

P_v is the time average power loss per unit volume, B_m is the peak flux density calculated as half the flux swing, and a, b and k are the Steinmetz coefficients, normally provided by the manufacturer. Typically, 1<a<3 and 2<b<3 and the actual coefficient values depend on the magnetic core material. Flux swing is the most important design parameter to minimize the loss, especially with AC excitation. B_m is equal to B_{sat} for the MPC circuit.

Magnetic loss, dielectric loss, skin effect, and dimensional resonance should also be considered at higher frequencies of interest [11][18][19], not typical of traditional MPC applications. Complex permeability, depicted in Figure 6(b), results in magnetic loss through its imaginary part, especially around and over the cutoff frequency of the magnetic core. The complex impedance of the inductor is given by:

$$\bar{Z} = j\omega\bar{\mu}L_0 = j\omega\mu' L_0 + \omega\mu'' L_0 = j\omega L_s + R_s \tag{16}$$

where the second term represents the parasitic resistor due to imaginary permeability, in series with the inductor. The inductor acts more like a resistor over the cutoff frequency. The complex permittivity of the magnetic core adds the parallel combination of a parasitic capacitor and resistor to the inductor model:

$$\bar{Y} = j\omega\bar{\varepsilon}L_0 = j\omega\varepsilon' C_0 + \omega\varepsilon'' C_0 = j\omega C_p + G_p \tag{17}$$

ε" in Equation (17) only models the displacement current in the material. Effective imaginary permittivity (ε_{eff}") should replace ε" when conduction current is not negligible:

$$\varepsilon''_{eff} = \varepsilon'' + \frac{\sigma}{\omega} \tag{18}$$

The magnetic and dielectric properties of the core material also contribute to more losses through skin effect and dimensional resonance. Skin effect occurs when the core physical dimension is greater than the skin depth:

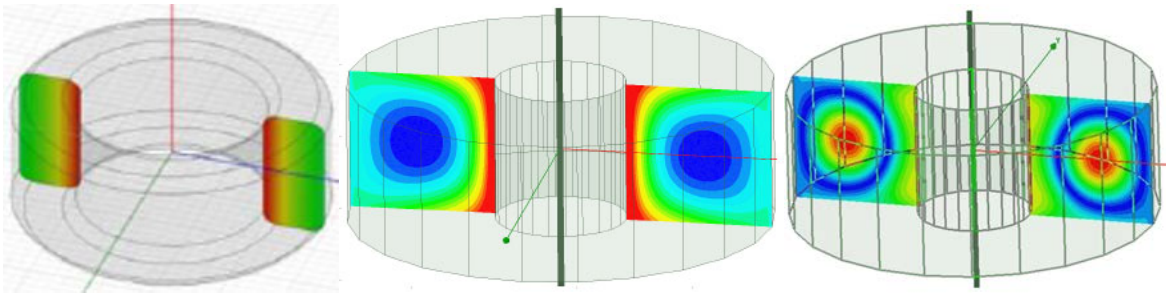
$$\delta \approx 2\rho\sqrt{\frac{\varepsilon}{\mu}} \quad \text{for} \quad \omega \gg \frac{1}{\rho\varepsilon} \tag{19}$$

and dimensional resonance occurs for core physical dimension greater than half wavelength:

$$\lambda = \frac{v}{f} = \frac{c}{f\sqrt{\mu\varepsilon}} \tag{20}$$

Both the skin effect and the dimensional resonance cause standing waves to be formed in the core, resulting in nonuniform flux distribution as depicted in Figure 14. This leads to localized magnetic saturation, reduced permeability, and higher core losses.

To minimize high-frequency losses, core dimensions need to be kept at a minimum and the core material properties need to be optimized. Parasitic capacitance and resistances and the dimensional losses can be reduced through low dielectric constant, ε_r and low magnetic and dielectric loss tangents. Material optimization for MPC at high frequencies can be achieved through insulated grains and grain-boundary engineering [20][21].



(a) (b) (c)

Figure 14. (a) Expected flux distribution in a toroid [11] and its variation with (b) skin effect [19] and (c) dimensional resonance [19].

3.15.6.2 Time-Reversal Pulse Compression

Evaluation of T-R based PC methods for SSA integration and amplification, as shown in Figure 15, is being conducted as a joint effort with NRL. As the published TR-PC papers focus on time-domain signal properties and the gain is defined as the ratio of maximum power level of the reconstructed signal at point C to that of the one-bit time reversed (OBTR) PC signal at point B, it is not possible to assess the frequency domain gain that can be obtained from the proposed integration. Unpublished data from on-going NRL research is being used for the analysis and the details cannot be shared in this report.

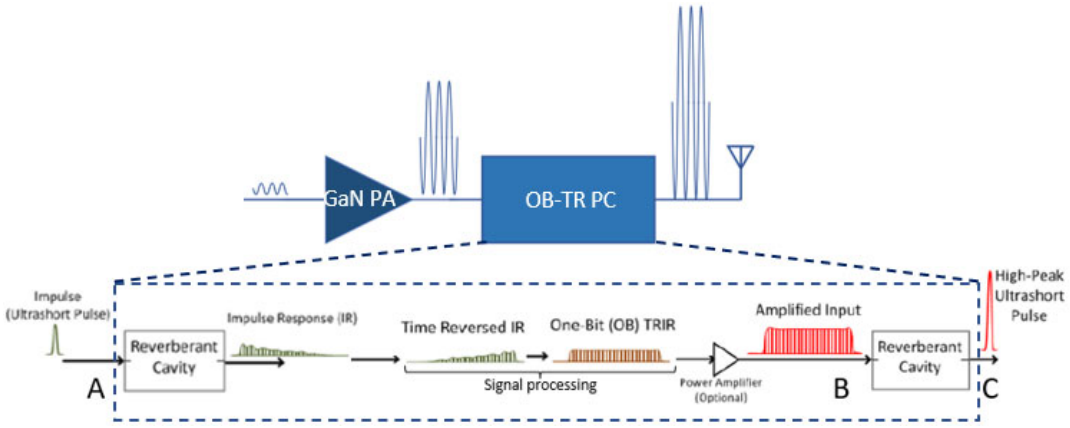


Figure 15. OB-TR PC for SSA integration.

TR PC preserves signal fidelity in the frequency domain due to phase correction as explained in [7-8] but suffers from loss, as the resonant cavity is a passive and dispersive circuit element. The OB-TR process adds gain to TR PC due to digitization; however, digitization also introduces phase errors, which translate into additional frequency components. When the gain is defined as the ratio between the system output and input (points C and A), a mean gain of more than 20 dB is observed in the frequency domain with an impulse input.

If the input to the system is other than an impulse, the bandwidth and the duration of the input signal will determine the gain. The TR PC gain drops significantly for lower signal bandwidths and increasing pulse widths, as detailed in the June 2022 MSR. Therefore, an SSA integrated with OB-TR PC cannot be operated in CW mode, but gain can be obtained in pulsed mode with narrow pulse widths. However, the pulse repetition frequency (PRF) will be limited as the compression gain drops for impulse response (IR) record lengths shorter than a limit duration, e.g. IR record length ≥1000 ns and PRF ≤ 1 MHz for the prototype in [8].

OB-TR PC can add gain to the SSA output if the SSA is operated in pulse mode. The PRF will be limited by achievable gain. The output signal will be distorted but can still be used for HPM purposes if sufficient gain is achieved. The feasibility study is on-going.

3.15.6.3 Summary and Recommendations

MPC was evaluated and modified for SSA integration. Theoretically, a frequency domain gain of 17 dB up to a few hundred MHz is possible with such integration, without taking into account the magnetic core losses. In order to operate the MPC at frequencies of interest, i.e., >500 MHz, a new magnetic core needs to be developed and a proposal for such a core has been prepared in collaboration with KRI. The details of MPC core requirements and the proposed material properties are summarized in Table 1. The loss models need to be incorporated in simulation models for a more accurate evaluation of achievable gain. A low-frequency prototype, at frequencies permitted by COTS magnetic cores, need to be built and tested for model verification. For future MPC efforts, material development and modeling efforts can be conducted simultaneously or sequentially.

Table 1. MPC magnetic core considerations and proposed material properties.

MPC Considerations	Related Equation	Requirement	KRI-MIDE Proposal
Saturation condition	$V > 2\pi \cdot B_{sat} \cdot N \cdot A_e \cdot f$	B_{sat} < 100 mT (for 1GHz MPC)	B_{sat} < 200±50 mT
Switch leakage	$\mu_{unsaturated} >> \mu_{saturated}$	$\mu_r >> 1$	μ_r > 25 (f_c > 0.5 GHz)
Hysteresis loss	$P_H = \alpha \cdot B_{sat} \cdot f$	$H_c \downarrow$ & $B_{sat} \downarrow$	H_c < 3 Oe
Eddy current loss	$P_e = \frac{\pi^2 \tau^2 B_{sat}^2 f^2}{\beta \rho}$	$\tau \downarrow$ & $\rho \uparrow$ & $B_{sat} \downarrow$	Insulated grains & $\rho = 10^8 - 10^{12}$ Ω-cm
Anomalous losses	$P_A \propto f$	domain wall movement	?
Magnetic loss	$R_{series} = \omega \cdot \mu'' \cdot N^2 \cdot \frac{A_e}{l_e}$	$\mu'' \downarrow$	$\tan\delta_\mu$ < 0.02
Dielectric loss	$G_{parallel} = \omega \cdot (\varepsilon'' + \frac{\sigma}{\omega}) \cdot \frac{A}{d}$	$\varepsilon'' \downarrow$ & $\rho \uparrow$	Insulated grains
Skin effect (Nonuniform flux)	$d < \delta \approx 2\rho \sqrt{\frac{\varepsilon}{\mu}}$ for $\omega \gg \frac{1}{\rho\varepsilon}$	$\rho \uparrow$ & $\varepsilon'' \downarrow$ & $\varepsilon_r \uparrow$ & $\mu \downarrow$	$\rho = 10^8 - 10^{12}$ Ω-cm & $\tan\delta_\mu$ < 0.02 & $\tan\delta_\varepsilon$ < 0.01
Dimensional resonance (Nonuniform flux)	$d < \frac{\lambda}{2} = \frac{c}{2f\sqrt{\bar{\mu} \cdot \bar{\varepsilon}}}$	$\varepsilon_r \downarrow$ & $\mu \downarrow$ & $\rho \uparrow$ & $\varepsilon'' \downarrow$	$\rho = 10^8 - 10^{12}$ Ω-cm & $\tan\delta_\mu$ < 0.02 & $\tan\delta_\varepsilon$ < 0.01

TR-based PC is being evaluated for SSA integration in collaboration with NRL. Frequency-domain gain is possible in case of pulsed amplifier operation with limited PRF and at the expense of signal fidelity.

Both MPC and TR-based PC methods have the potential for signal amplification in frequency domain. Despite the challenges, they might provide future alternatives to SSA power combining methods, which are costly in terms of SWAP-C2.

3.15.7 Outputs

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3.15.8 References

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3.16 Jet Impingement Thermal Management System

(J. Berg, R. Allen, S. Sobhansarband; Originally published in the July 2021 MSR)

3.16.1 Executive Summary

HPM systems require powerful and compact cooling systems in order to maintain operational capabilities. A key component that requires significant heat extraction (several hundreds of watts up to 1 kW) are silicon photoconductive semiconductor switches (Si-PCSS). Many methods of thermal management have been studied, which include (in order from lowest to highest heat extraction performance) passive cooling (heat sinks, cooling fins), passive multi-phase cooling (heat pipes), active single-phase liquid cooling (microchannel cooling systems), or active single-phase turbulent cooling (jet impingement systems). To dissipate up to 1 kW of heat, a single-phase jet impingement cooling system was designed. The jet impingement thermal management system (JI-TMS) was studied computationally using fluid dynamics modeling and experimentally through prototype fabrication and testing. The system used a pure silicone fluid (PSF) heat transfer fluid (HTF), chosen for its dielectric strength for operation in close proximity to kilovolt-scale electric fields. The JI-TMS design demonstrated the ability to compensate 200 W (200 MW/m^3) average power and maintain the average temperature of the Si-PCSS source at 50 °C (10 °C lower than a microchannel laminar-flow-based design of equivalent volumetric form-factor). The performance analysis of the optimized geometry and dielectric fluid had certain restrictions with regard to pressure threshold as the system's pressure should not be dramatically increased. Further iterations of the current design are unlikely to meet the stretch goal cooling requirement of >1 kW (1 GW/m^3) due to the large pressure drop that occurs. While jet impingement as a method of heat transfer should still be considered a viable method, the viscosity of the fluid presented a challenge in being able to create turbulent regimes in the JI-TMS. To overcome this challenge, decreasing the JI-TMS nozzle diameters by a factor of 10 and increasing the nozzle count by the same has the potential to increase convection of the coolant, thereby increasing heat extraction capabilities.

3.16.2 Technical Background

Managing thermal load is critical to the success of HPM systems. Traditional single-phase liquid cooling technologies such as laminar flow microchannels are ubiquitous in cooling applications (primarily for electronics). The microchannel systems are relatively easy to manufacture and perform comparatively with two-phase cooling systems such as heat pipes, but are performance limited and therefore not useful for power density systems. The major drawback with microchannel liquid cooling is associated with the laminar flow heat transfer fluids. Laminar flow has little to no convection. This lack of convection means that the primary driver of heat transfer in a microchannel cooling system is conduction of the fluid and the temperature differential of the fluid and heat sink. The largest temperature differential is created through a higher flow rate. If fluid convection is

employed, the thermal management system would then utilize the conduction of the fluid as well as the convection of the fluid to drive heat away from the heat component. With this additional medium of heat transfer, the heat extraction performance could be increased. This forced convection method is considered for HPM thermal management systems.

While a microchannel TMS fluid traverses the length of the heated surface in a laminar flow regime, a jet impingement (JI) TMS directs fluid normal to the heated surface though an array of nozzles. Figure 1 shows this process more clearly.

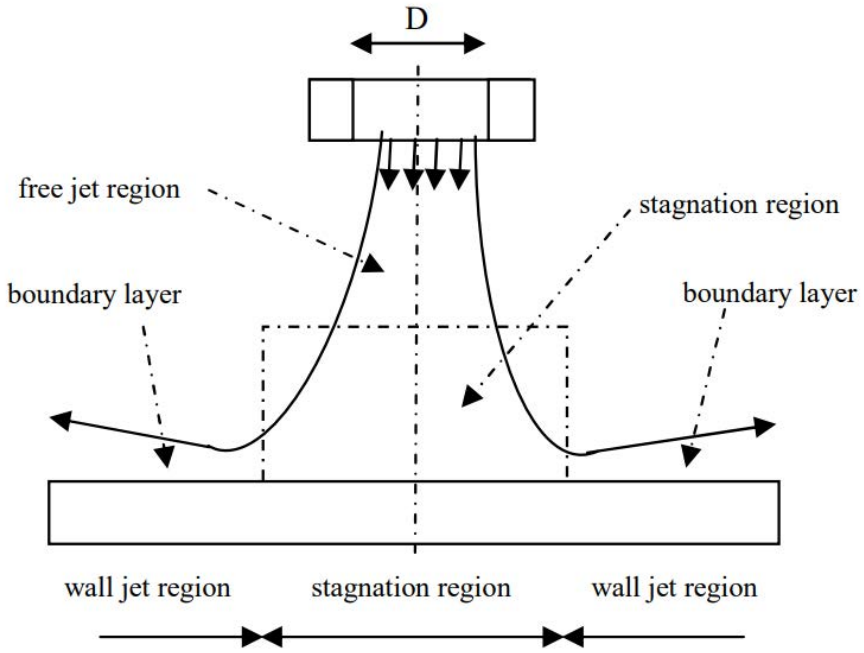


Figure 1. Diagram of jet impingement flow regimes.

Ideally, this flow orientation creates a central region (known as the stagnation region) that produces the maximum heat transfer of the fluid due to extreme turbulence. As fluid spreads out radially away from the stagnation region, the HTF creates vortices along the heated surface, which dramatically increase the heat transfer coefficient (HTC, *h*, units of W/m^{2}K. This increase in the HTC drives the heat transfer due to convection shown in the following equation.

$$Q = hA\Delta T$$

where Q is the heat removed in Watts, A is the area of focus that heat flux occurs, and ΔT represents the temperature difference between the heated surface and the fluid that contacts the wall.

Successful JI systems can yield HTC values of 4 × 10^4 – 1 × 10^5 W/m^{2}K or more [1], and have seen heat removal rates more than 40% higher than those of microchannel cooling systems [2]. In reality, there is no limit to the HTC value, though increasing it further comes

at the cost of exponentially increasing system pressure, as pressure is the driving force of the flow. This compares to laminar flow systems that maintain HTC levels on the order of hundreds to a few thousands of W/m^2K.

The specific HPM system component of interest is a photoconductive semiconductor switch (PCSS). The threshold goal for cooling the PCSS is to extract ~200 W of heat, with a stretch goal of removing 1 kW. With these goals in mind, we decided to pursue a JI-TMS design given its high HTC capabilities.

3.16.3 Methods

3.16.3.1 Computational Fluid Dynamics Modeling

Initially, computational fluid dynamics (CFD) modeling was used to model a microchannel TMS. The microchannel TMS that was modeled was based off of an experimentally tested TMS for PCSS cooling. With the experimental values of PCSS temperature, HTF flow rate, and applied average power to the PCSS, validation of the CFD model was performed. The HTF used in all simulations was a pure silicone fluid with a viscosity of 20 centistokes (hereafter known as PSF-20-cSt). As the PCSS will complete a circuit that handles kV's of electricity, PSF-20cSt was chosen for its dielectric strength. The high dielectric strength of the PSF-20-cSt provides a layer of safety to equipment and personnel in the event of leaks or other system malfunctions by acting as an electrical insulator.

Once confidence in simulating 3D multiphysics problems was gained, an initial jet impingement CAD model was created. The first model utilized 11 1-mm diameter nozzles that were evenly spaced and aligned along the center of the PCSS. The second model consisted of 26 nozzles that were arranged in a staggered pattern. Figure 2 shows a top down view of the outline of the PCSS (the large oval) and nozzle locations of each described geometry. An exploded cross section view of the staggered geometry is shown in Figure 3. Each of these models utilized the optimal design characteristics suggested by Tadhg S. O'Donovan, et al. and Aaron M. Huber, et al.[3,4]. The characteristics include nozzle to nozzle spacing, distance from nozzle exit to impingement surface, and nozzle diameter.

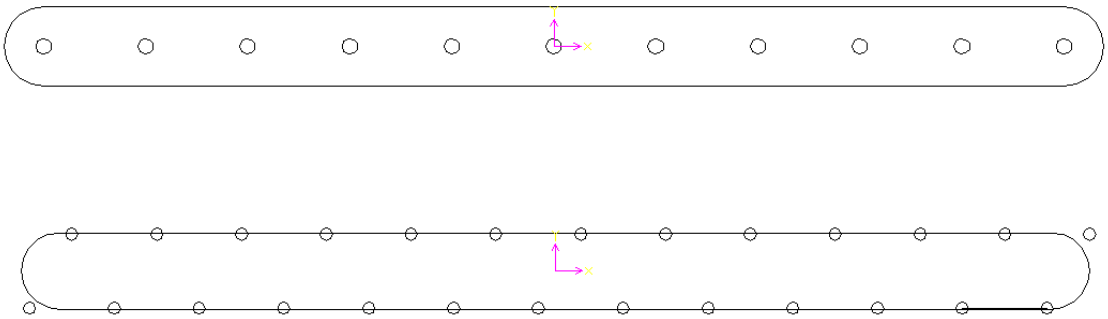


Figure 2. The jet impingement geometries showing nozzle locations relative to PCSS.

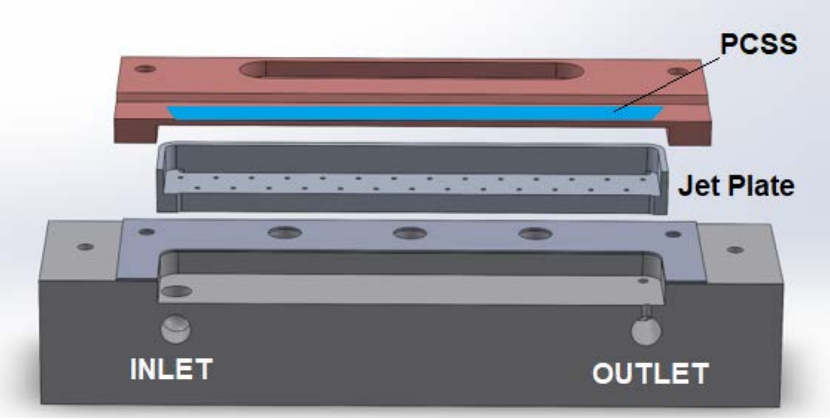


Figure 3. Exploded view of the CAD model.

Each geometry was modeled using a flow rate of 0.06 kg/s (approx. 1 gal/min). This flow rate corresponded to the flow rate used for the microchannel TMS used in prior experimentation. Two average powers of 100 and 200 W heat flux were applied to the PCSS. All geometries were studied with varying mesh sizes, with the largest mesh seeing approximately 1.7 million nodes. The CFD simulation utilized the Transition SST numerical solver. Each CFD simulation was set to run for 10000 iterations, or until no change in convergence was seen. Each model's finest mesh saw convergence of all residual error values below 10^{-4}.

3.16.3.2 Experimental Setup

The prototype staggered array JI-TMS consisted of five parts: a lid, a gasket, a base, a jet-plate, and the PCSS. The lid of the TMS was created from a copper-tungsten (Cu-W) alloy. A gasket was cut from a sheet of butyl-rubber and positioned between the lid and base for the purpose of leak mitigation. Once the parts were assembled, the semiconductor was soldered onto the Cu-W lid using a reflow oven to ensure a uniform bond. A 7 cm wide copper tab was soldered to the topside of the device to allow for a positive DC power supply connection and isolated from all other components using a dielectric sheet made from Rodgers 3003 laminate. A ground wire was secured to the Cu-W component to facilitate completing the current path loop. A chiller/pump was connected to the JI-TMS and was filled with PSF-20-cSt sourced from Clearco. An inline, spring-actuated flow meter was used to monitor the flow rate. Pressure readings were taken from an inline pressure gauge. A FLIR camera was mounted directly above the PCSS and JI-TMS to monitor real-time temperature. The complete setup can be seen in Figure 4. A view from the FLIR camera can be seen in Figure 5.

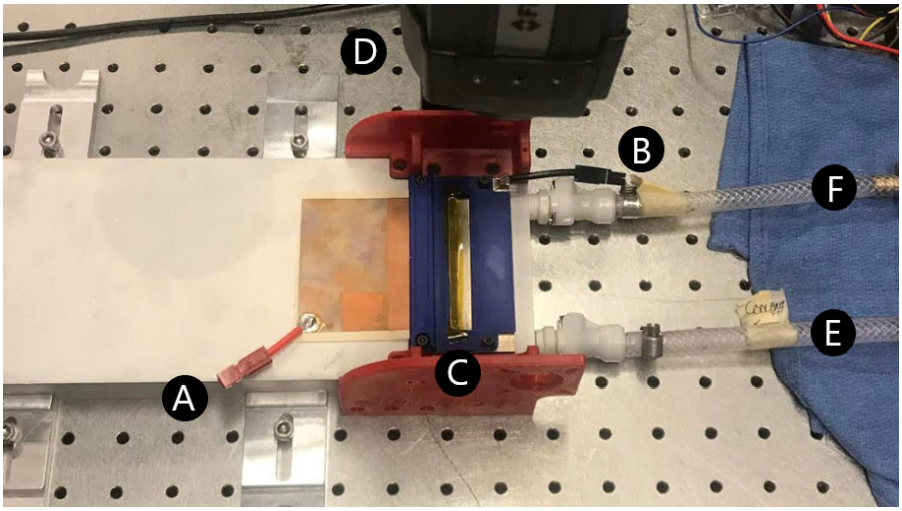


Figure 4 Experimental setup, A: Power, B: Ground, C: JI-TMS and device, D: FLIR camera, E: Inlet, F: Outlet.

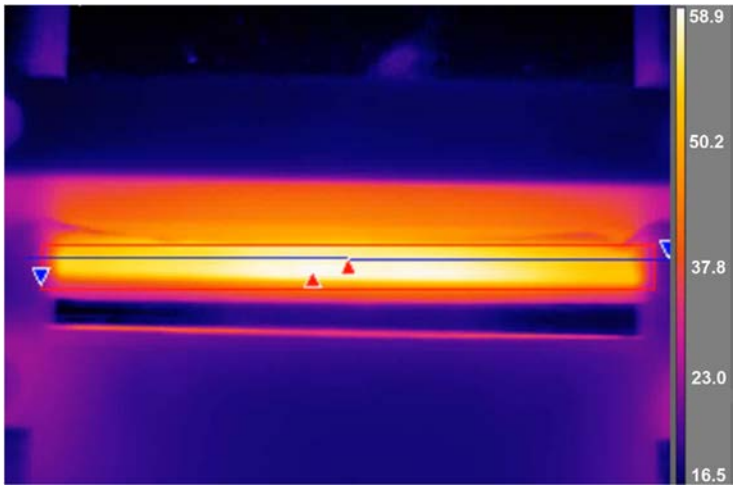


Figure 5 FLIR image of PCSS during experiment (°C).

Once the setup was completed, the camera and pump were turned on, followed by the power supply. The temperature of the PCSS was monitored until a steady state was reached, after which the power supply was turned off. The PCSS was allowed to cool until it reached near-ambient temperature.

3.16.4 Results and Discussion

According to the CFD results, the CFD staggered geometry model performed better than the single-row configuration in regard to keeping the PCSS at a lower temperature. Table 1.1 below summarizes the performance of each model.

Table 1. CFD and experimental results of the two JI-TMS designs.

	Single Row CFD	Staggered Array CFD	Experimental*
Pressure Drop (psi)	47.0	46.12	44.7
Heat Trans. Coef. At 200 W (W/m^2K)	20,071	28,472	N/A
Max Switch Temp at 100 W avg power (°C)	57.8	52.6	57.5
Max Switch Temp at 200 W avg power (°C)	114.0	99.0	98.2

*Only staggered geometry tested

The staggered geometry performed better than the single-row geometry by keeping the PCSS at a lower maximum temperature. The HTC value of the staggered geometry was nearly 30% greater than the single-row geometry. This higher HTC value in the staggered geometry is the primary reason for the temperature difference of 15.8 °C for the maximum PCSS temperature, as all boundary and initial conditions were the same for each CFD simulation, as well as the numerical method used. The staggered geometry was able to provide more cooling and keep the PCSS at a lower temperature. For this reason, a prototype of the staggered geometry was created, and the single-row geometry was not studied further.

The results from the CFD simulations were representative of the experimental values, though the temperature and pressure were overestimated slightly. Even though the TMS designs were able to cool the PCSS at 100 W, the numerical and experimental results show that the JI-TMS is unable to maintain the PCSS at a maximum temperature of 80 °C at 200 W of average power. The performance shortcoming stemmed from the requirement of the JI-TMS pressure head. The flow rate of 0.06 kg/s yielded a pressure drop of greater than 38 psi. This flow rate generates an HTC of the fluid of approximately 2.8×10^4 W/m^2K. As mentioned earlier, this HTC is lower than the 4×10^4 W/m^2K value that is indicative of the lower bounds of jet impingement TMS design. While the 4×10^4 W/m^2K value does not represent a hard boundary for achieving true jet impingement flow regimes, it could definitely be considered the lower bound of performance for this JI-TMS. To achieve the desired HTC, JI geometry calculations were utilized to determine the necessary flow rate to achieve a Reynold's number of 2200, a value indicative of transitioning from laminar to turbulent flow. To achieve this value, a flow rate of approximately 0.7 kg/s would be required (an order of magnitude greater). To determine the pressure head requirements for this flow rate, a CFD simulation was run at 0.2 kg/s (this value was chosen rather than the full 0.7 kg/s flow rate to maintain simulation stability).

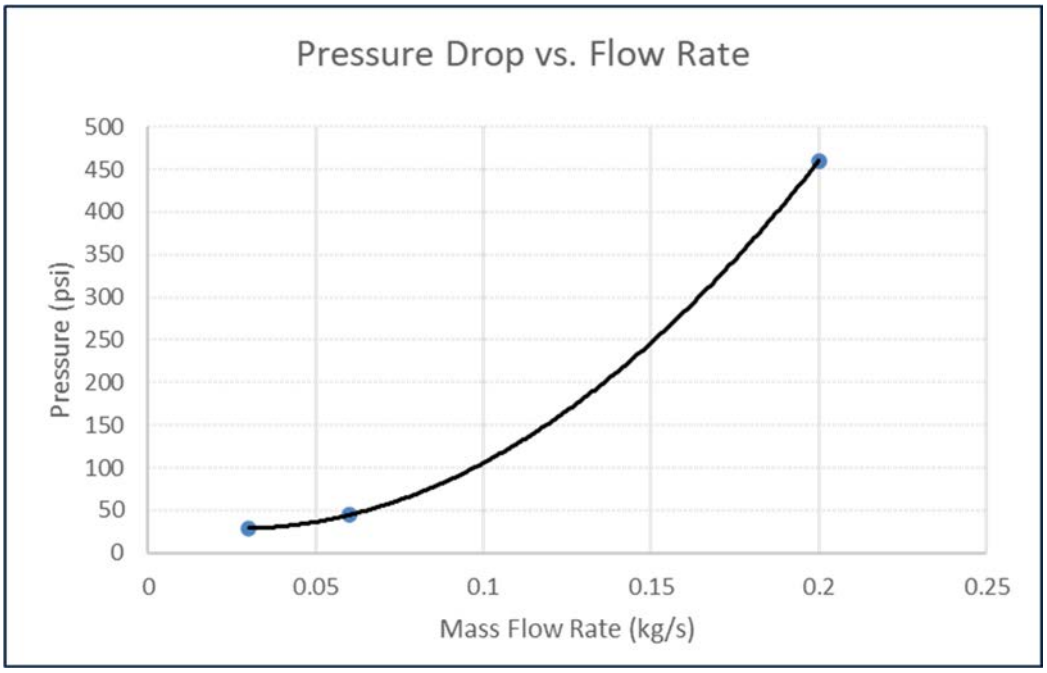


Figure 6. CFD results of the pressure drop increase due to increased flow rate.

According to the CFD model, at 0.2 kg/s flow rate, the pressure requirement is more than 450 psi, as shown in Figure 6. This pressure is achievable, though it goes against SWaP-C goals and, more importantly, it is still not enough to generate turbulent flow within the system thereby causing significant heat extraction rates. It was determined from these results that at this scale, no amount of geometric optimization would allow for the flow regimes necessary to remove ~1 kW/cm² without generating absurd system pressures requiring large and expensive support equipment.

3.16.5 Significant Findings

The JI-TMS optimized design was found to be able to compensate 200 W (i.e., >200 MW/m^3) average power and maintain the Si-PCSS source average temperature at 50 °C, which is 10 °C lower than the laminar-flow-based design of equivalent volumetric form-factor (cross-flow thermal management system) – used for the OSPRES Contract's source array demonstrator at the time of this writing. The performance analysis of the optimized geometry and dielectric fluid had certain restrictions with regard to pressure threshold as the system's pressure should not be dramatically increased. Further iterations of the current design are unlikely to meet the stretch goal cooling requirement of dissipating >1 kW (1 GW/m^3) due to the large pressure drop that occurs. While jet impingement as a method of heat transfer is still considered viable, the viscosity of the fluid presented a challenge in being able to create turbulent regimes in the JI-TMS. To overcome this challenge, decreasing the JI-TMS nozzle diameters by a factor of 10 and increasing the nozzle count by the same has the potential to increase convection of the coolant, thereby increasing heat extraction capabilities.

3.16.6 Outputs

[1] Berg, J. N., Allen, R. C., and Sobhansarbandi, S. (2021, Pending), A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation, International Journal of Thermal Sciences.

[2] Berg, J. N. (2021). Development of a Jet Impingement Thermal Management System for a Semiconductor Device with the Implementation of Dielectric Nanofluids. University of Missouri-Kansas City.

[3] Berg, J. N., & Sobhansarbandi, S. (2020, July). CFD Modeling of Thermal Management Systems for a Silicon Semiconductor Switch. In Heat Transfer Summer Conference (Vol. 83709, p. V001T09A011). American Society of Mechanical Engineers.

3.16.7 References

[1] K. Gould, S. Q. Cai, C. Neft, A. Bhunia, “Liquid jet impingement cooling of a silicon carbide power conversion module for vehicle applications”, IEEE Transactions on Power Electronics 30 (6) (2015) 2975–2

[2] M. K. Sung, I. Mudawar, “Single-phase hybrid micro-channel/micro-jet impingement cooling”, International Journal of Heat and Mass Transfer 51 (17-18) (2008) 4342–4352.

[3] Tadhg S. O’Donovan, et al. "Jet impingement heat transfer – Part I: Mean and root-mean-square heat transfer and velocity distributions". International Journal of Heat and Mass Transfer 50. 17(2007): 3291-3301.

[4] Aaron M. Huber, et al. "Effect of jet-jet spacing on convective heat transfer to confined, impinging arrays of axisymmetric air jets". International Journal of Heat and Mass Transfer 37. 18(1994): 2859-2869.

3.17 Development of Jet Impingement and Ultra-Compact Thermal Management Systems for a Semiconductor Device with the Implementation of Dielectric Nanofluids

(Jordan Berg, Justin Clark, Sam Sisk, Roy Allen, and Sarvenaz Sobhansarbandi)

3.17.1 Executive Summary

High-power microwave (HPM) systems require powerful and compact cooling systems in order to maintain operational capabilities. A key component that requires significant heat extraction (several hundreds of watts up to 1 kW) are silicon photoconductive semiconductor switches (Si-PCSS). Many methods of thermal management have been studied, which include (in order from lowest to highest heat extraction performance) passive cooling (heat sinks, cooling fins), passive multi-phase cooling (heat pipes), active single-phase liquid cooling (microchannel cooling systems), or active single-phase turbulent cooling (jet impingement systems). To dissipate up to 1 kW of heat per unit area (heat flux of 1 kW/cm^2) to maintain the device temperature below 80 °C, a single-phase jet impingement cooling system was designed. The jet impingement thermal management system (JI-TMS) was studied computationally using computational fluid dynamics (CFD) modeling and experimentally through prototype fabrication and testing. The proposed JI-TMS consists of an array of nozzles, impinging fluid onto the heated target surface. The JI-TMS used a pure silicone fluid (PSF) heat transfer fluid (HTF), chosen for its dielectric strength for operation in close proximity to kilovolt-scale electric fields. The device was exposed to two different power levels of 100 W and 200 W. By simulation, the semiconductor yielded a maximum switch temperature of 54.7 °C and 99 °C, for 100 W and 200 W power, respectively. Experimentally, the recorded values were 57.5 °C and 98.2 °C, for 100 W and 200 W power, respectively. Maximum deviation error of 5.89% between the CFD and experimental results validated the reliability of the CFD model for further analysis. To further increase the performance of the system, nanofluid samples were created using various nanoparticles and surfactants. The selected nanofluid showed a 14.6% and 15.6% temperature reduction for 100 W and 200 W average power simulations, respectively. The results from CFD analysis of JI-TMS design with integration of nanofluid demonstrated the ability to compensate 100 W (100 W/cm^2) average power and maintain the average temperature of the Si-PCSS source below 50 °C (10 °C lower than a microchannel laminar-flow-based design of equivalent volumetric form-factor), in-line with the SWaP-C2 objectives. The proposed JI-TMS design has certain restrictions with regard to pressure threshold, i.e. the system's pressure should not be dramatically increased as it negatively affects the pumping power. Further iterations of the current design are unlikely to meet the stretch goal cooling requirement of >1 kW (1 kW/cm^2) due to the large pressure drop that occurs. While jet impingement as a method of heat transfer should still be considered a viable method, the viscosity of the fluid presented a challenge in being able to create turbulent regimes in the JI-TMS. To overcome this challenge,

decreasing the JI-TMS nozzle diameters by a factor of 10 and increasing the nozzle count by the same factor has the potential to increase convection of the coolant, thereby increasing heat extraction capabilities. With the goal of creating turbulency and increasing convective heat transfer, an ultra-compact TMS (UC-TMS) with the ability to remove 1 kW/cm^2 of heat in a short time frame was developed. The proposed UC-TMS was comprised of an array of micro-sized jet nozzles with four outlet ports on each side to reduce the distance of the fluid's path and consequently reduce the pressure drop. For the purpose of comparison, de-ionized water and silicone fluid were chosen as HTFs. The results showed an average surface temperature of 74 °C and 37 °C for de-ionized water and silicone fluid, respectively. The proposed UC-TMS has shown an increased performance in removing heat at the heated target surface, compared to JI-TMS, however, the pressure changes need to be further investigated and the design needs to be prototyped and experimentally investigated.

3.17.2 Objective

A thermal management system (TMS) is required for cooling semiconductor-based pulse-power devices, with the goal of maintaining device temperature below 80 °C to avoid chip malfunctions. In-line with the SWaP-C2 objectives, the proposed TMS must be capable of providing up to 1 kW of heat per unit area (heat flux of 1 kW/cm^2). Moreover, certain limitations should be considered for the pumping power. The TMS should be designed to be small enough to be used anywhere from data centers to drones, thus 1 cm^2 is targeted, with the capability of scaling up the dimensions. Integrated chip cooling is being widely used to dramatically increase the operational power of high-voltage silicon-based power devices. High power density electronics employing jet impingement TMS (JI-TMS), have achieved 10's-of-kW of average power handling capabilities. Current state-of-the-art (SOTA) devices: a) include thick thermal interface layers that increase the amount of material through which heat must be transferred to the coolant, thus limiting the heat removal rate; b) rely on working fluid in both natural/forced convection; and c) include chiller/pump systems which consume power to produce thermal compensation, resulting in extreme pressures (100's-of-psi) to achieve optimal flow regime and cooling metrics

To achieve said high cooling densities, in this study several TMS designs were proposed, including microchannel, single row JI, staggered JI, double outlet staggered JI, In-Chip and Ultra Compact (UC) TMS, to achieve an enhanced heat transfer rate via the creation of turbulent flow through a nozzle array design. The proposed TMS designs focus on addressing the issues raised in the SOTA, while improving overall system performance by keeping device temperature below the targeted threshold.

3.17.3 Technical Background

The utilization of a thermal management system (TMS) for a semiconductor device is virtually mandatory for pulse-power applications due to the large amount of energy transferred within applications. These devices receive a significant amount of power (i.e., heat) that is to be dissipated, which can result in the degradation of the device if not properly managed. Therefore, equivalently powerful TMSs are required to be developed

to prevent device performance degradation [1]. M. Mahalingam performed thermal management analysis in semiconductor device packaging. They concluded that for quality performance and reliability, it is essential to limit the maximum temperature of the semiconductor device, typically in a range of 80–125 °C, which leads to large improvements in the thermal performance of a variety of packaging styles in use [2]. The semiconductor devices can be made from various materials such as silicon (Si), gallium nitride (GaN) and silicon carbide (SiC), to name a few. Among these materials, silicon is more commonly utilized in semiconductors as it is extremely abundant, incredibly cheap, and the wafer manufacturing technology is far more mature in comparison to its less developed competitors (e.g., SiC and GaN). However, silicon becomes increasingly inefficient with respect to temperature rise, as there is an increase in electrical resistivity of silicon with an increase in temperature [3]. Therefore, there should be a defined threshold to maintain the device temperature for sustained operation of the system, which can be achieved by a proper cooling system.

There are different methods utilized for semiconductors, computer processors, and devices alike to maintain a desired threshold temperature of the system. These techniques include thermoelectric coolers (TECs), heat pipes, natural convection methods, and microchannel liquid cooling, among the more common approaches. Methods of heat removal by means of heat pipes, TEC's, or liquid cooling techniques require the addition of heat sinks or radiators. This can be attributed to the fact that heat sinks and radiators can be remotely located away from the device or processors. Therefore, only the initial heat extraction rates need be accounted for, not the cooling capability of the heat sinks and radiators. L. Zhu et al. performed simulation analysis on the optimal heat exchanger size of TECs for application in electronic cooling. The simulation results show that maximizing the heat extraction rate depends on the contact area of the TEC. Moreover, a maximum cooling rate of 5 W/cm^2 was achieved for a standard commercial TEC module with a heat extraction surface area of 6.2 cm^2 [4]. M. Manno, Bao Yang, Avram Bar-Cohen have shown that by using a 100 μm thick substrate in a TEC, the micro-contact enhanced TEC could significantly reduce the temperature gradient in the substrate created by a 5 W/cm^2 hotspot to just 1.1 K/mm [5].

The application of heat pipes as a viable heat transfer method is ubiquitous. Arya et al. compared various mass percentages of carbon nanotubes (CNTs) to non-modified deionized water in a heat pipe. It was concluded that the addition of CNTs can increase the performance of the heat pipe by 40%, with a heat extraction rate of 120 W/cm^2 [6]. Z. J. Zuo, M. T. North, and K. L. Wert found that heat pipes can handle heat fluxes of around 200 W/cm^2 without the evaporator drying out [7]. J. Li et al. examined the thermal performance of a copper–water flat heat pipe composed of a novel wick structure made of a sintered hybrid copper fine powder. The results from Li et al.'s study show that the heat pipe could dissipate up to 100 W/cm^2 in a horizontal orientation [8].

Passive methods of heat extraction struggle to handle heat fluxes greater than 100 W/cm^2. This is due to passive TMS designs primarily being performance limited, being driven by the temperature differential of the system and thus creating low heat transfer

coefficient buoyancy-driven flows. Danish Ansari and Ji Hwan Jeong created a pin fin hot spot heat sink and achieved a maximum heat extraction rate of 160 W/cm^2 [9]. Microchannel cooling systems have been widely implemented in different areas of power electronic applications. K. Jung et al. investigated strategies to remove high heat fluxes (up to 1 kW/cm^2) from wide band gap semiconductors (e.g., SiC and GaN). They found that while two-phase cooling systems show better performance compared to single-phase cooling methods, microfabrication techniques associated with the manufacturing of those systems are extremely challenging, and their 1 kW/cm^2 heat extraction goal was never realized [10]. Ljubisa D. Stevanovic et al. performed CFD and experimental analysis of a microchannel TMS for a set of diodes and IGBT's. Their simulations estimated a heat extraction rate of 470 W/cm^2, and achieved an experimental value of 350 W/cm^2 [11].

Liquid jet impingement cooling is an effective cooling technique which can result in a high cooling efficiency due to the absence of the thermal interface medium and the lateral temperature gradient. The dominant characteristic that makes the JI-TMS more attractive compared with the other TMSs, is that the theoretical heat transfer coefficient (the capability of the system to transfer the heat) obtained with this cooling methodology is higher compared with other systems. Using a high-velocity fluid is a method for obtaining a high heat transfer coefficient. By implementing a pressurized nozzle, such high velocities can be created. The high-velocity fluid then impinges onto the target heated surface. Impinging jets come in a few different arrangements, there are circular and rectangular nozzles. Figure 1 shows the cross section of the jet impingement, and corresponding heated surface to nozzle diameter.

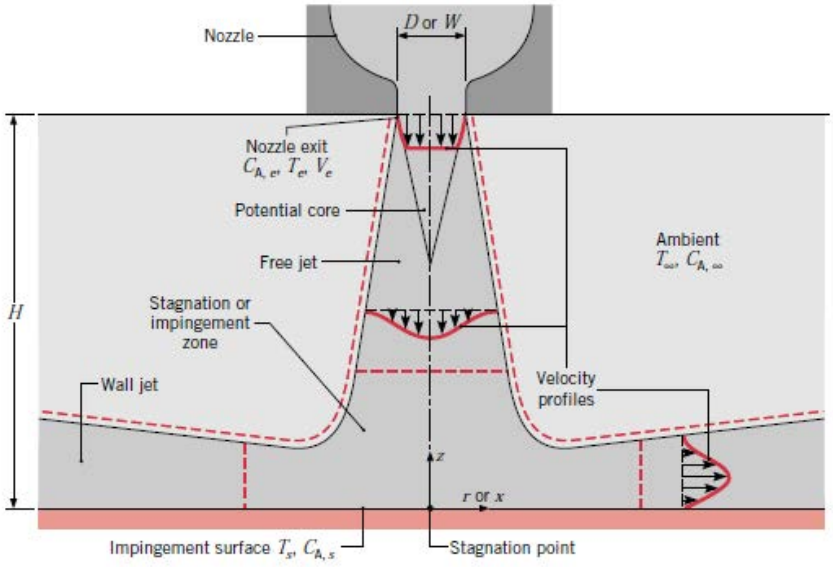


Figure 1. Cross section of the jet impingement system.

S. Narumanchi et al. performed a numerical analysis and computational fluid dynamics (CFD) modeling of single-phase and boiling-phase jet impingement cooling units, in which the selected type of heat transfer fluid (HTF) was water–glycol. Their simulation results suggested that single-phase jet impingement TMSs have the ability to dissipate heat fluxes up to 200 W/cm^2 [12]. K. Gould et al. had the most success with a jet impingement cooling system for a silicon carbide power module, achieving 167 W of heat removal [13]. Feng Zhou et al. concluded that the incorporation of jet impingement cooling systems would allow for power package sizes to decrease up to a factor of 10 if jet impingement cooling systems are utilized [14]. T. Tiwei presented a novel impingement based liquid cooling solution targeted to directly cool the backside of a high-performance chip. Their results show a low thermal resistance of 0.16 KW of the fabricated cooler for a low pumping power and the achievement of a heat flux of 500 W/cm^2 [15].

Summary of the state-of-the-art studies employing various cooling techniques and methodologies to investigate the system's performance are presented in Table 1. As it is shown in this table, the microchannel and liquid cooling methodologies were chosen for the purpose of this study, based on their potential capability in removal of a high amount of heat.

Table 1. Summary of state-of-the-art thermal management systems (TMSs).

Author	System	Method	Heat Flux
Arya et al. [6]	Heat pipe	Experimental	120 W/cm^2
Zuo et al. [7]	Heat pipe	Num & Exp	220 W/cm^2
Li, Lv [8]	Heat pipe	Experimental	100 W/cm^2
Ansari, Jeong [9]	Heat pipe	Numerical	160 W/cm^2
Stevanovic et al. [11]	Microchannel	Num & Exp	350 W/cm^2
Narumanchi et al. [12]	JI	Numerical	200 W/cm^2
Tiwei [15]	JI	Num & Exp	500 W/cm^2

3.17.4 Tasks, Milestones, and Status

Table 2. Tasks, milestones, and progress over 40 months project duration.

Tasks & Milestones	40 Months																					
	M1-M6			M7-12			M13-18			M19-M24			M25-M30			M31-M36			M37-M40		
Phase I, Task 1: Design and Comparison of Various TMS by CFD Modeling. (Berg)																						
Milestone 1: Desired design obtained, further needed modifications identified																						
Phase I, Task 2: Fabricated and tested the selected design with identified properties in Task 1. (Berg)																						
Milestone 2: Experimental and simulation results cross-validation, further needed enhancement on the heat transfer fluid identified																						
Phase I, Task 3: Thermal analysis of nanofluid based heat transfer fluid is performed by investigating the performance of 19 samples with different concentrations, properties of interest are specific heat capacity and thermal conductivity. (Berg)																						
Phase I, Task 4: CFD modeling of the TMS with the optimized HTF with high thermal capabilities. (Berg)																						
Milestone 3: Target heat removal rate achieved and the device temperature was well maintained below the desired operating temperature																						
Phase II: Design of a water-cooled integrated cooling system. (Clark)																						
Phase III: Design of a water-cooled ultra compact TMS (UC-TMS), with modified design of arrays of jets with the increased number of outlets to eliminate the pressure loss issue. (Sisk)																						
Milestone 4: Ultra Compact TMS design with high heat removal capability																						
	Deliverables																					
Technical reports																						
Journal, Conference Publications and Presentations																						
Final report																						

3.17.5 Methods and Approach

In this study, several TMS designs were developed including: microchannel, single row JI, staggered JI, double outlet staggered JI, In-Chip (IC), and Ultra Compact (UC). The TMS geometry was made in SOLIDWORKS/ANSYS Design Space Claim. Figure 2 shows the schematic of the developed TMS designs. For the purpose of this report and due to page limitations, the focus of the next few sections is on JI-TMS and UC-TMS, which were found to be the most effective compared with the other designs.

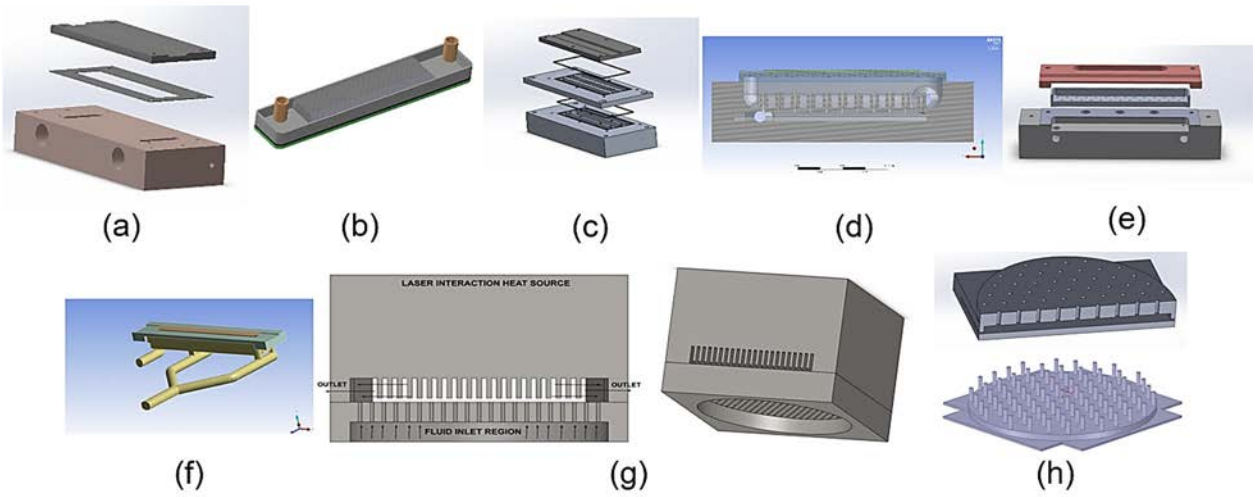


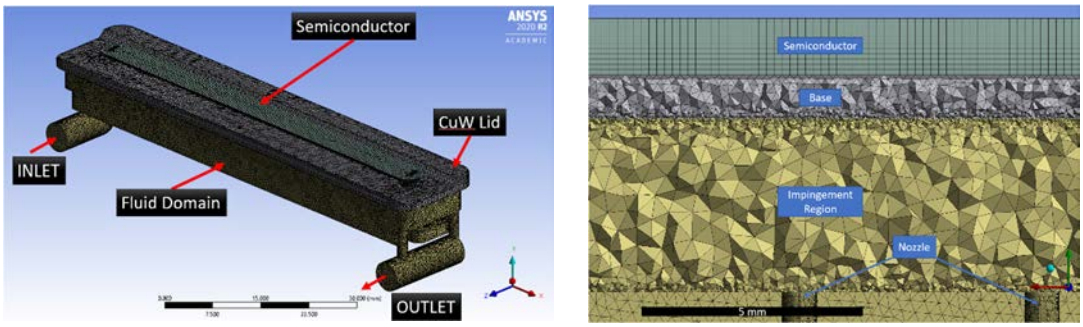
Figure 2. Various TMS designs developed in this work: (a) Crossflow (also a microchannel design), (b) Microchannel, (c) Array JI, (d) Single Row JI, (e) Staggered JI, (f) Double Outlet Staggered JI, (g) IC, (h) UC.

3.17.5.1 JI-TMS

The performance of proposed JI-TMS in this study was studied both by computational fluid dynamic (CFD) modeling (Phase I, Task 1), and experimental investigation (Phase I, Task 2). Furthermore, in order to evaluate the thermophysical properties of the selected heat transfer fluid (HTF) and improve its thermal characteristic by the integration of nanoparticles, thermal analysis of the fluid was performed (Phase 1, Task 3). The selected HTF was re-applied in the CFD modeling, and the results were compared (Phase 1, Task 4). The following subsections summarize these tasks.

CFD modeling (Phase 1, Task 1)

The JI-TMS design characteristics include nozzle-to-nozzle spacing, distance from nozzle exit to impingement surface, and nozzle diameter. In ANSYS software, the tetrahedral unstructured mesh was applied to the geometry with the patch conforming method to ensure mesh continuity (Figure 3). Face sizing of mesh areas were utilized in three areas to control the sizes of the elements where the geometry was smaller or the boundary layer was located. A grid independence study was performed with four different mesh sizes. The TMS model was then simulated under the transition shear stress transport (SST) viscous and k-omega model. Though the TMS is designed for a pulse-power application, pulsation of these devices is on the order of nanosecond time frames. The analysis was performed utilizing a constant heat generation throughout the volume of the semiconductor device along with a constant mass flow rate of heat transfer fluid (HTF) at the inlet. The HTF used in all simulations was a pure silicone fluid (PSF) with a viscosity of 20 centistokes (hereafter known as PSF-20-cSt).

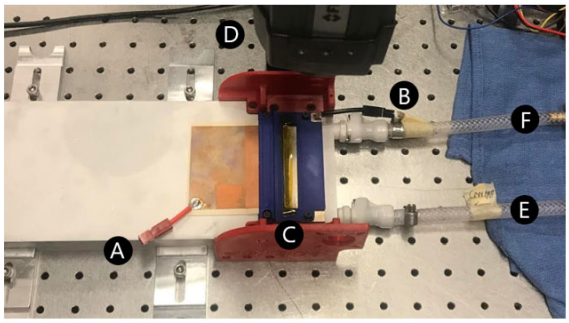


(a) (b)

Figure 3. (a) Ansys mesh setup, (b) close up view of fluid domain mesh.

Experimental analysis of the JI-TMS (Phase I, Task 2)

Validation of the JI-TMS model was performed experimentally to ensure the accuracy of the CFD results. The manufactured staggered array JI-TMS prototype consisted of five parts: a lid, a gasket, a base, a jet-plate, and a photoconductive semiconductor switch (PCSS) device. Once the parts were assembled, the semiconductor was soldered onto the Cu-W lid using a reflow oven to ensure a uniform bond (Figure 4). A chiller/pump was connected to the JI-TMS and was filled with PSF-20-cSt fluid sourced from Clearco. An inline, spring-actuated flow meter was used to monitor the flow rate. Pressure readings were taken from an inline pressure gauge. A FLIR camera was mounted directly above the PCSS and JI-TMS to monitor real-time temperature. Once the setup was completed, the camera and pump were turned on, followed by the power supply. The temperature of the PCSS was monitored until a steady state was reached, after which the power supply was turned off. The PCSS was allowed to cool until it reached near-ambient temperature.



A – Power connection
B – Ground
C – Switch and JI-TMS
D – FLIR A325sc
E – PSF-20cSt Inlet
F – PSF-20cSt Outlet

Figure 4. Experimental setup of JI-TMS.

Thermal analysis of the HTF (Phase I, Task 3)

As the HTF plays an important role on the system's overall performance, the thermal analysis of the HTF was performed to determine: (a) the deviation error between the

PSF's thermal properties and the manufacturer's reported value, and (b) the ways to improve its thermal characteristics. Several samples were placed in a platinum pan to be analyzed in a thermogravimetric analyzer (TGA). The TGA then heated the samples at a constant temperature ramp rate until a phase change occurred. These PSF samples were then weighed and hermetically sealed inside Tzero pans to be tested in a differential scanning calorimeter (DSC) to investigate their specific heat capacity (c_p) values at different temperatures. Once the results were obtained and compared with the manufacturer's reported values, further heat transfer enhancement of the HTF was performed. 18 nanofluid samples were created using various nanoparticles with different mass percentages with and without surfactants (Table 3). The thermal analysis of the developed nanofluid mixtures were performed with DSC and the results were compared.

Table 3. The developed nanofluid mixtures with various nanoparticles and surfactant mass percentages.

	SiC			Fe2O3			Al2O3		
Sample	1	2	3	1	2	3	1	2	3
Mass % NP	0.25	0.5	0.75	0.25	0.5	0.75	0.25	0.5	0.75
Mass % Surfactant	0.0043	0.0085	0.0128	0.0013	0.0025	0.0038	0.0125	0.0250	0.0375
Mass % Tergitol	0.0997	0.0995	0.0992	0.0997	0.0995	0.0992	0.0997	0.0995	0.0992
Actual % NP w/ surfactants	0.251	0.504	0.757	0.251	0.502	0.756	0.251	0.504	0.757
Actual % NP no surfactants	0.251	0.496	0.753	0.250	0.500	0.750	0.250	0.494	0.747

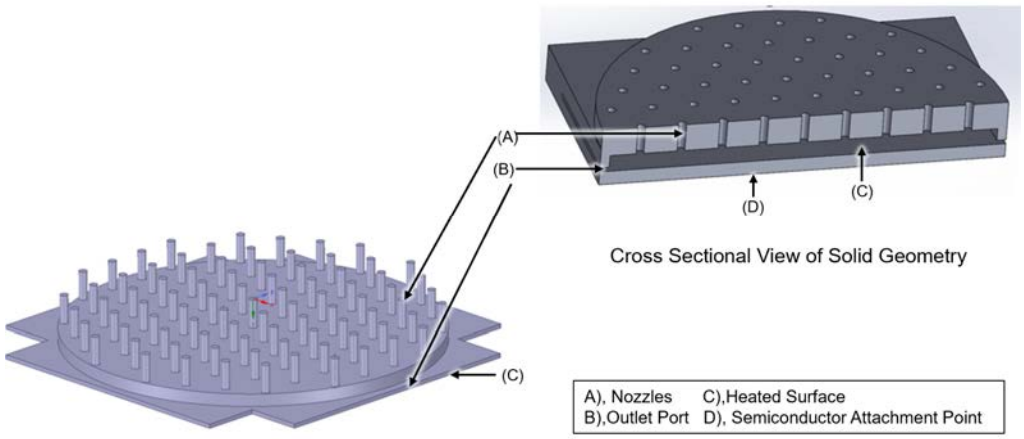
CFD modeling of the JI-TMS with optimized HTF (Phase I, Task 4)

Using the selected nanofluid mixture with enhanced thermophysical properties, the JI-TMS model was again simulated, and the results were compared with the PSF-20-cSt. For the purpose of the performance comparison, all other B.C.s remained the same for this analysis.

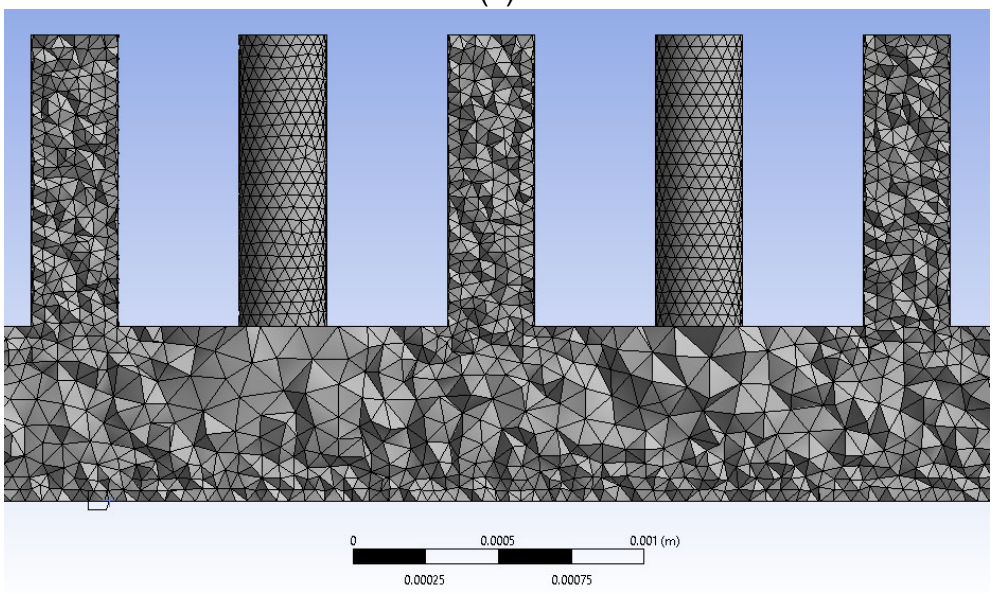
3.17.5.2 UC-TMS

The UC-TMS like the JI-TMS has geometric constraints such as nozzle to nozzle spacing (Ar), nozzle diameter (d), nozzle arrangement type, nozzle to target surface distance(H/d), and outlet placement and sizing. The geometric equations found within the literature were used in a way to maximize the amount of heat the fluid could extract from the target surface. The 1 cm^2 target surface allowed for 80, 0.3 mm nozzles in a triangular array. To maximize the heat transfer, the Ar ratio and H/d ratio are 0.04 and 2, respectively (Figure 5).

The CFD approach with similar B.C.s of the JI-TMS (mentioned in the CFD Modeling Section) was used to investigate the performance of the UC-TMS. Two different fluids, i.e., silicone fluid and de-ionized water, were chosen for the purpose of comparison.



(a)



(b)

Figure 5. UC-TMS: (a) Cross sectional view of fluid domain geometry, and (b) Cross sectional view of meshing in fluid domain.

3.17.6 Results and Discussion

3.17.6.1 JI-TMS

The significant results from the JI-TMS CFD simulation and experimental analysis are presented in Table 4. From the performed experiment, the maximum device temperature, coolant flow rate, and pressure were monitored. The pump/chiller used was pressure limited during the experimental test runs. This yielded a constant mass flow rate of 0.06 kg s coupled with a pressure drop of 263.7 kPa. The 100 W power dissipation in the semiconductor yielded a maximum switch temperature of 57.5 °C, while for the 200 W power a maximum switch temperature of 98.2 °C was recorded. The recording time measured the time to reach steady-state maximum temperature, at which point the power supply was turned off, then the pulse-power device was allowed to return to a steady

state low temperature. As the maximum temperature of the semiconductor was the primary concern, the temperature of the Cu–W lid was not measured.

Table 4. JI-TMS CFD simulation vs experimental results.

Avg Power Applied	CFD	Experimental	Difference
100 W	54.7 ℃	57.5 ℃	5.89 %
200 W	99.0 ℃	98.2 ℃	0.99 %

The obtained results showed maximum deviation error of 5.89% between the CFD and experimental results, which validated the reliability of the CFD model for further analysis. Comparing the CFD vs experimental results, it is noted that the CFD predicted the temperatures to be lower than the measured experimental values for 100 W of applied power. This could be caused by several factors, such as the relatively low resolution of the FLIR camera, which was used to measure the temperature, as well as the discrepancies in the applied power. Based on the reported results, the semiconductor device is likely to remain well under the 80 °C threshold that was set for the semiconductor when 100 W of power is applied. One flaw with the proposed JI-TMS design is the large pressure loss that occurs with the provided flow rate of 0.06 kg/s, recorded as 45.4 psi ± 0.5. While jet impingement flow regimes inherently require an increasingly large pressure drop to create more turbulent conditions, and by extension the heat transfer coefficient, the current model should be optimized to accommodate the largest pressure drop across the jet plate.

The obtained results from thermal analysis of the PSF-20c-cSt by DSC showed 13.12% difference on the specific heat capacity (c_p) compared with the reported value of the manufacturer, which could likely be the reason for the 5.89% difference in the simulation and experimental results. The specific heat capacity (c_p) results from the analysis of the developed nanofluid mixtures can be seen in Table 5. A 0.25 wt% mixture of silicon carbide with surfactants, with c_p of 1.254, was found to have the most significant heat capacity reduction which correlated with the greatest thermal conductivity enhancement of 3.5% among all the samples. The Maxwell equation, as represented below, developed by Yu and Choi was used to determine the thermal conductivity of the nanofluid mixture [16].

$$k_{nf} = k_{bf} \frac{kp + 2kbf + 2\varphi(kp - kbf)}{p + 2kbf - \varphi(kp - kbf)}$$

where φ represents the volume fraction of the nanoparticles in the fluid. Using this equation, the thermal conductivity of sample 1 was determined to be 0.147 W/mK versus the PSF 20cSt thermal conductivity of 0.142 W/mK, representing a 3.5% increase.

Table 5. Specific heat capacity results for various nanofluids.

Sample Number	Sample	Specific Heat Capacity (J/gC)
1	Silicon Carbide 0.25 wt %	1.254
2	Silicon Carbide 0.5 wt %	1.441
3	Silicon Carbide 0.75 wt %	1.442
4	Silicon Carbide 0.25 wt %*	1.538
5	Silicon Carbide 0.5 wt %*	1.570
6	Silicon Carbide 0.75 wt %*	1.451
7	Iron Oxide 0.25 wt %	1.464
8	Iron Oxide 0.5 wt %	1.549
9	Iron Oxide 0.75 wt %	1.59
10	Iron Oxide 0.25 wt %*	1.458
11	Iron Oxide 0.5 wt %*	1.462
12	Iron Oxide 0.75 wt %*	1.402
13	Aluminum Oxide 0.25 wt %	1.632
14	Aluminum Oxide 0.5 wt %	1.399
15	Aluminum Oxide 0.75 wt %	1.544
16	Aluminum Oxide 0.25 wt %*	1.376
17	Aluminum Oxide 0.5 wt %*	1.378
18	Aluminum Oxide 0.75 wt %*	1.430
19	PSF-20cSt	1.391

* No surfactant sample

Using the modified thermal conductivity value, new CFD simulations were performed for the 100 W and 200 W average power tests. Using the same setup, boundary, and initial conditions described in the CFD Modeling Section, but with the thermal conductivity value of the HTF as 0.147 W/mK, simulations were run using the 1.639M node mesh, as the mesh was shown to give accurate results when compared to the experimental results. After a convergence of 10^{-5} was seen for every residual, the simulations were stopped. The temperature contour plots of the 100 W and 200 W simulations can be seen in Figures 6 and 7, respectively. In order to reduce uncertainty in the theoretical thermal conductivity increase, sample 1 (SiC 0.25wt % with surfactants) was sent to a third-party to establish a measured thermal conductivity increase of the nanofluid over the base fluid. When the thermal conductivity of the sample was measured, the value was reported to be 0.197 W/mK. This value represents a 32.4% increase over the base fluid's thermal conductivity value as reported by the vendor, and a 25.4% increase over the theoretical thermal conductivity of sample 1. This 0.197 W/mK value was also used in the CFD model to gauge the maximum semiconductor temperature seen during the 100 W and 200 W average power simulations. Table 6 summarizes the results from the simulations using unmodified PSF-20cSt and the new results using the modified HTF with nanoparticles added, with the theoretical and measured thermal conductivity values.

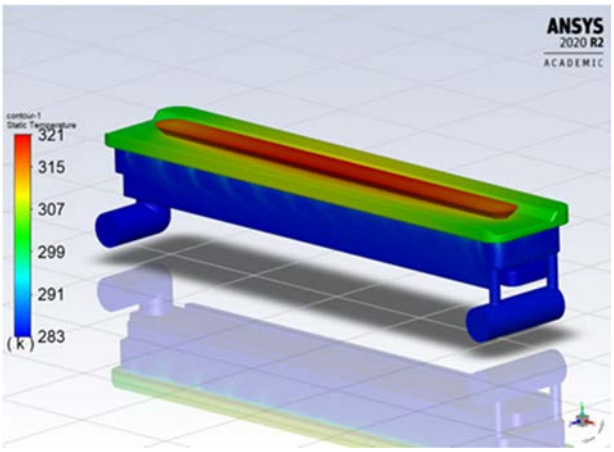


Figure 6. Temperature of the JI-TMS with nanofluid during 100 W average power.

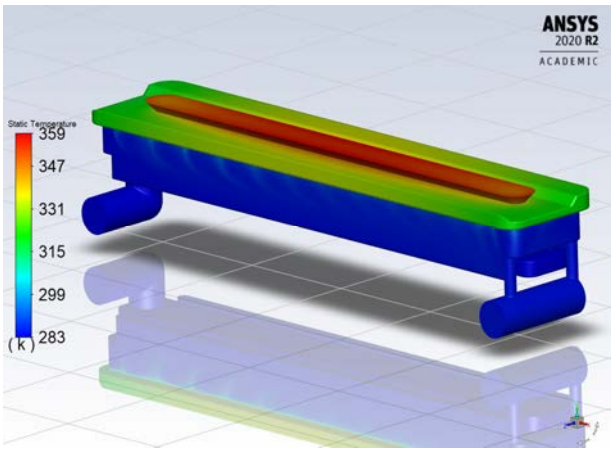


Figure 7. Temperature of the JI-TMS with nanofluid during 200 W average power.

As it can be seen from the CFD simulation results (represented in Table 6), even a small volume fraction of nanoparticles with a significantly higher thermal conductivity than that of the base fluid can impact the thermal performance of the JI-TMS. While the 200 W average power simulation still did not meet the 80 °C thresholds for the semiconductor device maximum temperature, the nanofluid HTF made a significant improvement in the reduction of the maximum temperature seen in the semiconductor device. With low volume fraction nanofluids generating heat extraction improvements of up to 15.6%, the incorporation of nanofluids into the JI-TMS will likely be utilized.

Table 6. Comparison of HTF performance on maximum semiconductor device temperature.

HTF	100 W Max. Temp (°C)	200 W Max. Temp (°C)
PSF-20cSt	54.7	99.0
Sample 1 k value(theory)	54.36	85.8
Sample 1 k value(measured)	46.7	83.49
% Improvement (theory)	0.6	13.3
% Improvement (measured)	14.6	15.6

3.17.6.2 UC-TMS

The achieved results from simulations using de-ionized water showed an average surface temperature of 74 °C, which is below the target temperature threshold of 80°C (which can be seen in Figure 9). By utilizing pure silicone fluid, with thermal conductivity of 0.0454 W/mK, the average surface temperature of 36.73 °C was achieved, which shows enhancement compared with the de-ionized water. Figure 8 shows the velocity vectors colored by temperature for both cases of water and silicone fluid, representing uniform heat distribution across the geometry for both fluids. Figure 9 shows JI contact displaying contour plot of uniform temperature distribution for the water, whereas some non-uniformity for silicone fluid.

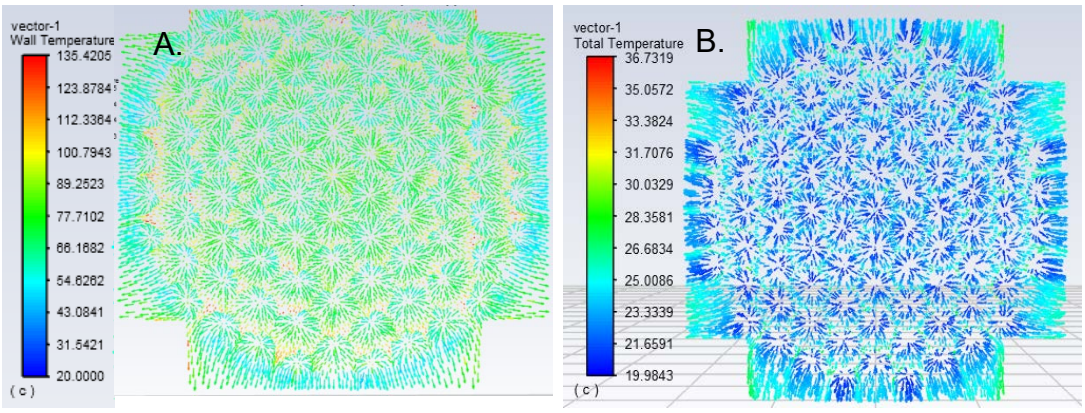


Figure 8. Top view of JI target surface, displaying contour plot of velocity vector colored by temperature. (A) Fluid is water; (B) fluid is pure silicone fluid.

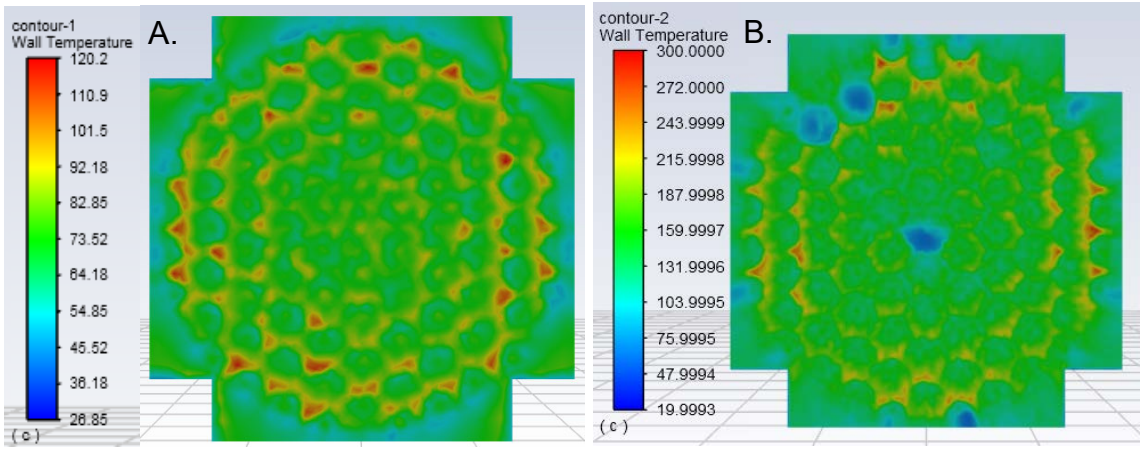


Figure 9. Top view of JI contact, displaying contour plot of temperature. (A) Fluid is water; (B) fluid is pure silicone fluid.

It was found that silicone fluid has an increased performance in removing heat at the target surface, the heat removal is limited due to viscosity being so high and the geometry being too small. However, the pressure drops need to be further investigated, which requires that the design be prototyped and experimentally investigated (future work).

3.17.7 Summary and Recommendations

The results from CFD analysis of the proposed JI-TMS design with integration of nanofluid demonstrated the ability to compensate 100 W (100 W/cm^2) average power and maintain the average temperature of the Si-PCSS source below 50 °C (10 °C lower than a microchannel laminar-flow-based design of equivalent volumetric form-factor), in-line with the SWaP-C2 objectives. The proposed JI-TMS design has certain restrictions with regard to pressure threshold, i.e., the system's pressure should not be dramatically increased as it negatively affects the pumping power. Further iterations of the current design are unlikely to meet the stretch goal cooling requirement of >1 kW (1 kW/cm^2) due to the large pressure drop that occurs. While jet impingement as a method of heat transfer should still be considered a viable method, the viscosity of the fluid presented a challenge in being able to create turbulent regimes in the JI-TMS. To overcome this challenge, decreasing the JI-TMS nozzle diameters by a factor of 10 and increasing the nozzle count by the same factor has the potential to increase convection of the coolant, thereby increasing heat extraction capabilities. With the goal of creating turbulency and increasing convective heat transfer, an ultra-compact TMS (UC-TMS) with the ability to remove 1 kW/cm^2 of heat in a short time frame was developed. The proposed UC-TMS was comprised of an array of micro-sized jet nozzles with four outlet ports on each side to reduce the distance of the fluid's path and consequently reduce the pressure drop. For the purpose of comparison, de-ionized water and silicone fluid were chosen as HTFs. The results showed an average surface temperature of 74 °C and 37 °C for de-ionized water and silicone fluid, respectively. The proposed UC-TMS has shown an increased performance in removing heat at the heated target surface, compared to the JI-TMS, however, the pressure changes need to be further investigated, which requires that the design be prototyped and experimentally investigated (future work).

3.17.8 Outputs

3.17.8.1 Publications

[1] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation," *International Journal of Thermal Sciences*, 172, 107254, **Feb 2022** [doi].

[2] J. Berg, and S. Sobhansarbandi. "CFD Modeling of Thermal Management Systems for a Silicon Semiconductor Switch." *ASME 2020 Heat Transfer Summer Conference collocated with the ASME 2020 Fluids Engineering Division Summer Meeting and the ASME 2020 18th International Conference on Nanochannels, Microchannels, and Minichannels*, Virtual, July 13–15, **2020**, American Society of Mechanical Engineers Digital Collection [doi].

3.17.8.2 Theses and Dissertations

[1] Jordan N. Berg, "Development of a Jet Impingement Thermal Management System for a Semiconductor Device with the Implementation of Dielectric Nanofluids," MS

Thesis in Mechanical Engineering, University of Missouri-Kansas City, **2021** [mospace].

3.17.8.3 Presentations

[1] S. Sisk and S. Sobhansarbandi, “In-Chip Cooling Technology within Semiconductor Switches,” *UMKC SUROP Symposium*, Kansas City, MO, September **2022** (Poster).

[2] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation”, Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29, **2021** (Poster).

[3] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures”, Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29, **2021** (Poster).

[4] J. Clark, R. C. Allen, and S. Sobhansarbandi, “Ultra-Compact Integrated Cooling System Development”, Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29, **2021** (Poster).

[5] J. Clark and S. Sobhansarbandi, “Ultra-Compact Integrated Product Cooling Technology,” *UMKC SUROP Symposium*, Kansas City, MO, September **2021** (Poster).

[6] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation”, UMKC OSPRES Grant Biannual Review, May **2021** (Poster Presentation).

[7] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures”, UMKC OSPRES Grant Biannual Review, May **2021** (Poster Presentation).

[8] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “Heat Transfer Potential and Pragmatism from Jet Impingement”, DEPS Posters and Presentations, Virtual, December 9, **2020** (Presentation).

[9] J. N. Berg, and S. Sobhansarbandi, “Thermal Design and Development of Cooling System for SiPCSS”, UMKC OSPRES Grant Biannual Review, September **2019** (Poster Presentation).

3.17.8.4 Students Graduated

1. Berg, Jordan, MS, Spring 21, Currently at: MRI Global, MO

3.17.8.5 Students Contributions

Sam Sisk (Spring 2022-Present)

Justin Clark (Spring 2021-Fall 2021)

3.17.9 References

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3.18 Tradespace Analysis of an Array of Electrically Small Antennas

(Bidisha Barman and Deb Chatterjee)

3.18.1 Executive Summary

The primary objective of this research was to investigate the functioning of a phased antenna array in the UHF range (0.3–1 GHz), which will have high gain (narrow beamwidth), reduced aperture area, high-power transmission, and beam steering capabilities (up to $\pm 60°$ from boresight). This involved two distinct efforts. First was the design, characterization, and experimental validation of a wideband electrically small antenna (ESA) element. Second, was to determine the extent to which the physical aperture size of an antenna array, composed of the designed ESA elements, could be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range, compared with present-art high-power-microwave-capable antenna arrays.

In this work, a technique to design wideband ($\geq 35\%$ bandwidth), high fidelity ($> 90\%$), coaxial probe-fed microstrip patch ESAs with improved power handling capabilities (~ 5 kW) and reasonable rE/V values, has been developed. The method has been experimentally validated in the 2.5–5 GHz range, using prototypes manufactured on TMM-6 and TMM-10i substrates, and in the UHF range (0.7–1.3 GHz), using a 3D-printed prototype on SLA substrate. Planar microstrip phased arrays, composed of the designed wideband, ESA elements, arranged in various lattice structures have been systematically studied. Investigations show that a transformation from square-grid-rectangular-aperture to triangular-grid-hexagonal-aperture leads to $\approx 46\%$ reduction in aperture area ($\approx 49\%$ reduction in number of array elements) with a tradeoff of ≈ 1.5 dBi (in 2.5–5 GHz) and ≈ 2.57 dBi (640–990 MHz range) gain reduction. The aperture area reduction, however, comes at the cost of limited beam steerability to $\pm 45°$ from boresight, compared to the $\pm 60°$ scanning capabilities achieved using the square-grid-rectangular-aperture arrays, at all frequency ranges.

3.18.2 Objective

The primary objective of this sub-project is to determine the extent to which the physical aperture size of an antenna array can be reduced while maintaining performance, in peak power density, bandwidth, and electronic beam steerability, over the UHF range (0.3–1 GHz), compared with present art high-power-microwave (HPM) capable antenna arrays.

The State-of-the-Art (SOTA) ultrawideband (UWB) antenna elements used for HPM capable antenna arrays include Horn, reflector, Vivaldi, and Valentine antennas. However, all these antenna elements have the common disadvantage of large physical aperture area. Therefore, the solution space includes the use of *electrically small antenna* (ESA) elements to make up the array. Since, miniaturization of antennas imposes a limitation on its gain-bandwidth product, the goal would be to optimize the ESA elements in terms of both bandwidth and boresight gain, followed by their arrangements in suitable

lattice structures (preferably, hexagonal/triangular) to achieve more than 20% overall aperture area reduction, compared with the present-art. Finally, this work also aims to provide a design guideline for UWB, coaxial probe-fed microstrip patch ESA elements and arrays for HPM applications.

3.18.3 Technical Background

High power microwave (HPM) systems are currently envisioned as viable alternatives to the conventional kinetic warfighting weapons, due to their capability of producing electromagnetic waves harmful to electronic equipment [1], [2]. The primary goal for an antenna, in this application framework, is to deliver effective radiated power (ERP), in 100s of MW, on to a specified angle in space, to achieve a required power density (as shown in Figure 1(a)). Arrays are preferred to fixed aperture antennas due to their capability of producing directive beams that can be electronically steered [3]. The specific power density S at a certain distance R from the array can be related to the realized gain G^R and input peak power P_{in} by the well-known equation [3]:

$$S(\theta,\phi) = \frac{P_{in}}{4\pi R^2} G^R(\theta,\phi)$$

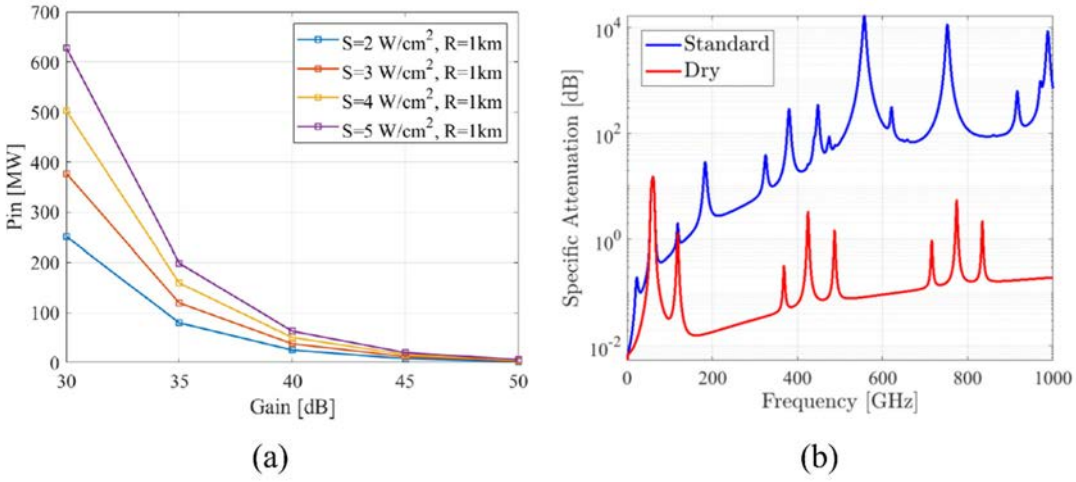


Figure 1. (a) Input peak power to the array vs. gain at 1 km from the antenna array. (b) Atmospheric gas attenuation spectrum obtained using the International Telecommunication Union (ITU) atmospheric gas attenuation model (via MATLAB).

Clearly, high power density can be achieved either by using a very high gain antenna and/or by supplying high peak power to the array. Although high power antennas appear to be an attractive solution, generating high power is economically and volumetrically undesirable. This leaves us with the choice of using high gain antennas, which are easy to develop when there is no area or real estate restriction. The problem arises when, to mitigate the atmospheric attenuation (see Figure 1(b)) and enable a compact radiator, the array must be designed at low frequency (0.3–1 GHz) with closely spaced elements; the antenna design now faces the major challenge of low gain and large physical aperture area.

Furthermore, to radiate short rise time pulses, the array antenna elements must have wide bandwidth (BW), typically varying from a few 100 MHz to 10 GHz [4]. This is because the antenna BW is inversely proportional to the rise time (t_r) of the input signal and is given by: $t_r = \frac{0.35}{BW}$.

The State-of-the-Art (SOTA) ultrawideband (UWB) antenna elements used for HPM-capable antenna arrays include horn, reflector, Vivaldi, and Valentine antenna elements. However, all these elements have the common disadvantage of large physical aperture area. One way to tackle the problem of large aperture area is to use and adapt *electrically small antenna* (ESA) theory to the individual and ensemble of radiating elements that make up the array. The two most important antenna parameters, viz. gain (or directivity) and bandwidth, are best captured using the gain-bandwidth product. Small antenna theory suggests that miniaturization of antennas imposes a limitation on their gain-bandwidth product [5], [6], leading to an inherent trade-off.

The information gleaned from the literature survey shows that microstrip patch antennas can be an attractive choice for antenna elements in a phased array due to their light weight, small size, monolithic designs, and performance tractability. However, conventional coaxial probe-fed patch antennas have two inherent drawbacks: (1) low impedance BW ($\sim 8-10\%$) [7] and (2) excitation of surface wave (SW) modes, which often manifests itself in the form of edge diffractions leading to scan blindness in a phased array. In this work, we aim to identify a microstrip patch based, ESA element, suitable for HPM-capable phased array applications, with comparable performance (in terms of BW, gain, HPM pulse transmission capabilities, etc.) with respect to the SOTA antenna elements.

3.18.4 Tasks, Milestones, and Status

The entire project has been primarily divided into four tasks:

No.	Task	Milestones	Status
(A)	Antenna element design and characterization	Developed a novel design technique for electrically small, coaxial-probe-fed, microstrip patch antenna that provides $\geq 30\%$impedance BW at operating frequencies in the UHF (MHz) to microwave (GHz) frequencies.	Complete
(B)	Manufacture and validate element performance	Validated the antenna design approach from MHz to GHz frequency range across various substrate parameters.	Complete
(C)	Antenna array design and characterization	Designed and systematically characterized planar microstrip phased arrays with reduced aperture architecture ($\sim 30\%$ reduction), without significant performance degradation, in terms of boresight gain (< 3 dBi reduction), beam-steering, power density, and high-power-handling capabilities.	Complete
(D)	Manufacture and validate antenna array performance	Validated design approach using a 3×3 array of wideband antenna elements in the 2.5–\5 GHz range.	Partially complete

3.18.5 Methods and Approach

3.18.5.1 Antenna Element Design

The wideband, microstrip patch ESA element design includes two steps: selection of optimum substrate parameters for surface wave (SW) reduction, followed by implementation of bandwidth enhancement technique.

(A) Optimum Substrate Selection

Broadband microstrip patch antennas designed on thick dielectric substrates tend to excite higher order SW modes [8]. As a result, phased arrays composed of such antenna elements can experience scan blindness [9]. In this section, a method to reduce higher order SW modes in a wideband microstrip patch antenna, by selecting optimum substrate parameters, is addressed.

To that end, in a single layer, grounded dielectric (of thickness h), the cutoff frequency of the nth order SW mode is given by [10]:

$$f_c = \frac{n}{4h\sqrt{\epsilon_d \mu_d - \epsilon_0 \mu_0}}$$

For TM modes, n = 0, 2, 4, ... and for TE modes, n = 1, 3, 5, ... The constitutive parameters of air and dielectric substrate are ϵ_0, μ_0 and ϵ_d, μ_d respectively. This implies that the dominant TM_0 SW mode propagates unattenuated with a zero-cutoff frequency (n = 0) and is difficult to suppress completely.

To reduce the impact of SW excitation, the first step is to select the operating frequency range of the antenna well below the cutoff frequency of the next higher order TE_1 SW mode ($f_h < f_c^{TE_1}$; f_h is the highest operating frequency of the antenna). In addition, the substrate parameters $h\sqrt{\epsilon_r}/\lambda$ must be selected in such a way that they correspond to a lower magnitude of residue associated with the dominant TM_0 SW mode. The details can be found in [11].

(B) Bandwidth (BW) Enhancement

For bandwidth enhancement, the generalized cavity model (GCM) [7] provides a good guideline for the canonical topology of a probe-fed patch. It was found using parametric studies based on GCM that the coaxial probe strategically positioned along the patch diagonal, at 2/3rd the distance between the patch center and corner gave the best results for the BW, without any reduction in gain. Validation of this feature was carried out using full-wave simulations (via Altair FEKO, CST Microwave Studio, and Ansys HFSS) and experiments [12] that confirmed this hypothesis. (To the best of our knowledge such an efficient patch design has not been reported till date [7].) The complete design flowchart

and the schematic of the proposed, wideband, microstrip patch antenna element is shown in Figure 2(a) and (b), respectively.

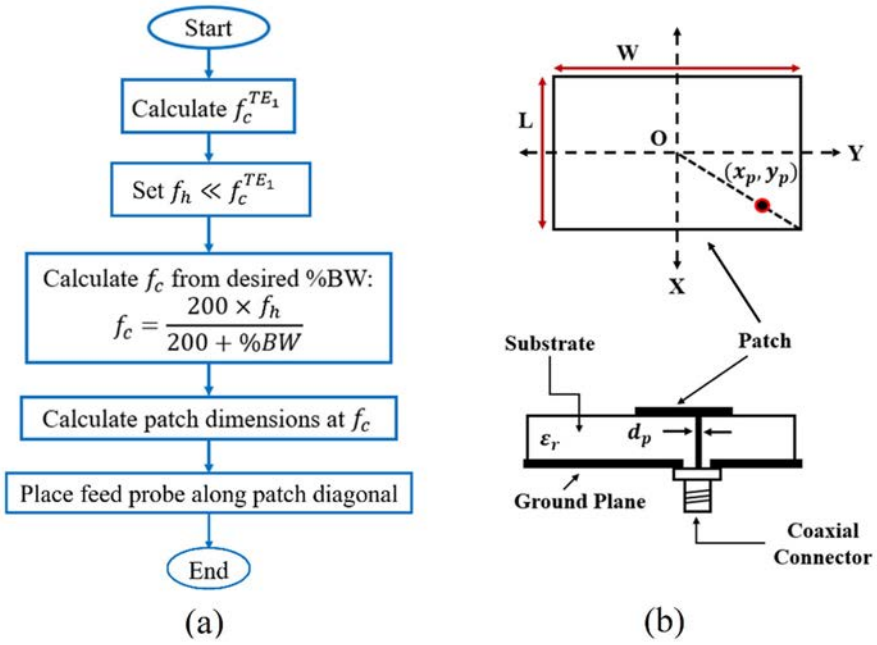


Figure 2. (a) Flowchart of the proposed, wideband, coaxially-fed, microstrip patch antenna design. (b) Schematic of the proposed antenna with probe location (x_p, y_p).

(C) *High Power Handling Capability (PHC)*

To achieve $> 30\%$ impedance BW from a coaxial-probe-fed microstrip patch antenna, the feed-probe should have a radius $r_p \geq 0.005\lambda$ (λ is the wavelength at the center frequency of operation) and must be placed strategically along the patch diagonal. This means at the desired UHF range (0.6–1 GHz) the radius of the feed-probes must be $r_p \gg 2$ mm. The commercially available SMA connectors that are normally used to feed microstrip patch antennas have $r_p \approx 0.65$ mm. Moreover, they can handle only about 400 W of input peak power at 1 GHz, which is undesirable for high power applications.

Therefore, to meet the requirements, a customized, tapered, coaxial connector (with $r_p \gg 0.005\lambda$) has been modeled. The cross-sectional schematic of the tapered coaxial connector is shown in Figure 3. It consists of two dissimilar coaxial lines with different dimensions and characteristic impedances (Z_1 and Z_3). The center conductor of the thicker section is used to excite the microstrip patch and has a radius, $r_{i1} = 6$ mm. The center conductor of the thinner section has the dimension of a commercially available SMA or N-type connector, viz. $r_{i3} = 0.65$ mm. An intermediate tapered section is used to match the characteristic impedances of these two coaxial sections. The tapering is necessary as the antenna must be connected to the ports of standard instruments (e.g., VNAs and/or signal generators). Also, this arrangement helps to improve the overall PHC, which has been verified using the thermal analysis of the models.

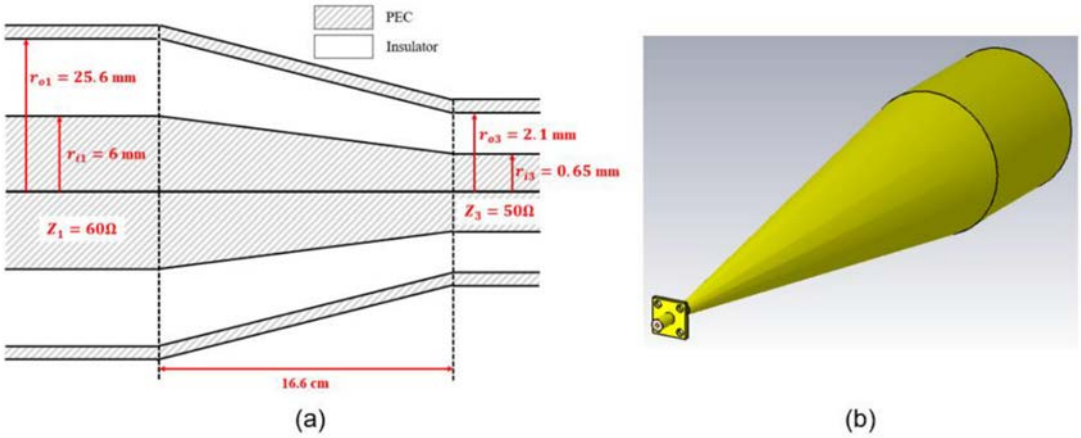


Figure 3. (a) Schematic and (b) CAD model of the tapered coaxial connector.

3.18.5.2 Array Antenna Design

Initially, a 15×15 square-grid array is modeled using the proposed, tapered coaxial-connector-fed, wideband, microstrip patch antenna elements arranged in a square aperture. The inter-element spacing d is calculated using the equation [13]:

$$\frac{d}{\lambda_h} \leq \frac{1}{\sin\theta_{sm} + \sin\theta_G}$$

Where, λ_h is the wavelength at the highest operating frequency, and θ_{sm} and θ_G are the maximum scan angle and the angle of closest grating lobe, respectively. To avoid interference between the main and grating lobes within the visible region: $\theta_G > \theta_{sm}$. Thus, for a maximum scan of $60°$, if the grating lobe location is fixed at $90°$, $d \leq 0.5359\lambda_h$.

To study the effect of reduced aperture area, some antenna elements from the four corners of the 15×15 square-grid-rectangular-aperture array are removed to form a hexagonal aperture. It has been shown in the literature that the number of antenna elements in an array can be reduced by 13.4% if they are arranged in a triangular lattice instead of a square one, within the same aperture area. Therefore, to reduce the number of antenna elements, the hexagonal aperture is populated by antenna elements arranged in a triangular grid. The maximum allowable inter-element spacing d in a triangular lattice is [13]:

$$\frac{d}{\lambda_h} \leq \frac{1.1547}{\sin\theta_{sm} + \sin\theta_G}$$

For a maximum scan of $60°$, if the grating lobe location is fixed at $90°$, $d \leq 0.6118\lambda_h$. Within the hexagonal aperture, the number of antenna elements (arranged in triangular lattice) are varied by changing d from $0.485 - 0.61\lambda_h$, resulting in three different arrays with 183, 139, and 114 elements.

All the four planar arrays (i.e., 15×15, 183-, 139-, and 114-Hex) are characterized, in terms of boresight gain, beam steering capabilities, and half-power beamwidths, via full-wave simulations in FEKO. The transformation from square-grid-rectangular-aperture to triangular-grid-hexagonal-aperture is shown in Figure 4.

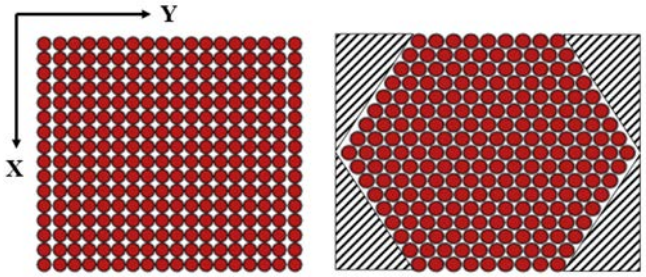


Figure 4. Schematic of (a) a square-grid-rectangular-aperture and (b) a triangular-grid-hexagonal-aperture array. The shaded region in (b) indicates removed elements for a square to hexagonal aperture transformation.

3.18.6 Results and Discussion

3.18.6.1 Antenna Element Design and Validation

Using the proposed methodology, initially two antenna elements were designed on TMM-6 and TMM-10i substrates, for operation in the 2.5–5 GHz range. Both antennas were fed by commercially available SMA connectors, placed at 2/3rd distance along the patch diagonal. The optimized design parameters of the antennas are enlisted in the first two rows of Table 1. Figure 5 shows the manufactured prototypes. A comparison of the measured and the simulated S_{11}-parameters and realized gains of the antennas are illustrated in Figure 6. Around 33% and 54% of impedance BWs were achieved, with an average gain of 5.5 dBi, from the two antenna elements, respectively. Furthermore, the antenna designed on TMM-10i substrate qualified as a quasi-ESA as its $ka = 0.67$ (Note: antennas are classified as ESAs when their electrical size $ka \leq 0.5$).

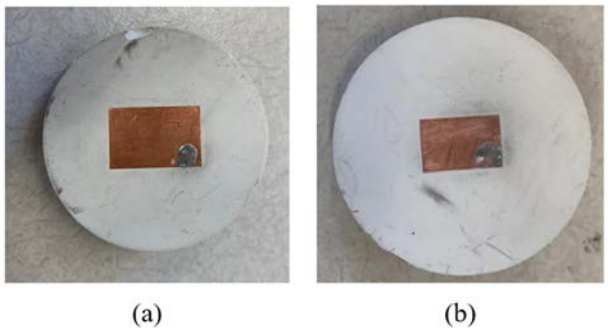


Figure 5. Manufactured prototypes of the coaxial-probe-fed microstrip patch antennas on 6.35 mm thick, circular-shaped, PEC-backed (a) TMM-6 ($\epsilon_r = 6, \tan\delta = 0.0023$) and (b) TMM-10i ($\epsilon_r = 9.8, \tan\delta = 0.002$) substrates, with the feed-probe placed along 2/3rd of the patch diagonal.

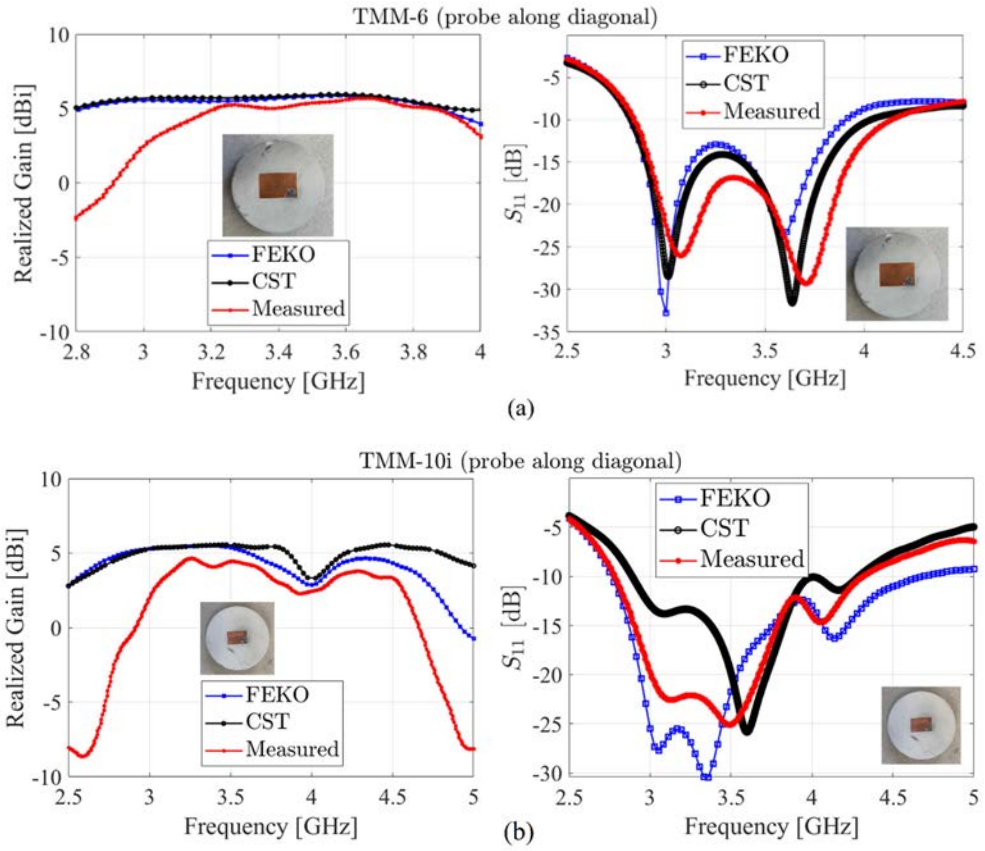


Figure 6. Simulated and measured realized gain and S_{11}-parameters of the coaxial-probe-fed, wideband, microstrip patch antenna, designed on (a) TMM-6 ($\epsilon_r = 6, \tan\delta = 0.0023$) and (b) TMM-10i ($\epsilon_r = 9.8, \tan\delta = 0.002$) substrates.

Having achieved satisfactory proof-of-concept of the proposed antenna design approach, at the high frequency range, the final prototype is manufactured for operation at the targeted UHF range (0.7–1.3 GHz). The antenna is manufactured on a 3D printed SLA substrate and is fed by a tapered, coaxial connector (Figure 7). The optimized antenna parameters can be found in Table 1.

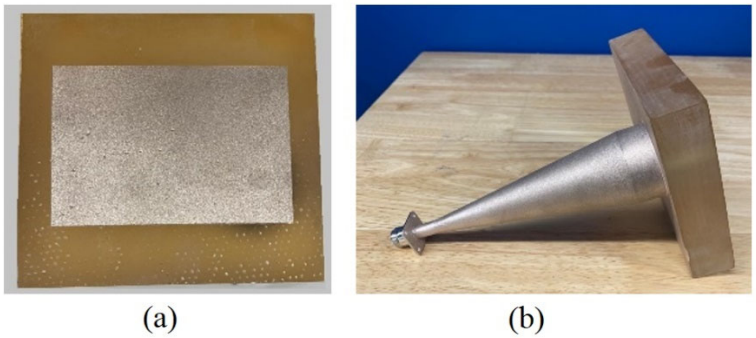


Figure 7. (a) Front and (b) side views of the tapered, coaxial-probe-fed, microstrip patch antenna manufactured on a 31.75 mm thick, PEC-backed, SLA ($\epsilon_r = 2.6, \tan\delta = 0.015$) substrate, for operation in the 0.7–1.3 GHz frequency range.

Table 1. Optimized design parameters of the wideband, coaxial-probe-fed, microstrip patch antennas designed on various substrate parameters.

Substrate	h (mm)	L (mm)	W (mm)	(x_p, y_p) (mm, mm)	r_p (mm)
TMM-6 ($\epsilon_r = 6$)	6.35	12.77	19.155	(4.26, 6.38)	0.65
TMM-10i ($\epsilon_r = 9.8$)	6.35	9.61	14.42	(3.20, 4.80)	0.65
SLA ($\epsilon_r = 2.6$)	31.75	80.54	120.81	(26.85, 40.27)	6 to 0.65

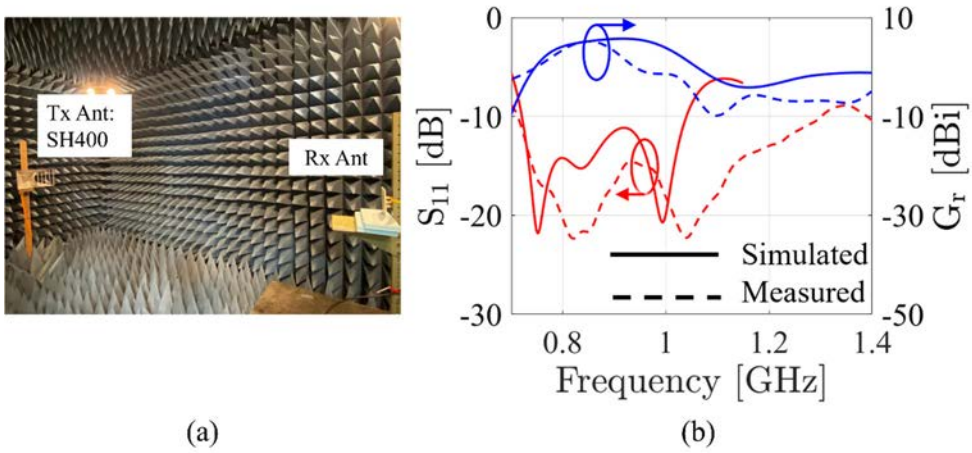


Figure 8. (a) Measurement setup. (b) Measured and simulated S_{11}-parameter and realized gain of the tapered, coaxial-connector-fed, wideband, microstrip patch antenna manufactured on SLA substrate.

Figure 8(a) shows the measurement setup, in the anechoic chamber, used for all the antenna measurements. A comparison between measured and simulated antenna parameters of the tapered, coaxial-connector-fed, SLA patch antenna is illustrated in Figure 8(b). Around 58% of measured impedance BW is achieved using the prototype.

Before subjecting an antenna to high power input pulses, its PHC is determined via simulation based thermal analysis, performed using Altair OptiStruct software. The thermal profiles of various antenna elements (as shown in Figure 9) that are designed using the proposed method, subjected to input peak power P_{in}, are studied. It is seen that the tapered-connector-fed antennas designed on TMM-10i and SLA substrates can handle $P_{in} \approx 4.5$ kW and ≈ 7 kW, respectively, without reaching the oxidization temperature of the copper surfaces. This is a significant improvement in the PHC of a simple microstrip patch antenna which can typically handle a few 100s of watts of input power.

After identifying the maximum PHC of the SLA prototype, it is subjected to various short rise time pulses, as shown in Figure 10. The high rE/V values (Table 2) indicate the suitability of the designed antenna element in transmitting sharp-rise-time pulses.

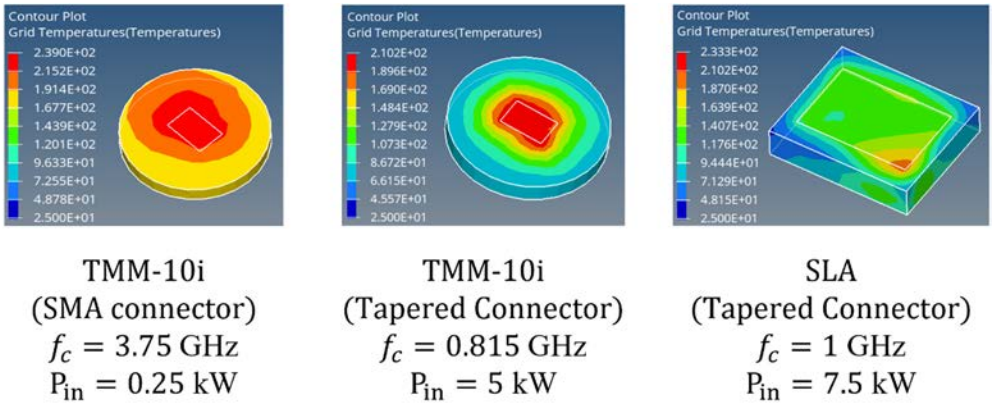


Figure 9. Thermal profiles of the antennas designed on various substrates and fed by different connectors.

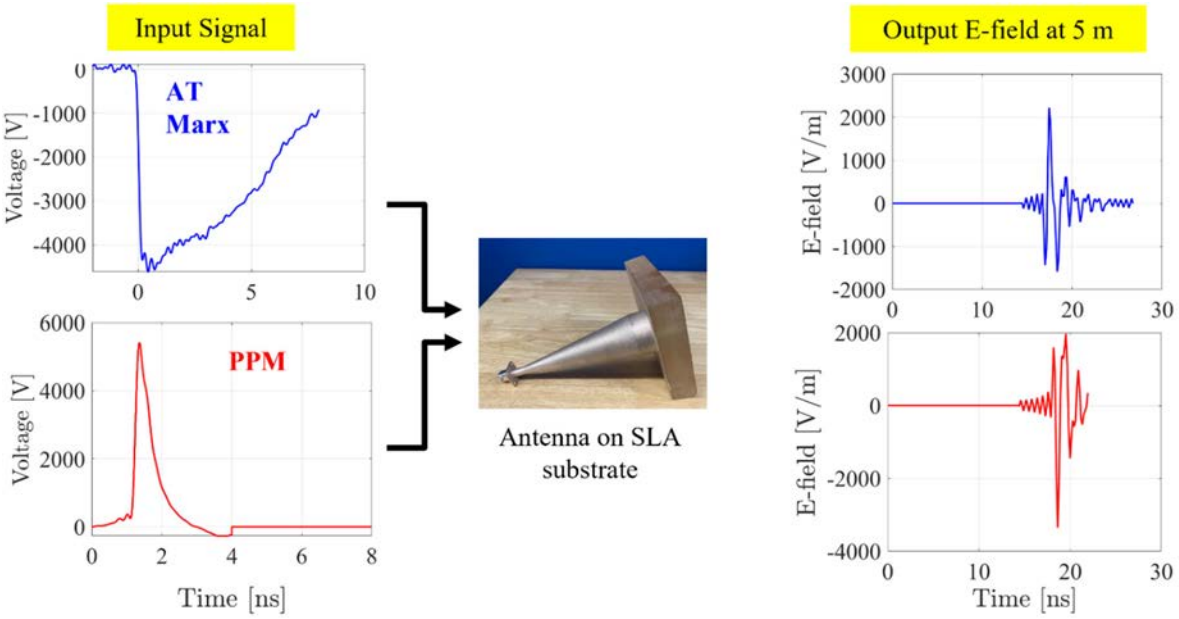


Figure 10. Time-domain E-field of the SLA patch antenna subjected to two different short rise-time input pulses.

Table 2. Optimized design parameters of the wideband, coaxial-probe-fed, microstrip patch antennas designed on SLA substrate.

Substrate	AT Marx		PPM	
	E-field (V/m)	rE/V at 5 m	E-field (V/m)	rE/V at 5 m
SLA ($\varepsilon_r = 2.6$)	2217.89	2.40	1967.72	1.82

3.18.6.2 Array Antenna Design and Validation

Using the proposed design technique, a tapered coaxial-connector fed, wideband, microstrip patch, ESA element was modeled on a 1.05-inch thick, TMM-10i substrate, for operation in the UHF range. The antenna was shown to provide $\sim 43\%$ impedance BW (0.64–0.99 GHz) with an average boresight gain of 5.65 dBi. Several of these antenna elements were arrayed to form a 15×15 array, with a surrounding ring of dummy elements, essentially making it a 17×17 array. The inter-element spacing was fixed at $d = 0.485\lambda_h$, with λ_h calculated at 990 MHz. The schematic of the 15×15 array is shown in Figure 11, and its characteristics are summarized in Table 3.

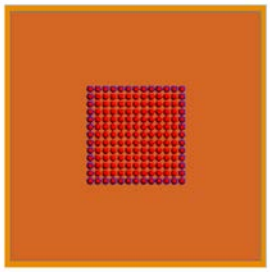


Figure 11. Schematic of the 15×15 planar array modeled in Altair FEKO, with a ring of dummy elements to improve its radiation performance.

Table 3. Summary of the 15×15 planar array parameters. (All results obtained using full-wave simulations in FEKO.)

No. of active elements	Radiating aperture area (m^2)	Volume (m^3)	Max. Gain (dBi)	Beam steerability	3-dB beamwidth Or HPBW	Impedance Match	PHC	Power density at 0.5 km
225	5.77	0.15	27.76	$\pm 60°$	$10.6°$at 0.64 GHz. $6.9°$ at 0.99 GHz.	50 Ω	1.012 MW (4.5 kW per element)	0.0318 W/cm^2

The effect of aperture area reduction on various array parameters is studied next, by systematically characterizing planar arrays of different aperture areas and lattice arrangements. As mentioned earlier in section 1.5.2, the 15×15 square-grid-rectangular-aperture array was transformed to triangular-grid-hexagonal-aperture arrays, with various inter-element spacings, resulting in three array configurations, viz. 183-Hex, 139-Hex, and 114-Hex. Performance comparison of the four different planar array configurations is provided in Table 4.

Table 4. Performance comparison of the various planar array configurations. (All results obtained using full-wave simulations in FEKO.)

Array	Element spacing (d/λ_h)	Aperture Area ($\mathbf{m^2}$)	Max. Gain (dBi)	PHC (MW)	Power Density at 0.5 km ($\mathbf{W/cm^2}$)	Scan Range (deg)
15×15 (With dummy elements)	0.485	5.77	27.76	1.012	0.0318	$\pm 60°$
183-Hex	0.485	3.10	26.09	0.8235	0.0104	f_L: $\pm 50°$
139-Hex	0.56	3.12	25.66	0.6255	0.0073	f_C: $\pm 45°$
114-Hex	0.61	3.16	25.19	0.513	0.0054	f_H: $\pm 45°$

Data in Table 4 shows that a transformation from square-grid-rectangular-aperture to triangular-grid-hexagonal-aperture leads to $\approx 45\%$ reduction in aperture area (5.77 to 3.16 m^2). This corresponds to $\approx 49\%$ reduction in the number of array elements (225 to 114) with a tradeoff of 2.57 dBi gain reduction (27.76 to 25.19 dBi). The aperture area reduction, however, comes at the cost of limited beam steerability to $\pm 45°$ from boresight, compared to the $\pm 60°$ scanning capability achieved from the square-grid-rectangular-aperture array, at all frequency ranges. Figures 12 and 13 show the comparison in boresight gain and beam steerabilities of the various array configurations considered above.

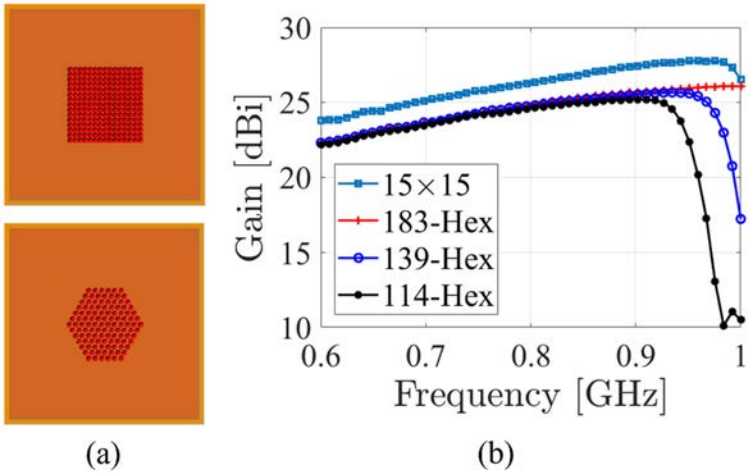


Figure 12. (a) FEKO simulation models of the planar arrays. (b) Boresight gain vs. frequency of the different planar array configurations.

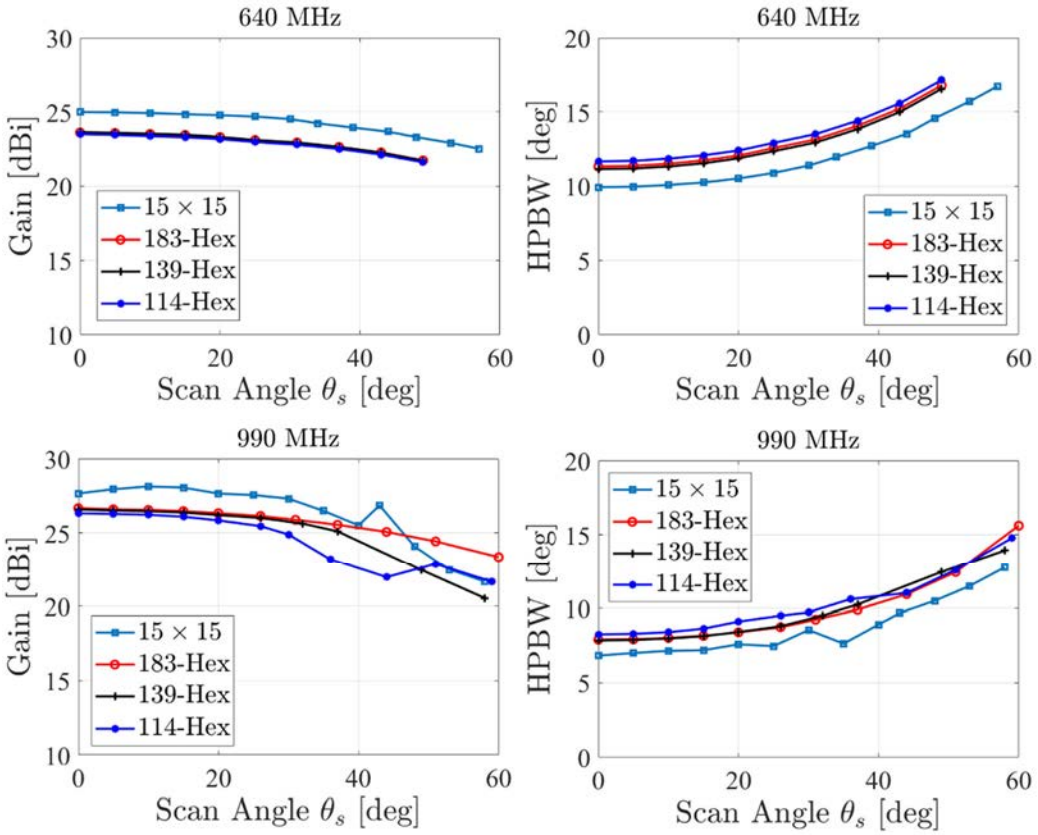


Figure 13. Gain and HPBW of the arrays as functions of scan angle at the lowest (640 MHz) and highest (990 MHz) frequencies of operation.

Due to unavailability of 1.05”-thick, TMM-10i substrate panel from the manufacturer, the array design methodology was validated on a smaller 3×3 array, on a 6.35 mm-thick, TMM-10i substrate panel, for operation at the 2.5–5 GHz range. Figure 14 shows the manufactured prototype of the 3×3 array. The measured and simulated S_{11}-parameters and realized gains of all the active antenna elements, within the array, showed reasonable agreement. For brevity, only the performance of the active center-most element is shown here, with the remaining antenna elements being matched terminated.

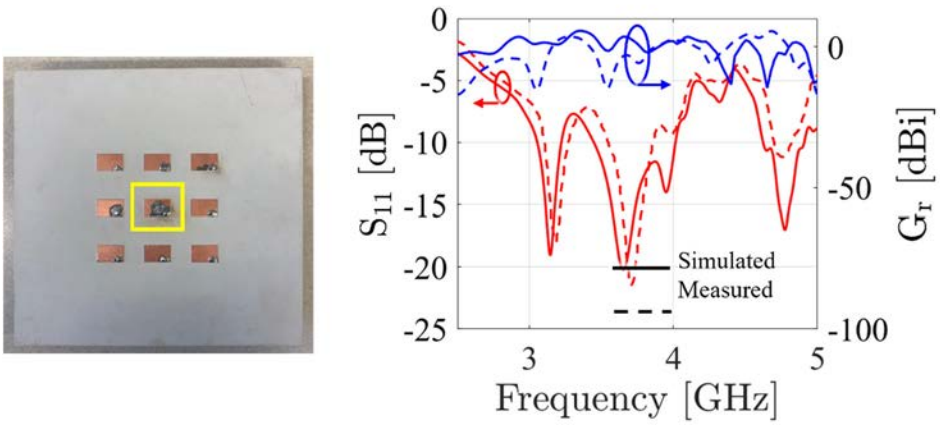


Figure 14. A 3×3 array of wideband (2.5–5 GHz) microstrip patch antenna elements and the comparison between the measured and simulated antenna parameters when only the center-most element of the array is excited, while others are matched-terminated.

3.18.7 Summary and Recommendations

In this work, a novel, wideband, electrically small, microstrip patch antenna design that provides $\geq 30\%$ impedance bandwidth, by strategic placement of the feed-probe along the patch diagonal, at UHF (MHz) to microwave (GHz) frequencies, has been proposed and experimentally validated. A method to diminish the excitation of surface waves, which often manifests as scan blindness in a phased array, by appropriate substrate parameter selection, has been introduced. The overall design method avoids any sophisticated prototyping and is a transformative approach in the design of electrically small microstrip antennas for UWB wireless applications.
The effects of different aperture shape and lattice arrangements on array gain and beam steerability have been studied for arrays modeled on PEC-backed substrates. Investigations show that a transformation from square-grid-rectangular-aperture to triangular-grid-hexagonal-aperture leads to $\approx 45\%$ aperture area reduction with a tradeoff of ≈ 2.57 dBi (640–990 MHz range) gain reduction. The aperture area reduction, however, comes at the cost of limited beam steerability to $\pm 45°$ from boresight, opposed to the $\pm 60°$ achieved from square-grid-rectangular-aperture arrays.

Moving forward, an interesting future work would be to explain the underlying physics behind the BW enhancement in the proposed microstrip ESA designs, using full-wave analysis of the structure via Sommerfeld Integrals [14]. This investigation is expected to reveal why at 2/3rd distance along the patch diagonal is the best match obtained, resulting in such a dramatic improvement in BW (from $\sim 10\%$ in conventional designs to $> 50\%$ in the proposed design). Another avenue is to investigate if the BW of the microstrip patch antennas can be reconfigured or further improved by implementing non-foster networks and/or non-linear circuit elements.

3.18.8 Outputs

3.18.8.1 Journal Publications

[1] B. Barman, D. Chatterjee, and A. N. Caruso, “Investigation on a Class of Wideband, Electrically Small, Microstrip Patch Antenna Elements for Phased Array Applications,” *IEEE Trans. Antennas Propag.* (In Preparation)

[2] B. Barman, K. C. Durbhakula, D. Chatterjee, and A. N. Caruso, “Comparison of Machine Learning Algorithms for Bandwidth Enhancement of a coaxial probe-fed Microstrip Patch Antenna,” *Applied Computational Electromagnetics Society*. (Under Review)

3.18.8.2 Conference Publications/Presentations

[1] B. Barman, D. Chatterjee, and A. N. Caruso, “On the Optimum Substrate Selection in a Wideband Microstrip Patch Antenna Design,” *2022 IEEE International Symposium on Antennas & Propagation & USNC-URSI Radio Science Meeting*, Denver, Colorado, USA, 2022, pp. 383-384. [doi]

[2] B. Barman, D. Chatterjee, and A. N. Caruso, “Time Domain Analysis of an UWB Electrically Small Microstrip Patch Antenna,” *2022 IEEE International Symposium on Antennas & Propagation & USNC-URSI Radio Science Meeting*, Denver, Colorado, USA, 2022, pp. 940-941. [doi]

[3] B. Barman, D. Chatterjee, A. Caruso, and K. Durbhakula, “Tradespace Analysis of a Phased Array of Microstrip Patch Electrically Small Antennas (ESAs),” *Directed Energy Professional Society, Directed Energy Systems Symposium,* Washington DC, 25-29 Oct. 2021. (Poster presentation)

[4] B. Barman, D. Chatterjee, and A. N. Caruso, “Probe-location Optimization in a Wideband Microstrip Patch Antenna using Genetic Algorithm, Particle Swarm and Nelder-Mead Optimization Methods,” *2021 International Applied Computational Electromagnetics Society Symposium (ACES)*, 2021, pp. 1-3. [doi]

[5] B. Barman, K. C. Durbhakula, B. Bissen, D. Chatterjee and A. N. Caruso, “Performance Optimization of a Microstrip Patch Antenna using Characteristic Mode and D/Q Analysis,” *2020 XXXIIIrd General Assembly and Scientific Symposium of the International Union of Radio Science*, Rome, Italy, 2020, pp. 1-4. [doi]

[6] B. Barman, D. Chatterjee, and A. N. Caruso, "Performance Optimization of Electrically Small Microstrip Patch Antennas on Finite Ground Planes," *2020 IEEE International Symposium on Antennas and Propagation and North American Radio Science Meeting*, Montreal, QC, Canada, 2020, pp. 1-2. [doi]

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[9] B. Barman, D. Chatterjee, and A. N. Caruso, “Analytical Models for L-Probe fed Microstrip Antennas,” *2019 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*, Atlanta, GA, USA, 2019. (One Page Abstract).

3.18.9 References

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3.19 Tradespace Analysis of Ultra-Wide-Band (UWB) Antenna Elements

(Kalyan Durbhakula; Originally published in the August 2022 MSR)

3.19.1 Executive Summary

In this tradespace analysis, we have assembled, compared, and analyzed multiple ultra-wide-band (UWB) single-element antennas using the information available in the literature to downselect at least 5 UWB antenna elements. A detailed comparison has revealed five specific UWB antenna elements that could potentially exceed the performance of the state-of-the-art (SOTA) balanced antipodal Vivaldi antenna (BAVA) upon careful study and optimization. The five antenna elements are then compared against the SOTA BAVA for reflection coefficient (S_{11}) bandwidth (≤10 dB), peak gain at the center frequency, directionality, full-width half-maximum, ringing, electronic beam steerability, high-power handling capability, and aperture efficiency. The comparison led to further downselection of antenna elements to: the Koshelev antenna, the Shark antenna, and the Fractal antenna. The Koshelev antenna packs multiple resonances over a wide frequency range in a smaller volumetric size, enabling UWB characteristics. The Shark antenna (a variant of the Bicone antenna) offers directionality without sacrificing bandwidth or gain. The Fractal antenna has a broader scope for shape optimization and bandwidth enhancement in a smaller aperture area. Future efforts will demonstrate improvements with respect to three downselected antenna elements using parametric sweep and/or metrics-based optimization.

3.19.2 Objective

Primary Problem: Determine the extent to which the physical aperture size of an antenna array, composed of patch elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with the present art high power microwave capable antenna arrays.

Solution Space: Through a survey, three new antenna elements (Fractal, Shark, and Koshelev) were identified. The downselected antenna elements can be further analyzed using tradespace study (via parametric sweep) to compare and demonstrate improvements in metrics such as bandwidth, antenna gain, and transient gain while maintaining the smallest aperture area possible.

State-of-the-Art (SOTA)/Deficiency in SOTA: The balanced antipodal Vivaldi antenna (BAVA) is the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power. The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

3.19.3 Technical Background

We expand on the methodology and technical reasoning employed towards the downselection of specific UWB antenna elements (or single elements) [1-21]. The tradespace analysis began with a thorough literature search on the existing wide range of antenna elements that possess the key UWB performance metrics. In this effort, a list of key metrics has been put together that helps with comparing downselected antenna elements and therefore make important design decisions for further tradespace studies.

Figure 1 shows a total of 29 different antenna and size, weight and power (SWaP) metrics (or research parameters) that are available for comparing selected UWB antenna elements. Some of these metrics (scattering parameters, radiated electric field, bandwidth, realized gain, etc.) are readily available directly from measurement/simulation, while others (fidelity factor, impulse response, energy density, envelope, etc.) require post-processing. It is practically difficult to compare antenna elements for all these metrics; therefore, we have downselected to the most important ones. The downselected metrics are frequency-dependent dimensions (size expressed in terms of wavelength at the center frequency), bandwidth (in hertz), peak gain (dBi), directionality (Omni vs directional) in both planes (E-plane & H-plane), ringing, electronic beam steering, aperture efficiency, and effective radiated power. In the time-domain response of antennas, other metrics such as transient gain (rE/V), and radiated electric field are also deemed to be important and were considered for some comparisons.

Research Parameter/Metric Context Description:

1. Physical aperture area
2. Effective aperture area
3. Aperture efficiency
4. Center frequency
5. Bandwidth
6. Realized gain
7. Directionality
8. E-plane, H-plane patterns
9. Half-power beamwidth
10. Side lobe levels
11. Electronic Beam Steering
12. Mutual coupling
13. Peak/Avg. power
14. Pulse shape (Mono./Diff./Bipolar)
15. Radiated E-field
16. Waveform dispersion
17. rE/V
18. Pulse width
19. Rise time
20. Fidelity factor
21. Envelope
22. Pulse repetition frequency
21. Impulse response/Transfer function
22. Full width half maximum (FWHM)
23. Effective radiated power (ERP)
24. Polarization
25. Energy density
26. Energy pattern
27. Ringing
28. Breakdown voltage
29. Profile, Cost, Manufacture difficulty

Figure 1. A list of different antenna metrics (single element and array) under a time-domain excitation.

The design requirements have been defined to assist with the design optimization.

- Wide frequency band (500 MHz or more) or cover the short pulse frequency spectrum.
- Withstand input waveforms with high peak-to-peak input voltages (>10 MW) and high pulse repetition frequencies (10’s to 100’s of kHz).
- Possess directionality in the E-plane and the H-plane.

Based on the taxonomies defined above, a select list of single-element antennas has been identified for UWB HPM applications. The list consists of:

1. Shark antenna (high aperture efficiency)
2. TEM horn (Flare, Exponential, K) and double ridge guide horn
3. Log-periodic dipole (dispersive, low power handling capability)
4. Spiral antenna (small aperture area, circular polarization)
5. Helical antenna (difficult to steer and circular polarization)
6. Full and half Impulse radiating antenna, lens IRA
7. Centered and offset reflectors
8. Fractal antennas (good fidelity factor)
9. Bowtie antenna (omnidirectional in H-plane)
10. Monocone antenna (omnidirectional in H-plane)
11. Koshelev antenna (withstand > 460 kV peak to peak)
12. Leaky-wave antenna (high directivity, difficult to steer)
13. Valentine antenna

The pros (green text) and cons (red text) provided an initial understanding of radiating properties. The antennas with pros have been downselected and compared against the SOTA BAVA using the downselected key performance metrics. Table 1 presents a comprehensive comparison of the downselected antenna elements and the BAVA. The comparison is drawn from the designs reported in the literature. Although they do not exceed the performance of the BAVA, the downselected antennas have not yet been rigorously optimized for our metrics of interest (bandwidth, low ringing/fidelity, aperture efficiency, etc.). The comparison presents how each of the downselected antenna elements perform when compared against the SOTA BAVA and identifies metrics requiring improvement through design optimization and tradespace study. Out of five initially identified antenna elements, the spiral antenna and the leaky-wave antenna were removed from contention. The spiral antenna is omni-directional, whereas the leaky-wave antenna has limited scope for bandwidth enhancement and possesses minimum (<30° steerability). The Koshelev, Shark, and Fractal antennas have been selected as the final candidates for shape optimization and tradespace study. Figure 2 shows computer-aided design (or fabricated) models of the three downselected antennas.

Table 1. Antenna Element Survey for Reduced Aperture Area UWB Arrays.

Antenna element type	Dimensions (single element)	Bandwidth	Peak gain (dBi)	Directionality		FWHM	Ringing	Aperture efficiency
				E-plane	H-plane			
BAVA (SOTA)	-	>25:1	8	Dir.	Dir.	Low (≈135 ps)	Low (≈150 ps)	>90%
Spiral antenna	D=λ/π	10:1	7.5	Dir.	Dir.	Around 200 ps	Around 250 ps	40% to 50%
Shark antenna	λ/3.52 × λ/3.36 × λ/1.91	10:1	7–8	Dir.	Dir.	Lower than vivaldi	Unknown	Unknown
Koshelev antenna	-	6:1	6–8	Dir.	Dir.	Unknown	Unknown	85% (energy efficiency)
Fractal antenna	-	4:1	4–6	Dir.	Dir./Omni	Assuming low (100 to 200 ps) due to good fidelity factor reported in literature	Assuming low due to good fidelity factor	>90%
Leak wave antenna	0.83λ (length, 1D)	≈2:1 or less	7–8	Dir.	Dir.	Higher than Vivaldi	Higher than Vivaldi	50% to 60%

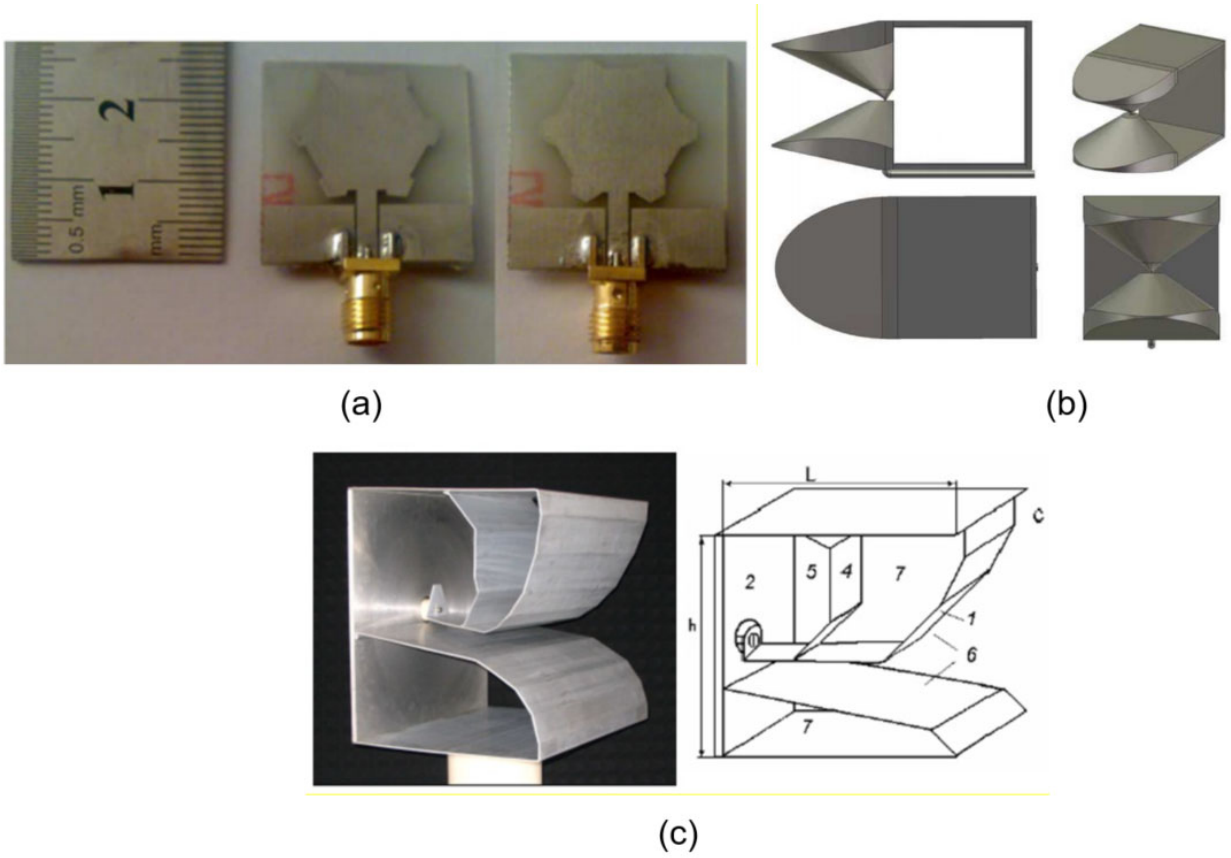


Figure 2. (a) Fractal antenna (b) Shark antenna and (c) Koshelev antenna.

3.19.4 Summary and Recommendations

The tradespace analysis revealed three new UWB antenna elements that meet the OSPRES grant objective in terms of power handling and compactness while meeting the desired bandwidth (>500 MHz) and high transient gain (>1). The three elements will need to be further studied and optimized for a one-to-one comparison against the SOTA.

The Koshelev, Shark, and Fractal antennas offer the potential for bandwidth enhancement in a smaller aperture area than the SOTA leading to high aperture efficiency. Some challenges remain in the field of manufacturability such as obtaining smooth hexagon edges in the Fractal antenna (for better high-frequency performance) and fabricating tapered coax (50 ohms to 150 ohms) in the Shark antenna.

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3.20 Tradespace Analysis of Ultra-Wide-Band (UWB) Koshelev Antenna

(Alex Dowell and Kalyan Durbhakula)

3.20.1 Executive Summary

Ultrawideband (UWB) antennas are an ideal choice for transmitting high-power and fast rise-time (on the order of 100s of picoseconds) microwave signals. While several classes of UWB antennas exist for non-dispersive radiation, the Koshelev antenna has shown particular success, especially with handling gigawatt input power. However, some fundamental limitations remain. To address these, we have performed a tradespace study on the Koshelev antenna and array topologies to enhance bandwidth, transient gain, antenna gain, and aperture efficiency. Simulation results showed that the proposed Koshelev antenna performed better than the state-of-the-art (SOTA) balanced antipodal Vivaldi antenna (BAVA) in terms of transient gain and aperture area, although it did not show an advantage in terms of steerability. In the case of an array, the high-transient gain from the Koshelev antenna relative to the BAVA suggests that it would be an ideal choice for a ground-based HPM system. A prototype of the Koshelev antenna with partial dielectric transformer was measured for gain and demonstrated convergence with the simulated gain data from 0.35 to 1.8 GHz. The 3-D printed antenna prototype fabricated by the UMKC team is functioning as expected and demonstrates our ability to design, optimize, and prototype an ultrawideband antenna that can yield fundamental improvements impactful to the mission.

3.20.2 Objective

Determine the extent to which the physical aperture area of a Koshelev antenna array, composed of Koshelev antenna elements, can be reduced, while maintaining or improving the performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

3.20.3 Technical Background

3.20.3.1 Motivation

The Koshelev antenna was invented by Victor I. Koshelev in 1997, and it has been heavily investigated by Russian scientists for its ultrawideband properties, simple design, and high transient fields. The Koshelev antenna (otherwise known as the combined antenna) can retain the RF source waveform properties (high fidelity) in receive mode and supports high peak input powers (>1 GW) [1]. The Koshelev antenna has gained traction in the high-power microwave weapons community for its past success [2-5]. This led us to downselect the Koshelev antenna as one of the radiators under investigation to try and improve on the state-of-the-art (SOTA).

3.20.3.2 Background

The idea of the Koshelev antenna surged from the unsatisfactory testing of a 2D unbalanced combined (electric monopole + magnetic dipole) antenna prototype, which

had pattern failure at the upper bounds of their frequency range. The 2D unbalanced combined antennas are then replaced by 3D TEM horn-based unbalanced combined antenna named after its creator V. I. Koshelev. In short, the Koshelev antenna is a combination of a transverse electromagnetic (TEM) horn with an exponential profile, an electric monopole, and two magnetic dipoles [4]. The combination of all yields an UWB response with an excellent impedance bandwidth, transient gain, and radiation pattern.

3.20.3.3 Application Space

The Koshelev antenna finds application in high-power microwave weapons, electronic warfare, radar systems, and anywhere an ultrawideband response is needed. The Koshelev antenna is ideal for applications that require high directionality, ultrawideband properties, minimal dispersiveness, minimum group delay, and high-power handling capability.

3.20.3.4 Overview of SOTA

The Koshelev and the balanced antipodal Vivaldi antennas (BAVA) are considered as the SOTA for this effort. The Koshelev antenna designs reported in [1-7] were taken as the baseline in this effort to try and improve some of its metrics such as reflection coefficient bandwidth, antenna peak gain at the center frequency, transient gain (rE/V), half-power beamwidth, and beam steerability in the case of an array. On the other hand, the BAVA is considered the best out of the pool for its high-transient gain, UWB response, and ability to handle high input powers.

3.20.3.5 Deficiencies in SOTA

The Koshelev antenna designs reported in [1-7] were almost identical, with the emphasis only on improving power handling capability. The reported designs had a maximum antenna bandwidth ratio of 3:1, which does not beat the BAVA bandwidth ratio (20:1). The primary issue with having a low antenna bandwidth ratio is the inability of SOTA Koshelev antenna to radiate fast rise-time signals (coming out of RF sources) successfully into free space. The inability to radiate such signals would result in decreased effects on the target. In addition, the SOTA Koshelev antenna and the SOTA BAVA element have a transient gain of 0.7 and 1, respectively. It is ideal to have high transient gain values (>1.5) from a single element to see desired effects. Other deficiencies include low aperture efficiency, low peak gain at the center frequency, and difficulty in manufacturing.

3.20.3.6 Technical Overview of Solution Space

The solution space includes improving the SOTA Koshelev antenna for a higher antenna bandwidth ratio, high transient gain (>1.5), high peak gain at the center frequency, high aperture efficiency, and ease of manufacturing. The SOTA Koshelev antenna from [1-7] was utilized as the initial design and was parametrized to perform tradespace studies. The Koshelev antenna has a unique design that can generate an UWB response by effectively merging radiation characteristics from a transverse electromagnetic (TEM) horn antenna with exponentially tapered flares, an electric monopole, and magnetic

dipoles over a wide frequency range [1]. This opens an opportunity to investigate the design parameter space and understand parameter effects on impedance bandwidth, radiation pattern, electric field distribution, and other metrics via a tradespace study.

3.20.4 Tasks, Milestones, and Status

(A) Perform a preliminary parameter study to identify design parameters that considerably reduce the physical aperture area of the Koshelev antenna element. Perform tradespace studies on design parameters such as feed position (*F*), length (*L*), and alpha (α). Obtain various antenna metrics data, compare, and analyze / JAN21–MAR21 / Complete.

- Milestone: Reduce the physical aperture size of the Koshelev antenna to at least 95% of its original design and show minimal to no variation in the bandwidth, gain and increased aperture efficiency.

(B) Reduce Koshelev antenna aperture size (H×W) to equal to or less than 90 mm × 90 mm, equal to that of the SOTA BAVA, for direct antenna metrics comparison / MAR21–APR21 / Complete.

- Milestone: The optimized design parameters must yield 900 MHz ± 200 MHz bandwidth, rE/V greater than 1, peak gain around 3 dBi at 900 MHz, and aperture efficiency equal to or greater than 130% at 900 MHz.

(C) Using the optimized model from (B), build various array simulation models/topologies to perform a tradespace study and report tradeoffs between array antenna metrics such as center element reflection coefficient (S_{11}) value, gain vs theta at constant phi, physical aperture area, aperture efficiency, and rE/V / MAY21–JULY21 / Complete.

- Milestone: Develop/showcase an optimized Koshelev array model that exceeds an aperture efficiency of 130% with a high rE/V.

(D) Study response from optimized Koshelev antenna array when excited with different monopolar, differential, and bipolar pulse signals of interest. Investigate and analyze the response from the optimized Koshelev antenna array when excited by different excitation patterns / AUG 21–DEC 21 / Complete.

- Milestone: Provide a table comparing the Koshelev antenna array response metrics and narrow down the suitable pulse signals. Recommend (if any) changes to the downselected pulse signal(s) that can further improve the radiation efficiency and/or transient gain.

(E) Design an impedance transformer to transition the signal from a coax cable to the input of the Koshelev antenna element / JULY21–AUG21 / Complete.

- Milestone: Recommend the optimum impedance taper design (with minimum reflections and maximum power transfer) with the optimum dimensions to successfully

convert the high-voltage, short-rise-time input signal from a coax cable to the feed of the Koshelev antenna array.

(F) Prototype a single element Koshelev antenna using 3-D printed parts, metalize, assemble and test for reflection coefficient, gain as a function of frequency, and radiated electric field at 1-m, 2.5-m, 5-m and 10-m (if feasible) distances. / JAN22–SEP22 / Partially Complete.

- Milestone: Experimentally demonstrate a 3D-printed Koshelev antenna with a performance comparable to the standard sheet metal variant of the Koshelev antenna. Report performance of 3D printed Koshelev antenna, compare against the performance of balanced antipodal Vivaldi antenna (BAVA), and recommend any overall improvements to the fabrication/prototyping/testing methods.

3.20.5 Methods and Approach

In this project, computational electromagnetic solvers were used to simulate and analyze the UWB Koshelev antenna and to perform tradespace studies. The computational EM solvers are available in commercial EM software such as Altair FEKO, CST Studio Suite, Ansys HFSS, COMSOL Multiphysics, etc. In this project, we have utilized CST Studio Suite for its advanced frequency domain and time-domain solvers. In comparison to other software, the CST Studio Suite uses accelerating frequency sweep techniques to achieve solution convergence at the same time. The frequency domain solver was used to obtain scattering parameters, antenna gain at various frequencies, and antenna radiation efficiency. The time-domain solver was primarily used to obtain time-harmonic electromagnetic fields as a function of time. This solver is useful and highly recommended to visualize the 1-D, 2-D, and 3-D electric fields.

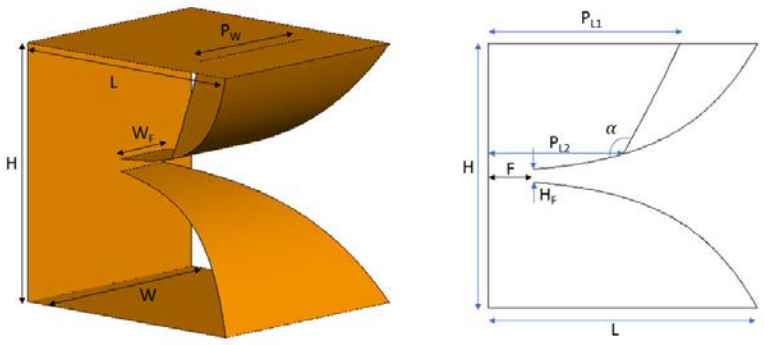
The above solvers were used to simulate and analyze the single element and different array topologies. Multiple RF metrics were calculated, compared, analyzed, and improved upon using the two solvers.

The antenna prototype was fabricated using fused deposited modeling (FDM) 3-D printed polymer method. The FDM builds parts layer by layer by selectively depositing melted material in a predetermined path.

3.20.6 Results and Discussion

3.20.6.1 Initial Design

We began the work by modeling the baseline Koshelev antenna design provided in [5] using CST Studio Suite. The initial design of the Koshelev antenna, which is shown in Figure 1 yielded a promising impedance bandwidth response (shown in Figure 2(a)) with a bandwidth ratio of at least 10:1. A higher bandwidth ratio can be obtained with a further increase in the simulated frequency range. Figure 2(b) shows the peak gain profile as a function of frequency at boresight.



(a) (b)

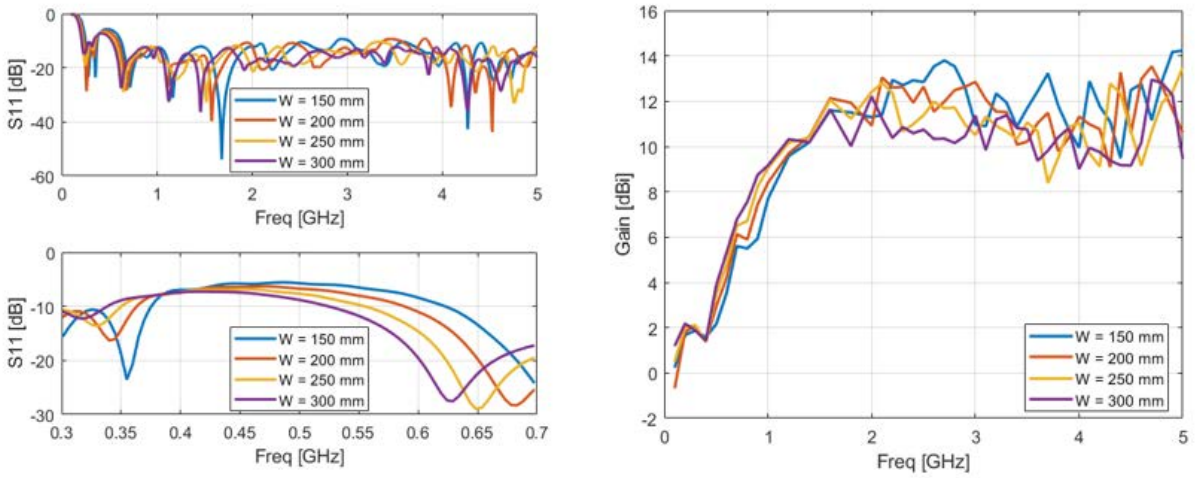
Figure 1. Koshelev antenna with design parameters: H = 293 mm, W = 268 mm, L = 300 mm, W_F = 70 mm, P_W = 169 mm, F = 50 mm, H_F = 14.3 mm, P_{L1} = 150 mm, P_{L2} = 213 mm, and α = 26.86°. (a) 3D view, and (b) side view.

The width of the Koshelev antenna has been varied over a pre-selected range and the corresponding reflection coefficient (S_{11}) and gain as a function of frequency are shown in Figure 2. Figure 2(a) shows the full frequency range and a zoomed-in (0.3 GHz to 0.7 GHz) frequency range to notice the shift in S_{11} as the width value increases. In Figure 2(a), as the width decreases from 300 mm (purple curve) to 150 mm (blue curve), the –10 dB lower frequency shifts from 0.5 GHz to 0.7 GHz. In Figure 2(b), the gain at lower frequencies did not differ a lot when compared against each other, however, at high frequencies, some difference can be noticed.

Overall, the gain curve did not vary drastically when the physical aperture area was reduced by 50% meeting the milestone#A.

3.20.6.2 Tradespace Study of Single Element

A tradespace study has been performed on the length (*L*), feed position (*F*), and angle alpha (*α*) design parameters of the Koshelev antenna. Once an understanding of the length (*L*) design parameter of the Koshelev antenna was established, we performed a tradespace study on angle alpha (*α*) and feed position (*F*).



(a) (b)

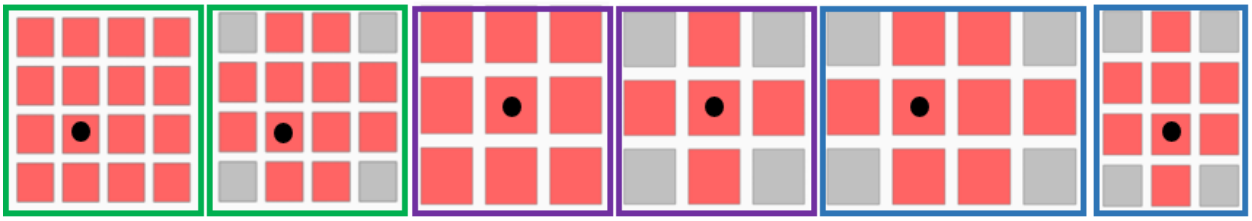
Figure 2. (a) Reflection coefficient (S_{11}) in dB and (b) gain in dBi for four different widths.

An onset of $\alpha = 90°$ implies that the center adjusting plate is perpendicular to the top exponential profile, an $\alpha < 90°$ implies the center adjusting plate is leaning toward the reflector side of the antenna, and an $\alpha > 90°$ implies the center adjusting plate is leaning toward the aperture side of the antenna. It is helpful to choose an alpha (α) value greater than 90°, i.e., the center adjusting plate leaning towards the aperture side. A larger α value (>120°) is recommended to avoid unnecessary reflections from the electric monopole. A feed position too close to the back reflector could excite unintended or perturb intended currents on the back reflector. A feed position (F) between 5 and 20 mm ($F = 1/20 < L < 1/10$) can be chosen to achieve an optimum bandwidth.

Based on the observations from the initial tradespace study of the Koshelev antenna, the antenna aperture size and other design parameters have been adjusted to come close to the required aperture size (90 × 90 mm^2). We have been able to meet our target metrics, which are provided in milestone#B and can be found in detail in Table 5.2.2 in [12].

3.20.6.3 Tradespace Study of Array

We have carried out an effort to develop simulation models of various array topologies and execute the models for their array antenna metrics. Figure 3 shows various array topologies considered for this study. The black dot represents the centermost element of that topology which could have the worst-case S11 value due to maximum mutual coupling.



(a) (b) (c) (d) (e) (f)

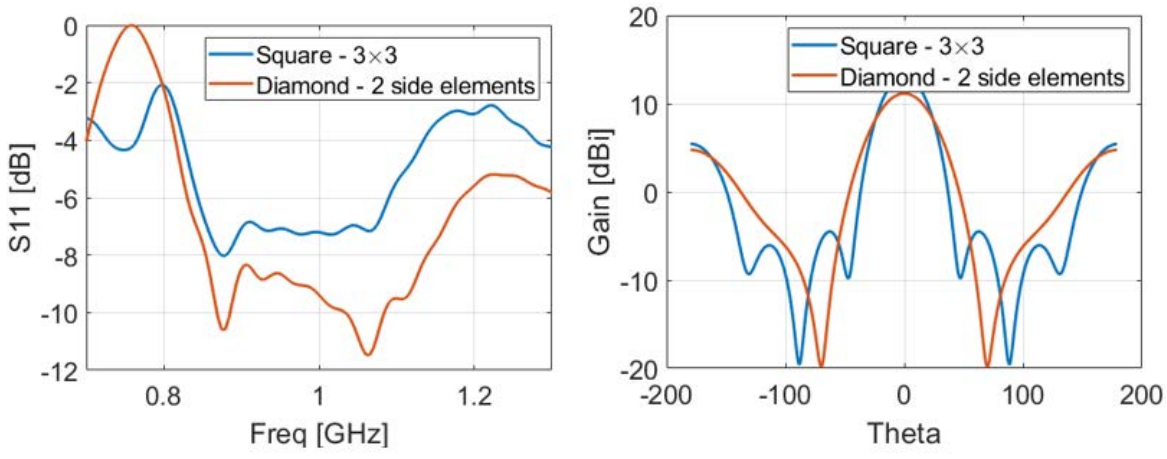
Figure 3. Array topologies under study. (a) Square – 4×4, (b) Octagon – 2 side elements, (c) Square – 3×3, (d) Diamond – 2 side elements, (e) Hexagon – 2 side elements (4×3), and (f) Ellipse – 3×4.

Table 1. Area of Koshelev array topologies with $S_x = S_y$ = 50 mm.

Array shape	Size of an array	Area
Square	4×4	0.2844 m^2
Octagon	2 side elements	0.2554 m^2
Square	3×3	0.1504 m^2
Diamond	2 side elements	0.074 m^2
Hexagon	2 side elements	0.1374 m^2
Ellipse	3×4	0.1598 m^2

Figure 4(a) compares the S_{11} value of the center element of a square (3×3) and a diamond array. From Figure 4(a), it is evident that a diamond array has a better S_{11} value over the desired bandwidth than the square topology. A slight decrease in peak gain is expected due to the reduced number of elements in the case of the diamond array, however, an improvement in the side lobes can be noticed. The gain comparison is shown in Figure 4(b).

Preliminary analysis tells us that smaller inter-element spacings only affect higher frequencies and would not necessarily deteriorate performance at low frequencies. If this result holds, it would be wise to use smaller spacings for optimum realized gain even though it may result in a decreased gain.



(a) (b)

Figure 4. (a) Center element S_{11} value and (b) gain as a function of theta angle comparison between the 3×3 square Koshelev array and 2 side diamond Koshelev array.

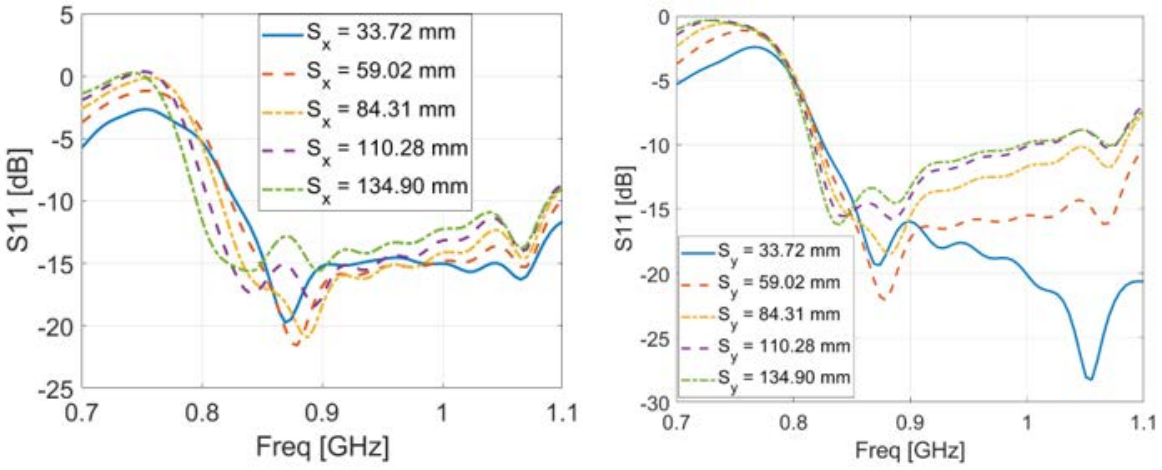
In contrast, a poor S_{11} value with excellent gain will always result in an unsatisfactory realized gain which can be seen with inter-element spacing equal to 170 mm.

The element spacing in the time domain is determined by the pulse duration, which is given by the following equation:

$$S_x = S_y = K\tau_p c_0 \tag{1}$$

where S_x & S_y are the interelement spacing variables in the x-axis and y-axis. In (1), K is a numeric constant, τ_p is the pulse duration, and c_0 is the speed of light in m/s. For the first study, we kept the value of K_y= 0.464 and varied $K_x$from 0.25to 1 ns. For the second study, we kept the value of K_x= 0.464 and varied K_y from 0.25 to 1 ns. An optimum K_x & K_y value have been identified. The criterion for optimum output is set when the S_{11} value stays below the –10 dB line over as wide a bandwidth as possible centered around 900 MHz. In conjunction with the S_{11} value, the gain pattern with minimum side lobe can also be considered as the optimum variable. In Figure 5, the S_{11} value of the centermost element of the diamond Koshelev array has been plotted for the two studies mentioned above. Figure 5(a) shows the S_{11} value for constant S_y and variable S_x, while Figure 5(b) shows the S_{11} value for constant S_x and variable S_y.

In Figure 5(a), the bandwidth calculated at a center frequency of 900 MHz shifted left as the value of S_x increased. The shift is significant at the lower frequency end of the spectrum than at the higher frequency end of the spectrum. Therefore, an intermediate value between 84.31 and 110.26 mm can be chosen as the optimum value of S_x. On the other hand, Figure 5(b) showed a significant change in the S_{11} value as the value of S_y was varied while keeping S_x constant.



(a) (b)

Figure 5. (a) S_{11} value of center element of diamond Koshelev array over the desired frequency range for different S_x values with a constant S_y (= 62.59 mm) value, and (b) S_{11} value of center element (#3) of diamond Koshelev array over the desired frequency range for different S_y values with a constant S_x (= 62.59 mm) value.

It is evident that the maximum bandwidth in Figure 5(b) is obtained by the smallest S_y value. An optimum S_y value of 84.31 mm can be chosen. In conclusion, the diamond-shaped Koshelev antenna array was determined as the optimal array shape reducing the aperture area by 25% and a rE/V > 5 while only losing gain by 1.5 dBi at the center frequency partially satisfying metrics provided in milestone#C.

3.20.6.4 Array Excitation Pattern Study

In another effort, we have tested the optimized antenna array with seven excitation patterns to understand the array behavior under these excitations. The uniform and Gaussian excitation patterns yielded a maximum peak gain of 11 dBi at boresight (θ = 0°). However, the Gaussian and uniform excitation patterns also yielded the maximum side lobe level. Alternatively, the Taylor, Binomial, and Chebyshev excitation patterns yielded gain values close to 10 dBi at boresight. Moreover, these 3 excitation patterns yielded minimum side lobe levels without reduction in HPBW. The cosine and cosine-square excitation patterns yielded a low peak gain value of 5 dBi at boresight with higher side lobe levels than other excitation patterns. Table 2 shows the electric field, transient gain, and energy density comparison between the excitation patterns. Overall, the Gaussian and uniform excitations were identified as the optimal excitation patterns to achieve maximum energy density and rE/V satisfying the milestone#D.

Table 2. Optimized Koshelev antenna array E-field response metrics at 10 m under different excitation patterns.

Excitation Pattern	Epeak [V/m]	rE/V	Ed [uJ/m2]
Uniform	1309.3	2.42	0.83
Cosine	326.27	0.6	0.05
Cosine-square	326.27	0.6	0.05
Taylor	743.46	1.37	0.26
Binomial	817.77	1.51	0.32
Chebyshev	849.92	1.57	0.34
Gaussian	1133.72	2.05	0.59

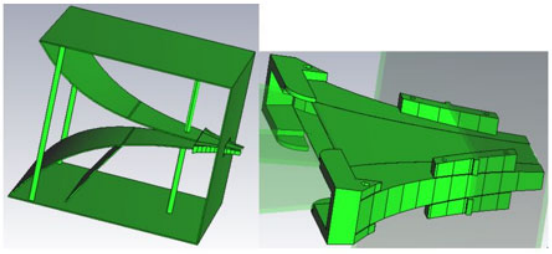
3.20.6.5 Prototyping and Measurement

One of the advantages with the proposed Koshelev antenna is its ability to achieve UWB response without increasing aperture area. The UWB response in simulations can be achieved by using a balanced feed. In reality, the balanced feed can be made possible by desgining an impedance transformer. In theory, an impedance transformer that has a relative permittivity that matches the free space permittivity at the transformer-antenna interface and has a tapered dielectric that linearly increases the permittivity until it reaches the N-type feed would minimize losses due to reflections.

$$vol\ \% = \frac{\varepsilon_{reff}-1}{\varepsilon_{ro}-1} \quad (1)$$

where v is the volume percentage, ε_{ref} is the permittivity of the material at that volume percentage, and ε_{ro} is the solid body permittivity of the material. The transformer was designed using the permittivity of an ultraviolet (UV) curable resin to see if a stereolithography (SLA) printer would be able to print the transformer. After several iterations of the impedance transformer design, we determined that the partial dielectric impedance transformer would interface well with the Koshelev antenna by minimizing reflections and field nonuniformity. More details on the optimization of impedance transformer can be found in [13-16].

After reviewing S_{11} and boresight gain results from 0.1–5 GHz, it was determined that the partial dielectric impedance transformer integrated with a Koshelev antenna meets the desired performance requirements and should be prototyped. Before fabrication could begin, a structural support case study was conducted to identify where adequate structural support could be added to the partial dielectric impedance transformer integrated with a Koshelev antenna CAD model with minimal RF performance degradation. The Koshelev antenna with the support structure and the partial dielectric transformer was prototyped, assembled, and tested. Figure 6(a) shows the finalized CAD model and Figure 6(b) shows the 3-D printed and metalized prototype.



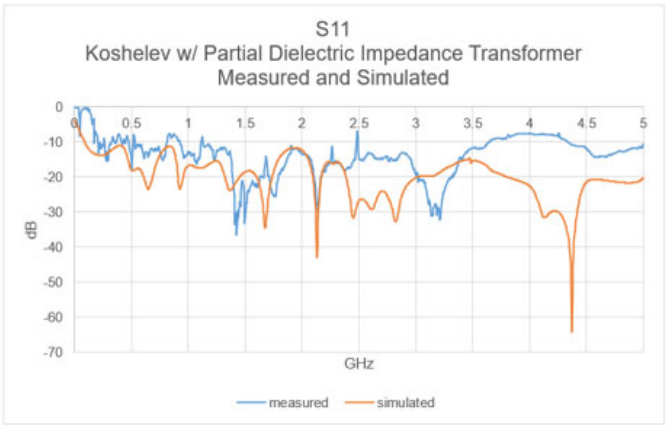
(a)



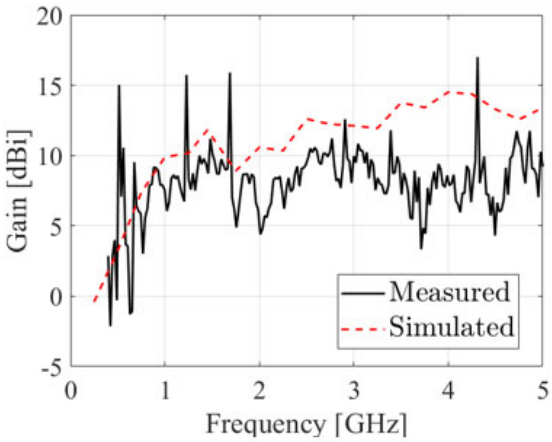
(b)

Figure 6. CAD models of (a) a partial dielectric impedance transformer integrated with a Koshelev antenna and antenna structural support (b) a partial dielectric impedance transformer with front and rear structural support.

The 2.5 mm thick frame of the Koshelev Antenna, a partial dielectric impedance transformer, and structural support were 3-D printed out of PLA. The copper foil was applied to all surfaces, except for part of the transformer and the structural support, using adhesive tape. The last step in the fabrication process was to solder on an N-type connector horizontally to the top and bottom traces, shown in Figure 6(b).



(a)



(b)

Figure 7. Comparing S_{11} of a simulated Koshelev antenna integrated with a PLA partial dielectric impedance transformer.

After fabrication, the prototype of the Koshelev antenna integrated with a PLA partial dielectric impedance transformer with structural support was tested and compared to the simulated S_{11} results, shown in Figure 7(a). The simulated and measured results Figure show a good agreement over the entire frequency range from 0.3–5 GHz. Some losses can be noticed from the measured result (between 3.5 and 4.5 GHz) because of the fabrication imperfections that could arise in the 3-D printing, assembly, and in the metallization stages of the prototype. The gain comparison is shown in Figure 7(b).

Table 3. An EM simulation comparison of metrics of interest between the Koshelev antenna and SOTA BAVA.

	Single Element		4x4 Array	
	BAVA	Koshelev Antenna	BAVA	Koshelev Antenna
Aperture size – (cm^2)	**12 × 12**	**9.1 × 10**	**63.7 x 63.7**	**55 × 58**
Physical Aperture area (m^2)	**0.0144**	**0.0091**	**0.4058**	**0.3190**
Operating frequency range - fc±BW (MHz)	**900 ± 200**	**900 ± 180**	**950 ± 50**	**900 ± 100**
Peak gain at 900 MHz (dBi)	**3.7**	**4.5**	**14.7**	**15**
Transient Gain - rE/V	**0.4**	**1.2**	**6.5**	**9.67**
Half-Power Beamwidth(°)	**115**	**83**	**26.2**	**30**
Aperture Percentage at 900 MHz (%)	**143**	**243**	**63**	**87**

In addition, we have drawn a comparison between the Koshelev antenna and the SOTA BAVA using some of the important antenna metrics obtained via simulations. Table 3 demonstrates this comparison between the two antennas for the single element and the 4x4 array topology meeting most of the goals (except beam steering) described in milestone#F.

3.20.7 Summary and Recommendations

(B) An initial validation of the Koshelev antenna was performed using CST Studio Suite. The initial simulated results agreed with the antenna metrics published in the open literature [1]. An UWB bandwidth response (10:1 bandwidth ratio) and a rE/V > 1 have been obtained from our initial simulations validating the design and our approach.

(E) The tradespace study of feed position provided a deeper understanding of how its position impacts the S_{11} value bandwidth. An optimum value for feed positions i.e., $F = 1/20 < L < 1/10$ is recommended to achieve maximum bandwidth. The tradespace study of the antenna length (L) is straightforward. A longer antenna length will radiate

better at lower frequencies. However, physical size restrictions/requirements must be kept in mind in determining the antenna length. Finally, a larger α value (>120°) is recommended to avoid unnecessary reflections from the electric monopole.

(F) From a thorough tradespace study, the aperture size of the Koshelev antenna (single element) is determined to be 90 mm x 100 mm to achieve desired antenna metrics performance proposed in the milestone. All metrics described in the milestone have been successfully achieved via simulations except the desired bandwidth (200 MHz on both sides) at 900 MHz center frequency. The bandwidth achieved via simulations is 900 ± 100 MHz.

(G) We were able to determine that the diamond topology is the optimum shape. The interelement spacing study revealed that S_y has the least effect on the output; therefore, a smaller spacing value can be chosen to reduce the physical aperture area of the Koshelev array.

(K) We have studied seven different excitation patterns to identify the optimal excitation pattern that yields maximum energy density and rE/V. The study determined that the uniform and Gaussian excitation patterns as the optimum excitation patterns. Choosing either the uniform or Gaussian excitation pattern would yield maximum electric field at the boresight for an arbitrary input signal.

(L) A partial dielectric impedance transformer Koshelev antenna prototype was fabricated, assembled, and measured for continuous wave response. The reflection coefficient and the measured gain values from the Cu-foil plated prototype agreed with the simulated values at least up to 2 GHz yielding an impedance bandwidth of 1.7 GHz with a measured gain of 8 dBi at 900 MHz. Using simulations, we demonstrated that the proposed Koshelev antenna (as a single element and as an array) performs exceedingly well in comparison to the SOTA BAVA with few exceptions as listed in Table 3.

3.20.8 Outputs

1. OSPRES Grant Review Meeting Spring 2021

2. OSPRES Grant Review Meeting Fall 2021

3. DEPS 2022 Presentation

4. OSPRES/PTERA Review Meeting Fall 2022

5. A. Dowell, and K. Durbhakula, “An UWB and High Gain Combined Antenna for HPM Applications,” *in International Symposium on Antennas and Propagation*, Portland, Oregon, USA, July 2023 (in preparation).

6. A. Dowell, and K. Durbhakula, “Novel Combined Antenna Design with Partial Dielectric Impedance Transformer for HPM and EW Applications,” *IEEE Transactions on Antennas and Propagation*, July 2023 (in preparation).

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[15] ONR HPM Program – Monthly Status Report – JULY 2021

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3.21 Tradespace Analysis of Ultra-Wide-Band (UWB) Shark Antenna

(S. Brasel, K. Norris, and K. Durbhakula; Originally published in the January 2022 MSR)

3.21.1 Executive Summary

The Shark antenna design had initially offered hope in achieving ultra-wideband (UWB) radiation with high transient gain values due to its unique truncated bi-cone shape. We believed that by carrying out a systematic study, we could uncover something fundamental that could help with enhancing the directional antenna pattern as well as a design that could handle tens of megawatts as input power. The objective was to propose an electrically small Shark antenna that can retain bandwidth as well as improve transient gain value over the state-of-the-art. Our approach has been to perform a systematic study by carefully investigating improvements and degradations on certain metrics at all frequencies of interest and for a given time-domain waveform. We have found two specific Shark antenna design parameters to heavily influence the bandwidth and gain to be the cone height (*h*) and distance to backplane (*d*). The study has yielded insights into the workings of the Shark antenna through parametrized and optimization studies, which have been helpful in the miniaturization of this antenna. However, the improvements (in terms of transient gain) were not significant enough. For this reason and to shift more of our efforts to the more promising Koshelev antenna, we have made a decision to sunset this study.

3.21.2 Objective

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced, while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: An array of Shark antenna elements with an emphasis on inter-element and intra-element spacing effects is a good candidate for UWB HPM systems which maintain a reduced aperture area with respect to the current state-of-the-art. In the literature, the Shark antenna has already been shown to achieve a wide 20:1 impedance bandwidth, low dispersion, and a sectoral (also referred to as directional) radiation pattern.

Sub-Problem: The design parameter space of the Shark antenna has not been studied rigorously in the literature and therefore the effect of these parameters on the antenna metrics is not understood. In addition, the Shark antenna has been shown to be not very directive in the H-plane. Preliminary studies have shown that aperture efficiencies at low frequencies are much better than at higher frequencies.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Explore the Shark antenna array tradespace by generating different array topologies/lattices (hexagonal, octagon, square, elliptical) with different intra- and interelement spacing combinations.

Relevance to OSPRES Grant Objective: The Shark antenna dimensions were established to be frequency dependent and can be readily modulated to fit the spectrum characteristics of an ultra-fast rise time input pulse.

3.21.3 Technical Background

The Shark antenna is a form of bi-cone antenna with a reflector connected to the top ends of the bi-cone. In addition, the bi-cones of the Shark antenna are truncated vertically (E-plane) and slightly tilted/inclined to make the antenna directional in the E-plane. Desrumaux et al [1] is the only known group working on the Shark antenna. The authors of [1] claim that the primary purpose in the development of this antenna is to demonstrate miniaturization, improve the front-to-back ratio, and have it be non-dispersive. The authors performed simulation studies on multiple parameters of the Shark antenna. Figure 1 shows the gradual transition of the Shark antenna design starting from a simple bi-cone antenna design.

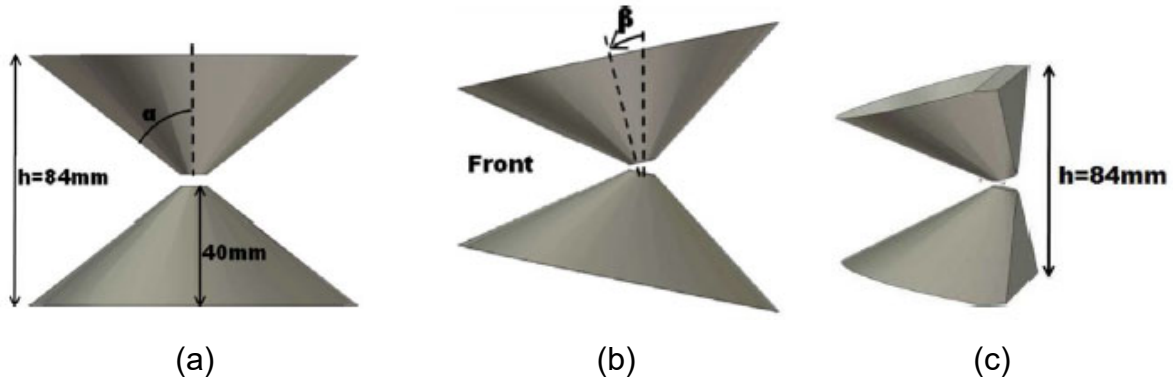
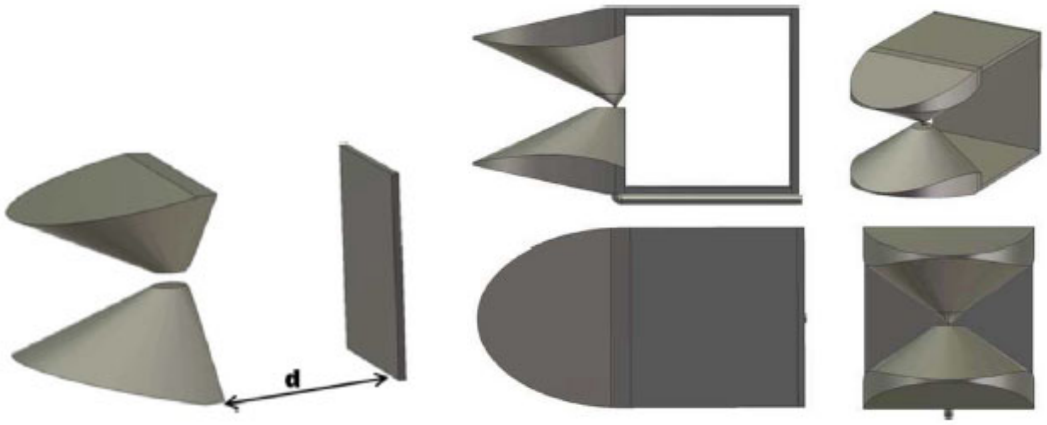


Figure 1. (a) Traditional bi-cone (b) Inclined bi-cone and (c) Truncated bi-cone.

As reported in [1], a big disadvantage with a bi-cone antenna is that its radiation pattern is omnidirectional in the H-plane. To make the antenna directional in one of the planes, the two cones have been inclined at a certain angle (β), which can be seen in Figure 1(b). As seen in Figure 1(c), the cones are truncated to improve the radiation in front of the antenna. To further assist in improving the radiation pattern in front of the antenna, a reflector plate has been added at the back of the antenna, which can be seen in Figure 2(a). A complete design of the Shark antenna can be seen in Figure 2(b).



(a) (b)

Figure 2. (a) Adding a reflector at the back. (b) Complete Shark antenna model.

This completes the design of the Shark antenna. It is reported in [1] that the width, height, and length of the Shark antenna are electrically small at the initial operating frequency/wavelength. This is one of the reasons to consider this antenna for further study by our group. The authors did not report any detailed parameter study in [1] to really understand their effect on the radiation. It was also reported that the Shark antenna array has a good front-to-back ratio, which is useful to have in transient UWB radiation. For these reasons, this antenna was pursued to improve our understanding of another transient UWB antenna as well push the state-of-the-art.

3.21.4 Tasks, Milestones, and Status

(A) Complete initial design, simulation, and validation of the Shark antenna / JAN21 / Complete.

(B) Validate Shark antenna design using the LEWIS supercomputer over a wider range of frequency results (up to 20 GHz) / FEB–MAR21 / Complete.

(C) Identify Shark antenna design parameters which contribute significantly to bandwidth, gain, and physical aperture area. Determine which parameters contribute most to performance improvement/size reduction/ FEB–MAR21 / Complete.

(D) Perform a tradespace study by simulating the Shark antenna with varying cases of flare angle, cone length, and distance to backplane. Gain a general understanding of how these parameters affect impedance bandwidth, rE/V, gain and HPBW / FEB–MAY21 / Complete.

- Milestone: produce a detailed summary of change in impedance bandwidth, rE/V, HPBW in H-plane and E-plane as a function of flare angle (α), cone height (h), and distance to backplane (d) / Complete.
- Milestone: Choose the optimal Shark antenna design that has the lowest operating frequency within size requirements based on tradespace study / Complete.

(E) Using the optimal Shark antenna design in (D), simulate various array geometries including hexagonal, rectangular, and circular arrays. Determine which array geometries are optimal and analyze aperture fields and aperture efficiencies. Further study the effect of different time-domain waveforms in the far-field radiated by the optimized Shark antenna array / MAY–NOV21 / Complete.

- Milestone: Produce a report which states the effects of various array geometries for the Shark antenna. The optimal array geometry chosen should have the least interference between elements, therefore yielding higher impedance bandwidth and higher aperture efficiency. Overall, the optimal Shark array geometry should have at least 20% impedance bandwidth at 900 MHz center frequency for the centermost element with 130% array aperture efficiency, ± 60 degrees beam steering capability, and rE/V equal to or greater than 4. Identify a waveform that combines well with the optimized Shark antenna array in terms of peak electric field, rE/V, and energy density.

(F) Begin prototyping and validation of optimal Shark antenna single element. / JUN–DEC21 / Complete.

- Milestone: Have a finished Shark antenna prototype. Compare S11 and radiation pattern with simulated Shark antenna.

3.21.5 Methods and Approach

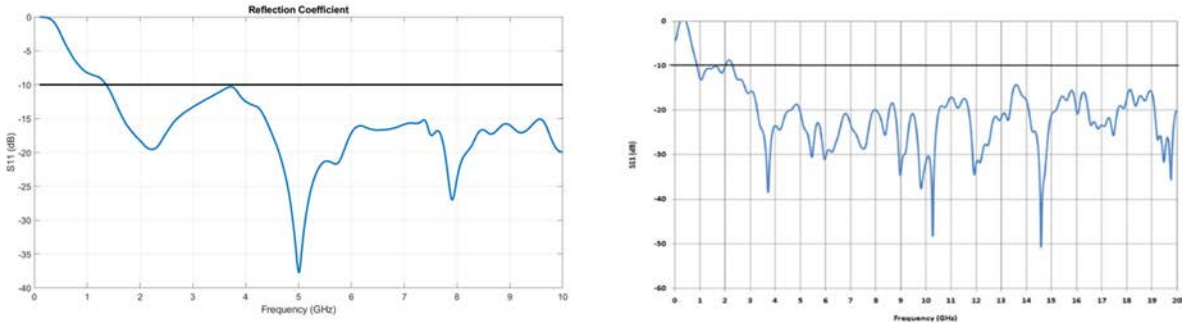
The methodology used in this study is relatively straightforward. The single element Shark antenna design has been initially parametrized to understand each design variable effect on the antenna performance. The parametrization has been carried out using the commercial electromagnetic (EM) wave solver CST microwave studio. Each design variable has been systematically varied and studied to understand its effect on antenna input impedance, antenna bandwidth, antenna pattern, peak gain, half-power beamwidth in E-plane and H-plane, transient gain, time domain electric field, and electric field frequency spectrum. After detailed investigation, an optimum single element Shark antenna of aperture area of 90 mm x 30 mm has been finalized and fabricated. Using simulations, the optimized single element Shark antenna has been converted into various array shapes with different interelement spacing values. A detailed time-domain study by feeding different pulses of interest has been carried out.

3.21.6 Results and Discussion

The study initially started with validating the Shark antenna design reported in [1]. In this section, we present some of the important antenna metrics (reflection coefficient, frequency domain gain, transient gain, E-plane beamwidth, H-plane beamwidth, and aperture efficiency) for both optimized single element Shark antenna and for an optimal array topology. Furthermore, we compared the above metrics for both single element and array designs in a table to be able to clearly see the tradeoffs between different design parameter values and for different array topologies. We have also included time-domain electric field responses especially for different array topologies. The frequency domain

and time-domain studies clearly determined a particular array topology to be the optimum topology.

First, the reflection coefficient (S11) of the shark antenna has been shown to be matched to the reference input impedance (i.e., Z_{input} = 150 Ω) from ~1.5–10 GHz (Figure 3).



(a) **(b)**

Figure 3. Original Shark antenna S11 result (a) from CST simulation (b) from [1].

From Figure 4, we can notice that the Shark antenna cases with a large flare angle (α) value are not well matched to the reference impedance of 150 Ω. The α = 20° and α = 45° cases are matched to the reference impedance over a wide range. From Figure 4, we can notice that smaller α values perform better at low as well as high frequencies.

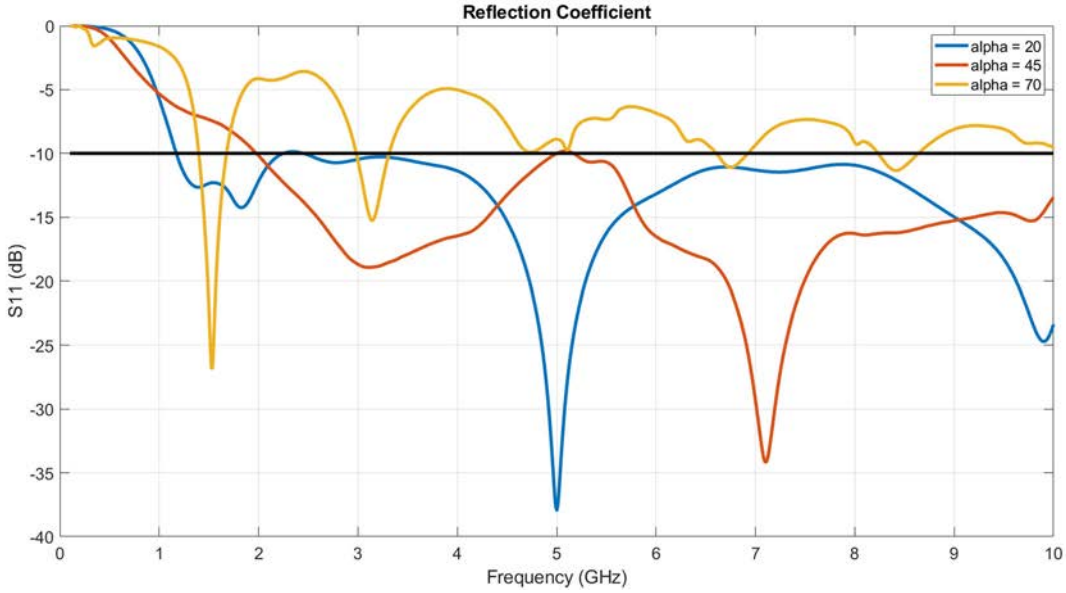
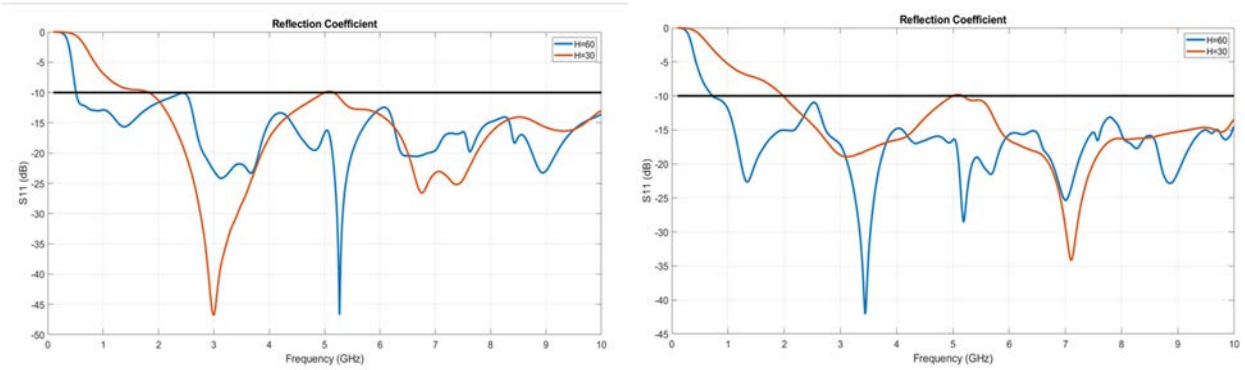


Figure 4. Reflection coefficient for *h* = 30 mm and *d* = 7 mm cases.



(a) (b)

Figure 5. Reflection coefficient: (a) α = 45° d = 45 mm (b) α = 45° d = 75 mm.

From Figure 5. the h = 60 mm case performs better than the h = 30 mm case for both values of d, as the reflection coefficient curve is below the –10dB line for a wider range of frequencies. Our preliminary study indicated that smaller alpha (α) values and larger h values resulted in improved S11 performance.

Table 1. Shark parametric study results.

H	d	Flare Angle	Frequency Dependent Dimensions (W,H,L) $\lambda = \frac{c}{5.5e9}$	Physical Aperture area $A_{phs} = W * H$	Bandwidth	Lowest Cutoff Frequency	Peak gain (5.5 GHz)	Directionality (5.5 GHz)		Aperture Efficiency (%) (5.5 GHz)
								E-plane	H-plane	
30 mm	75 mm	20°	$\frac{\lambda}{2.497}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.59177}$	~0.001354 m^2	>10:1	1.168 GHz	3.534 dBi	48.7°	188.2°	61.79525764
		45°	$\frac{\lambda}{0.909}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.492}$	~0.00372 m^2	>10:1	2 GHz	4.874 dBi	89.1°	97.8°	31.02057555
		70°	$\frac{\lambda}{0.3349}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.337}$	~0.01022 m^2	Poor BW	1.39 GHz	5.573 dBi	49°	200°	12.91056991
60 mm	75 mm	20°	$\frac{\lambda}{1.249}, \frac{\lambda}{0.447}, \frac{\lambda}{0.5}$	~0.00533 m^2	>10:1	0.625 GHz	5.196 dBi	107.4°	69.4°	23.08071189
		45°	$\frac{\lambda}{0.455}, \frac{\lambda}{0.447}, \frac{\lambda}{0.373}$	~0.01464 m^2	>10:1	0.731 GHz	6.813 dBi	30°	54.4°	11.01804594
		70°	$\frac{\lambda}{0.165}, \frac{\lambda}{0.447}, \frac{\lambda}{0.220}$	~0.0402 m^2						
30 mm	45 mm	20°	$\frac{\lambda}{2.497}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.59857}$	~0.001354 m^2	>10:1	1.219 GHz	3.959 dBi	39.8°	125.6°	69.22677561
		45°	$\frac{\lambda}{0.909}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.492}$	~0.00372 m^2	>10:1	1.793 GHz	4.850 dBi	46.3°	228.5°	30.86782754
		70°	$\frac{\lambda}{0.331}, \frac{\lambda}{0.8798}, \frac{\lambda}{0.413}$	~0.01022 m^2	Poor BW	1.453 GHz	5.402 dBi	120.1°	73.9°	12.51442646
60 mm	45 mm	20°	$\frac{\lambda}{1.249}, \frac{\lambda}{0.447}, \frac{\lambda}{0.699}$	~0.00533 m^2	>10:1	0.644 GHz	4.653 dBi	82.8°	73.6°	20.66869754
		45°	$\frac{\lambda}{0.455}, \frac{\lambda}{0.447}, \frac{\lambda}{0.473}$	~0.01464 m^2	>10:1	0.512 GHz	8.425 dBi	37.1°	79.5°	13.62498708
		70°	$\frac{\lambda}{0.165}, \frac{\lambda}{0.447}, \frac{\lambda}{0.249}$	~0.0402 m^2						

Table 1 presents a comparison of physical aperture area, bandwidth, lowest cutoff/operating frequency (–10 dB), peak gain, E-plane beamwidth, H-plane beamwdith, and aperture efficiency at the center frequency. Table 1 shows that the Shark antenna with a larger physical area yields the maximum gain at the center frequency (5.5 GHz) and smallest aperture efficiency value. Therefore, the Shark antenna design with the most optimal aperture efficiency is the case with the smallest overall size, as highlighted in Table 1, and is considered for further studies. Taking the above design as the optimized single element Shark antenna design, we proceeded to investigate various array shapes.

A 3 x 3 Shark antenna array has been simulated. When creating the Shark antenna array, one can choose to connect the reflector plate of the individual elements or not. Both options have been explored as shown in Figure 6.

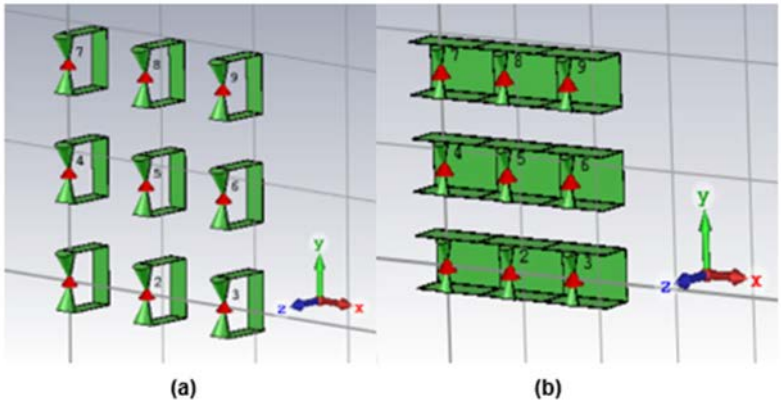


Figure 6. 3 x 3 Shark antenna array: (a) disconnected reflectors (b) connected reflectors.

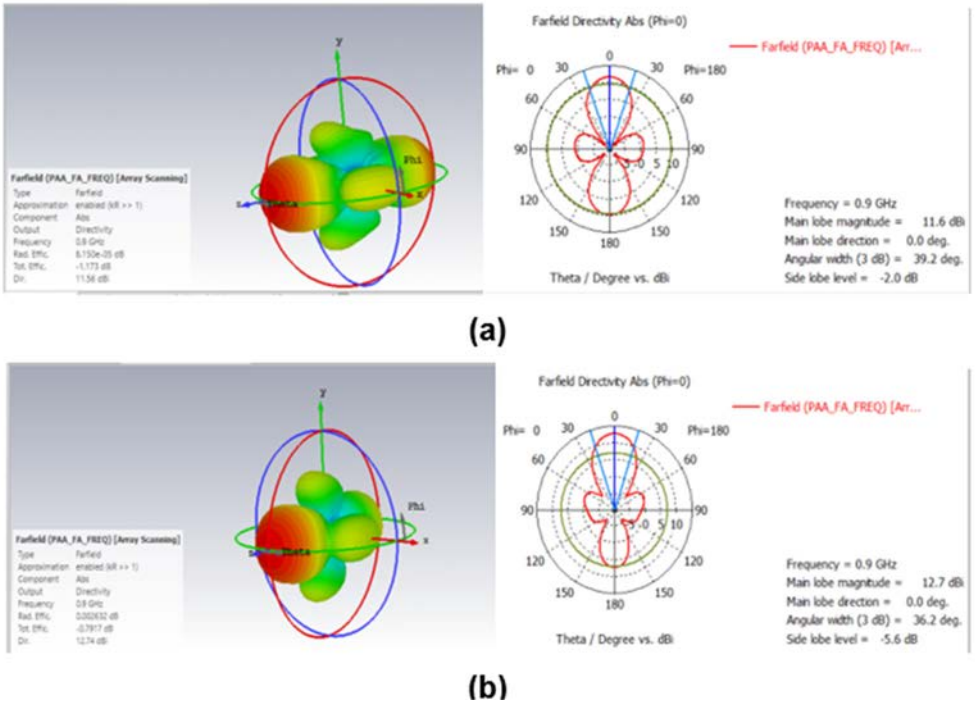


Figure 7. 900 MHz radiation pattern of square arrays for an (a) unconnected reflector (b) connected reflector.

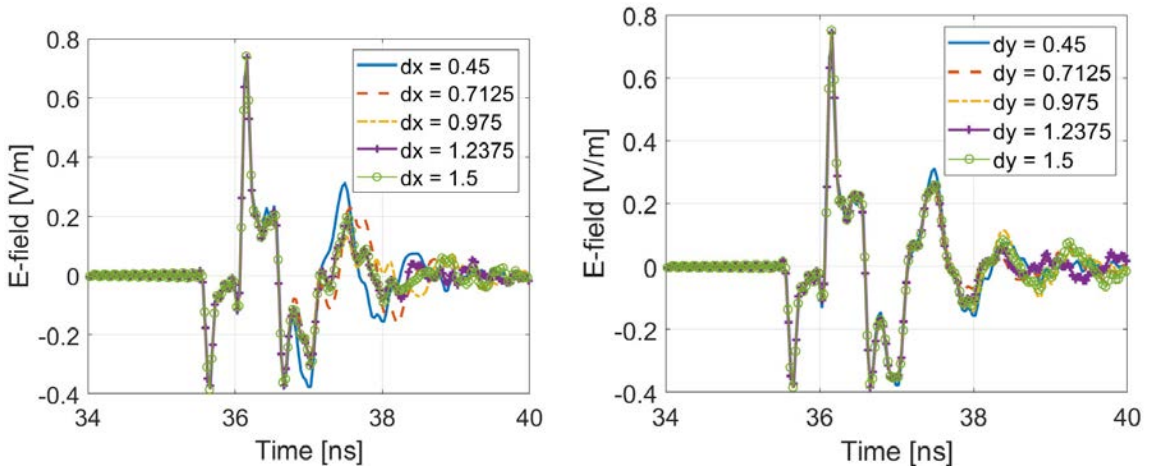
From Figure 7 it is evident that a connected reflector yields higher peak gain at 900 MHz than the unconnected reflectors. Therefore, we have chosen to use connected reflectors for the remainder of the Shark antenna array studies. Later, we compared the square Shark antenna array output response to that of hexagon and ellipse Shark antenna array output responses. The hexagon and ellipse shaped arrays had in total 8 elements. In comparison, the ellipse Shark antenna array turned out to be the optimum for its performance. This comparison has been shown in Table 2.

Table 2. Performance comparison of Shark array geometries.

Geometry	# of Elements	Max Gain (900MHz) (dBi)	Aperture Efficiency (%)	rE/V (1m)	rE/V (2m)	Beamwidth (°)	Sidelobes (dB)
square	9	12.719	53.13	8.91	9.25	36.2	-5.6
hexagon	8	11.728	52.38	7.98	8.21	32.4	-4.5
ellipse	8	12.408	52.3	7.86	8.13	40.4	-5.2

The efforts to fabricate the optimized single element Shark antenna were initiated to validate the simulation results. In parallel, we extended our study and analysis to feeding time-domain pulses of interest to the optimized elliptical Shark antenna array.

A normalized 900 MHz damped rectangular wave has been fed to the array elements to obtain the time domain radiated electric field at 10-meters distance from the aperture of the array antenna (Figure 8). From comparing the frequency spectrum plots in Figure 9(a) and Figure 9(b), a significant difference can be noticed in Figure 9(a), which shows that the radiated electric field is more sensitive to the interelement spacing variable in the x-axis (H-plane) than in the y-axis (E-plane). In Figure 9(a), the 900 MHz peak frequency spectrum has been obtained for the interelement spacing value of d_x = 0.45.



(a) (b)

Figure 8. Simulated electric field at 10-meter distance from the aperture of the elliptical Shark antenna for different (a) interelement spacing values in the x-axis, and (b) interelement spacing values in the y-axis.

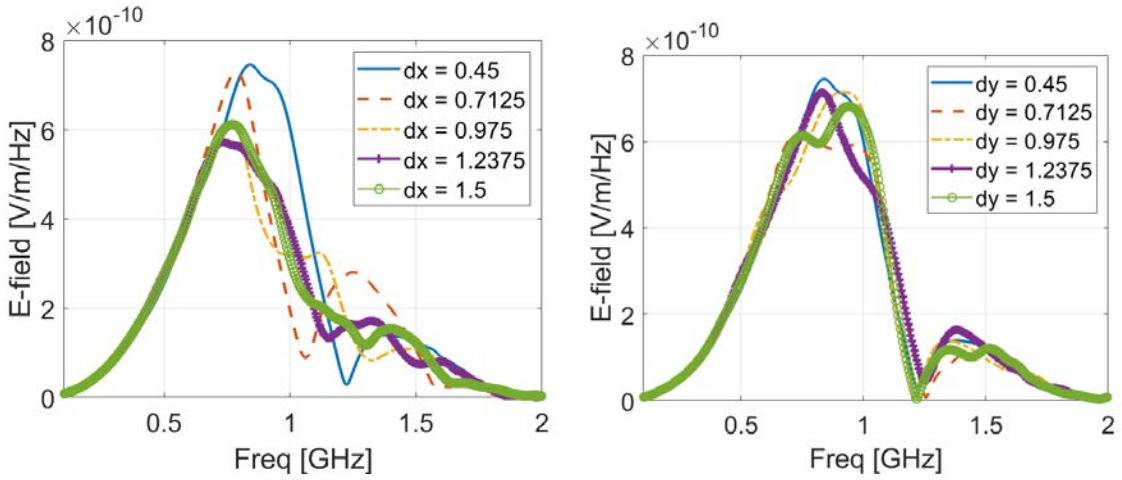


Figure 9. Frequency spectrum of the simulated electric field at 10-meter distance from the aperture of the elliptical Shark antenna for different (a) interelement spacing values in the x-axis, and (b) interelement spacing values in the y-axis.

The optimized single element Shark antenna element was prototyped in August 2021. Figure 10 shows two views of a 3D printed and metallized Shark antenna. The back plate is cut out from an aluminum sheet, whereas the cones were 3D printed and coated using nickel paint.

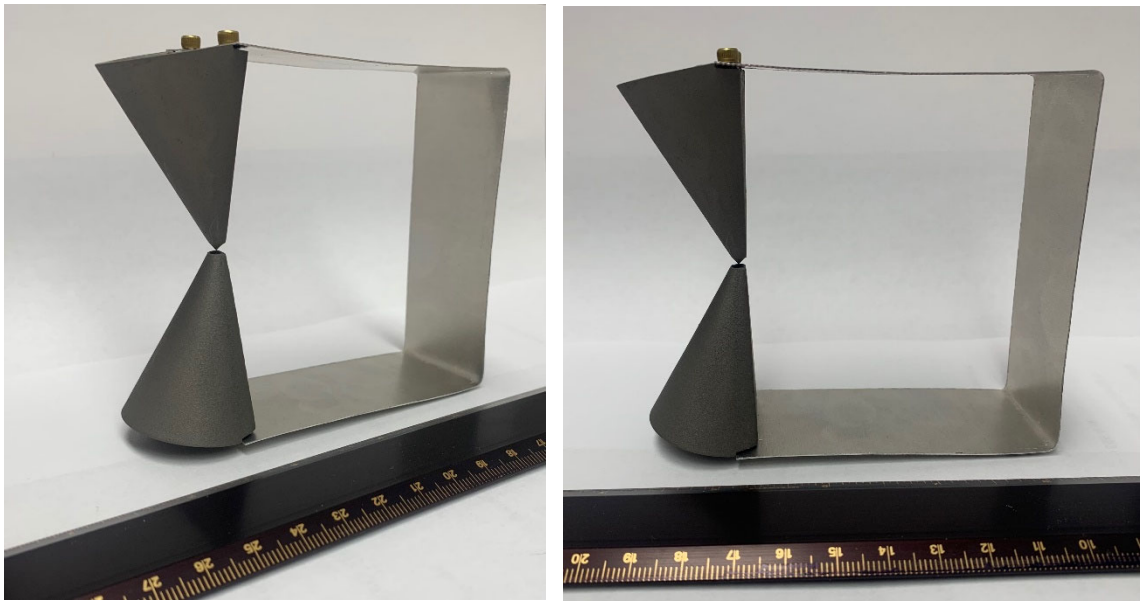


Figure 10. 3D printed and Metallized Single Element Shark antenna.

Later, we tried feeding other pulses of interest to the elliptical Shark antenna array as well as to the other array topologies to draw a comparison of time-domain electric field at 10 m distance. This comparison is shown in Figure 11. It is evident that the square topology has the maximum peak E-field values followed by hexagonal and elliptical topologies.

Similar observations were noted from feeding other pulses. This drew us to a preliminary conclusion that an unconventional Shark antenna array shape may not yield maximum peak E-field. One advantage noticed with unconventional array shapes is the decrease in side lobe level compared to square.

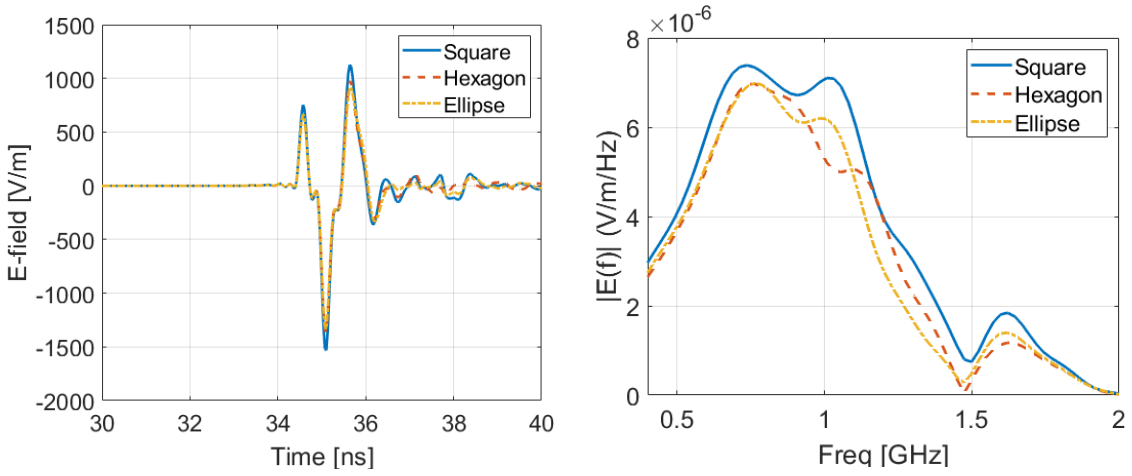


Figure 11. Radiated electric field at 10 m distance from three array topologies when excited by mega-impulse bipolar signal. (a) E-field in time domain and (b) frequency spectrum of E-field.

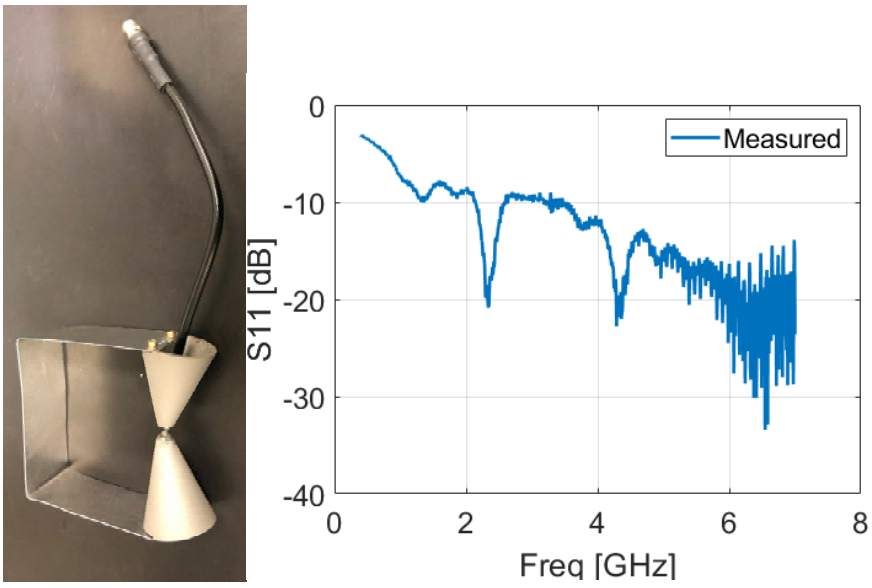
We have also simulated the elliptical Shark antenna array with different pulses and obtained their peak E-field at 10 m, transient gain, and energy density values. Table 3 shows these values for different pulses. The rE/V for an array is not satisfactory. This further led us to believe that this design may not be a right choice.

Table 3. Elliptical Shark antenna array response with different pulse source waveforms at 10 meters distance.

Pulse source	Epeak [kV/m]	rE/V	Ed [uJ/m2]
AT Marx	1.2	2.6	1.26
MI0731	1.3	2.5	2.33
DSRD 2x2	0.3	0.4	0.31
DSRD 4x2	0.78	0.4	2.25
NPG22	0.16	0.08	0.54
PPM2022	1.3	0.6	9.1

The assembled prototype of the optimized single element Shark antenna is shown in Figure 12(a). The S11 result for the 3D printed and metallized single element Shark antenna is shown in Figure 12(b) First the reflections are high before 2 GHz, which is

unacceptable. Although the performance was satisfactory from 2 GHz to 4.5 GHz, the unusual noise at beyond 4.5 GHz might imply that it is difficult to achieve the required feed precision using the tools available at our disposal. This cemented our belief that it perhaps may be worth focusing our efforts on better antennas such as the Koshelev antenna and sunset the Shark antenna effort.



(a) (b)

Figure 12. Measured reflection coefficient of the optimized single element Shark antenna.

3.21.7 Summary and Recommendations

(A-B) The Shark antenna has been designed, simulated, and validated according to [1].

(C) The Shark antenna design parameters that have been found to contribute significantly to bandwidth performance, directivity, and gain are the cone height (*h*) and distance to backplane (*d*).

(D) The Shark antenna tradespace study has been completed and has provided insight into the Shark antenna design space. Increasing the cone height *h* yields better impedance bandwidth at low frequencies and is more directive in the E and H planes. However, increasing *h* results in a larger aperture area. To remain within 90 x 90 mm, the maximum *h* value is 45 mm; with this the lowest operating frequency of 815 MHz is achievable.

(E) The elliptical Shark antenna array topology yielded the optimum array metrics, which can be found in Table 2. The array metrics obtained from the elliptical Shark antenna array are closer to the desired metrics provided in milestone (E). The interelement spacing variable study has provided insight into the workings of a Shark antenna array. The Shark antenna array is more sensitive to the interelement spacing variable in the H-plane than in the E-plane. The elliptical topology has significantly smaller

sidelobe level values and similar frequency-domain gain or transient gain values when compared against square and hexagonal topologies. If the input is a monopolar signal, a hexagonal or an elliptical topology is preferred. If the input is a bipolar signal, an elliptical topology is recommended for its decent transient gain value with significantly smaller sidelobe levels.

Recommendations: Overall, the Shark antenna is ideal for applications that can utilize a miniaturized version and slightly directive antenna version of a bi-cone antenna. The Shark antenna is also ideal for applications that do not require high transient gain values and require wider beamwidth in the H-plane. The two Shark antenna design parameters that stood out during this study to have the maximum effect were the cone height and distance to backplane. Employing a robust stochastic algorithm could further improve the transient gain value. In addition, more detailed study of the array topology is needed to study the interaction between individual Shark antenna elements.

3.21.8 References

[1] L. Desrumaux, A. Godard, M. Lalande, V. Bertrand, J. Andrieu and B. Jecko, "An Original Antenna for Transient High Power UWB Arrays: The Shark Antenna," in IEEE Transactions on Antennas and Propagation, vol. 58, no. 8, pp. 2515- 2522, Aug. 2010, doi: 10.1109/TAP.2010.2050418.

3.22 Tradespace Analysis of Ultra-Wide-Band (UWB) Fractal Antenna

(Sai Indharapu and Kalyan Durbhakula)

3.22.1 Executive Summary

Fractal antennas are low-profile microstrip antennas with ultra-wide-band (UWB) properties and a physical aperture area significantly smaller than the balanced, antipodal Vivaldi antenna (BAVA). The goal was to perform a tradespace study on a fractal antenna that could attain the maximum possible bandwidth without significantly increasing the aperture area over the desired frequency range. A hexagonal patch antenna with individual hexagon-shaped fractal elements was chosen as the antenna element with which to carry out the tradespace study. Out of many relevant design parameters, the hexagon patch radius '*a*' and fractal element radius '*b*' were determined to have the maximum effect on the aperture area and bandwidth. The physical aperture area of the optimized fractal antenna was reduced by 7% over the initial design while maintaining the bandwidth ratio (3.3:1) and peak gain (3.2 dBi) at the center frequency. Furthermore, an octagonal fractal antenna array has the optimum antenna performance metrics with reduced aperture area (0.0632 m^2) and side lobes while retaining the bandwidth and array gain as 15.7 dBi. Compared to the state-of-the-art balanced antipodal Vivaldi antenna, the proposed fractal antenna element demonstrated a 3% reduction in aperture area while retaining similar antenna gain (2.58 dBi at 900MHz) and aperture efficiency (i.e., 208%) values. Whereas, the octagonal-shaped fractal antenna array has produced a 30.47% higher bandwidth with a 0.25% smaller aperture area than SOTA BAVA. The obtained aperture area reduction is highly beneficial when the element design is converted into an array. We determined that the conventional tradespace study using full-wave solvers is computationally expensive, particularly with such a vast parameter space to cover, which triggered us to shift our focus to machine-learning-based optimization to cut down the simulation time.

3.22.2 Objective

Primary Problem: Determine the extent to which the physical aperture area of an antenna array, composed of antenna elements, can be reduced while maintaining performance in peak power density, bandwidth, and electronic beam steerability over the UHF range (0.4–1 GHz), compared with present-art high-power-microwave-capable antenna arrays.

Solution Space: Fractal antennas possess exceptional fidelity factor values (>0.9), which describe how well the shape of the input pulse is retained at an observation point in the far-field. Their high degree of freedom provides an opportunity to develop systematically modified patch shapes, which in turn leads to improved bandwidth while retaining high fidelity factor values.

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is considered to be the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

Deficiency in the SOTA: The BAVA design parameter space has been exhausted over the past couple of decades. The physical aperture area still remains very large and there is no viable path through tradespace study for further physical aperture area reduction.

Solution Proposed: Design, simulate, validate, and perform a tradespace study on the design parameter space of the selected fractal antenna element using commercially available electromagnetic (EM) wave solvers.

Relevance to OSPRES Grant Objective: The fractal antenna achieves an ultra-wideband (UWB) response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against a SOTA BAVA, dual ridge horn antennas etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

3.22.3 Results and Discussion

The fractal antenna produces UWB characteristics with an omnidirectional radiation pattern. Fractal antennas are known for their space filling ability and a very long electrical length [1]. Such techniques allow for the design of miniaturized wideband antennas with radiation patterns and input impedance characteristics approaching those of electrically large antennas. Adding fractal elements to the corner of the antenna will achieve multiple closely spaced resonating frequencies. Closely spaced resonant frequencies will help with bandwidth enhancement. In addition, fractal antennas are low-cost, low profile, and easy to fabricate.

From the initial literature search on various fractal antennas, a hexagon patch design with hexagon fractals was selected for further investigation. The fixed fractal antenna was designed using commercially available EM solvers (FEKO, CST), illustrated in Figure 1 The structure of the studied fractal antenna has a hexagon patch, hexagon fractal elements at the edge of the patch, transmission line feed, two rectangular plates, and a ground plane, effectively forming a coplanar waveguide fed patch antenna.

An initial parametric analysis of a simple hexagonal patch antenna with and without fractals has been carried out. The hexagon patch antenna with hexagon fractals shows better bandwidth over the simple hexagon patch antenna [Figure 1.(a)]. In addition, results in Figure 2(a) follow the multiple resonance trend as shown in Figure 2 (b), which shows a change in the upper frequency of the bandwidth. The difference between simulated results and results from [1] could be due to the missing information of the ground plane type and its dimensions in [1].

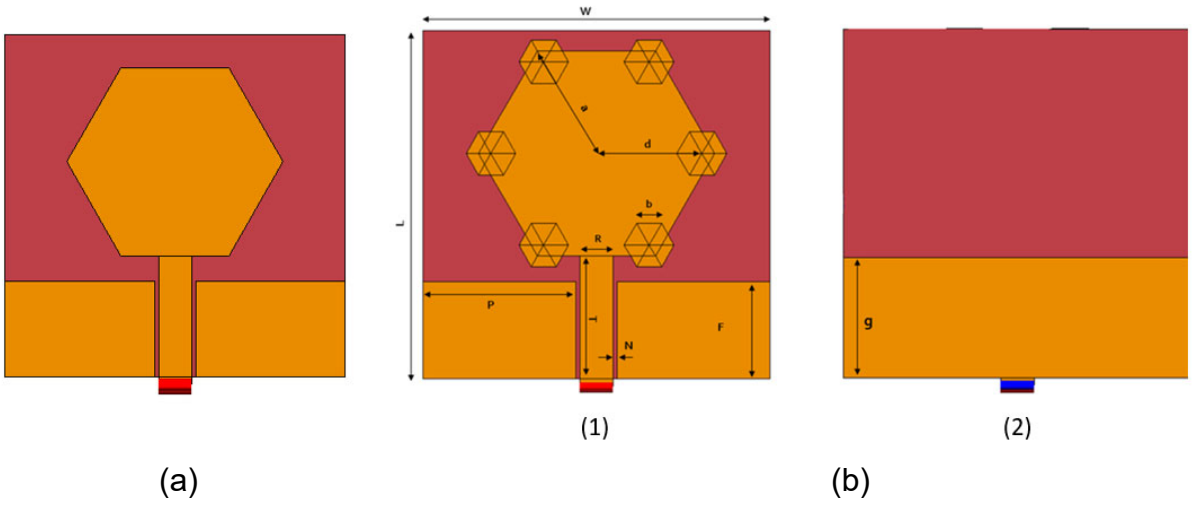


Figure 1. (a). Geometry of hexagon patch antenna **(b)**. Geometry of hexagon patch antenna with hexagon fractals: (1) top view (2) bottom view. *L* = 25 mm, *W* = 25 mm, *T* = 8.85 mm, *N* = 0.3 mm, *P* = 11 mm, *F* = 7 mm, *R* = 2.4 mm, *a* = 8.5 mm, *d* = 7.6 mm.

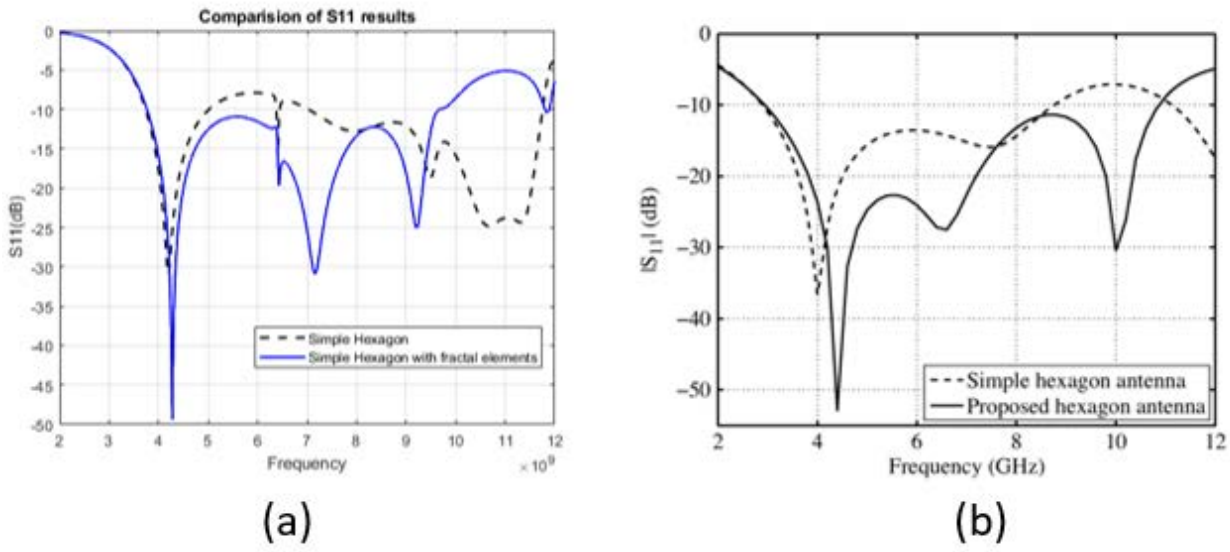


Figure 2. (a) Comparison of S_{11} results of simple hexagon with fractals and without fractals for *g* = 7.8 mm & *b* = 1.8 mm (b) S_{11} results from [1].

After validating the hexagonal patch antenna with and without fractals, each of the other design variables were studied to understand and improve the S_{11} bandwidth.

3.22.3.1 Parametric study of design variable, "ground length (g)"

The length of the ground plane has been shown to significantly impact the reflection coefficient, as can be observed in Figure 3. This observation was not reported in [1]. It is observed that an increase in ground plane length up to the length of the transmission line

improves the return loss curve to below –10 dB, which increases bandwidth. Also, an improvement in impedance characteristic is observed for higher *g* values. A sudden dip in between 7–9 GHz frequencies might be due to a calculation error of the EM solver. However, a further increase in ground plane length negatively impacts the reflection coefficient. We conclude that the further increment in ground plane length will cause disturbance to the intended radiation pattern of the hexagonal patch, thereby causing a decrease in the reflection coefficient.

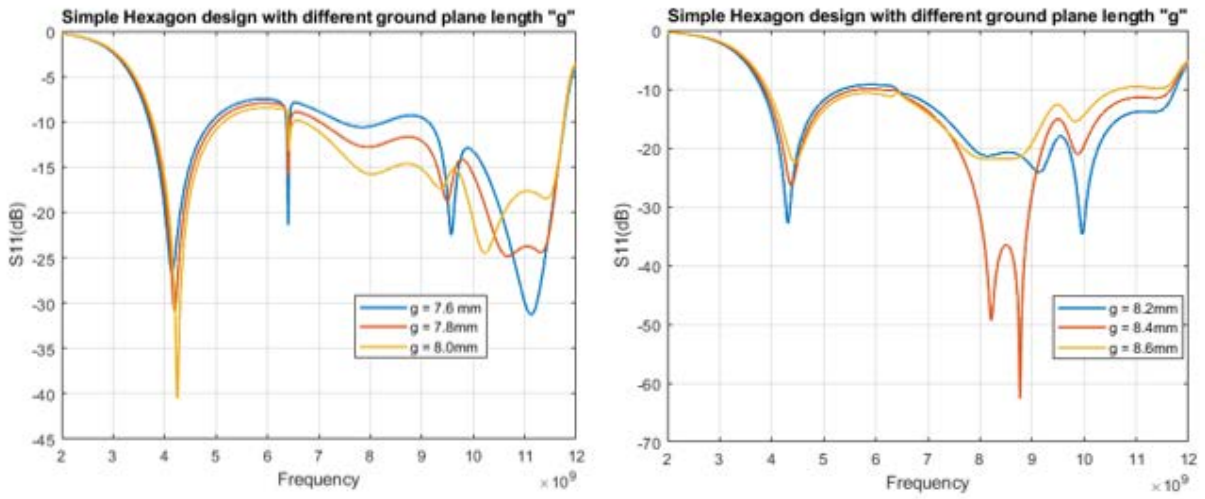


Figure 3. S_{11} for simple hexagon geometry with different ground plane lengths.

3.22.3.2 Parametric study of design variable, "fractal radius (b)"

From our preliminary study of a hexagon patch antenna, the increase in bandwidth is caused due to an increase in closely spaced resonant frequencies, which can be observed in Figure 4. A hexagon patch antenna with a hexagon fractal element radius equal to 1.8 mm yields multiple resonant frequencies with enhanced bandwidth. The higher the fractal radius *b* the narrower the bandwidth and vice-versa. However, it is important to not make *b* too small, which leads to a dual or tri-band resonance, much narrower in bandwidth than the desired UWB behavior.

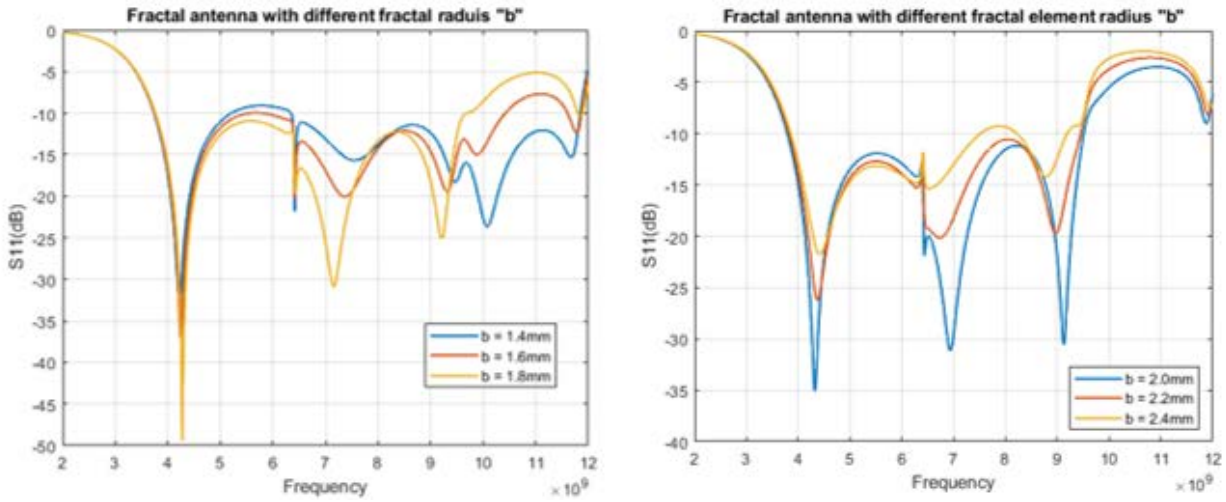


Figure 4. S_{11} results for fractal antenna with different fractal element radius.

With the help of build-in optimization algorithms in FEKO and an initial value of *b* (i.e., 1.8 mm) obtained from the parametric study, OPTFEKO has been employed to optimize the fractal radius *b* and further increase the bandwidth. The optimization was performed over 51 discrete frequency points from 2 GHz to 12 GHz. Figure 5 illustrates the improvement in bandwidth at the optimum *b* value, i.e., 1.66 mm.

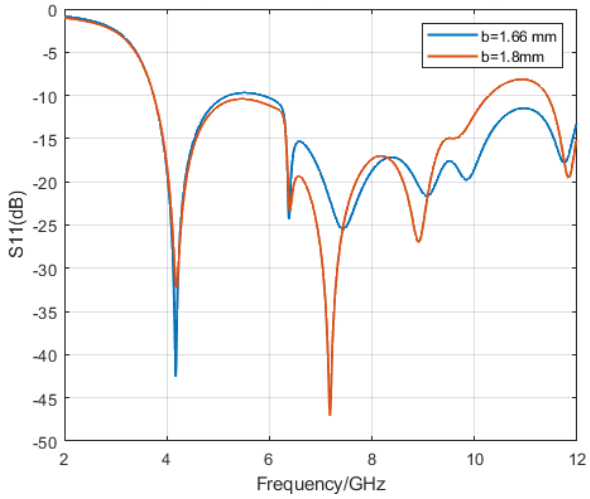


Figure 5 S_{11} results for fractal antenna with different “b” values.

Table 1. Comparison of fractal antenna metrics obtained from parametric study, optimization algorithm.

Antenna Element Type		**Fractal Antenna (*b* = 1.8 mm)**	**Optimized Fractal Antenna (*b* = 1.66 mm)**
Substrate Dimensions (mm)		25 × 25 × 1	25 × 25 × 1
Radiating Patch Dimensions (mm)		18.8 × 18.8	19.5 × 19.5
Physical Aperture Area (mm^2)		0.353	0.381
Bandwidth		2.5:1 f_L = 3.8 GHz, f_U = 9.5 GHz	3:01 f_L = 4 GHz, f_U = 12 GHz
Peak Gain (dBi) (f_C)		3.5 (7 GHz)	3.42 (7.8 GHz)
Directionality	E-plane (f_C)	69° (7 GHz)	64.8° (7.8 GHz)
	H-plane (f_C)	71° (7 GHz)	57.0° (7.8 GHz)
Aperture Efficiency (f_C)		50% (7 GHz)	40% (7.8 GHz)

3.22.3.3 Parametric study of design variable, "hexagon radius (a)"

To further investigate the effect of antenna design variables, the hexagonal patch radius *a* was studied with the help of an optimization algorithm. To decrease physical aperture area and to increase aperture efficiency, OPTFEKO has been employed to find the new optimum value for hexagon radius *a*. The antenna metrics S_{11} and gain are shown in Figure 6. The optimized value of *a* (8 mm) decreases the physical aperture area by 7% and increases the aperture efficiency by 29%. Other antenna metrics are shown in the third column of Table 2.

Table 2. Comparison of fractal antenna metrics obtained from parametric study, optimization algorithm.

Antenna Element Type		**Original Fractal Antenna (*a* = 8.5 mm, *b* = 1.8 mm, *N* = 6 & *fc* = 6.65 GHz)**	**Optimized Fractal Antenna (*a* = 9 mm, *b* = 1.66 mm, *N* = 14 & *fc* = 7.8 GHz)**	**Optimized fractal Antenna (*a* = 8 mm, *b* = 1.66 mm, *N* = 6 & *fc* = 7.8 GHz)**
Substrate Dimensions (mm)		25 × 25 × 1	25 × 25 × 1	25 × 25 × 1
Radiating Patch Dimensions (mm)		18.8 × 16.2	18.5× 16.4	18.5 x 16
Physical Aperture Area (mm^2)		0.3	0.3	0.2
Bandwidth		2.5:1 f_L = 3.8 GHz, f_U = 9.5 GHz	3:1 f_L = 4 GHz, f_U = 12 GHz	2.6:1 f_L = 3.8 GHz, f_U = 9.5 GHz
Peak Gain (dBi) at f_C		3.5	3.9	3.2
Half-Power Beamwidth (HPBW)	E-plane (f_C)	69°	63.4°	71°
	H-plane (f_C)	71°	57.5°	80.4°
Aperture Efficiency (f_C)		120%	92%	115%
rE/V		0.6	0.6	0.7

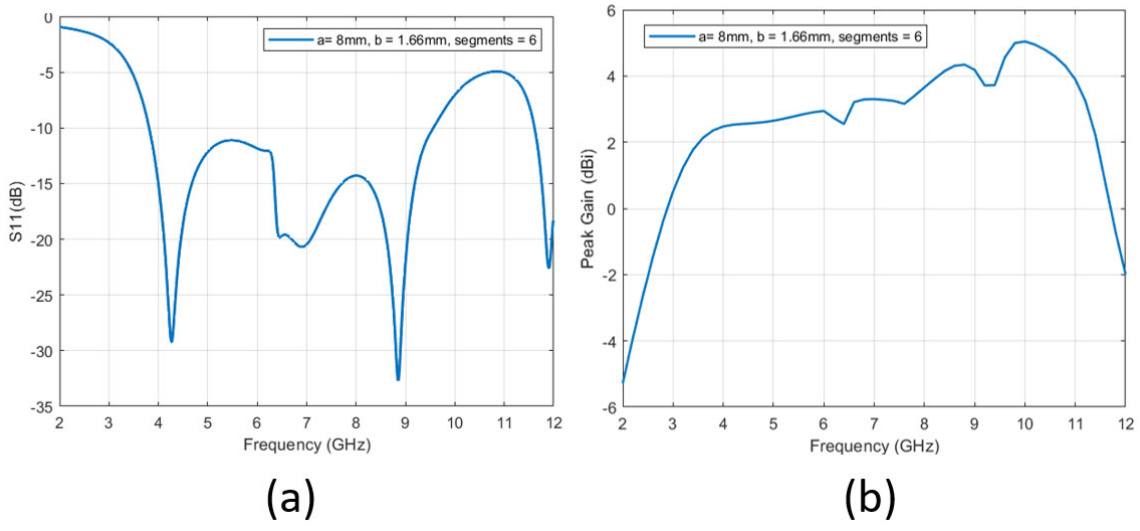


Figure 6. (a) S_{11} for antenna geometry with *a* equals 8 mm, and (b) gain vs. frequency.

3.22.3.4 Frequency scaling the current fractal antenna design

The initial antenna design has been modified to achieve a center frequency of ~1.3 GHz. The modified antenna output metrics such as gain and bandwidth have no variation from the initial design. The antenna response S_{11} and gain are shown in Figure 7, and other antenna metrics such as bandwidth, physical aperture area, and aperture efficiency are compared to state-of-the art BAVA antenna in Table 3.

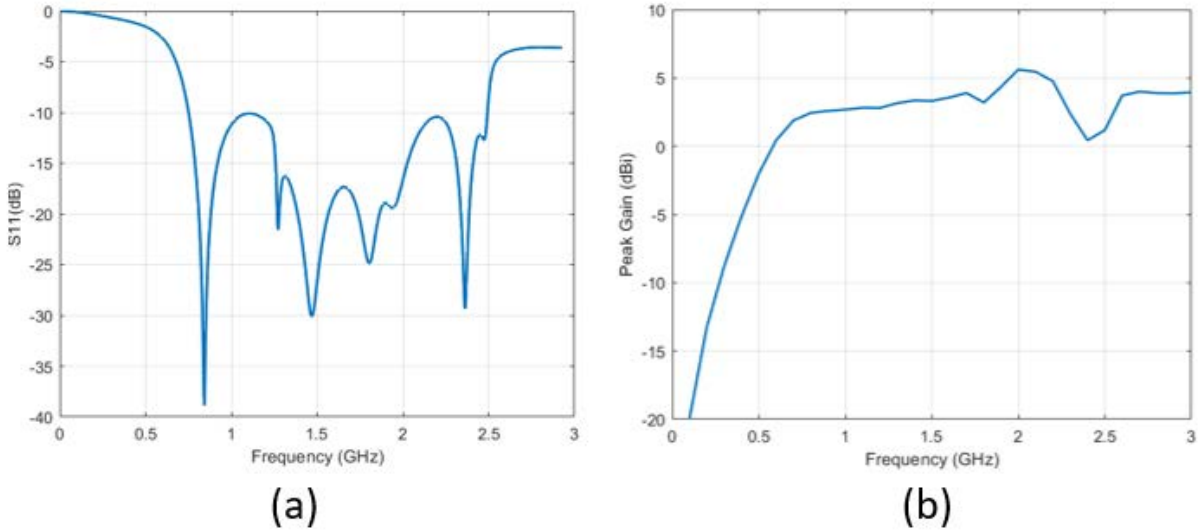


Figure 7. (a) S_{11} for antenna with *a* = 42.5 mm, *b* = 8.5 mm, and *d* = 38 mm, and (b) gain vs. frequency.

Table 3. Comparison of fractal antenna output response metrics with state-of-the-art BAVA.

Antenna Element Type	Aperture Size (mm)	Physical Aperture Area (mm^2)	Bandwidth	Peak Gain (900 MHz) (dBi)	HPBW at 900 MHz		Aperture Efficiency
					E-plane	H-plane	
SOTA BAVA	90 × 90	0.0081	10:1	3	Unknown	Unknown	217%
Fractal Antenna	93 × 85	0.0079	3.33:1	2.58	83.2°	96.2°	208%

3.22.3.5 Antenna fabrication and testing

The designed fractal antenna has been fabricated and tested using a vector network analyzer (VNA). The measured S_{11} response of the fabricated antenna has good

agreement with the S_{11} response of the simulated antenna. The comparison of S_{11} responses is illustrated in Figure 8.

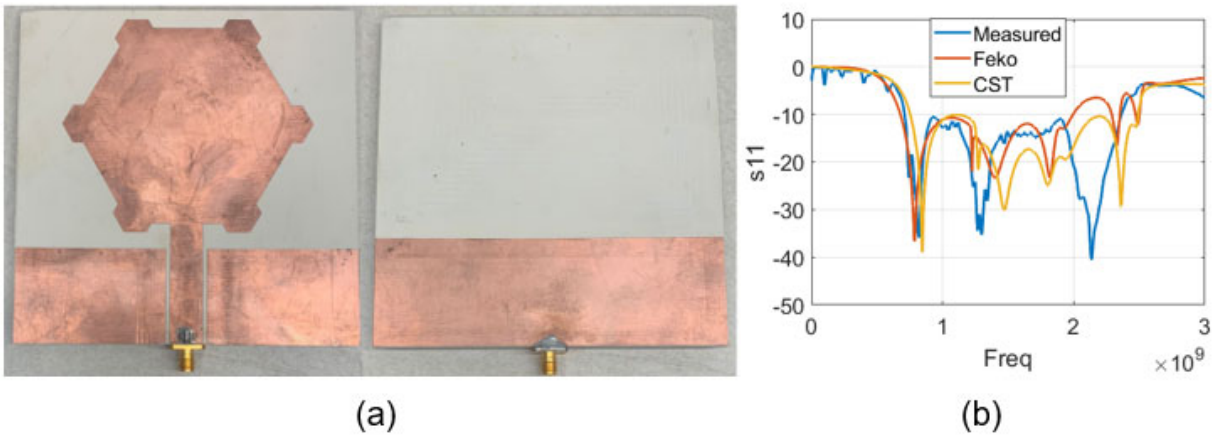


Figure 8. (a) Fabricated antenna (b) reflection coefficient (S_{11}) from Feko, CST, and vector network analyzer (VNA).

3.22.3.6 Tradespace study of fractal antenna array

After concluding the parametric study of the fractal antenna and frequency scaling it to achieve a center frequency of ~1.3 GHz, a tradespace analysis of fractal antenna array geometries has been carried out to analyze and compare antenna metrics. In this process, a square shaped array geometry with sixteen elements, a diamond-shaped array geometry with five elements, an octagon-shaped array geometry with twelve elements, and a hexagon-shaped array geometry with eight elements were arbitrarily selected and designed using commercial electromagnetic (EM) software. Figure 9 illustrates the designed array geometries.

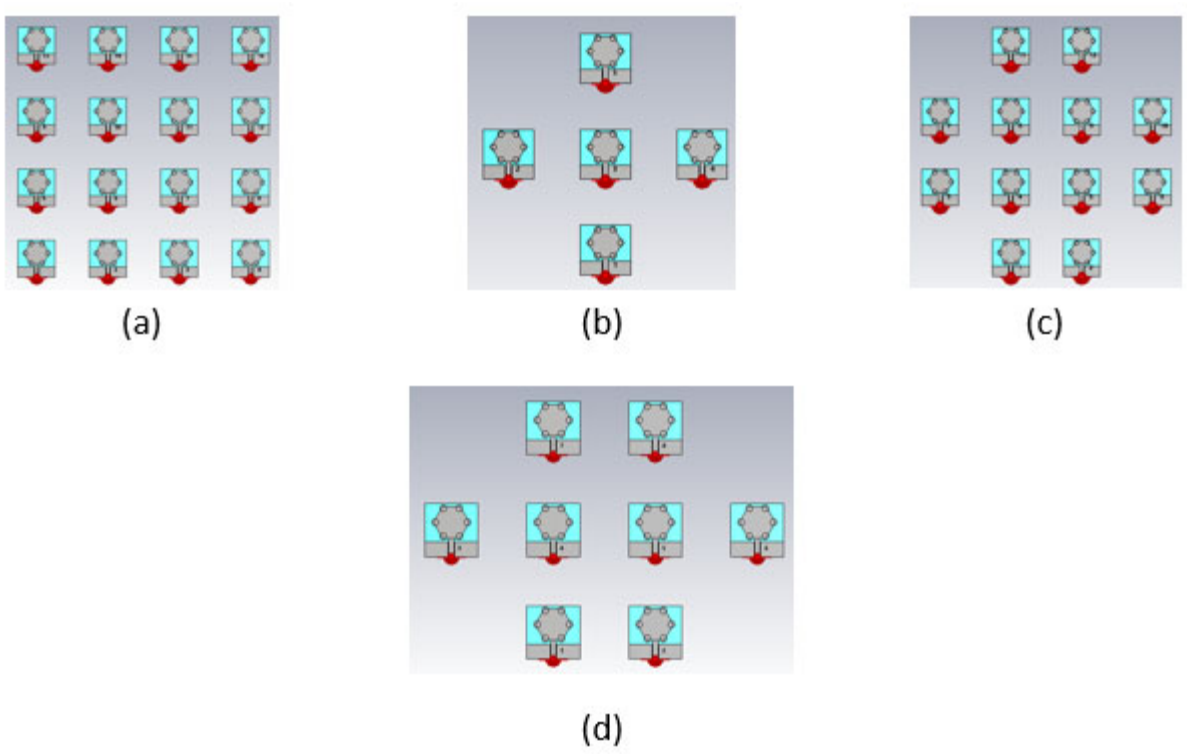


Figure 9. Fractal antenna array geometries: (a) square array geometry, (b) diamond array geometry, (c) hexagon array geometry, and (d) octagon array geometry.

From Figure 10(a), the antenna array with octagonal geometry has lower sidelobe levels while maintaining equivalent gain at 0 degrees. The S_{11} response of the center elements is shown in Figure 10(b). The antenna arrays with hexagonal geometry and octagonal geometry attain maximum bandwidth. Table 4 summarizes the physical aperture area, efficiency, and gain at 900 MHz of all the above-mentioned antenna array geometries. Whereas, the peak gain at 900 MHz for BAVA array is 12.04 dBi with a physical aperture area of 0.0648 m^2 and a 21% of aperture efficiency.

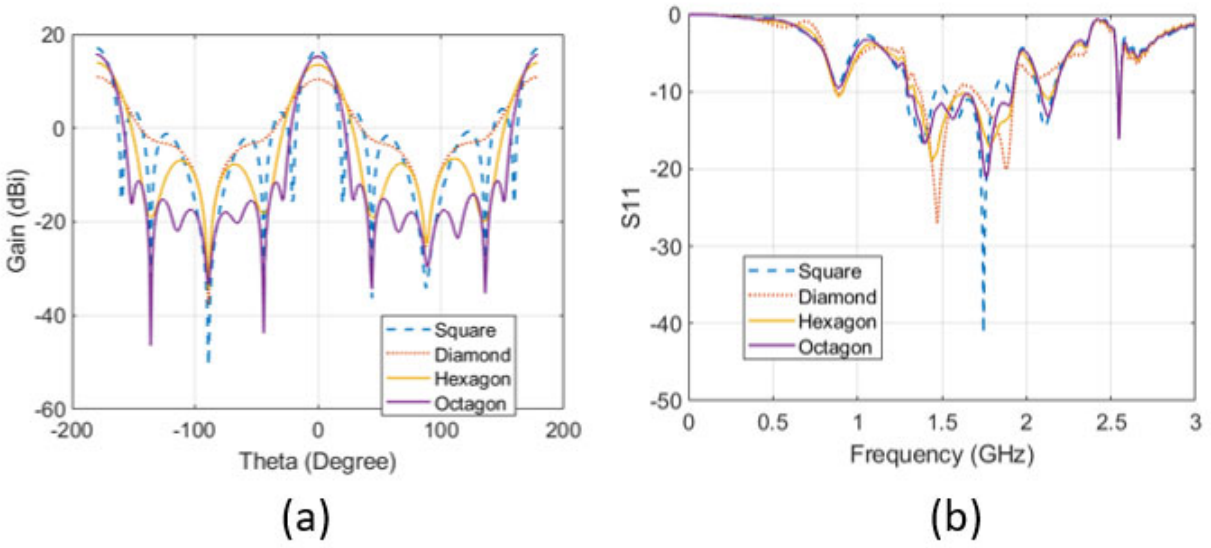


Figure 10. (a) Gain as a function of theta for different fractal antenna array geometries at 900 MHz (b) S_{11} response of center element of array geometries.

Table 4. Array antenna metrics of different antenna array geometries.

Antenna Array Geometry	Physical Aperture Area (mm^2)	Peak Gain (dBi) (900 MHz)	Aperture Efficiency (900 MHz)
Diamond	135.6	10.9	80.8%
Hexagon	280.8	13.9	78.4%
Octagon	483.6	15.7	68.1%
Square	714.0	17.0	63.2%

3.22.4 Summary and Recommendations

From the initial literature search on fractals, a hexagonal patch with hexagon fractals was selected and further investigated. After designing the fractal antenna on an EM solver, a tradespace analysis was carried out to understand the importance of the fractal elements. The addition of fractal elements resulted in achieving multiple resonating frequencies. After validating the initial design, several design parameters (*a*, *b*, *d*, *g*) were studied individually. Starting with ground length *g* from the parametric analysis, increasing ground plane length up to the length of the transmission line improves the return loss. As a result, the *g* value is set to 7.9 mm. Unlike the ground plane length, the fractal antenna radius *b* increase has a positive impact at a lower frequency and a negative impact at a higher frequency. The initial value of *b* was set to be 1.8 mm, but an increase in bandwidth was observed with a new value of 1.66 mm from the optimization algorithm. Finally, the hexagonal patch radius *a* was studied with the help of an optimization algorithm and

yielded an optimum value of 8 mm, which decreased the physical aperture area by 7% and increased aperture efficiency by 29%. The initial design was then modified to achieve a center frequency of 1.3 GHz, and the antenna output metrics had no variation from the initial setup. The modified antenna was fabricated and tested using a vector network analyzer (VNA), which demonstrated good agreement with simulation results in terms of bandwidth.

Further, four different fractal antenna array geometries (i.e., square, diamond, hexagon, and octagon) have been designed and simulated. Upon comparing antenna array metrics, the octagonal fractal antenna array has yielded minimal sidelobe levels with a gain of 15.7 dBi at 900 MHz, close to the square geometry but with a 32.2% lower physical aperture area. Therefore, the octagonal fractal antenna array has been chosen as the optimum geometry with reduced aperture area and reduced side lobes while retaining the bandwidth and gaining milestone metrics. Finally, the bandwidth ratio produced by the fractal antenna (3.3:1) element is relatively lower than that of the SOTA BAVA (10:1). Still, the peak gain at 900 MHz and the aperture efficiency of the fractal antenna element (i.e., 2.58 dBi and 208%) are considerably close to the SOTA BAVA (3 dBi and 217%) with a lower physical aperture area. The octagonal-shaped fractal array has produced a 30.47% larger gain at 900MHz than SOTA BAVA with 0.25% less physical aperture area and 147% greater aperture efficiency.

Recommendations: The fractal antenna can attain UWB characteristics and is an ideal choice for smaller-size applications. The gain response of the designed antenna stayed relatively consistent and exhibits complete bandwidth stability over the UHF range. As the selected antenna has an intricate patch shape with complex fractals, the scope is endless and therefore the application of machine learning (ML) was chosen for more efficient and effective design & optimization. This was pursued as an extension of this work, and will be described in a subsequent report.

3.22.5 References

[1] H. Fallahi and Z. Atlasbaf, "Study of a Class of UWB CPW-Fed Monopole Antenna With Fractal Elements," in IEEE Antennas and Wireless Propagation Letters, vol. 12, pp. 1484-1487, 2013, doi: 10.1109/LAWP.2013.2289868.

3.23 Machine Learning Analysis of Ultra-Wide-Band Antenna Arrays

(Sai Indharapu and Kalyan Durbhakula)

3.23.1 Executive Summary

Ultrawideband patch antennas are a key requirement of the OSPRES program due to their low profile and high-fidelity factor. Most existing patch antennas have complex patch designs and a large number of adjustable parameters (> 10), making it a computationally expensive job to optimize these for reduced aperture area (AA) and converge to the best design. The current state-of-the-art evolutionary optimization algorithms have shown promising results. Still, they consume a lot of time and memory as electromagnetic (EM) wave solvers (commercially available solvers used to calculate output responses of 3D modeled antenna designs) calculate full wave solutions in each optimization iteration. To tackle this problem, we proposed a machine-learning-assisted optimization technique to enhance the performance of optimization algorithms while consuming low computation resources. A hexagonal-shaped fractal antenna was selected for this study due to its complex design (10 adjustable parameters) and high-fidelity factor. The radial basis function and the least-squared regression models employed for a fractal antenna element have produced excellent prediction accuracy with RMSE values less than zero. In contrast, k-nearest neighbor (kNN) and linear regression (LR) models used for fractal antenna array response prediction have relatively higher RMSE values, indicating poor prediction accuracy. Further, the proposed machine-learning-assisted optimization approach applied to a fractal antenna for AA reduction has yielded a 9% increased bandwidth and reduced AA by 6% with >90% less computational time than conventional optimization. Finally, a standalone graphical user interface (GUI) embedded with kNN and LR models was developed to enable users to perform antenna element efficiently & array response prediction, machine learning (ML) validation, analysis comparison, and design optimization.

3.23.2 Objective

Primary Problem: Applying traditional techniques for optimizing antenna elements and antenna arrays for aperture area reduction is a computationally expensive process as they iteratively compare full-wave solutions.

Solution Space: Machine learning models have gained popularity for fast convergence rate, improved accuracy, and flexibility. The efficiency of traditional optimization algorithms can be improved by employing trained ML models as a fitness function.

Sub-Problem:

ML can suffer from underfitting or overfitting the training model, leading to deviations in the predicted output.

State-of-the-Art (SOTA): Conventional full-wave EM solvers such as the method of moments (MoM), multi-level fast multipole method (MLFMM), finite element method

(FEM), and finite difference time domain (FDTD) method are currently being used to study, analyze and assess the performance of UWB antennas.

Deficiency in the SOTA: UWB antenna optimization using conventional EM solvers utilizes significant computational time and memory resources.

Solution Proposed:

(i) Train, validate, test, and compare multiple ML models for quicker and more accurate prediction of antenna array response for different physical aperture areas.

(ii) Replace the fitness function of an optimization algorithm with a trained ML model to enhance the efficiency of the optimization algorithm.

Relevance to OSPRES Grant Objective: The fractal antenna achieves a UWB response, a mandatory requirement of the OSPRES grant objective, in a small volume footprint and similar physical aperture area when compared against the SOTA BAVA, dual ridge horn antennas, etc. Furthermore, the microstrip-design-based fractal antenna can efficiently handle electronic steering by integrating the feed network on the same board. This eliminates the need to build a separate feed network external to the fractal antenna using bulky coaxial cables.

Risks, Payoffs, and Challenges:

(i) A majority of the fractal antenna geometries yield an omnidirectional pattern in the H-plane, which can be a risk. However, efforts are underway to mitigate this pattern without deteriorating bandwidth.

(ii) Payoffs include developing a library of antenna metrics data for various fractal shapes and sizes.

(iii) Design challenges and numerical calculations concerning specific fractal shapes could arise after performing a certain number of iterations to improve the bandwidth further.

(iv) Fractal antennas were known to generate gain loss at random frequencies over their operating frequencies. Therefore, achieving gain stability over the desired frequency range can be a significant challenge.

3.23.3 Technical Approach: Fractal Antenna

To demonstrate this study, a coplanar waveguide-fed fractal antenna is referenced from [1]. The antenna design comprises a hexagonal-shaped fractal element at each corner. The monopole is designed on an FR4 substrate with a thickness of 1.5 mm, a permittivity of 4.4, and a loss tangent of 0.002. Figure 1 illustrates the antenna geometry along with the initial design parameters.

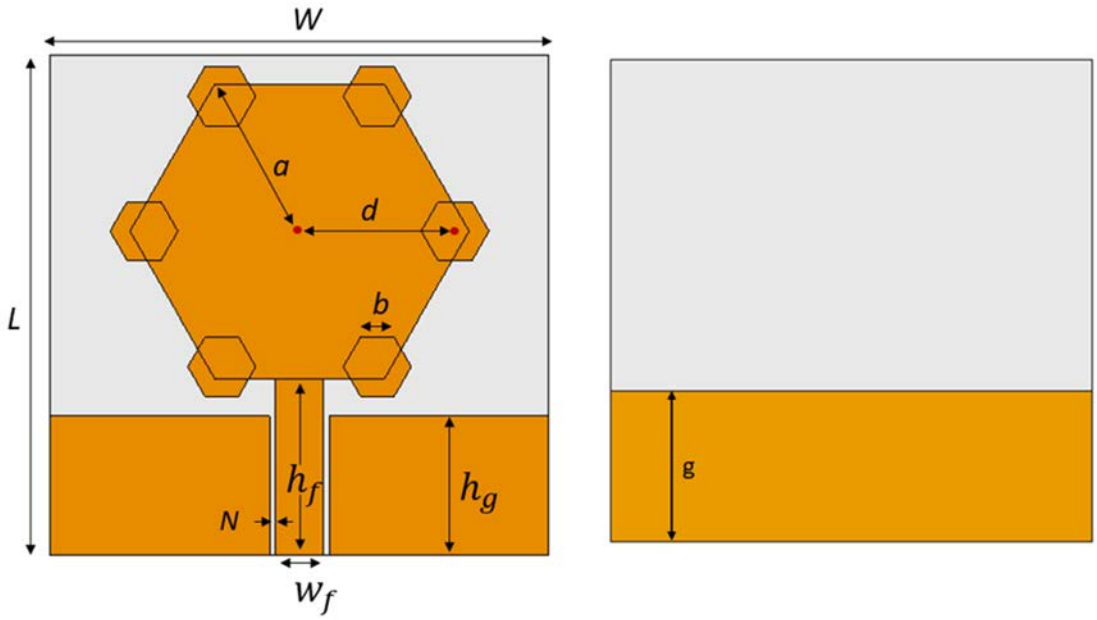


Figure 1. The geometry of the hexagon patch antenna with hexagon fractals. (a) Top view (b) bottom view; a = 8.5 mm, b =2 mm, d = 7.6 mm, R = 2.4 mm, N = 0.3 mm, T = 8.85 mm, F = 7 mm, W = 25, L = 25 mm, g = 7.98 mm.

3.23.4 Tasks, Milestones, and Status

(A) Apply machine learning (ML) models available in Altair Hyperstudy (2021) on the fractal antenna to try and understand the possibilities and limitations of ML models for fast and efficient antenna metrics prediction and optimization. Through successful testing, an ML model can replace conventional EM simulators for speedier optimization and prediction.

- Milestone: Recommend the most accurate and efficient ML model available in Altair Hyperstudy (2021) for antenna element and array metrics prediction. Status: Complete

(B) Apply ML models on the octagon fractal antenna array lattice to extend the prediction capabilities of ML models.

- Milestone: Recommend the best suitable ML model implemented/developed using Python programming for array antenna metrics prediction. Status: Complete

(C) Develop a graphical user interface (GUI) to ease employing ML models to predict antenna output responses.

- Milestone: Incorporate the developed automated data extraction scripts and ML scripts into the GUI to enable the users to predict antenna response quickly. Status: Complete

3.23.5 Results and Discussion

3.23.5.1 Study and Analysis of Machine Learning Models for Fractal Antenna Element Response Prediction using Altair Hyperstudy

Altair Hyperstudy is a commercial software incorporated with various machine learning models. With the help of Altair Hyperstudy, it is possible to generate training data using Altair FEKO, train the selected ML models, and test the result. Initially, three ML models, i.e., radial basis function (RBF), least squared regression (LSR), and hyper kriging (HK), were employed individually to predict the reflection coefficient response of a UWB fractal antenna. The HK model exhibited poor accuracy even with increased training data and therefore was exempted from future studies. The training dataset size for each algorithm was raised to see if the prediction output accuracy increased. Four training dataset sizes (5, 10, 15, and 20) were considered. Each training dataset contains *a* and *b* as inputs and corresponding output (S_{11} response) for 30 different discrete frequency points over a range of 100 MHz to 3 GHz. The results of the above study are illustrated below in Figure 2.

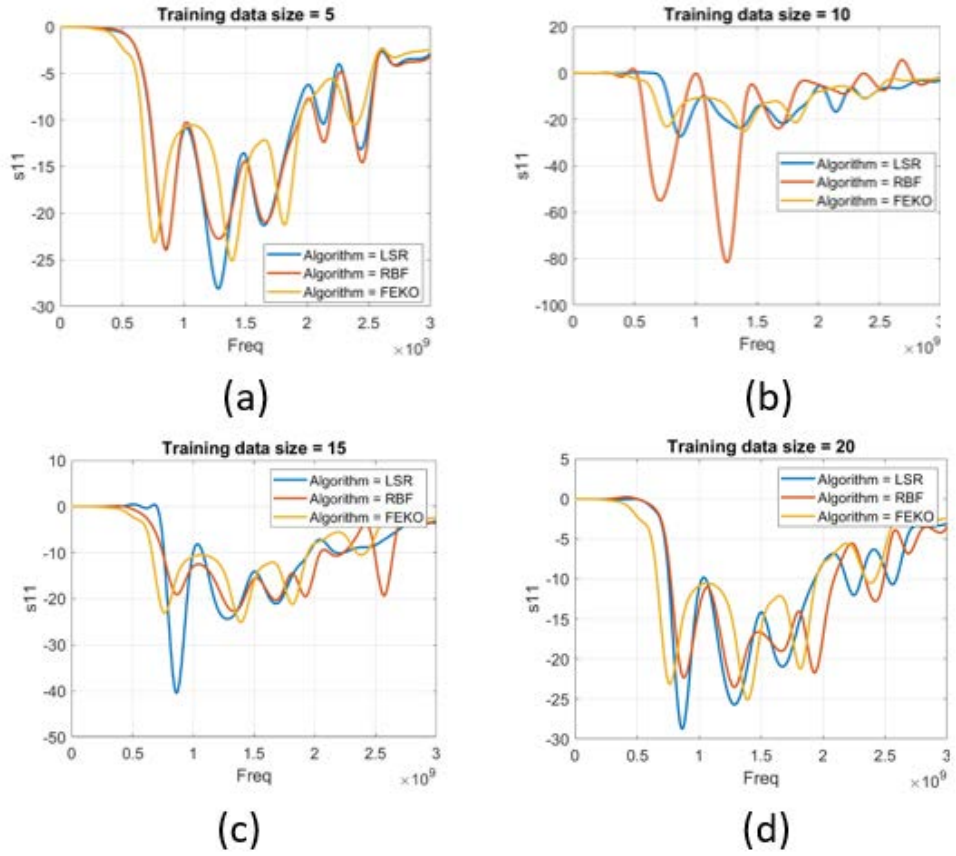


Figure 2. (a) comparison of reflection coefficient (S_{11}) comparison of LSR, RBF, and FEKO for training data set sizes of (a) 5, (b) 10, (c) 15, and (d) 20.

Except for the training data set size equal to 10, the other three results from the LSR model and the RBF model agree with FEKO, as shown in Figures 2(a), 2 (c), and 2(d), respectively. While the LSR model and RBF model agree with each other and with FEKO, the RBF model is in better agreement with FEKO regarding S_{11} values and the S_{11} bandwidth. These results indicate that the RBF ML algorithm can be applied to predict the S_{11} performance of a fractal antenna.

In the case of gain response prediction, the RBF model and LSR model were trained with *a* and *b* values in the training data input, while the training data output has gain values for the respective *a* and *b* values. The training data was generated for 30 discrete frequency points over a range of 100 MHz to 3 GHz with a step size of 100 MHz. This step was taken to eliminate interpolated data in training. Figure 3 shows that both the RBF and LSR models agree with the FEKO response.

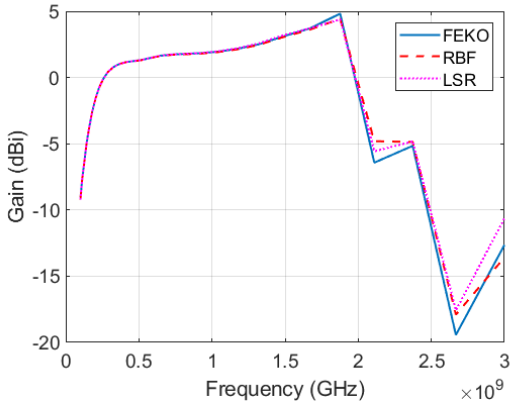


Figure 3. Gain (dBi) comparison of FEKO with radial basis function (RBF), least square regression (LSR).

Further, the ML models, RBF and LSR, were employed to predict the electric field strength radiated by the fractal antenna in the far field region. So, in developing training data, the hexagonal patch radius *a* and fractal side length *b* values were used in the training input. The corresponding electric field strength at 30 discrete frequency points over a range of 100 MHz to 3 GHz with a step size of 100 MHz was used in the training data output. Figure 4 illustrates the electric field strength of a fractal antenna at three far-field points (i.e., 100, 200, and 300 mm) predicted by the ML models and calculated using FEKO. The prediction of the ML model (RBF) has a very close agreement with that of the FEKO response.

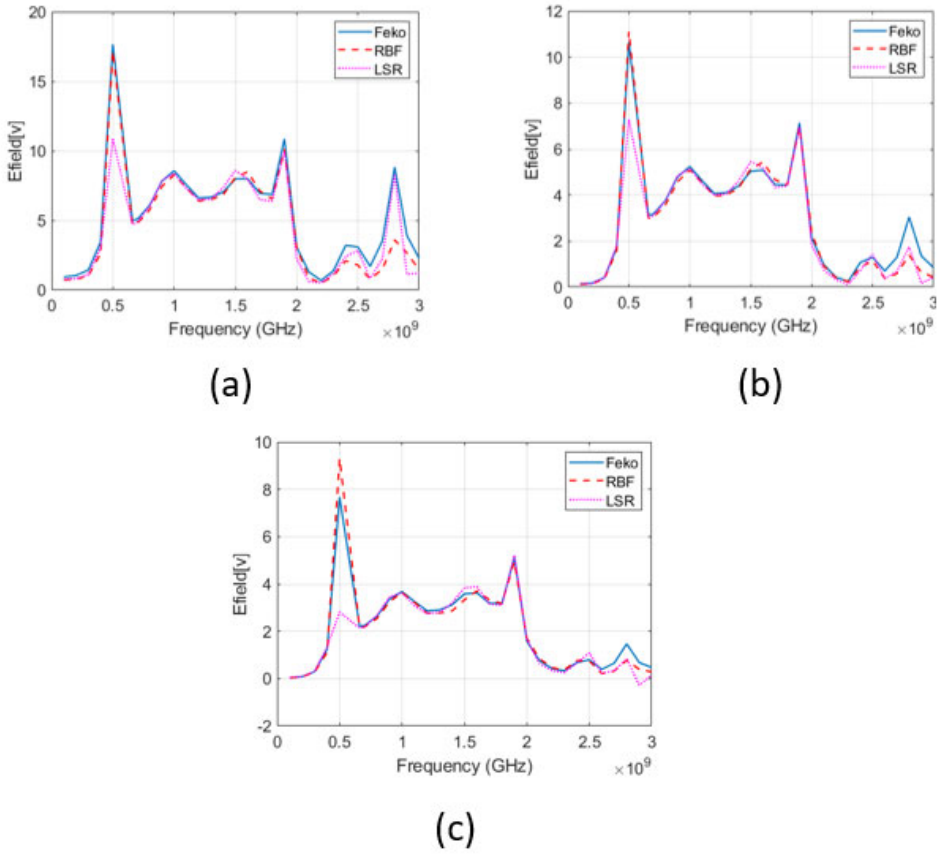


Figure 4. The electric field strength in a far-field region at a distance (a) 100 mm, (b) 200 mm, and (c) 300 mm from a fractal antenna.

Finally, RMSE was calculated between the RBF and LSR modesl for each antenna output response and tabulated in Table 1. RMSE for both RBF and LSR models is less than zero indicating good generalization capability. In comparing the RBF model to the LSR model, the RMSE values from the RBF ML model are lower than the LSR ML model.

Table 1. RMSE comparison of the RBF model with the LSR model.

Antenna output response		RMSE values	
		RBF	LSR
S_{11}		0.0430	0.0108
Gain		0.4517	0.5325
E-field at	100 mm	0.0280	0.0268
	200 mm	0.3972	0.7249
	300 mm	0.3505	0.9228
E-field (time domain)		kNN	
		0.22	

Furthermore, the kNN model, available in the sckit-learn package, was validated for E-field response in the time domain. The complete process of generating a Gaussian pulse and using it as input to perform a time-domain analysis was performed using CST microwave studio. Figure 5(a) illustrates the custom-generated Gaussian pulse (Fmin = 700 MHz and Fmax = 3 GHz), and Figure 5(b) is the comparison of kNN and CST response for the test data. The training data was selected to cover extreme points of the antenna design variable values used to generate the training data. As a result, the RMSE value for the kNN is as low as 0.2246, indicating a good generalization capability of the ML model.

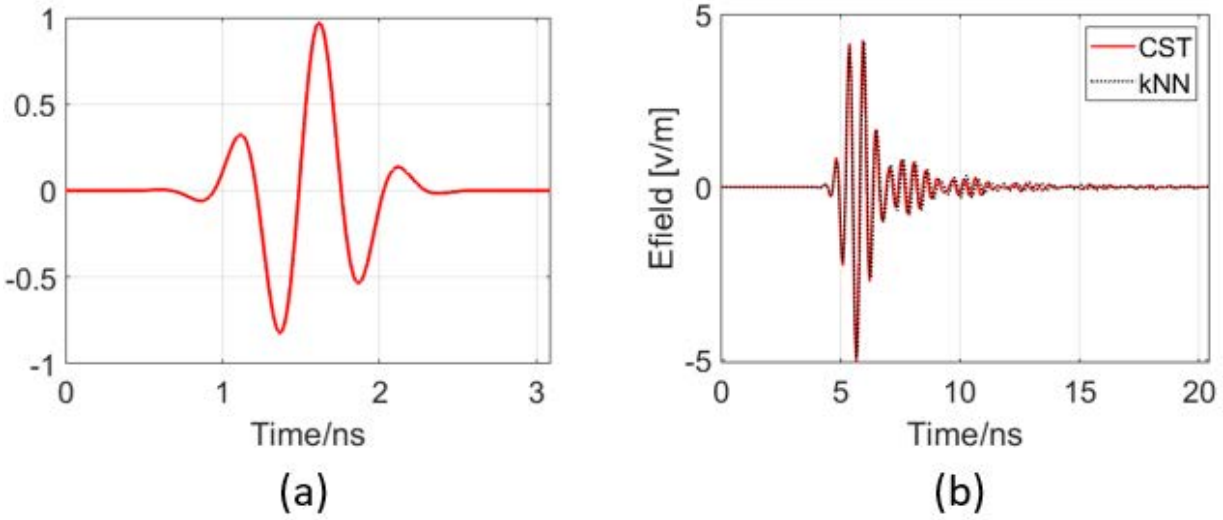


Figure 5. (a) Input gaussian pulse, (b) Comparison of E-field response calculated from CST and predicted by kNN ML model.

The ML models (RBF model, LSR model, HK model) available on Altair Hyperstudy were thoroughly examined, and the performance of each model is evaluated by comparing the response from ML prediction against CST or FEKO response. From the initial study, the RBF and LSR models have shown excellent agreement with FEKO with significantly less training data and RMSE values. As the application of ML models using Altair Hyperstudy is limited to an antenna element, applying ML models for antenna response prediction and optimization is carried out using python scripting.

3.23.5.2 Study and Analysis of Machine Learning Models for Octagonal Shaped Fractal Antenna Array.

In the array response prediction, we tried to predict the reflection coefficient (S_{11}) of non-symmetric individual elements in an array shape. For example, in an octagon array shape, the S_{11} of a central component and any corner element is unique. Therefore, the S_{11} of another aspect would be equal to the center or corner elements, as shown in Figure 6.

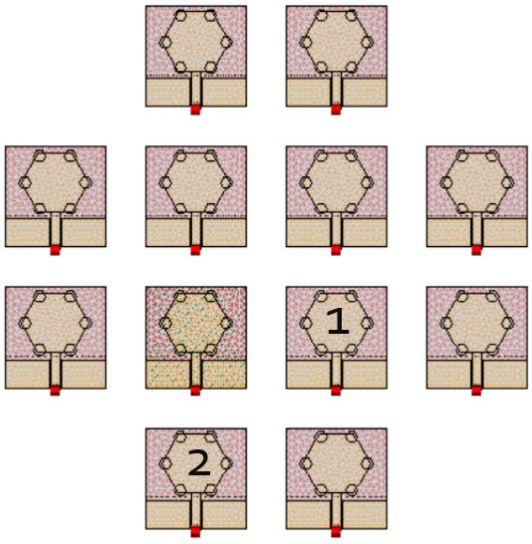


Figure 6. An octagonal shape fractal antenna array with a center element is indicated as '1', and the corner element is shown as '2'.

The ML prediction of reflection coefficient (S_{11}) for the center and corner elements has been expanded using a new algorithm linear regression (LR) available on the scikit learn package. Figure 7 compares the standard FEKO output against S_{11} predicted using kNN and LR ML models. We can observe that the LR ML model agrees better with the FEKO output than the kNN model. This can be seen for both center and corner elements. Table 2 compares the RMSE values obtained from the kNN and LR models in their prediction of S_{11} for the center and corner elements. It is evident from Table 2 that the LR ML model implemented in Python yields a lower value than the kNN ML model for the center and corner elements.

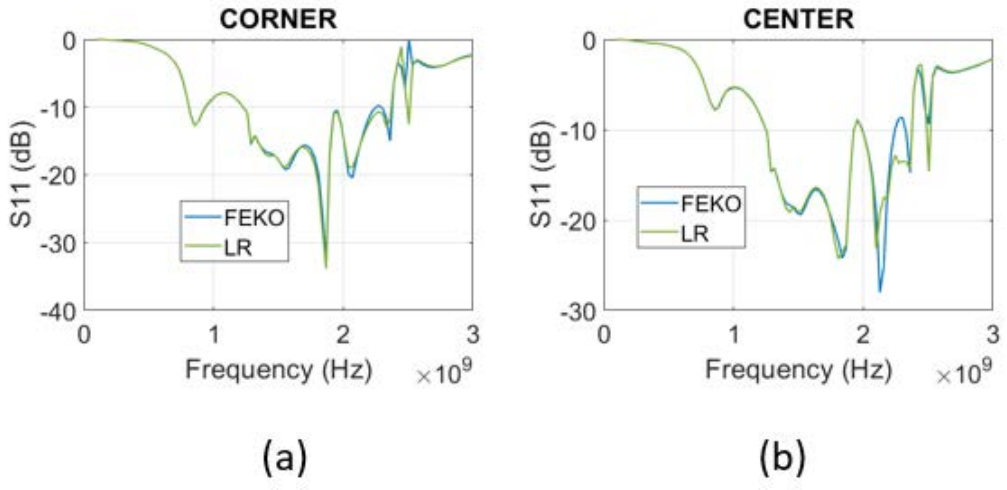


Figure 7. Compare S11 predicted by kNN and LR ML models against FEKO for (a) corner element and (b) center element.

Boresight gain is an important metric when characterizing an antenna's performance. Therefore, the models have been applied to predict gain at boresight for the optimized octagon antenna array. Figure 8 compares the gain predicted using kNN and LR ML models against FEKO gain for the optimized octagon antenna array. Both ML models, kNN and LR, have shown decent agreement in the gain prediction over the frequencies of interest. The RMSE values obtained from kNN and LR gain prediction are 4.8379 and 4.1652, respectively. Although these values are lower than the S_{11} RMSE values, we believe the numerical error causes this massive error in the FEKO training data around 2.5 GHz, as shown in Figure 8. One way to solve such numerical errors is to employ excellent mesh to discretize the antenna geometry.

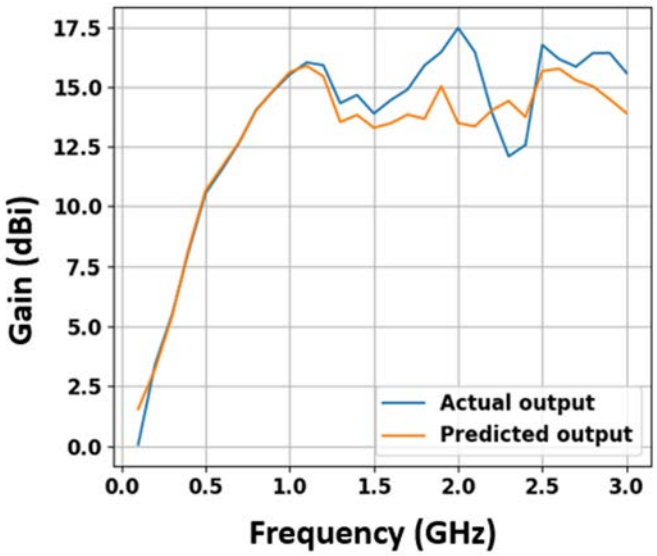


Figure 8. Gain prediction using kNN and LR ML models.

Further, kNN and LR models were applied for gain (theta) predictions. To generate the training data for five different sets, the interelement spacing (IE) between individual antenna elements has been varied. Five antenna array designs with different IE values (i.e., 80 mm, 90 mm, 100 mm, 110 mm, 120 mm) are simulated using CST studio. To validate the trained ML model, a new IE value (i.e., 125 mm) is considered. Figure 9 demonstrates the comparison between the two ML models against the radiation pattern obtained from CST. The plot shows that both the KNN and LSR models have a good agreement with CST. The LSR prediction deviated from the CST result in the region where sidelobes are prominent. However, KNN showed a better understanding of CST across the full θ-angle. From Table 2, the RMSE value of the KNN model is 2.4225, whereas the RMSE value for the LSR model is 4.3635. The KNN model performs better with lower RMSE values compared to LSR.

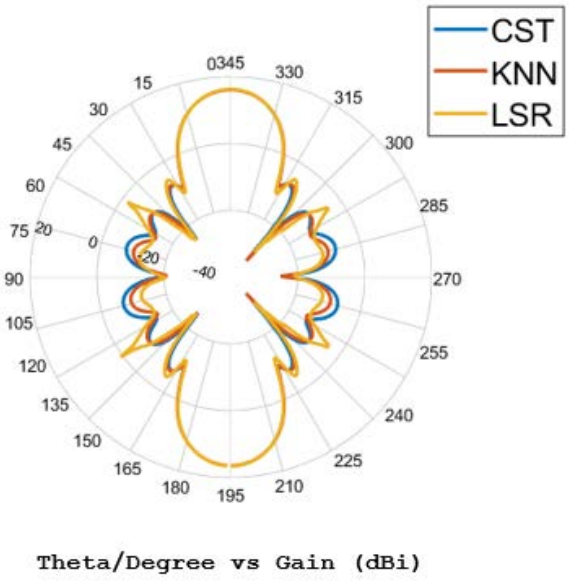


Figure 9. KNN and LSR prediction for gain as a function of theta.

Table 2. RMSE comparison of ML models (Antenna Array).

	RMSE values	
	kNN	LSR
S_{11}	2.2(center) and 1.7 (corner)	NA
Gain	4.8	4.1
Radiation pattern	2.4	4.3
E-field	0.04	NA

Table 3 shows that the computational resources consumed by ML models for antenna array response predictions are much lower than conventional EM solvers.

Table 3. Computational resources comparison of ML models (Antenna Array)

	Conventional approach	ML approach
Antenna response calculations	Using FEM, MoM solvers	Using a trained ML model
Computational time (Fractal antenna array)	~90 mins	<1 sec*

*Does not include simulation time utilized to generate the training data.

The antenna output responses are a non-linear function of design parameters, so the ML models require large amounts of training data. In the antenna array response prediction, unlike the antenna element, no. of features and training data size has decreased due to the high computational time consumption involved in each simulation. Although kNN has produced smaller RMSE values, the generalization of kNN can be further improved with more extensive training data.

3.23.5.3 Development of a Standalone GUI for Antenna Design Analysis using Machine Learning.

A new GUI is developed to enhance the usage of ML models for antenna design response prediction with a visual representation. Unlike the Python scripts, GUI is generalized to extract the training data from *.out (FEKO output) of any antenna irrespective of the geometry size, the frequency range of interest, etc. Further, the extracted data will be stored in excel sheets that can be used as training data for ML models. Finally, GUI can be used to import the extracted training data and train the available ML models. In addition, ML models like KNN and LSR were added to the GUI.

Antenna output response prediction using the GUI:

The following steps are then used for extracting training data for antenna output response prediction on the GUI (Figure 10(a)):

1. Start the process by loading the training input data using the “Load input data” button.
2. In the next step, select the folder contating the *.outfiles using the “Load training output data” button.
3. Finally, Load the test output data using the “Load test output data” button.

Further, the steps below are followed for training and validating the trained ML model:

4. Select the ML model from the drop-down list and train the model using the “Train the model” button.
5. “Validate” button is used to open the validation window.

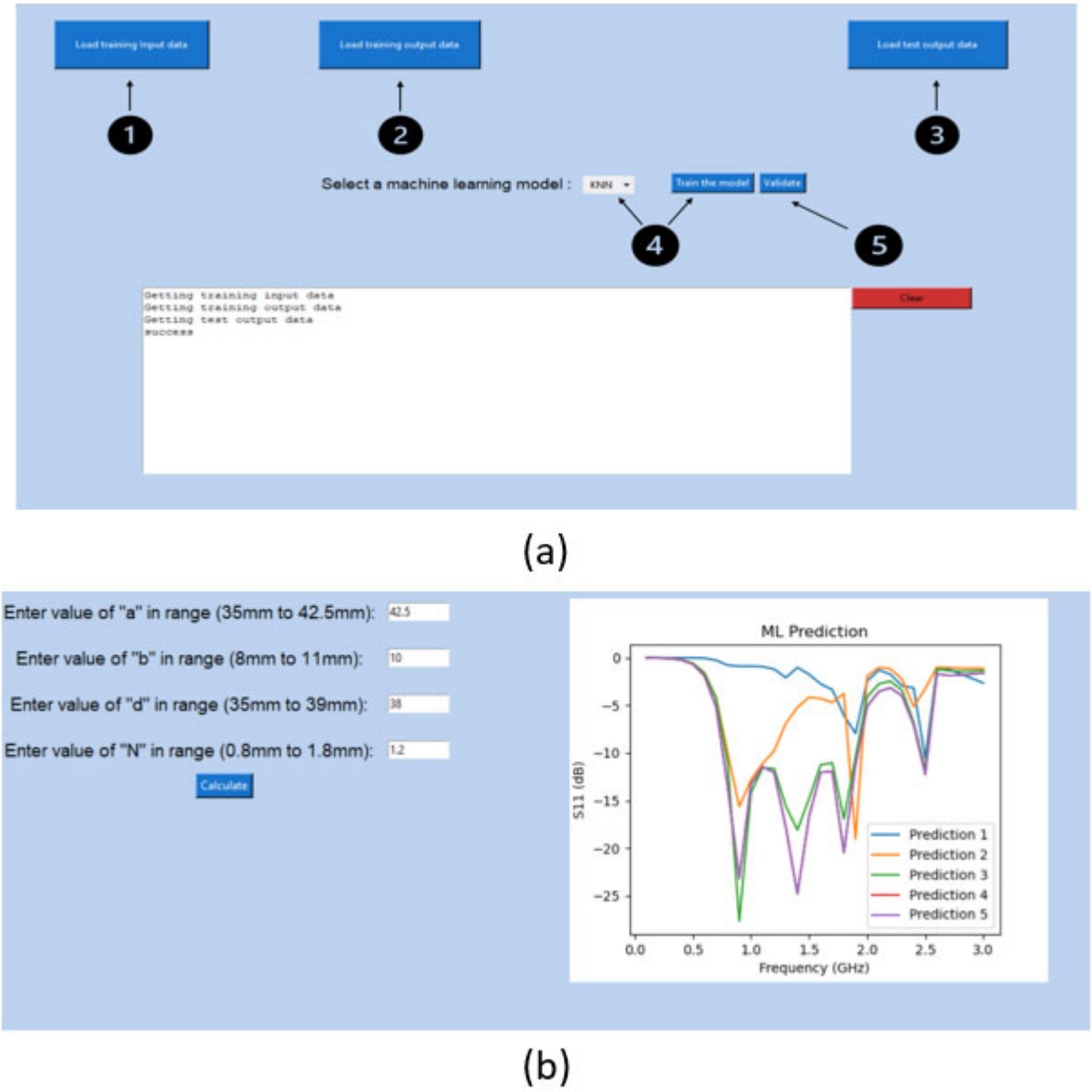


Figure 10. Snapshot of (a) main window and (b) validation window.

Parametric sweep analysis using the GUI:

Parametric sweep analysis on the GUI is performed using a trained ML model. The user can give real-time input and visualize the antenna output response.

Below is the description of the widget in Figure 12(a) and the workflow to perform parametric seep analysis on the GUI:

1. The “Select output type” list is used to specify within the GUI the output response type used in the training data.

2. The “Calculate” button predicts the output response for the user input.
3. The “SweepAnalysis” button opens the parametric sweep window ().
4. “Frequency minimum” & “Frequency maximum” entry fields are used to specify the frequency range of the selected antenna.

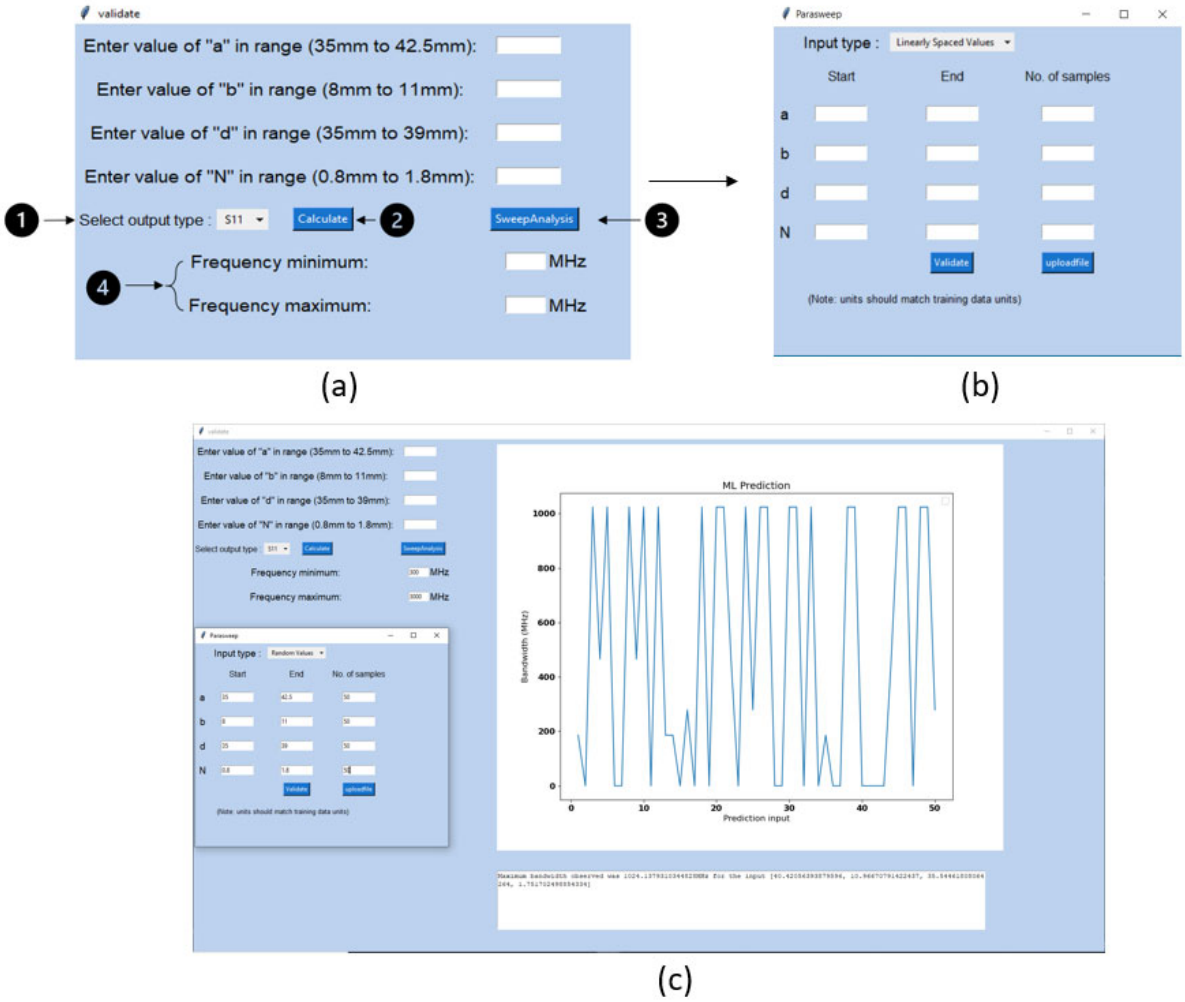


Figure 11. (a) Snapshot of the validation with the “SweepAnalysis” option, (b) Entry field window for parameter ranges, and (c) Snapshot of the validation window with example plot and the text field.

Antenna array analysis using the GUI:

With the new “Antenna Array Analysis” option added to the GUI, users can now calculate Aperture area and Aperture efficiency (given Gain value) for single input or thorough analysis. This option will allow users to learn and uncover the relationship between the physical aperture area and other antenna response metrics. In addition, the GUI allows the user to select from a standard antenna array shape or a custom shape, as shown in Figure 12. Each option requires input from the user (side length of the antenna array shape or an equation to calculate the physical aperture area).

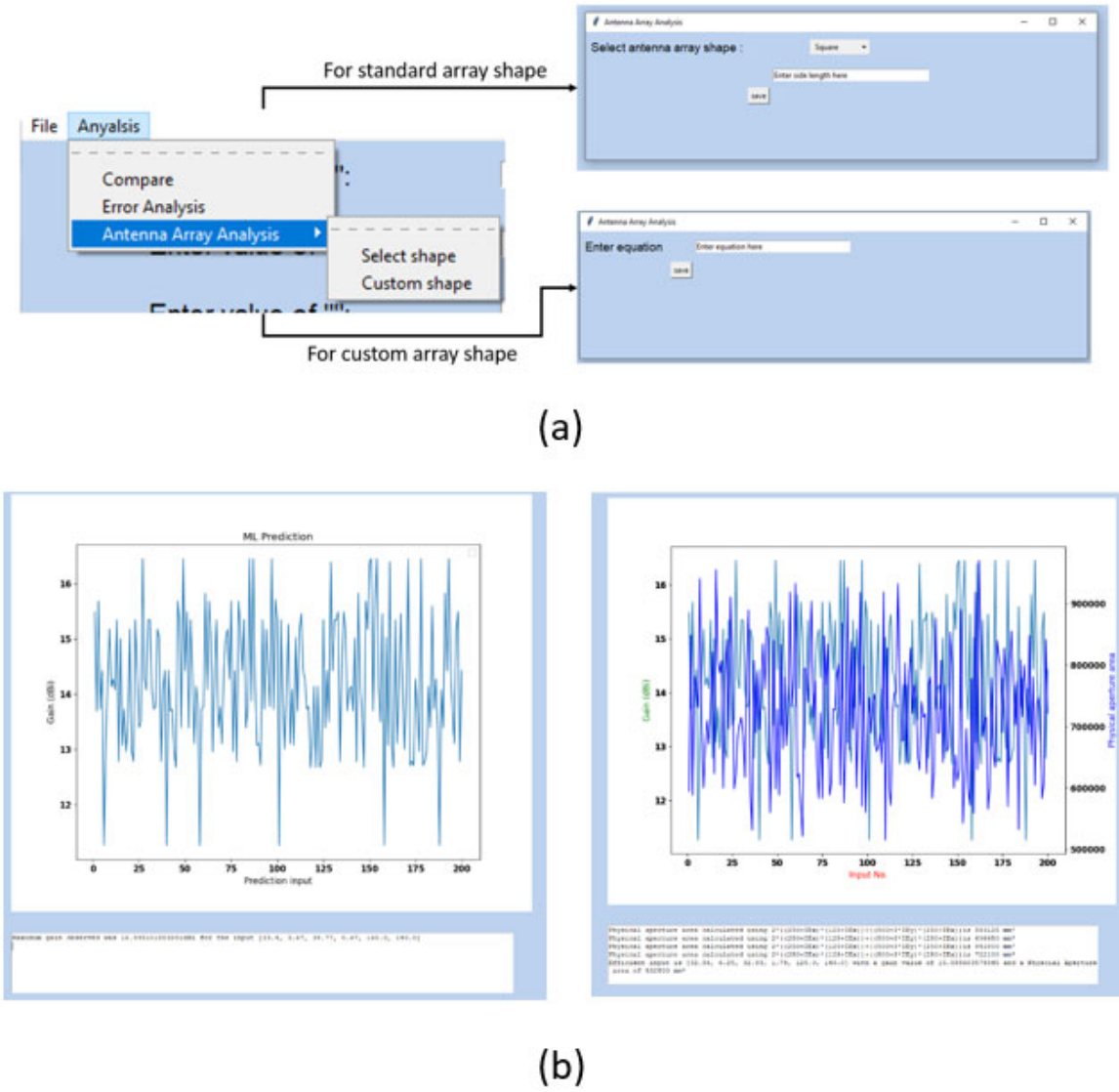


Figure 12. (a) A block diagram illustrating the workflow of Antenna Array Analysis, (b) a Snapshot of the validation window demonstrating results obtained from the analysis.

Many features, like error calculations, antenna array analysis, parametric sweep analysis, etc., were added to the GUI. However, unlike the Altair Hyperstudy, the GUI is not limited to antenna element analysis. Although other essential features like grid search operations, optimization algorithms, automating the generation of training data through the GUI, and tuning the hyperparameters of the selected ML models, the option to import a new machine learning model can be added to the GUI.

3.23.6 Summary

(A) The ML models available in Altair Hyperstudy (radial basis function (RBF) and least square regression (LSR)) were employed and evaluated to predict the output response of a fractal antenna. The RBF and LSR models were down-selected from the initial three ML models (i.e., RBF, LSR, and HK) based on this evaluation. However, the RBF model performed well in the prediction of S_{11}, while the LSR model performed slightly better for gain and electric field predictions. In addition, for time-domain electric field prediction, we recommend using the kNN ML algorithm.

(B) The kNN ML model and the LR ML model available in the scikit-learn ML package were employed to predict output responses of an octagonal-shaped fractal antenna array. The initial application of the kNN ML model for predicting the antenna array bandwidth response of center and corner elements yielded positive results. The new LR ML model yielded improved RMSE values (over kNN) in its prediction of reflection coefficient (27.8% less RMSE for the center element and 19.7% less RMSE for the corner element) when compared against CST response. On the other hand, the RMSE values for gain (as a function of theta) prediction using the LR ML model have a 55.5% increase over kNN prediction. Finally, kNN provides better generalization to predict the reflection coefficient, whereas LR provides a better abstraction to expect frequency domain gain in the case of a fractal antenna array.

(C) A GUI was developed to handle antenna response prediction of an antenna element and array geometry. The GUI requires training data for an antenna (single-element or array) of user choice and predicts the desired antenna output response (S_{11}, antenna gain, radiation pattern, electric field) for a range of test data within a few seconds. The GUI has been configured to perform parametric sweep analysis for S_{11} and gain, electric field, and radiation pattern response outputs for the fractal antenna design. Based on feedback/suggestions from other in-house researchers, key features such as data comparison plots, error calculations, data exporting, and antenna array analysis were added to the GUI. Furthermore, the antenna array analysis option displayed the most efficient input combination for which the antenna array has less physical aperture area and high gain. Finally, the RMSE values for the predicted outputs (i.e., S_{11} and growth, electric field, radiation pattern) of an antenna array were close to 0, and the computational time was reduced from 90 mins to less than 1 sec for a single simulation. The existing GUI version has many features that need to be available on Altair Hyperstudy (i.e., antenna array response analysis, Parametric sweep analysis). Still, other features like grid search operations, optimization algorithms, automating the generation of training data through the GUI, tuning the hyperparameters of the selected ML models, option to import a new machine learning model can be added to the next version to make it a complete package for ML embedded antenna analysis.

3.23.7 Recommendations and Future Work

The study and analysis of applications of ML models for antenna elements and antenna arrays have shown the viability of using ML models for antenna design optimization and prediction. The accuracy or the RMSE values can be improved by increasing the training data size and performing a hyperparameter tunning before employing the ML models. In the future, our goal is to stimulate ML models by using them for automation by designing and analyzing antennas using computer-aided methods. This allows users to develop application-specific antennas without any domain expertise.

3.23.8 Outputs

[1] S. S. Indharapu, A. N. Caruso and K. C. Durbhakula, "Supervised Machine Learning Model for Accurate Output Prediction of Various Antenna Designs," 2022 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (AP-S/URSI), 2022, pp. 495-496, doi: 10.1109/AP-S/USNC-URSI47032.2022.9886262.

[2] S. S. Indharapu, A. N. Caruso and K. C. Durbhakula, "Study of Machine Learning Algorithms for Output Response Prediction of a UWB Fractal Antenna," 2021 IEEE Indian Conference on Antennas and Propagation (InCAP), 2021, pp. 510-512, doi: 10.1109/InCAP52216.2021.9726312.

3.23.9 References

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4 OUTPUTS

4.1 Students Graduated

Name	Degree	Last Known
Al-Shaikhli, Waleed	MS Spring 20	Genuen, KS; Cognitive Copper, KS
Alsultan, Khulud	PhD Spring 21	King Saud University, Saudi Arabia
Azad, Wasekul	PhD Summer 21	Applied Materials, Sunnyvale, CA
Berg, Jordan	MS Spring 21	MRI Global, MO
Bhamidipati, John	PhD Spring 22	Intel, NM
Bissen, Bear	MS Spring 19	Capella Space, San Francisco, CA
Bozarth, Ethan	BS 21	
Brasel, Sadie	BS Spring 21	Graduate Student, Rice University, TX
Clark, Justin	BS 22	MRI Global, MO
Dowell, Alexander	BS Spring 22	Graduate Student, UMKC
Fazekas, Max	MS Summer 21	
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Fry, Spencer	BS Spring 2021	Garmin, KS
Hamdalla, Mohamed	PhD Fall 21	MIDE, MO
Hanif, Abu	PhD Spring 21	Intel Corporation, OR
Harmon, Aaron	BS 18	PhD Student, Missouri Univ. of Science & Tech.
Harp, Joshua	MS 19	Small Business
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Herrington Shawn	PhD Summer 21	Honeywell Aerospace, NM
Karnes, Simeon	BS Spring 21	Graduate Student, UMKC
Klappa, Paul	MS Spring 21	Sierra Nevada Corporation, NV
Kovarik, James	MS Spring 21	
Kramer, Noah	MS Spring 19	MIDE, MO
Labrada, Dario	BS Spring 20	Honeywell Aerospace, FL
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory, CA
Landwehr, Colby	BS Fall 21	Burns & McDonnell
Reed, Demetri	BS Spring 22	Evergy, MO
Renzelman, Jeff	MS Spring 18	Sensata Technologies, MA
Roy, Sourov	PhD Spring 21	BTCPower, Orange County, CA
Smith, Cody	BS 20, MS 21	Winchester Ammunition, MO
Thompson, Heather	MS 20	University of Missouri-Kansas City, MO
Wagner, Adam	MS Fall 20	Los Alamos National Laboratory, NM
Utt, Anthony	BS	
Xia, Shengxuan	BS	PhD Student, Missouri Univ. of Science & Tech.

4.2 Journal Publications

4.2.1 In Preparation

[1] F. Berber Halmen *et al.*, “Magnetic Pulse Compression with High-Frequency, Continuous-Wave Input,” In Preparation, **2023**.

[2] G. Bhattarai *et al.*, “Optimizing Multi-Stacked Nanosecond DSRD-Based Pulser: Theory, Simulation, and Experiment,” *IEEE Transactions in Power Electronics*, In Preparation, **2023**.

[3] M. Hamdalla, V. Khilkevich, D. G. Beetner, A. N. Caruso, A. M. Hassan, “Characteristic Mode Analysis Justification of the Stochastic Electromagnetic Field Coupling to Randomly Shaped Wires,” *IEEE Transactions on Electromagnetic Compatibility*, In Preparation, **2023**.

[4] S. S. Indharapu, A. N. Caruso, K. C. Durbhakula, “Machine Learning Assisted Antenna Design Optimization of UWB Fractal Antenna,” TBD, In Preparation, **2023**.

[5] J. K. P Bhamidipati, G. Bhattarai, A. N. Caruso, “Effect of Proton Irradiation Induced Localized Defect/Trap Clusters on Silicon Photoconductive Semiconductor Switch (Si-PCSS) Recovery Time and Leakage currents,” *Solid-State Electronics,* In Preparation, **2023**.

[6] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “UHF and L-Band Frequency Generation at MW Peak Power using Diode-based Nonlinear Transmission Lines as Pulse Forming Networks,” *Transactions on Plasma Science*, In Preparation, **2023**.

[7] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “Electrically Tunable Diode-based Nonlinear Transmission Line,” *TBD*, In Preparation, **2023**.

[8] B. Barman, D. Chatterjee, and A. N. Caruso, “Design and Analysis of a Class of Wideband, Electrically Small, Microstrip Patch Antenna Elements for Phased Array Applications,” *IEEE Antennas and Propagation Magazine,* In Preparation, **2023**.

4.2.2 Submitted / Under Revision

[9] M. S. Richman, J. A. Harp, N. S. Petersen, T. D. Fields, A. M. Hassan, R. B. Hoffman, J. Tiller, J. W. Luginsland, J. Rushing, and A. N. Caruso, “High-Power Microwave Effects and Performance Against Formations of Unmanned Aircraft Systems,” *Journal of Defense Research and Engineering*, Submitted August 23, **2022**.

[10] E. W. Gasta, E. D. Krulewich, M. A. Mardikes, N. S. Petersen, A. H. Stark, T. D. Fields, and R. B. Hoffman, “Surface and Airborne HPM Effector Capabilities Realized by Computational Wargaming,” *Journal of Defense Research and Engineering*, Submitted May 27, **2022**, Resubmitted revised version.

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4.2.3 Published / In Press

[14] M. Z. M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Electromagnetic Compatibility Analysis of Quadcopter UAVs Using the Equivalent Circuit Approach," *IEEE Open Journal of Antennas and Propagation*, vol. 3, pp. 1090-1101, **Sept 2022** [doi].

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4.3 Conference Publications

4.3.1 Submitted / Accepted

[1] A. Dowell and K. Durbhakula, “An UWB and High Gain Combined Antenna for HPM Applications,” *in International Symposium on Antennas and Propagation*, Portland, Oregon, USA, July **2023** (in preparation).

[2] A. Dowell and K. Durbhakula, “Novel Combined Antenna Design with Partial Dielectric Impedance Transformer for HPM and EW Applications,” *IEEE Transactions on Antennas and Propagation*, July **2023** (in preparation).

[3] S. Bellinger, A. Caruso, and A. Usenko, “Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme,” *GOMACTech*, San Diego, CA, March 20-23, **2023**.

4.3.2 Presented

[4] A. Usenko, A Caruso, S. Bellinger, S. Dhungana, and R. Allen, “Adopting Processes from Mainstream Silicon Technology to Discrete Power Devices Technology,” *2nd Annual Workshop on Solid State Devices and Applications for Directed Energy at GE Research*, Niskayuna, NY, October 26-28 **2022**.

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[6] S. Xia, J. Hunter, A. Harmon, M. Z. M. Hamdalla, A. M. Hassan, C. Hwang, V. Khilkevich, D. G. Beetner, "A Fast Cascading Method for Predicting the Coupling from External Plane Waves to PCBs," *2022 IEEE International Symposium on EMC+SIPI*, Spokane, Washington, August 1-5, **2022**, pp. 152-157 [doi].

[7] J. Hunter, S. Xia, A. Harmon, M. Z. M. Hamdalla, A. M. Hassan, V. Khilkevich, D. G. Beetner, "A Segmentation Strategy for Structures with Common Mode Coupling,"

2022 IEEE International Symposium on EMC+SIPI, Spokane, Washington, August 1-5, **2022**, pp. 415-420 [doi].

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[19] T. Layman, T. D. Fields, and O. A. Yakimenko, "Evaluation of Proportional Navigation for Multirotor Pursuit," AIAA SciTech Forum, Virtual Event, January 11-21, **2021** [doi].

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[48] W. Azad, S. Roy, A. S. Imtiaz, and F. Khan, "Microelectromechanical System (MEMS) Resonator: A New Element in Power Converter Circuits Featuring Reduced EMI," *2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, Niigata, May 20-24, **2018**, pp. 2416-2420 [doi].

4.4 Conference Presentations

4.4.1 Submitted / Accepted

[1] S. Bellinger, A. Caruso, and A. Usenko, "Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme" *GOMACTech* 2023, San Diego, CA, USA, March 20-23 **2023** (*submitted*).

4.4.2 Presented

[2] A. Usenko, A. Caruso, S. Bellinger, S. Dhungana, R. Allen, "Adopting Processes from Mainstream Silicon Technology to Discrete Power Devices Technology" *2nd Annual Workshop on Solid State Devices and Applications for Directed Energy at GE Research*, Niskayuna, NY, October 26-28 **2022** (*submitted*).

[3] S. Sisk and S. Sobhansarbandi, "In-Chip Cooling Technology within Semiconductor Switches," *UMKC SUROP Symposium*, Kansas City, MO, Sept **2022** (poster).

[4] S. Bellinger, A. Caruso, A. Usenko, "New Paradigm on Making Semiconductor Opening Switches for Pulsed Power," *2021 23rd IEEE Pulsed Power Conference*, Denver, CO, Dec. 12–16, **2021** (oral, virtual).

Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29 **2021**:

[5] B. Barman, D. Chatterjee, A. Caruso, and K. Durbhakula, "Tradespace Analysis of a Phased Array of Microstrip Patch Electrically Small Antennas (ESAs)" (Poster)

[6] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation" (Poster)

[7] J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures" (Poster)

[8] J. Bhamidipati, M. Paquette, R. Allen, and A. Caruso, "Photoconductive Semiconductor Switch Enabled Multi-Stage Optical Source Driver" (Poster)

[9] G. Bhattarai, J. Eifler, S. Roy, M. Hyde, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "All Solid-State High-Power Pulse Sharpeners" (Poster)

[10] S. Brasel, K. Norris, R. Allen, A. Caruso, and K. Durbhakula, "Efforts to Reduce Physical Aperture Area of Ultra-Wideband Arrays" (Poster)

[11] A Caruso, "ONR Short Pulse Research and Evaluation for c-sUAV: Supporting and Sub-Programs Overview" (Oral)

[12] J. Clark, R. C. Allen, and S. Sobhansarbandi, “Ultra-Compact Integrated Cooling System Development” (Poster)

[13] J. Eifler, S. Roy, M. Hyde, G. Bhattarai, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “TCAD Optimization of Epitaxially Grown Drift-Step Recovery Diodes and Pulser Performance” (Poster)

[14] N. Gardner, M. Paquette, and A. Caruso, “Diode-Based Nonlinear Transmission Lines Capable of GHz Frequency Generation at Single MW Peak Powers” (Poster)

[15] M. Hamdalla, A. Caruso, and A. Hassan, “The Shielding Effectiveness of UAV Frames to External RF Interference” (Poster)

[16] M. Hamdalla, A. Caruso, and A. Hassan, “A Predictive-Package for Electromagnetic Coupling to Nonlinear-Electronics using Equivalent-Circuits and Characteristic-Modes (PECNEC)” (Poster)

[17] M. Hyde, J. Eifler, S. Roy, G. Bhattarai, A. Usenko, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Development of an Evaluation Network for Drift Step Recovered Diodes through and Augmented Design of Experiment” (Poster)

[18] S. Indharapu, A. Caruso, and K. Durbhakula, “Machine Learning Based Ultra-Wideband Antenna Array Optimization and Prediction” (Poster)

[19] F. Khan, W. Azad, and A. Caruso, “A Scalable Multilevel-Modular 10 kV Silicon Carbide MOSFET Architecture for Pulsed Power Applications” (Poster)

[20] D. F. Noor, J. Eifler, M. Hyde, G. Bhattarai, S. Roy, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “DSRD-IES Pulsed-Power Generator Topology Study Using Machine-Learning-Based Feature Selection Optimization and Predictive Learning” (Poster)

[21] S. Roy, J. Eifler, M. Hyde, G. Bhattarai, D. Noor, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Systematic Topological Optimization of DSRD-Based IES Pulse Generator” (Poster)

[22] S. Shepard and A. Caruso, “Tubular Core Optical Power Amplifier” (Poster)

[23] H. Thompson, M. Paquette, and A. Caruso, “Minimizing On-State Resistance in GaN:X Photoconductive Semiconductor Switches (PCSSs) for Direct Modulation” (Poster)

[24] A. Usenko, J. Eifler, S. Roy, G. Bhattarai, M. Hyde, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “New Paradigm in Fabrication of Semiconductor Opening Switches for Pulsed Power” (Poster)

[25] J. Harp, A. Caruso, T. Fields, R. Allen, M. Paquette, A. Hassan, J. Currie, N. Kramer, T. Ory, B. Bissen, K. Durbhakula, “Short Pulse Research and Evaluation for sUAS (OSPRES): Program Update”

[26] J. Harp, A. Caruso, T. Fields, R. Allen, J. Currie, N. Kramer, B. Bissen, R. Butler, S. Karnes, S. Herrington, C. Smith, D. Reed, P. Klappa, P. Meyerhoffer, Z. Drikas, M. McQuage, C. Hoshor, B. Grady, J. Lancaster, “OSPRES cUAS Effects Summary”

[27] J. Harp, N. Kramer, T. Ory, and A. Caruso, “Coaxial Ringdown Oscillator (CRO)”

[28] M. S. Richman, N. Petersen, J. Harp, A. Norris, and T. D. Fields, “Fixed HPM Effector Capabilities Realized Through Computational Wargaming”

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[29] S. Bellinger, A. Caruso, A. Usenko, “Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme,” *240th Electrochemical Society Meeting*, Orlando, FL, Oct. 10–14, **2021** (oral) [doi].

[30] J. Clark and S. Sobhansarbandi, “Ultra-Compact Integrated Product Cooling Technology,” *UMKC SUROP Symposium*, Kansas City, MO, Sept **2021** (poster).

[31] S. R. Shepard and H. A. Thompson, “Self-focusing in Guided and Un-guided Media,” submitted to the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, **2021** (oral).

[32] W. Azad, S. Roy, and F. Khan, “A Four-State Capacitively Coupled High-Voltage Switch Powered by a Single Gate Driver,” *47th IEEE Conference on Plasma Science*, Singapore, December 6-10, **2020** (oral).

[33] J. Hunter, S. Xia, A. Harmon, A. Hassan, V. Khilkevich, and D. Beetner, “Simulation-Driven Statistical Characterization of Electromagnetic Coupling to UAVS,” *Annual Directed Energy Science and Technology Symposium*, March **2020** (abstract appeared, but talk cancelled due to pandemic).

***

Directed Energy Professional Society, Annual Directed Energy Science and Technology Symposium, West Point, NY, March 9-13 **2020**:

[34] W. Spaeth, J. Kovarik, R. Allen, S. Fry, B. Bissen, E. Myers, and A. Caruso, “Wideband Parallel Plate to Coaxial Cable Taper”

[35] S. C. Wagner, J. E. Currie, E. R. Myers, and A. N. Caruso, “Quickly Determining Minimum HPC Source Requirements Using Binary Search”

[36] D. Labrada, N. Flippin, and A. N. Caruso, “Rapid Prototyping Nanosecond Pulse Drivers Based on Drift Step Recovery Diode”

***

Government Microcircuit Applications & Critical Technology Conference (GOMAC Tech), Albuquerque, NM, March 25-28 **2019**:

[37] C. Hauptmann, J. Bhamidipati, E. R. Myers, S. Bellinger, and A. N. Caruso, “Reduced Recovery Time in SiPCSS Photoconductive Switches”

[38] E. Myers, J. Bhamidipati, C. Hauptmann, S. Bellinger, A. Conway, and A. N. Caruso, “Picosecond High Power Switching Technologies”

[39] H. Thompson, N. Kramer, E. R. Myers, J. Crow, A. Khoeler, and A. N. Caruso, “GaN Optimization for Use in Photoconductive Switch”

***

[40] B. Barman, D. Chatterjee, and A. N. Caruso, “Analytical Models for L-Probe fed Microstrip Antennas,” *Proceedings of the IEEE Antennas and Propagation International Symposium and National Radio Science Meeting*, Atlanta, Georgia, USA, July 7-12, **2019** (1 page URSI Abstract).

***

Directed Energy Professional Society (DEPS) Annual Directed Energy Science and Technology Symposium, Destin, Florida, USA, April 8-12 **2019**:

[41] R. Butler, A. Gantt, and E. R. Myers, “Mechanical Challenges of Modular Photoconductive Semiconductor Based HPM Sources”

[42] S. Young, M. Richman, J. Bhamidipati, S. Fry, J. Crow, E. Myers, and A. Caruso, “Two-Dimensional Optoelectronic Pulsed Power Switches: Initial Effort”

[43] A. Wagner, J. Lancaster, E. Myers, and A. Caruso, “Rapid Cost Effective RF Component Prototyping Using 3D Printers”

[44] H. A. Thompson, N. J. Kramer, A. Utt, J. Crow, E. R. Myers, A. D. Koehler, and A. N. Caruso, “Cost-to-benefit analysis of GaN for Photoconductive Semiconductor Switches (PCSS)”

[45] C. D. Landwehr, S. Fry, J. Scully, S. Bellinger, E. R. Myers, and A. N. Caruso, “Low Leakage Electroluminescence For Improving SiPCSS Hold Off”

[46] J. Kovarik, B. Barman, D. Chatterjee, and A. N. Caruso, “Some Investigations Into Applications Of Electrically Small Antennas As Phased Array Elements”

[47] S. R. Fry, E. R. Myers, S. L. Bellinger, and A. N. Caruso, “Maximizing SiPCSS Efficiency For HPM Sources”

[48] D. Chatterjee, B. Barman, J. Kovarik, and A. N. Caruso, “Studies On Antenna Characterization And Propagation Of High Power Pulsed Electromagnetic Waves With Minimal Spatial Dispersion”

***

Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium, Oxnard, CA, Feb 26-March 2, **2018**:

[49] J. Scully, N. J. Kramer, P. Doynov, N. M. Flippin, E. Cash, S. Kovaleski, E. R. Myers, and A. N. Caruso, “Photo- and Electro-Luminescence Studies of Silicon-Based Photo-Switches”

[50] C. Hauptmann, E. R. Myers, A. N. Caruso, J. B. Newhook, J. Verzella, S. L. Bellinger, and P. G. Doynov, “Thermal Analysis of a PCSS through TCAD Simulation”

[51] N. Flippin, E. R. Myers, and A. N. Caruso, “Fast Rise Time Switches: Drift Step Recovery Diode”

[52] J. Hunter, Y. Liu, D. Floyd, A. Hassan, V. Khilkevich, and D. Beetner, "Characterization of the Electromagnetic Coupling to UAVs"

[53] E. R. Myers, N. J. Kramer, P. Doynov, N. Flippin, J. Scully, E. Cash, S. Kovaleski, J. Beaudin, S. Bellinger, and A. N. Caruso, "High Power and Electronically Steerable Compact Phased Arrays: Design Considerations"

[54] N. Kramer, A. Koehler, T. Anderson, K. Hobart, F. Kub, S. Bellinger, B. Montag, J. Mcgeehan, Y. Morel, P. Doynov, C. Hauptmann, E. Myers, and A. Caruso, "Carbon Compensated Gallium Nitride for PCSS Applications"

***

Directed Energy Professional Society (DEPS) Annual Science and Technology Symposium, Huntsville, AL, February 13-17 **2017**:

[55] N. Kramer, S. Bellinger, B. W. Montag, J. E. McGeehan, Y. C. Morel, and A. N. Caruso, "Recent Results of Silicon Based Photoconductive Solid State Switches for 500kHz Continuous Pulse Repetition Frequency."

4.5 Theses and Dissertations

[1] Bidisha Barman, "Design, Characterization, and Analysis of a Class of Wideband Microstrip Path Antennas," PhD Dissertation, UMKC, **2023**, In preparation.

[2] Nicholas Gardner, "Diode-Based Nonlinear Transmission Lines as a High-Power Radio Frequency Source," PhD Dissertation, UMKC, **2023**, In preparation.

[3] John Keerthi Paul Bhamidipati, "Pulse Generation, Shaping, and Optimization Solutions for Solid-State-Switch-Enabled High-Power Microwave Generation Systems" PhD Dissertation in Physics and Electrical Engineering, UMKC, **2022** [mospace].

[4] Mohamed Hamdalla, "RF Coupling to Realistic Wire Systems in Complex Environments," PhD Dissertation in Electrical Engineering, UMKC, **2021** [mospace].

[5] Khulud AlSultan, "Scalable Acceleration of The Characteristic Mode Analysis Computational Toolbox Using Big Data Techniques," PhD Dissertation in Computer Science and Electrical Engineering, UMKC, **2021** [mospace].

[6] Jordan N. Berg, "Development of a Jet Impingement Thermal Management System for a Semiconductor Device with the Implementation of Dielectric Nanofluids," MS Thesis in Mechanical Engineering, University of Missouri-Kansas City, **2021** [mospace].

[7] James C. Kovarik, "Wideband High-Power Transmission Line Pulse Transformers," MS Thesis in Electrical Engineering, UMKC, **2021** [mospace].

[8] Wasekul Azad, "Development of Pulsed Power Sources Using Self-Sustaining Nonlinear Transmission Lines and High-Voltage Solid-State Switches," PhD Dissertation in Electrical Engineering, UMKC, **2021** [mospace].

[9] Paul Klappa, “Implementation and Assessment of State Estimation Algorithms in Simulation and Real-World Applications,” MS Thesis in Mechanical Engineering, UMKC, **2021** [mospace].

[10] Shawn Herrington, “Toward a Framework for Systematically Categorizing Future UAS Threat Space,” PhD Dissertation in Electrical and Computer Engineering, UMKC, **2021** [mospace].

[11] Waleed Al-Shaikhli, “Numerical Analysis of Helical And Log-Periodic Antennas For Short Pulse Applications,” MS Thesis in Electrical Engineering, UMKC, **2020** [mospace].

[12] Joshua Harp, “Development of an Adaptive Electromagnetic Interference Testing Method,” MS Thesis in Mechanical Engineering, UMKC, **2019** [mospace].

4.6 IP Disclosures Filed

[1] Khan, Azad, “A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Using Custom High-Voltage Isolated Gate Driver, Coupling, and Snubber Circuit,” 21UMK015, DEC202022.

[2] D. Beetner, V. Khilkevich, A. Hassan, S. Xia, J. Hunter, A. Harmon, “Rapid Prediction of Electromagnetic Coupling to Electronic Circuits and Harnesses,” 22UMK006/22MST007, 2022.

[3] A. Usenko, A. Caruso, S. Bellinger, “Diode Stack and Method of Manufacturing Thereon,” 22UMK003, 12AUG2021.

[4] A. Usenko, A. Caruso, S. Bellinger, “Diode and Method of Making the Same,” 21UMK021, 28JUNE2021.

[5] Bhamidipati, Myers, Caruso, “Cascaded Laser Diode (Array) Implementation with WBG PCSS to Source RF Pulse Generation,” 21UMK009, 04NOV2020.

[6] Shepard, “A Low Noise Optical Amplifier,” 21UMK007, 14SEPT2020.

[7] Eifler, Myers, “Photoconductive Contact Pattern for Enhanced Charge Collection,” 21UMK012, 08JUL2020.

[8] Shepard, “A Novel Optical Fiber Amplifier,” 20UMK012, 02JUN2020.

[9] Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna,” 20UMK011, 19APR2020.

[10] Doynov, “Scalable Modular System for High-power Microwaves Generation,” 20UMK010, 19APR2020.

[11] Doynov, Caruso, “High-efficiency High-power Microwave Generation using Multipass Non-linear Network Topologies,” 19UMK017, AUG292019.

[12] Doynov, “Pulse Differential High-power Microwave Generation,” 19UMK007, 02JAN2019.

[13] Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal,” 19UMK008, 28DEC2018.

[14] Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output,” 19UMK005, 28SEPT2018.

4.7 Provisional Patent Applications Filed

[1] D. Beetner, et al., “Method and System to Rapidly Predict Electromagnetic Coupling to Electronic Circuits and Harnesses,” US Provisional Patent Application 63/388,999, filed 01/04/2023.

[2] F. Khan, A. N. M. Wasekul, “A Multilevel-Modular 10 kV Silicon Carbide MOSFET Module Using Custom High-Voltage Gate Driver, Coupling, and Snubber Circuits,” US Provisional Patent Application 63/331,780, filed 04/15/2022.

[3] Plamen Doynov, James Prager, Tim Ziemba, Anthony N. Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, USPTO Provisional Serial No. 62/737,185, filed 09/272018.

4.8 Non-Provisional Patent Applications Filed

[4] A. Usenko, A. Caruso, S. Bellinger, “Stacked Diode with Side Passivation and Method of Making the Same,” US Patent Application 17/946,022, filed 09/15/2022 (provisional 63/245,778 filed 09/17/2021).

[5] A. Usenko, A. Caruso, S. Bellinger, “Diode and Method of Making the Same” US Patent Application 17/855,735, filed 06/30/2022 (provisional 63/216,550 filed 06/30/2021)

4.9 Patents

[1] P. Doynov, A. Caruso, “Multi-Pass Nonlinear Network for Microwave Generation” US Patent No. 11558036, Issued 01/17/2023 (US Patent Application 17/455,026, filed 11/16/2021).

5. APPENDIX A: FINAL PROGRAM REVIEW PRESENTATIONS

Overview. The OSPRES Grant Final Review was held in conjunction with the OSPRES and PTERA Fall Technical Review and Exchange at the University of Missouri-Kansas City. The OSPRES Grant session was held on November 2, 2022, and consisted of 9 talks covering the cumulative efforts from the latter half of the OSPRES Grant program. Approximately 50 internal and 25 external (government, industry, academia) participants RSVP'd for this session, with approximately 2/3 of these in attendance. The agenda is provided below and the talks compiled in this Appendix.

1230-1300	Lunch
1300-1320	OSPRES Grant Motivation and Overview (Caruso, Paquette)
1320-1350	Sub-ns Pulse Generation Using Drift-Step Recovery Diodes (Bhattarai, Eifler)
1350-1420	Solid-State Switch and Diode Devices (Bellinger)
1420-1450	Novel Process Flow for Manufacturing of Drift Step Recovery Diodes (Usenko)
1450-1505	Break
1505-1535	Design Considerations for Photoconductive Semiconductor Switches (PCSS) (Bhamidipati, Eifler)
1535-1555	Diode-Based Nonlinear Transmission Lines for Ultra-High Frequency Generation (Video) (Gardner)
1555-1635	UWB Antenna Tradespace Analysis Outcome with Emphasis on Futuristic Design Methodologies (Durbhakula, Barman)
1635-1655	Optical Fiber Lasers and Amplifiers (Shepard)
1655-1715	Design and Development of a Jet Impingement Thermal Management System (Video) (Sobhansarbandi)
1715-1720	Day 1 Closing

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for c-sUAV Study (OSPRES Grant)

N00014-17-1-3016
09/30/2017-09/29/2022

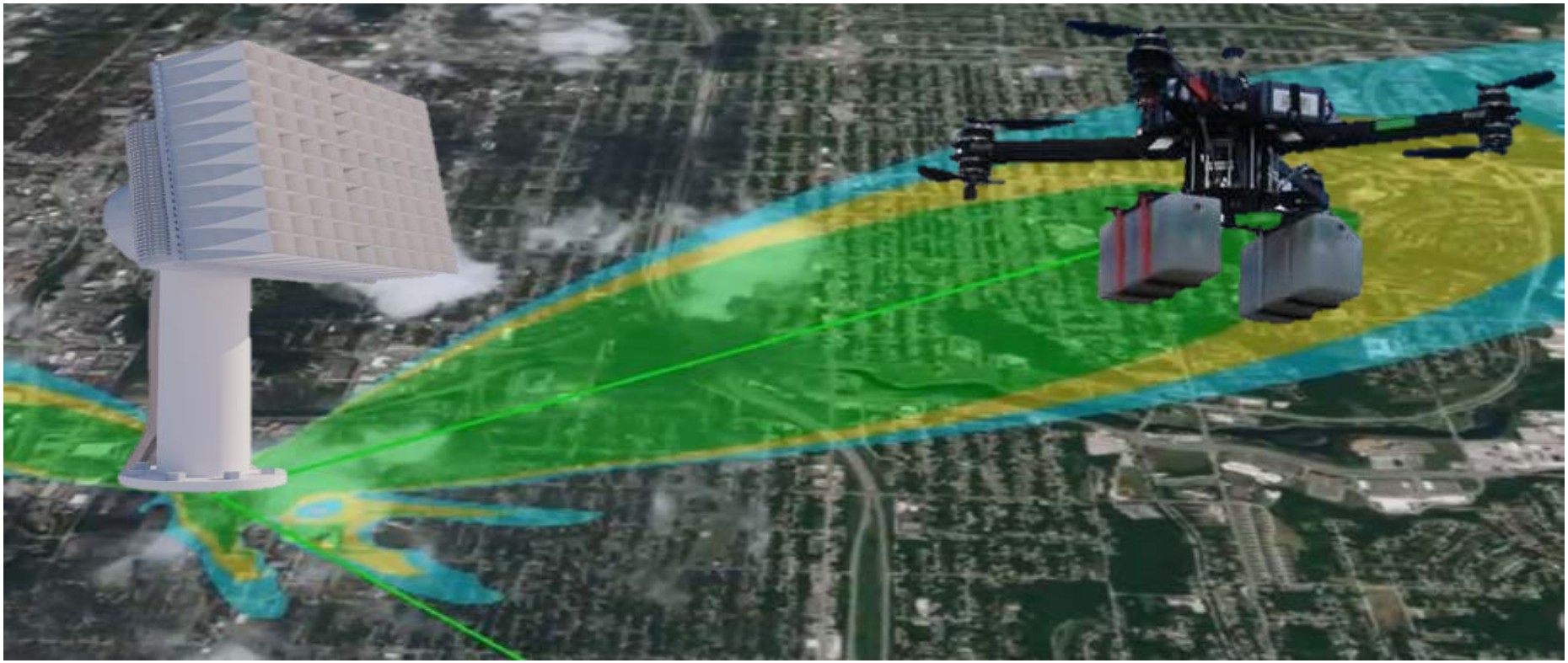
OSPRES-G Overview

M.M. Paquette (all things that went right)
A.N. Caruso (responsible for anything that went wrong)

paquettem@umkc.edu
carusoan@umkc.edu

DISTRIBUTION STATEMENT A: Distribution authorized to all OSPRES Grant and Contract performers, and any uncompensated OSPRES collaborators. Further dissemination per the Office of Naval Research, Ryan Hoffman (ryan.b.hoffman.civ@us.navy.mil, 703-696-3873) or higher DoD authority.

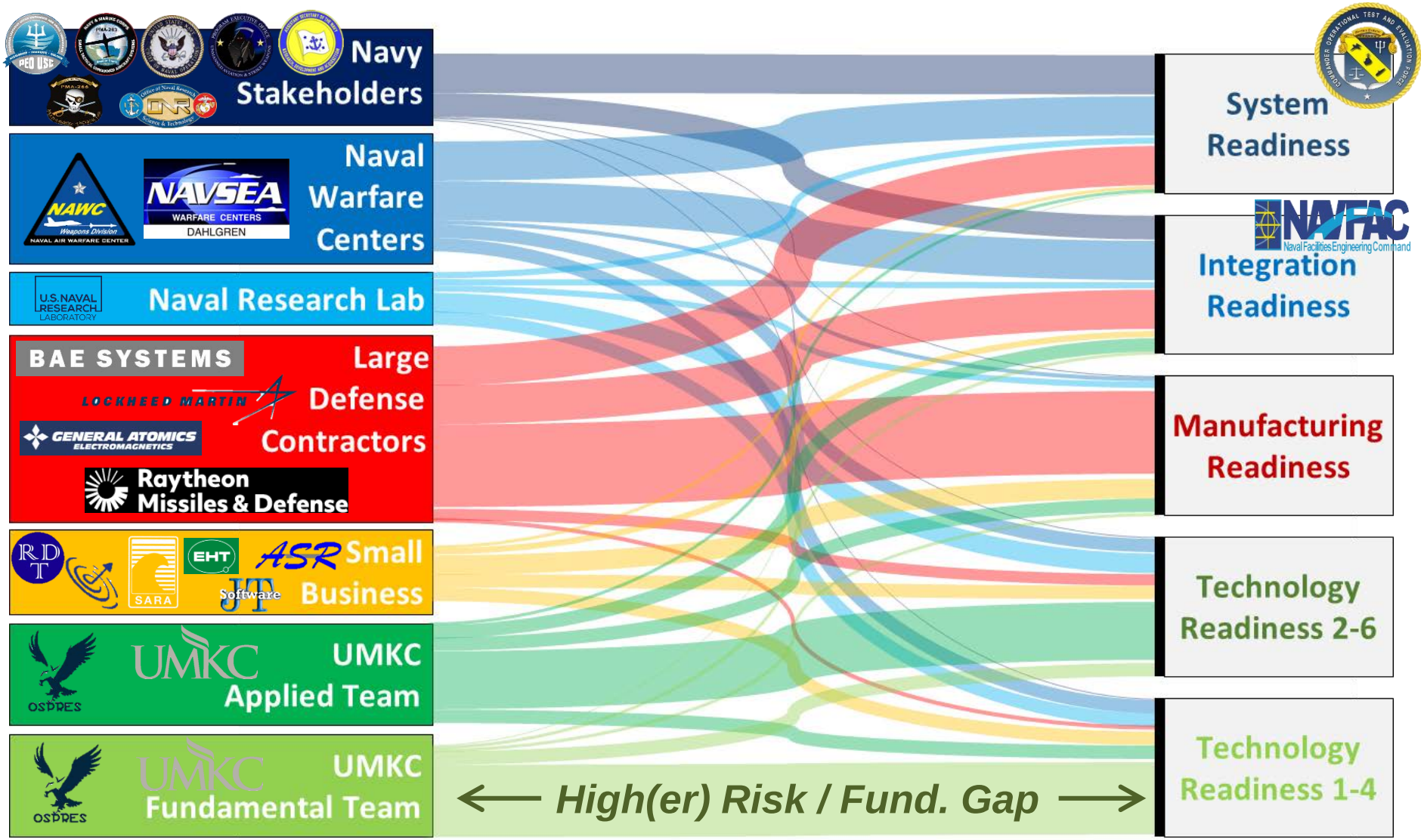
OSPRES Mission/Objective



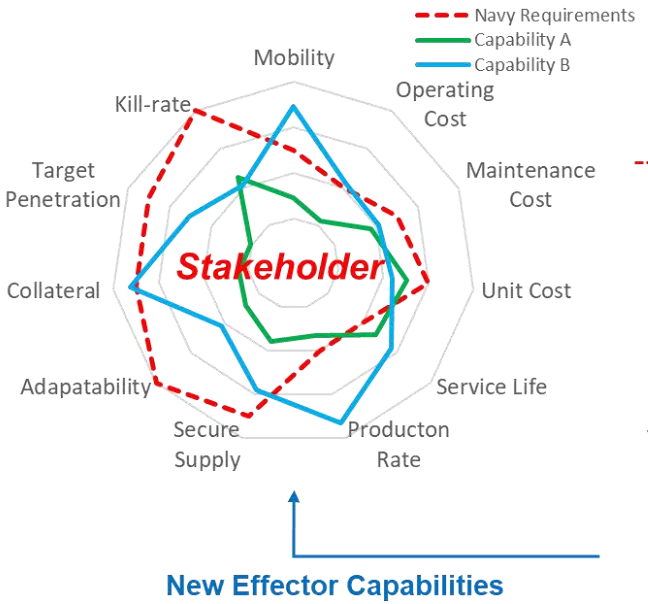
HPM-based Counter-sUAS Development (↓TRL ↑ Innovation)

→ Develop, downselect and predict effects of high power microwave drivers and electronically steerable compact radiators whose waveform(s) capacity, enable level 4/5 lethality on sUAS with the least power density and highest reasonable efficiency.

OSPRES-G/C Swim Lane

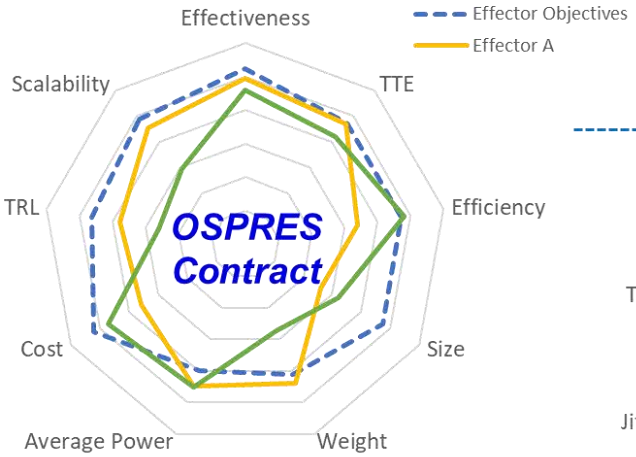


Roles & Requirements



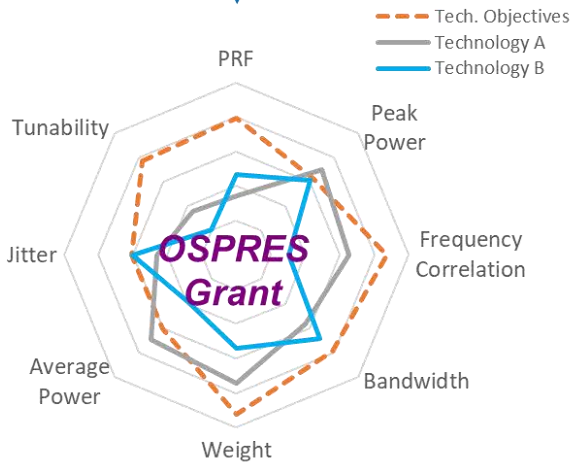
New Effector Capabilities

Navy Capability Gaps



New Tech. Capabilities

Effector Capability Gaps

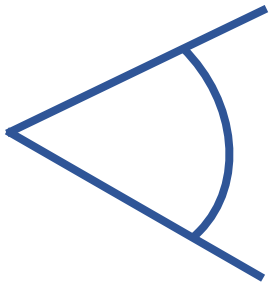


OSPRES Grant:
UAS-HPM fundamental, high(er)-risk, enabling technology development that can be transitioned to the OSPRES Contract.

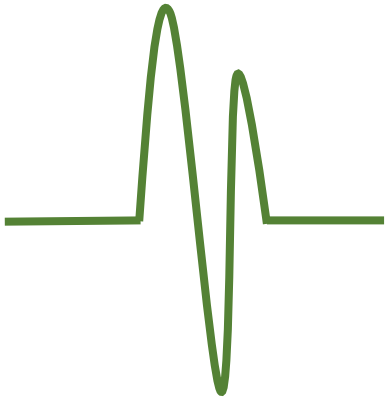
OSPRES Contract:
UAS-HPM pragmatic, effects-driven effector development that can be transitioned to fulfill Navy capability gaps

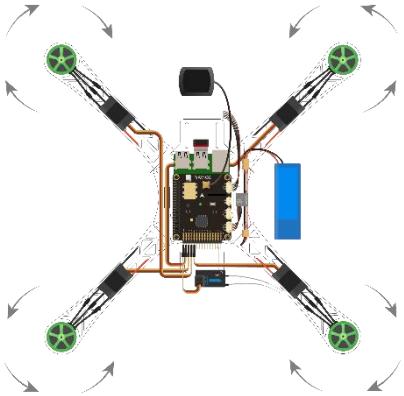
OSPRES Original Pillars

Identify

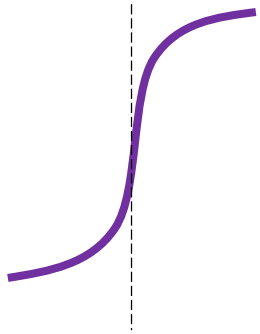


Generate/Couple Microwave





Assess

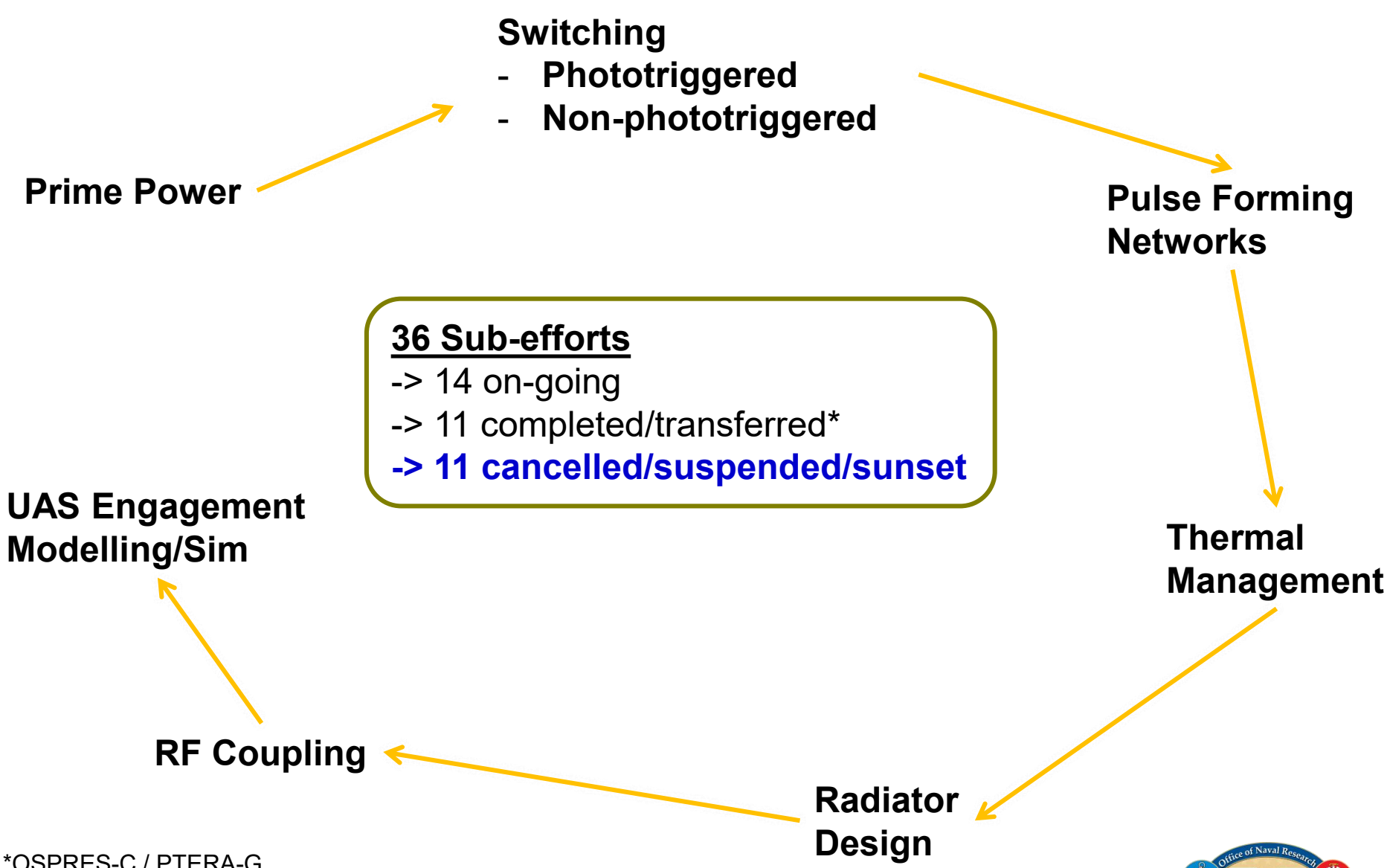


Deep Learning Alg.
Training Set Dev.
Advanced Environ.

Pulse Power Formation
High Voltage Switching
Advanced Materials
Triggering
Antenna Design

Diagnostics
Adv. Design of Expt.
Simulation
Phen. Theory Dev.

OSPRES-G Final Pillars



*OSPRES-C / PTERA-G

Example Questions / Problems / Challenges

Can the $1/r^2$ limit be overcome in the far field?

How to beat the *electrically small antenna* limit?

For P_{peak}>GW, how far can the RF perf parameters be tuned?

Does *learning-based* optimization work in RF design?

What are the theoretical/practical conversion Efficiencies, tunability and SWAP limits of NLTLs?

Can general rules be developed for RF coupling/disruption on classes of electronics?

What are ideal test matrices for multi-dim and stoichastic mechanism(s) of action?

Mechanisms-Strategy

Technical Approach(es) to:

Electronic Steering: control inter-element interaction / ↓ cascaded jitter

Tunable Waveforms: $\Delta L_{parasitic}$, $\Delta L_{element}$, $\Delta C_{element}$, $X_{dynamic}$

Inter-element Time Comp.: seed laser gain control, negative feedback / temp comp

Areal Heat Transfer: jet impingement and other turbulent flow considerations

UHF Aperture Area: electrically small tradespace eval, D/Q (directivity/qual-fact) ratio

System Volume: direct microwave modulation, non-phototriggered pulsers

1064-nm Laser SWaP-C: fiber laser, multi-stage optical amplifier

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Management Approach (Ideal):

Fail Fast -> high/med-risk milestone-gates, sunset or transition and move to next*

*unless on PhD track

OSPRES Sub-Effort Examples

On-going Sub-System Projects

- High-Average Power Fiber Laser ● ‡
- Multi-stage Optical Amplifier ● ‡
- Engagement Level Model Development ● ● ● ‡
- UHF Arrays: Physical Aperture Area Reduction ● ‡
- HV-Solid State Charging Switch ● ‡
- RF Coupling ● ‡
- Drift Step Recovery Diode Optimization ● ‡
- Impulse Radiating Antenna Design ●
- Direct RF Modulation via UWBG-PCSS ● ‡
- Diode-based NLTL for f_c>400-MHz ● ‡

Sunset Projects

- Positive Feedback-NLTL ● ‡
- Minimally Dispersive Waves ●
- Multi-ferroic-NLTL ● ●
- *Ab Initio* → TCAD ‡
- Avalanche-based PCSS ●
- Gyromagnetic-NLTL ●
- Super Resolution from Deep Learning ●
- Multi-stage BPFTL ●

Completed Projects

- PCSS Top Contact Optimization ●
- Non-perturbing UAV Diagnostics ● ‡
- Noise Injection as HPM Surrogate ● ‡
- SiC:N,V Properties (w/ LLNL) ● ‡
- Adaptive Design-of-Experiments ● ‡

System-level Relationship

- ● Source Scalability/Modularity/SWaP-C^2
- ● Waveform Tunability
- ● Effects Prediction
- ‡ MS/PhD Project

Ab Initio Informed TCAD

Multi-Physics (soup-to-nuts) prediction of semiconductor switch forward behavior

***Ab Initio* Calculations**
-> First-principles electronic structure

↓

TCAD (Technology Computer-Aided Design)
-> M&S development/optimization of semiconductor process tech/devices

↓

SPICE (Technology Computer-Aided Design)
-> M&S development/optimization of semiconductor process tech/devices

↓

Full Wave EM Solver
-> Integral Equations – Method of Moments, Finite Elements, Finite Differences in Time Domain, Finite Integration Technique)

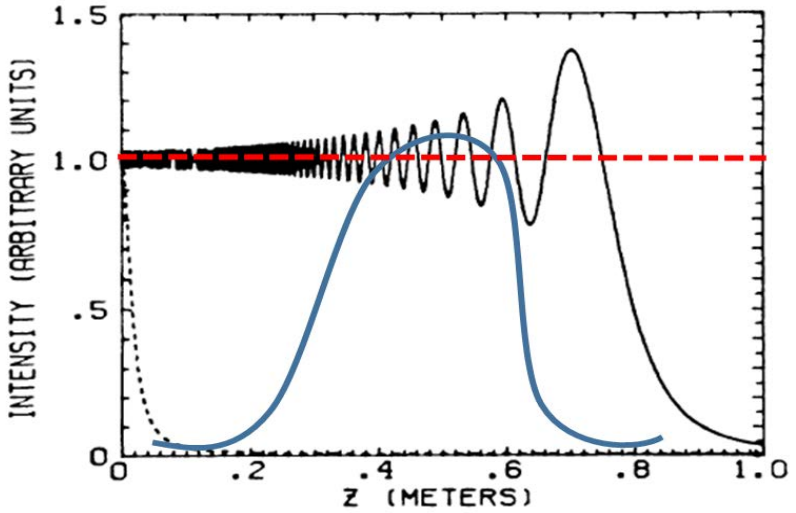
https://www.synopsys.com/silicon/tcad.html
https://silvaco.com/tcad/
https://www.comsol.com/semiconductor-module

Minimally Dispersive Waves

Waves whose propagation distance exceeds the Rayleigh distance:

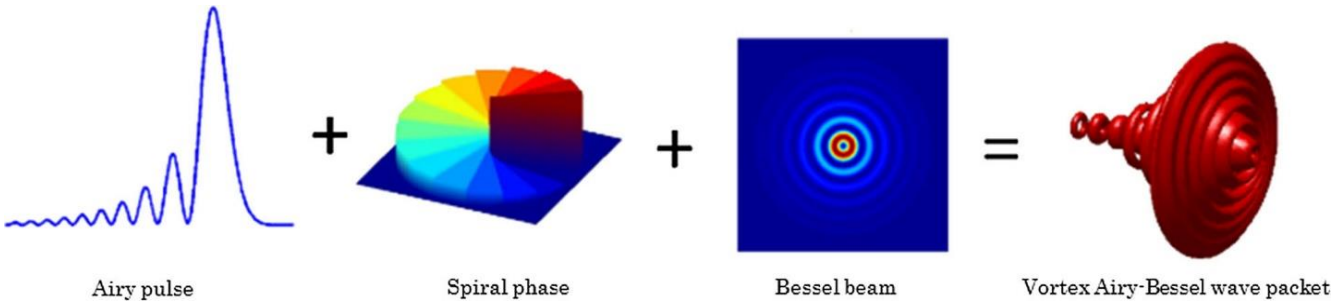
$$Z_R = \frac{\pi r_o^2}{\lambda}$$

Leverage advances in simulation, materials, corrective optics, and functionals to find, design and demonstrate the largest possible Z.



Phys. Rev. Lett. **58** (1987) 1499

Diffraction and dispersion free propagation

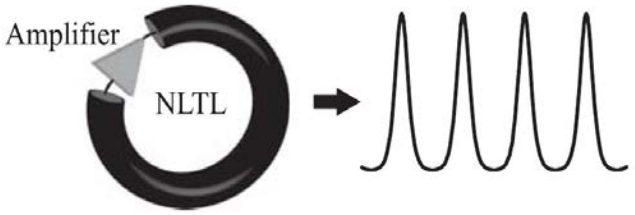


Chinese Optics Lett. **15** (2017) 030009

Nature: Light **10** (2021) 160

Non-Linear Transmission Line Variants

Positive Feedback



Attribute: Real time control of waveform through amplifier tuning from a small solid state package (stable soliton stream).

Goal: Scale 10-kW to 200-kW.

IEEE Trans. Micro. Theory Tech. **54** (2006) 373

Gyromagnetic Pulse Width Enhancement

$$\tau = \frac{1}{\gamma \Delta H}$$

Ferrimagnetic relaxation time

Resonance line width

Gyromagnetic ratio (fixed)

From 5- to 500-ns w/ single crystal YIG

Multiferroic-based Tunability

LLG equation

$$\frac{\partial \boldsymbol{M}}{\partial t} = -\gamma(\boldsymbol{M} \times \boldsymbol{H}_{eff}) + \frac{\alpha}{M_s}\left(\boldsymbol{M} \times \frac{\partial \boldsymbol{M}}{\partial t}\right)$$

Precession term: Determines ω of RF generated

Damping term: Determines pulse length and the lowest possible ω

***For a FM/FE heterostructure:**

$\gamma \rightarrow \frac{\gamma}{1+\beta}$ $\quad \alpha \rightarrow \frac{\alpha+\xi\beta}{1+\beta}$

where β is electrically tunable

***Electrically* tune:**

- Center frequency
- Lowest obtainable ω
- Pulse length

Funding Forward Recommendations

OSPRES sunset/unfinished/seed efforts could mean a boon for others to launch from

→ ONR/AFOSR/ARO – 6.1/6.2 Grant, SBIR/STTR, MURI
→ NRL/AFRL/ARL: partnership (CRADA) w/ one/more investigators
→ Prime Industry: in-house (IR&D) concept realization/improvement

---

HV Switch: a US solution is needed outside BEHLKE; treat as essential DoD device

Fiber Laser: realize/demonstrate/prove hollow fiber concept (National Lab proveout)

Patch Antenna Array: adapt concepts learned for commercial comms (SB transition)

D-NLTL: SWaP and real-time tunability enable small airborne applications (PC alt)

Coaxial Ringdown Oscillator (CRO): lots of design/improvement space (SB transition)

MDW: no vacations at Northwest Polytechnic; akin to QIST/AI (ripe for MURI)

RF Coupling & Effects: Bob Gardner (GTRI), NSWC-DD, DA-WARDEN (need capture)

Quantitative Program Output*

Students supported/graduated:

15 BS
12 MS
7 PhD
15 in-progress

Participants:

8 SB (2 VOSB)
5 DoD Labs
2 NNSA Labs
1 DoD CTR

Intellectual property base contributions:

13 published journal papers
5 journal papers submitted
7+ journal papers in-preparation
46 conference papers
55 conference presentations
10 theses/dissertations
12 IP disclosures
4 provisional patents
2 non-provisional patents
1 allowed/issued patent

Events/Fires:

Coastal Trident (2018 – 2022)
10+ Live Fire (SPDE)
25k+ Effects Studies

*OSPRES-G/OSPRES-C combined

Journal Publications

1. M. Z. M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Electromagnetic Compatibility Analysis of Quadcopter UAVs Using the Equivalent Circuit Approach," *IEEE Open Journal of Antennas and Propagation*, vol. 3, pp. 1090-1101, **Sept 2022** [doi].

2. M. Z. M. Hamdalla, J. M. Roacho-Valles, A. Caruso, and A. M. Hassan, "Electromagnetic Compatibility Study of Quadcopter UAVs: Characteristic Mode Analysis of the Frame's Material and Shape Effect," *Progress In Electromagnetics Research M*, Vol. 112, 1-14, **2022** [doi].

3. K. Alsultan, M. Z. M. Hamdalla, S. Dey, P. Rao, and A. M. Hassan, "Scalable and Fast Characteristic Mode Analysis Using GPUs," *Applied Computational Electromagnetics Society Journal (ACES)*, vol. 37, no. 2, pp. 156-167, **July 2022** [doi].

4. N. Gardner, K. C. Durbhakula, and A. N. Caruso, “Design Considerations for Diode-Based Nonlinear Transmission Lines,” *AIP Advances*, 12, 055012, **May 2022** [doi].

5. B. K. Lau, M. Capek and A. M. Hassan, "Characteristic Modes: Progress, overview, and emerging topics," *IEEE Antennas and Propagation Magazine*, vol. 64, no. 2, pp. 14-22, **April 2022**.

6. J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation,” *International Journal of Thermal Sciences*, 172, 107254, **Feb 2022** [doi].

7. M. Z. M. Hamdalla, B. Bissen, J. Hunter, Y. Liu, V. Khilkevich, D. G. Beetner, A. N. Caruso, and A. M. Hassan, “Characteristic Mode Analysis Prediction and Guidance of Electromagnetic Coupling Measurements to a UAV Model,” *IEEE Access*, 10, 914–925, **Dec 2021** [doi].

8. W. Azad, F. Khan, and A. N. Caruso, “A Medium Power, Self-Sustaining, Configurable RF Pulse Generation Circuit Using a Nonlinear Transmission Line and Power Amplifier in a Closed Loop Configuration, *IEEE Transactions on Plasma Science*, vol. 49, no. 7, pp. 2183–2194, **July 2021** [doi].

9. S. Roy, W. Azad, S. Baidya and F. Khan, “A Comprehensive Review on Rectifiers, Linear Regulators and Switched-Mode Power Processing Techniques for Biomedical Sensors and Implants utilizing In-body Energy Harvesting and External Power Delivery,” *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 12721–12745, **Nov 2021** [doi].

10. P. Klappa and T. D. Fields, “Impact of High Powered Microwave-based Sensor and Actuator-level Disruptions on Unmanned Aerial Vehicle Performance,” *Journal of Defense Research and Engineering*, Volume 2, Issue 2, **June 2021**.

11. M. Hamdalla, A. N. Caruso, and A. M. Hassan, "Predicting Electromagnetic Interference to a Terminated Wire Using Characteristic Mode Analysis," *Applied Computational Electromagnetics Society Journal (ACES)*, Vol. 35, No. 11, pp. 1318-1319, **Nov 2020**.

12. N. J. Kramer, L. F. Voss, A. M. Conway, P. V. Grivickas, M. Bora, D. L. Hall, and A. N. Caruso, “Extrinsic Absorption Pathways in Vanadium-Doped SiC Measured Using a Total Internal Reflection Geometry,” *Physica Status Solidi A*, 217, 20000315, **Aug 2020** [doi].

13. K. C. Durbhakula, D. Chatterjee, and A. M. Hassan, “An Efficient Algorithm for Locating TE and TM Poles for a Class of Multiscale Inhomogeneous Media Problems,” *IEEE Journal on Multiscale and Multiphysics Computational Techniques*, vol. 4, no. 1, pp. 364–373, **Dec 2019** [doi].

Intellectual Property

IP Disclosures

D. Beetner, V. Khilkevich, A. Hassan, S. Xia, J. Hunter, A. Harmon, “Rapid Prediction of Electromagnetic Coupling to Electronic Circuits and Harnesses,” 2022.

S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” 12AUG2021.

S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same,” 28JUNE2021.

Bhamidipati, Myers, Caruso, “Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources,” 21UMK009, 04NOV2020.

Shepard, “A Low Noise Optical Amplifier,” 21UMK007, 14SEPT2020.

Eifler, “Photoconductive Contact Pattern for Enhanced Charge Collection,” 08JUL2020.

Shepard, “A Novel Optical Fiber Amplifier,” 20UMK012, 02JUN2020.

Doynov, “High-power High Repetition Rate Microwaves Generation with Differentially Driven Antenna,” 20UMK011, 19APR2020.

Doynov, “Scalable Modular System for High-power Microwaves Generation,” 20UMK010, 19APR2020.

Doynov, “Pulse Differential High-power Microwave Generation,” 19UMK007, 02JAN2019.

Doynov, “Non-linear Network Topologies with Reutilized DC and Low-frequency Signal,” 19UMK008, 28DEC2018.

Doynov, Caruso, “Non-Linear Transmission Line Topologies for Improved Output,” 19UMK005, 28SEPT2018

Provisional Patents

S. Bellinger, A. Caruso, A. Usenko, US Provisional Patent Application “Stacked Diode with Side Passivation and Method of Making the Same,” filed 09/10/2021.

S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same” US Provisional Patent Application 63/216,550, filed 06/30/2021.

P. Doynov, A. Caruso, “High-Efficiency High-Power Microwave Generation using Multipass Non-Linear Network Topologies,” filed 11/26/2019.

Plamen Doynov, James Prager, Tim Ziemba, Anthony N. Caruso, “Non-Linear Transmission Line Topologies for Improved Output”, USPTO Provisional Serial No. 62/737,185, filed 09/272018.

Non-Provisional Patents

S. Bellinger, A. Caruso, A. Usenko, “Stacked Diode with Side Passivation and Method of Making the Same,” US Patent Application 17/946,022, filed 09/15/2022.

S. Bellinger, A. Caruso, A. Usenko, “Diode and Method of Making the Same” US Patent Application 17/855,735, filed 06/30/2022.

Allowed/Issued Patents

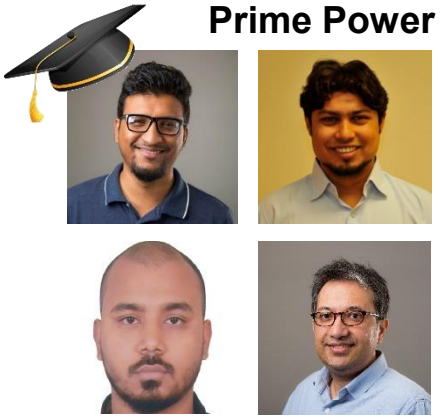
P. Doynov, A. Caruso, “Multi-Pass Nonlinear Network for Microwave Generation” US Patent Application 17/455,026, filed 11/16/2021 (Allowed 10/13/2022).

Students Graduated/Transitioned to Workforce

Name	Degree	Last Known
Al-Shaikhli, Waleed	MS Spring 20	Genuen, KS; Cognitive Copper, KS
Alsultan, Khulud	PhD Spring 21	King Saud University, Saudi Arabia
Azad, Wasekul	PhD Summer 21	Applied Materials, Sunnyvale, CA
Berg, Jordan	MS Spring 21	MRI Global, MO
Bhamidipati, John	PhD Spring 22	Intel, NM
Bissen, Bear	MS Spring 19	Capella Space, San Francisco, CA
Bozarth, Ethan	BS 21	
Brasel, Sadie	BS Spring 21	Graduate Student, Rice University, TX
Clark, Justin	BS 22	MRI Global, MO
Dowell, Alexander	BS Spring 22	Graduate Student, UMKC
Fazekas, Max	MS Summer 21	
Floyd, Dennis	BS	Naval Air Warfare Center Weapons Division
Fry, Spencer	BS Spring 2021	Garmin, KS
Hamdalla, Mohamed	PhD Fall 21	MIDE, MO
Hanif, Abu	PhD Spring 21	Intel Corporation, OR
Harmon, Aaron	BS 18	PhD Student, Missouri Univ. of Science & Tech.
Harp, Joshua	MS 19	Small Business
Hauptman, Cash	BS Spring 18	University of Nebraska-Lincoln
Herrington Shawn	PhD Summer 21	Honeywell Aerospace, NM
Karnes, Simeon	BS Spring 21	Graduate Student, UMKC
Klappa, Paul	MS Spring 21	Sierra Nevada Corporation, NV
Kovarik, James	MS Spring 21	
Kramer, Noah	MS Spring 19	MIDE, MO
Labrada, Dario	BS Spring 20	Honeywell Aerospace, FL
Lancaster, John	MS Spring 17	Lawrence Livermore National Laboratory, CA
Landwehr, Colby	BS Fall 21	Burns & McDonnell
Reed, Demetri	BS Spring 22	Evergy, MO
Renzelman, Jeff	MS Spring 18	Sensata Technologies, MA
Roy, Sourov	PhD Spring 21	BTCPower, Orange County, CA
Smith, Cody	BS 20, MS 21	Winchester Ammunition, MO
Thompson, Heather	MS 20	University of Missouri-Kansas City, MO
Wagner, Adam	MS Fall 20	Los Alamos National Laboratory, NM
Utt, Anthony	BS	
Xia, Shengxuan	BS	PhD Student, Missouri Univ. of Science & Tech.

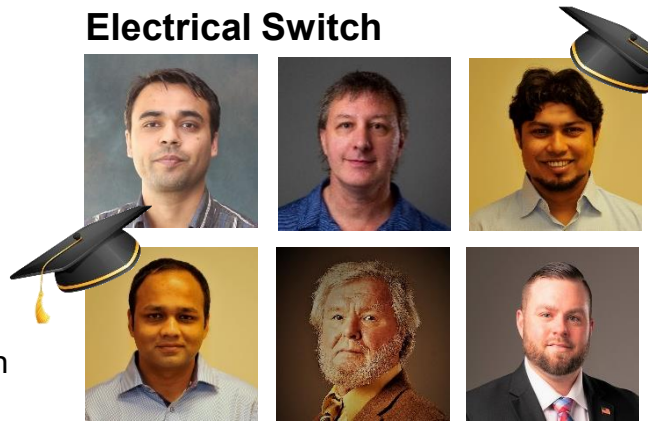
Contributors (OSPRES-G)

Prime Power



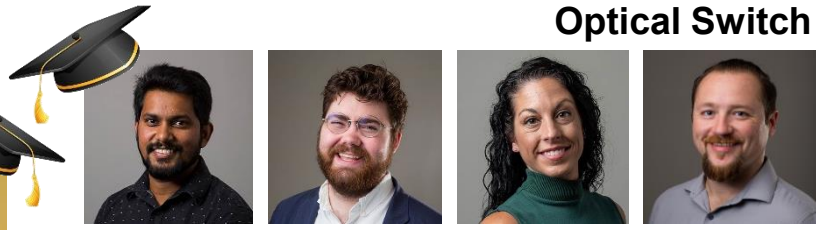
Azad, Hanif, Sarwar, Khan

Electrical Switch



Bhattarai, Bellinger, Eifler, Hanif, Hyde, Noor, Roy, Usenko, Allen

Optical Switch



Bhamidipati, Eifler, Kramer, Labrada, Rulis, Thompson, Utt, Myers

Optical Source



Shepard

Pulse-Forming Network



Bhamidipati, Berber, Doynov, Gardner

RF Coupling



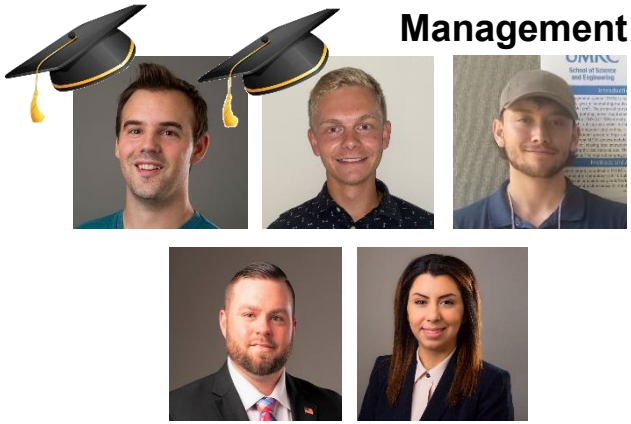
Al-Shaikhli, Alsultan, Hamdalla, Hassan

UAS Engagement Modeling & Sim



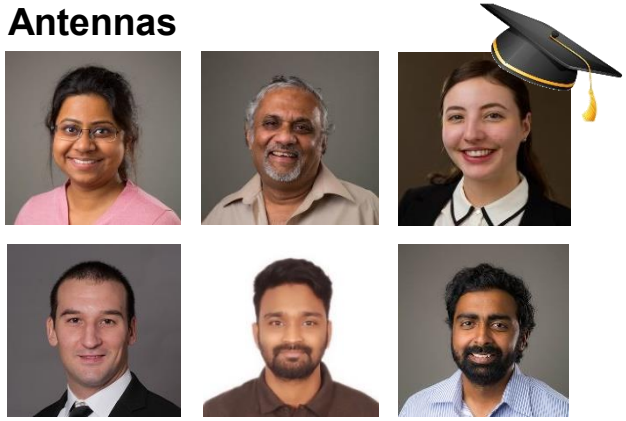
Herrington, Karnes, Klappa, Petersen, Smith, Fields

Thermal Management



Berg, Clark, Sisk, Allen, Sobhansarbandi

Antennas

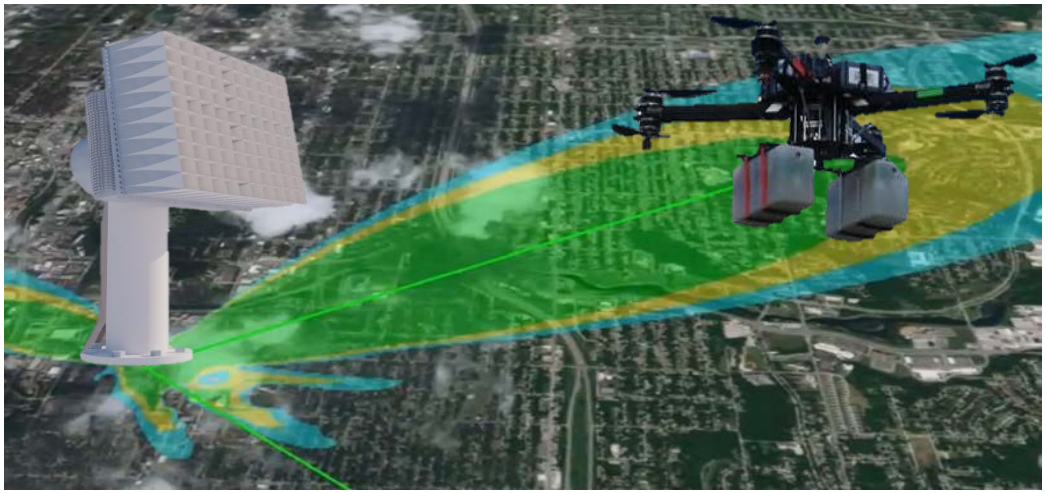


Al-Shaikhli, Barman, Chatterjee, Brasel, Dowell, Indharapu, Durbhakula

Agenda – OSPRES-G Session

1230-1300	Lunch
1300-1320	OSPRES Grant Motivation and Overview (Caruso, Paquette)
1320-1350	Sub-ns Pulse Generation Using Drift-Step Recovery Diodes (Bhattarai, Eifler)
1350-1420	Solid-State Switch and Diode Devices (Bellinger)
1420-1450	Novel Process Flow for Manufacturing of Drift Step Recovery Diodes (Usenko)
1450-1505	Break
1505-1535	Design Considerations for Photoconductive Semiconductor Switches (PCSS) (Bhamidipati, Eifler)
1535-1555	Diode-Based Nonlinear Transmission Lines for Ultra-High Frequency Generation (Video) (Gardner)
1555-1635	UWB Antenna Tradespace Analysis Outcome with Emphasis on Futuristic Design Methodologies (Durbhakula, Barman)
1635-1655	Optical Fiber Lasers and Amplifiers (Shepard)
1655-1715	Design and Development of a Jet Impingement Thermal Management System (Video) (Sobhansarbandi)
1715-1720	Day 1 Closing

Thank you

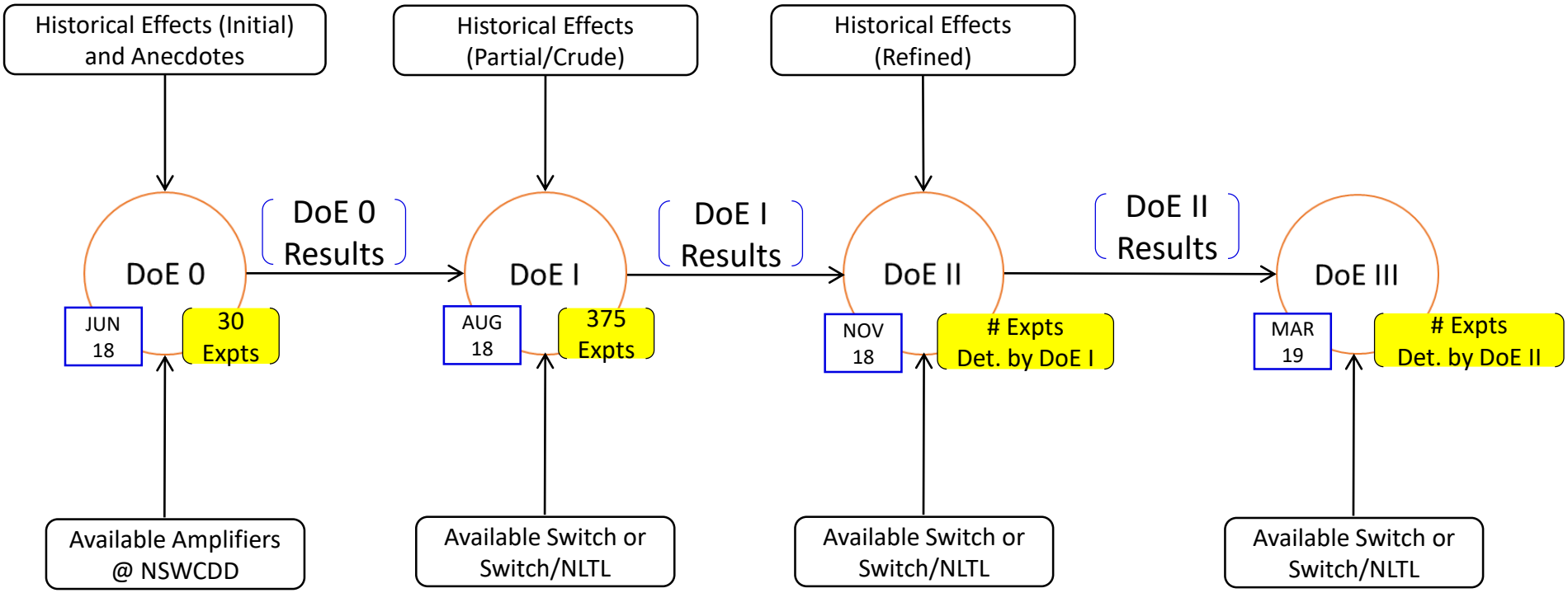


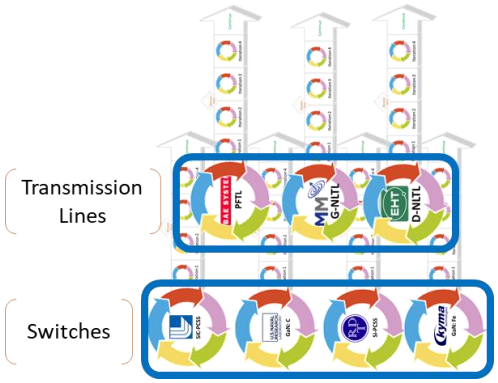
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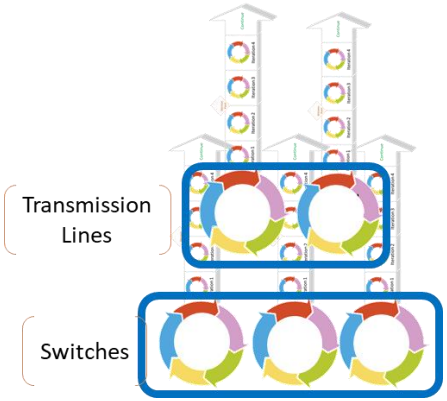


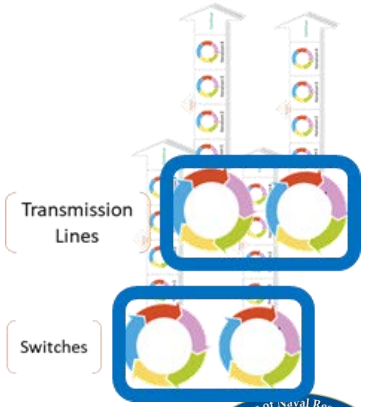
-- Backup Slides --

Adaptive Design of Experiments

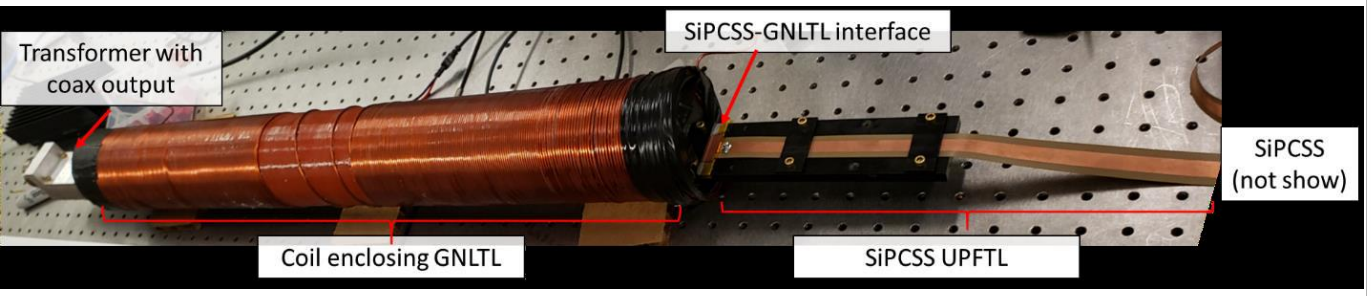


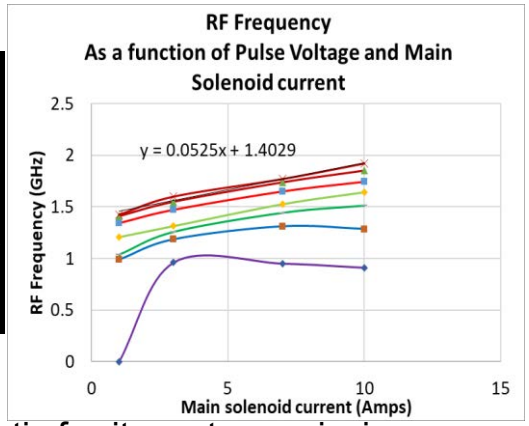


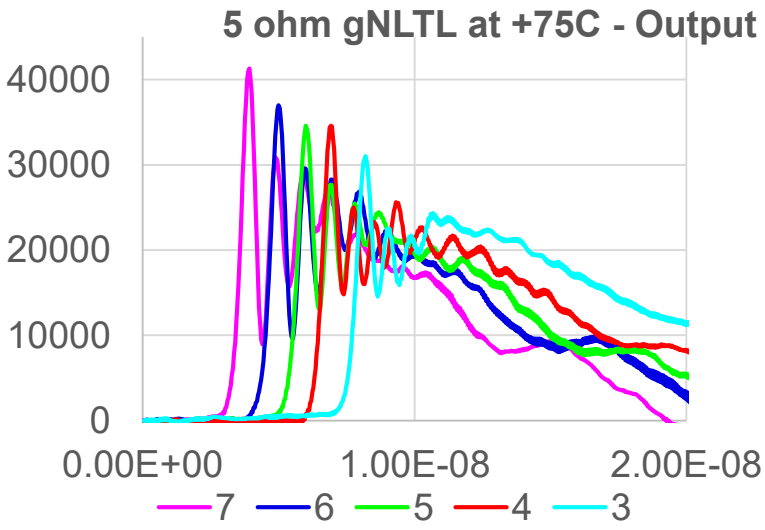




SiPCSS-gNLTL Overview (Metamagnetics)

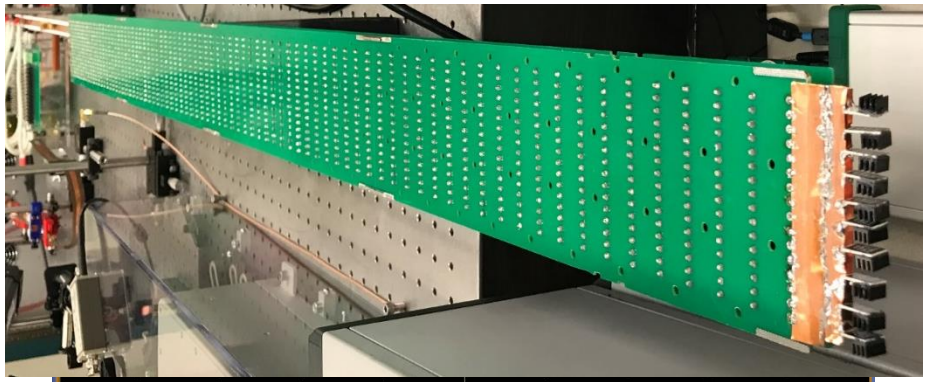


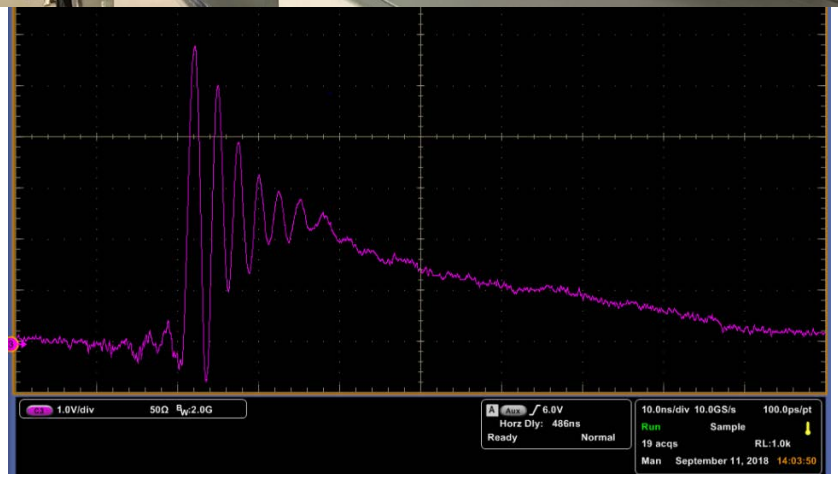




- Exploits non-linear gyromagnetic ferrite as transmission line dielectric
- Processing magnetic moments cause oscillations in transmitted pulse (think push-pull)
- Prototype at UMKC generates damped sine at ~1 GHz
- Tunability via control of solenoid around gNLTL (no tunability demonstrated in 5-Ohm prototype at UMKC)
- Oscillations not present until ~ 1+ kV (200 kW), only a portion of that is RF (i.e., lots of DC which requires rejection in GTEM).
- No cooling design, limited average power

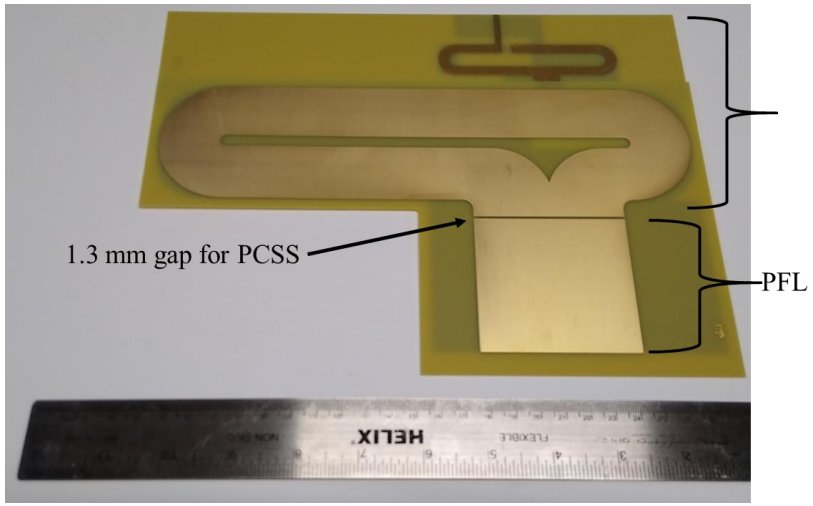
(SiPCSS)-dNLTL Overview

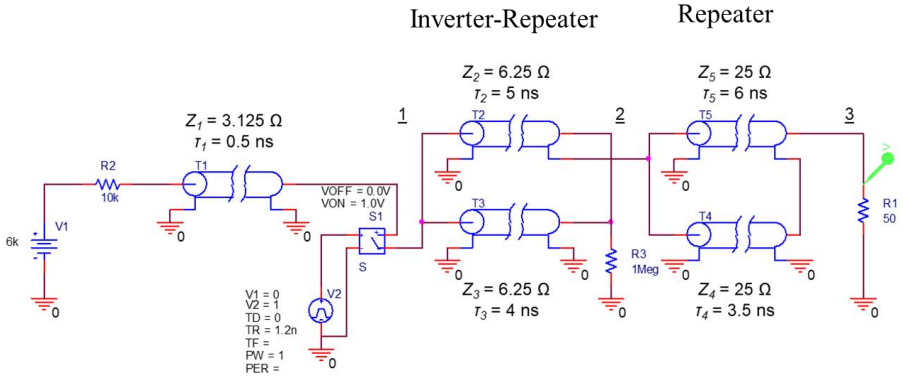




- Exploits non-linear diode capacitance distributed along transmission line
- Discrete elements store/release charge periodically (and nonlinearly) leading to pulse oscillations
- Prototype at UMKC generates damped sine at ~400 MHz
- No known tunability
- Oscillations not present until ~ 6+ kV (200 kW), only a portion of that is RF (i.e., lots of DC which requires rejection in GTEM).
- Driving with SiPCSS has been unsuccessful so far (pulse reflected off input)
- We have inductive adder designed to drive dNLTL (will produce waveform shown on left)

SiPCSS-PIRFO (NanoEM) Overview

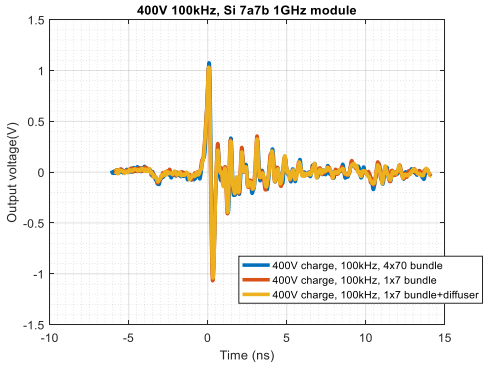


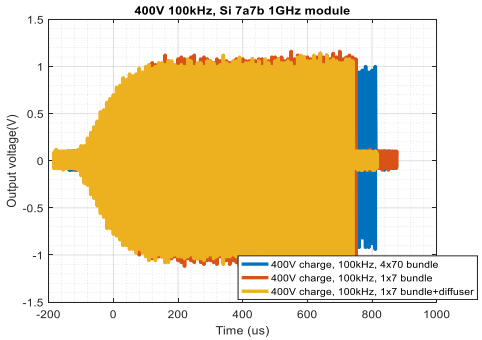


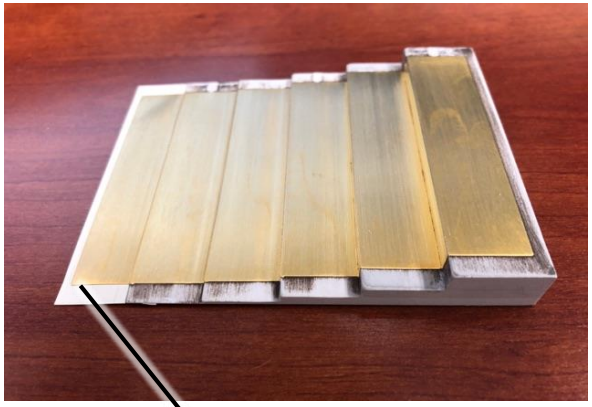
Pulse-input RF-output (PIRFO)

- Linear pulse forming transmission line
- Exploits impedance and propagation time mismatch to form pseudo-arbitrary waveforms
- Waveform results from hardware design, i.e. one waveform per module
- No evidence thus far for tunability
- Peak powers are roughly 25% of SiPCSS peak due to initial PFN type (generic PFN, could be increased to 100%)
- At extremely high rep rates, (e.g., ~100 MHz), PIRFO could operate at quasi-continuous multi-frequency mode (requires switch capable of rep rate).

SiPCSS-BPFTL Overview

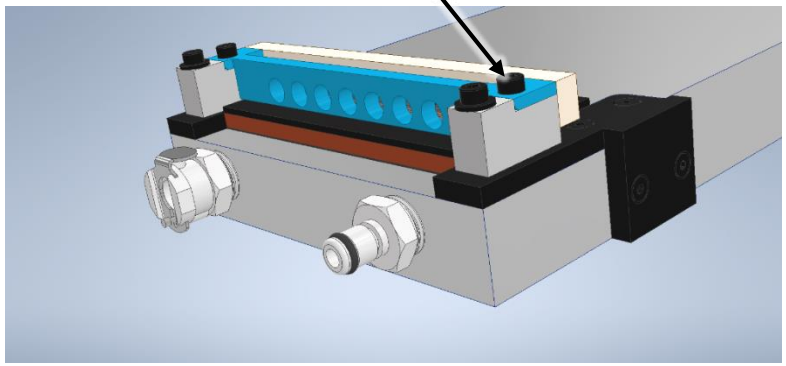




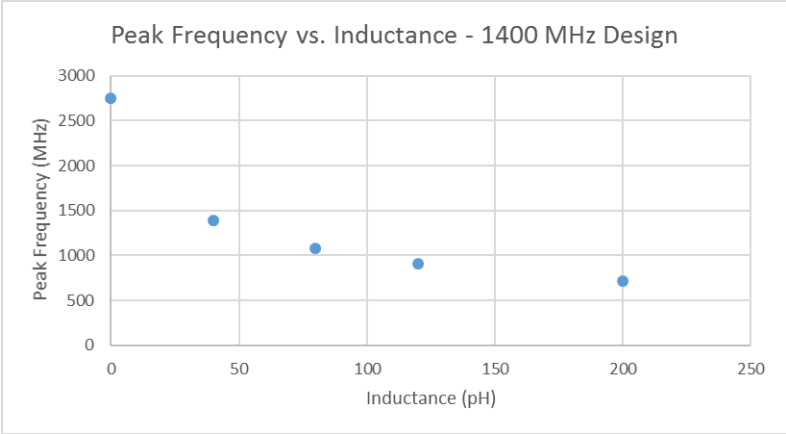


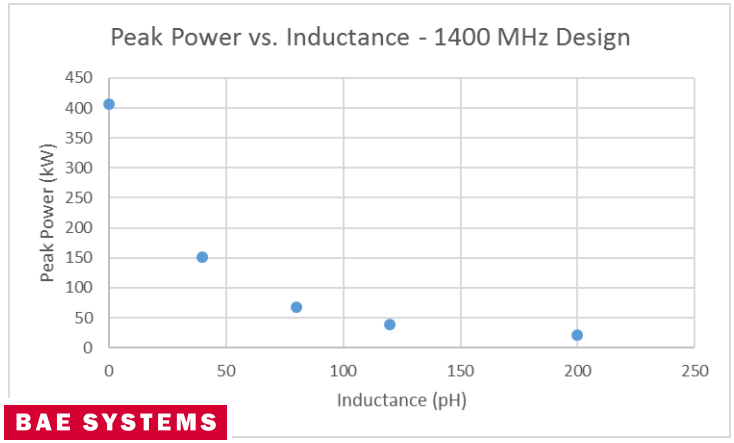
Bipolar pulse-forming transmission line (BPFTL)

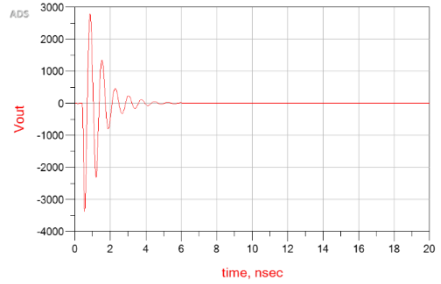
- Linear pulse forming transmission line
- Exploits impedance steps and parasitic or “integration” inductance to convert charge stored to bipolar pulse.
- Transforms impedance (increases)
- 3 prototype modules (700 Mhz, 1.0 GHz, 1.4 GHz)
- designed for same output geometry (easily swapped)
- Tunability achieved by adjusting position of laser on switch (introducing inductance by changing current path through switch)
- BAE has demonstrated up to at least 1.1 Ghz or more
- UMKC has only successfully tested 400 MHz design (limited by measurements and integration scheme)

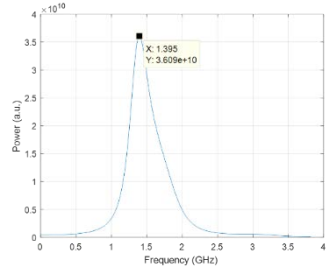


1.4GHz SiPCSS BPFTL Tunability

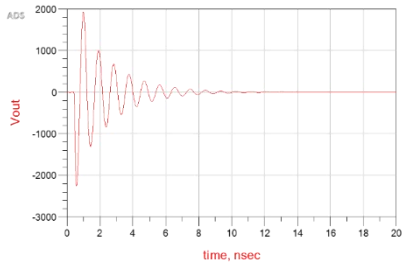


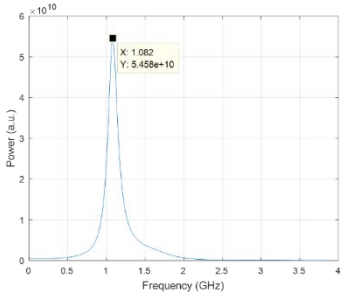




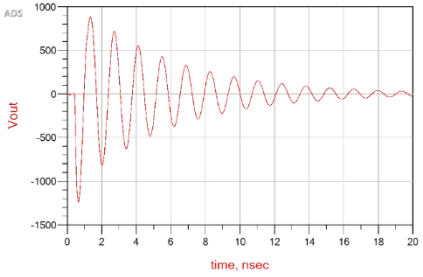


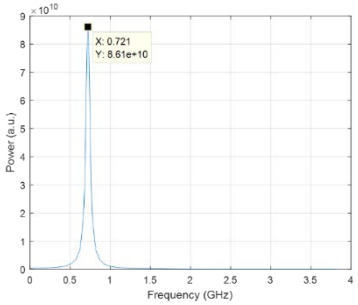
f_c ~ 1.4 GHz
$P_{relative}$ ~ 1
BW ~ 500 MHz
$f_{max,3dB}$ ~ 1.7 GHz





f_c ~ 1.1 GHz
$P_{relative}$ ~ 0.5
BW ~ 175 MHz
$f_{max,3dB}$ ~ 1.2 GHz





f_c ~ 700 MHz
$P_{relative}$ ~ 0.1
BW < 100 MHz
$f_{max,3dB}$ ~ 750 MHz

BAE SYSTEMS

OSPRES *Subcontractor* Personnel (FY20)

OSPRES Grant Overview [20]

SARA – Barret Lamb, Robert Koslover, Jonathan Parson, Matt Wisher

RDT – Steve Bellinger

NanoEM – Kevin O'Connor

BAE – McGeehan, Yannick Morel

EHT – Tim Ziemba, James Prager, Ken Miller

ASR – Mike Abdalla, Mike Skipper

Metamagnetics – Anton Geiler, Michael Geiler

John Tiller Software – John Tiller, John Rushing (UAH), John Luginsland (CS)

OSPRES *Govt Partner* Personnel

OSPRES Grant Overview [30+]

ONR – Hoffman, McQuage, Kunapareddy

NSWC-DD – Walker, Chen, Chaparro, Cevallos

NRL – Schumer, Andreadis, Drikas, Croman, Meyerhofer, Dougherty

NSWC-PHD – Jaeger, Went, Went

LLNL – Voss, Conway

USASMDC – Rader, Lai

KC-NSC – Timpson, Byers

AFRL/SDPE/XZIC/RDHPS – Kanistros, Hoff

KC-FBI - Bakken

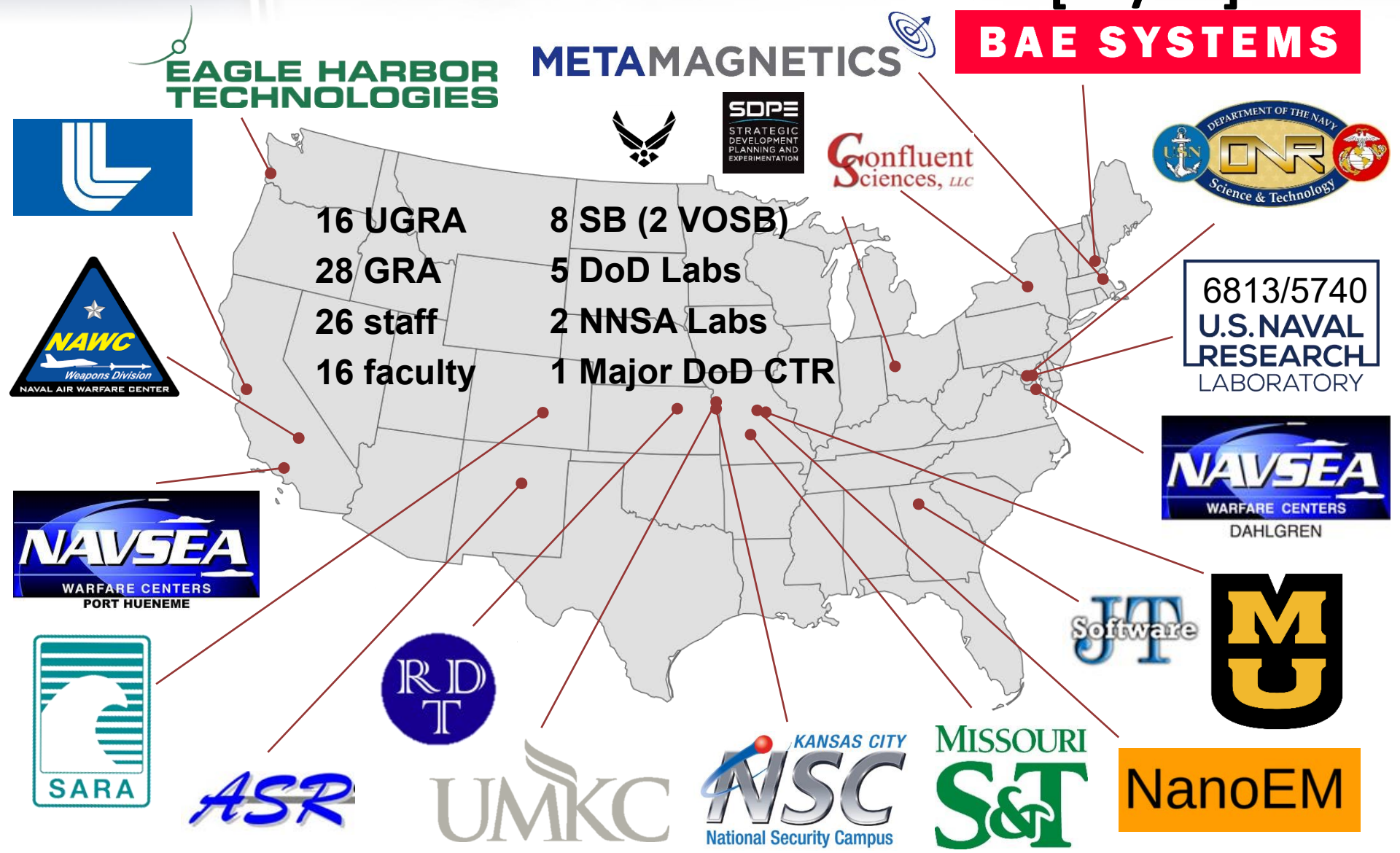
NAWCWD-CL – Higgins

DARPA-TTO – Nichols, Tun, Avicola

MOD-DSTL – Taylor, Hubbard

OSPRES Entities/Personnel (FY20)

OSPRES Grant Overview [14/16]



OPSRES: Gap/Deficiency *HOW*

OSPRES Grant Overview

Future/Needed/Wish-List/Potential Projects

Co-axial Impedance Transformer (5 → 50-Ω)

High gain/power Ultra-low Jitter Seed Laser

Aging of UAV Autopilot Systems and Modules

Avalanche Transistor-based Pulsed Power

Vector Inversion Generators

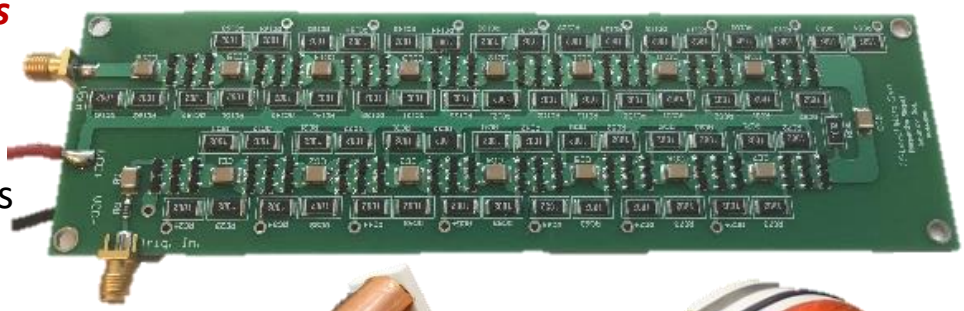
MOSFET-based Pulsed Power

Packaging for Semiconductor-based Pulsed Power

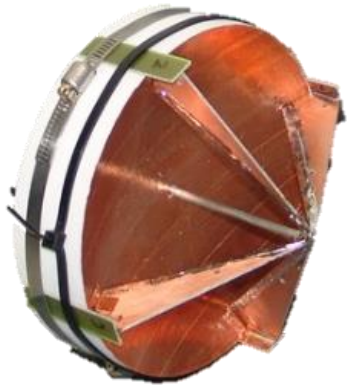
Avalanche Shaping/Sharpening

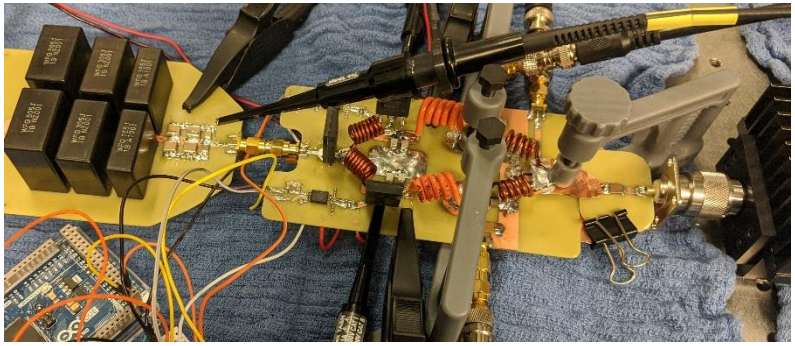
Large DoD Prime / GOV Defined

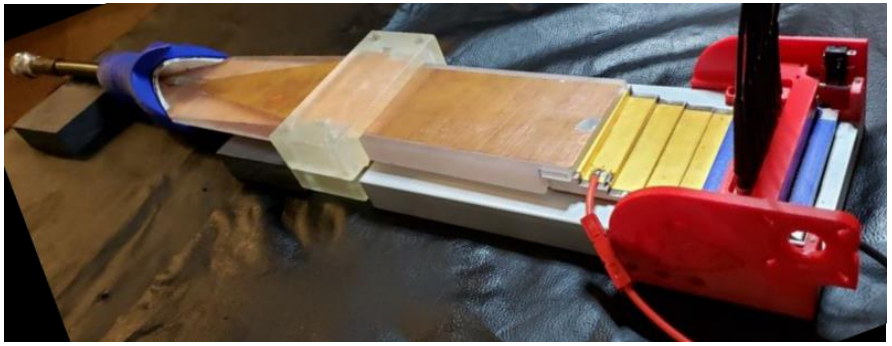
Many more……



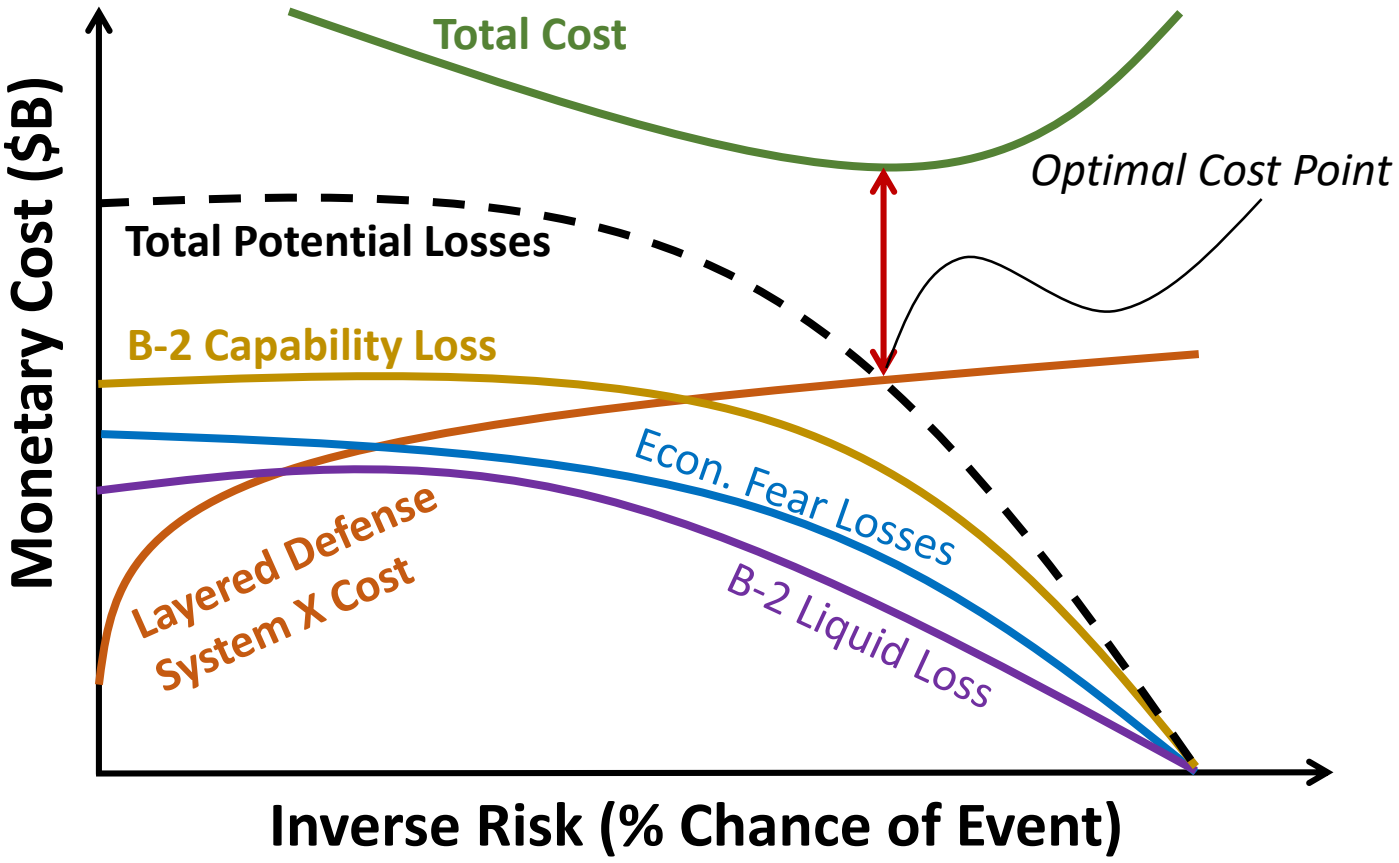








Motivation


Total Cost
Optimal Cost Point
Total Potential Losses
B-2 Capability Loss
Econ. Fear Losses
Layered Defense
System X Cost
B-2 Liquid Loss
Monetary Cost ($B)
Inverse Risk (% Chance of Event)

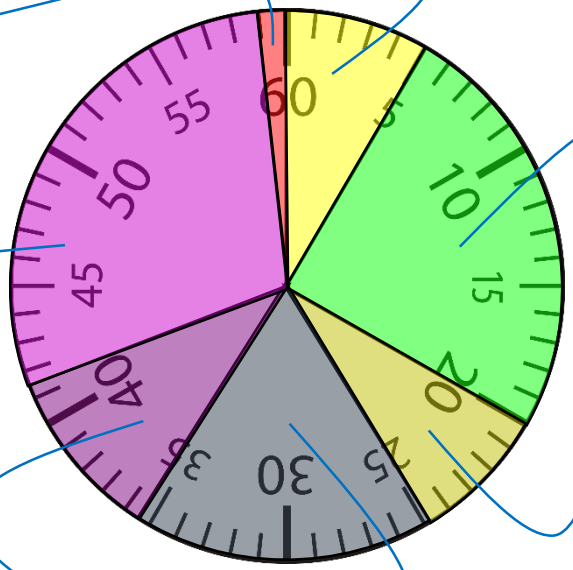
Motivation

Commit Authority Decision Time
[Authorizes Neutralizer Unit to Target/Track]

Time-to-Effect
[Neutralizer Specific]

90 – 120 sec!

Identify Target(s)
[per Approved ID Policy, including Combat ID….friendly, threat, unknown]



Deconfliction/Coordination Time [Coordinate control measures w/ Liaisons and Threats to Friendly Forces]

Engagement Authority Decision Time [Authorizes Neutralizer Unit to Engage]

Targeting Cycle [Synchronize Fires to meet Commanders Effects Objective]

Fires Response Synchronization Time
[Possibly a real-time Mission Level Model Rec.]

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for c-sUAV Study (OSPRES Grant)

N00014-17-1-3016
09/30/2017-09/29/2022

Sub-ns Pulse Generation using Drift-Step Recovery Diodes

Gyanendra Bhattarai, Jay Eifler

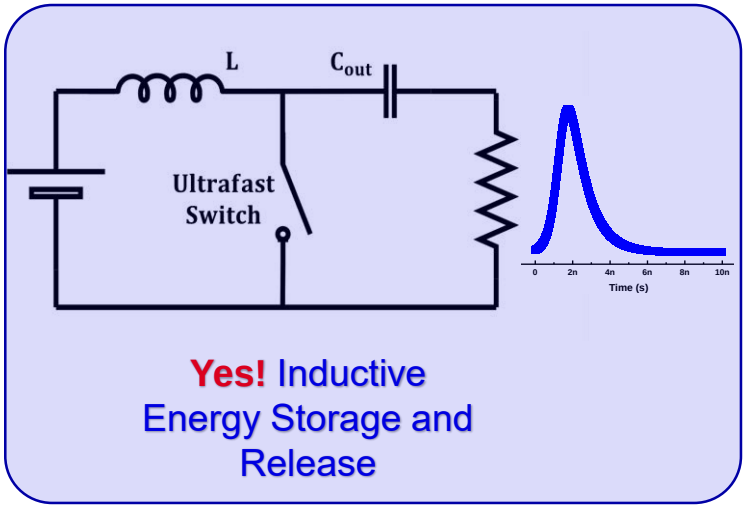
gb5h4@umkc.edu

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Motivation

Ultra-Short Pulse Source

- All-Solid-State
- Nano/Sub-Nanosecond
- High-Voltage
- Non-Optical



Yes! Inductive Energy Storage and Release

Old: Exploding wires
New: Semiconductor

Switch Fabrication

- No COTS fast semiconductor opening switches available in the US.
- Available diodes are made with old (60 years) technology.

Theory and Optimization

- Many circuit topologies exist but not optimized
- No standard circuit working principle/theory
- Very crude optimization scheme (energy, efficiency, PRF)

Objective: Primary

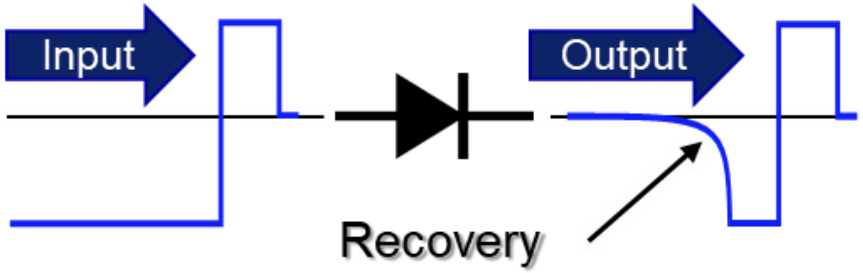
Solid-State Pulse Generator

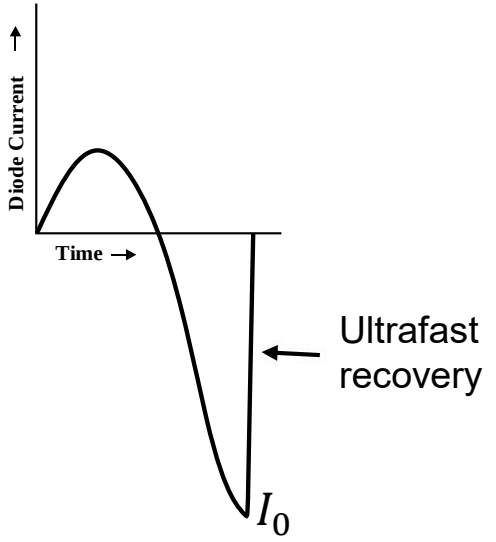
- Achieve
  - Peak Voltage > 10 kV
  - Risetime <1 ns
  - PRF ~100 kHz
  - Volume < 1 liter

Fundamental:

- Identify and develop the best semiconductor opening switches (SOS)
- Develop LT-Spice models for DSRDs
- Develop pulser circuit theory and circuit optimization Scheme

Technical Approach: DSRD-basd Pulser





Drift Step Recovery

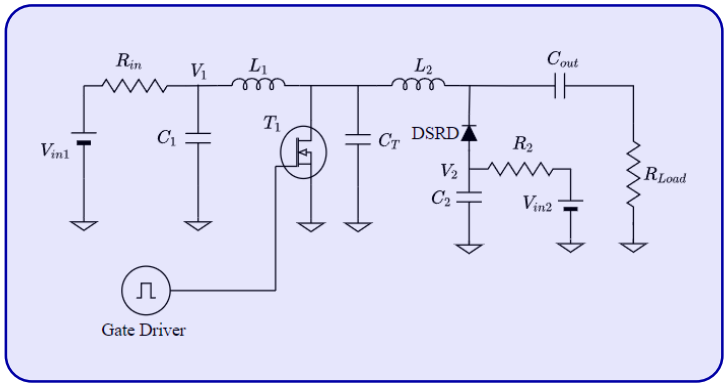
- Forward current injects charge carriers.
- Injected carriers (electron-hole plasma) survive for some time.
- Reverse bias extracts those carriers.
- Diode recovers, depletion layer emerges
- Diode becomes insulating.

If passed through an inductor L

$$V_{out} \propto L\frac{dI}{dt}$$

$$U_{out} = \frac{1}{2}LI_0^2$$

Pulser Requirements and Limitations



- Minimum reverse current of 200 A
- Nanosecond diode recovery

$$\frac{dI}{dt} > 200\text{A/ns}$$

- Diode stack with breakdown voltage

$$V_{\text{BR}} \geq 10\ \text{kV}$$

DSRD Diode

- COTS diodes are not available.
- Optimum diode doping profile is not known.
- Diode manufacturing process is not optimized
- Characterizations are not standard.
- SPICE models are not available.

Optimization

- Working principle/theory is not available.
- Circuit optimization is overwhelmingly tedious as there is no systematic scheme.

Drift Step Recovery Diodes: Objectives

Design and Modeling

DSRD doping profile must produce:

- High peak voltages (500 V – 1200 V per individual DSRD in DSRD stack)
- Fast risetimes (<= 2 ns at 4 kV peak voltage)
- High reverse current while maintaining DSRD fast risetime (>= 200 A/cm^2)

DSRD SPICE Models must capture:

- Correct DSRD operation for peak voltage, risetime and reverse current
- Correct DSRD operation for range of input voltages and trigger durations
- Interaction between pulser circuit and DSRD to predictively design and optimize DSRD-based pulsers

Characterization

- Low (<= 1 A) and high (up to 100 A) power forward current-voltage (IV) curves
- Capacitance-voltage (CV curves) up to 40 V reverse bias
- Reverse recovery testing (up to 200 V reverse bias)
- Reverse breakdown testing up to 3000 V

KPI for selecting best performing DSRD:

- Maximum on-state resistance (mΩ order) of DSRD stack
- Forward voltage drop at 50 A (for power diodes)
- Reverse breakdown voltage (limited by stack height)

DSRD TCAD Modeling and Simulation

Problem

How does DSRD doping profile affect DSRD pulser performance?

Method: TCAD Modeling

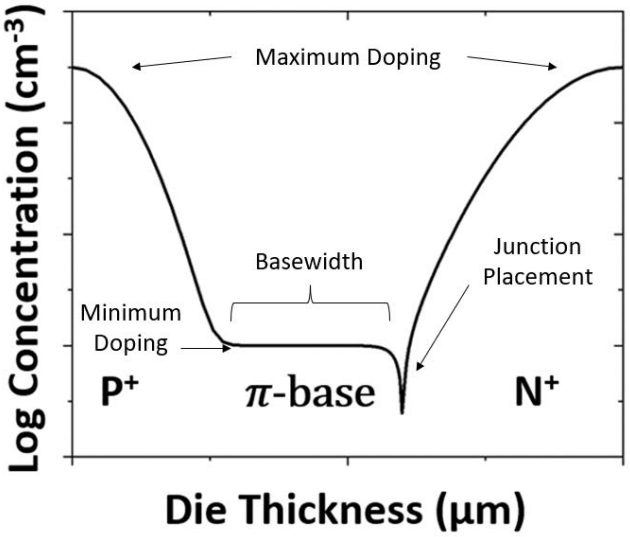
TCAD can model DSRD including doping profile and device geometry (area, thickness, stack height)

TCAD does not allow use of device manufacturer models so limited in DSRD pulser simulation (SPICE simulation and device models can be used)

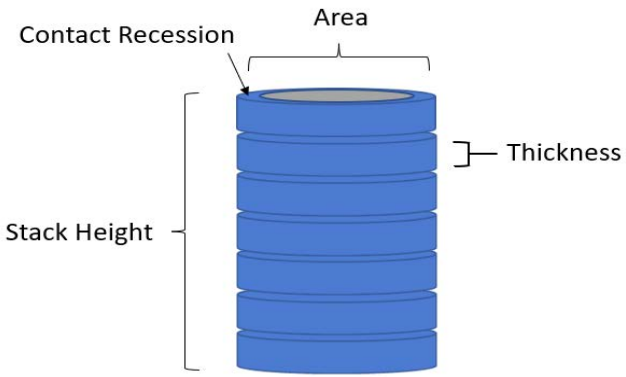
Outcome

First use of TCAD optimized exponential doping profile for DSRD, provided to the manufacturer (SPT)

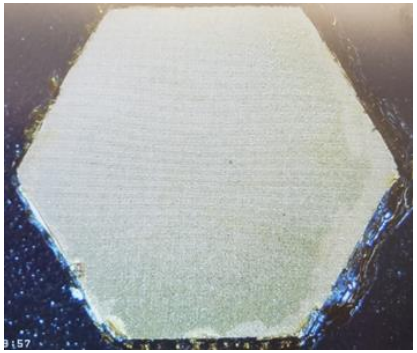
Standard Doping Profile



Geometry of DSRD Stack



Gen2 DSRD



21-stack DSRD



Area: 0.5 cm^2 and up
Thickness: ~200 µm
Stack Height: 1-40 DSRD

DSRD Characterization Measurements

Problem

What are the key performance indicators (KPI) of DSRD in DSRD pulsers?

Objective

Experimentally characterize DSRD for KPI and SPICE device model parameters

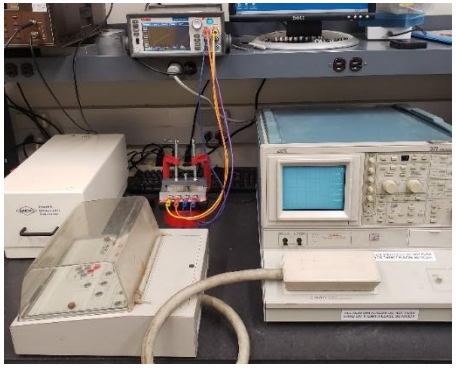
Key Performance Indicators

Series Resistance (R_s), Breakdown Voltage (V_B), Zero-Bias Junction Capacitance (C_0), Reverse Recovery Time (τ_R)

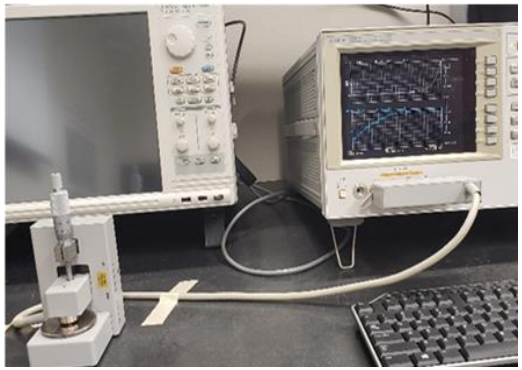
Outcome

R_S and V_B successfully selected top performing DSRD

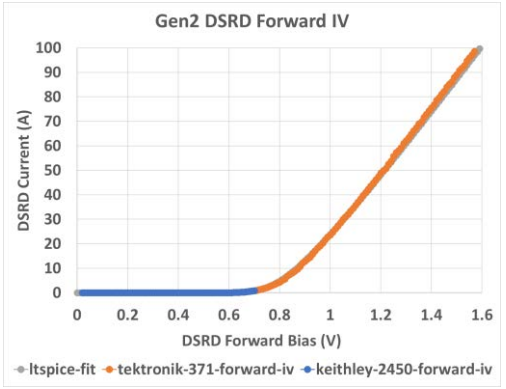
Methods: Standard Diode Measurements

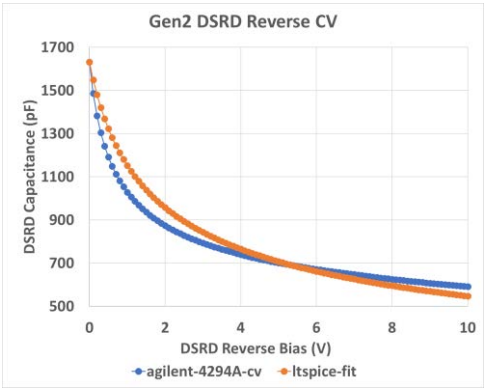


Current-Voltage (IV)



Capacitance-Voltage (CV)





Characterization allows selection of best performing DSRD and development of DSRD SPICE model

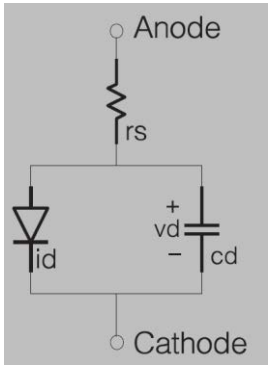
DSRD SPICE Modeling

Problem

What experimental data and device model are needed to model DSRD for pulser application?

Method

LTspice standard diode model fitted to forward IV, reverse CV and reverse breakdown used to model DSRD



Standard diode equivalent circuit model

First known attempt to model DSRD with standard diode model

$$i_D = I_s\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right]$$

Modified Shockley diode equation

Outcome

Parameterized LTspice DSRD models are optimized for DSRD pulser designs.

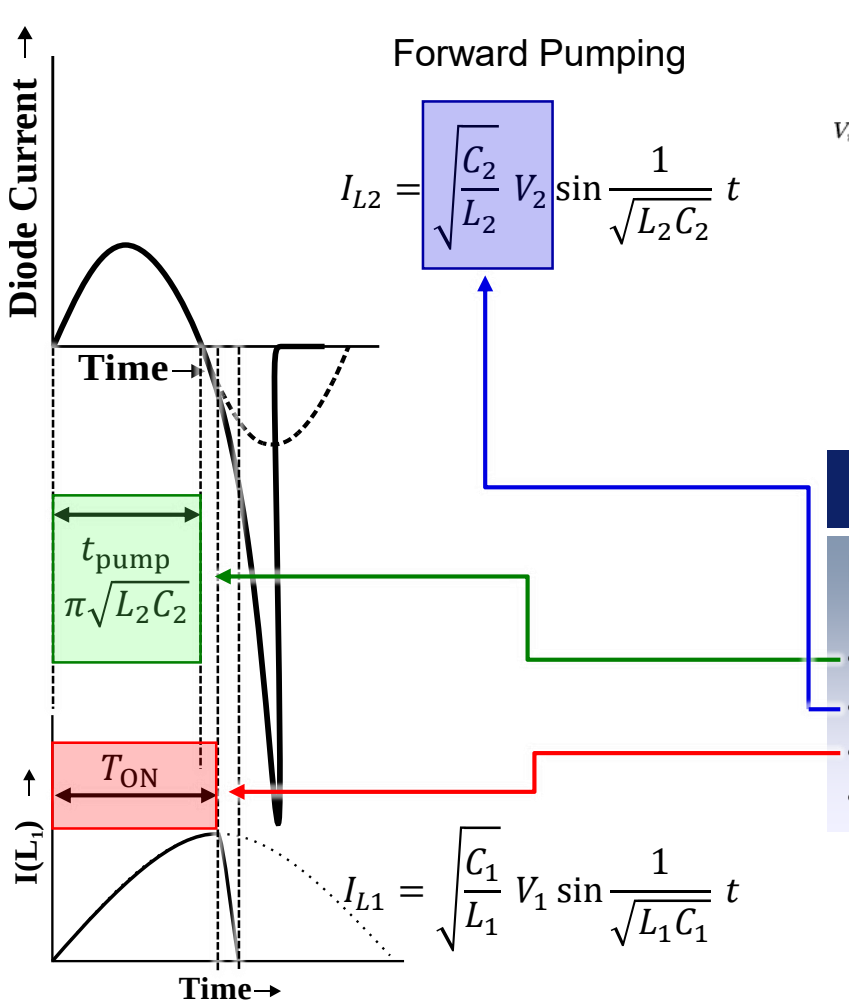
Diode	IS	N	IKF	RS	Error-2450	Error-371	CJO (pF)	M	Error-Cap	Transit Time (s)	Error-RRT
gen2.2-d1	1.00E-13	0.8	0.01	0.0068	2.94E-03	1.045	1425.5	0.39	4.07E-11	8.90E-06	3.32E-07
gen2.2-d2	1.00E-13	0.8	0.01	0.0066	2.66E-03	0.693	1348.92	0.36	3.32E-11	9.40E-06	2.92E-07
gen2.2-d3	1.00E-13	0.8	0.013	0.0073	2.42E-03	0.906	1431.42	0.41	4.12E-11	8.10E-06	3.38E-07
gen2.2-d4	1.00E-13	0.8	0.007	0.0109	5.17E-03	0.918	1478.53	0.4	4.24E-11	9.50E-06	3.58E-07
gen2.2-d5	1.00E-13	0.8	0.01	0.0078	3.02E-03	1.374					
gen2.2-d6	1.00E-12	0.9	0.037	0.0128	3.85E-03	0.623	1448.09	0.39	4.12E-11	8.40E-06	4.04E-07
gen2.2-d7	1.00E-13	0.8	0.01	0.0073	2.54E-03	0.749	1404.6	0.38	3.75E-11	8.90E-06	4.58E-07
gen2.2-d8	1.00E-12	0.9	0.04	0.0065	5.12E-03	0.467					
gen2.2-d9	7.00E-13	0.9	0.04	0.0084	3.61E-03	0.922	1446.94	0.39	4.02E-11	9.50E-06	3.78E-07
gen2.2-d10	1.00E-13	0.8	0.007	0.007	6.25E-03	0.620	1314.43	0.35	3.02E-11	9.60E-06	3.66E-07
**gen2.2-d11											
gen2.2-d12	1.00E-13	0.8	0.01	0.0063	3.41E-03	0.706	1485.72	0.4	4.31E-11	9.50E-06	3.48E-07
gen2.2-d13	1.00E-13	0.8	0.007	0.0073	6.84E-03	0.850					
**gen2.2-d14											

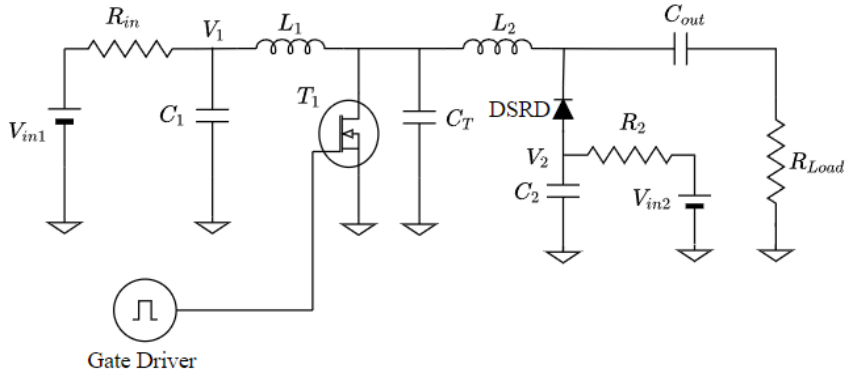
**broken

DSRD-based Pulser Circuit: Objectives

- Review and determine the best circuit topology for DSRD-based pulser circuit.
- Develop a working principle/theory for DSRD-based pulser utilizing inductive energy storage and release.
- Extend the theory for stacking DSRD pulsers in series and parallel for linear voltage gain.

Circuit Theory: Problems



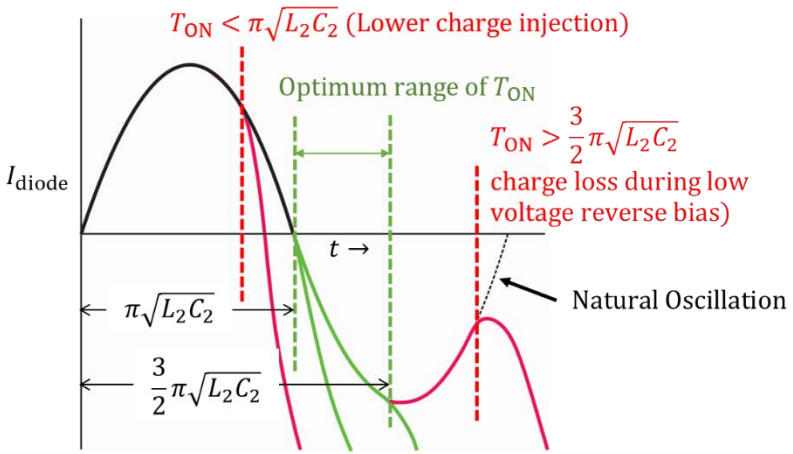


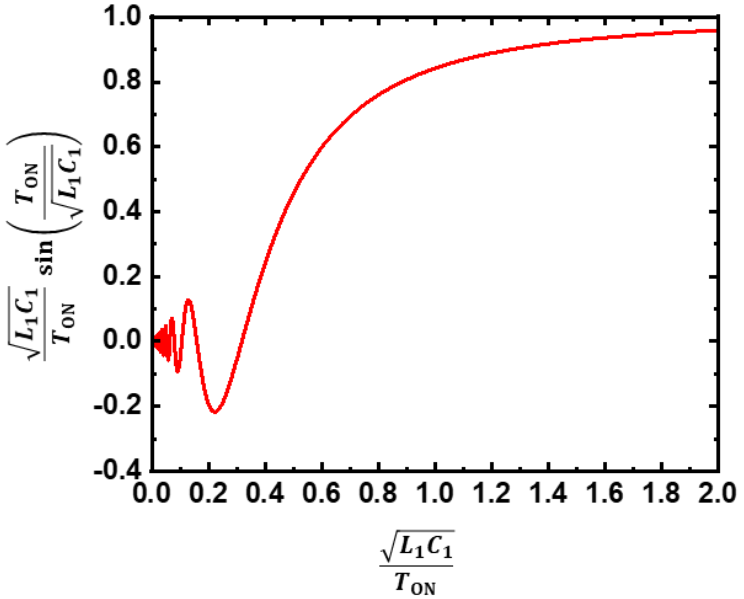
Problems:

For a target output voltage and risetime, what are

- The optimum forward pumping time (t_{pump})?
- The optimum forward pumping current (I_2)
- The optimum trigger length (T_{ON})
- $L_1, C_1, L_2, C_2, V_{\text{in1}}, V_{\text{in2}}$

Circuit Theory: Results





- $T_{ON} < t_{pump}$ results in less charge injection for same operation conditions
- $T_{ON} > 1.5\ t_{pump}$ results in low voltage charge extraction
- $t_{pump} \leq T_{ON} \leq 1.5\ t_{pump}$ is optimum range. (??)

$$V_{L1} = \frac{T_{ON}}{t_{off}} V_{in1} \left[\frac{\sqrt{L_1C_1}}{T_{ON}} \sin\left(\frac{T_{ON}}{\sqrt{L_1C_1}}\right)\right]$$

- C_1 can be as large as required.

Circuit: Optimization Scheme

Problem

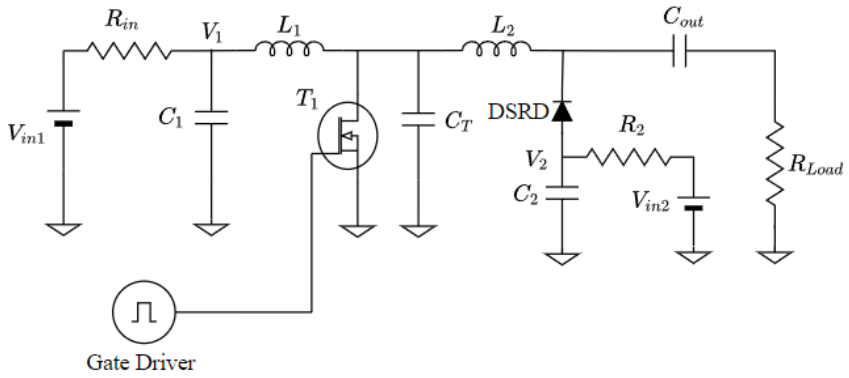
How do we get the target output voltage with maximum gain, efficiency and pulse repetition frequency (PRF)!

Solution: Use LT-Spice Sims

- Set minimum prime voltage
  $$V_{\text{in1}} = V_{\text{in2}} = 50\ \text{V}$$
- Start with small charge injected
  $$Q_{\text{inj}} = 10\ \mu\text{C}$$
- Vary the pumping time
  $$t_{\text{pump}} = 100\ - 1000\ \text{ns}$$

$$C_2 = \frac{1}{2}\frac{Q_{\text{inj}}}{V_{\text{in2}}}, L_2 = \frac{1}{C_2}\left(\frac{t_{\text{pump}}}{\pi}\right)^2$$

- Set Trigger length
  $$T_{\text{ON}} = 1.25\ t_{\text{pump}}$$
- Set $L_1 = L_2$
- Set a large capacitor
  $$C_1 = 100\ \mu F$$

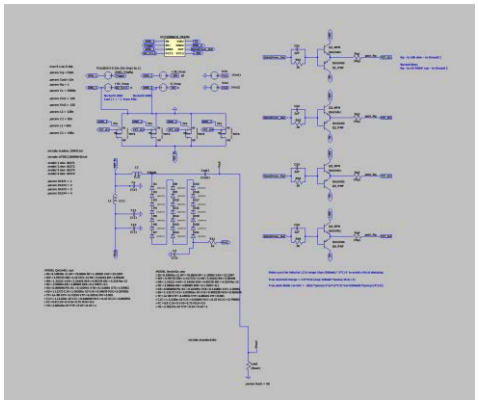


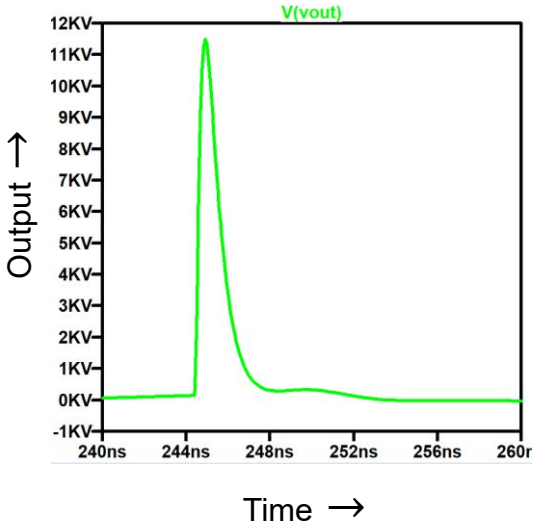
Optimum t_{pump} → Optimize T_{ON} → Optimize L_1

Make sure the MOSFET current and MOSFET Voltage do not exceed their limits.

Pulser Circuit: Simulation and Experiment

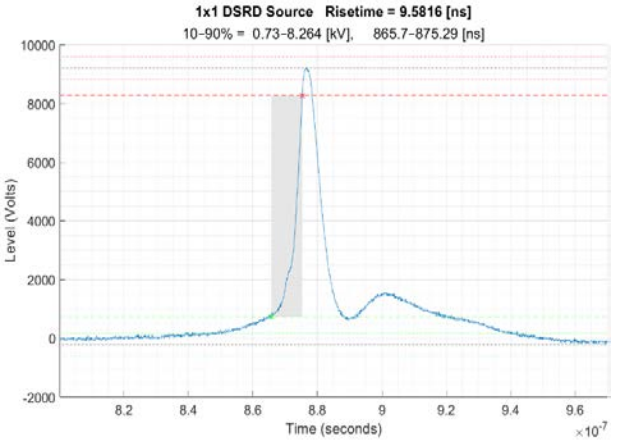
LT-Spice Simulation

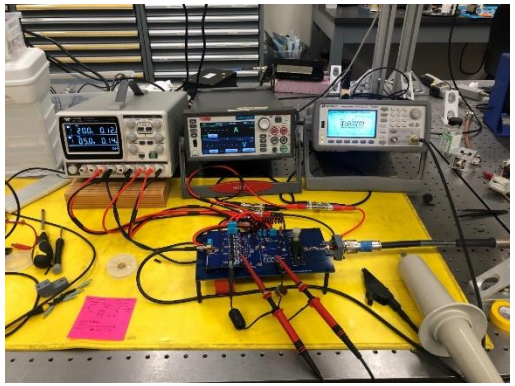




Experimental Setup and Results







$$V_{\text{peak}} = 9.2\ \text{kV}$$
$$t_{\text{rise}(10-90)} = 9.58\ \text{ns}$$
$$t_{\text{rise}(20-90)} = 5\ \text{ns}$$

Outputs

- **Manuscript in Preparation**
- G. Bhattarai, "Optimizing multi-stacked nanosecond DSRD-based pulser: theory, simulation, and experiment" Intended to publish in IEEE transactions in power electronics

- **Conference Presentations**
- S.Bellinger, A.Caruso, A.Usenko, "New Paradigm on Making Semiconductor Opening Switches for Pulsed Power" oral presentation (virtual) at 2021 23th IEEE Pulsed Power Conference, Dec. 12-16, 2021, Denver, CO.
- S.Bellinger, A.Caruso, A.Usenko, "Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme", at 240th Electrochemical Society Meeting, Oct. 10-14, 2021, Orlando, FL – oral (online) presentation
- G. Bhattarai, J. Eifler, S. Roy, M. Hyde, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "All Solid-State High-Power Pulse Sharpeners" (Poster)
- J. Eifler, S. Roy, M. Hyde, G. Bhattarai, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "TCAD Optimization of Epitaxially Grown Drift-Step Recovery Diodes and Pulser Performance" (Poster)
- M. Hyde, J. Eifler, S. Roy, G. Bhattarai, A. Usenko, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "Development of an Evaluation Network for Drift Step Recovered Diodes through and Augmented Design of Experiment" (Poster)
- D. F. Noor, J. Eifler, M. Hyde, G. Bhattarai, S. Roy, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "DSRD-IES Pulsed-Power Generator Topology Study Using Machine-Learning-Based Feature Selection Optimization and Predictive Learning" (Poster)
- S. Roy, J. Eifler, M. Hyde, G. Bhattarai, D. Noor, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, "Systematic Topological Optimization of DSRD-Based IES Pulse Generator" (Poster)

Personnel



Roy Allen



Alex Usenko



Jay Eifler



Sourov Roy



Abu Hanif



Gyanendra Bhattarai



Shailesh Dhungana



Steven Bellinger



Neal Strathman



John Bhamidipati

Summary

DSRD Doping Profile

- TCAD was used to determine the best DSRD doping profile. An exponential doping profile is predicted as the best for the first time among other alternatives.

Diode Characterization/SPICE Modeling

- A SPICE model for DSRD is developed for the first time based on the standard diode model, which has produced experimental output very close to the simulated.

Circuit Theory and Optimization

- A simplified working principle/theory for DSRD-based pulser circuit is developed.
- A systematic scheme for circuit optimization is presented which has reduced simulation time significantly and resulted in expected pulsed output voltage.

Recommendations & Future Work

Diode Characterization/SPICE Modeling

- Measure dynamic reverse breakdown voltage using pulser setup (Transitioned to PTERA project)
- LT-spice model development and parameterization could continue for new DSRD, as well as further testing of the robustness of the models and the parameters.
- CMC diode model development and testing (Transitioned to PTERA project)
- DSRD characterization methods and testing (Transitioned to PTERA project)
- DSRD doping profile, defects and geometry determination using TCAD simulations (Transitioned to PTERA project)

Circuit Theory and Optimization

- Extension of circuit theory to include series and parallel stack of pulsers to increase voltage output (Transitioned to PTERA project)
- Alternative circuit topology for optimized pulsed output (Transitioned to PTERA project).

Solid-State Pulse Sharpener

- Solid-state closing switches (SCS/SAS) for sub nanosecond pulse sharpening.

Questions

Thank You

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for c-sUAV Study (OSPRES Grant)

N00014-17-1-3016
09/30/2017-09/29/2022

Solid State Switch and Diode Devices

Steven Bellinger

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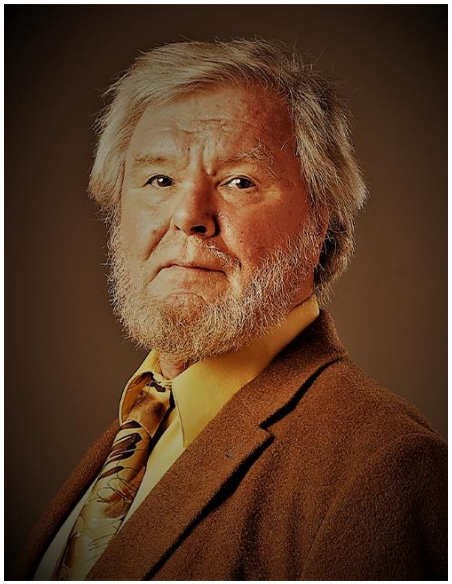
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Motivation

- **WHY: Short Pulse power generators can improve performance with semiconductor devices designed to work in a pulsed mode.**
- **Commercial availability of these diodes is very limited, e.g., Si Photoconductive Solid-State Switches (Si-PCSS) & Drift Step Recovery Diodes (DSRDs/SOSs/SASs)**
- **Need for more commercially available and varied pulsed-power diodes, e.g., Si-PCSS, SOS, SAS, DSRDs.**
  - Still leveraging 20-60 year-old manufacturing methods and equipment.
- **Main motivation is to manufacture pulsed-power diodes (Si-PCSSs & DSRDs) using some recent mature methods combined with traditional technology and methods.**
- **Our approach is to apply new processes and old processes where necessary to manufacture high-performance power diodes Today.**

Diode manufacturing Team

Many other people at MIDE were involved



Alex Usenko
Research Professor
MIDE



Steven Bellinger
President / CEO

SPT & RDT



Neal Strathman
Technician

RDT

Outline

- **Si-PCSS Manufacturing Methods**
  - Designs
  - Lessons Learned
  - Results

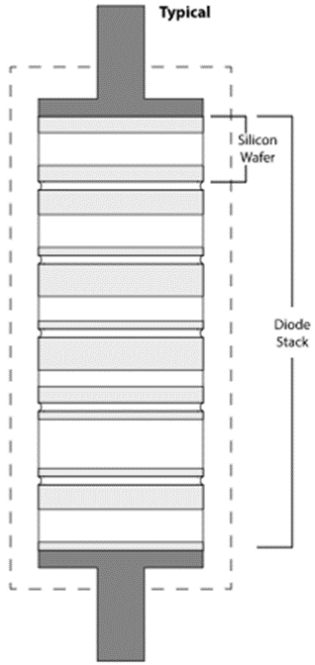
- **DSRD Manufacturing Methods**
  - Designs
  - Lessons Learned
  - Results

Objective

- **Manufacture Si-PCSS for laser triggered pulsed power.**
  - Milestone: Improve edge passivation to increase peak holding voltage. COTS single diode holding voltage ~1200VDC. Increase to 10KVDC per single element.
  - Milestone: Change geometry to match to a Cylindrical Ringdown Oscillator (CRO).
  - Milestone: Increase manufacturing readiness level (MRL) to 8 (pilot line).

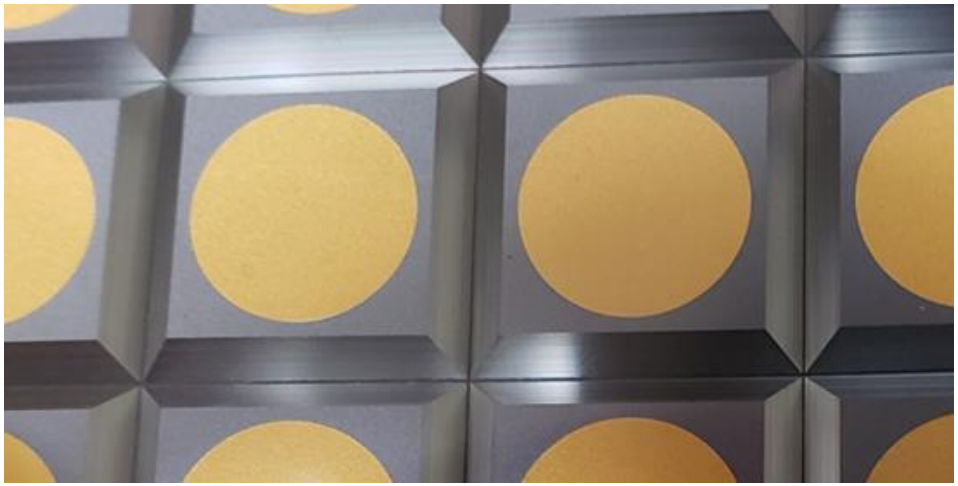


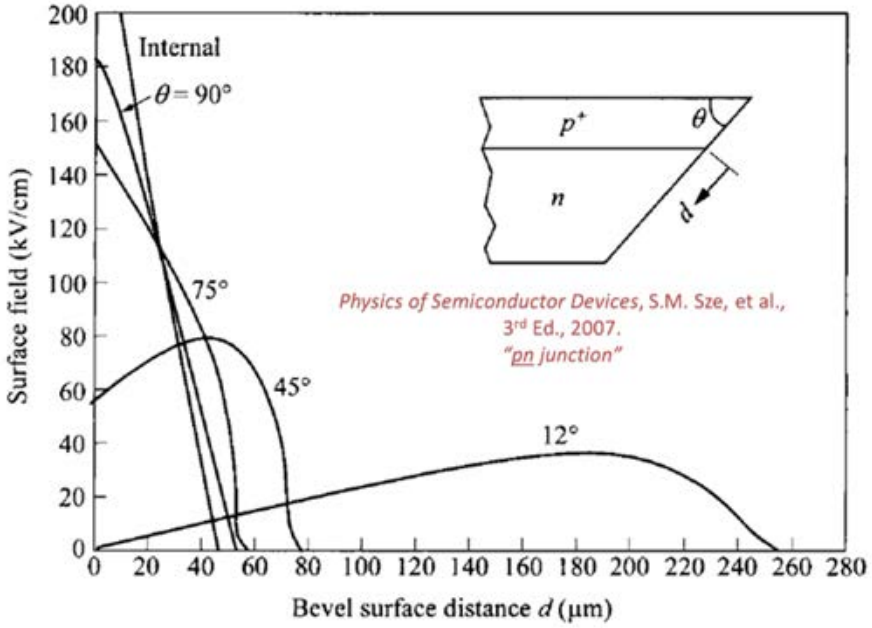
- **Manufacture DSRDs for pulsed power.**
  - Milestone: Improve edge passivation to increase peak holding voltage to 1kV per chip.
  - Milestone: Improve Dopant Profile Control
  - Milestone: Stack DSRD chips to attain peak holding voltage of: threshold 10kV & target 20kV.
  - Milestone: Increase manufacturing readiness level (MRL) to 8 (pilot line).



Technical Background and Approach

- **Diode Structure and Edge Passivation of switch devices are the two most important features of their hold-off voltage capability.**
- **Current practice in high voltage community: Beveled edge and deep-graded junction dopant design methods employ theoretical and simplified manufacturing methods to optimize diode operation under high electric fields.**
- **Beveled edge for reduced electric field at edge. Beware of dangling bonds and fixed electric-trap states at edge from singulation.**

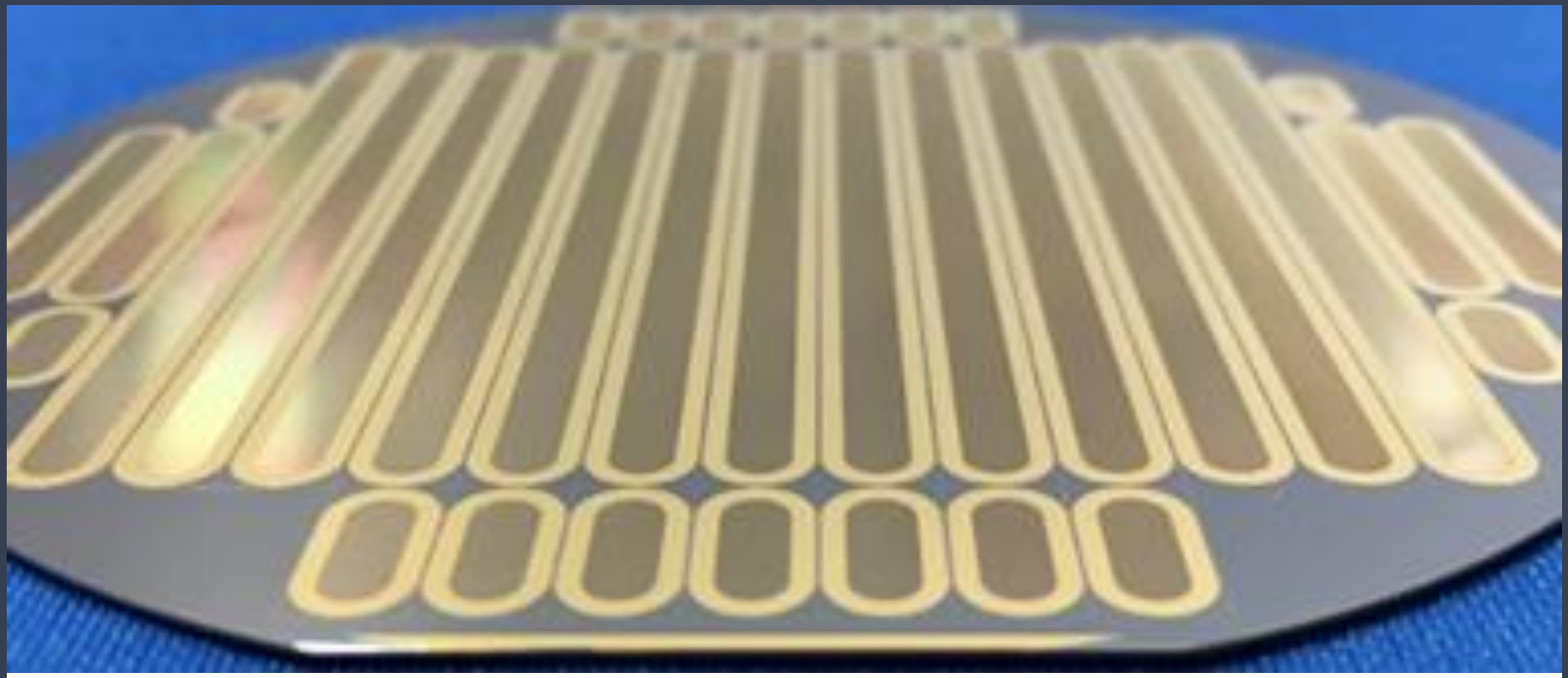




Si-PCSS and DSRD Design & Practical Difficulties

- Switch Parameters:
  - *pin* junction-area and wafer thickness (to the breakdown limit)
  - Voltage-holding and sweepout characteristics for variant diode-structures & geometries:
    - Length versus width of Si-based switch
    - P- & N-type junction diffusion profiles
  - For Si-PCSS Optical energy density, placement, metal trace window pattern, and antireflective coating. Optical absorption length and absolute pulse energy on the degree of bulk conductivity (current carrying → thermal-generation)

- Diode Edge Passivation :
  - Bevel to reduce electric field at singulation edge.
  - Mass production methods for edge passivation.
- Packaging: contact leads (inductance), potting, cooling, Si-PCSS laser window.

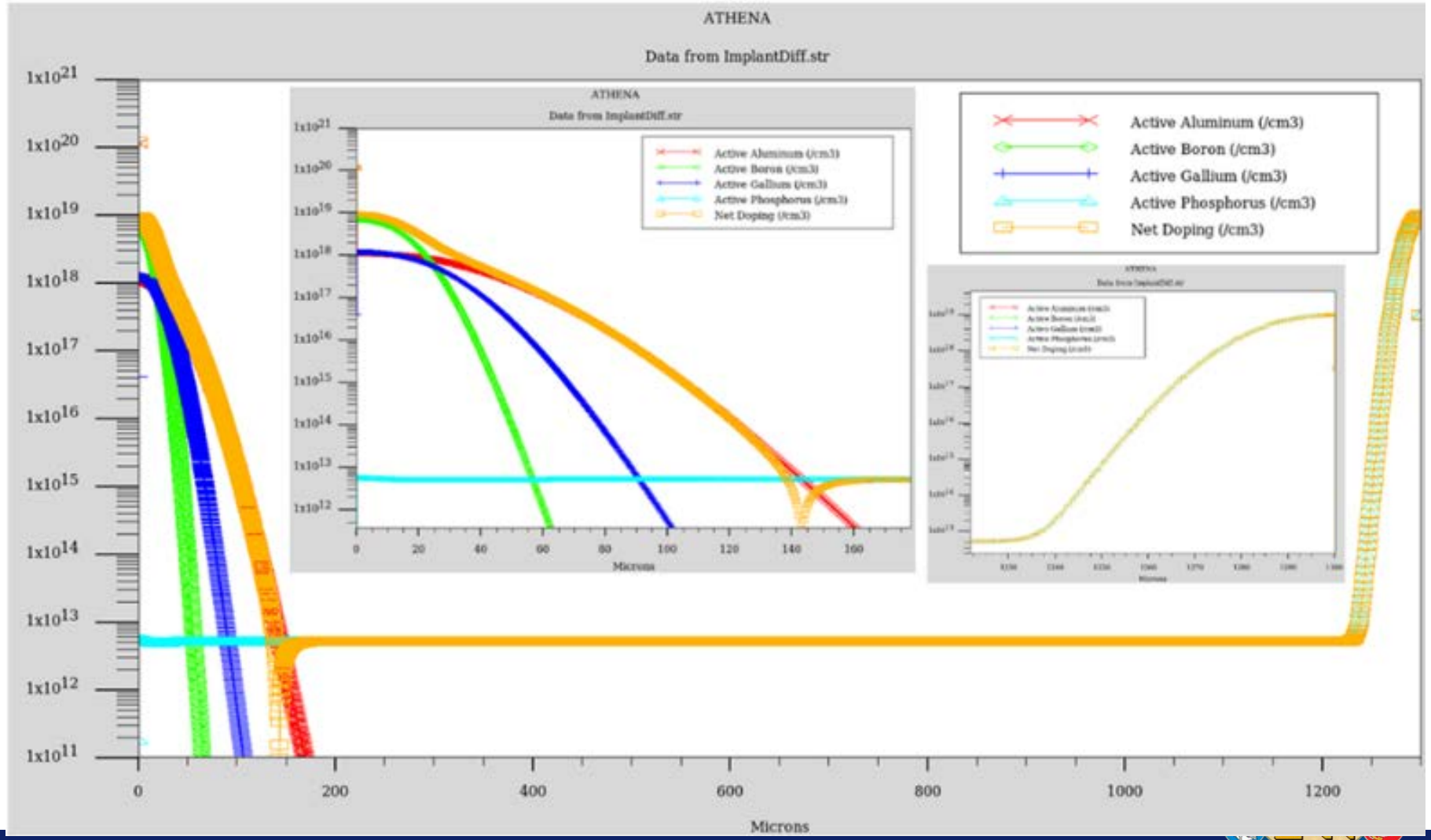


Si-PCSS

Si-PCSS Dopant Profile

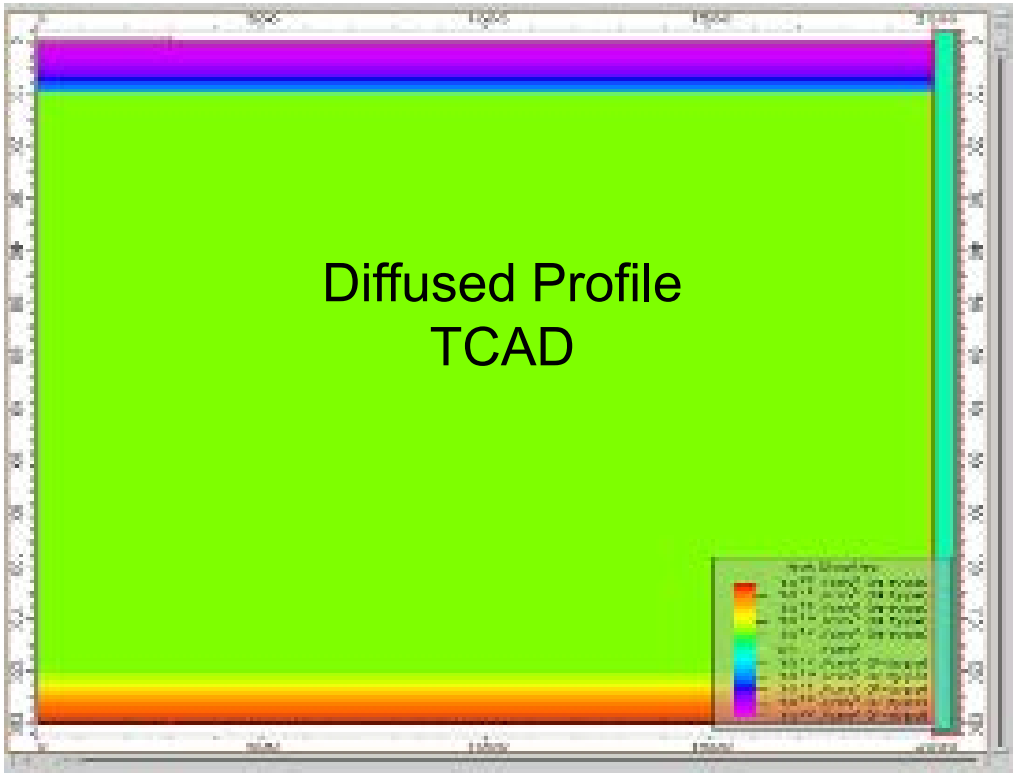
- **Simulated Profile**

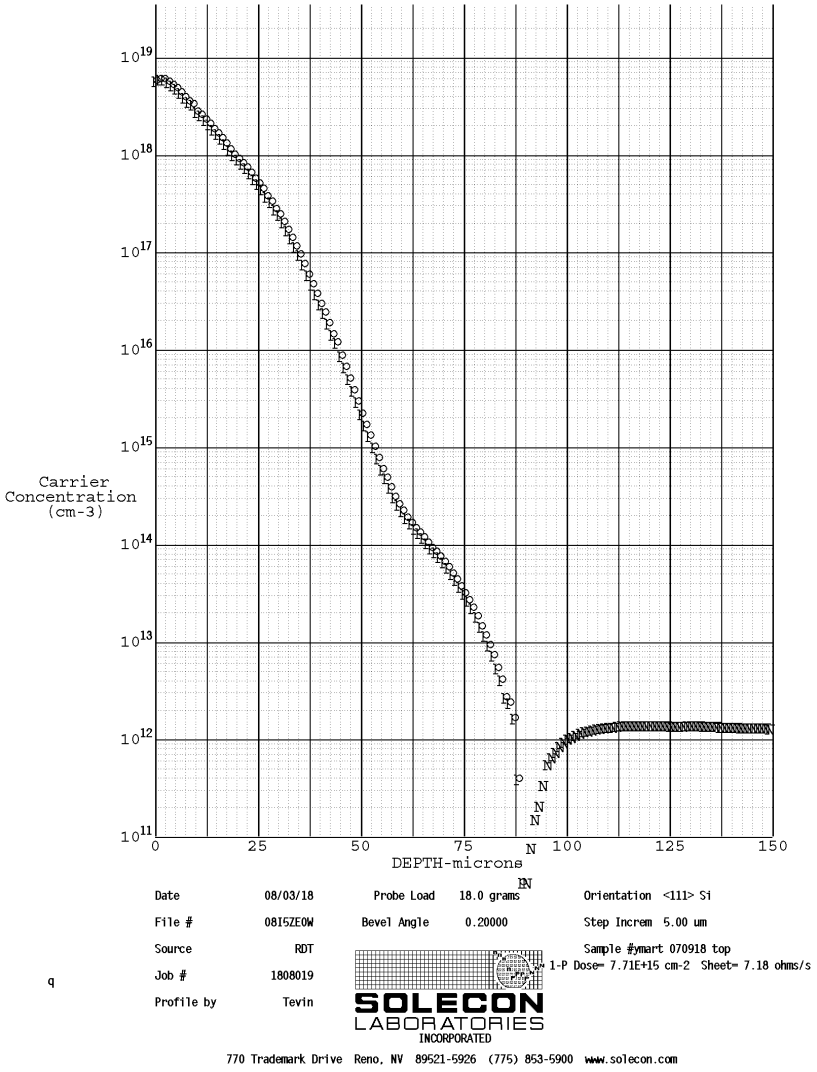
Vertical dopant diffusion profile in TCAD with multiple dopants (net = orange)



Si-PCSS Dopant Profile

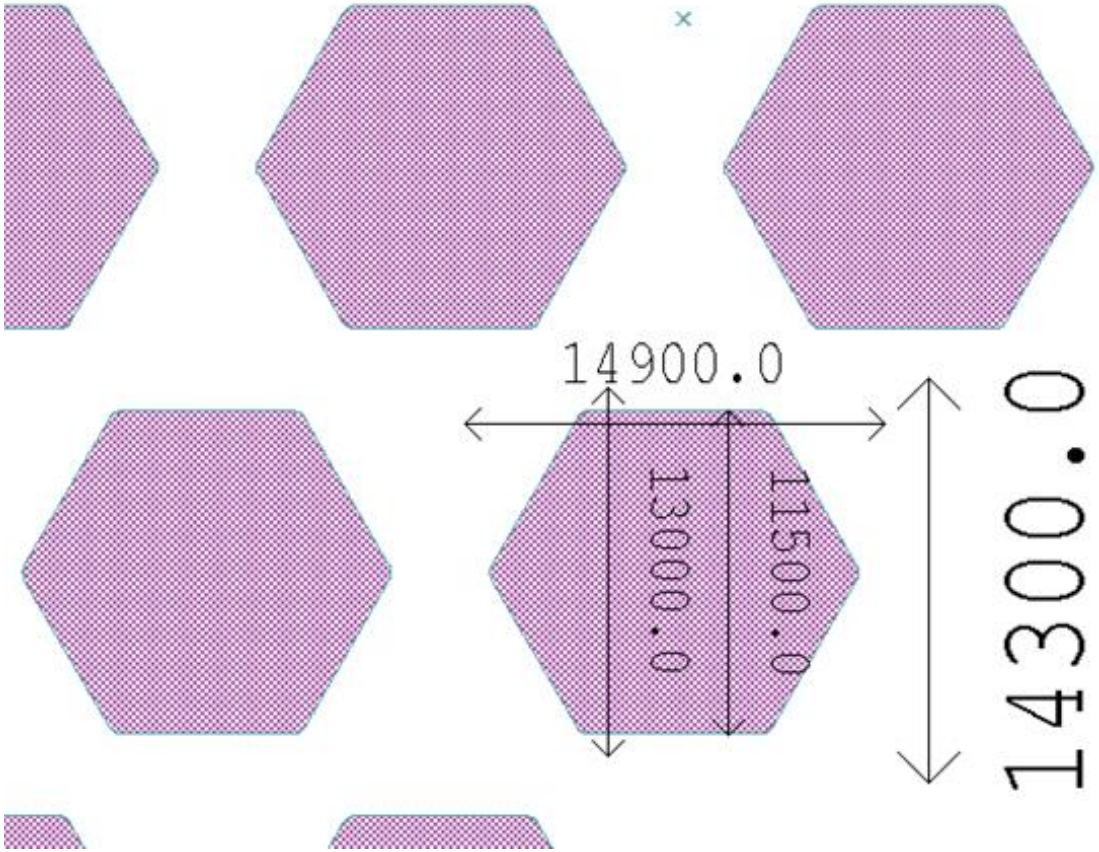
- **Implant B/Al for p-type side, can do Ga to smooth dip**
- **Implant P for n-type side**
- **Si3N4 LPCVD Out-diffusion Cap**
- **1250C for 48hrs**





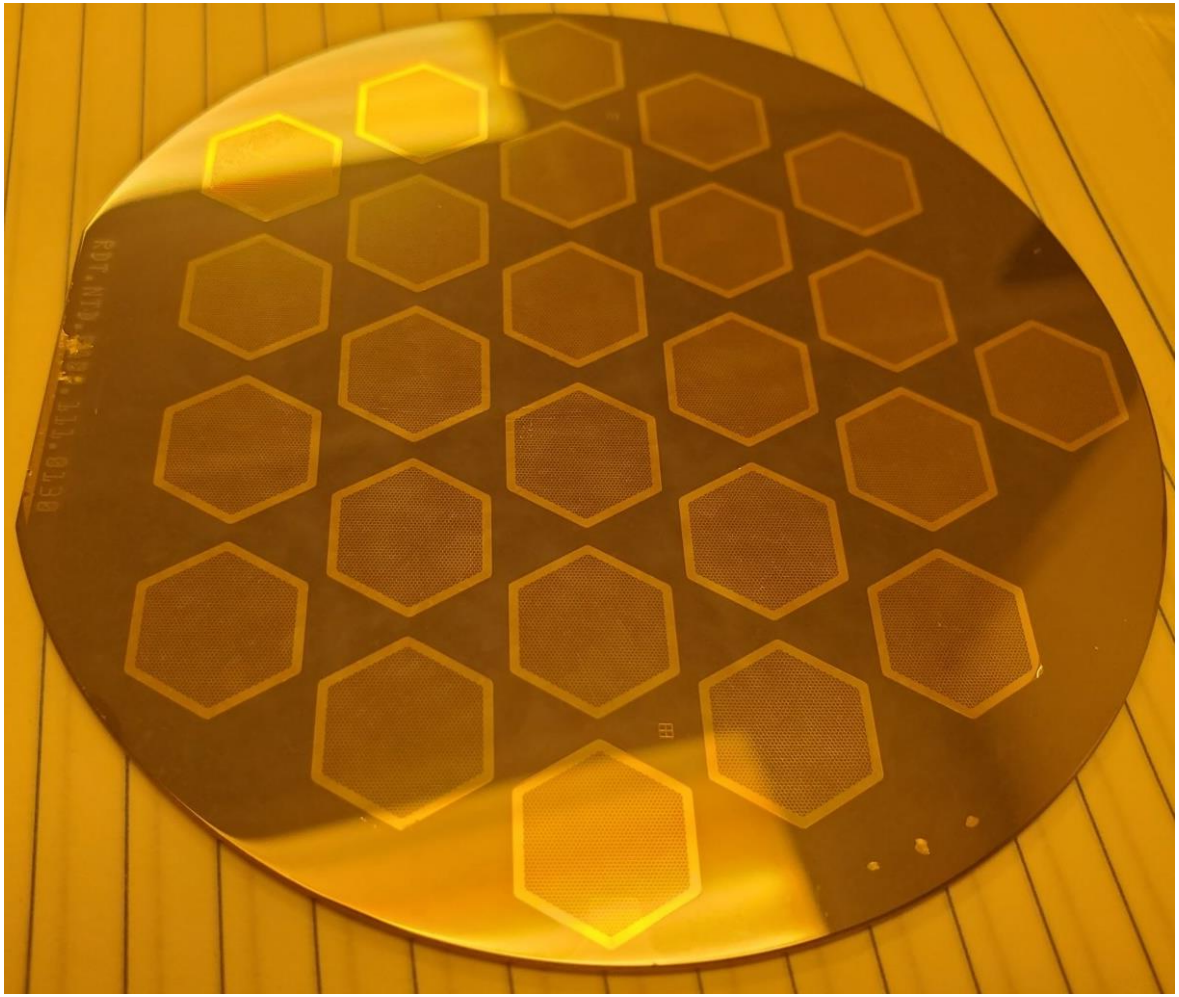
Si-PCSS Pattern

- **Design and Dimensions (microns) of Si-PCSS Chips**
  - Hex pattern to reduce Si Waste during singulation
  - Significantly reduce required laser energy by at least 10% from designing and optimizing Si-PCSS top contact: Hex Metal Array



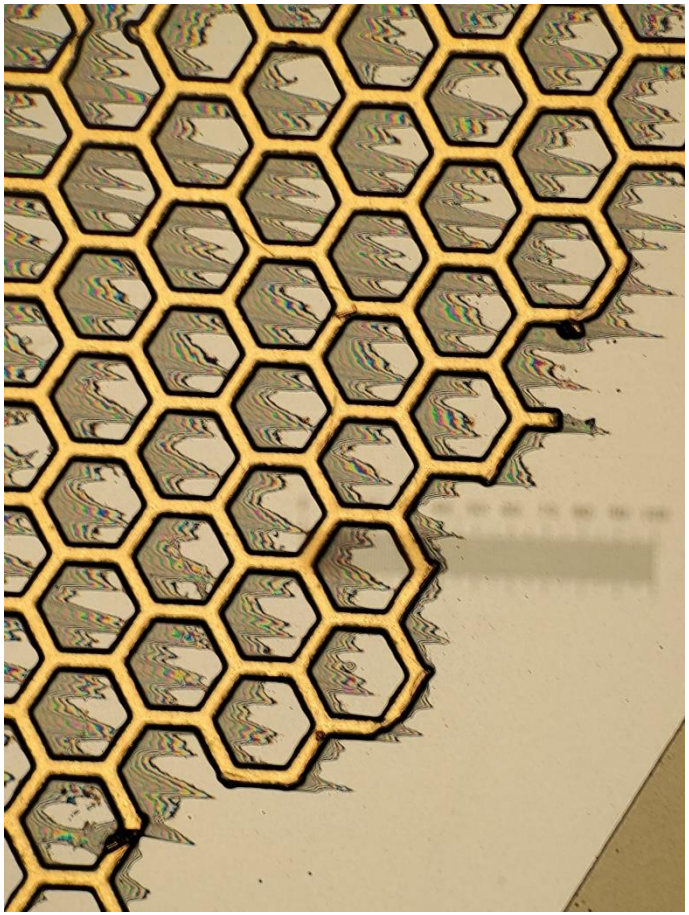
Si-PCSS Metal Patterning

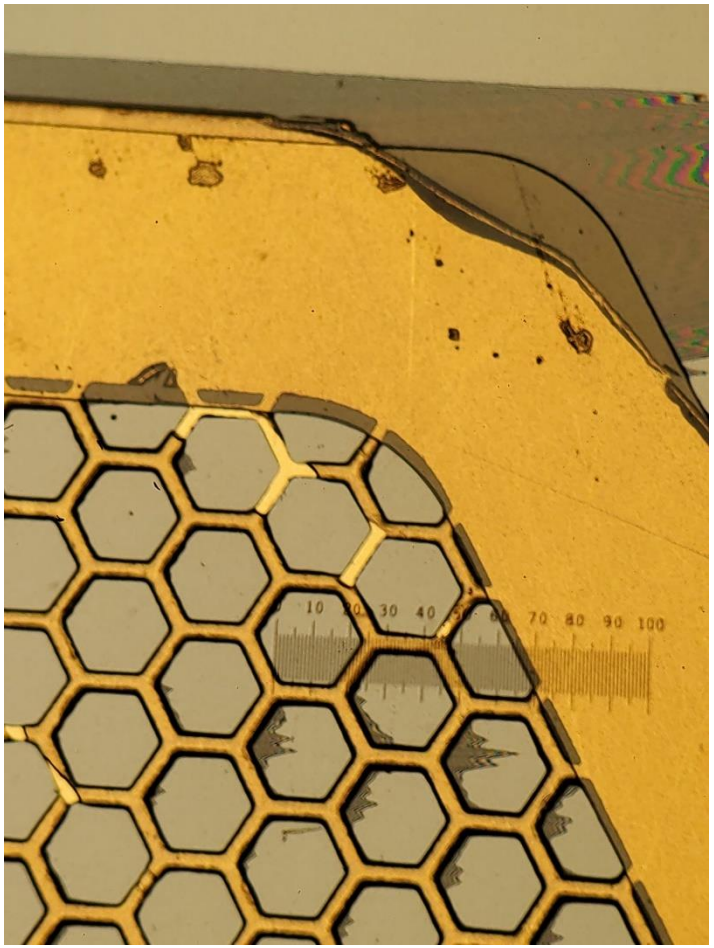
- **Photolithography Metal Liftoff**
  - Ebeam evap metal: Ti/Cu/Ti/Au (2um thick Cu for higher current)



Lessons Learned

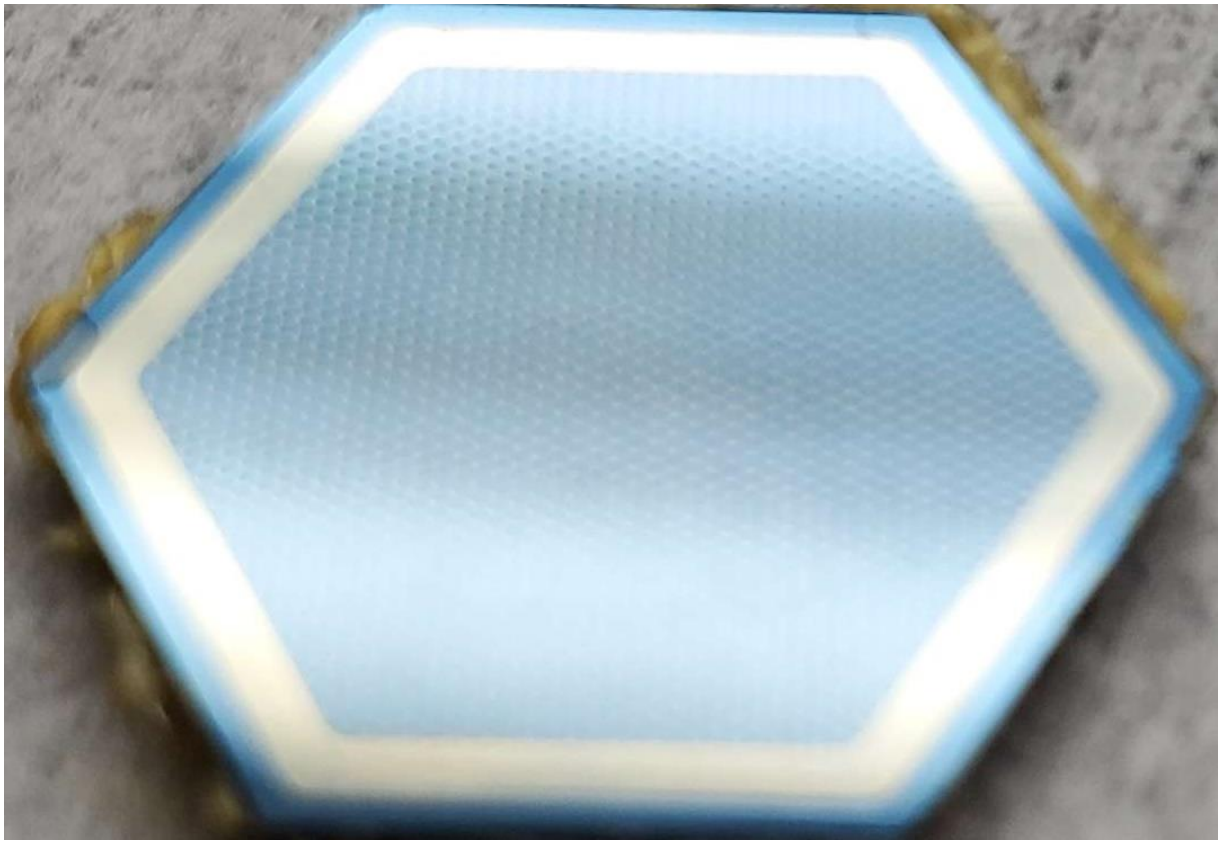
- **Photoresist Cross-linking due to Basic pH Surface from Cu/Au metals**





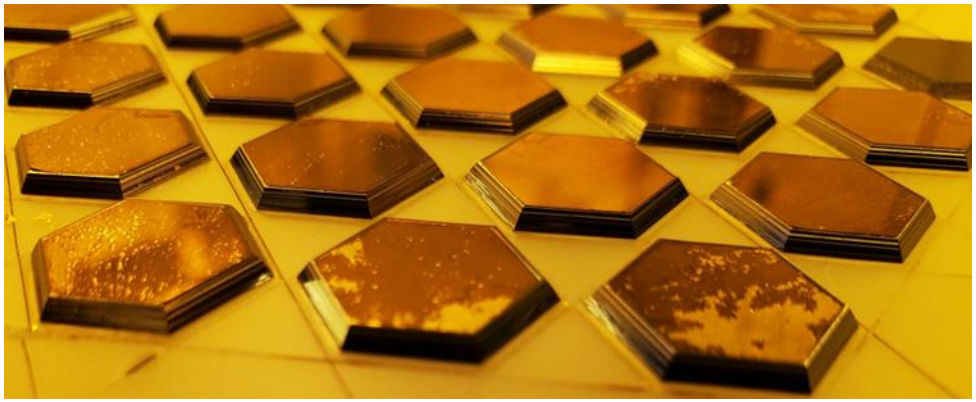
Lessons Learned

- **Reactive Sputter Si3N4 antireflective coating over everything**
  - ARC coating falls off Au-Metal layer, hence, no need for PR liftoff process



Lessons Learned

- **HNA and TMAH Metal Damage ->**
  - Pro: Batch wafer process
  - Con: very aggressive and non-selective
- **Black-wax Spin on Protection**
  - Pro: Spin on and very resistive to HNA
  - Con: Opaque, not easily patternable





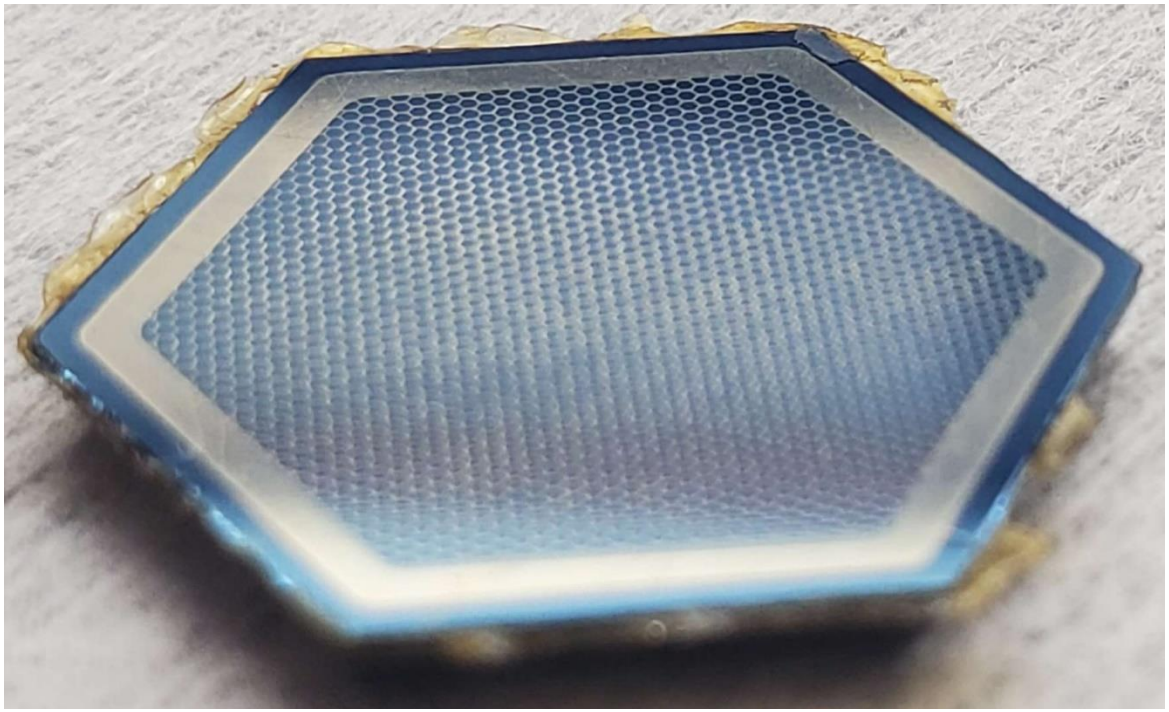
Lessons Learned

- **XeF2 is still the preferred edge singulation-damage removal.**
- **Pros:**
  - Very selective to Si and nothing else.
  - No Acid/Base caustic chemistry
  - No plasma damage
- **Cons:**
  - Limited to 1-wafer at a time
  - Remove F^- and dangling bonds
    - Experimenting with O2 vac anneal or Ozone



Si-PCSS Chips/Devices

- **Bevel 60deg. at 75% through wafer, then straight cut through to prevent chipping.**
- **Topside metallization of Hex Si-PCSS Chip**
  - Manufactured with polyimide coating at edge
  - Hex metal pattern to improve current collection and sweep out on opening.

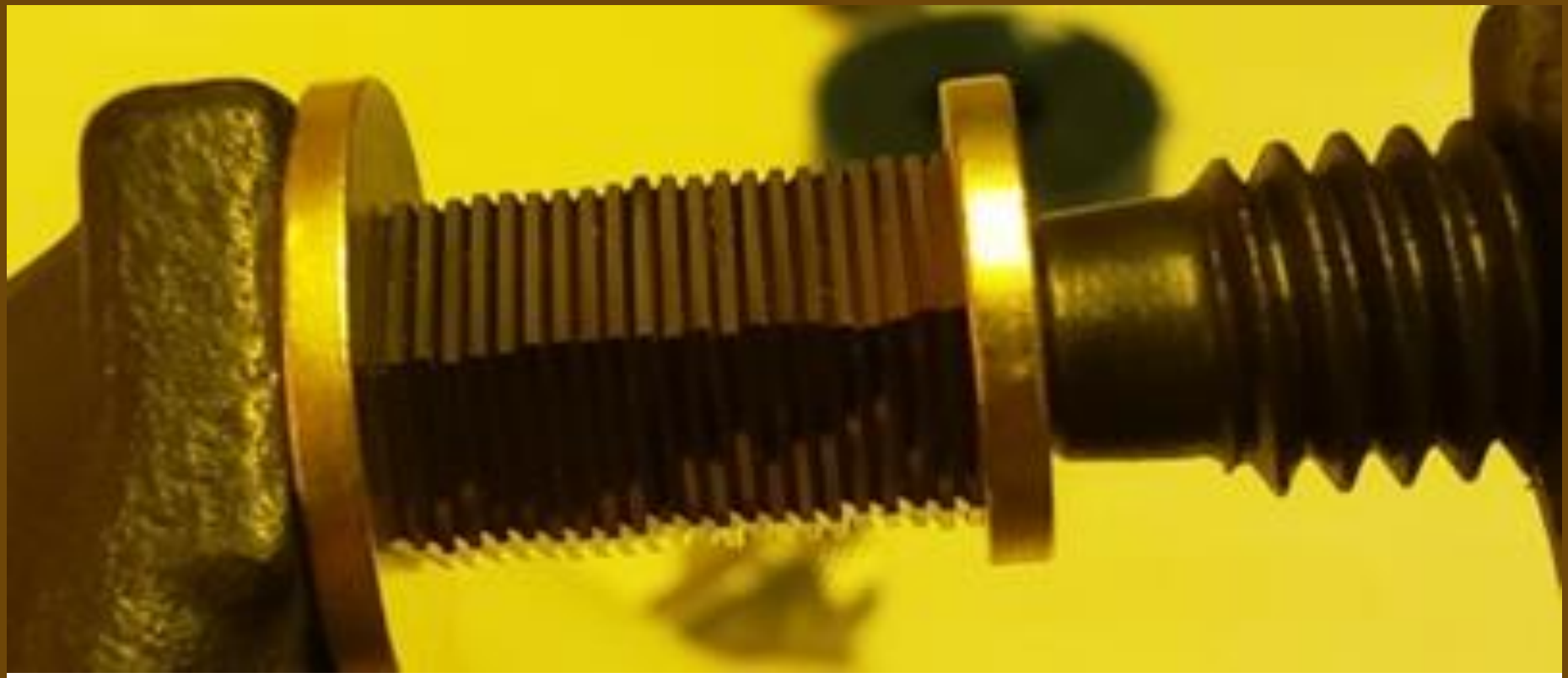




Results

- **Si-PCSS Peak Holding Voltage**

ID#: 023-22-HEX-8		ID#: 023-22-HEX-3	
Volts	**Current**	**Volts**	**Current**
2.5kV	35uA	2.5kV	25uA
5kV	104uA	5kV	95uA
7.5kV	502uA	7.4kV	485uA
		10kV	604uA



Epi-DSRD

Epi-DSRD

- **We refer to this as Gen-2 DSRD.**
- **<u>Epitaxial Growth:</u>**

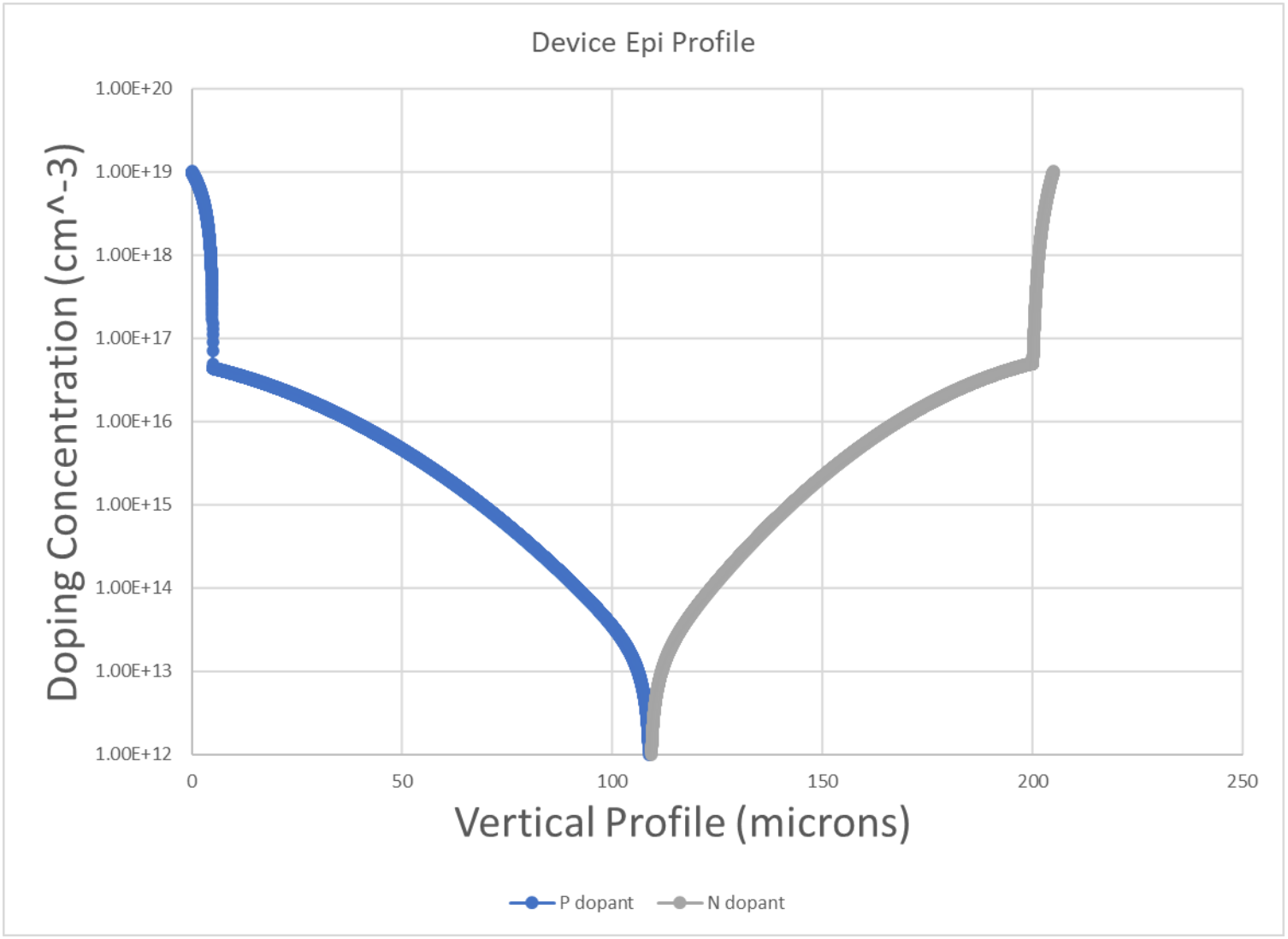
PROs:

- Gives precise control over junction placement and graded profile.
- Allows for an abrupt dopant concentrations.
- Allows for development of a manufacturing process that will yield more uniform doping structures.

CONs:

- Difficult to grow 200um thick epitaxy layer of varying dopant concentration.
- Hard to find vendor.

Epi-DSRD Target Dopant Profile



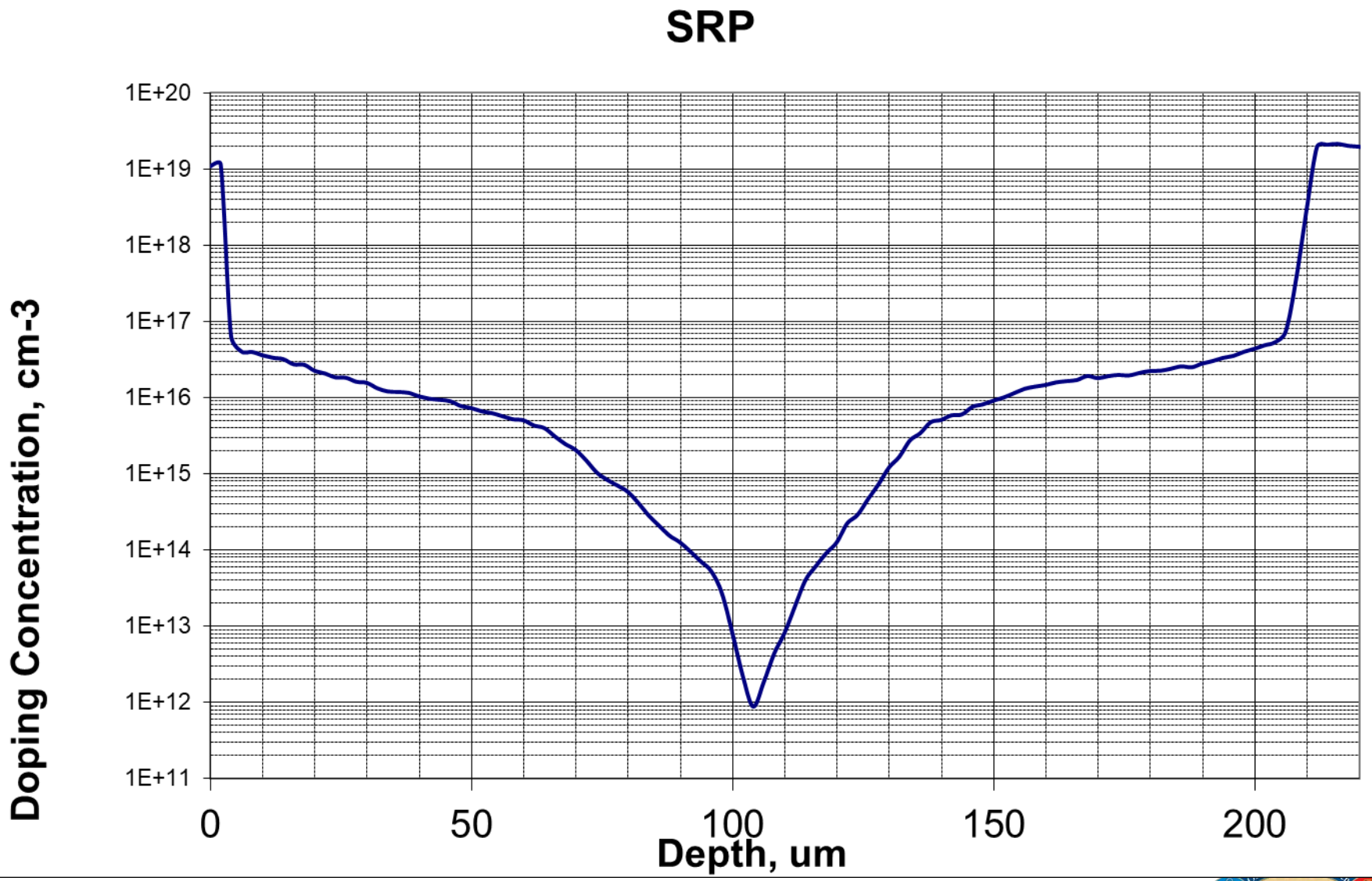
Epi-DSRD Epitaxy Layer Stackup

- **Note 1. Substrate thickness 400 um is likely the thinnest due to high Epi thickness.**
  - Not safe to use thinner substrate because of the mechanical stress that will occur during Epi growth.
- **Note 2. Different dopants (Phos VS Boron) give different resistivity levels while concentration is matched.**
- **Possible Issues: Resistivity gradient of graded layers is too large which may result in a "stepped" non-continuous shape of curve.**
  - Start with a stepped profile and proceed by increasing the number of steps until the curve looks smooth.
- **Manufacturing Methods: Can epi-layering be performed by doing a 1- 5 micron stair-step function, and then can thermally anneal the concentration and through diffusion create a pseudo linear junction?**
  - Annealing during epitaxy steps (>1000C) creates a smoothed profile.

Epi-DSRD Specification

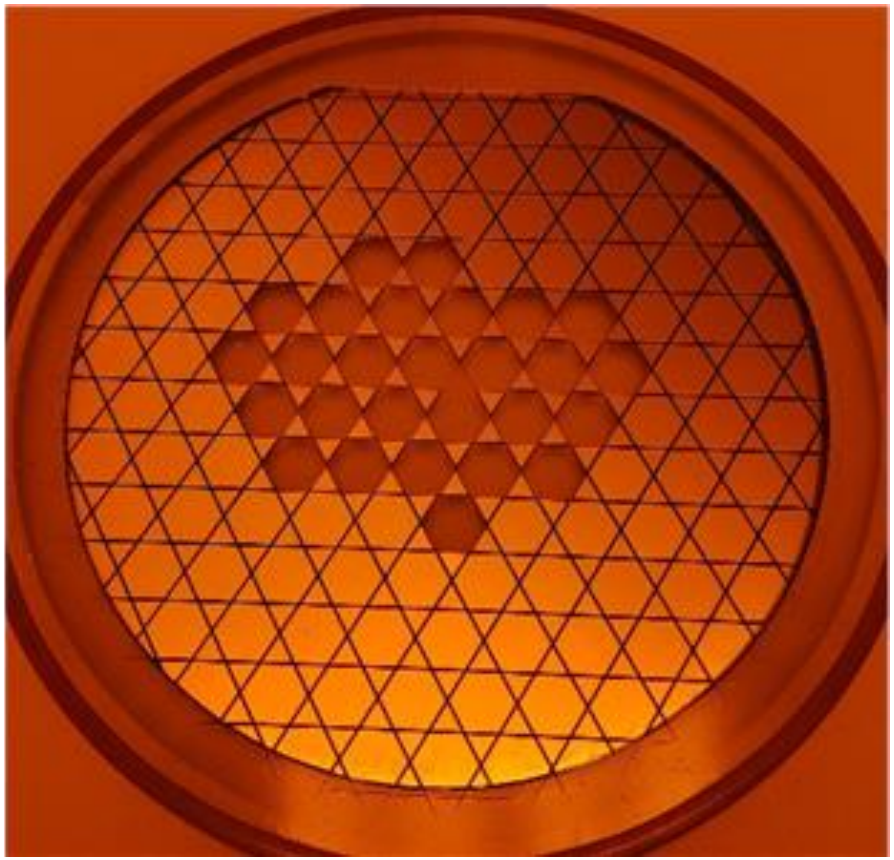
Layer No.	Sub/Epi	Type	Dopant	Thickness um	Concentration at/cm3	Resistivity ohm-cm
0	Substrate, vendor provided	N++ (100), vendor choice; 1 semi standard flat	As, vendor choice	600 um (thin as possible), will need to polish down to 10-20 um after epi.	1E19	0.003
1	Epi	N graded	Phos	100	5E16 → 1E12	0.14 → 4400
2	Epi	P graded	Boron	100	1E12 → 5E16	14600 → 0.35
3	Epi	P+	Boron	5	1E19	0.009

Epi-DSRD As-Built Profile



Metallization

- **Evaporated Metal on Both Sides of 150mm Wafer**
  - Cr/Au Optimum for Thermocompression Bonding
  - Note: Cr/Au holds up well to HNA

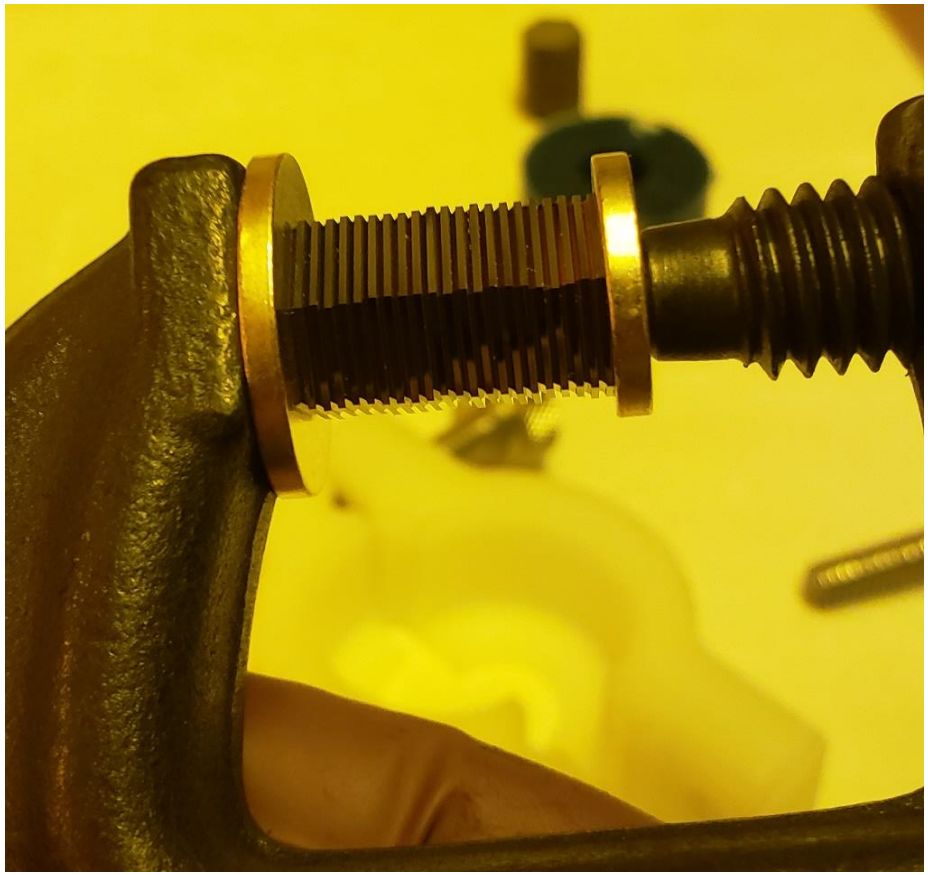




DSRD Chip Stacking

- **Chip Bevel and Stacking of DSRD**
  - Thermocompression Bonding of Chips: Vacuum oven at 500C

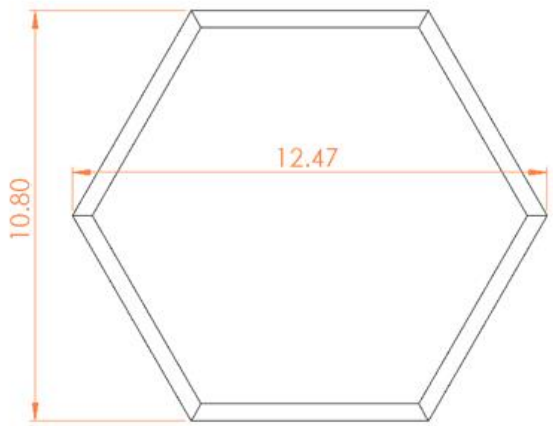


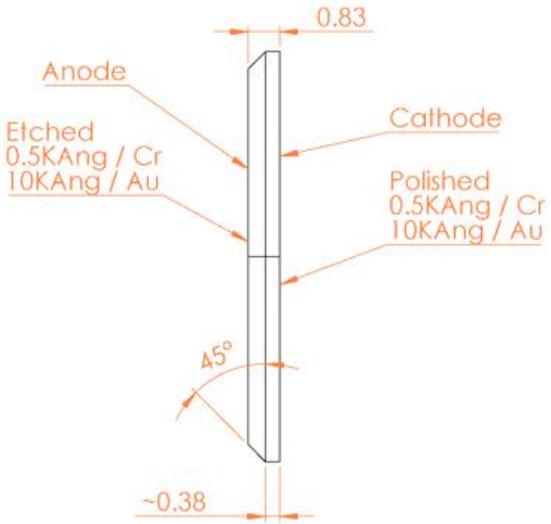


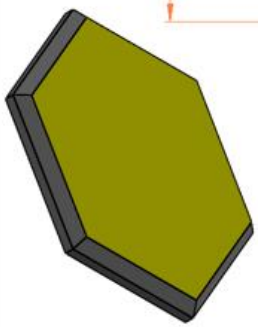
DSRD Chip Drawing

Ref: DSRD Bare Chip Drawing

Part #: DSRD-B01.EP2







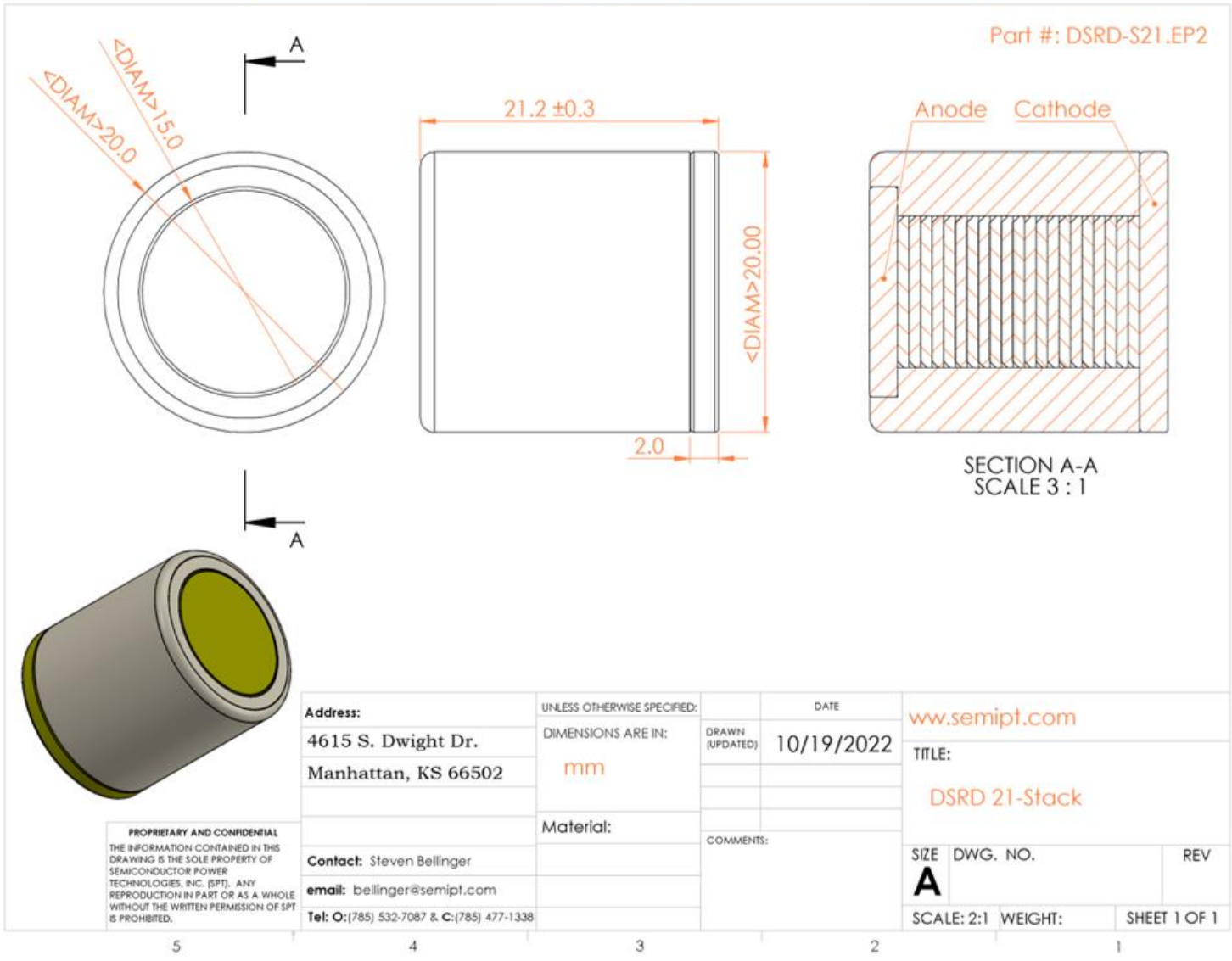
Address: 4615 S. Dwight Dr. Manhattan, KS 66502	UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN: mm	DRAWN (UPDATED) 10/19/2022	ww.semipt.com	
	Material: Si	COMMENTS:	TITLE: DSRD Bare Chip	
Contact: Steven Bellinger email: bellinger@semipt.com Tel: O:(785) 532-7087 & C:(785) 477-1338			SIZE A	DWG. NO. / REV
			SCALE: 5:1	WEIGHT: / SHEET 1 OF 1

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21-Stacked Package Drawing

21-Stacked DSRD w/ Epoxy-Overmold Drawing

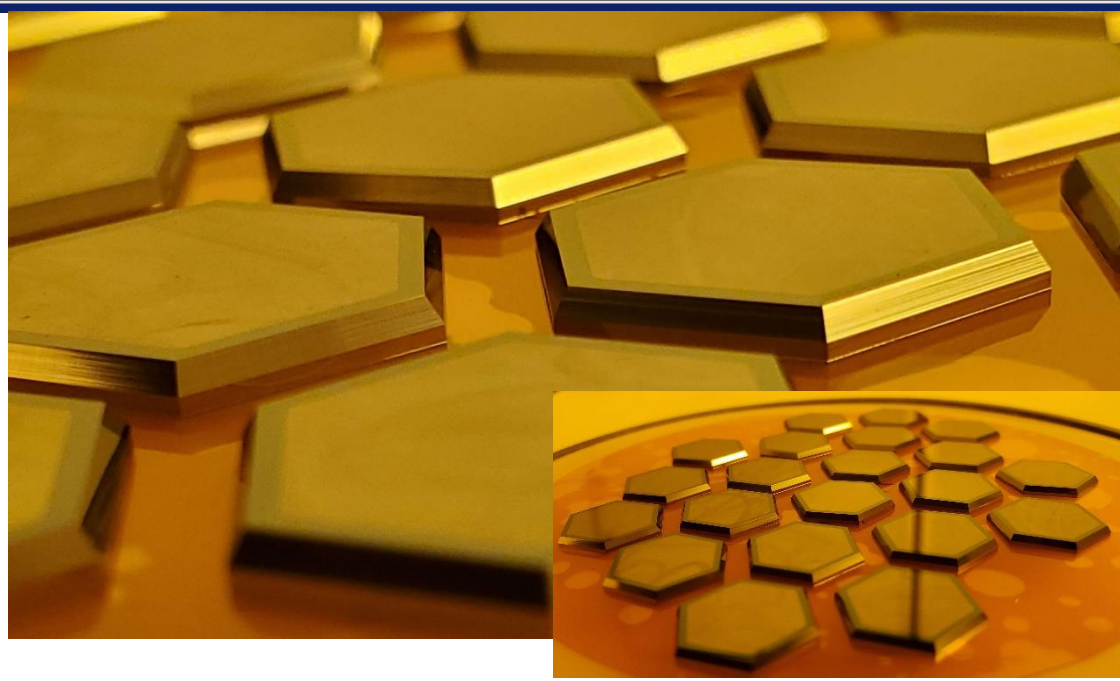


- **DSRD Electronic Properties Testing**

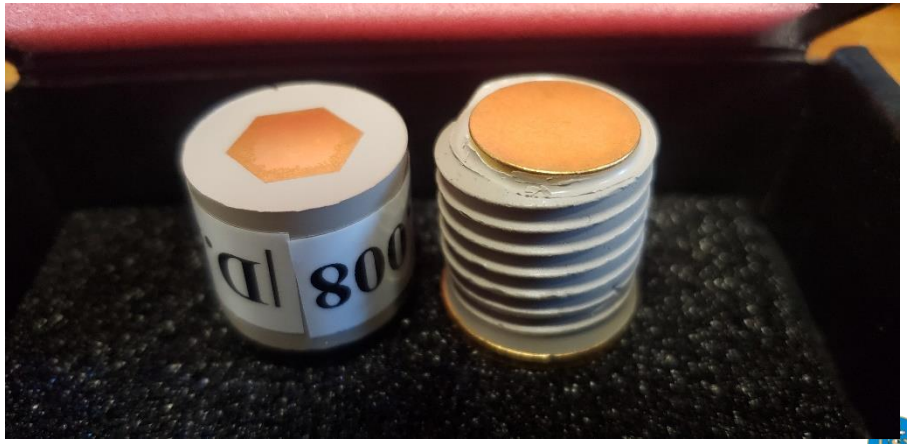
ABSOLUTE MAXIMUM RATINGS (T_a = 21° C)			
PARAMETER	**SYMBOL**	**VALUE**	**UNIT**
DC Reverse voltage	V_R	15,000	VDC
Reverse current	I_R	1.0	mA
Operating temperature range	T_{amb}	-40 to 50	° C
Storage Temperature	T_{stg}	-40 to 150	° C

Outputs: 100s of DSRDs and PCSS Chips

- **List:**
  - Si-PCSS Chips/Devices
  - DSRD Packaged Stacks







Summary & Future Work

- **Manufactured Si-PCSS and DSRD Chips for Pulsed Power Research**
- **Leveraged SOTA Epitaxy to create custom dopant profile for DSRDs**
- **Developed new manufacturing methods and approaches for diode edge field relaxation and passivation**
- **Stacked DSRDs to increase peak hold-off voltage**
- **Looked at new approaches for packaging for thermal considerations**

- **Future Work:**
  - Electron irradiate lifetime killer in Si-PCSS to improve recovery 20MR dose
  - DSRD and Si-PCSS edge passivation improvements: Ozone, vacuum oxidation, glass encapsulation.
  - Glass Passivation or Al2O3 Laser-Sintered Passivation
  - Wafer level DSRD Stacking --- See Alex Usenko Presentation

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for c-sUAV Study (OSPRES Grant)

N00014-17-1-3016
09/30/2017-09/29/2022

Novel Process Flow for Manufacturing of Drift Step Recovery Diodes

Alex Usenko

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Motivation

- **OSPRES uses short pulses. It needs pulse generators. In turn, this require semiconductor devices designed to work in a pulsed mode. Commercial availability of these devices – DSRDs – drift step recovery diodes is very limited.**
- **Moreover, all the commercially available DSRDs are manufactured using 60-years old technology.**
- **Therefore, the pulsed performance of commercially available DSRDs is not much different from 60-years old ones.**
- **Main motivation is to manufacture DSRD using different than traditional technology to get to the higher level of the performance.**
- **Our approach is to adopt new processes already developed in semiconductor industry into DSRD manufacturing process flow.**

Objective

- **Manufacture DSRDs with major performance metrics exceeding competitors**
- **Achieve rise time <1 ns for pulses 10 kV or higher**
- **Milestones:**
  - Develop novel process integration scheme for DSRD manufacturing
  - Prove technical feasibility of every new process step used in the process flow
  - Optimize recipes for each of the process steps
  - Manufacture a lot of DSRDs sufficient for testing and use in the pilot pulsers

Process Flow Comparison

Process Steps	Traditional Process Flow	Our Novel Process Flow
Wafer Preparation	Thinning	None
Doping	Diffusion	Graded Epitaxy
Metallization	Blanket Deposition	Selective Plating
Patterning	Photolithography	Photolithography
Die Side Termination	Mechanical Sawing	Anisotropic Etch
Die Side Passivation	Polymer Coating	Stain Etch
Stacking	Soldering or Eutectic	Intermetallic bonding

Technical Background and Approach

- **Our approach is to replace doping, termination, passivation, metallization and stacking process steps by adopting new processes developed in various areas of semiconductor industry to DSRD manufacturing. Specifically:**
  - Doping: replace diffusion by graded epitaxy
  - Termination: replace mechanical sawing by anisotropic etch
  - Passivation: replace polymer coating by stain etch
  - Metallization: replace blank metal deposition by selective deposition
  - Stacking: replace eutectic bonding by intermetallic bonding
- **Notice: we are replacing all the steps in the DSRD process flow except of one - photolithography**
- **Next 3 slides illustrate our novel process integration scheme**

Optional: Outline

- **Sub-projects**
  - Develop graded epitaxy process
  - Develop die side termination process
  - Develop die side passivation process
  - Develop metallization process
  - Develop die stacking process
  - Run full DSRD process flow based on the process steps developed

Process flow – part 1

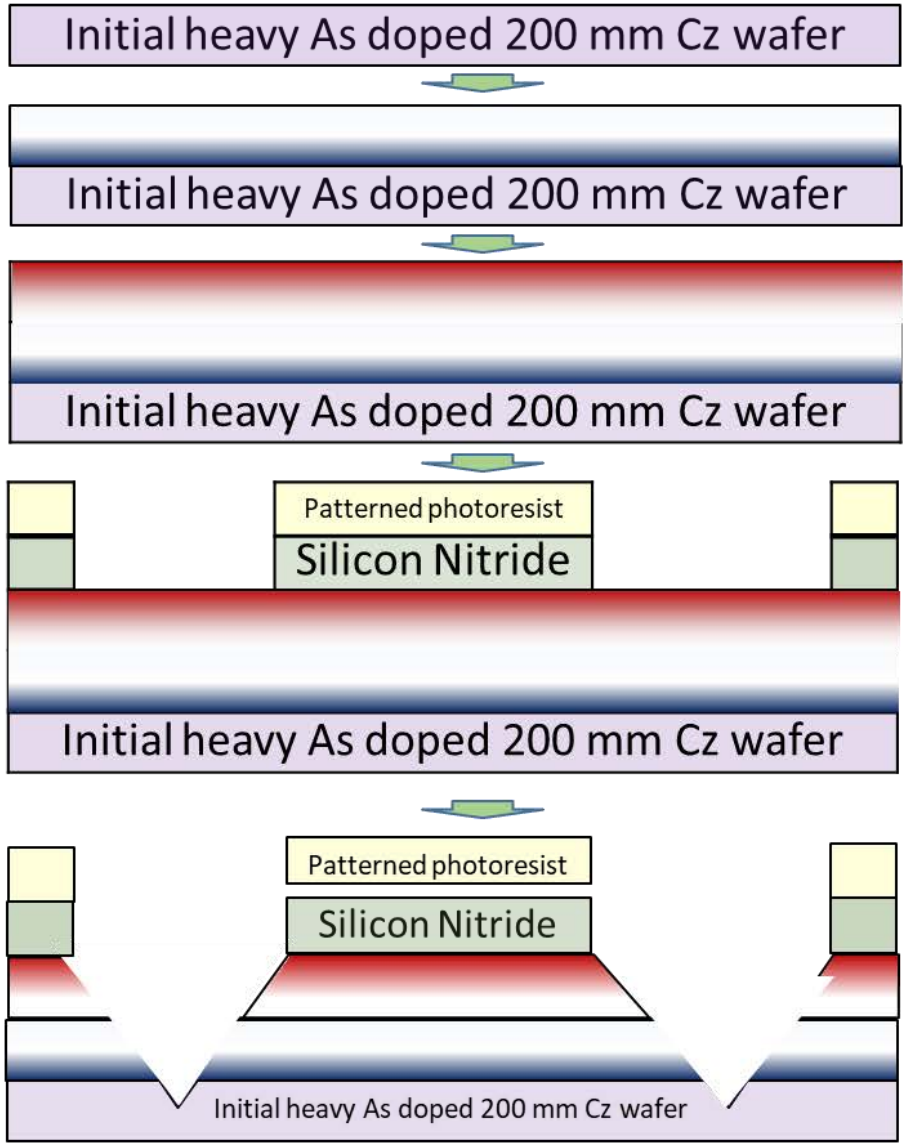
Stable mechanical substrate and internal getter

N-doping profile formed

P-doping profile formed, P-n Diode structure ready!

Preparing to divide into individual diode dies

Divide into dies.
But it is still single wafer!



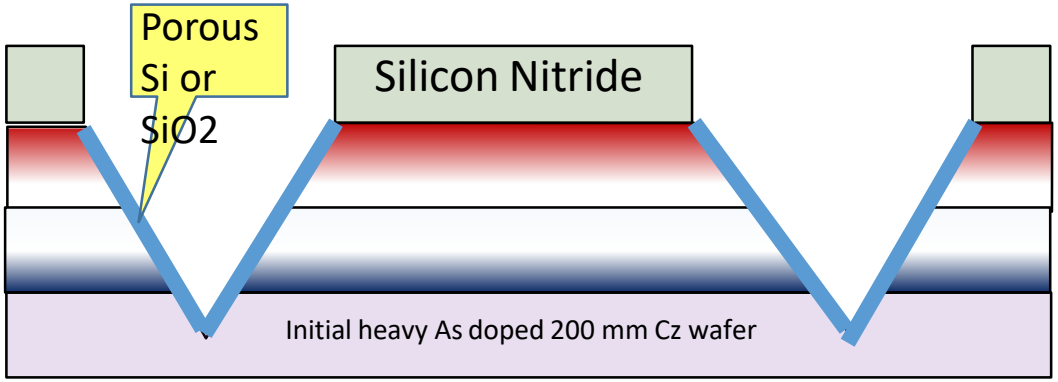
US Patent application 63/245778

Si3N4 mask deposition and patterning

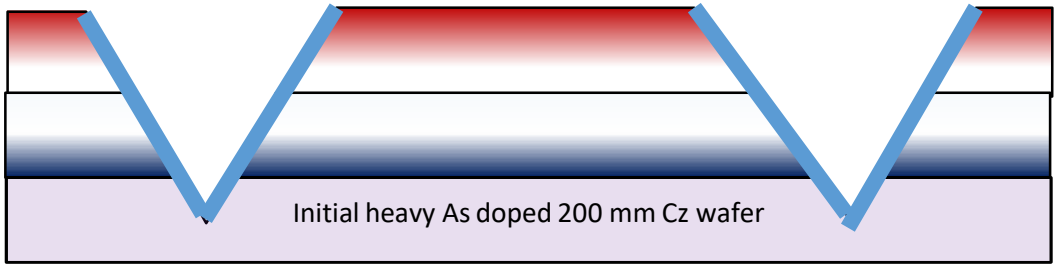
Anisotropic etch in TMAH

Process flow – part 2

No metallization yet, so we have opportunity to passivate diode side walls by oxidation

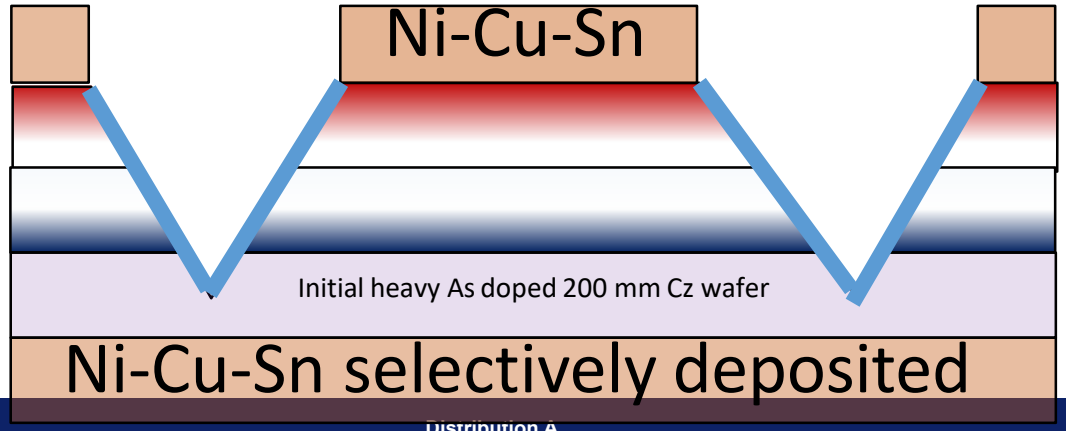


Stain etch or Oxidation



Strip nitride

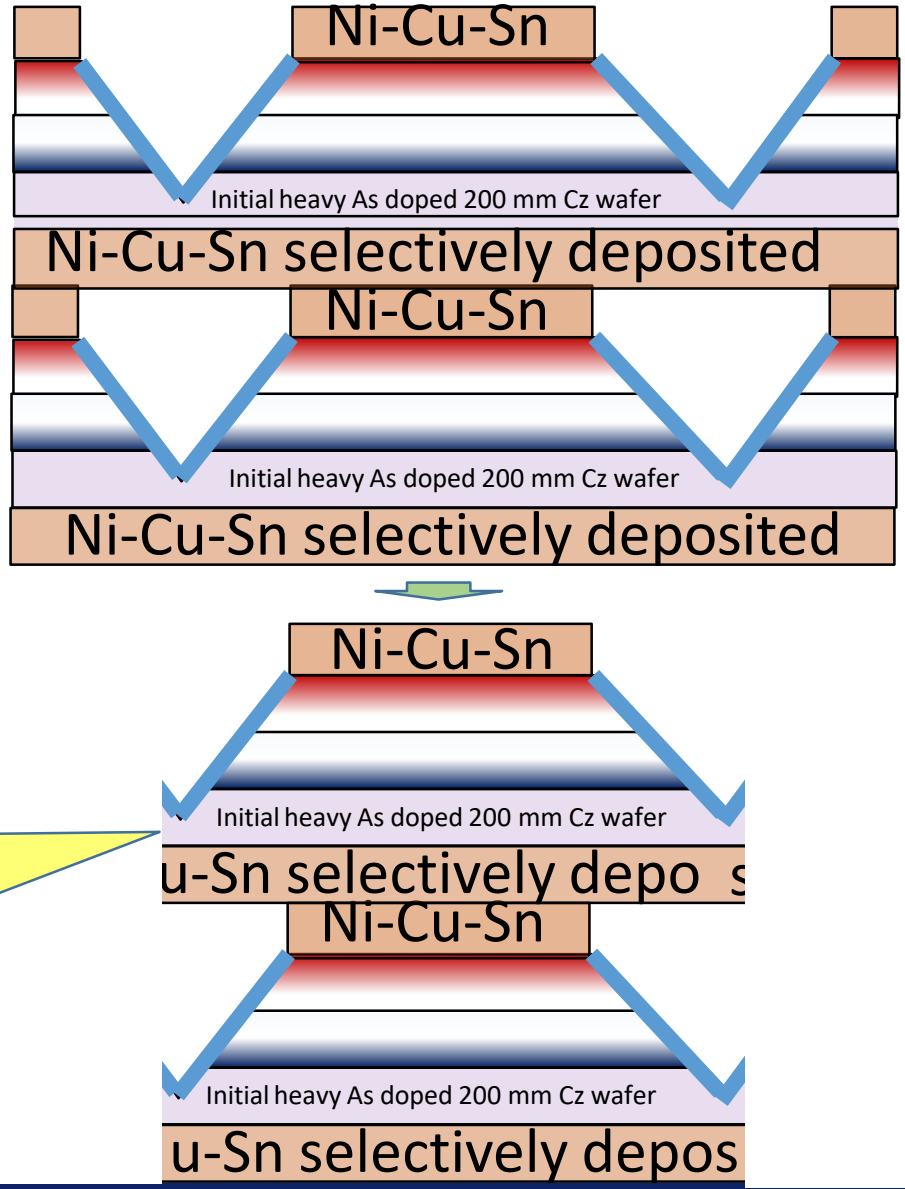
Ohmic contacts to all diodes on wafer. Nickel for adhesion to Si, Cu/Sn – for further bonding by intermetallic compound, no any solders



Selective Electroless deposition of Nickel, Copper, Tin stack

Process flow – part 3

By heating aligned wafer stack above Tin melting temperature, Cu_3Sn_5 intermetallic compound welds all wafers together



Bonding required number of wafers into stack

No need to protect or passivate the cut line sides - it is beyond of active area of diode

Dicing wafer stack into diode stack!

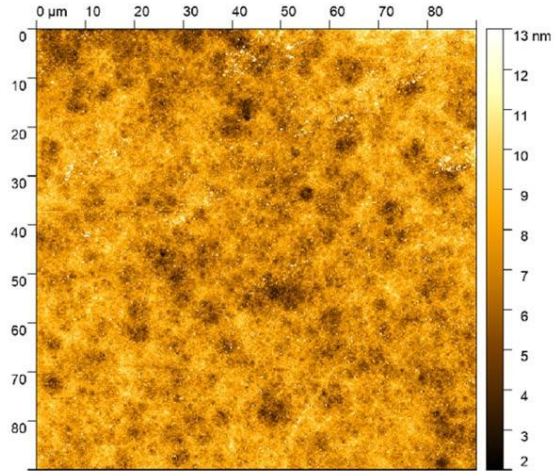
Results: Die Side Termination Step – slide 1

- **In the diode process flow we have replaced mechanical sawing by anisotropic etch. Reasons:**
  - Sawing leaves ~50 microns cracks in Si crystal. It needs further etching of the damaged Si. Etching is in HNA (HF:nitric:acetic mixture). HNA is undesirable being an autocatalytic (non-controllable) process.
  - Top and bottom of the die must be masked from HNA. HNA is extremely aggressive, only two materials can be used as the mask – black wax or gold. Black wax or gold is hard to selectively deposit
  - The anisotropic etch does not leave any cracks, it leaves a pristine <111> faceted Si surface.
  - Masking for anisotropic etch is easy – SiO_2 is OK, whether the etching is in KOH or in TMAH.
  - Competitors DSRDs all have mechanically sawed vertical die side wall, meaning low breakdown voltage due to surface breakdown
  - Anisotropic etch of <100> wafer gives 57° angle, thus improved breakdown voltage
  - Though the anisotropic etch using know recipes results in rough <111> surface
  - We have developed new etch recipe that result in very smooth Si surface.
  - The recipe is TMAH:water:DMSO; it is not known in the art
  - Next slide shows Si surface roughness comparison for traditional anisotropic etching recipe and our new recipe

Results: Die Side Termination Step – slide 2

- We have developed new anisotropic process recipe, with an intention to get a smooth etched surface (= higher breakdown voltage)
- AFM measurements confirms this, see below
- Rms roughness in the standard recipe is 271 nm (middle image) – more than 2 orders of magnitude higher then in our new recipe – 1.97 nm (left image)
- Etching rate is 1 micron/minute for the standard recipe, 0.5 micron/minute in our recipe and 0.1 micron/minute in TMAH:DMSO
- The drastic roughness improvement is due to fast release of hydrogen bubbles from Si surface. Square pyramids in the standard recipe are at places where the hydrogen bubbles (reaction byproduct) mask Si surface

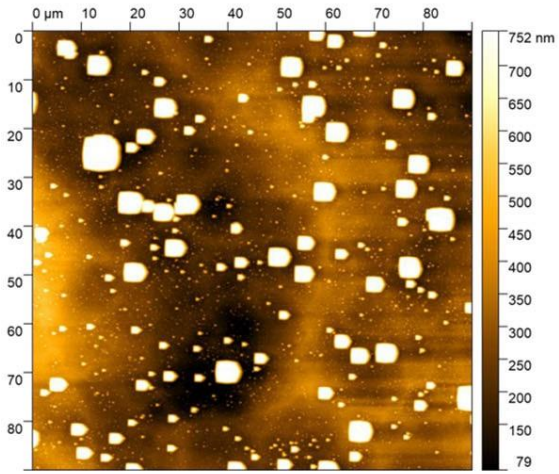
RDT6S1 TMAH:DMSO:DI



File: UMKC - 20220524 - 00048.nid

Average value: 7.61 nm
RMS roughness (Sq): 1.97 nm
Mean roughness (Sa): 1.15 nm

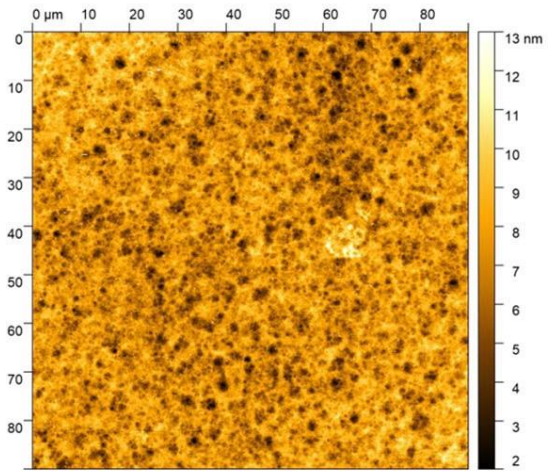
RDT6S2 DI:TMAH



File: UMKC-RDT6S2_20220601_00001.nid

Average value: 337 nm
RMS roughness (Sq): 271 nm
Mean roughness (Sa): 148 nm

RDT6S3 DMSO:TMAH

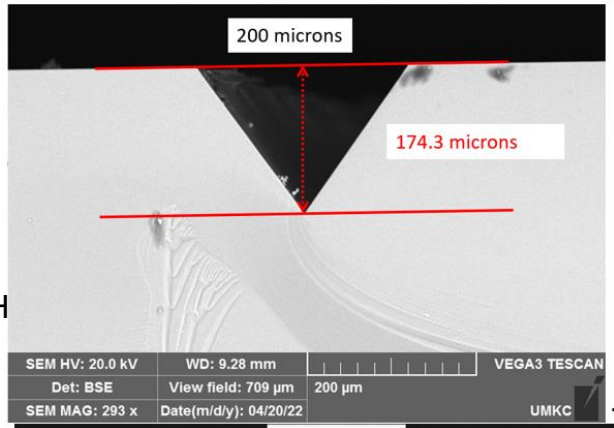


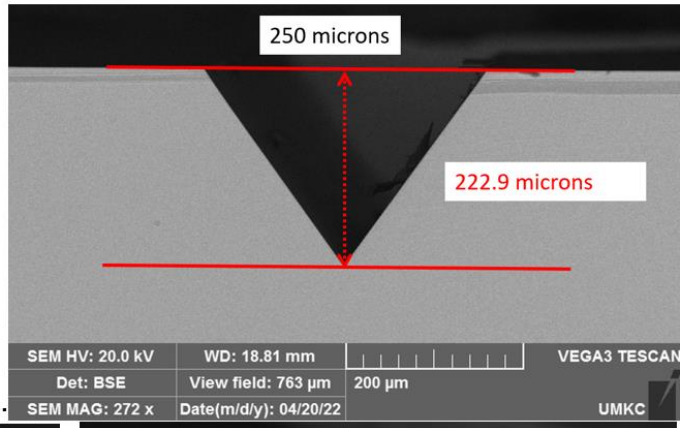
File: UMKC-RDT6S3_20220601_00004.nid

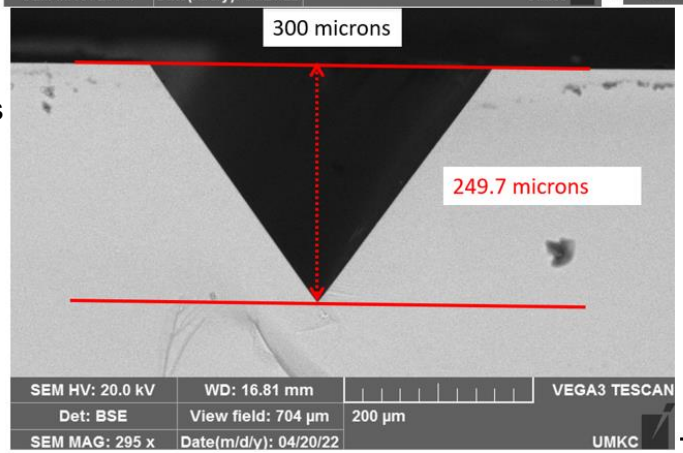
Average value: 7.27 nm
RMS roughness (Sq): 1.46 nm
Mean roughness (Sa): 1.10 nm

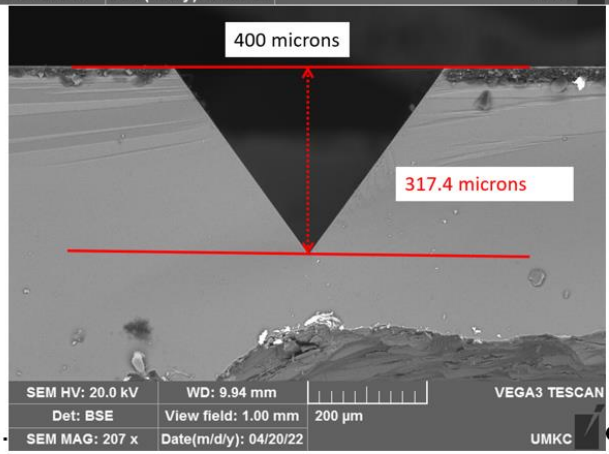
Results: Die Side Termination Step – slide 3

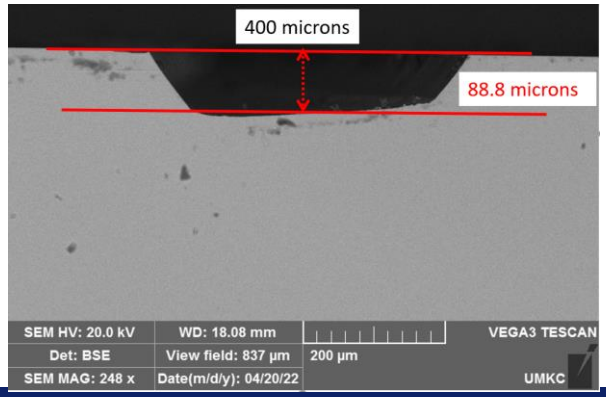
- Images to the right are SEM cross sections of the V-groves obtained by anisotropic etch through the mask with different widths of windows.
- The etching used our optimized new recipe TMAH:DMSO:water 1:1:2
- Image below shows V-grove shape etched in a standard recipe – 5% TMAH in water. The v-groove is truncated, which means the process fail.
- Images on the right shows near perfect triangle shape, no truncating for all window sizes. This means a wide window for the process specs variations and guarantees high yield.





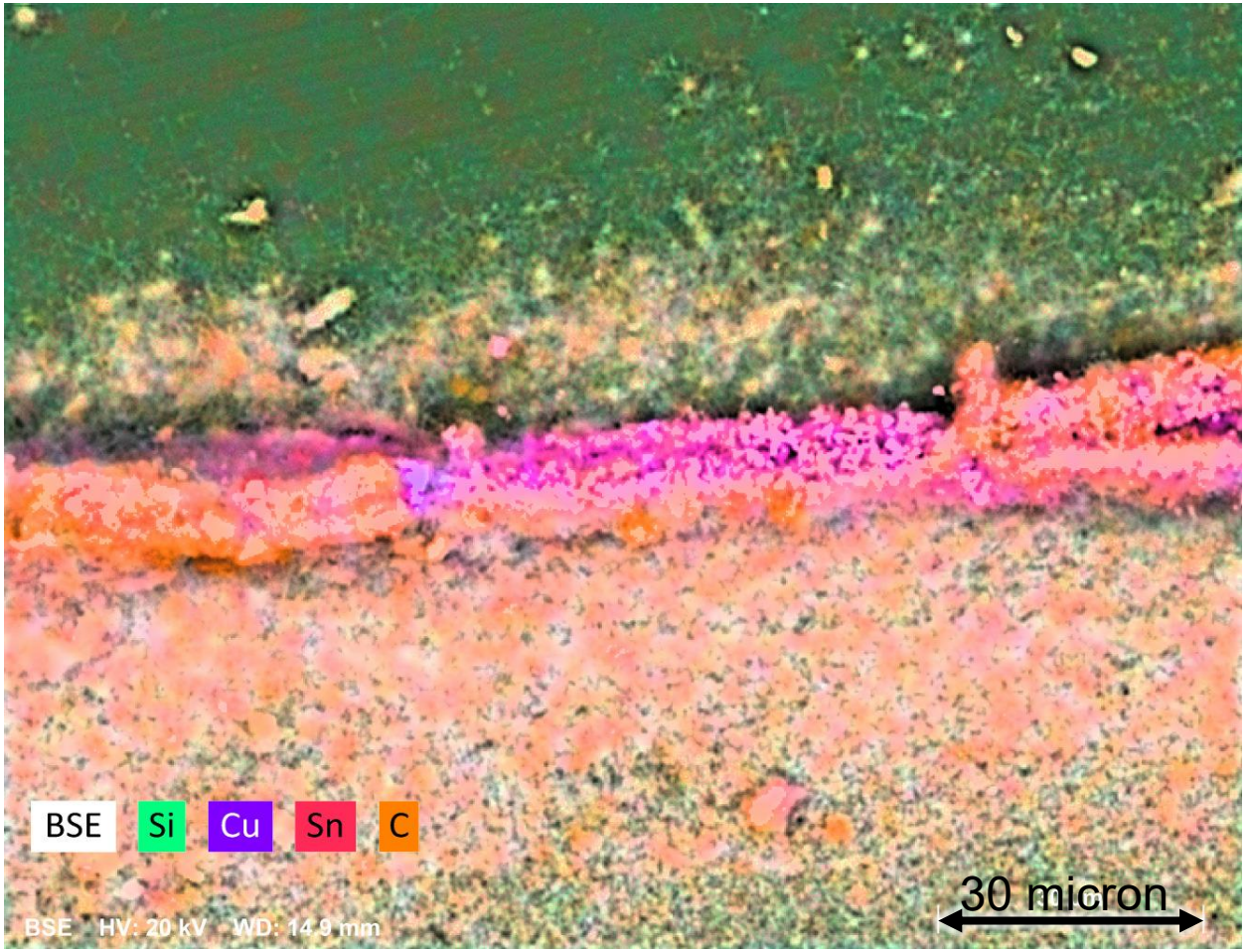






Results: Stacking Step

- In our process flow we use SLID (solid-liquid interdiffusion bonding) technology instead of traditional soldering or eutectic bonding
- We stack entire wafers instead off stacking individual dies, thus saving on the assembly operation.
- SLID uses copper and tin layers. When heated above the melting point of tin, CuSn intermetallic compound is formed having melting temperature about 550C thus making much more stable bond as compared to the traditional PbSn solder.
- Another advantage is that the CuSn layer is much thinner then PbSn. Therefore, the metal layer causes much lower mechanical shear stress. Eventually it improves reliability and service time of the stacked DSRD.
- Image on the right shows complete bonding with no voids between top and bottom Si dies. No blue color layer meand that entire Copper layer has been converted into the CuSn intermetallic compound. .



Outputs -2022

- **Patent applications**
- S.Bellinger, A.Caruso, A.Usenko, "Diode and Method of Making the Same" *US Patent Application (non-provisional) 17/855735* filed 06/30/2022.

- S.Bellinger, A.Caruso, A.Usenko, "Stacked Diode with Side Passivation and Method of Making the Same" *US Patent Application (non-provisional) 17/946022* filed 09/15/2022.

- **Conference Publications**
- A.Usenko, A.Caruso, S.Bellinger, S.Dhungana, R.Allen, "Improved Manufacturing Process for High Voltage Pulse Diodes" *Proceedings of The IEEE International Power Modulator and High Voltage Conference*, Knoxville, TN, June 19-23, 2022.

- A. Usenko, S. Dhungana, A. N. Caruso and S. L. Bellinger Electroless Nickel Plating for Ohmic Contacts to Silicon Power Devices, abstracts of 242nd Electrochemical Society Meeting, Oct.9-13, 2022, Atlanta, GA.

- **Conference Presentations**
- A.Usenko, A.Caruso, S.Bellinger, S.Dhungana, R.Allen, "Improved Manufacturing Process for High Voltage Pulse Diodes" *IEEE International Power Modulator and High Voltage Conference*, Knoxville, TN, June 19-23, 2022 (oral).

- A. Usenko, S. Dhungana, A. N. Caruso and S. L. Bellinger Electroless Nickel Plating for Ohmic Contacts to Silicon Power Devices, 242nd Electrochemical Society Meeting, Oct.9-13, 2022, Atlanta, GA (oral).

- **Conferences – submitted**
- A.Usenko, A.Caruso, S.Bellinger, S.Dhungana, R.Allen, "Adopting Processes from Mainstream Silicon Technology to Discrete Power Devices Technology" 2nd Annual Workshop on Solid State Devices and Applications for Directed Energy at GE Research in Niskayuna, NY, on October 26-28.

- S.Bellinger, A.Caruso, A.Usenko, "Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme" GOMACTech 2023, March 20-23, 2023 San Diego, CA USA

Outputs -2021

- **Patent applications**
- S.Bellinger, A.Caruso, A.Usenko, “Diode and Method of Making the Same” US Provisional Patent Application 63/216,550 filed June 30, 2021..

- S.Bellinger, A.Caruso, A.Usenko, “Stacked Diode with Side Passivation and Method of Making the Same” US Provisional Patent Application 63/245778 filed 09/17/2021

- **Conference Publications**
- Usenko, Alex, Anthony N. Caruso, and Stteven L. Bellinger. "Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme." ECS Meeting Abstracts. No. 31. IOP Publishing, 2021.

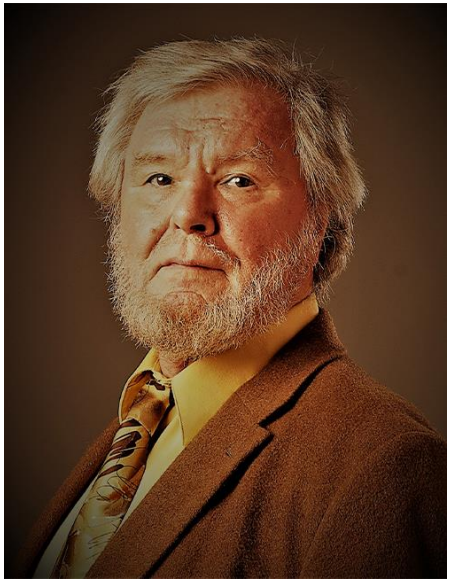
- A. Usenko, S. Dhungana, A. N. Caruso and S. L. Bellinger Electroless Nickel Plating for Ohmic Contacts to Silicon Power Devices, abstracts of 242nd Electrochemical Society Meeting, Oct.9-13, 2022, Atlanta, GA.

- **Conference Presentations**
- S.Bellinger, A.Caruso, A.Usenko, “New Paradigm on Making Semiconductor Opening Switches for Pulsed Power” oral presentation (virtual) at 2021 23th IEEE Pulsed Power Conference, Dec. 12-16, 2021, Denver, CO.
- S.Bellinger, A.Caruso, A.Usenko, “Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme”, at 240th Electrochemical Society Meeting, Oct. 10-14, 2021, Orlando, FL – oral (online) presentation
- G. Bhattarai, J. Eifler, S. Roy, M. Hyde, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “All Solid-State High-Power Pulse Sharpeners” (Poster)
- J. Eifler, S. Roy, M. Hyde, G. Bhattarai, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “TCAD Optimization of Epitaxially Grown Drift-Step Recovery Diodes and Pulser Performance” (Poster)
- M. Hyde, J. Eifler, S. Roy, G. Bhattarai, A. Usenko, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Development of an Evaluation Network for Drift Step Recovered Diodes through and Augmented Design of Experiment” (Poster)
- D. F. Noor, J. Eifler, M. Hyde, G. Bhattarai, S. Roy, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “DSRD-IES Pulsed-Power Generator Topology Study Using Machine-Learning-Based Feature Selection Optimization and Predictive Learning” (Poster)
- S. Roy, J. Eifler, M. Hyde, G. Bhattarai, D. Noor, J. Bhamidipati, A. Usenko, M. Pederson, M. Paquette, A. Caruso, S. Bellinger, L. Voss, and R. Allen, “Systematic Topological Optimization of DSRD-Based IES Pulse Generator” (Poster)

Personnel

Diode manufacturing sub-team

Many other people at MIDE and at subcontractors were involved



Alex Usenko
Research Professor
MIDE



Shailesh Dhungana
Postdoc
MIDE



Steven Bellinger
President
Semiconductor Power Technologies



Neal Strathman
Technician
Semiconductor Power Technologies

Summary

- **Novel manufacturing technique for DSRDs has been developed**
- **A lot of DSRDs Gen2 have been fabricated**
- **Testing of devices from a finished Gen2 lot shown better pulsed performance compared to DSRDs manufactured by competitors**
- **Manufacturing of next Gen3 lot continues**
- **Process for Gen3 being patented**
- **Brief comparison of our process to state-of-the-art process:**
  - For doping: diffusion replaced by graded epitaxy – resulting in optimal doping profile
  - For stacking: eutectic bonding replaces by intermetallic – exclude failures due to thick metal
  - For side termination: sawing replaced by anisotropic etch – increases breakdown voltage
  - For side passivation: polymer coating replaced by stain etch – better yield/cost
  - For metallization: blank deposition replaced by selective one – cost saving and higher yield

Recommendations & Future Work

- **Our novel process integration scheme is developed for a specific niche device – DSRD, as this device is relevant to OSPRES goals. However, this process flow can be used for much wider class of discrete silicon power diodes – SAS (silicon avalanche shaper) and TVS (transient voltage suppressor).**
- **Under PTERA program we will develop technologies and optimize process recipes for individual steps of our novel integration scheme.**
- **Upon issue of patents, we will be ready to license our process and know how to trusted foundries.**

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for c-sUAV Study (OSPRES Grant)

N00014-17-1-3016
09/30/2017-09/29/2022

Design Considerations for PCSS

Heather Thompson, John Bhamidipati, Jay Eifler, Michelle Paquette & Anthony Caruso

J.Bhamidipati@umkc.edu*

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Optical Switch Team - UMKC

Current:

Eifler



Post-Doc

Bhamidipati



PhD Student (graduated)

Kramer



PhD Student/Staff

Thompson



PhD Student

Former:

Meyer



Staff

Fry



Undergrad Student/Staff (graduated)

Labrada



MS Student (graduated)

Utt



Undergrad Student (graduated)

OSPRES Mission

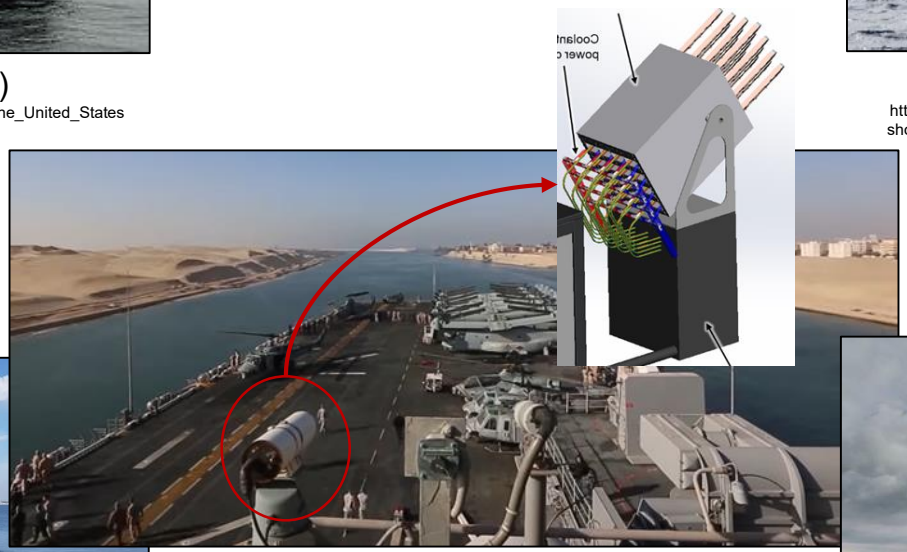


Sea Fighter (FSF-1)
https://en.wikipedia.org/wiki/List_of_current_ships_of_the_United_States_Navy

Navy need for cUAV defense systems that are cost effective and provide a small form-factor.



USS Henry M. Jackson
https://www.military.com/daily-news/2020/10/23/video-shows-us-navy-experimenting-drones-make-deliveries-submarine.html





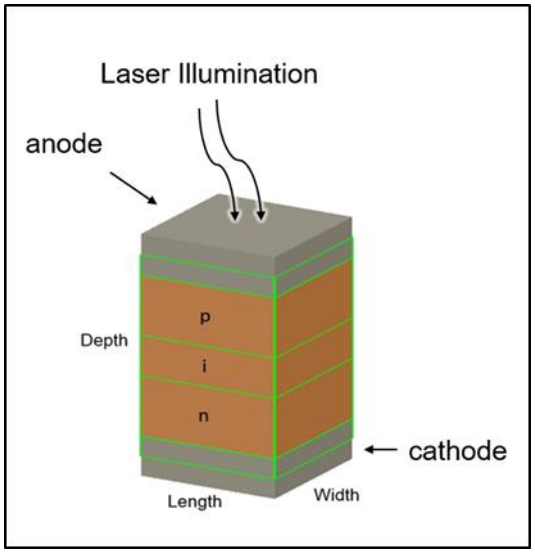
Counter Drone System
https://defense-update.com/20191025_repmus19.html



N-AUDS – Naval/Maritime Defense
https://liteye.com/products/counter-uas/

Photoconductive Semiconductor Switch (PCSS)

PCSS is used as a source driver to convert voltage/current pulses into RF frequency for EM transmission.



PCSS is a PIN diode using the photoconductive property of semiconductors.

Some Considered Technologies for OSPRES

Si PCSS
- Cost Effective
- Med. Laser Requirements



SiC PCSS
- Direct RF
- High Thermal Conductivity
- High Voltage



GaN PCSS
- Increased Efficiency
- High Voltage
- Higher operating temp.



DSRD
- No Laser
- Simplified Operation



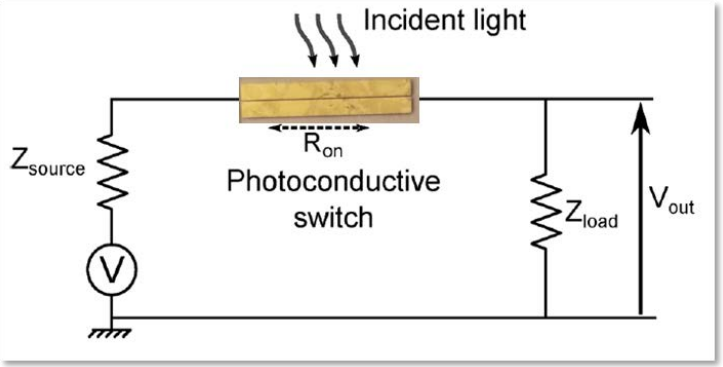


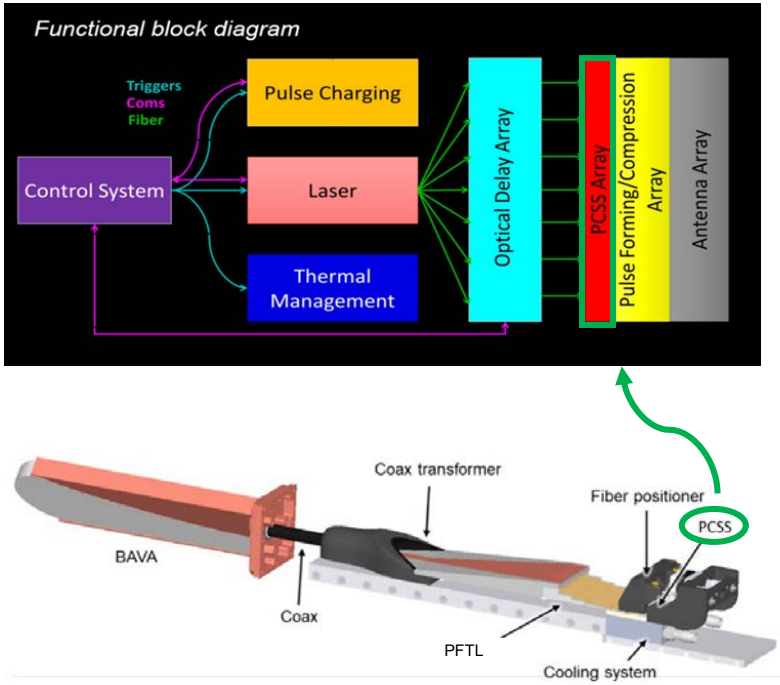
7cm *0.5cm Si-PCSS

Why PCSS?

Benefits of PCSS:

- Isolation of control circuits
- Compact form factor
- Low switching jitter
- Sub-ns rise and fall times



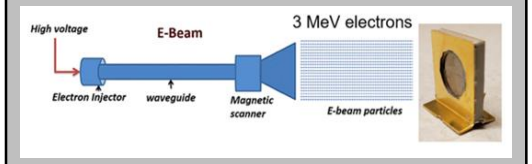


Targets for RF Generation:

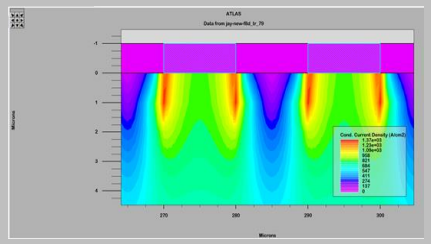
- On-state resistance of <1Ω
- Shot lifetime of >$1*10^9$
- Hold off voltage > 10 kV
- Peak pulse power of > 3 MW
- Recovery time < 500 ns
- Pulse width 1-10 ns
- Switching efficiency > 50%

Outline

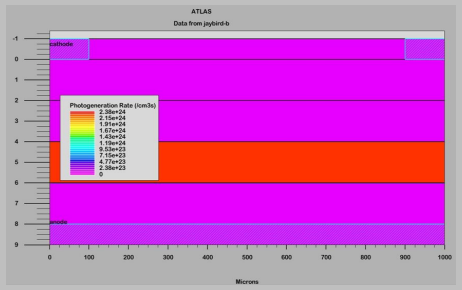
Lifetime Killing in Si PCSS



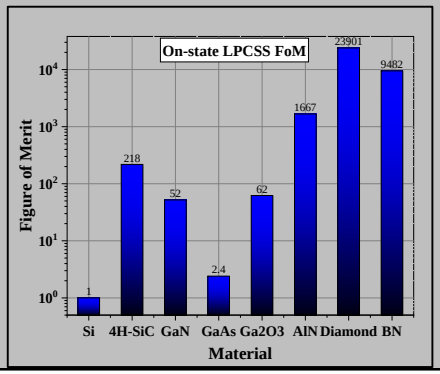
Si PCSS Top Contact Optimization



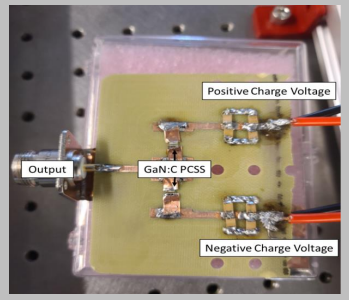
SiC Optical Thyristor



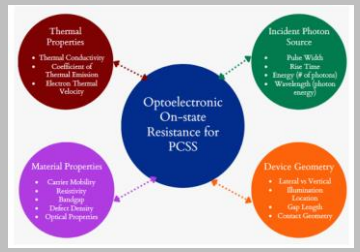
FOM for PCSS



GaN PCSS Direct RF Modulation

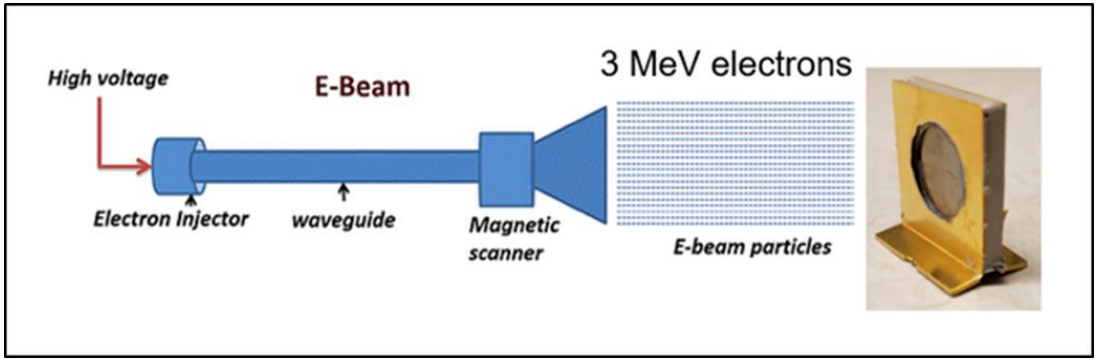


GaN PCSS Minimizing On-state Resistance

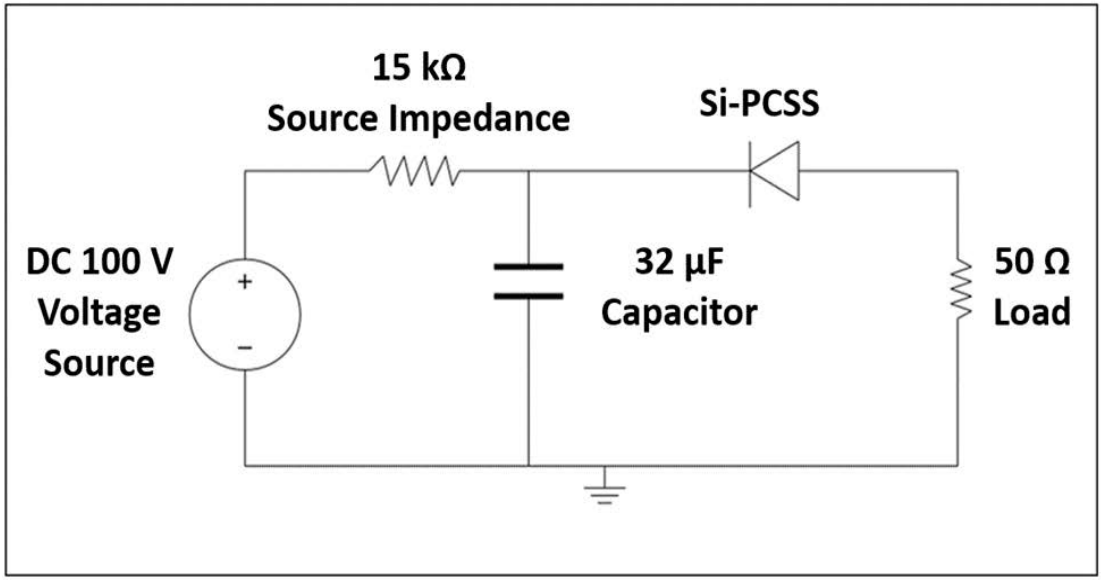


Lifetime Killing in Si PCSS: Background

Enabling higher pulse repetition rates, decreasing switching losses and increasing energy efficiency through reduction of carrier lifetime using electron irradiation.



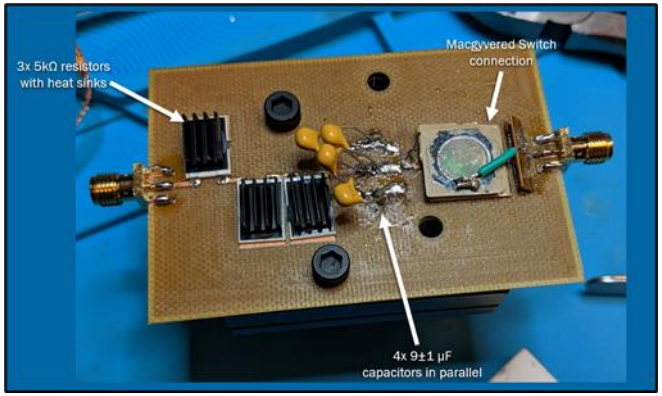
- To enable high pulse repetition rates (PRR) up to 1 MHz, recovery times <1 μs are required
- Electron irradiation cheaper than other irradiation methods
- TCAD simulations are performed in capacitive discharge circuit (at right) for recovery times

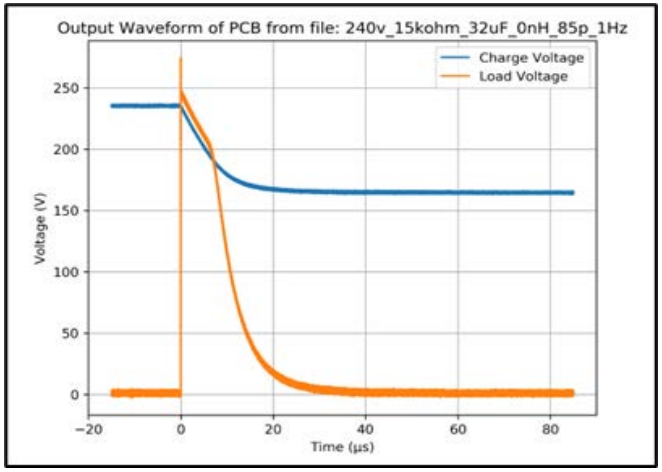


Lifetime Killing in Si PCSS: Simulation Details

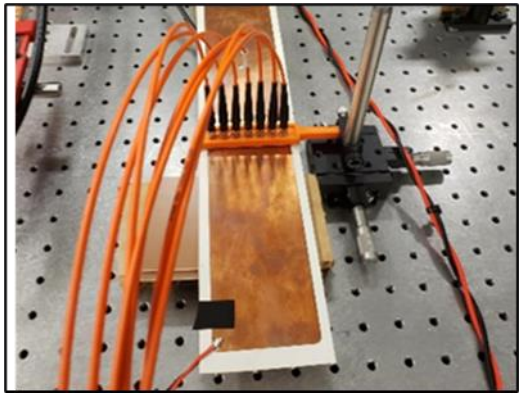
- Due to TCAD computational limitations a capacitor rather than transmission line (TL) discharge is used
- We study photo-illuminated recovery by discharging a capacitor through the switch into a load
- Ultimately interested in pulse forming network incorporating transmission lines (TL)

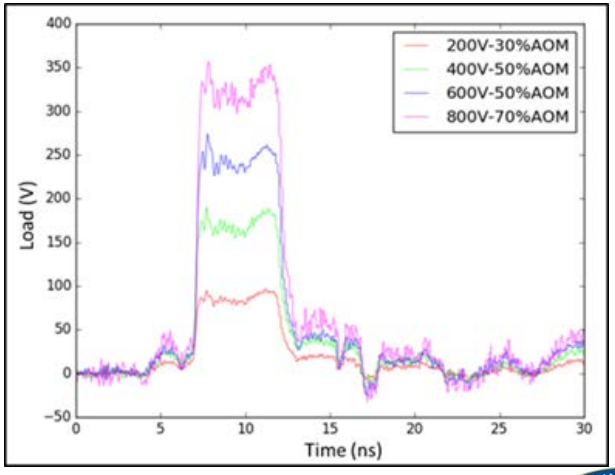
PCB Capacitive Test Circuit with Si-PCSS





Si-PCSS integrated into TL



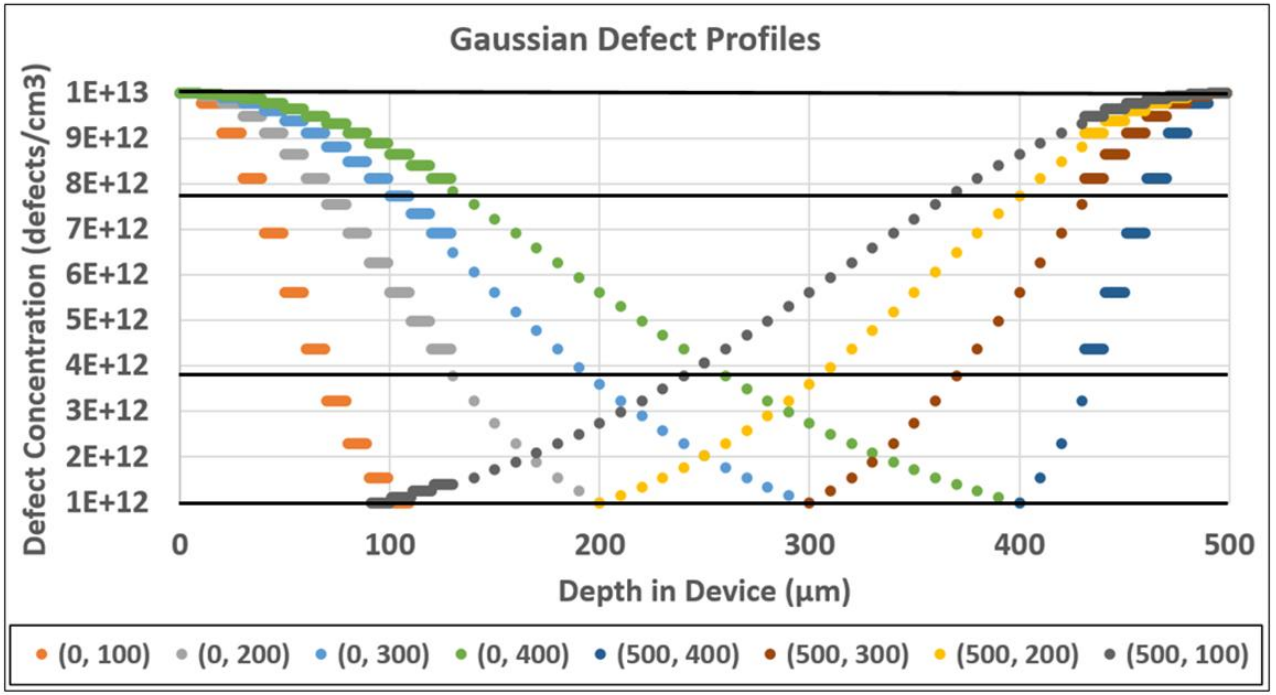


Lifetime Killing in PCSS: Defect Profiles

- Uniform and sloped defect profiles from electron irradiation are simulated
- ~3 MeV electrons produce uniform defect profiles
- Lower energy electrons (270 keV-700 keV) produce sloped defect profiles

Uniform Defect Profile Concentration (defects/cm^3)
No Defects
1.0×10^{12}
3.9×10^{12}
7.8×10^{12}
1.0×10^{13}
1.0×10^{14}
1.0×10^{15}

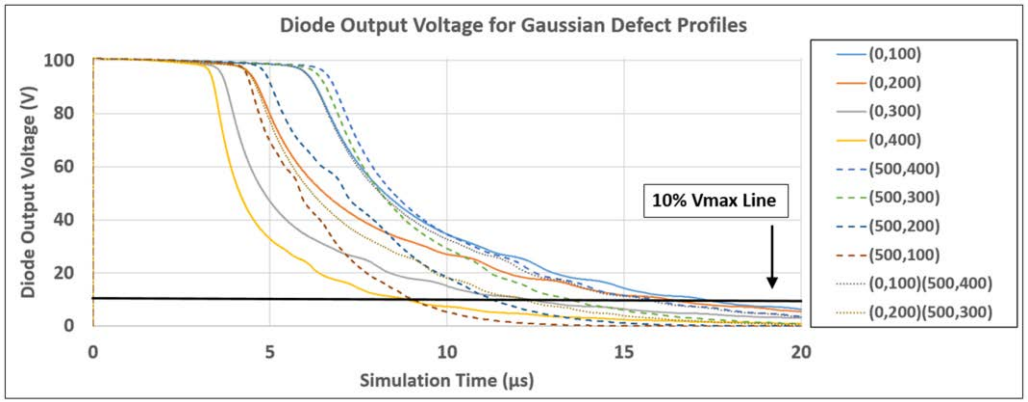
Gaussian Defect Profile Depths (μm)
(0,100)
(0,200)
(0,300)
(0,400)
(500,400)
(500,300)
(500,200)
(500,100)
(0,100) (500,400)
(0,200) (500,300)

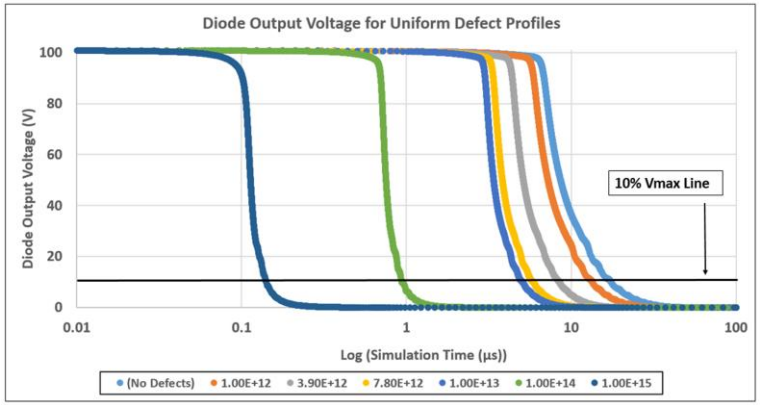


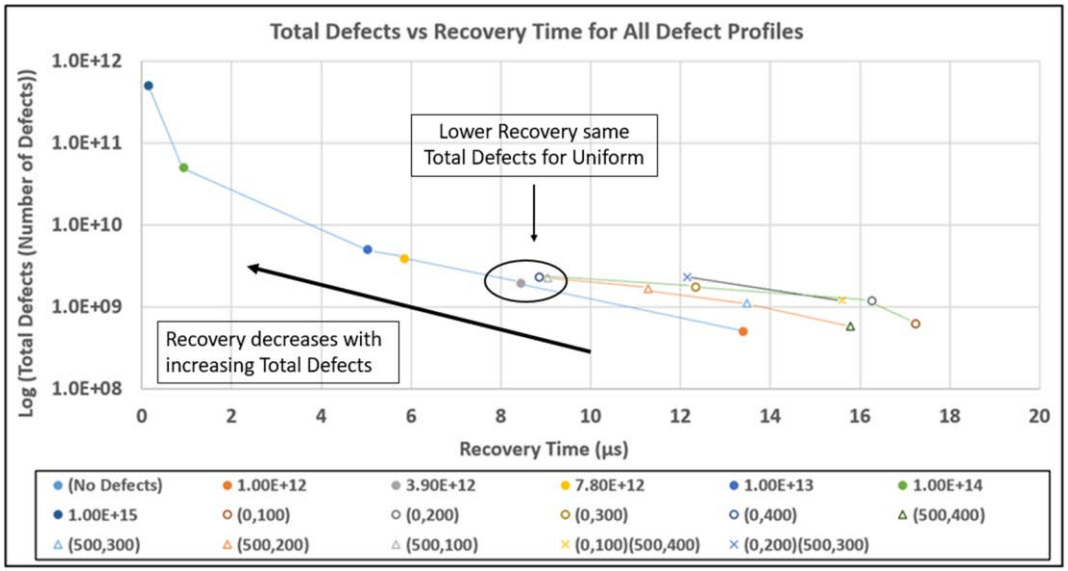
Gaussian profile key guide: (0, depth) or (500, 500 - depth)

Lifetime Killing in Si PCSS: Results

- Uniform and sloped defect profiles reduce recovery time near equally based on the total number of defects
- Uniform defect profiles can have more total defects and reduce recovery time more
- Recovery time set to 10% Vmax of pulse







TCAD simulation showed increased defects (thus increased irradiation dose) produced larger recovery time reduction than initially expected, therefore dose was increased from 10 MRad to 20-40 MRad resulting in decreased recovery times

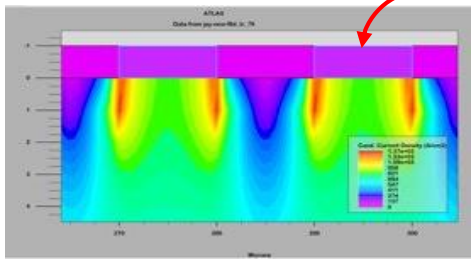
Future Work:

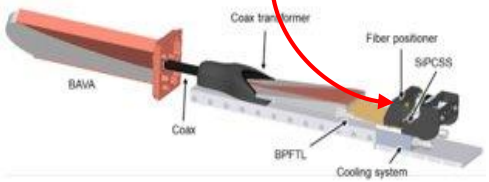
- Using TCAD simulation compare switching losses between uniform and sloped electron irradiation defect profiles
- Compare uniform, sloped and combinations of uniform and sloped defect profiles

Si PCSS Top Contact Optimization: Background

By optimizing PCSS top contact geometry, reduction in laser energy for minimizing on-state resistance (R_{on}) can be achieved, thus helping meet OSPRES laser SWaP-C² objective.







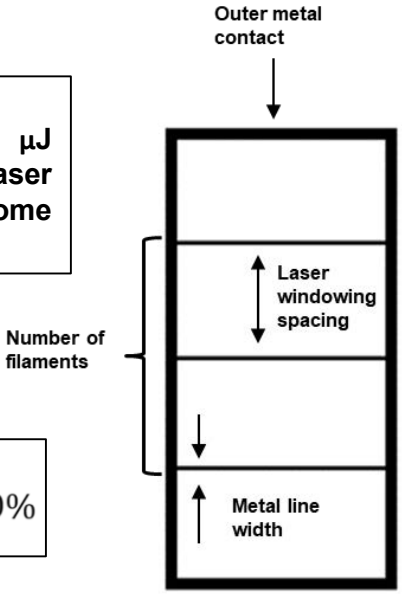
Criteria/Metrics for HPM Source Improvement

Quantitative Criteria/Metric	Representative Values
Percent laser energy reduction	10% - 30%
Laser energy difference at fixed R_{on}	< 30 µJ
Laser windowing spacing	10 µm - 1000 µm
Metal line width	10 µm
Number of filaments	< 1000s
Incident laser energies	1 µJ – 1000 µJ
On-state resistance (R_{on})	< 1 Ω

Research Parameter/Metric Context Description:

1. **Percent laser energy reduction (E_{per}):** E_{20} is the laser energy at some R_{on} for 20 µm spacing, E_{wid} is wider spacing energy required at same R_{on}, positive percent gives reduction
2. **Laser energy difference at fixed R_{on} (ΔE_{Ron}):** the numerator in E_{per} equation, necessary to compare at one R_{on} value which necessitates two laser energies and therefore a difference, not constant across R_{on} as with E_{per}
3. **Laser windowing spacing:** gap between metal filaments crossing the length of the switch to let in laser light, metal width limited by cost of manufacturing
4. **Incident laser energies:** 50 µJ – 100 µJ, stable and deliverable to switch
5. **On-state resistance:** subohm, depends on load resistance for PFN efficiency, static resistance of PCSS after laser illumination until charge storage time

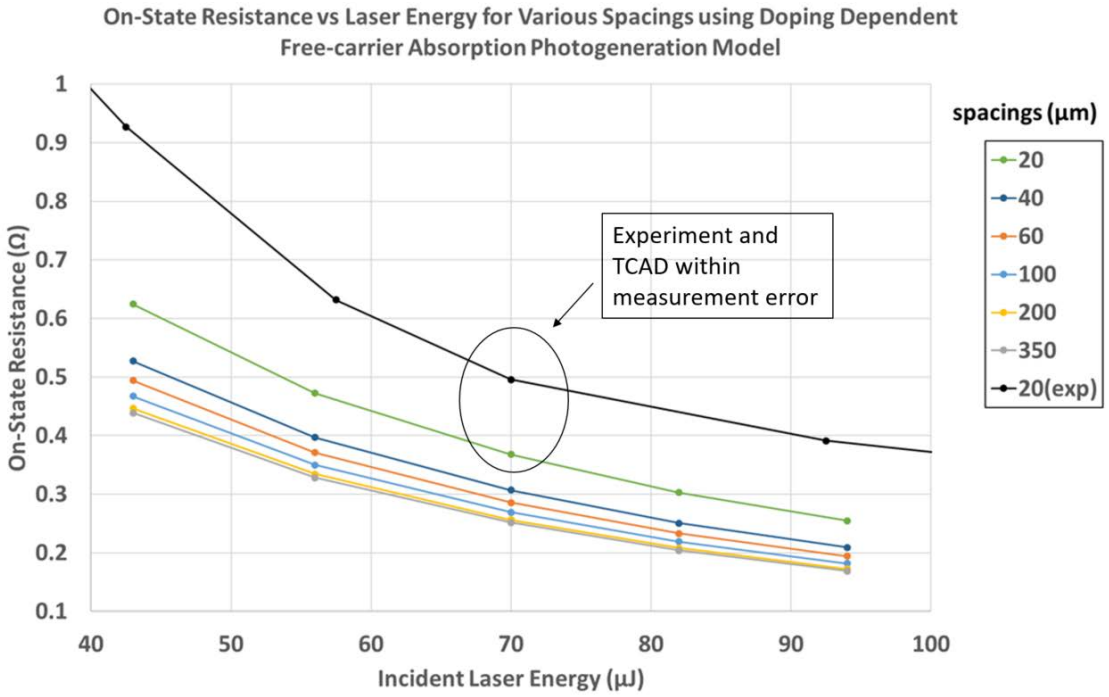
For example:
30% reduction using 100 µJ laser energy gives 30 µJ laser energy reduction (for some R_{on} and spacing)



$$E_{per} = \frac{E_{20} - E_{wid}}{E_{20}} * 100\%$$

Si PCSS Top Contact Optimization: Results

Impact on Switch/Laser Requirements



- R_{on} is the critical parameter for PCSS efficient and intended operation in the BPFTL
- Ratio of load resistance and R_{on} is a major determiner of efficiency for the HPM system

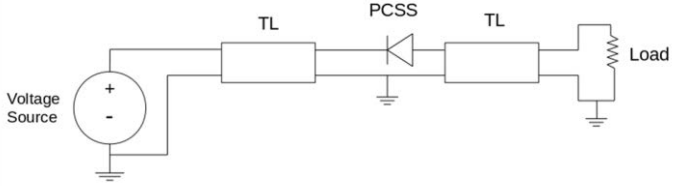
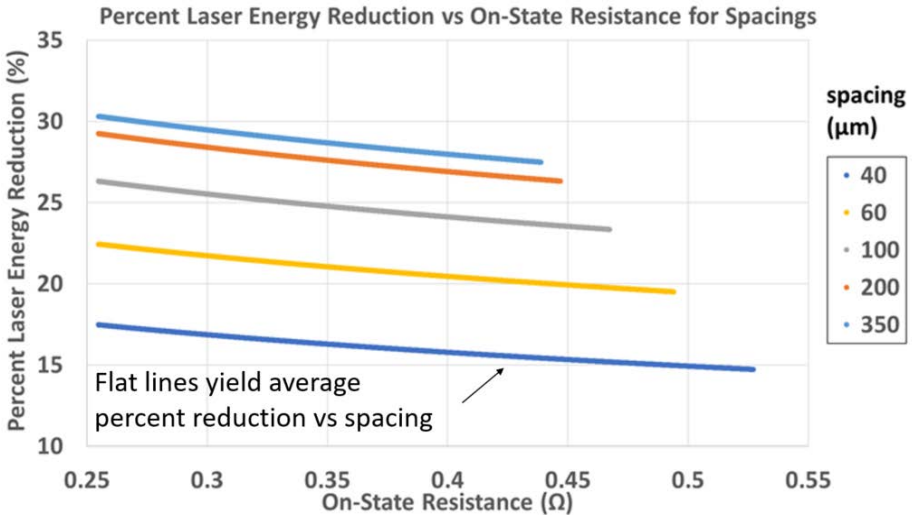
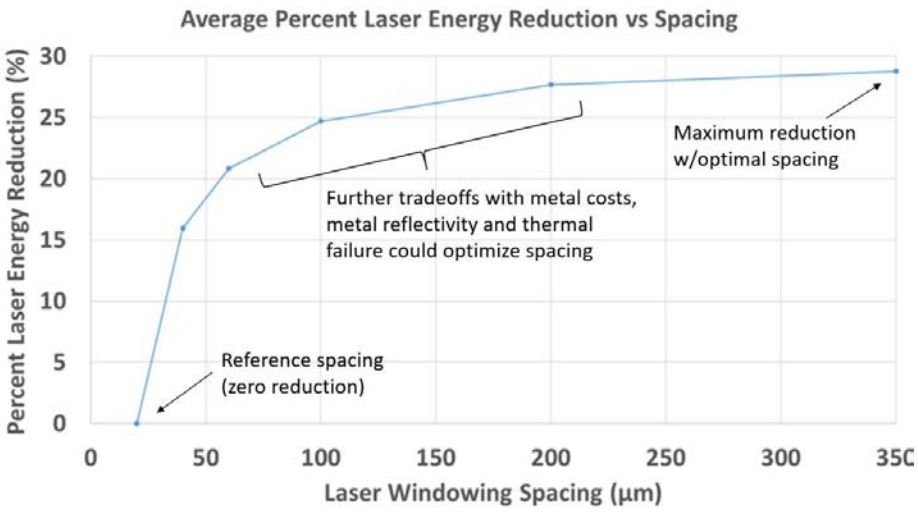


Figure 1: Schematic of PCSS circuit

- Can visually inspect spacing curves at fixed R_{on} for laser energy differences
- These spacings manufactured into 1 cm and 7 cm Si-PCSS switches at RDT (testing and sim/exp comparison forthcoming)

Si PCSS Top Contact Optimization: Results





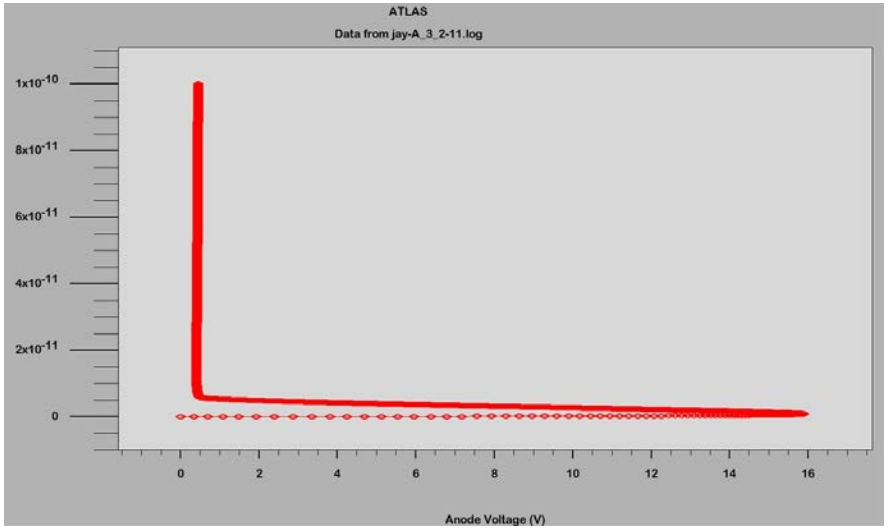
- Percent reduction vs R_{on} calculated from power law interpolation of R_{on} vs laser energy (previous slide)
- Larger than 350 µm spacing percent reduction decreases, overlapping smaller spacings
- Relatively flat percent reduction across Ron obtained using realistic laser energies (40 µJ – 100 µJ)

- **Maximum possible reduction was 28.8% at 350 um spacing**
- Thermal failure due to spot heating near contacts due to high current density leads to additional cooling requirement (push spacing lower)
- Cooling and laser requirements can be considered together for optimal spacing using thermal TCAD solutions
- Metal costs and metal reflectivity push spacing higher

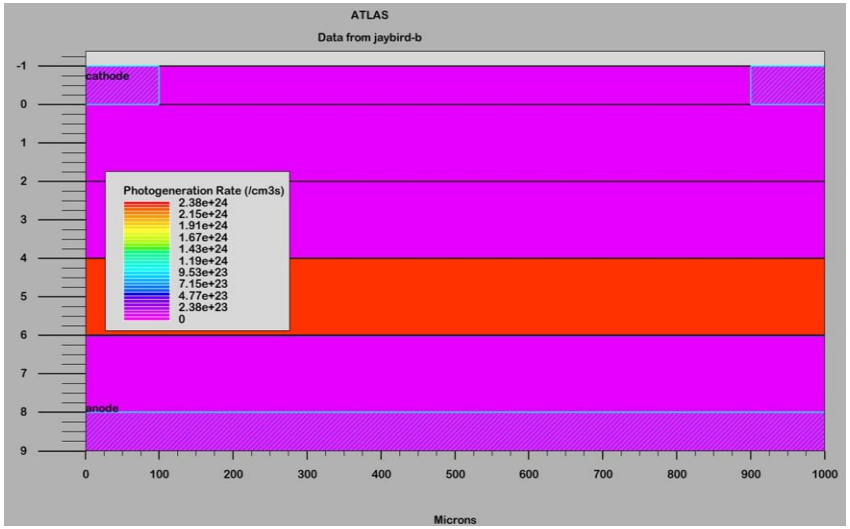
SiC Optical Thyristor: TCAD Feasibility

Optically initiated SiC thyristors can produce fast current rise-rates by eliminating the current spreading delay of conventional thyristors and when stacked hold high-voltages to overcome the limitations of available PN diode and thyristor technology for pulsed power applications

Conventional DC IV of Thyristor in TCAD



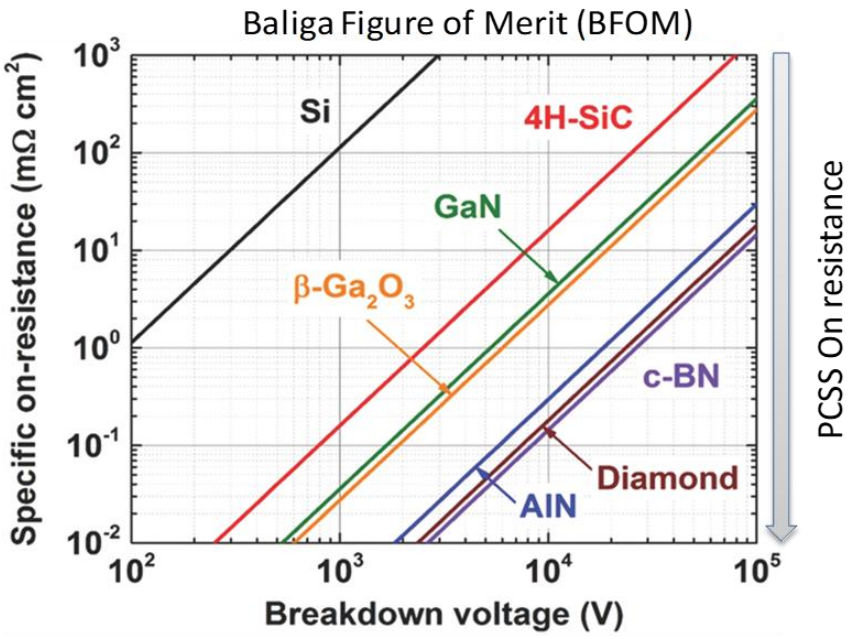
Optical Absorption of 532 nm Light in P-doped Layer



- Encountered numerous difficulties in simulating optical thyristor in TCAD even though published examples sist of light triggered thyristor.
- SiC parameters inaccurate in TCAD.
- Mixed-mode to allow external circuitry did not converge properly.
- With improved SiC models (especially Vanadium compensated SiC), communication with TCAD vendor, and more simulations, SiC optical thyristor TCAD simulations should be possible demonstrating known action.

FOM: Background and Approach

Figure of Merit (FOM):
A numerical expression representing the performance or efficiency of a given device, material, or procedure.



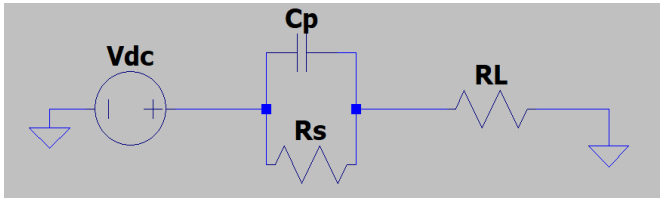
Advanced Electronic Materials, Volume: 4, Issue: 1, First published: 04 December 2017, DOI: (10.1002/aelm.201600501)

Limitations of existing FOM:

- Previous FOM exclusive to electrically triggered devices
- Omission/misinterpretation of key factors that determine performance
- Emphasis on engineering point-of-view
- No intersection with PCSS devices

Trade-off between V_{BD} and $R_{on\text{-}sp}$

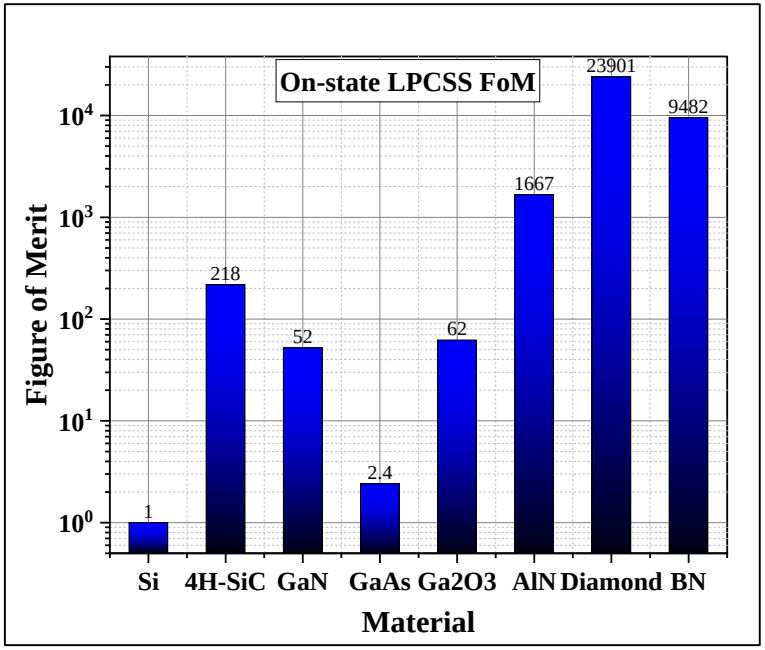
PCSS breaks trade-off

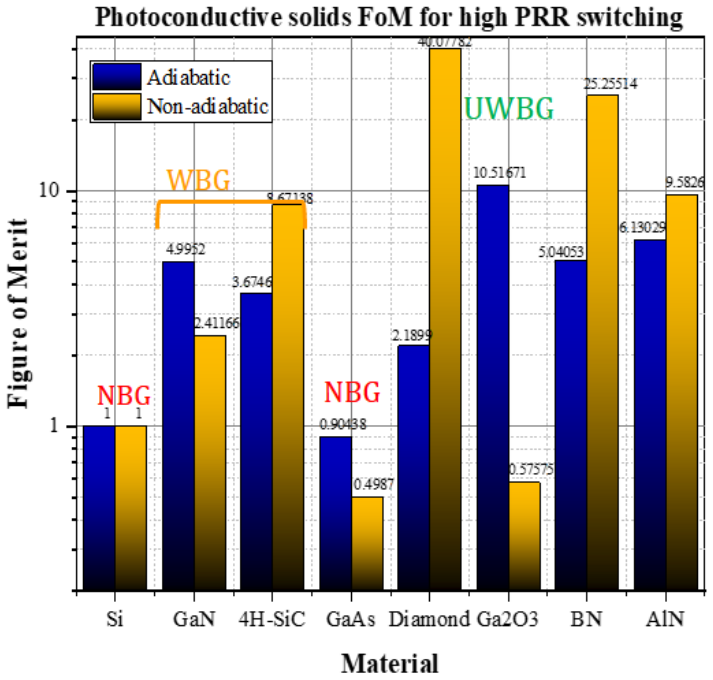


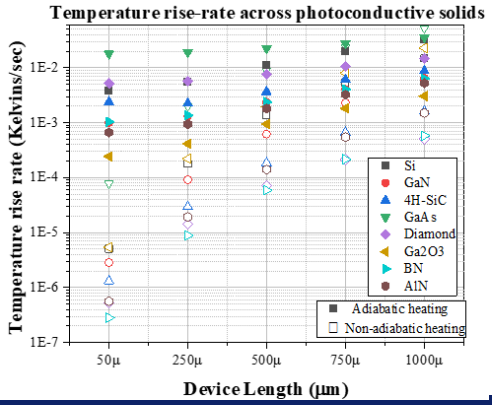
PCSS equivalent circuit (includes internal resistance and parasitic capacitance)

FOM: Results

$$\text{On-state FOM} = \frac{E_C^2 E_g \eta t_r k_{th}}{h\nu}$$







Nonadiabatic temperature change: $\Delta T = \frac{Q}{t}\frac{d}{kA}$

Adiabatic temperature change : $\Delta T = \frac{Q}{mC}$

Q - heat dissipation rate, C - material's specific heat and m-mass (density and volume dependent), ΔT- temperature change, $\frac{Q}{t}$ –heat-dissipation rate , k - thermal conductivity of the material (Watts/m-K), A - surface area and d-device thickness.

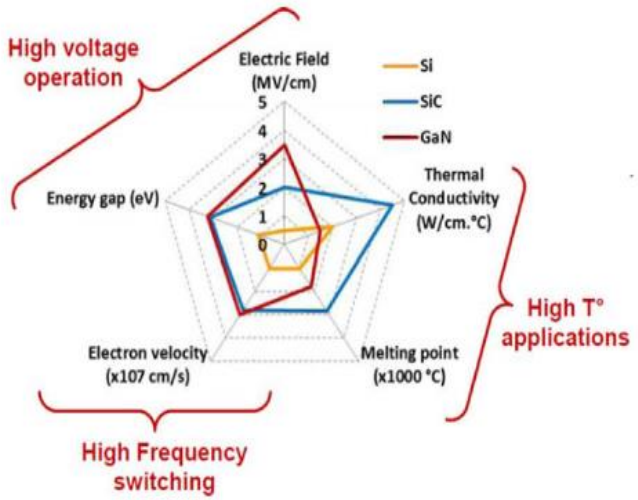
Takeaway:

At 50 kHz PRR under adiabatic conditions, Ga_2O_3 and GaN performed the best in UWBG and WBG solids, respectively.

However, under non-adiabatic conditions, diamond and SiC were found to perform better than others

Does not include cost and size considerations.

GaN:C PCSS: Background



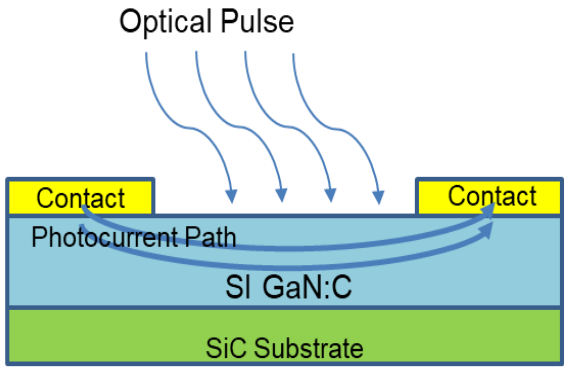
https://digitalrepository.unm.edu/cgi/viewcontent.cgi?article=1439&context=ece_etds

Alternative PCSS material for compact cUAV systems with greater efficiency and power handling.

GaN:C benefits:

- Electric field breakdown → higher operating voltage
- Increased electron velocity → increased switching frequency
- High temperature operation
- Enables smaller, thinner devices with higher efficiency than Si or GaAs
- ns-order recovery

Lateral PCSS Schematic

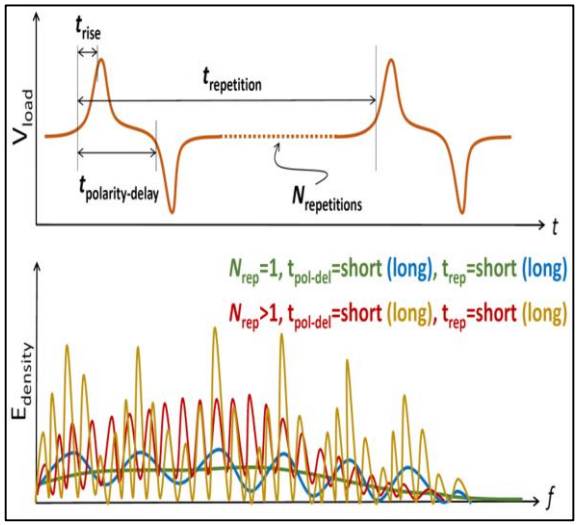


Parameter	SOTA (Si-PCSS)	Proposed (GaN:C-PCSS)	Parameter Description
Breakdown Field (V/cm)	$3*10^5$	$3.3*10^6$	N/A
Cooling System Capacity (W/cm^2)	500	250	Based on current cooling requirements of Si-PCSS
Incident Energy per Output Power (μJ/MW)	25	6.67	Incident laser energy as a function of PCSS output power, based on 4 MW output
Device Area (cm^2)	1-7	<1	Based on current OSPRES PCSS devices
Operating Temperature (°C)	<160	500	Operating temperature for GaN:C PCSS will be limited based on PCB components
Recovery time	μs Scale	ps - ns Scale	Recovery time for GaN:C is laser and material dependent
Saturation Velocity (cm/s)	$1*10^7$	$2.5*10^7$	N/A
Max Operating Frequency (GHz)	3.8	>12	N/A

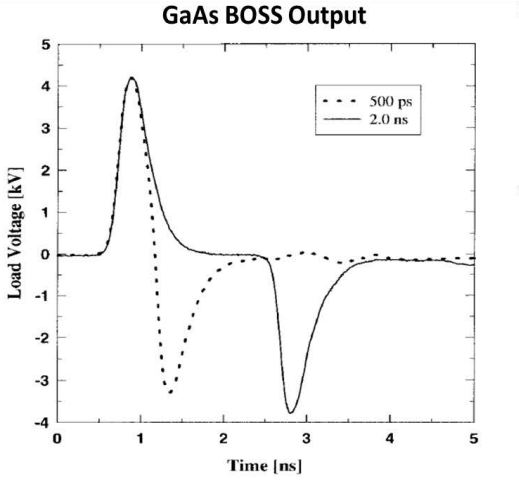
GaN:C PCSS Direct RF Modulation: Background

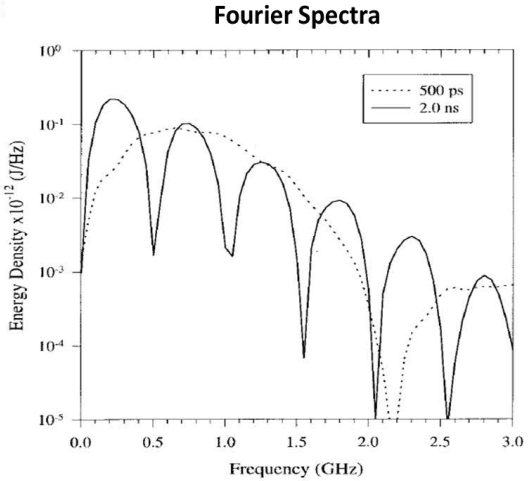
Reduction in cUAV system size by eliminating pulse-forming transmission lines and offering frequency agility.

Methods of direct RF Modulation



Direct RF Modulation Using GaAs





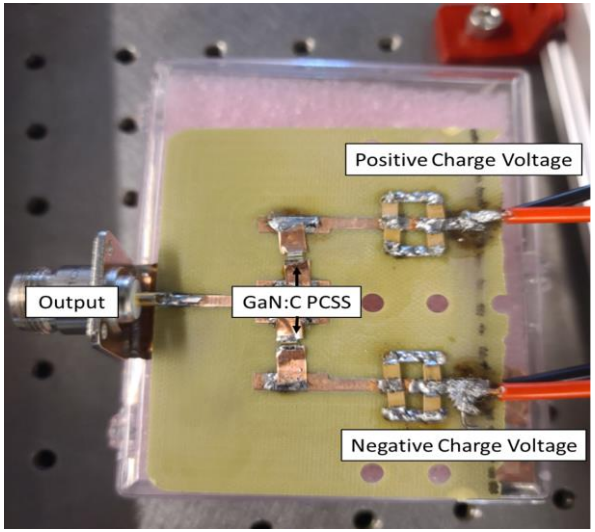
Stoudt, D. C., Richardson, M. A., & Peterkin, F. E. (1997). Bistable optically controlled semiconductor switches in a frequency-agile RF source. IEEE Transactions on Plasma Science, 25(2), 131–137. https://doi.org/10.1109/27.602483

Output can be altered by changing incident photon source rise time, pulse width, and time delay between pulses.

In literature, direct RF Modulation successfully demonstrated using GaAs PCSS.

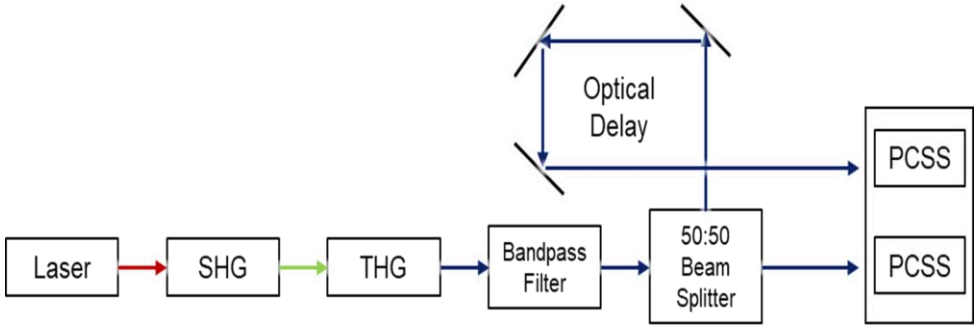
GaN:C PCSS Direct RF Modulation: Setup

GaN:C PCB for Bipolar Modulation

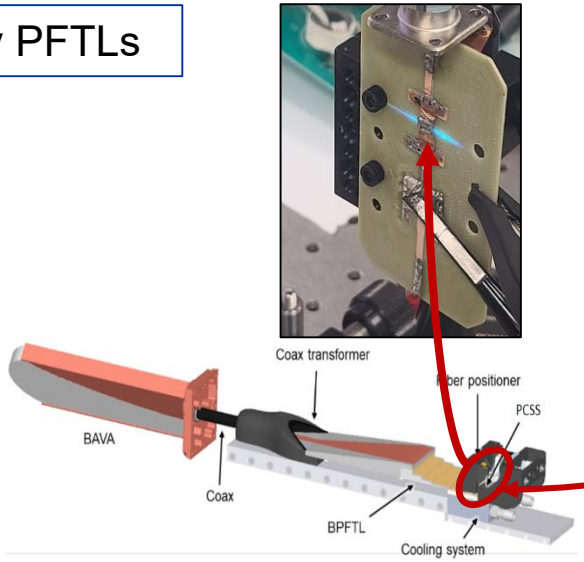


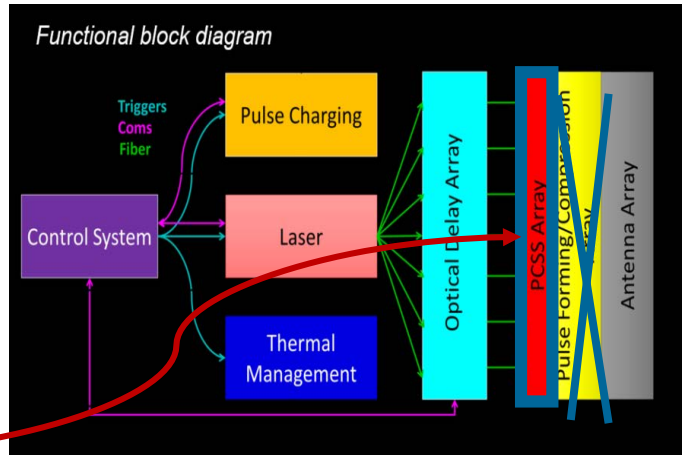
PCB in place of bulky PFTLs

Optical Delay Schematic

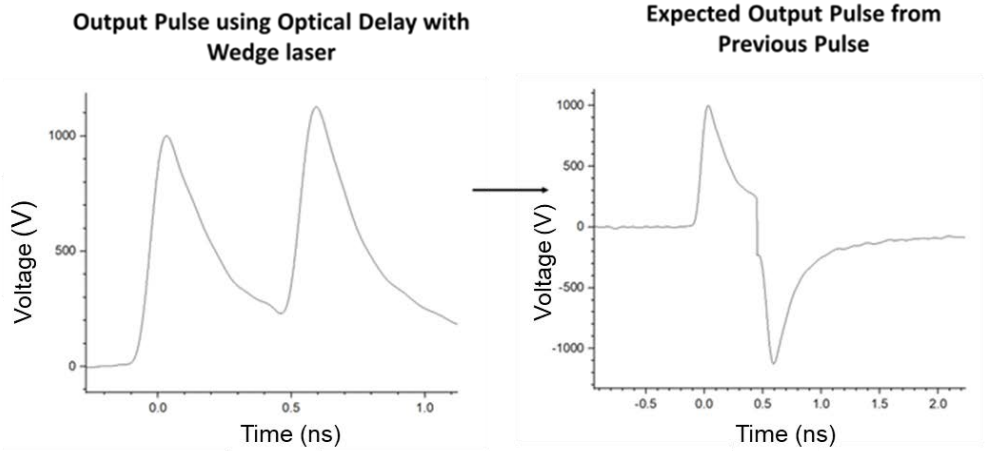


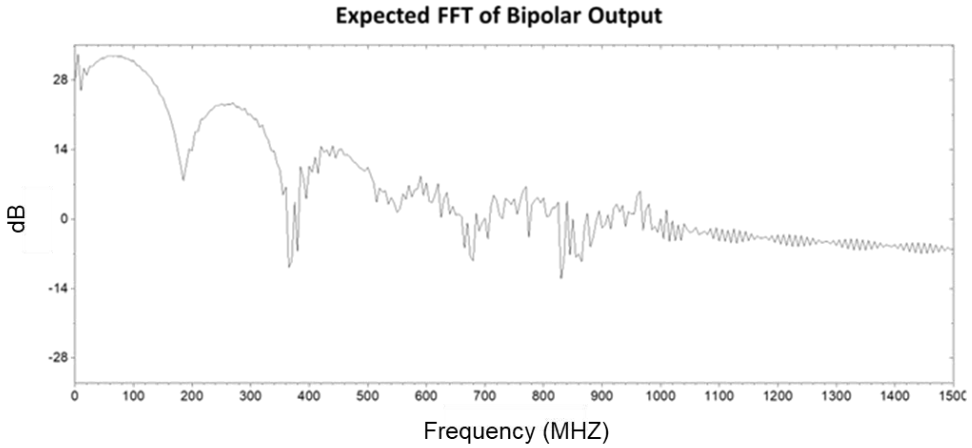
Free-space optical delay used

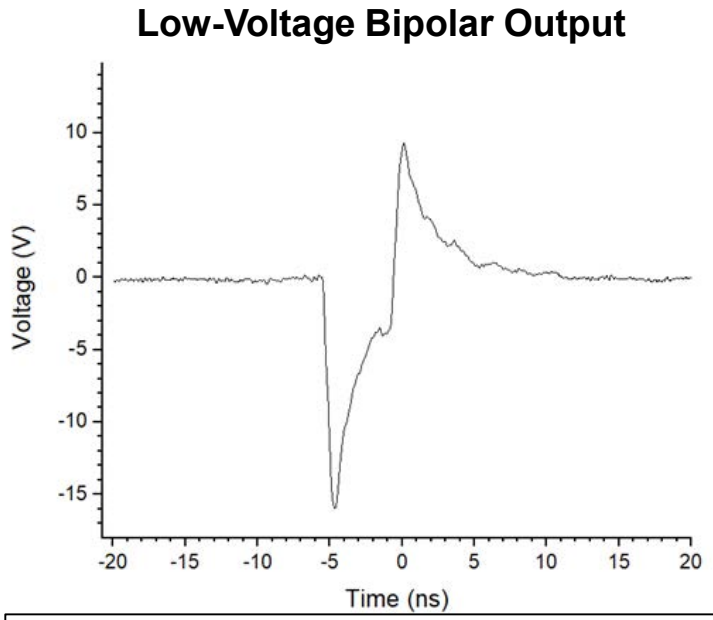




GaN:C PCSS Direct RF Modulation: Results







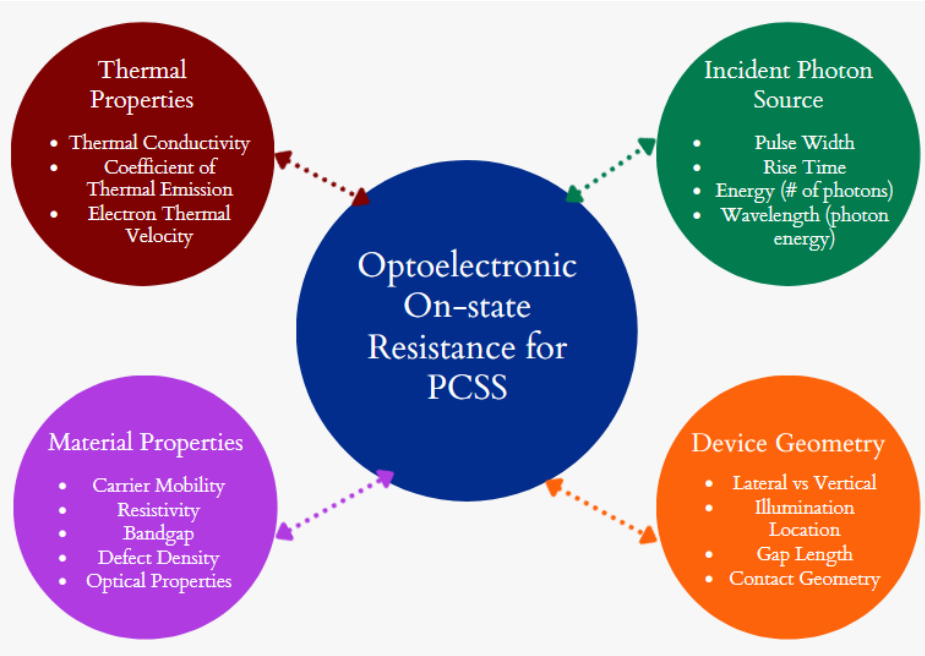
- Demonstrated low voltage, bipolar proof-of-concept with ~70 ps pulse width laser.
- Too little usable laser energy after conversion to 355 nm → Needs laser with greater conversion efficiency to achieve quicker rise-time/pulse width.

- Unipolar modulation demonstrated at <2kV
- Peak voltages limited to <2 kV due to lack of passivation
- Output used to predict bipolar output at same operating voltage
- Bipolar output has a reduction in freq. response due to non-radiating DC content

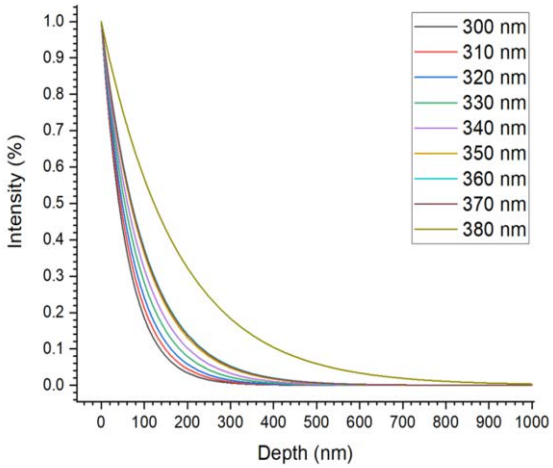
GaN:C PCSS Minimizing On-state Resistance

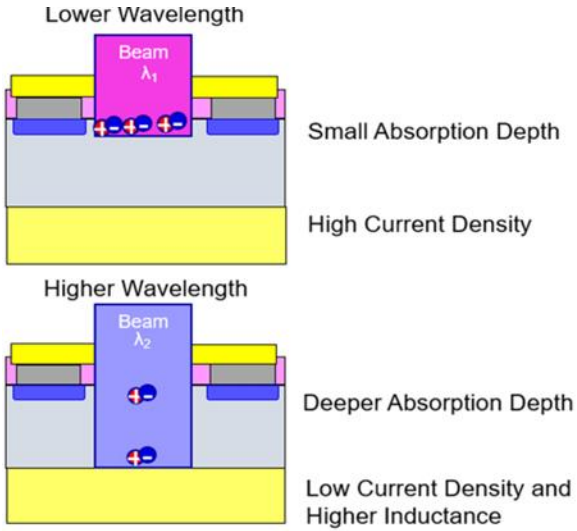
Reason: To reduce cUAV size and cost via PCSS efficiency increase.

On-state Resistance Parameters



Intensity vs device depth by wavelength



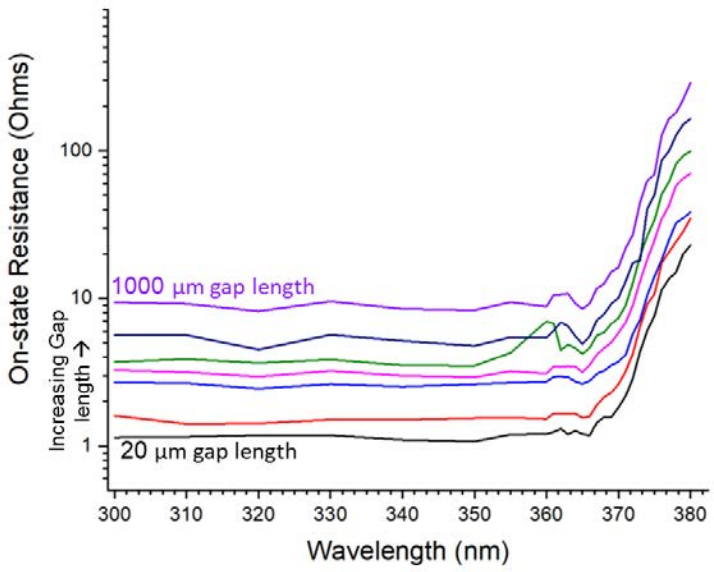


A lot of factors affect on-state resistance in GaN PCSS. Our focus was on **wavelength** and **incident energy.**

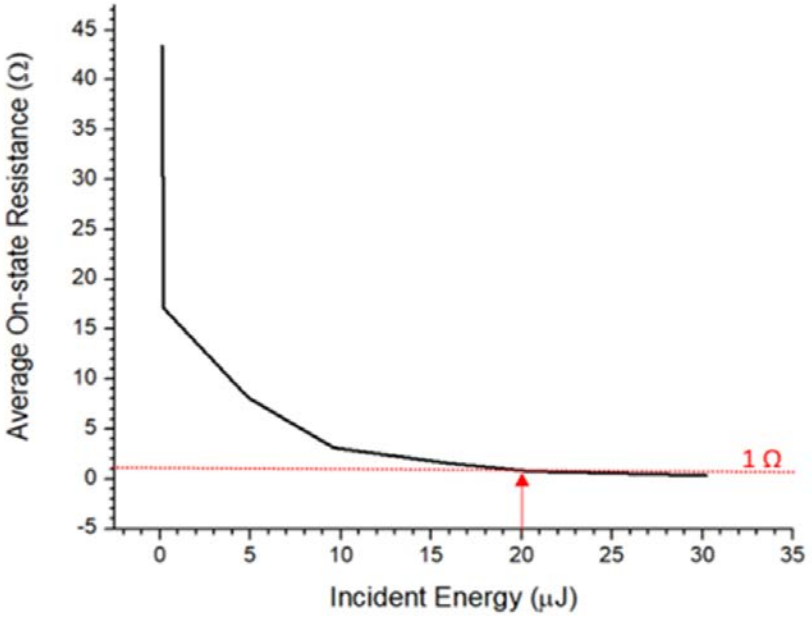
J. F. Muth *et al.*, "Absorption coefficient, energy gap, exciton binding energy, and recombination lifetime of GaN obtained from transmission measurements," *Appl. Phys. Lett.*, 1997. (Upper right graph)

GaN:C PCSS Minimizing On-state Resistance

On-state resistance as a function of wavelength



On-state resistance as a function of incident energy for 500 µm gap length



With an Increase in gap length:

- Operating voltage increased
- Minimum on-state resistance achieved is limited without increase in incident energy

At **wavelengths >370 nm an exponential increase in the on-state resistance** was seen for all gap lengths.

On-state resistance: ~1 Ω, at approximately 20 µJ

Energies above this level do not generate excess carriers and instead contribute to device heating

Summary

Top Contact Optimization

- Maximum possible reduction was 28.8% at 350 um spacing.
- Thermal failure due to spot heating near contacts due to high current density leads to additional cooling requirement (push spacing lower).
- Cooling and laser requirements can be considered together for optimal spacing using thermal TCAD solutions.
- Metal costs and metal reflectivity push spacing higher.

Lifetime Killing in Si PCSS

- Uniform and sloped defect profiles from electron irradiation were simulated.
- Uniform and sloped defect profiles both reduce recovery time near equally based on the total number of defects.
- Uniform defect profiles can have more total defects and reduce recovery time more.

FOM

- At 50 kHz PRR under adiabatic conditions, Ga_2O_3 and GaN performed the best in UWBG and WBG solids, respectively.
- However, under non-adiabatic conditions, diamond and SiC performed better.
- Does not include cost and size considerations.

Direct RF Modulation

- Unipolar modulation demonstrated at <2kV
- Bipolar output has a reduction in non-radiating DC content
- Successful low voltage, bipolar proof-of-concept using ~70 ps pulse width laser.
- Too little usable laser energy after conversion to 355 nm using ps laser → Need setup with greater conversion efficiency to achieve quicker rise-time/pulse width.

Minimizing On-state Resistance

- On-state resistance: ~1 Ω, at approximately 20 μJ.
- Energies above this level do not generate excess carriers and instead contribute to device heating.
- At wavelengths >370 nm there is an exponential increase in the on-state resistance for all gap lengths, so photon sources above this wavelength are not usable.

Recommendations & Future Work

Si PCSS:

Top Contact Optimization

- Non-provisional patent being sought; drafting for journal publication, transferred to OSPRES contract
- Additional TCAD studies for doping optimization with top contact, possible geometric effects, application to vertical SiC and GaN PCSS, and thermal effects on cooling optimization

Lifetime Killing in Si PCSS

- Using TCAD simulation compare switching losses between uniform and sloped electron irradiation defect profiles
- Compare uniform, sloped and combinations of uniform and sloped defect profiles

FOM:

- FOM can be extended to include device-level evaluation with material-specific optical-to-electrical power conversion rates and device-level recombination times.
- Include recombination-enabled energy loss component for more accurate results at device-level.

GaN:C PCSS

Direct RF Modulation

- Use alternative picosecond photon source to allow for modulation at higher RF frequency outputs.
- Optimize lateral GaN:C devices via contact and geometry optimization to prevent surface flashover between contacts at >2kV at <1 Ω on-state resistance.

Minimizing On-state Resistance

- Utilize TCAD and COMSOL to simulate effects of material, device, and circuit level changes on on-state resistance.

Outputs

Top Contact Optimization:

IP Disclosure

Eifler, "Photoconductive Contact Pattern for Enhanced Charge Collection", July 8, 2020.

Proton Irradiation:

Journal Article:

(In preparation) J. K. P Bhamidipati, G. Bhattarai, A. N. Caruso, "Effect of Proton Irradiation Induced Localized Defect/Trap Clusters on Silicon Photoconductive Semiconductor Switch (Si-PCSS) Recovery Time and Leakage currents," *Solid-State Electronics,* In Preparation, 2022.

FOM:

Journal Article:

John Keerthi Paul Bhamidipati, Eliot R. Myers, Adam M. Conway, Lars F. Voss, and Anthony N. Caruso, "Figure of Merit Development for Linear-Mode Photoconductive Solid-State Switches," *IEEE Transactions on Electronic Devices*, Under Revision, 2020.

IP Disclosure:

Bhamidipati, Myers, Caruso "Multi-Stage Photo-Stimulated WBG-PCSS Driven RF Pulse Generation System Implementing Miniature Optical Sources", 21UMK009, 04NOV2020

Dissertation:

John Keerthi Paul Bhamidipati, "Pulse Generation, Shaping, and Optimization Solutions for Solid-State-Switch-Enabled High-Power Microwave Generation Systems" PhD Dissertation in Physics and Electrical Engineering, UMKC, 2022.

GaN:C PCSS:

Conference Presentations:

H. A. Thompson, N. J. Kramer, A. Utt, J. Crow, E. R. Myers, A. D. Koehler, and A. N. Caruso, "Cost-to-benefit analysis of GaN for Photoconductive Semiconductor Switches (PCSS)," *Directed Energy Professional Society (DEPS) Annual Directed Energy Science and Technology Symposium,* Destin, Florida, USA, April 8-12, 2019**.**

Thank you!

Extra Slides

Different Switch Technologies

A solid-state switch can be used as a source driver to convert voltage and current pulses into RF frequencies for electromagnetic transmission.

Switch Tech.	SOTA	Pros	Cons
GaAs-PCSS	• >10 kV hold-off • Optically induced avalanche capable • Sub-ns t_r • ~ns fall time (t_f)	• Electrical isolation • Mature device tech. • High e^- mobility • Sub-ns transients	• Device degradation due to Joule heating • Low device lifetime • Avalanche at >10kV • COTS unavailability
GaN-PCSS	• >5 kV hold-off • Sub-ns t_r • ns-order t_f	• Electrical isolation • Sub-ns transients • Avalanche@3.5kV/cm	• Immature device tech. • Expensive • COTS unavailability
Silicon Avalanche Switch (SAS)	• >>5 kV hold-off • Sub-ns t_r • ns-order t_f	• Avalanche @1kV/ns rise rate • Inexpensive solution • sub-ns risetime possible	• High jitter & carrier lifetime • COTS unavailability
FET-run frozen wave generator	N/A	• Inexpensive • FET implementable • Tunable transients	• Bipolar pulse – not ideal for LDA trigger
GaN-FET closing switch	• 2-ns t_{rise} • >900V V_{ds}	• Inexpensive • COTS availability	• Need for additional pulse shaping network for current gain stage
Opto-diodes & opto-couplers	• 15 kV hold-off • Integrated high gain LED	• Electrical isolation • High voltage rating • Integrated optical source	• Need >100-µJ optical pulse energy • Slow turn-off (~ 3 µs)

Some Considered Technologies for OSPRES

Si PCSS

- Cost Effective
- Med. Laser Requirements



SiC PCSS

- Direct RF
- High Thermal Conditions
- High Voltage



GaN PCSS

- Increased Efficiency
- High Voltage
- High Thermal Conditions



DSRD

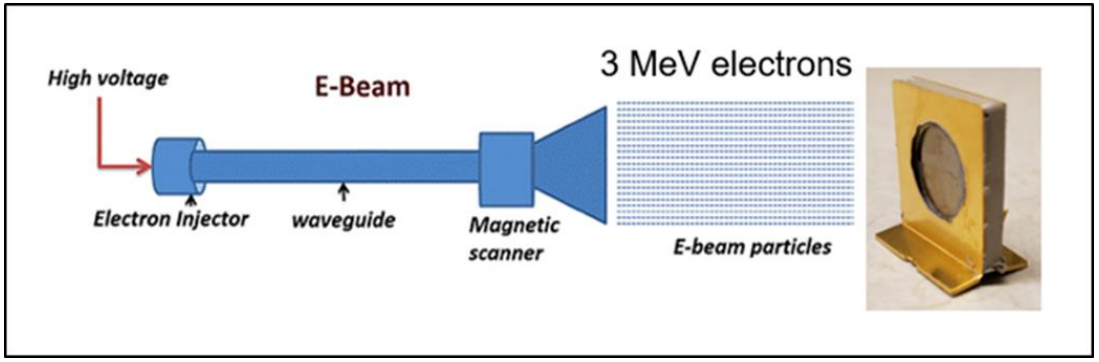
- No Laser
- Simplified Operation

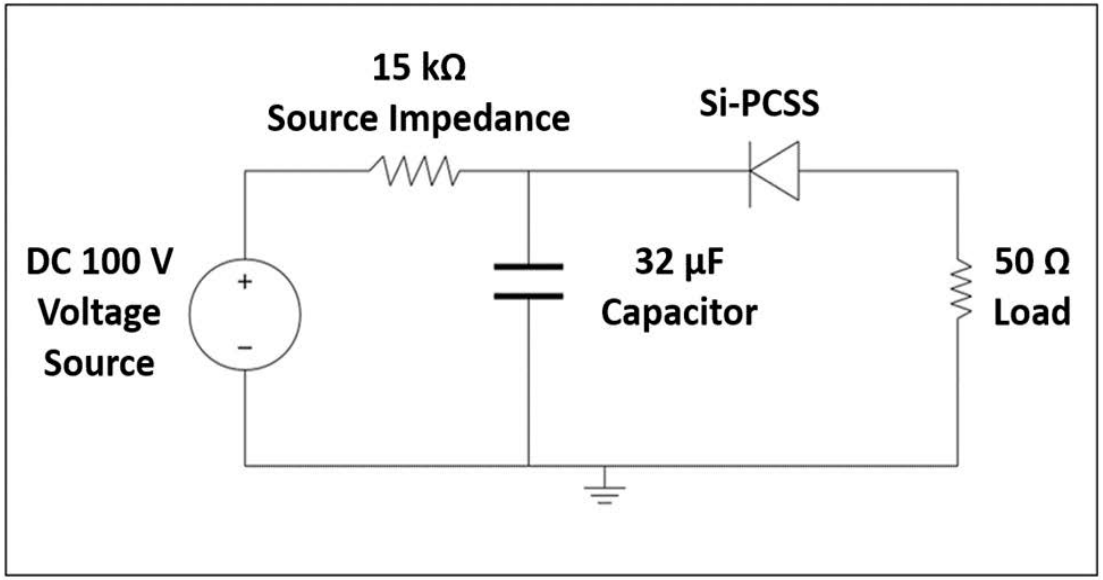


Lifetime Killing in Si PCSS: Background

Enabling higher pulse repetition rates, decreasing switching losses and increasing energy efficiency through reduction of carrier lifetime using electron irradiation.

- For Si PCSS to enable high pulse repetition rates (PRR) up to 1 MHz, recovery times <1 μs are required
- Electron irradiation, to reduce carrier lifetime and the Si-PCSS recovery time, does not require a vacuum for irradiation samples and is therefore cheaper than other irradiation methods
- Faster recovery times also reduce switching losses, increasing energy efficiency required for high PRR pulser systems
- TCAD simulations are performed in capacitive discharge circuit (at right) for recovery times

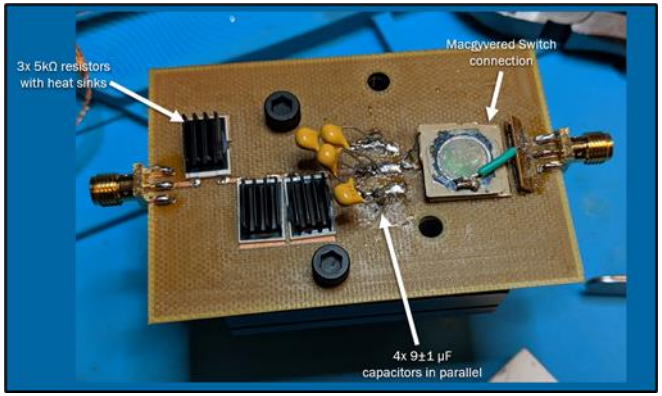


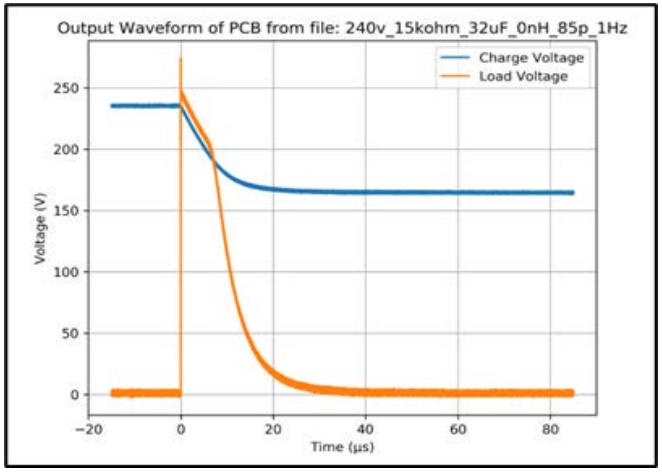


Lifetime Killing in Si PCSS: Simulation Details

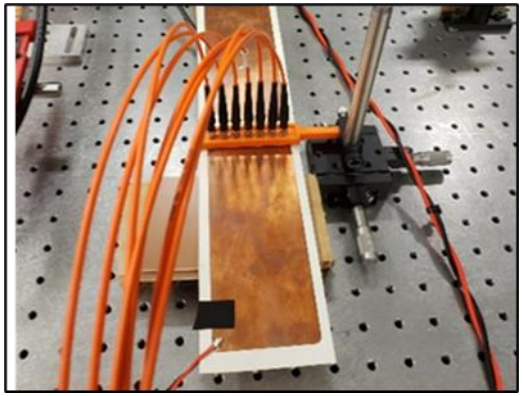
- Due to computational limitations in TCAD a capacitor discharge rather than transmission line (TL) discharge is used
- We study photo-illuminated recovery by discharging a capacitor through the switch into a load
- Ultimately interested in pulse forming network incorporating transmission lines (TL)

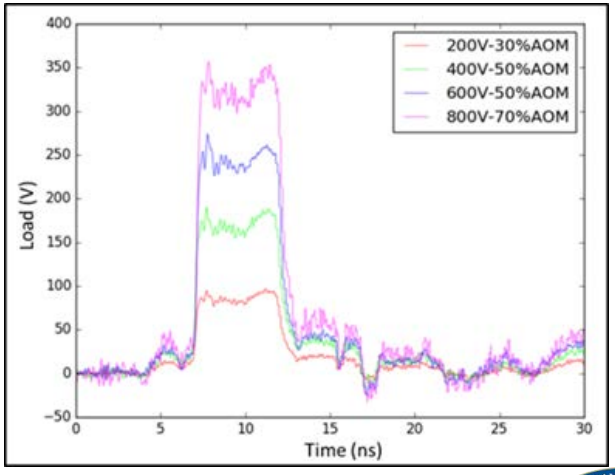
PCB Capacitive Test Circuit with Si-PCSS





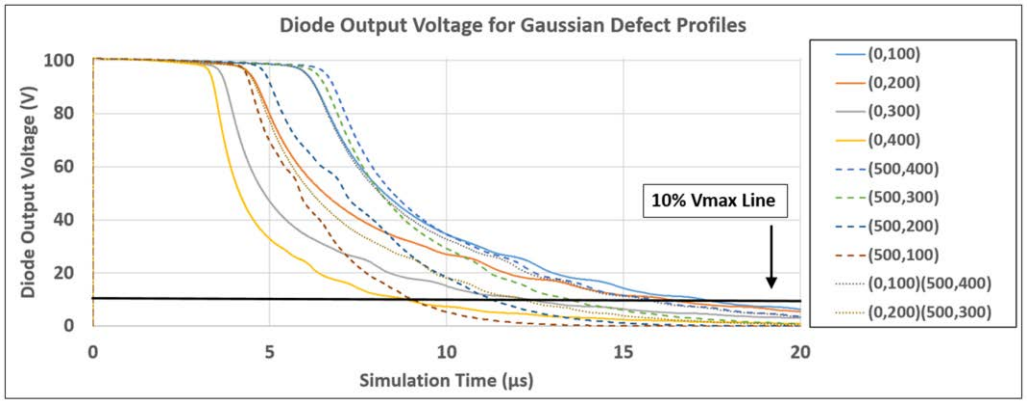
Si-PCSS integrated into TL

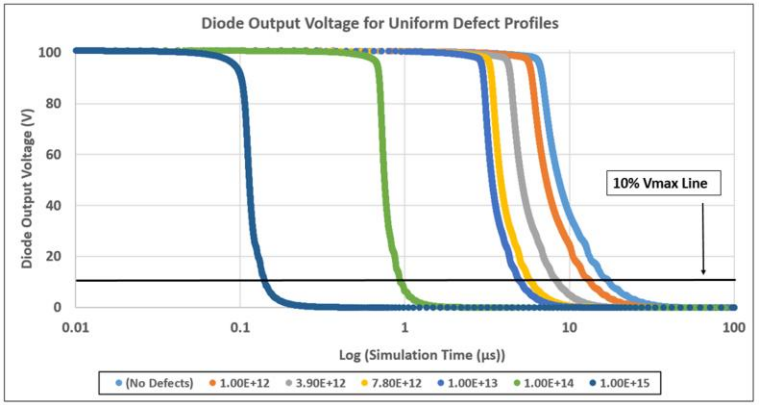


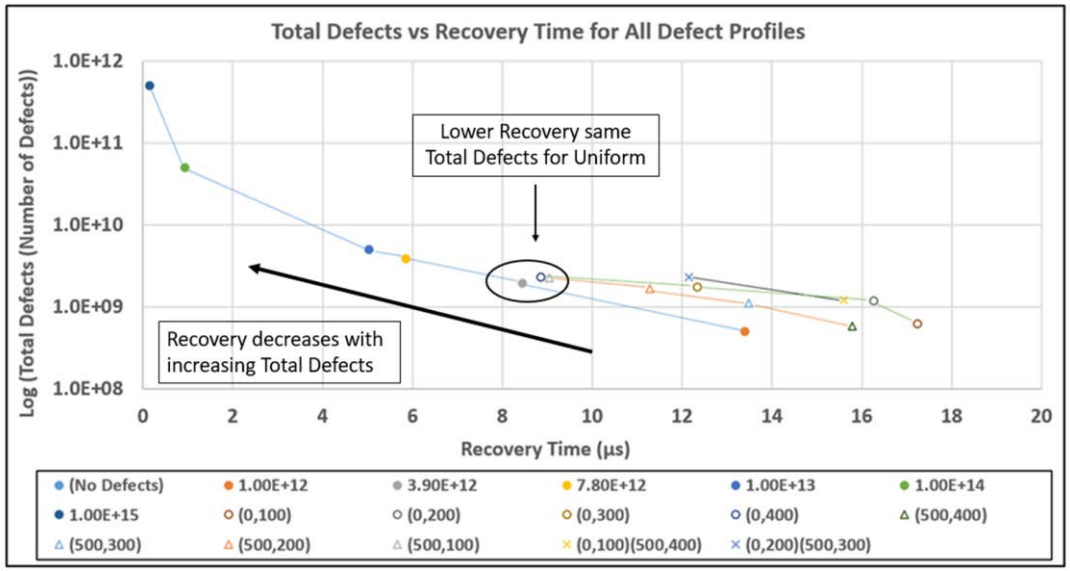


Lifetime Killing in Si PCSS: Results

- Uniform and sloped defect profiles both reduce recovery time near equally based on the total number of defects
- Uniform defect profiles can have more total defects and reduce recovery time more
- Recovery time set to 10% Vmax of pulse







Future Work:

- Using TCAD simulation compare switching losses between uniform and sloped electron irradiation defect profiles
- Compare uniform, sloped and combinations of uniform and sloped defect profiles

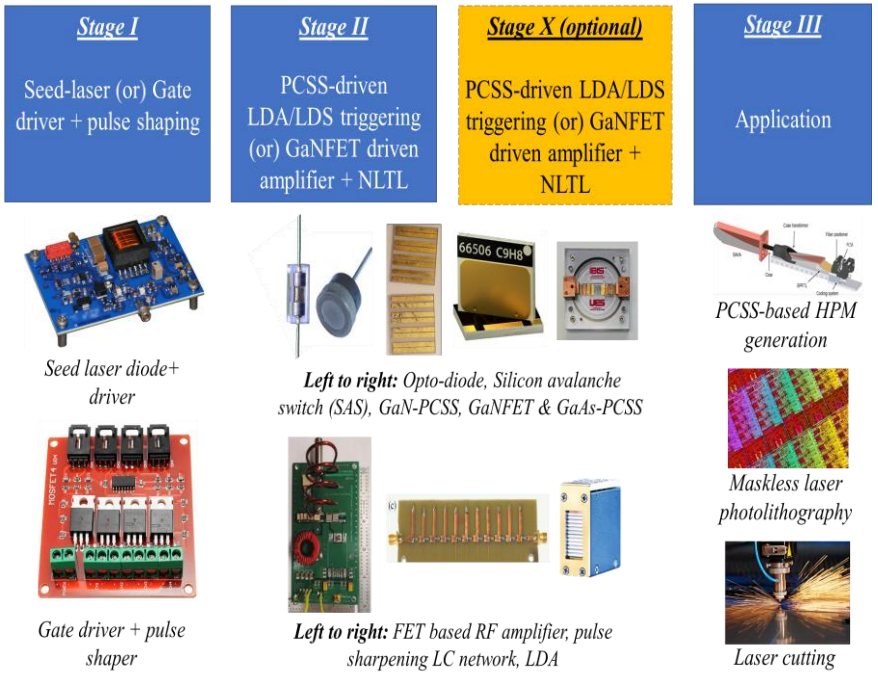
Compact, Inexpensive Alternatives for Optical Source Drivers: Background

Alternative solution for conventional laser driver subsystem allowing for enhanced SWaP-C^2 and decrease in HPM system cost, volume, and power (optical and electrical) requirements.

Switch Technology Comparison

Switch Tech.	SOTA	Pros	Cons
GaAs-PCSS	• >10 kV hold-off • Optically induced avalanche capable • Sub-ns t_r • ~ns fall time (t_f)	• Electrical isolation • Mature device tech. • High e^- mobility • Sub-ns transients	• Device degradation due to Joule heating • Low device lifetime • Avalanche at >10kV • COTS unavailability
GaN-PCSS	• >5 kV hold-off • Sub-ns t_r • ns-order t_f	• Electrical isolation • Sub-ns transients • Avalanche@3.5kV/cm	• Immature device tech. • Expensive • COTS unavailability
Silicon Avalanche Switch (SAS)	• >>5 kV hold-off • Sub-ns t_r • ns-order t_f	• Avalanche @1kV/ns rise rate • Inexpensive solution • sub-ns risetime possible	• High jitter & carrier lifetime • COTS unavailability
FET-run frozen wave generator	N/A	• Inexpensive • FET implementable • Tunable transients	• Bipolar pulse – not ideal for LDA trigger
GaN-FET closing switch	• 2-ns t_{rise} • >900V V_{ds}	• Inexpensive • COTS availability	• Need for additional pulse shaping network for current gain stage
Opto-diodes & opto-couplers	• 15 kV hold-off • Integrated high gain LED	• Electrical isolation • High voltage rating • Integrated optical source	• Need >100-μJ optical pulse energy • Slow turn-off (~ 3 μs)

Multi-state Pulse Application and Sharpening



Compact, Inexpensive Alternatives for Optical Source Drivers: Results

Si-PCSS & Si-optodiode (VMI) Testing

Si-optodiode

- R_{on} of **0.143 Ω** at **200 µJ and**
- t_{rise} of **329.4 ps** with a **6.038 Ω** R_{on} at 21 **µJ**

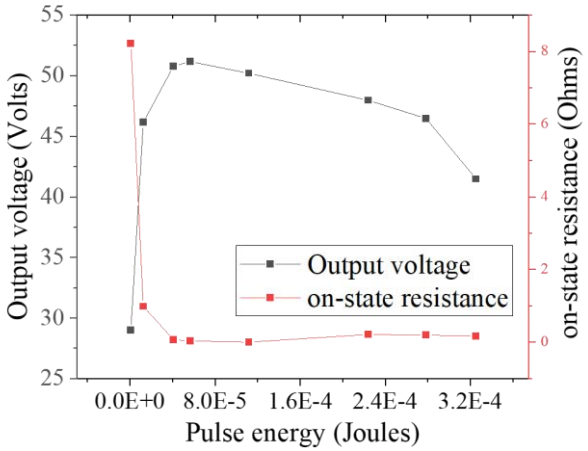
Si-PCSS

- R_{on} of < **0.325 Ω** at >250 µJ/pulse

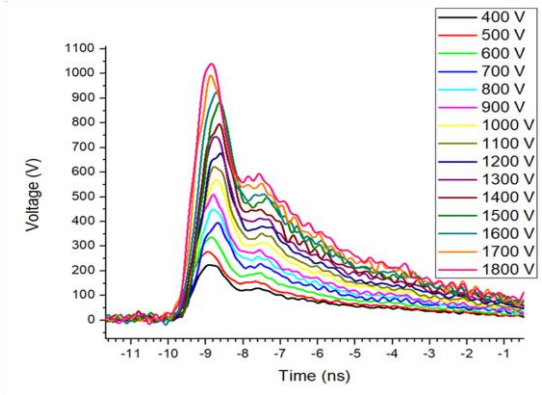
GaN-PCSS Testing

Expected: Persistent (Avalanche?) conductivity at >3kV/cm
Result: Testing using 355 nm laser excitation → linear mode at 18 kV/cm

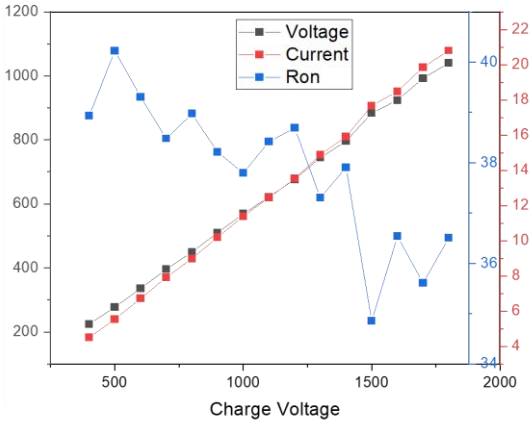
Si-PCSS trends



1000 µm gap length GaN:C PCSS at 63 µJ/pulse



On-state resistance trends at the same optical energy



Devices failed to satisfy the metrics (R_{on} = 72 mΩ and t_{rise} < 200-ps at <40 µJ) → infeasible as an alternative to GaN-PCSS.

Avalanche mode not achieved as expected at >3kV/cm

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for c-sUAV Study (OSPRES Grant)

N00014-17-1-3016
09/30/2017-09/29/2022

Diode-Based Nonlinear Transmission Lines for Ultra High Frequency Generation

Nicholas Gardner

nghvc@umsystem.edu

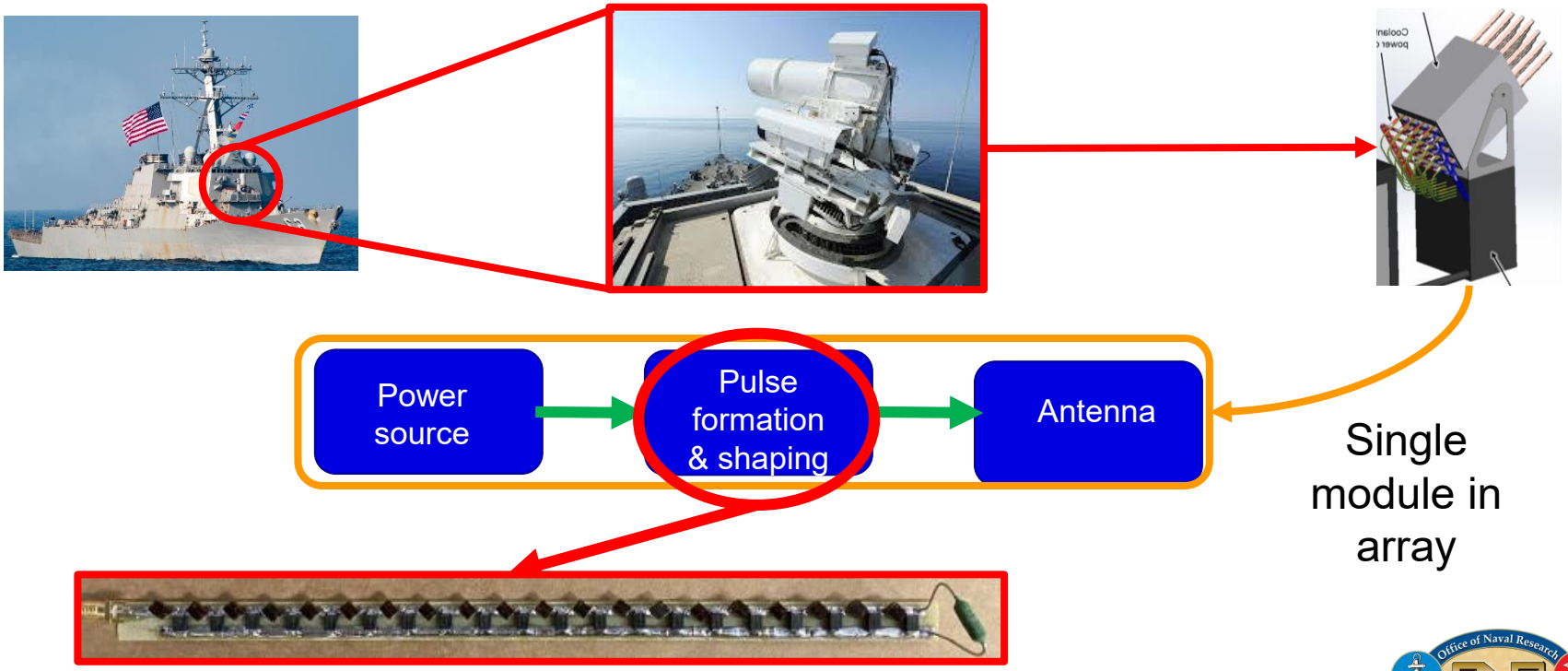
DISTRIBUTION STATEMENT A: Distribution authorized to all OSPRES Grant and Contract performers, and any uncompensated OSPRES collaborators. Further dissemination per the Office of Naval Research, Ryan Hoffman (ryan.b.hoffman.civ@us.navy.mil, 703-696-3873) or higher DoD authority.

Motivation

Primary Problem: The size, weight, and cost of pulse forming/shaping networks (PFNs) need to be reduced and optimized for Navy afloat missions.

Solution: Develop a diode-based nonlinear transmission line (D-NLTL) as a pulse shaping network for the conversion of energy to the ultra-high frequency (UHF) band (0.3–3 GHz) at single MW peak power.

State-of-the-Art: D-NLTL prototypes have been shown to generate center frequencies of 0.2–0.5 GHz at kV amplitudes in a light-weight small-footprint circuit. Simulations of LE-NLTLs indicate achievable frequencies in the single GHz range.



Motivation

Deficiency in the SOTA/Sub Problem:

- While D-NLTLs have produced frequencies above 100 MHz there is not a reliable design process capable of predicting frequency generation based on component selection
- D-NLTLs have yet to demonstrate frequency production in the UHF (0.3-3GHz) range and/or MW peak powers

Solution Proposed:

- Characterize diode parameters affecting frequency generation in the UHF band and identify limits/desired ranges required for UHF generation.
  - diode frequency response
  - diode reverse bias hold-off voltage
  - diode small signal capacitance,
  - diode chip/package parasitics
- Use identified metrics to design D-NLTLs capable of MW UHF generation

Objective

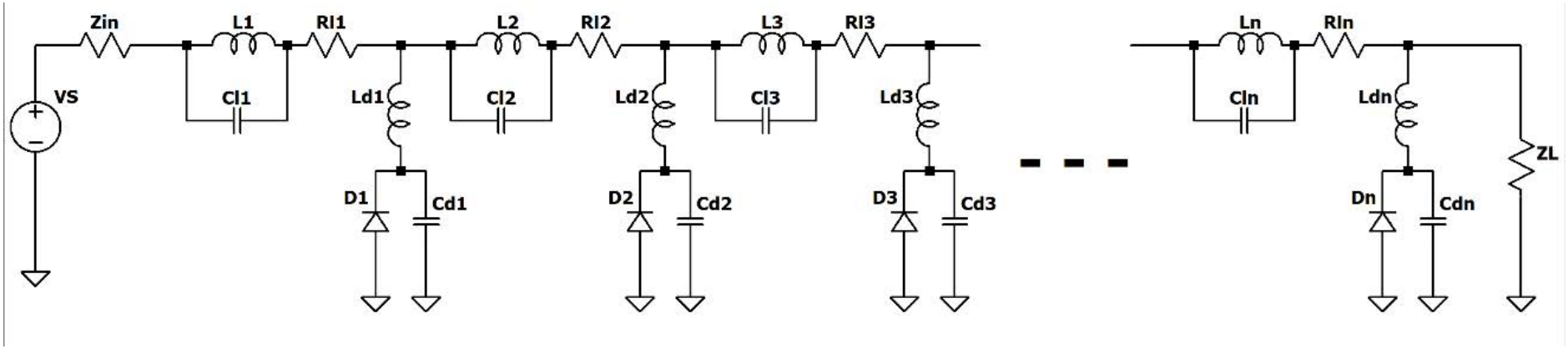
Objective 1: Increase the center frequency generation capabilities of the D-NLTL network into the UHF range (0.3 – 3GHz) in a compact, low cost, modular/scalable package.

Objective 2: Develop a design and fabrication process for D-NLTLs operating above 100MHz center frequencies.

Outline

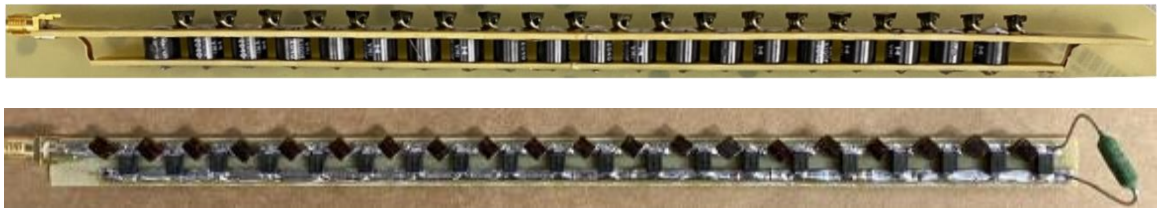
I. **Theoretical/Technical Background**
   I. D-NLTL Structure
   II. D-NLTL Soliton Generation
   III. Measurements of Interest
II. **Results**
   I. D-NLTL Design Metrics
   II. D-NLTL Electric Tunability
   III. MW-GHz D-NLTLs
III. **Outputs**
IV. **Personnel**
V. **Summary**
VI. **Future Avenues**

D-NLTL Structure



- A lumped element transmission line with a series inductance and shunt capacitance
- A reverse bias p-n junction provides shunt capacitance
- As a signal passes through a given cell the amplitude of the signal causes the depletion zone to increase, decreasing capacitance
- C_{Ln}, L_{dn}, R_{Ln}, C_{Dn} represent sources of loss in each diode and inductor

C_{Ln}	Inductor Coil Capacitance
L_{dn}	Diode Lead Inductance
R_{Ln}	Inductor Coil Resistance
C_{Dn}	Diode Shunt Capacitance



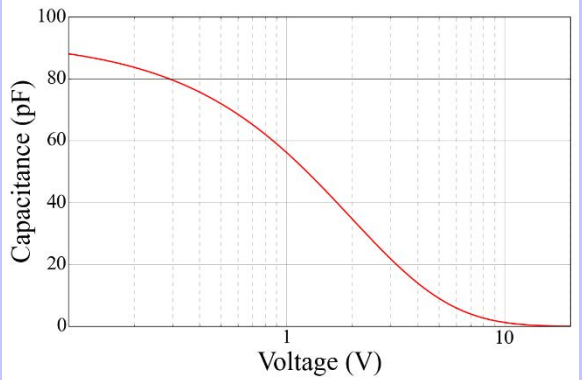
Soliton Generation

D-NLTLs increase frequency content by breaking signals into component solitons

Propagation rate

$$v = \frac{1}{\sqrt{LC}}$$

Diode C(V) curve



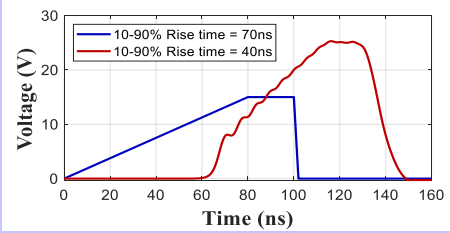
Rise time reduction

$$\Delta T = n\left(\sqrt{(LC)_i} - \sqrt{(LC)_f}\right)$$

Excitation rise time + Rise time reduction

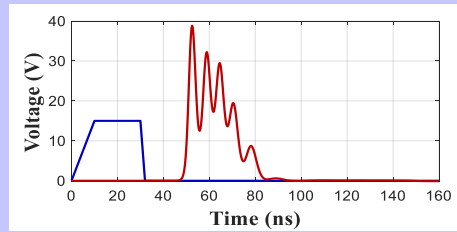
$tr_{in} \gg \Delta T$

Rise time reduction

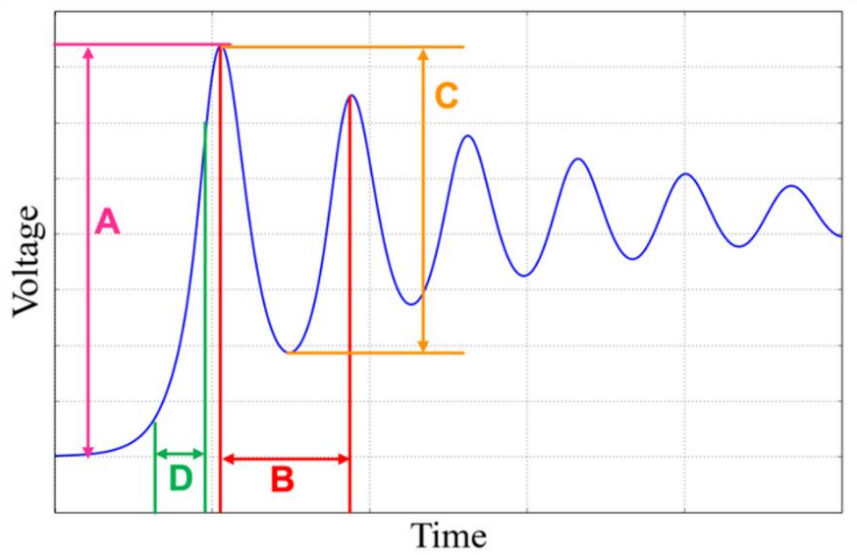


$tr_{in} \ll \Delta T$

Soliton formation



Measurements of Interest



Measurement	Description	Symbol	Unit
Peak Power (A)	Measured as the amplitude of the first soliton in time domain. Indicates the peak power output of the D-NLTL.	P_{max}	W
Center Frequency (B)	Measured as the inverse of the time between solitons in time domain. Measured as the peak after the DC bias in frequency domain.	f_c	MHZ
Voltage Modulation Depth (C)	A ratio of the depth between solitons in time domain to the peak amplitude. Gives an indication of D-NLTL efficiency with respect to max theoretical efficiency.	VMD/n_{RF}	%
Bragg Frequency (D)	The max frequency capable of propagating in a D-NLTL network. Measured as the inverse of rise time in time domain.	f_{Bragg}	MHZ

D-NLTL Design Metrics – Parameter Space

Motivation: Prototypes consistently failed to produce desired frequencies based on simulations

Solution:

- Study the waveform response to variations in several input and network parameters on a prototype in a known functioning range - sub 100 MHz center frequency
- Compare results back with simulation and identify necessary parameters in simulation and design
- Use results and simulation comparison to construct a LV D-NLTL capable of operating above 200 MHz
- Compile metrics into a coherent set of design parameters

Excitation space

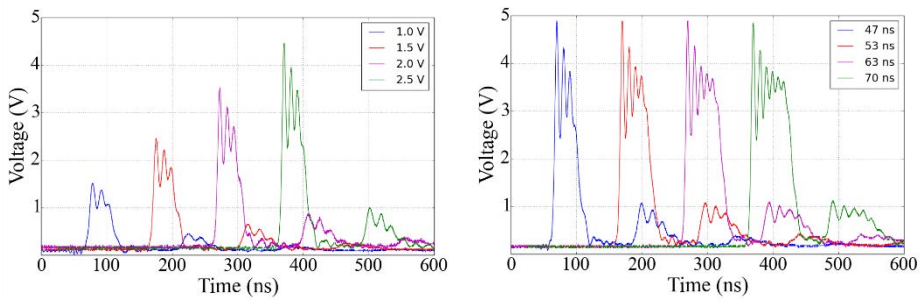


Image: (A) Excitation amplitude. (B) Excitation width

- Pulse amplitude increases: P_{pead}, f_c, f_{Bragg}, and n_{rf}
- Pulse width only had an appreciable affect on soliton count
- Pulse rise time had no measurable effect when under the conditions for soliton formation

Take Away:

- Rise time < ΔT for soliton formation – otherwise little effect
- Amplitude needs to be capable of driving desired saturation

Network space

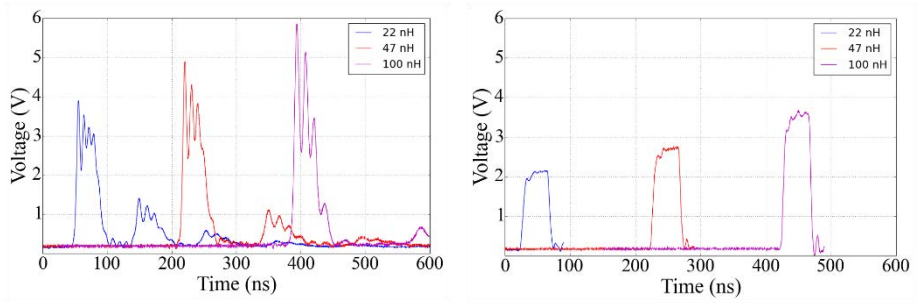


Image: (A) Induction effect on waveform. (B) Induction effect on injected pulse

- Induction value is inversely correlated with f_c, and f_{Bragg}.
- Induction heavily influences average impedance
- VMD can be increased by increasing length, but at a hit to f_c
- C(V) curve is most heavily influenced by junction capacitance and grating coefficient

Take Away:

- There is a balance between efficiency and center frequency
- C(V) Curve must hit saturation for a given excitation amplitude

Corresponding Paper: "Design Considerations for Diode based Nonlinear Transmission Lines" [1] - Published May 2022 – AIP Advances

D-NLTL Design Metrics – Prototype Metrics

200+ MHz prototype: A 40 cell D-NLTL based on a SMV1702 model diode and a 22 nH cell inductance was constructed based off the following:

- A usable cell inductance range of 10 – 100 nH
  - 10 nH keeps cell inductance above trace inductance
  - 100 nH keeps diode capacitance above PCB capacitance
- 40 Cells + 22 nH inductance produced the max simulation frequency with VMD>50%
- SMV1702 could handle voltages up to 20V but would reach an order magnitude decrease in capacitance around 2-4 V

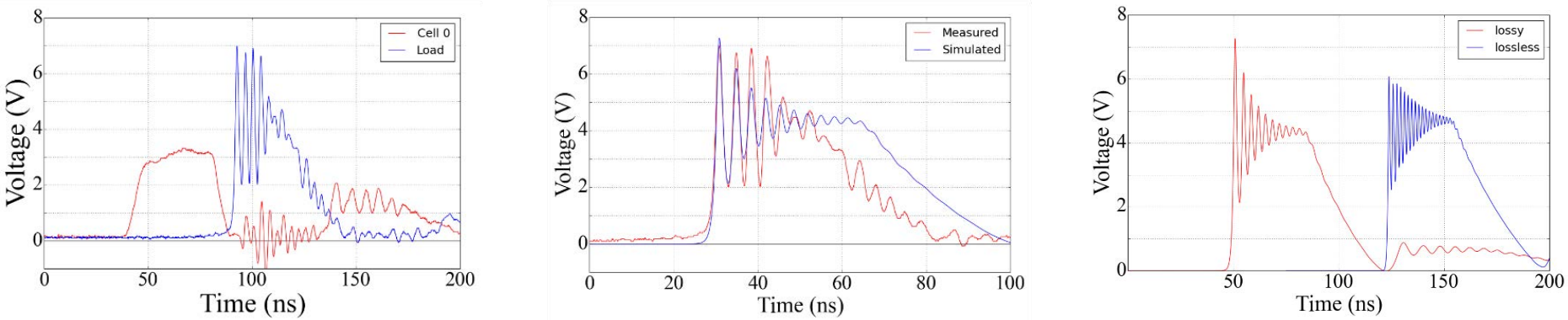


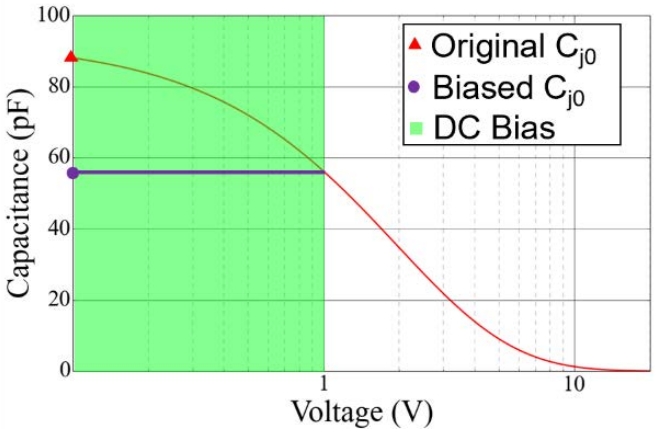
Image: (Left) Prototype measurement, (Middle) measurement v lossy sim comparison, (Right) lossy v lossless sim comparison

	Prototype	Lossy Sim	Lossless Sim
f_c (MHz)	256	249	543
f_{Bragg} (MHz)	446	574	1.01

Corresponding Paper: "Design Considerations for Diode based Nonlinear Transmission Lines" [1] - Published May 2022 – AIP Advances

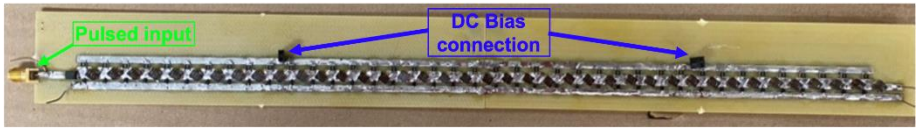
D-NLTL Electric Tunability – f_c Control

Idea: Applying a DC bias to each diode alters the behavior of the CV curve and therefore the frequency characteristics of the system

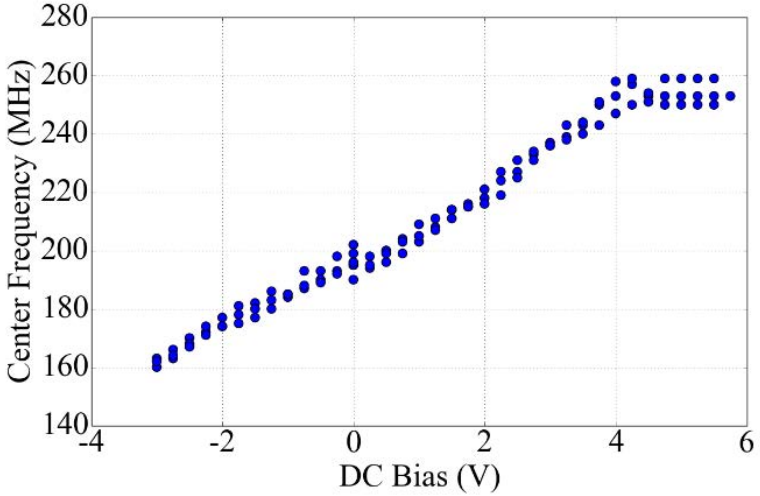


Prototype:

- A 40 Cell D-NLTL based on the SMV1702 Diode
- DC bias applied through 1 Ωk surface mount resistances



Results



Summary

- Application of a DC bias which matches the polarity of the line will increase the generated center frequency
- Application of a DC bias with polarity opposite of the line will decrease the generated center frequency

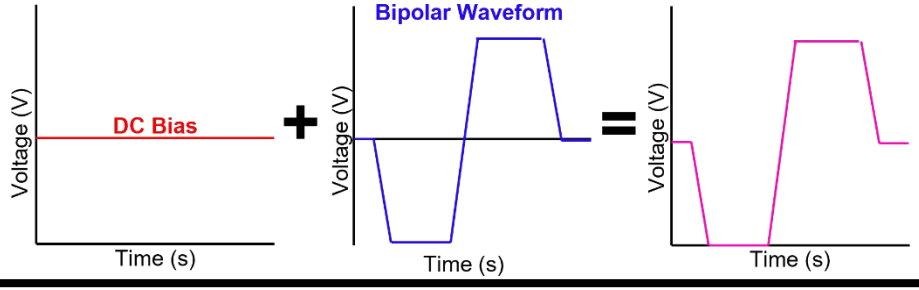
Corresponding Paper: “Electrically Tunable Diode Based Nonlinear Transmission Lines” [2]

In Preparation

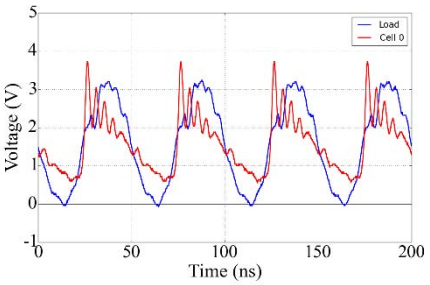
D-NLTL Electric Tunability – Bipolar Excitation

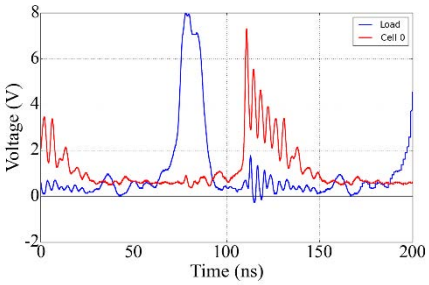
Idea:

- Directional nature of diodes does not allow for use of bipolar excitations
- If a DC bias is applied equal to the negative polarity amplitude of the bipolar signal the negative portion will drop the line to zero saturation and effectively impart a pulse with amplitude equal to to V_{pp}



Results





- (Left) a 20 MHz 10V_{pp} sine wave excitation
  - f_c = 214 MHz
- (Right) an 8 MHz 10V_{pp} 20% duty cycle square wave
  - f_c = 260 MHz

Impedance matching results

Signal Shape	Square (DC = 0V)	20 MHz Sine (DC = 3.7V)	8 MHz Square (DC = 6.2V
f_c (MHz)	190	214	260

- Bipolar signal + DC bias produces a greater f_c
  - The signal is better able to saturate the line
- At the source-line interface a bipolar pulse imparts a smaller voltage displacement from equilibrium
  - Reduced displacement = less effect from impedance mismatch
  - A 10 V square wave produces a lesser amplitude after the source-line interface than the 10V_{pp} square wave on the biased line

Summary

- Bipolar pulses can be compatible with a D-NLTL if the line is biased to the negative polarity amplitude
- Use of a bipolar pulse increases the generated frequency as compared to a mono polar pulse with amplitude equal to V_{pp} of the bipolar pulse
  - The bipolar pulse transfers more energy into the D-NLTL as the smaller amplitude (as measured from V=0) is affected less by the source-line impedance mismatch

Corresponding Paper: “Electrically Tunable Diode Based Nonlinear Transmission Lines” [2]

In Preparation

MW-GHz D-NLTL

Set up:

- Two D-NLTLs, one with a single K100F model diode per cell, one with 2 K50F model diodes in series per cell.
- In simulation both lines could handle peak voltages of 12 kV and put out f_{Bragg} in the single GHz range

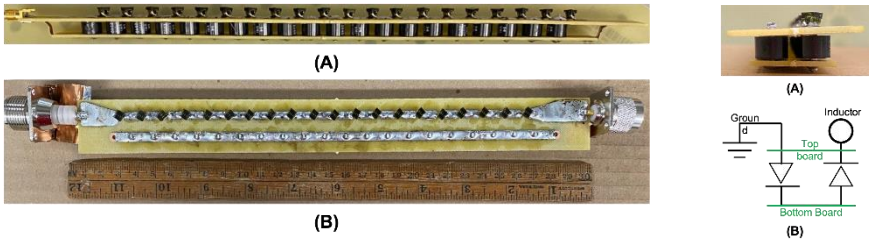
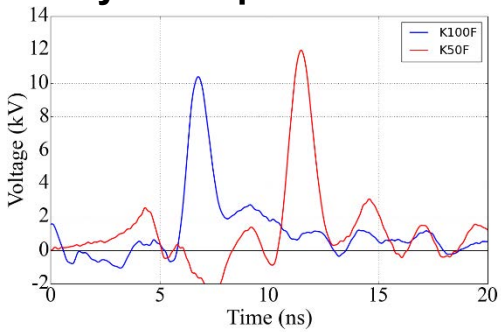


Image: (Top Left) K100F D-NLTL, (Bottom Left) K50F D-NLTL, (Top Right) end view of K50F line, (Bottom Right) schematic of diode set up in K50F D-NLTL

Drift step recovery diode pulsed source:



	f_{Bragg} (GHz)	P_{max} (MW)
Source	0.833	2.42
K50F	1.44	2.88
K100F	1.58	2.33

PCSS based pulsed source:

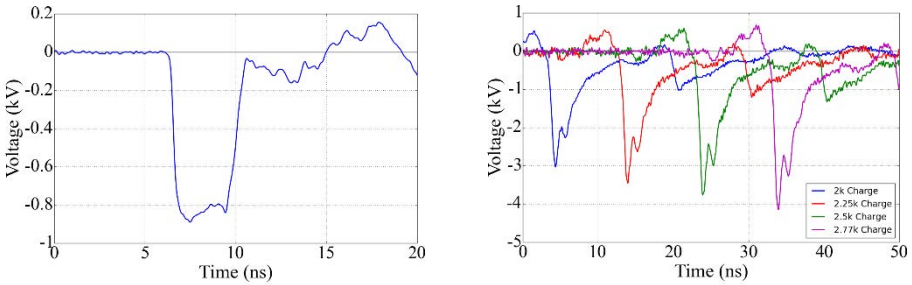


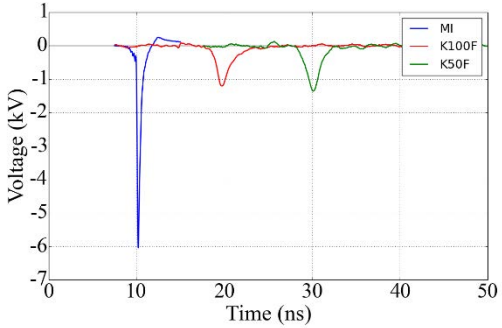
Image: (left) PCSS geometry. (Right) K100F results for 4 PCSS charge levels

Results:

- K100F line rebuilt to handle (-) polarity signals
- Excitation successfully broken into solitons
- 756 MHz f_c on all PCSS charge levels
- 1.19 GHz f_{Bragg} on all PCSS charge levels

Mega-Impulse pulsed source:

The frequency content of the MI source was primarily above the NLTL bragg limit. As a result, both lines functioned as low pass filters greatly attenuating the signals.



Corresponding Paper: “UHF and L-Band Frequency Generation at MW Peak Power using Diode-based Nonlinear Transmission Lines as Pulse Forming Networks” [3]

In Preparation

Summary

D-NLTLs are a promising PSN technology for compact RF systems but are limited by design difficulties, impedance matching issues, and lack of documented UHF and MW powers.

D-NLTL Design Metrics

- Provided increased clarity in D-NLTL design for f_c>100 MHz
- **Improves cost and time efficiency of design process**

D-NLTL Electric Tunability

- A DC bias + Bipolar excitation can lessen impedance mismatch effects
- **Improved matching improves prospects for implementation as a subsystem in a HPM system**

GW GHz D-NLTL

- Demonstrated the capability of D-NLTLs to produce MW power and UHF frequencies
- **If a D-NLTL is to be used as a PSN/PFN in a HPM system MW power and UHF generation are required**

Recommendations & Future Work

Open questions:

- How do NLTL design metrics correspond to custom diode fabrication?
  - COTS diodes are not designed for D-NLTL application – Do they need to be?
  - What metrics need to be set?
- What is the limit to D-NLTL frequency performance?
  - Is it limited more by the diode model or the substrate the line is built on?

Future avenues:

- Non-linear/dynamic impedance matching
  - Difficulties in D-NLTL implementation arise from matching a static impedance with the dynamic impedance of the D-NLTL
- Achieve tuning without affecting C(V) curve
  - DC bias is relatively easy to apply, but negatively affects VMD when used for frequency tuning
- Push the center frequency of HV lines further into the UHF Band
  - K50F and K100F results are promising
  - Source excitation needs to have a width of at least 3-5 ns for multi soliton formation
  - Charge capabilities of the PCSS strip line use limited the tests.

D-NLTL personell

Research Team



Nicholas Gardner



John Bhamidipati



Plamen Doynov*

Contributors



Dario Labrada*



Roy Allen



Kaylan Durbhakula

- High Voltage Sources
- Technical Writing/Manuscript contributions

*** Former member of MIDE**

Journal Publications

In Publication

[1] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “Design Considerations for Diode-Based Nonlinear Transmission Lines,” AIP Advances, 12, 055012, May 2022

In Preparation

[2] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “Electrically Tunable Diode-based Nonlinear Transmission Line,” *TBD*, In Preparation, 2022.

[3] N. Gardner, K. C. Durbhakula, and A. N. Caruso, “UHF and L-Band Frequency Generation at MW Peak Power using Diode-based Nonlinear Transmission Lines as Pulse Forming Networks,” *TBD*, In Preparation, 2022.

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for c-sUAV Study (OSPRES Grant)

N00014-17-1-3016
09/30/2017-09/29/2022

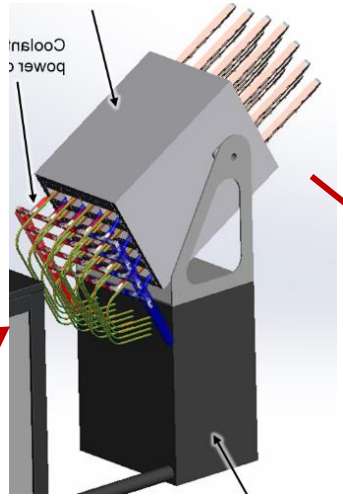
Ultrawideband Antenna Tradespace Analysis Outcome with Emphasis on Futuristic Design Methodologies

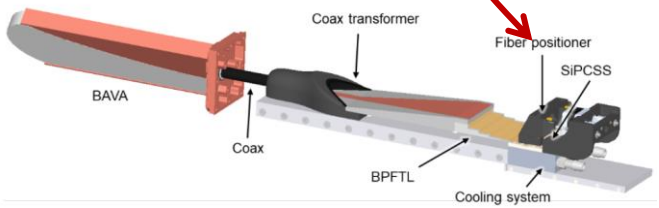
Bidisha Barman, bbcnk@mail.umkc.edu
Alex Dowell, addkbr@mail.umkc.edu
Sai S. Indharapu, sinf5@mail.umkc.edu
Kalyan Durbhakula, kalyandurbhakula@umkc.edu

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Motivation







Antenna that demonstrates ultrawide impedance bandwidth (> 500 MHz) with large transient gain (rE/V > 1), and maximum beam steerability (from an array)

Fundamental Motivation: To study, understand, improve and show tradeoffs between chosen antenna metrics (bandwidth, gain, steerability etc.) using multiple ultrawideband (UWB) antenna element and array designs.

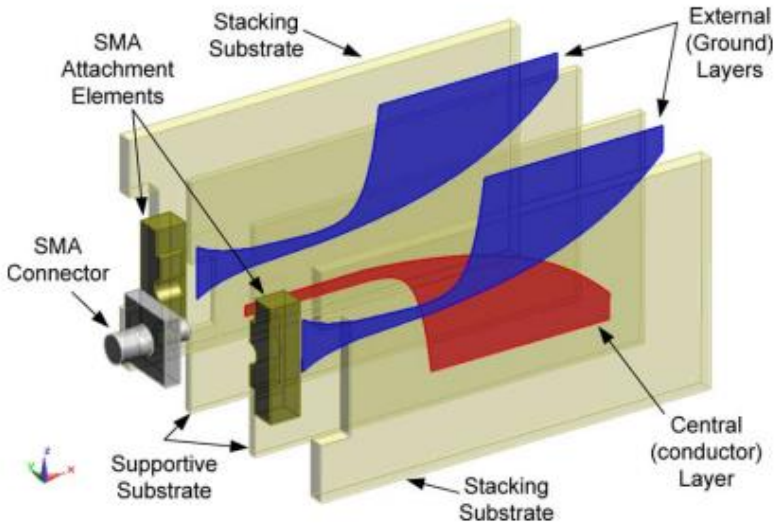
Applied Motivation: An UWB antenna with improved antenna metrics over the state-of-the-art to demonstrate enhanced high-power microwave (HPM) system efficiency.

Relevancy to OSPRES Mission: This work yields novel UWB antenna designs that are steerable to wide-angles and with high-transient gain tailored to match with the spectral content of short pulsed waveforms therefore enhancing the mission success rate.

State-of-the-Art

State-of-the-Art (SOTA): The balanced antipodal Vivaldi antenna (BAVA) is the SOTA antenna element due to its exceptional 20:1 impedance bandwidth ratio as well as the ability to handle tens-of-MW input power.

***Deficiency in the SOTA*:** The BAVA design parameter space has been exhausted over the past couple of decades. Despite its peak electric field dominance, the spectral content of BAVA is spread out over a range of frequencies resulting in loss of energy sometimes outside the frequencies of interest.

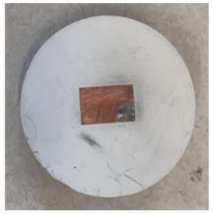


SOTA metrics

Antenna element type		BAVA (single element)
Aperture size		12 cm × 12 cm
Physical Aperture area		0.0144 m^2
Operating frequency range (fc±BW)		900 MHz ± 200 MHz
Peak gain at 900 MHz		3.7 dBi
Transient Gain		0.4
Half Power(-3 dB) Beam Width	E-plane	117°
Aperture Percentage at 900 MHz		143%
Scan Range at 900 MHz		±60°

Outline

I. **Electrically Small Antenna**

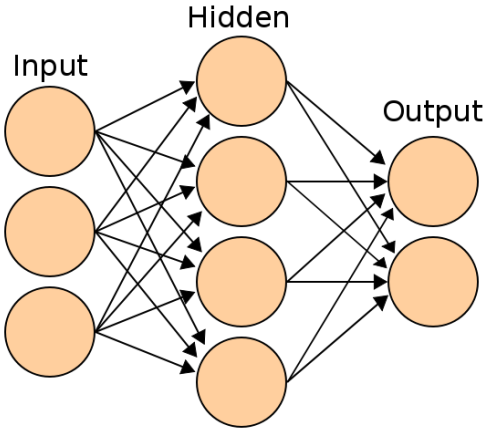


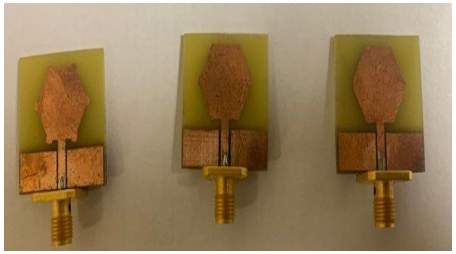


II. **Koshelev Antenna with Partial Dielectric Transformer**



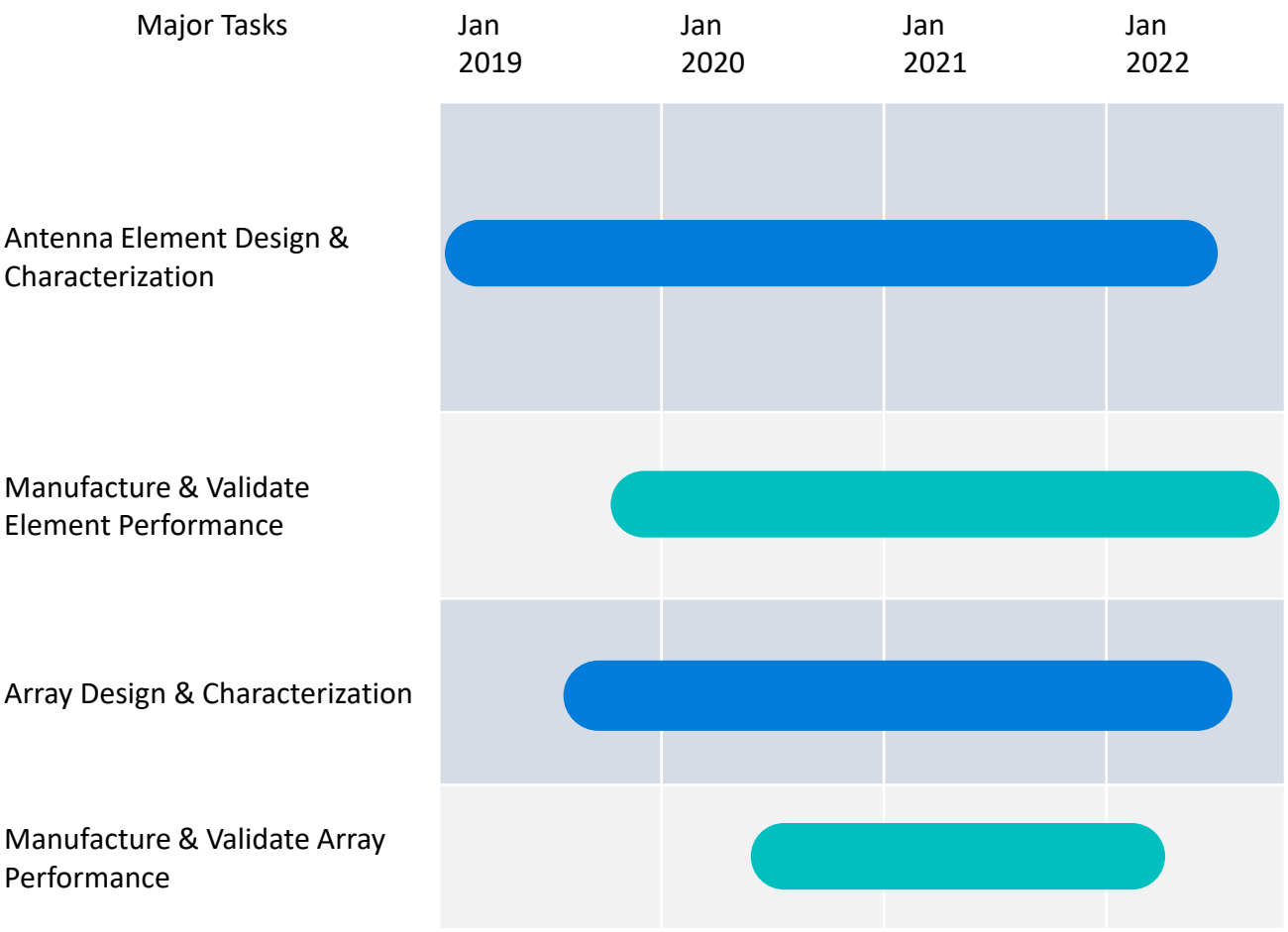
III. **Machine Learning Inspired Antenna Metrics Prediction and Optimization**





Objectives, Tasks and Milestones

Objective: Determining the extent to which the physical aperture size of the antenna array can be reduced, while maintaining performance (in peak power density, bandwidth and electronic beam steerability of short pulses) over the UHF range (0.6-1 GHz); Comparing with present art - HPM capable antenna arrays.



Milestones

- ❑ Developed a novel, coaxial-probe-fed, microstrip patch, ESA design that provides >30% BW.
- ❑ Avoids sophisticated prototyping.
- ❑ Validated design approach from UHF (MHz) to microwave (GHz) frequency range.
- ❑ Studied aperture shape and lattice structures.
- ❑ $\pm 60°$ beam steerability achieved.
- ❑ Validated design approach using 2×2 and 3×3 arrays.

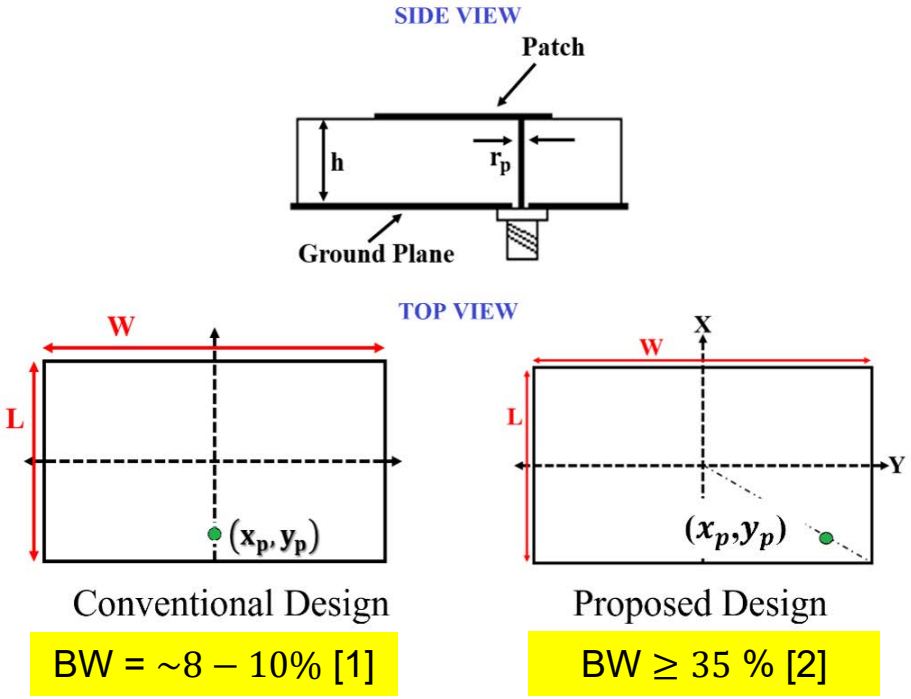
Antenna Element Design

Requirement(s):

1. ESA ($ka < 0.5$).
2. Wide bandwidth (BW) – short rise-time pulse transmission ($BW \propto 1/t_r$)
3. High power handling capability (PHC).

Coaxial probe-fed Microstrip patch antennas:

- Low fabrication complexity.
- Light weight & low volume.
- Ease to make electrically small.
- Narrow BW
- Low PHC



Conventional Design

BW = ~8 – 10% [1]

Proposed Design

BW ≥ 35 % [2]

Some Antenna Design Examples using Proposed Method

Substrate	Freq. Range (GHz)	BW
TMM-10i ($\varepsilon_r = 9.8$)	2.5-5	55%
TMM-6 ($\varepsilon_r = 6$)	2.5-5	37%
RT/duroid ($\varepsilon_r = 2.2$)	0.7-1.2	36%
TMM-10i ($\varepsilon_r = 9.8$)	0.6-1	43%

[1] R. Garg, P. Bhartia, I. Bahl, and A. Ittipiboon, *Microstrip Antenna Design Handbook*. Boston, USA: Artech House, 2000.
[2] B. Barman, *et. al.*, "Performance Optimization of a Microstrip Patch Antenna using Characteristic Mode and D/Q Analysis," *2020 XXXIIIrd URSI-GASS*, Rome, Italy, 2020, pp. 1-4.

Antenna Element: Experimental Validation

Element Design

Experimental Validation

Antenna Metric Comparison

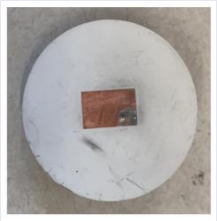
Array Design

Array Aperture Area Reduction

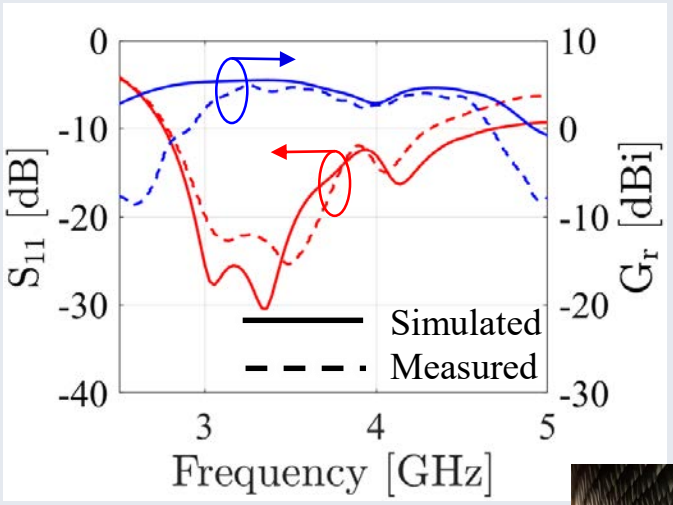
Array Design: Experimental Validation

Frequency Range: 2.5-5 GHz

$ka = 0.67$
(Quasi-ESA)



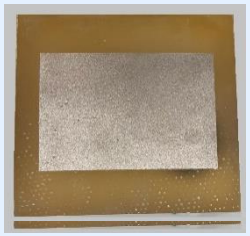
Antenna designed on TMM-10i substrate ($\varepsilon_r = 9.8$)



	BW
Simulated	54.94%
Measured	52.57%

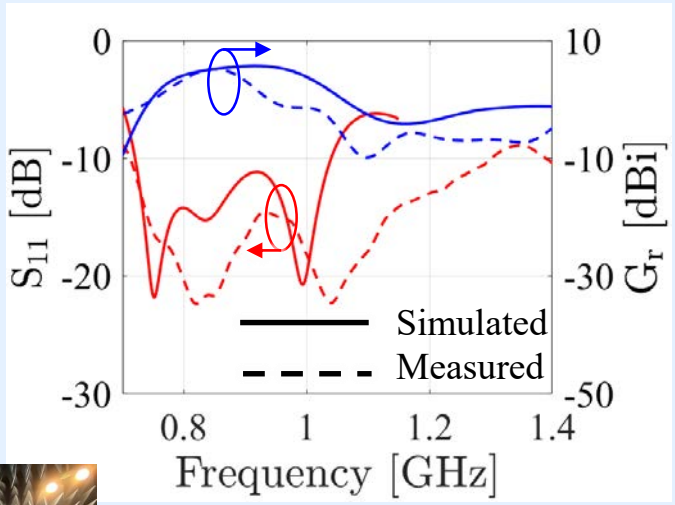


Frequency Range: 0.7-1.3 GHz





Antenna on 3D printed SLA ($\varepsilon_r = 2.6$) substrate with tapered coaxial-connector



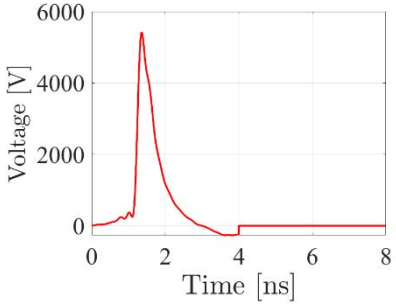
	BW
Simulated	36.2%
Measured	58.3%

The measured data provided a proof-of-concept for the proposed antenna design approach.

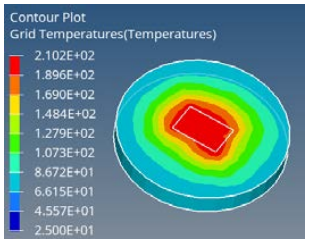
Antenna Element: Metric Comparison

Other studies performed:

- ❑ Time-domain analysis of the antenna elements, subjected to short rise-time pulses (CST Microwave Studio).
- ❑ PHC of antennas using thermal analysis (Altair Optistruct).



Input Pulse



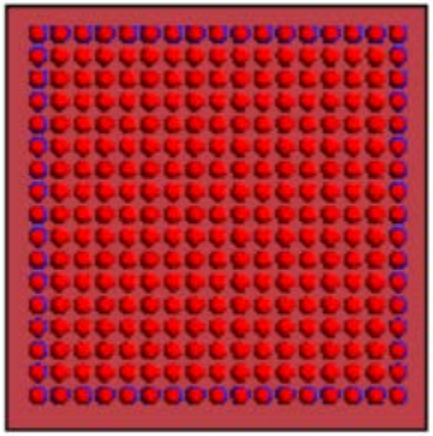
Thermal Profile of Antenna

Antenna element type	IRA [3]	Magnetic EZ [4]	Printed BAVA	Microstrip Patch (This work)
Physical Aperture area (m^2)	0.1257	~0.0012	0.0081	0.0019
Operating frequency range ($f_c \pm BW/2$)	12 GHz ± 12 GHz	510 MHz ± 1.53 MHz	900 MHz ± 200 MHz	899 MHz ± 169 MHz
Peak gain at f_c (dBi)	~10	~5	3	5.67
Transient Gain (rE/V)	1.18 (at 5.5 m)	-	0.4 (at 10 m)	0.73 (at 10 m)
Max. PHC (kW)	$\gg 8$	-	~0.5	4.5

[3] S. -F. Wang and Y. -Z. Xie, "A Method to Evaluate the Performance of Ultra-Wideband Antennas for the Radiation of High-Power Electromagnetic Pulses," *IEEE Trans. Antennas Propag.*, vol. 70, no. 8, pp. 7142-7146, Aug. 2022.
[4] J. Ng, R. W. Ziolkowski, J. S. Tyo, M. C. Skipper, M. D. Abdalla and J. Martin, "An Efficient, Electrically Small, Three-Dimensional Magnetic EZ Antenna for HPM Applications," *IEEE Trans. Plasma Science*, vol. 40, no. 11, pp. 3037-3045, Nov. 2012.

Array Design

A 15×15 planar array is composed of the designed antenna elements, on TMM-10i substrate, arranged in **square lattice**.



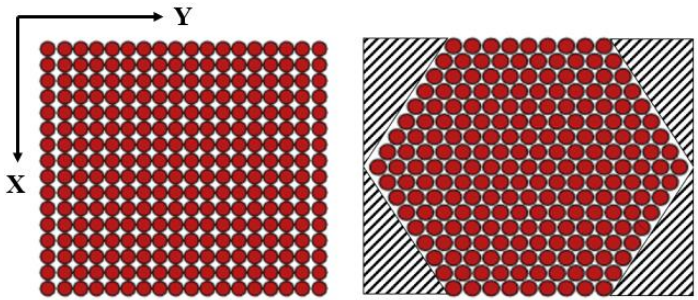
Schematic of the Array

- A ring of dummy elements placed around the 15×15 Array – to improve radiation pattern.
- λ_h calculated at 990.6 MHz.

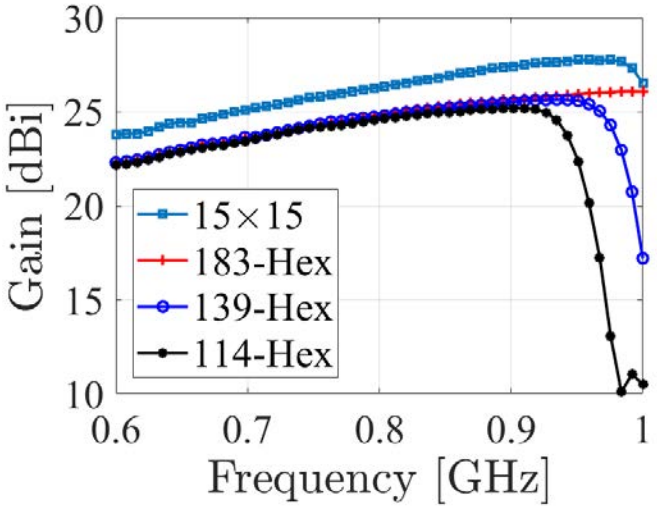
Parameters	Values
No. of active Elements	225
Operating Freq.	0.64-0.99 GHz
Inter-element spacing	$0.485\lambda_h$
Radiating Aperture Area	5.77 m^2 (w/o Gnd) 7.56 m^2 (Gnd)
Volume	0.15 m^3 (w/o Gnd) 0.2 m^3 (Gnd)
Max. Gain	27.76 dBi
Beam Steerability	$\pm 60°$
3 dB Beamwidth	10.6° (0.64 GHz) 6.9° (0.99 GHz)
Impedance Match	50Ω
Power Handling Capability	1.012 MW (4.5 kW per element)
Power density at 0.5 km	0.0192 W/cm^2

Array Aperture Area Reduction

Array model transformed from square to hexagonal lattice (elements in the shaded area removed) → $\approx 46\%$ Aperture Area Reduction with < 2 dBi gain drop.



Finite Square Ground Plane

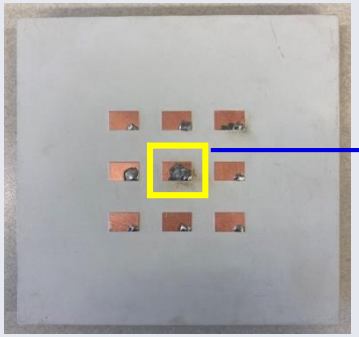


Array	Element spacing (d/λ_h)	Aperture Area (m^2)	Max. Gain (dBi)	PHC (MW)	Power Density at 0.5 km (W/cm^2)	Scan Range (deg)
15×15 (with dummy elements)	0.485	5.77	27.76	1.012	0.0192	$\pm 60°$
183-Hex	0.485	3.10	26.09	0.8235	0.0107	f_L: $\pm 50°$ f_C: $\pm 45°$ f_H: $\pm 45°$
139-Hex	0.56	3.12	25.66	0.6255	0.0073	
114-Hex	0.61	3.16	25.19	0.513	0.0054	

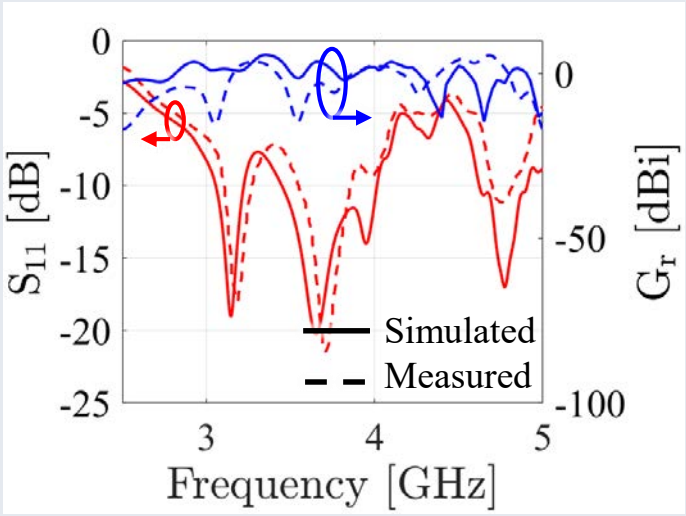
P_{in}/element = 4.5 kW

Array Design: Experimental Validation

Frequency Range: 2.5-5 GHz

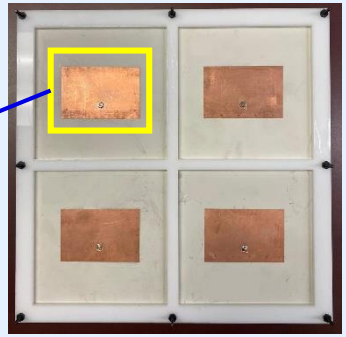


3 × 3 array of wideband antenna elements on TMM-10i substrate ($\varepsilon_r = 9.8$)

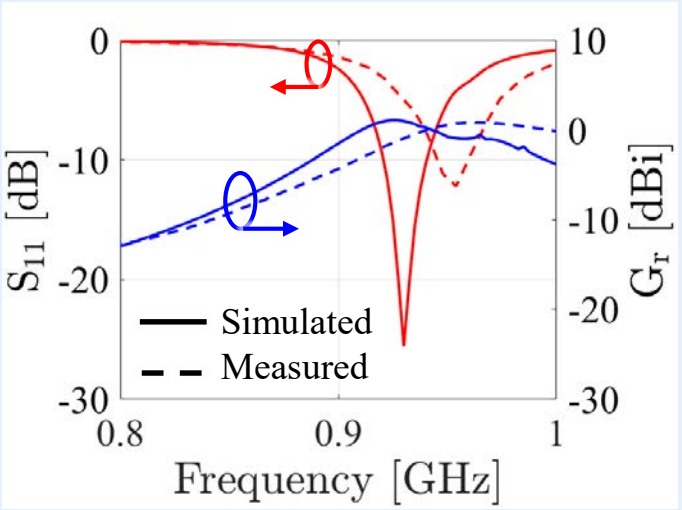


Active Element

Frequency Range: 0.8-1 GHz



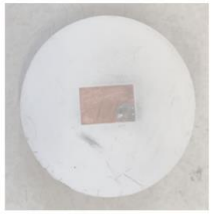
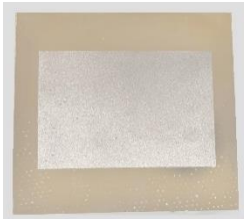
2 × 2 array of narrowband antenna elements on TMM-10i ($\varepsilon_r = 9.8$) substrate.



The design approach is validated using small array prototypes.

Outline

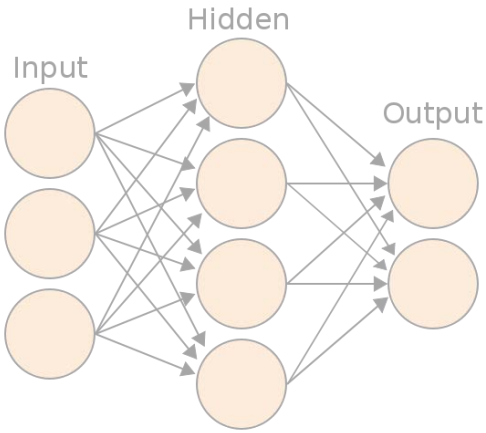
I. Electrically Small Antenna

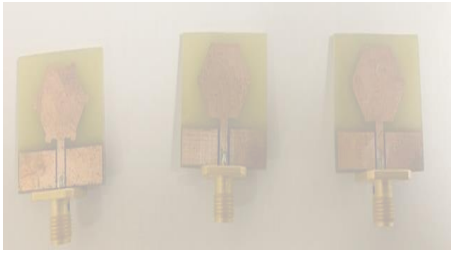




II. Koshelev Antenna with Partial Dielectric Transformer



III. Machine Learning Inspired Antenna Metrics Prediction and Optimization





Objective

Objective: Demonstrate an operational Koshelev antenna prototype which shows a 5× increase in bandwidth ratio (from 4:1 to 20:1) over traditional Koshelev antenna and a 2 dBi increase in gain at the center frequency of interest and a higher transient gain (rE/V > 1) over a single BAVA element.

(A)Perform tradespace studies on design parameters to reduce the Koshelev antenna aperture size than 12 cm x 12 cm.

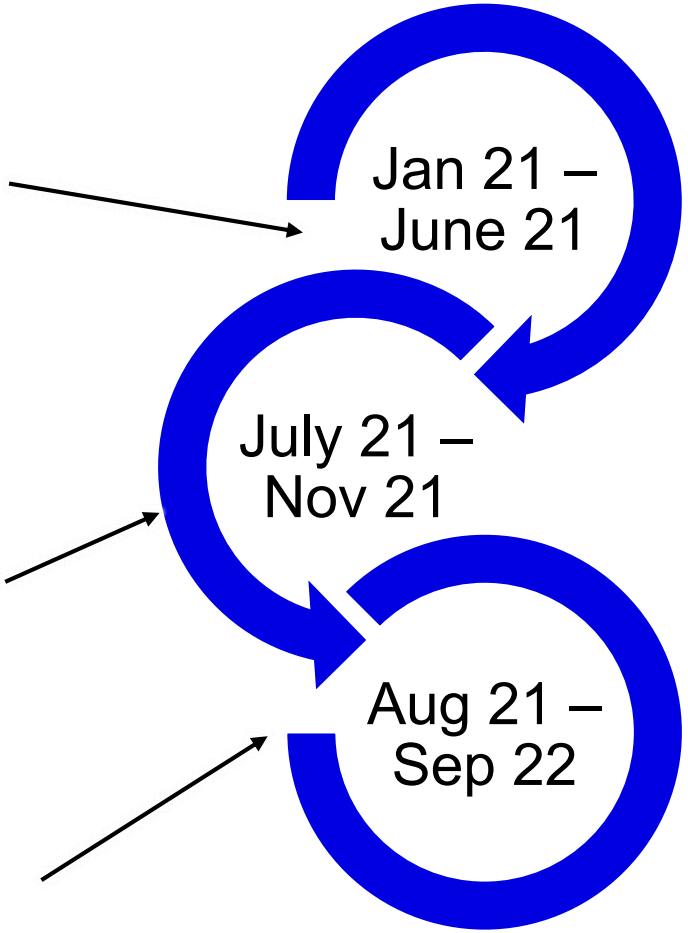
- **Milestone:** Identify Koshelev antenna design parameters that significantly alter the bandwidth, rE/V, peak gain and aperture percentage. Provide a recommendation on the optimum design parameters.

(B) Explore impedance taper designs, study monopolar and bipolar excitations, and simulate different array models based on the optimized single element Koshelev antenna model.

- **Milestone:** Recommend the optimum impedance taper design (with minimum reflections and maximum power transfer) with the optimum dimensions and an optimum array shape that yields maximum bandwidth (900 MHz ± 'x' MHz), peak gain > 15 dBi at 900 MHz and an aperture percentage > 100% .

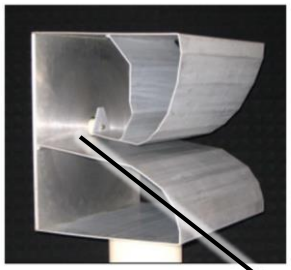
(C) Prototype single element Koshelev antenna and perform antenna measurements.

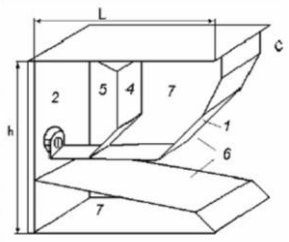
- **Milestone:** Demonstrate a functional 3-D printed Koshelev antenna yielding measured data comparable to the simulation data.



Technical Background and Approach

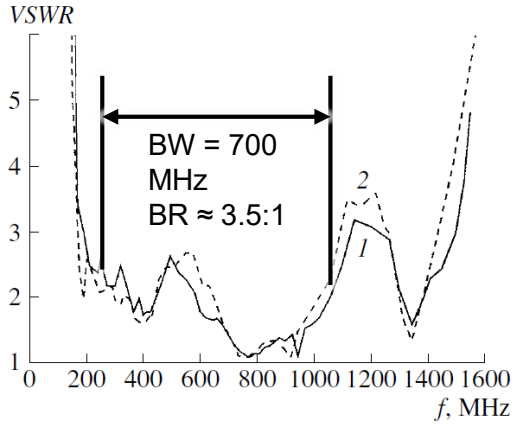
Koshelev Antenna (Unbalanced) + Balanced Design + Partial Dielectric Filling



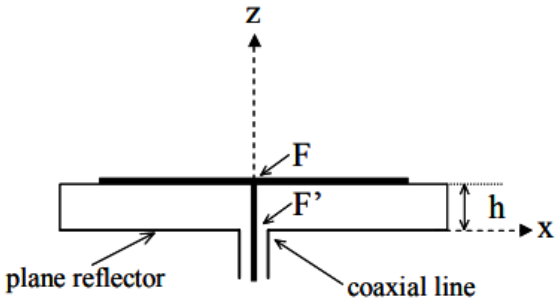


30 x 30 x 32 cm

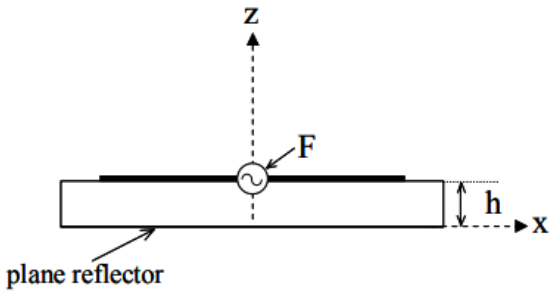
Unbalanced design



The Koshelev antenna is made up of TEM horn with exponential profile, an electric monopole and two magnetic dipoles.



Unbalanced feed

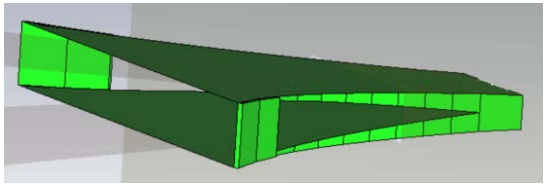


Balanced feed

Inspired from the designs of RF balanced to unbalanced (balun, 1:1) and antennas like balanced antipodal Vivaldi antenna



Traditional Transformer



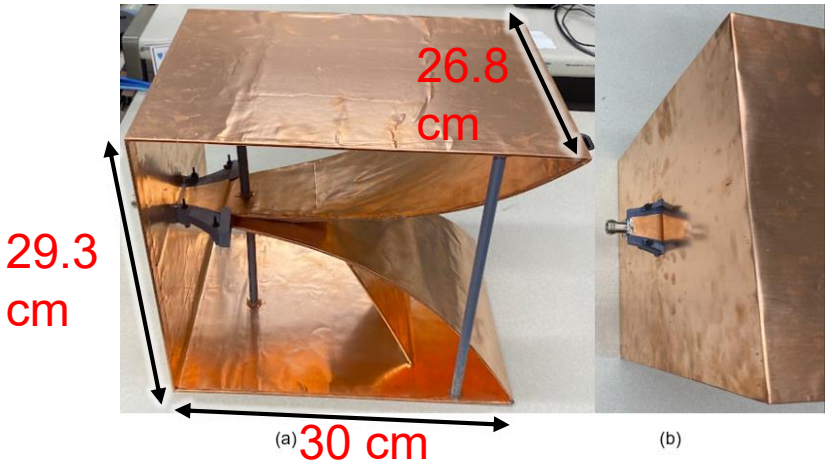
Proposed Transformer

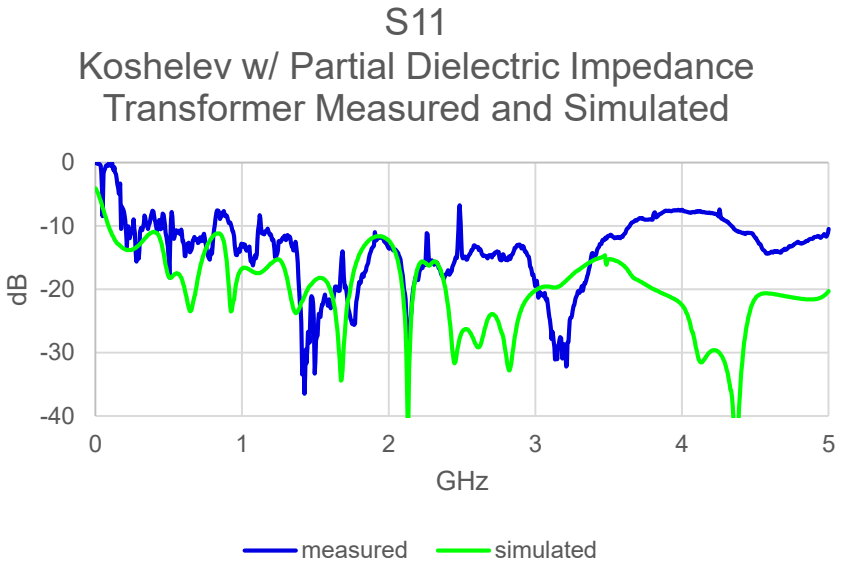
$$v = \frac{\varepsilon_{reff} - 1}{\varepsilon_{ro} - 1}$$

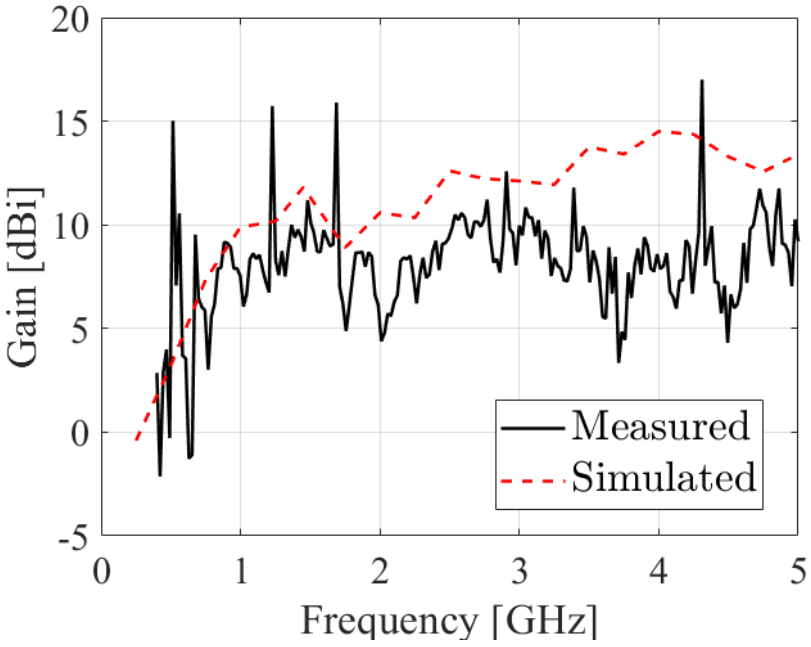
Effective relative permittivity and its corresponding design variable values utilized to design new partial dielectric impedance transformer model.

We have utilized commercial full-wave EM solver CST Studio Suite to design, simulate, analyze and perform tradespace studies.

Koshelev Antenna – Results & Summary







- After a series of iterations, the prototype of single element Koshelev antenna (top left figure) produced expected results.
- The measured reflection coefficient (S_{11}) values agreed with the simulated values (top right figure) from 0.3 to 2.5 GHz.
- The gain measurements (bottom left figure) were performed in a free-space environment with a separation distance of 4 meters.
- A functional 3-D printed Koshelev antenna has been demonstrated that can hold off 10s of MWs of power and <100 ps short pulses satisfying some of the OSPRES-G requirements.

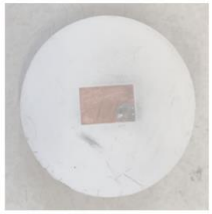
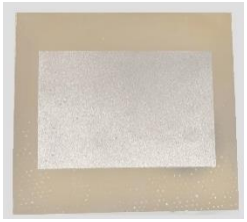
Metrics Comparison – Koshelev vs BAVA

Antenna Metrics		Single Element		4x4 Array	
		BAVA	Koshelev Antenna	BAVA	Koshelev Antenna
Aperture size (H×W) - **cm²**		**12 × 12**	**9.1 × 10**	**63.7 x 63.7**	**55 × 58**
Physical Aperture area (m^2)		**0.0144**	**0.0091**	**0.4058**	**0.3190**
Operating frequency range (fc±BW in MHz)		**900 ± 200**	**900 ± 180**	**950 ± 50**	**900 ± 100**
Peak gain at 900 MHz [dBi]		**3.7**	**4.5**	**14.7**	**15**
Transient Gain (rE/V)		**0.4**	**1.2**	**6.5**	**9.67**
Half-Power (-3 dB) Beamwidth	E-plane	**115°**	**83°**	**26.2°**	**30°**
Aperture Percentage at 900 MHz		**143%**	**243%**	**63%**	**87%**
Scan range at 900 MHz		**N/A**	**N/A**	**±60°**	**±55°**

In a comparison of SOTA BAVA and the proposed Koshelev antenna using simulation data, the proposed antenna exceeds the SOTA antenna performance in most of the chosen metrics. A prototype of the proposed antenna needs to be fabricated to perform one-to-one comparison against the SOTA BAVA.

Outline

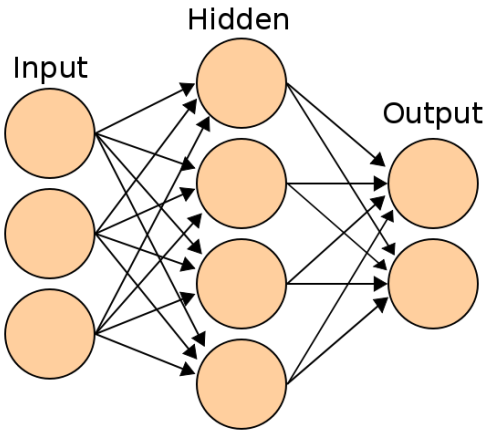
I. Electrically Small Antenna

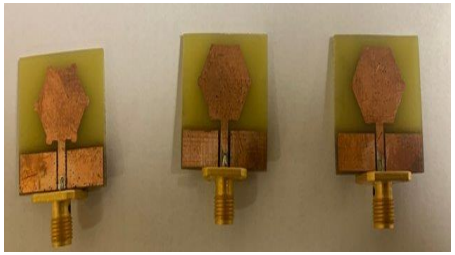

II. Koshelev Antenna with Partial Dielectric Transformer



III. Machine Learning Inspired Antenna Metrics Prediction and Optimization



Machine learning optimized boards



Objective

Objective: The primary objective of this work is to identify and apply machine learning (ML) models to optimize the antenna element and array designs for aperture area reduction using minimal computational resources.

(A) Apply ML models available in Altair Hyperstudy (2021) on an antenna geometry to try and understand the advantages and limitations of ML models.

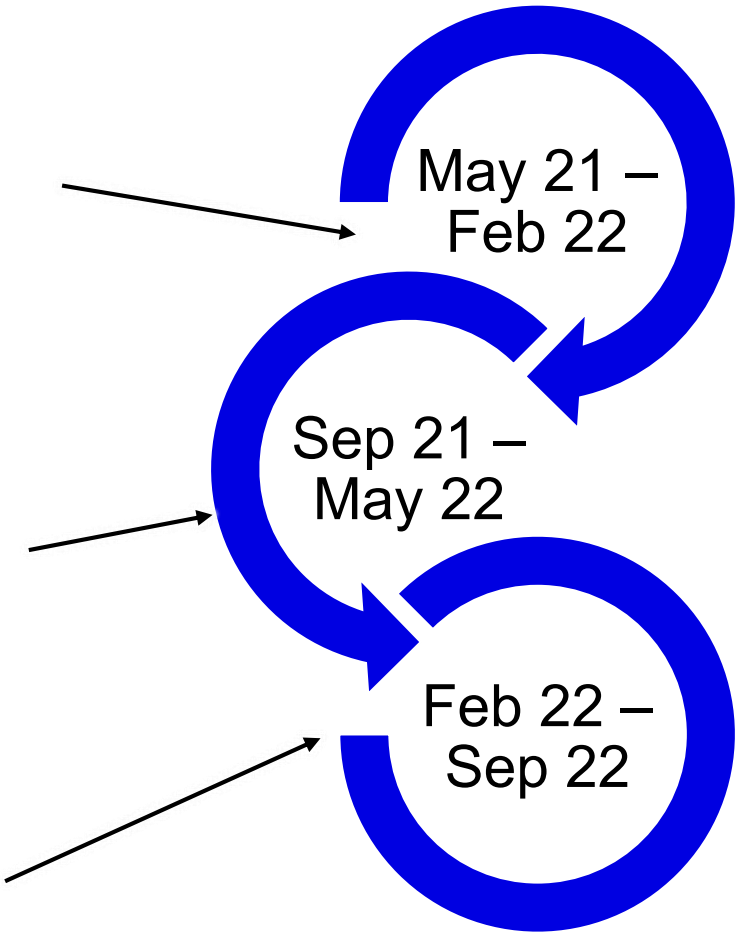
- **Milestone:** Recommend an effective ML model for antenna performance prediction in the time- and frequency domains.

(B) Apply ML models on the antenna array lattice to extend the prediction capability beyond a single element.

- **Milestone:** Recommend the best suitable ML model implemented/developed using Python programming for array antenna metrics prediction.

(C) Develop, validate, and demonstrate a graphical user interface (GUI) to automate the process of employing ML models to predict the antenna output response.

- **Milestone:** Incorporate the developed automated data extraction scripts and ML scripts into the GUI to enable the user to predict antenna response 100x faster than full-wave solvers.



Technical Background and Approach

Conventional antenna array design and simulation includes utilization of full-wave electromagnetic (EM) solvers that are commercially available. Employing optimization solvers such as genetic algorithm and particle swarm optimization on top of full-wave EM solvers is time and memory-inefficient.

We employed supervised ML models such as least square regression (LSR), k-nearest neighbors (kNN) and radial basis function (RBF) to predict the antenna array response after sufficient training and validation.

Conventional Approach

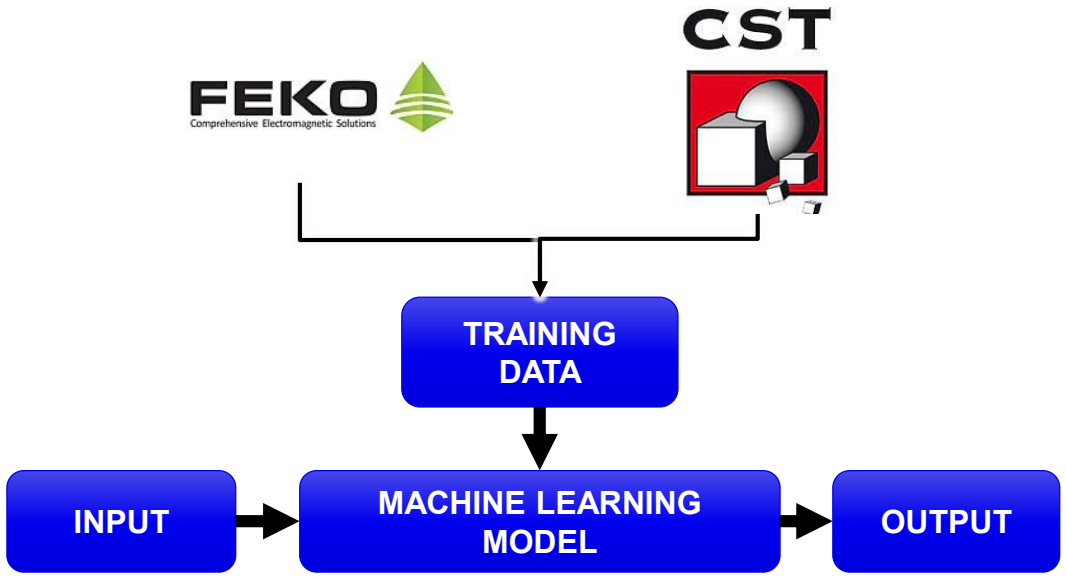
FEKO Comprehensive Electromagnetic Solutions

CST

Ansys HFSS

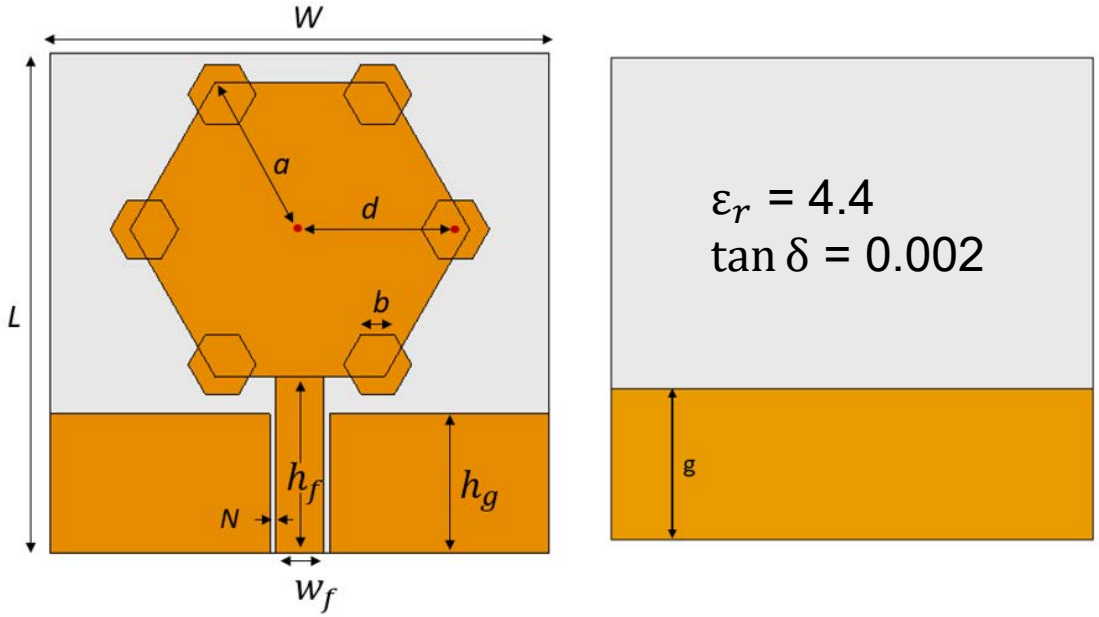
1. Method of Moments
2. Multi-Level Fast Multipole Method
3. Finite Element Method
4. Finite-Difference Time-Domain Method

Proposed Approach



Antenna Element Selection

Antenna Geometry



- For this study, a UWB co-planar waveguide (CPW) Fractal antenna is considered [1] for its low-profile and high-fidelity factor.
- Fractal antenna is a complex design with large number of adjustable parameters which becomes a tedious job to perform parametric study.
- From the initial comprehensive parametric study, we were able to determine that using full-wave EM solvers was computationally expensive, which triggered us to shift our focus to ML-based optimization to cut down the simulation time and yield improvements with a quick turnaround.
- Training data was generated and fed to ML models for antenna response prediction followed by optimization.

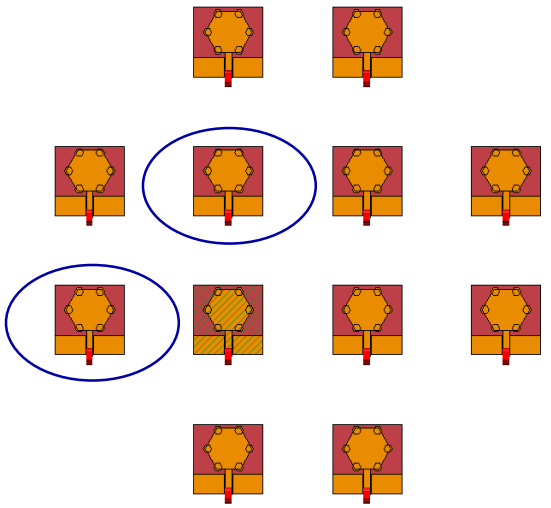
Initial Design Parameter values:

Design parameter	*a*	*b*	*d*	*g*	W_f	h_f	h_g	*L*	*W*	*N*
Value (mm)	8.2	1.7	7.7	2.4	2.4	8.8	7	25	25	0.2

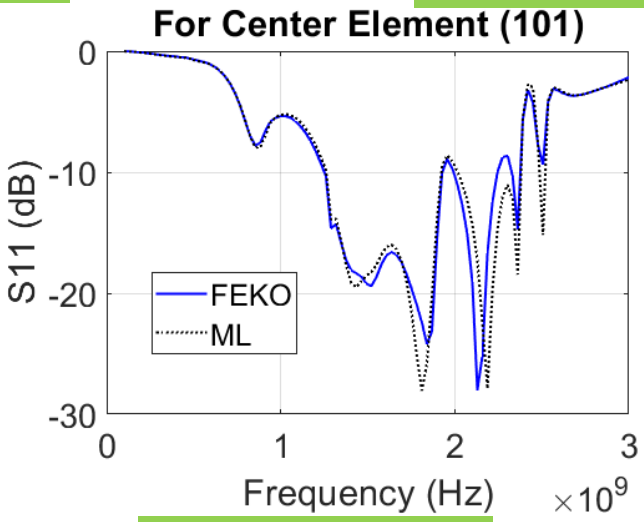
[1] H. Fallahi and Z. Atlasbaf, “Study of a class of uwb cpw-fed monopoleantenna with fractal elements,”IEEE Antennas and Wireless PropagationLetters, vol. 12, pp. 1484–1487, 2013

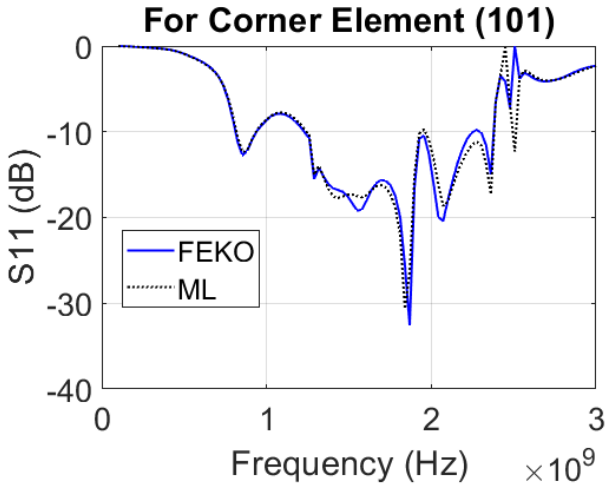
Fractal Antenna Array – ML Prediction

Optimized Octagon Fractal Antenna Array

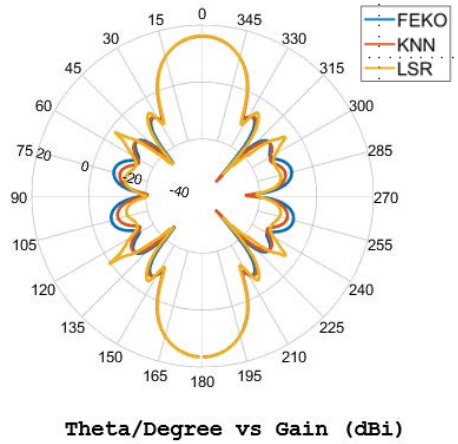


Reflection Coefficient vs Frequency

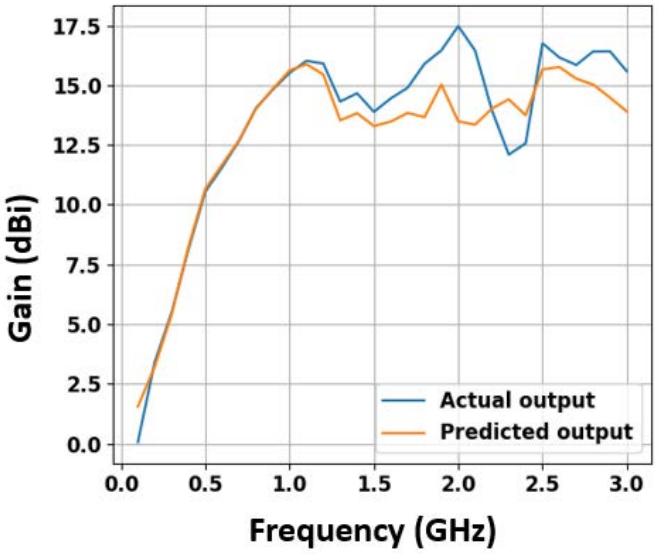




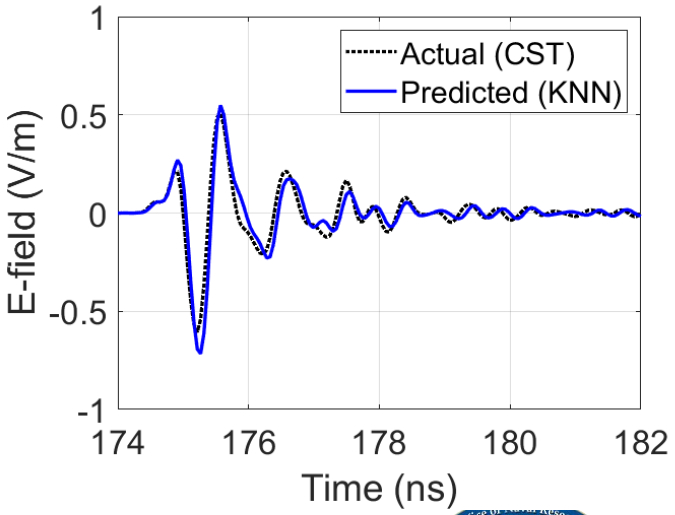
Radiation Pattern



Antenna Gain



Electric Field vs Time



Computational Resources Comparison

$$Root\ mean\ squared\ error\ (RMSE)\ =\ sqrt(mean((y\ -\ \hat{y}\ ).\hat{}2))$$

Antenna Metric	RMSE	
	Single Element	Array
S_{11}	0.04	2.23 (center), 1.73 (corner)
Gain	0.45	1.36
Radiation pattern	N/A	2.42
E-field vs time at 10 meters	0.22	0.04

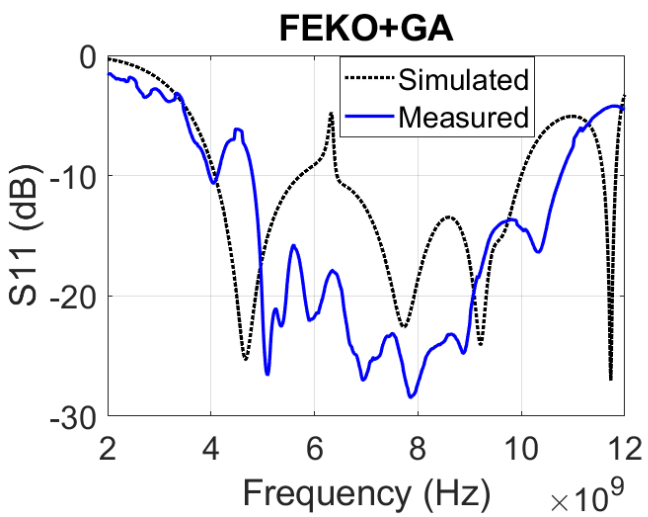
The calculated RMSE values for single element design are significantly lower than 1 while for the array design the values are greater than 1. A RMSE value around 1 is considered as a good prediction in the ML community.

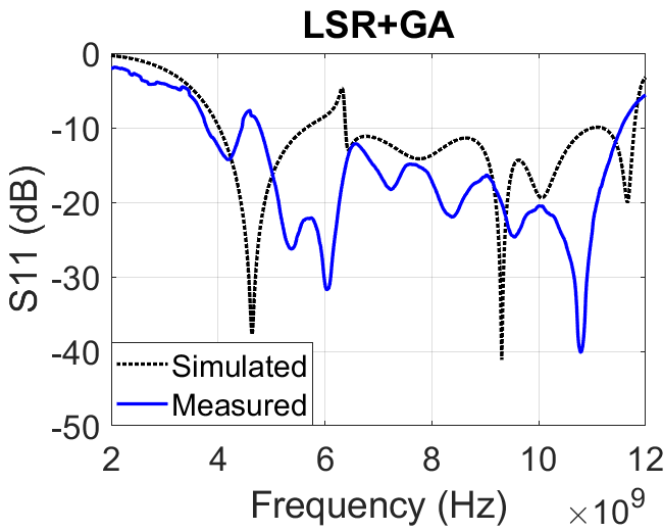
Approach	Computational time for results estimation	Computational time for optimization (on average)
FEKO+GA	~90 mins	4 – 6 days
RBF/LSR+GA	<1 milli sec*	Few seconds to minutes

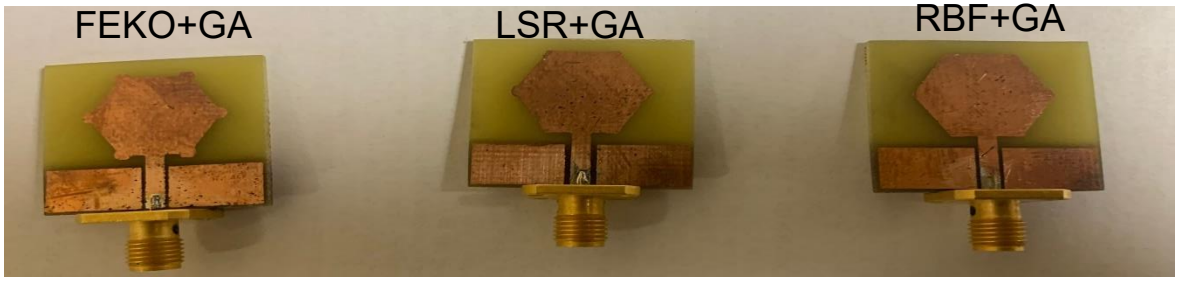
*Does not include simulation time utilized to generate the training data.

The computations were carried out on a Dell laptop with Intel® Core™ i7-10810U CPU @ 1.10 GHz, 4-cores and 16 GB RAM. Computational resources consumed by ML models are very less compared to that of conventional EM solvers.

Measured vs Simulated Results







Approach	Data collected from	F_{lower} [GHz]	F_{upper} [GHz]	Bandwidth [GHz]	Bandwidth [%]
FEKO+GA	FEKO (Simulation)	4.07	9.99	5.92	84
	Photolithography (measured)	4.80	10.76	5.96	76
LSR+GA	FEKO	4.02	11.78	7.76	98
	Photolithography	3.79	11.55	7.76	101
RBF+GA	FEKO	4.13	11.37	7.23	93
	Photolithography	3.84	11.37	7.52	99

The machine learning-based optimization results yielded antenna design variables that produced higher bandwidth than traditional optimization in 1/10th the time. The ML-based optimization effort can be streamlined to desired antenna metric(s) using minimal computational resources reducing the time to design, prototype and evaluate.

OSPRES-G Antenna Team

Deb Chatterjee



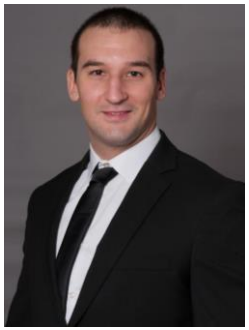
Kalyan Durbhakula



Bidisha Barman



Alexander Dowell



Sai S. Indharapu



Outputs

Journal Publications

In Preparation

- S. S. Indharapu, A. N. Caruso, K. C. Durbhakula, “Machine Learning Assisted Antenna Design Optimization of UWB Fractal Antenna,” TBD, In Preparation, 2022.
- B. Barman, D. Chatterjee, K. C. Durbhakula, and A. N. Caruso, “Tradespace Analysis of Wideband, Electrically Small Microstrip Patch Antenna Elements for Phased Array Applications,” *IEEE Antennas and Propagation Magazine,* In preparation, 2022.

Submitted / Under Revision

- B. Barman, K. C. Durbhakula, D. Chatterjee, and A. N. Caruso, “Comparison of Machine Learning Algorithms for Bandwidth Enhancement of a Coaxial Probe-fed Microstrip Patch Antenna,” Applied Computational Electromagnetics Society (ACES), Under Revision (Accepted with Major Revisions), 2022.

Conference Presentations

- B. Barman, D. Chatterjee and A. N. Caruso, "Probe-location Optimization in a Wideband Microstrip Patch Antenna using Genetic Algorithm, Particle Swarm and Nelder-Mead Optimization Methods," 2021 International Applied Computational Electromagnetics Society Symposium (ACES), 2021, pp. 1-3 [doi].
- B. Barman, K. C. Durbhakula, B. Bissen, D. Chatterjee, and A. N. Caruso, “Performance Optimization of a Microstrip Patch Antenna using Characteristic Mode and D/Q Analysis,” 2020 XXXIIIrd General Assembly and Scientific Symposium of the International Union of Radio Science, Rome, Italy (online conference), Aug 29-Sept 5, 2020, pp. 1-4 [doi].
- S. S. Indharapu, A. N. Caruso and K. C. Durbhakula, "Supervised Machine Learning Model for Accurate Output Prediction of Various Antenna Designs," 2022 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting (AP-S/URSI), 2022, pp. 495-496.
- S. S. Indharapu, A. N. Caruso and K. C. Durbhakula, "Study of Machine Learning Algorithms for Output Response Prediction of an UWB Fractal Antenna," 2021 IEEE Indian Conference on Antennas and Propagation (InCAP), 2021, pp. 510-512.

Summary

- Developed a design technique for electrically small, coaxial-probe-fed, microstrip patch antenna that provides >30% BW at operating frequencies in the UHF (MHz) to microwave (GHz) frequencies. The method avoids any sophisticated prototyping and is a transformative approach in the design of electrically small microstrip antennas for ultrawideband wireless applications.
- Designed and systematically characterized planar microstrip phased arrays with reduced aperture architecture (~ 46% reduction), without significant performance degradation, in terms of boresight gain (< 3 dBi reduction) and beam-steerability.
- A modified and bandwidth improved Koshelev antenna has been developed from 4:1 (unbalanced) to 33.3:1 (balanced) without increasing the aperture area while maintaining the nominal gain over the bandwidth and a high-transient gain value (> 1). A functional 3-D printed and metallized prototype has been developed and compared against its simulation data ensuring a new path to develop low-cost HPM desired UWB antennas.
- The machine learning-based antenna response prediction and optimization approach has demonstrated its viability to develop next-generation HPM-based UWB antenna designs with a specific optimization goal (i.e., aperture area reduction in this context).

Recommendations & Future Work

Transition to PTERA-Grant

- ✓ Investigating into the gain/bandwidth improvement of the designed wideband, microstrip patch antenna elements, using active circuits (composed of non-linear elements).
- ✓ Add optimization algorithms to the GUI and enable users to employ optimization algorithms with the trained ML models.
- ✓ Include a pre-tested RBFNN to the GUI and automate the process of tunning the neural network.

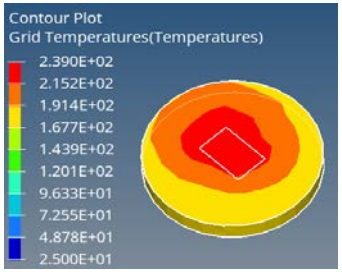
Antenna Element: Power Handling Capability (PHC)

To identify the max. PHC, temperature profile(s) of the antenna(s) are studied subjected to various input peak powers (P_{in}).

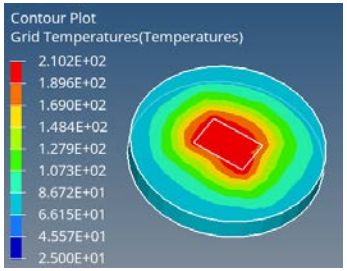
Oxidation temp. of Copper ≈ 200℃
Decomposition temp. [3]
TMM-10i: T_d = 425℃
RT/duroid: T_d = 500℃
Max. PHC of typical SMA ≲ 400 W at 1 GHz [4]

Temperature profiles of antennas [5]

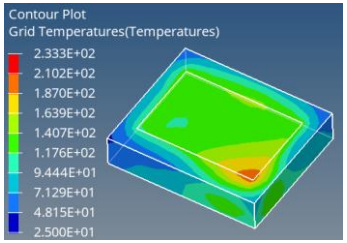
TMM-10i
$f_c = 3.75$ GHz
$P_{in} = 0.25$ kW



TMM-10i
$f_c = 0.815$ GHz
$P_{in} = 5$ kW



RT/duroid
$f_c = 1$ GHz
$P_{in} = 7.5$ kW



Substrate	Freq. (GHz)	Feed	PHC
TMM-10i	2.5-5	SMA	≤ 200 W
TMM-10i ($\varepsilon_r = 9.8$)	0.6-1	Tapered coax	≤ 4.5 kW
RT/duroid ($\varepsilon_r = 2.2$)	0.7-1.3	Tapered coax	≤ 7 kW

Comment: Increased PHC achieved using tapered coaxial feed.



[3] https://www.rogerscorp.com/
[4] https://mpd.southwestmicrowave.com/wp-content/uploads/2020/09/Southwest-Microwave-Power-Rating.pdf
[5] https://www.altair.com/optistruct

Summary

- Developed a design technique for electrically small, coaxial-probe-fed, microstrip patch antenna that provides >30% BW at operating frequencies in the UHF (MHz) to microwave (GHz) frequencies.
- The method avoids any sophisticated prototyping and is a transformative approach in the design of electrically small microstrip antennas for ultrawideband wireless applications.

Antenna Type	Volume	Freq. Range (GHz)	Gain (dBi)	Pol.
IRA [6]	2.24×10^{-2}	0.18-7	~ 10	-
Combined Antenna [6]	2.7×10^{-2}	0.18-7	~ 10	-
Magnetic EZ [7]	$\sim 9 \times 10^{-5}$ $(ka = 0.436)$	0.51	-	-
Probe-fed microstrip patch – TMM10i (proposed)	9.5×10^{-4} $(ka = 0.67)$	0.6-1	5.67	Circular (2.9-3.2 GHz) Linear (otherwise)

- Designed and systematically characterized planar microstrip phased arrays with reduced aperture architecture (~ 46% reduction), without significant performance degradation, in terms of boresight gain (< 3 dBi reduction) and beam-steerability.

[6] S. -F. Wang and Y. -Z. Xie, "A Method to Evaluate the Performance of Ultra-Wideband Antennas for the Radiation of High-Power Electromagnetic Pulses," *IEEE Trans. Antennas Propag.*, vol. 70, no. 8, pp. 7142-7146, Aug. 2022.
[7] J. Ng, R. W. Ziolkowski, J. S. Tyo, M. C. Skipper, M. D. Abdalla and J. Martin, "An Efficient, Electrically Small, Three-Dimensional Magnetic EZ Antenna for HPM Applications," *IEEE Trans.Plasma Science*, vol. 40, no. 11, pp. 3037-3045, Nov. 2012.

Machine Learning

- An algorithm that leverages data for performance predictions or decisions without being explicitly programmed to do so.
- Learning corresponds to adjusting the values of the parameters in the model.

$$y = f(x)$$

$$(s_{11}) = f\ (design\ parameters)$$

Output *Trained model* *Input*

From EM solvers

Generate Data

↓

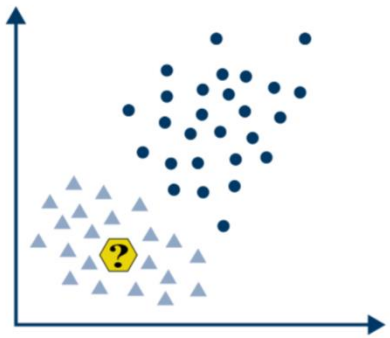
Train model

↓

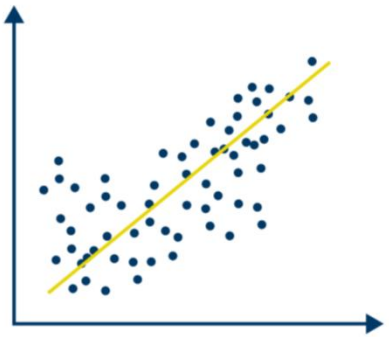
Evaluate model

↓

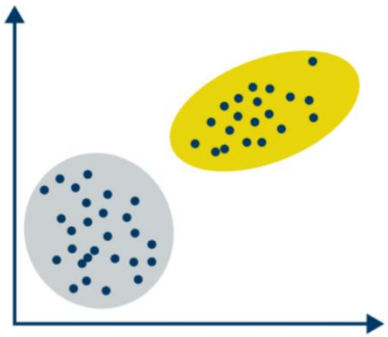
Deploy as a surrogate model



Classification

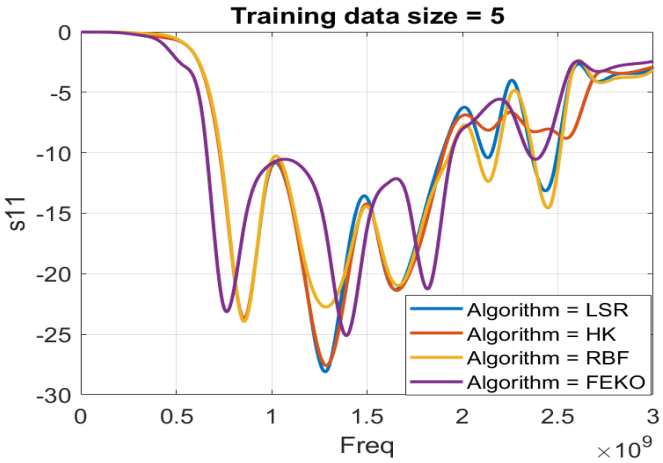


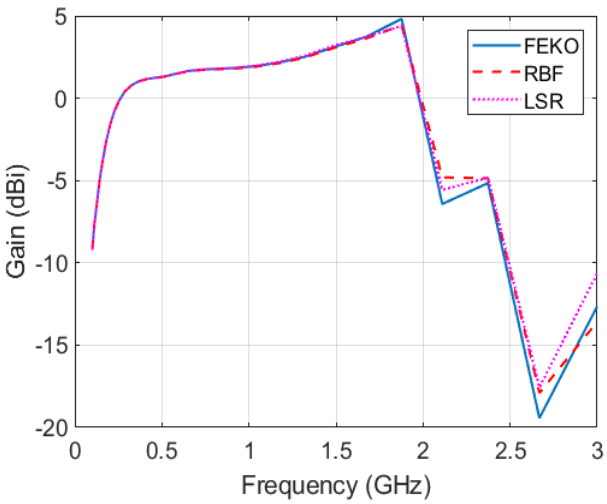
Regression

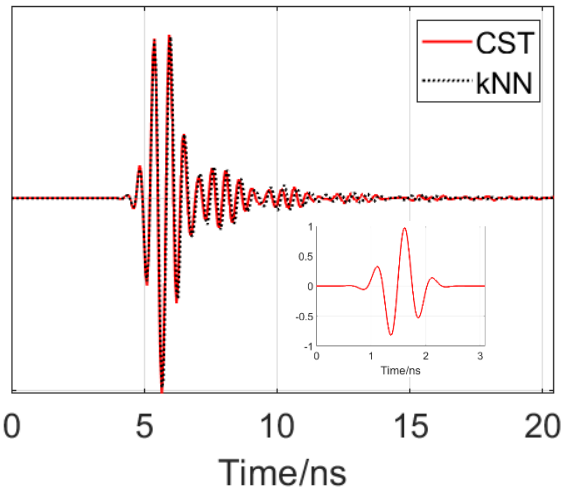


Clustering

Fractal Antenna Element - Results







Antenna output response		RMSE values	
		RBF	LSR
S_{11}		0.04	0.01
Gain		0.45	0.53
E-field (frequency domain) at	100 mm	0.02	0.02
	200 mm	0.39	0.72
	300 mm	0.35	0.92
E-field (time domain)		0.22	

The gain and electric field responses predicted by the ML models and the kNN model have shown good agreement with that of FEKO/CST results.

The root mean square error (RMSE) values in all of these cases have remained below 1, which is an indication of well-trained models.

Antenna Element Type	Aperture size (mm)	Physical Aperture area (mm^2)	Bandwidth	Peak gain (900 MHz) (dBi)	HPBW at 900 MHz		Aperture Percentage
					E-plane	H-plane	
SOTA BAVA	90 × 90	0.0081	10:1	3	Unknown	Unknown	217%
Fractal Antenna	93 × 85	0.0079	3.33:1	2.58	83.2°	96.2°	208%

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for c-sUAV Study (OSPRES Grant)

N00014-17-1-3016
09/30/2017-09/29/2022

Optical Fiber Lasers and Amplifiers

Scott Shepard

shepardsr@umkc.edu

DISTRIBUTION STATEMENT A: Distribution authorized to all OSPRES Grant and Contract performers, and any uncompensated OSPRES collaborators. Further dissemination per the Office of Naval Research, Ryan Hoffman (ryan.b.hoffman.civ@us.navy.mil, 703-696-3873) or higher DoD authority.

Motivation – The Problem

Laser size and costs have long been the Achilles heel of **HPM** systems, in which they are used to trigger a **PCSS** (photoconductive semiconductor switch).

Fiber Lasers comprised of optical fiber amplifiers, fed by a low-power stable seed laser diode, can offer a cost-effective, low-weight and small-volume solution. Larger surface areas of active media also diminish the cooling requirements.

.



⇒



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Problem is even fiber lasers **cost** too much (if **power** such that one per PCSS).

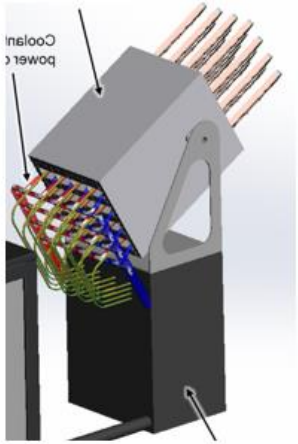


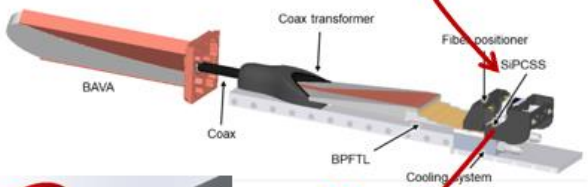
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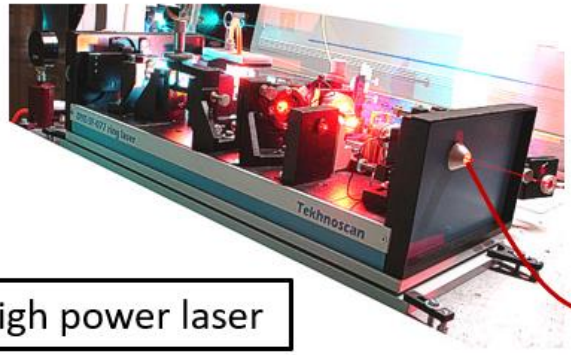


Motivation – the tie to the OSPRES Mission

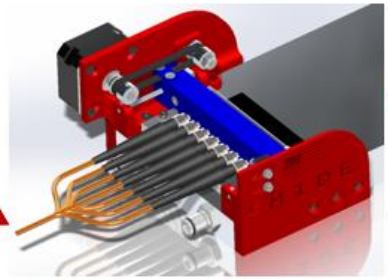








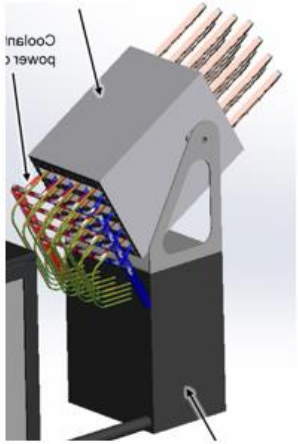
High power laser

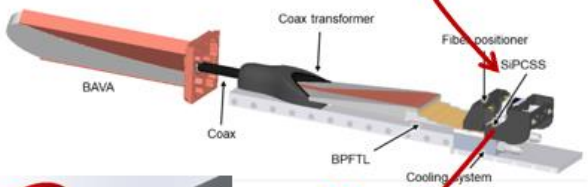


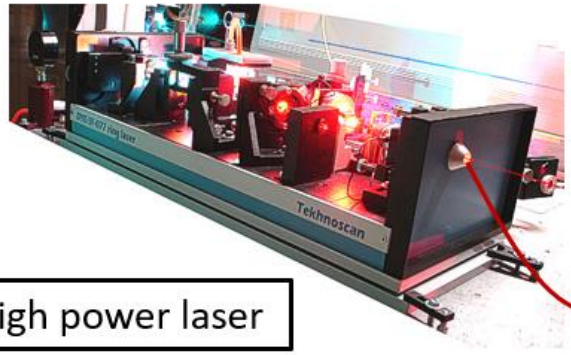
Triggers the PCSS

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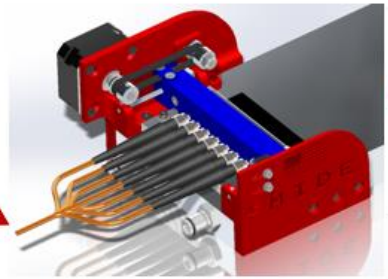








High power laser



Triggers the PCSS

System **cost** also lower If **power** high enough to trigger ALL PCSS in an array.

Motivation – Fiber Laser SOTA and Deficiencies

State-of-the-art (SOTA): Yb-doped fiber amplifiers optimized for LIDAR, cutting…

Deficiency in SOTA: Optical pump power system costs account for over 50% of the budget for each laser (in this class, for optical fiber as well as normal/free-space embodiments).

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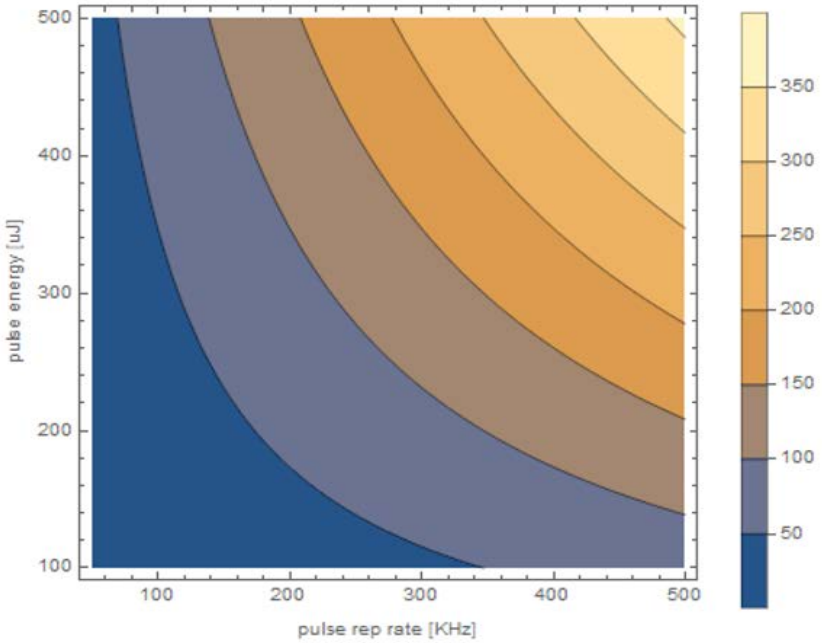
Pump Power Cost [in K$]

- **e.g., at 240uJ and 500kHz we'd have**
  - **172.8 K$ for that Pave = 120 W case**

c = 1.44 Pave

c in [K$] COTS

Pave in [W]



Pave = PRR Ep

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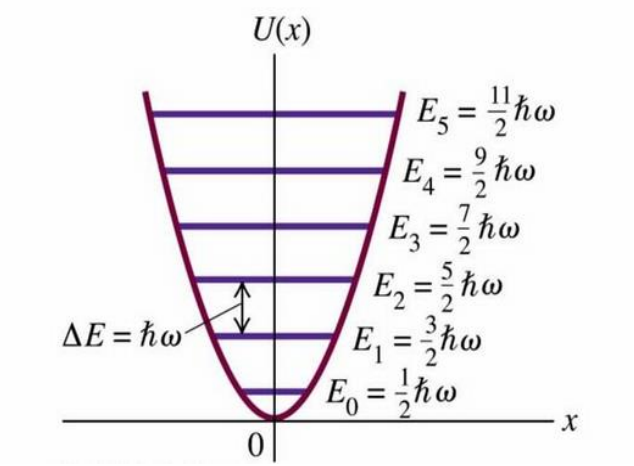
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Linear gain theory says
Pase = h f (G-1) BW

At 1064 nm with a 1 nm optical BW that's 49.5 nW (G-1)

With G = 8 x 10^(6) we'd be over the 100 uW "limit" (for heating due to ASE-induced PCSS leakage current) by a factor of 3960 !

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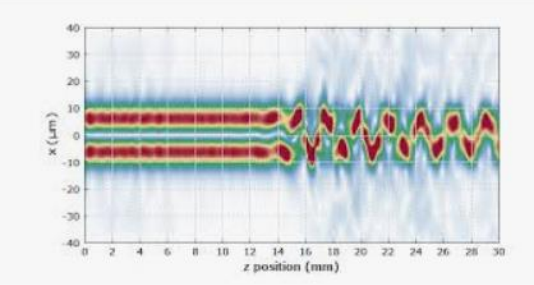
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Deficiency in SOTA: Amplified spontaneous emission (ASE) noise creates timing-jitter (limiting HPM steerability) and heat.

Deficiency in SOTA: Fiber nonlinearities limit laser operating power.

Fiber amplifiers with cores of **circular** cross-section have reached a fundamental limit due to the conflicting constraints of thermal lensing (proportional to core area) and nonlinear impairments, such as stimulated Brillouin and stimulated Raman scattering (inversely proportional to core area).

Thermal lensing like self-focusing cause beam to break-up and/or be cast out of the core.



Objectives

Objective 1: **Reduce the overall laser system cost by a factor of 2.**

Proposed Solution: **A pre-burst optical pumping scheme to reduce costs by more than 2.**

Program outcome: **Simulations reveal that our technique can reduce optical pumping power costs by a factor of 40, with tolerable pre-burst ASE enhancement.**

[improvement factor = 1/(duty-cycle of burst)]

Example: high performance laser of 240 uJ/pulse at 500 kHz rep. rate

(120 W) originally at 173 K$ in pump power cost could be pumped for only 4.3 K$.

It breaks the "pump power cost bottleneck."

Objectives

Objective 2: **Develop a low timing-jitter fiber laser at higher operating power.**

Proposed Solution: **Exploit gain saturation to suppress the ASE;**

and alter the fiber core to a tubular geometry to mitigate nonlinearities.

Program outcome: **Simulations show:**

gain saturation (in a properly staged design)

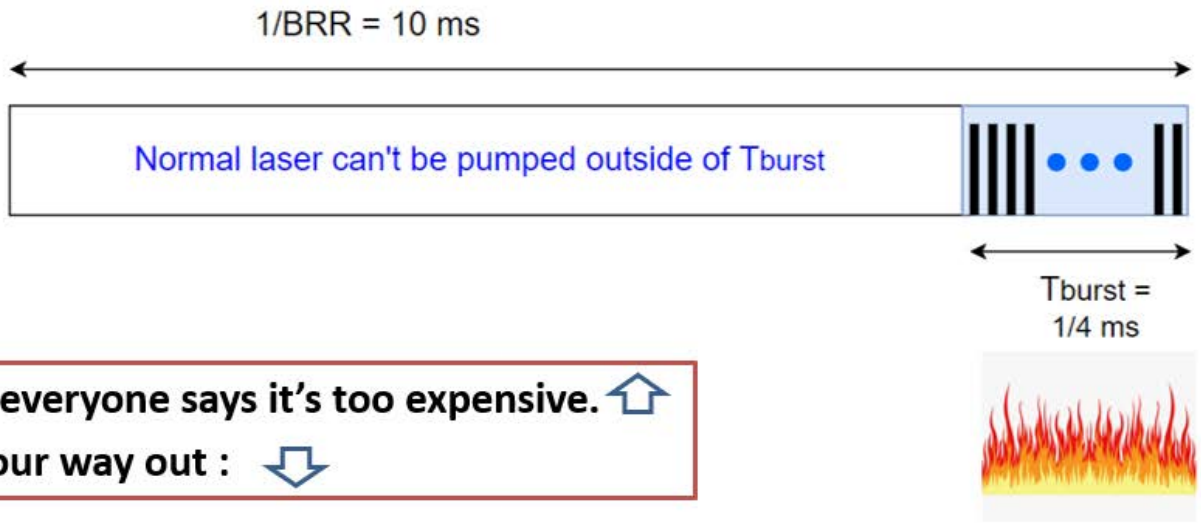
can suppress ASE by 3 orders of magnitude;

and tubular-core power amplifiers

can improve the power limit (from self-focusing) by

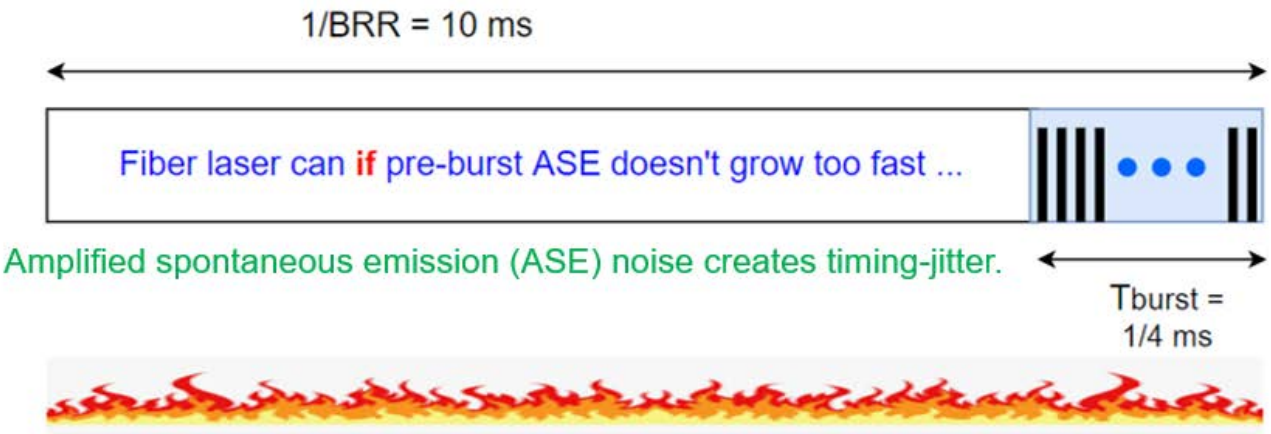
2 orders of magnitude.

Pump Power Cost Reduction (can pump low and slow, if…)



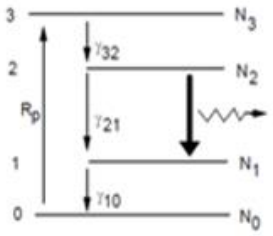
That's why everyone says it's too expensive.

But here's our way out :



A Simple Gain Model (with saturation but without fiber nonlinearities)

THE EQUATIONS



$$\frac{d}{dt}N_2 = -\frac{N_2}{\tau_L} - 2^*\sigma v_g N_2 n_L + R_p$$
$$\frac{d}{dt}n_L = -\frac{n_L}{\tau_p} + 2^*\frac{\sigma v_g}{V}N_2\left(n_L + \frac{1}{V}\right).$$

$\gamma 10$ *is fast so* $N1 \sim 0$

BECOME =>

$$\frac{d}{dt}g = -\frac{g - g_0}{\tau_L} - \frac{gP}{E_{sat}}$$
$$\frac{d}{dt}P = -\frac{1}{\tau_p}P + \frac{2g}{T_R}(P + P_{vac})$$

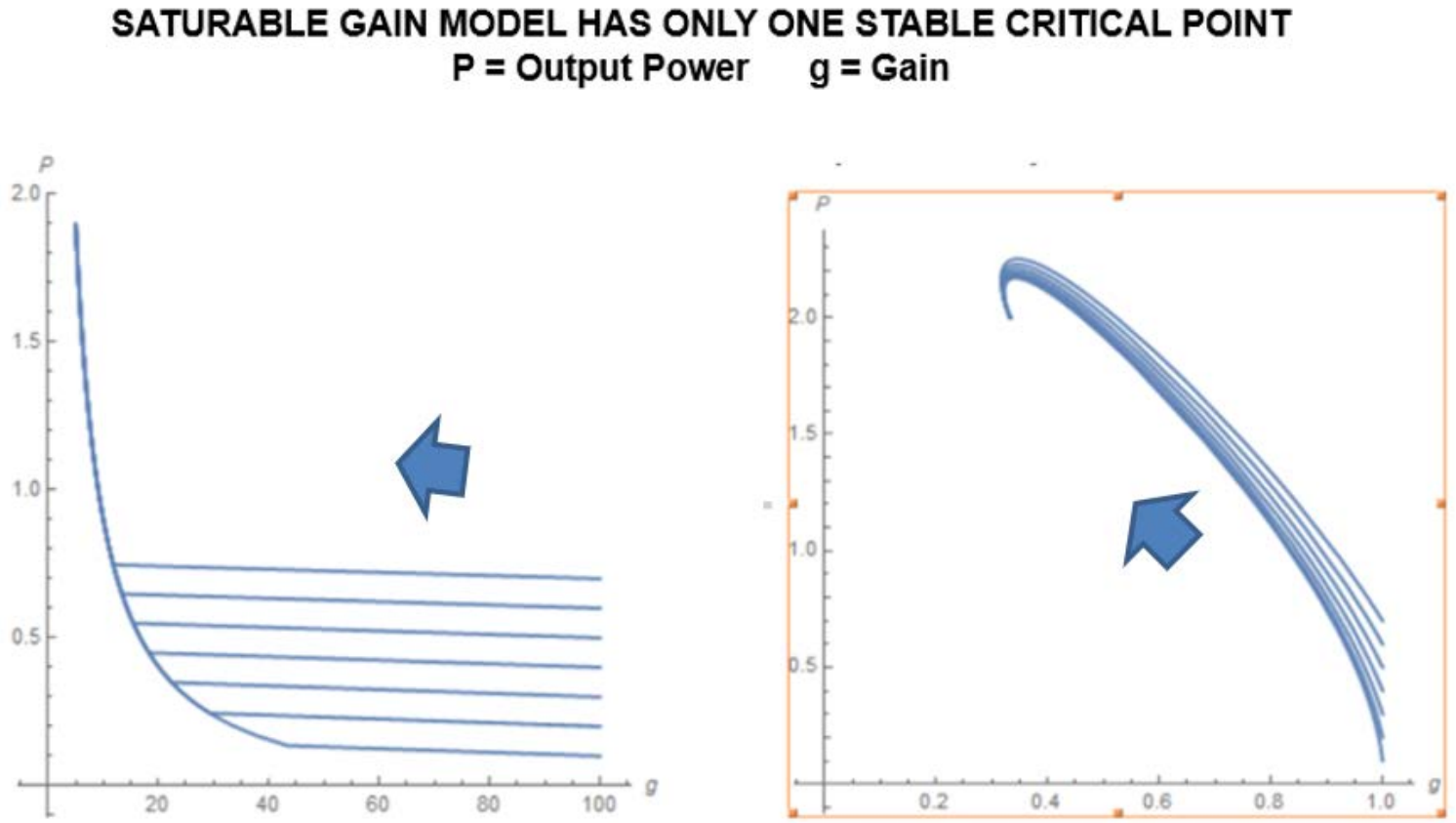
THE CONSTANTS

g_0 = initial gain, linearly proportional to the pumping rate/pump power
T_p = cavity loss time constant (or loss per length in fiber amp)
$E_{sat} = P_{sat}\,T_L$ where T_L = "T1" = "T_{sp}" = spontaneous decay rate time constant
and P_{vac} = ½ (h f) BW > 1 nW at 1064 nm is what turns into ASE

Technical Background and Approach

We design the saturation point parameters (core diameter…)

in each amplifier stage to suppress the ASE.



Technical Background and Approach

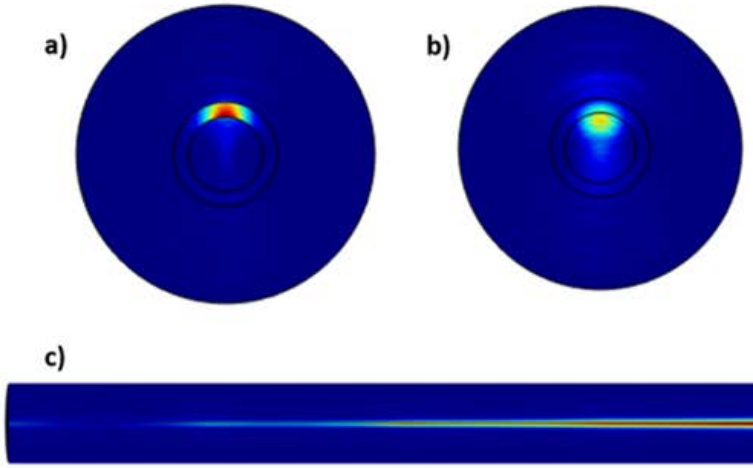
Higher power operation by changing core geometry from circle to tube

thermal advantages but also...



Nonlinear scattering limits the energy in circular and rectangular core fiber; but a tubular geometry can collect such into a hollow-core mode in air.

a) Gaussian spot input on glass tube



b) refracts preferentially to inside of tube

c) causing growth of air-core mode

Results – Pump Power Cost Reduction

Factor of 40 example

- @ burst rep.rate = 100Hz there's 10,000 usec (10 ms) per burst
  - which is huge w.r.t. Tburst = 250 usec
- Now Ed = N Ep of interest and Ed = (Pave)(Tburst)
  - for classic example (like our Neolase) of Ep = 240uJ and N=125
  - Ed = 30 mJ which is also = (120 W) (250 usec)
- To supply that we only need Pbr = (30 mJ)/(10ms) = 3 W !!

Bottom line ⇒

- Like a "gigantic pulse" or "Q-gated" laser
  - we build for a long time then "let 'er rip"
  - then nonlinearities clobber us but at least we've a way out of the pump cost bottleneck

Trick only works because:

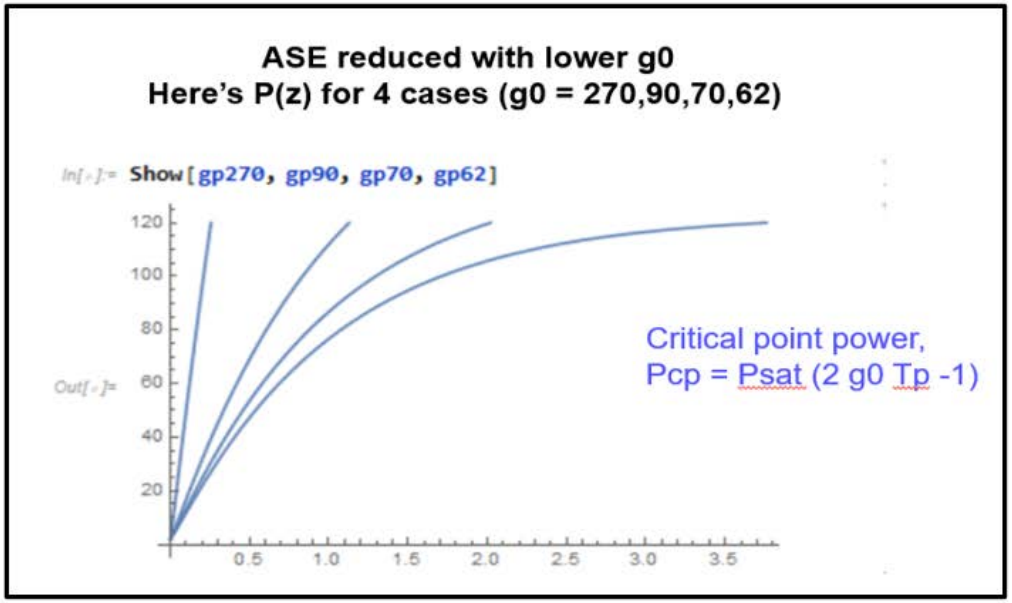
1) we can hold pump power for 10 ms and
2) our ASE doesn't grow much in 10 ms

Results – ASE suppression via gain saturation

Lower the critical point to our operating point

Linear gain theory said we're too high by 3960

But our gain isn't linear – it saturates !



Lowering g0
lowers P_{cp}
but fiber longer

We can also lower $P_{sat} = I_{sat} A_{eff} \sim d^2$
where d = fiber core diameter
So…

Results – ASE suppression via gain saturation

Factor of 9,525 example

now … have a practical design example

for G = 8 x 10^6 case

which beats the factor of 3960



- **ASE suppressed by 9525**
- we lowered Pcp via g0 and Psat (via mode diameter d)
- while keeping d above damage thresholds in each stage

Results – High Power Optical Amplifier Tube

Factor of 100 example

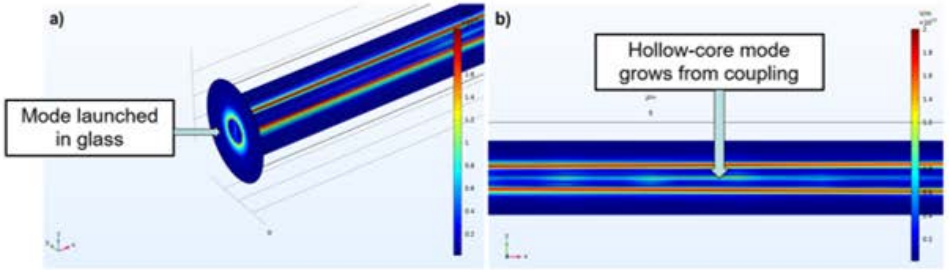


Thermal Advantages of tubular core over circular and rectangular core fiber

Thermal mode instability and thermal lensing limit operating power.
We circumvent these via:

- **a matter of scale**
  a 2.5 mm outer diameter Yb-doped tube, of 100 micron thickness
  increases the surface area (hence the heat transfer) by a **factor of 100** and
  increases the cross-sectional area (hence nonlinear thresholds) by **204**
  with respect to a 50 micron core fiber of the same unit length
- **the existence of a hollow-core mode which supports propagation in air**
  thereby acting like an **energy reservoir** for the glass tube amplifier

Results – High Power Optical Amplifier Tube



Nonlinear Scattering Advantages of tubular over circular and rectangular core fiber

Self-focusing (from the intensity dependent refractive index of any glass) scatters energy out of a waveguide and so limits its operating power.

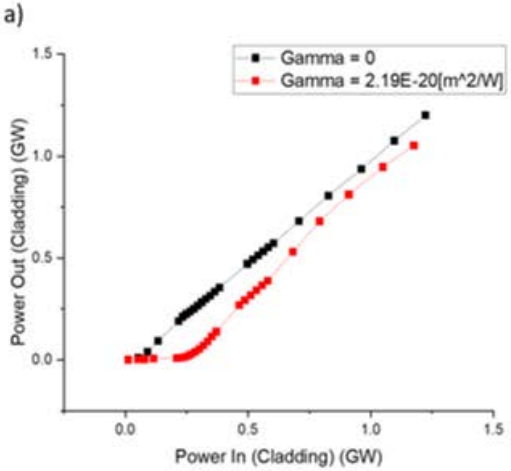
The tubular geometry dramatically reduces this limit via:

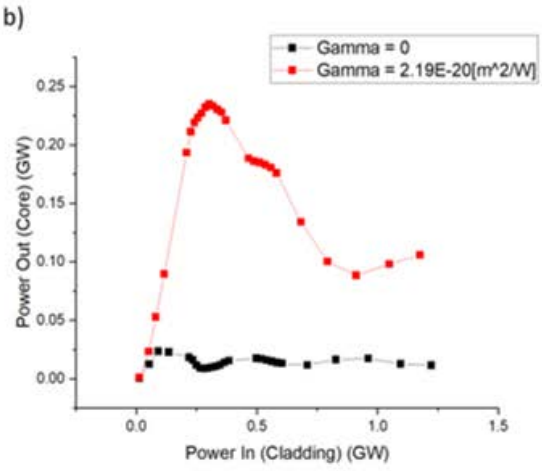
- **symmetry breaking**
  a **preferential scattering** of light towards the **inside** of the tube is caused by the curvature of the surface (in contrast to a flat rectangular slab waveguide for which the scattering would be symmetric; i.e., equal on both sides)
- **an accumulation effect**
  energy (which would have been lost) is coupled into the **hollow-core mode**

Results – High Power Optical Amplifier Tube

Now call air "core" and glass "cladding"

Refractive index
$n = n_0 + \gamma I_0$
depends on
intensity I_0





$\gamma \neq 0$ creates
self-focusing

a) Power Out of the **cladding**/glass (where it's launched) is reduced when $\gamma \neq 0$. **Self-focusing acts to throw energy out of the glass cladding.**

b) 96% of the dispelled energy **gets trapped in** the **core**/air (demonstrated here for an operating point range of 1 MW to 1 GW).

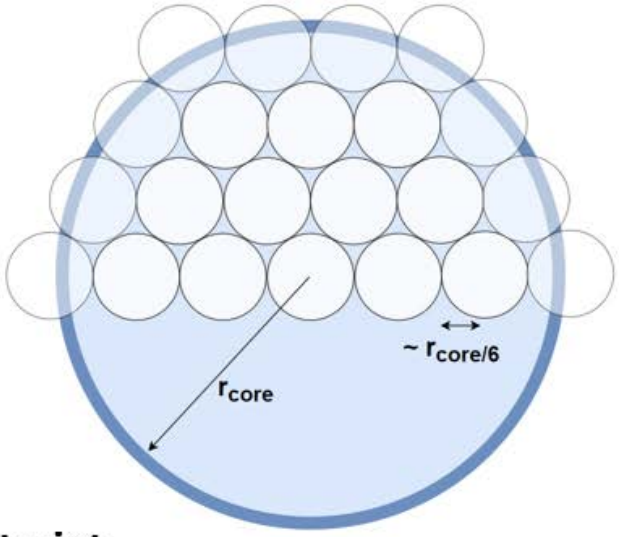
Note: we can control the coupling by simply adjusting the operating point.

Results – High Power Optical Amplifier Tube

Core up to 1 GW and cladding up to 10 GW

Applications of tubular core high power amplifiers include HPM and HEL.
In HPM: we could drive an array of (up to 100) Si-PCSS with a single laser.

Splitting a tubular amplifier output into 37 passive power-delivery fibers (22 shown) would drive 12 PCSS with 3 passive power-delivery fibers each.



- **eliminates optical timing-jitter constraint**
  since each power delivery path is passive they cannot contribute to jitter
- **output beam profile controlled by simply adjusting the operating point**
  from uniform (for HPM) to Gaussian (for HEL)

Outputs & Personnel

- **S. R. Shepard and H. A. Thompson, "Self-focusing in Guided and Un-guided Media," presented at the *2021 OSA Nonlinear Optics Topical Meeting, Virtual Event*, August 9-13, 2021.**
- **Presentations at: DE-CDEW Program Review (2022); NRL virtual meeting (2022); LLNL virtual meeting (2021).**
- **Invention Disclosures:**
- **Shepard, "A Low Noise Optical Amplifier," 21UMK007, 14SEPT2020.**
- **Shepard, "A Novel Optical Fiber Amplifier," 20UMK012, 02JUN2020.**

- **Students**
  - Heather Thompson
  - John Bhamidipati

Summary – Most Significant Findings

- **Our pre-burst optical pumping scheme simulations showed that we can drop the pump power costs by a factor of 40 with pre-burst ASE power levels below the heating level tolerance of 100 μW.**
- **For a proposed system gain of 8 million, a linear gain theory predicted the in-burst ASE would be over our heating level spec. by a factor of 3960, but by exploiting the nonlinearity of gain saturation we find that we can suppress the ASE by over 7000.**
- **We made (to our knowledge) the first observation of self-focusing effects that are not determined by beam power alone. We found instead that these can also be controlled via the geometric factors within a waveguide (such as fiber core diameter).**
- **We made (to our knowledge) the first observation that a mode exists in the air within a simple glass tube into which we can couple energy from the mode in the glass. Thus, an amplifier (in the doped and pumped glass) can operate at higher powers.**

Summary – Most Significant Findings

- Advancements in the very high-power operating point (tens of GW) of our tubular optical amplifier (and the existence, size and spatial uniformity of its air-core mode) were shown to permit a single laser to trigger an array of several (up to 100) Si-PCSS – reducing the laser system cost and eliminating the optical timing jitter constraint. The symmetry breaking of the scattering from self-focusing in a curved waveguide was shown to enable such.
- We calculated SWaPC improvement examples for the use of a single optical power tube to drive an array of PCSS (relative to a normal free-space implementation of the laser system) finding a cost reduction factor (for a 100 element array) of 83 at reduction in size by a factor of 290. For a 12 element array these improvement factors are 21 and 35.
- Complicated entrance optics for the tubular amplifiers greatly simplified by passively splitting a single source into a 4 “spots” to illuminate the wall of the tube. Found that with 4 spots of radial polarization we can still achieve GW core and 10 GW cladding power levels.
- Showed that one device can cover both DoD applications of HMP and HEL by simply changing the operating power point to adjust the output beam profile from almost uniform to almost Gaussian (respectively).

Recommendations & Future Work

- **Power combiners are important components in high-power fiber laser systems and to that application we have shown (in recent MSRs) how one can leverage our power tube technology via: tubes within tubes (which are mode-coupled) and/or spectral combiners.**
- **Therein water in a glass tube outperforms commercially available photonic crystal fiber (with a 90% transmission bandwidth of 300nm, in comparison to 80nm, at a length of 2 meters).**
- **Our understanding of how arrays of mode-coupled tubes can yield photonic resonances at optical frequencies maps into similar effects realizable at RF (600 MHz to 6 GHz). Thus, much of this work is being transitioned into PTERA objectives for the design of novel reconfigurable patch and horn antennas.**

ONR Short Pulse Research, Evaluation and non-SWaP Demonstration for c-sUAV Study (OSPRES Grant)

N00014-17-1-3016
09/30/2017-09/29/2022

Design and Development of a Jet Impingement Thermal Management System for a Semiconductor Device with the Implementation of Dielectric Nanofluids

Sobhansarbandi, Berg, Clark, Sisk

sarvenaz@umkc.edu

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Spring 2022-Present

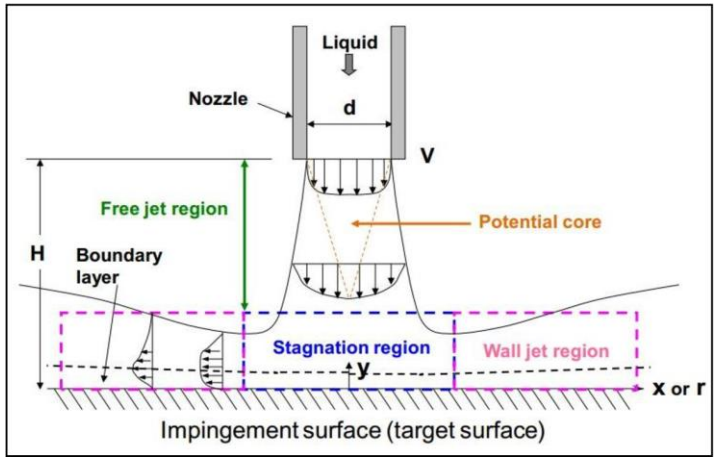
Outline

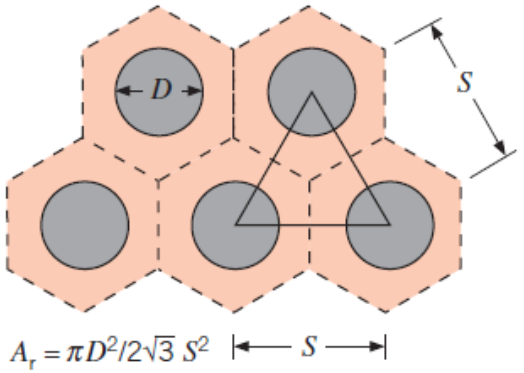
- Motivation
- Timeline and Objectives
  - Milestones
  - Phase I-Task 1: Various TMS Design/Developments (Berg)
  - Phase I-Task 2: Fabrication of TMS Design/Developments (Berg
  - Phase I-Task 3: Heat Transfer Fluid (HTF) Analysis (Berg)
  - Phase I-Task 4: CFD modeling with the selected HTFs
  - Phase II: IC-TMS (Clark)
  - Phase III: UC-TMS (Sisk)
- Technical Background and Approach
- Results
- Outputs
- Summary
- Recommendations & Future Work

Motivation

- ***Primary Problem:*** A thermal management system (TMS) is required for cooling semiconductor-based pulse-power devices with the goal of maintaining the device temperature below 80 ℃ to avoid chip malfunctions. In-line with the SWaP-C^2 objectives, the proposed TMS must be capable of providing 1 kW/cm^2 cooling rate to account for the amount of applied heat flux to the surface of the chip. Moreover, certain limitations should be considered for the pumping power. The TMS should be designed to be small enough to be used anywhere from data centers to drones, thus 1 cm^2 is targeted, with the capability of scaling up the dimensions.

- ***Solution Space:*** To achieve such high cooling densities, we propose a modified jet impingement TMS (JI-TMS) design which is expected to achieve an enhanced heat transfer rate due to the creation of turbulent flow by the unique design of nozzles array.



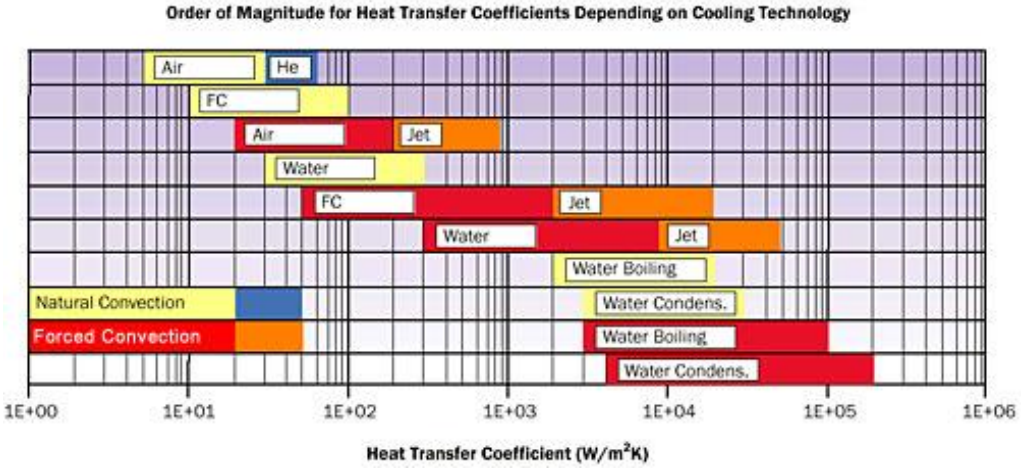


Motivation

- ***Sub-Problem:*** The turbulency formed from the array of nozzles on the targeted surface creates an extreme pressure loss, which is mainly from the large amount of jet nozzles impinging fluid streams interfering with other fluid streams. The pressure must be sustained to enable proper cooling and circulation processes.

- ***State-of-the-Art (SOTA):*** Integrated chip cooling is being widely used to dramatically increase the operational power of high-voltage silicon-based power devices. High power density electronics employing JI-TMS's have achieved 10's-of-kW of average power handling capabilities.

- ***Deficiency in the SOTA:*** Current SOTA devices: a) include thick thermal interface layers that increase the amount of material through which heat must be transferred to the coolant, thus limiting the heat removal rate; b) rely on working fluid in both natural/forced convection; c) Chiller/pump systems consumption of power to produce thermal compensation, extreme pressures (100's-of-psi) to achieve optimal flow regime and cooling metrics.

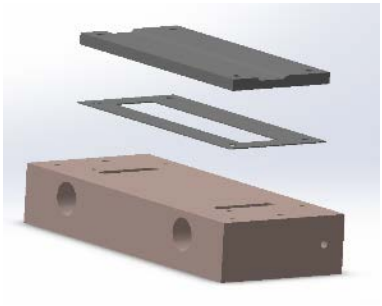


Lasance, C., Technical Data column, ElectronicsCooling, January 1997.

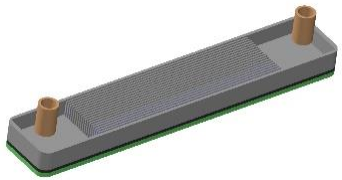
Timeline and Milestones

Tasks & Milestones	40 Months																			
	M1-M6			M7-12			M13-18			M19-M24			M25-M30			M31-M36			M37-M40	
Phase I, Task 1: Design and Comparison of Various TMS by CFD Modeling (Berg)																				
Milestone 1: Desired design obtained, further needed modifications identified					■															
Phase I, Task 2: Fabricated and tested the selected design with identified properties in Task 1 (Berg)																				
Milestone 2: Experimental and simulation results cross-validation, further needed enhancement on the heat transfer fluid identified					■															
Phase I, Task 3: Thermal analysis of nanofluid based heat transfer fluid is performed by investigating the performance of 19 samples with different concentrations, properties of interest are specific heat capacity and thermal conductivity. (Berg)																				
Phase I, Task 4: CFD modeling of the TMS with the optimized HTF with high thermal capabilities (Berg)																				
Milestone 3: Target heat removal rate achieved and the device temperature was well maintained below the desired operating temperature														■						
Phase II: Design of a water-cooled integrated cooling system (Clark)																				
Phase III: Design of a water-cooled ultra compact TMS (UC-TMS), with modified design of arrays of jets with the increased number of outlets to eliminate the pressure loss issue (Sisk)																				
Milestone 4: Ultra Compact TMS design with high heat removal capability																				■
	Deliverables																			
Technical reports																				
Journal, Conference Publications and Presentations																				
Final report																				

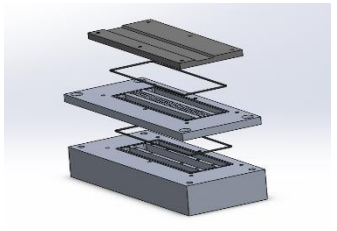
Objective (Berg)



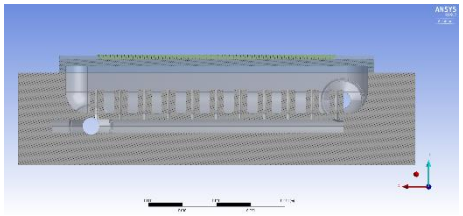
Crossflow
(also a microchannel design)



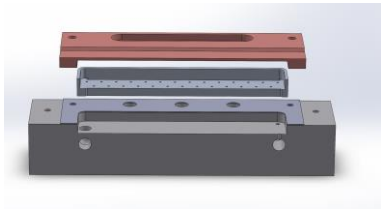
Microchannel



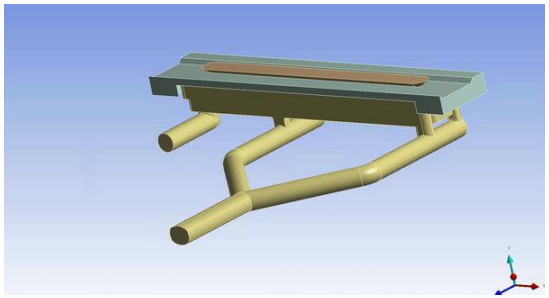
Array Jet Impingement



Single Row Jet Impingement

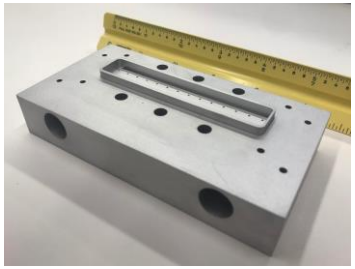


Staggered Jet Impingement

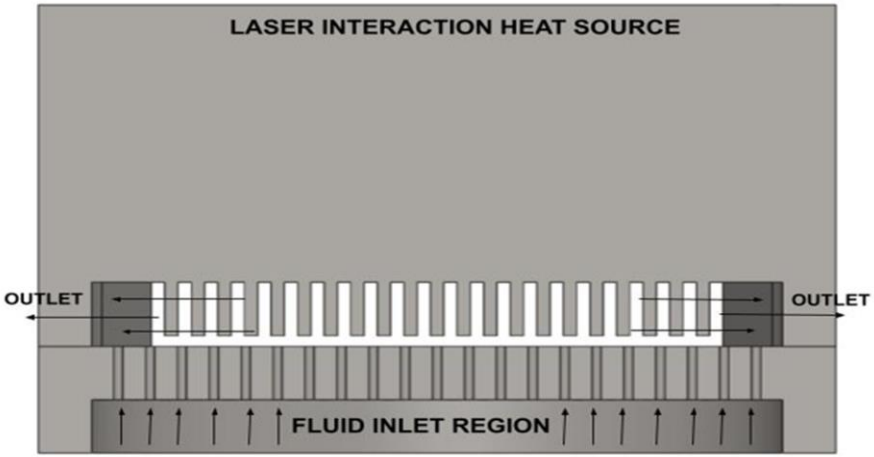


Double Outlet Staggered JI

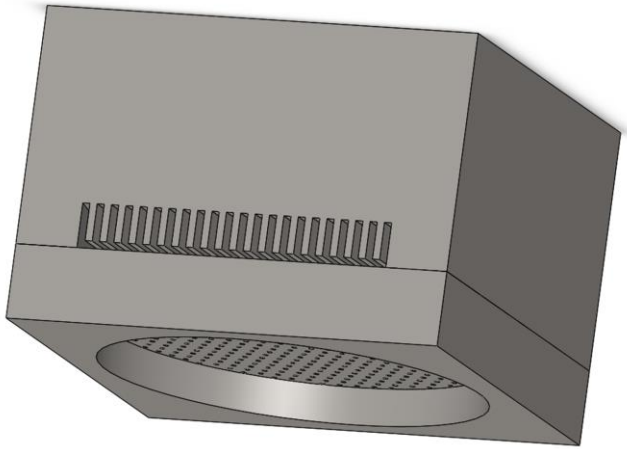
Prototype of Staggered Jet Impingement



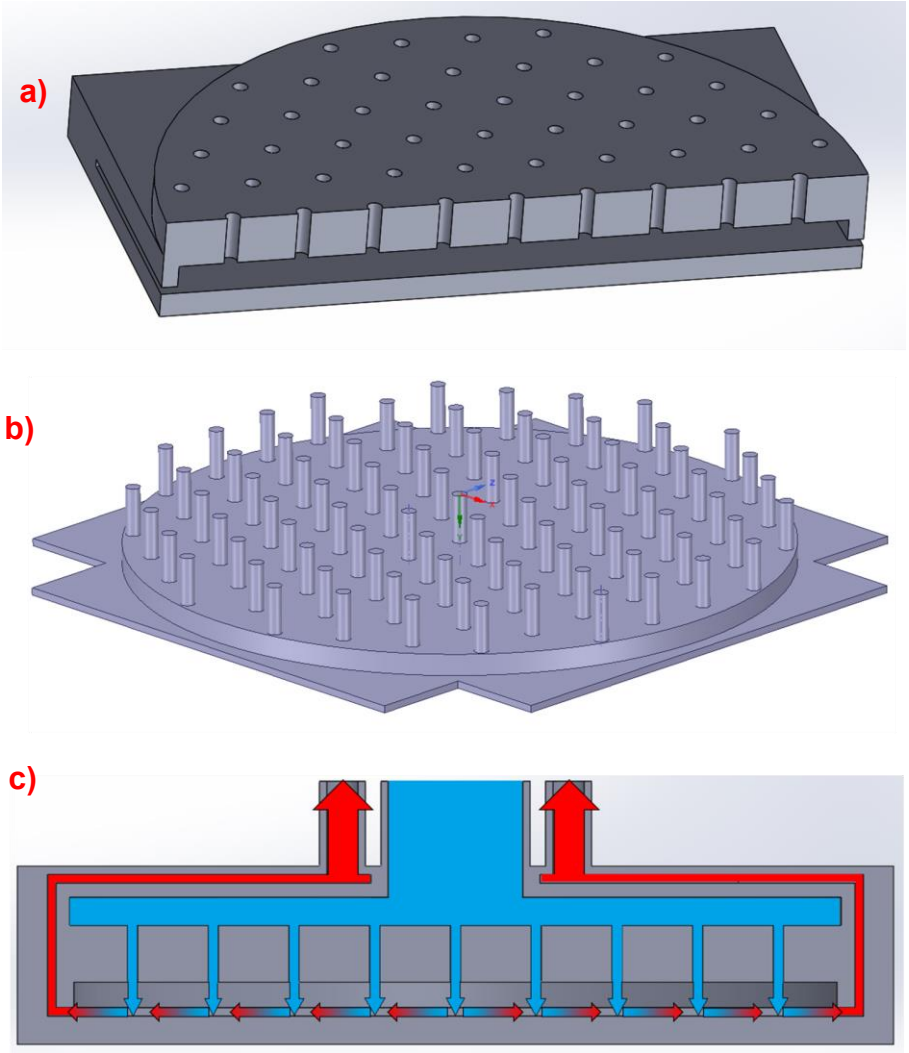
Objective (Clark Left, Sisk Right)



Initial Concept Model Cross-Sectional View



Preliminary design of jet impinging microchannel device



Optimal IC-TMS design: a. Cross sectional isometric view; b. Fluid volume view; and c. Cross section of fluid flow.

Technical Background and Approach (Berg)



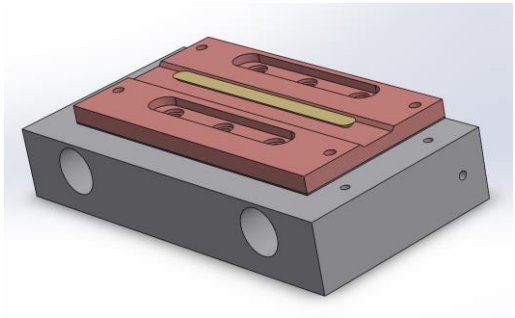
Thermal Management System Interface

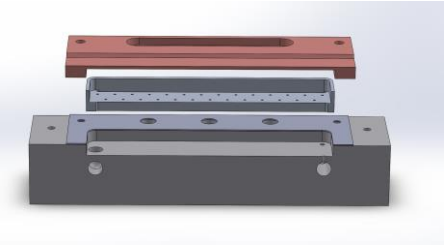
Length	Width	Height
70 mm	5 mm	1.6 mm

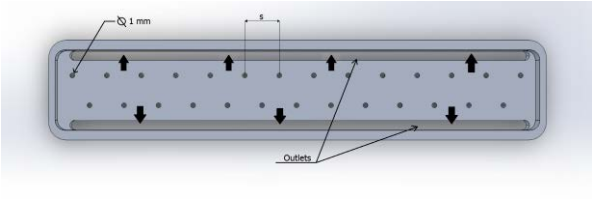
Additional constraint:
Extract heat through semiconductor base!

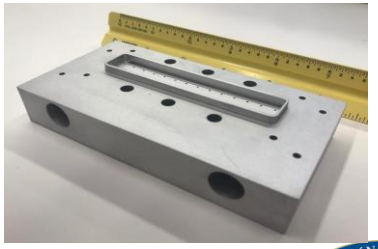
Jet Impingement Thermal Management System (JI-TMS)

- Array of 27 nozzles;
- Alternating pattern;
- Jet plate acts as manifold before nozzles;
- Flow converges before exiting JI-TMS





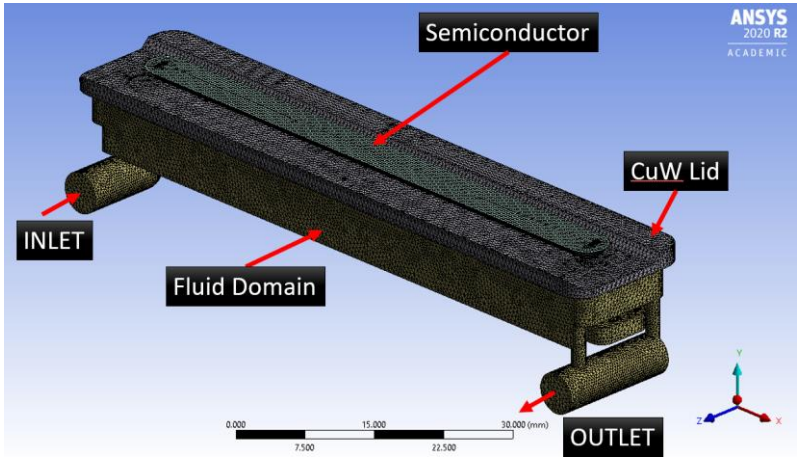




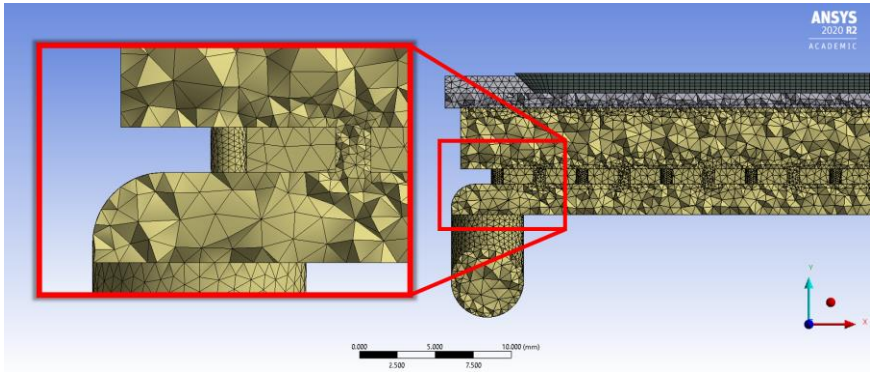
Technical Background and Approach (Berg)

Geometry and Mesh

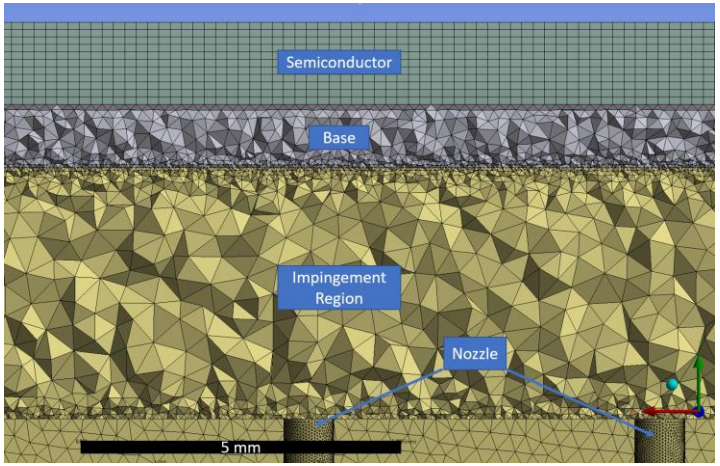
- Tetrahedral mesh elements;
- Maximum skewness < 0.85;
- Orthogonal quality > 0.1;
- Mesh sizes from 187k to 1.639M nodes;
- Fluid dynamics and heat transfer equations solved at each node.



1.639M node mesh



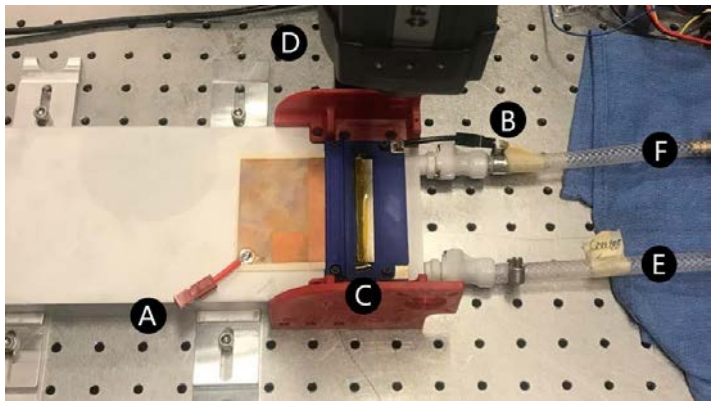
C/S Close up of Inlet and Jet 827k



1.639M node mesh C/S Close up

Experimental Setup

- Heat input was applied and varied with a power supply, though measured with multimeters. The semiconductor acted as a resistive heating element.;
- A pump/chiller was used to circulate and cool the PSf-20cSt and maintain a 10 ℃ coolant temp;
- Temperature captured via FLIR camera;
- Pressure data via spring actuated in-line gauge.



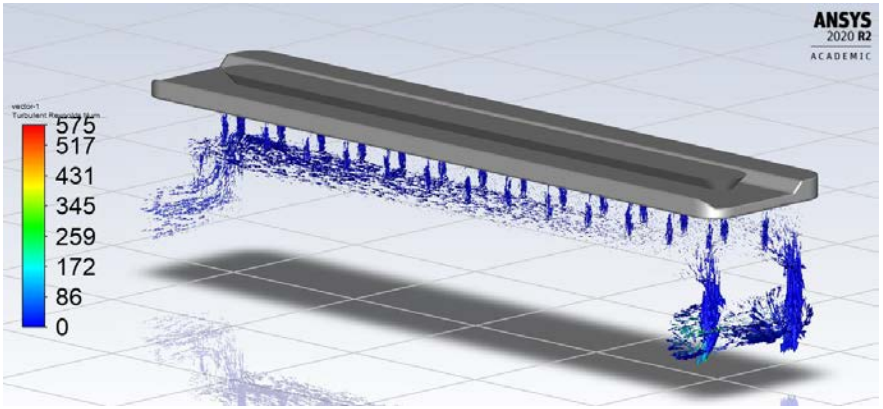
A – Power connection
B – Ground
C – Switch and JI-TMS
D – FLIR A325sc
E – PSF-20cSt Inlet
F – PSF-20cSt Outlet

FLIR A25sc Specs	
Resolution	320 x 240
Accuracy	±2 % of reading
Range	0°C to 350°C

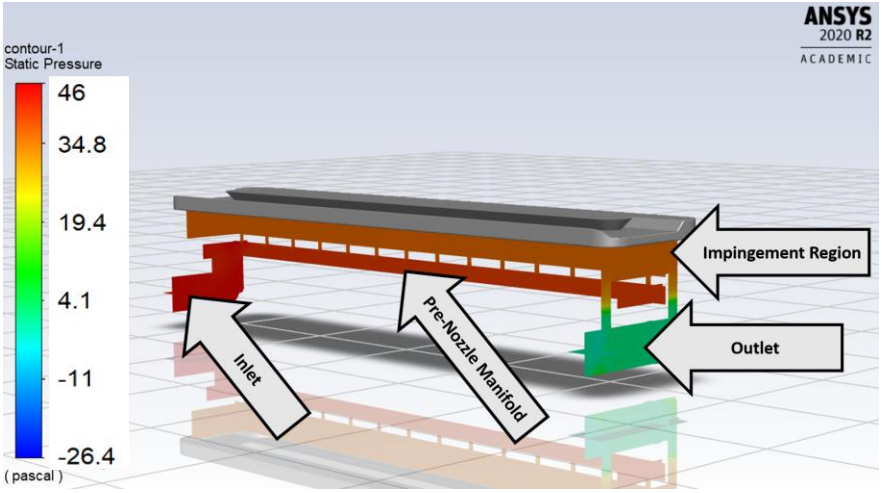
Results (Berg - Simulation)

Property	100 W Test	200 W Test
Max Switch Temperature	54.7 ℃	99 ℃
Pressure Drop	45.9 psi	

- Results given using **1.639M node mesh**
- Reynolds number <u>not indicative of turbulent flow.</u>



Reynolds number



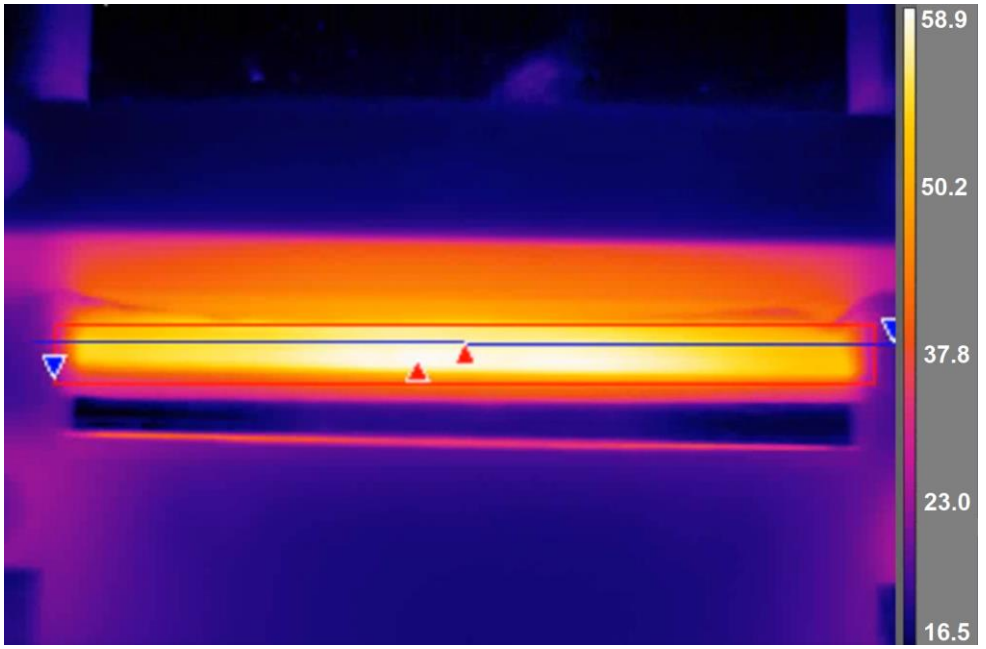
Static Pressure

Results (Berg - Experimental)

Property	100 W Test	200 W Test
Max Switch Temperature	57.8 ℃	98.2 ℃
Pressure Drop	45.4 psi	

- At 45.4 psi pressure drop, a higher flow rate is desired to increase capability of the system. However, it should be within the capability of pumping system.

- With the given geometry, materials, and flow conditions:
  - the JI-TMS is unable to keep the semiconductor below the 80 ℃ threshold at 200 W average power applied to the semiconductor.



FLIR thermal imagery of semiconductor during 100 W Avg. Power Test

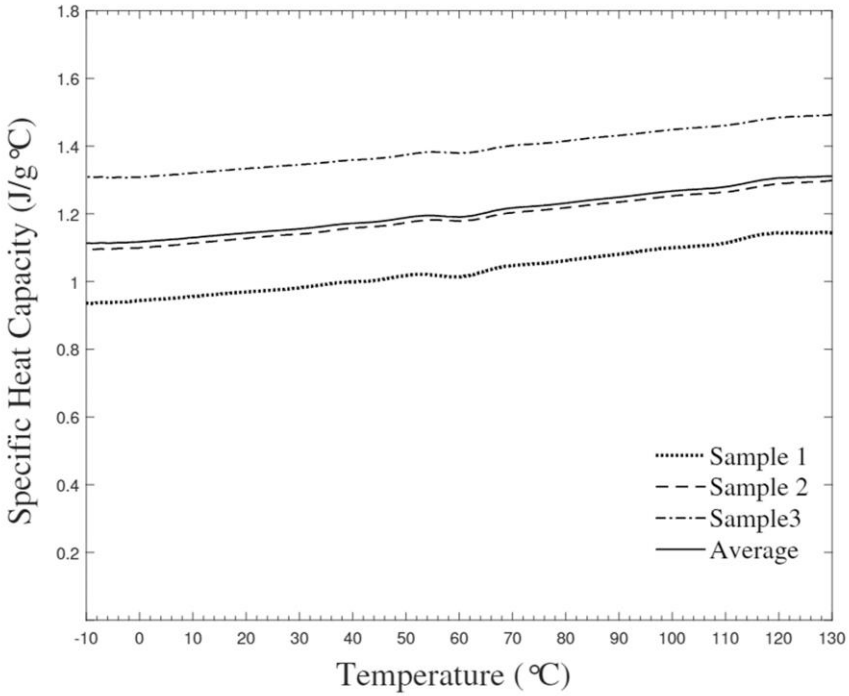
Avg Power Applied	CFD	Experimental	Difference
100 W	54.7 ℃	57.5 ℃	5.89 %
200 W	99.0 ℃	98.2 ℃	0.99 %

Technical Background and Approach (Berg – Heat Transfer Fluid Analysis)

Problem Statement: Given the deviation of the CFD and the experimental results, as well as visual contaminants in the PSF-20cSt, the PSF's thermophysical properties were studied.

- Vendor states that PSF 20-cSt has a **1.6** J/g℃ heat capacity value at 25℃
- Differential Scanning Calorimeter (DSC) testing shows an average Cp value of **1.16** J/g℃ at 25℃.

A difference of 27.5 %



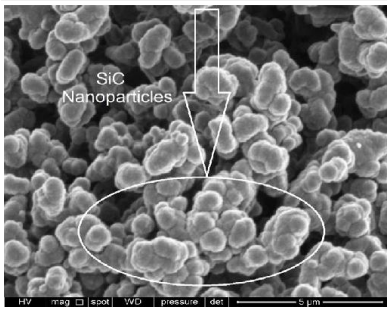
Specific heat capacity of PSF 20-cSt vendor reported value vs actual value

Technical Background and Approach (Berg – Heat Transfer Fluid Analysis)

Goal: To increase Thermal Conductivity of HTF



+



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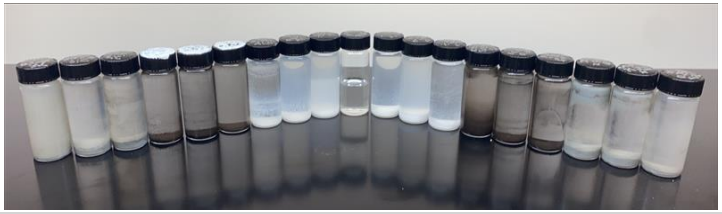


- Pure Silicone Fluid 20cSt
- Nanoparticle with High Thermal Conductivity
- Surfactant to Increase Stability

→ Create a High Conductivity Nanofluid Mixture

✓ To maintain the dielectric properties of the HTF, **only ceramic nanoparticles** were considered.

Nanofluid preparation

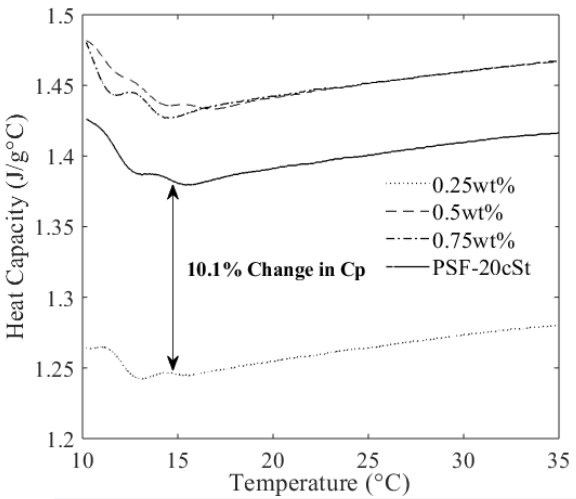


	SiC			Fe2O3			Al2O3		
Sample	1	2	3	1	2	3	1	2	3
Mass % NP	0.25	0.5	0.75	0.25	0.5	0.75	0.25	0.5	0.75
Mass % Surfactant	0.0043	0.0085	0.0128	0.0013	0.0025	0.0038	0.0125	0.0250	0.0375
Mass % Tergitol	0.0997	0.0995	0.0992	0.0997	0.0995	0.0992	0.0997	0.0995	0.0992
Actual % NP w/ surfactants	0.251	0.504	0.757	0.251	0.502	0.756	0.251	0.504	0.757
Actual % NP no surfactants	0.251	0.496	0.753	0.250	0.500	0.750	0.250	0.494	0.747

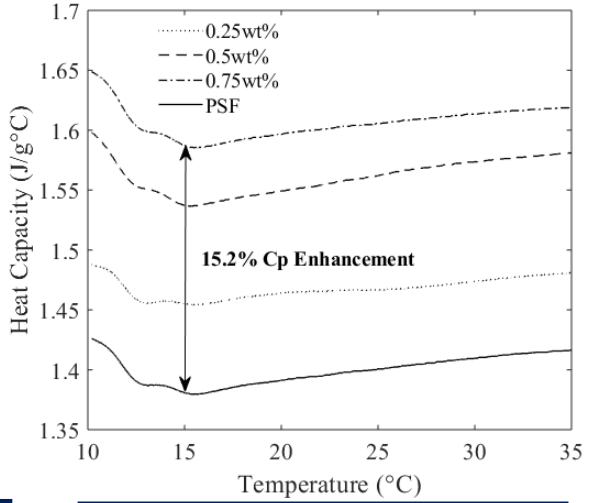
Results (Berg – Heat Transfer Fluid Analysis)

Sample Number	Sample	Specific Heat Capacity (J/gC)
1	Silicon Carbide 0.25 wt %	1.254
2	Silicon Carbide 0.5 wt %	1.441
3	Silicon Carbide 0.75 wt %	1.442
4	Silicon Carbide 0.25 wt %*	1.538
5	Silicon Carbide 0.5 wt %*	1.570
6	Silicon Carbide 0.75 wt %*	1.451
7	Iron Oxide 0.25 wt %	1.464
8	Iron Oxide 0.5 wt %	1.549
9	Iron Oxide 0.75 wt %	1.59
10	Iron Oxide 0.25 wt %*	1.458
11	Iron Oxide 0.5 wt %*	1.462
12	Iron Oxide 0.75 wt %*	1.402
13	Aluminum Oxide 0.25 wt %	1.632
14	Aluminum Oxide 0.5 wt %	1.399
15	Aluminum Oxide 0.75 wt %	1.544
16	Aluminum Oxide 0.25 wt %*	1.376
17	Aluminum Oxide 0.5 wt %*	1.378
18	Aluminum Oxide 0.75 wt %*	1.430
19	PSF-20cSt	1.391

* No surfactant sample



Silicon Carbide with Surfactants Samples



Iron Oxide with Surfactants Samples

Measured thermal Conductivity Results

$$k_{nf} = k_{bf}\frac{k_p + 2k_{bf} + 2\phi(k_p - k_{bf})}{k_p + 2k_{bf} - \phi(k_p - k_{bf})}$$

Using measure Cp, theoretical k value was estimated using modified Maxwell equation.

As Silicon Carbide 0.25 wt% WS had largest drop in Cp, it shows highest k increase.

A 3.5% increase in thermal conductivity!
0.142 W/mK ⟶ 0.147 W/mK

Measured thermal Conductivity Results

Silicon Carbide 0.25 wt %

Iron Oxide 0.25 wt %

- Samples tested to obtain measured nanofluid thermal conductivity value;
- A significantly higher k value was obtained over the theoretical!

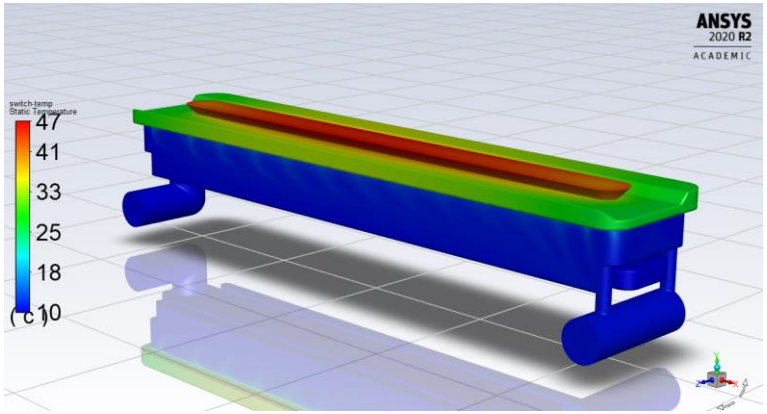
Measured values shows a 32.4% increase in thermal conductivity over vendor value!

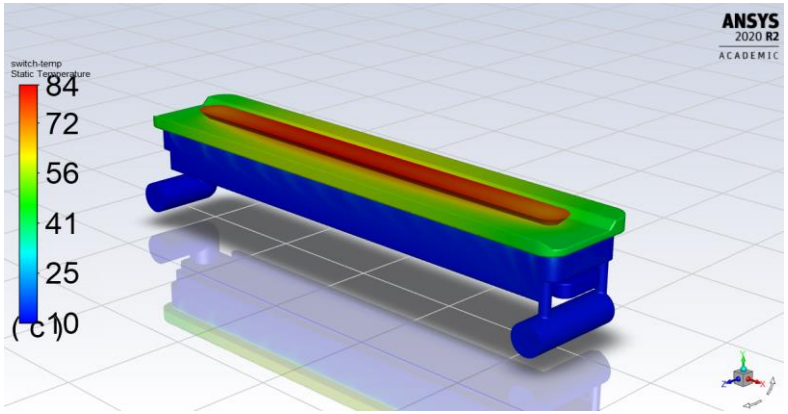
Temperature (°C)	Thermal Conductivity (W/m·K)	Total Thermal Resistance (m^2·K/W)
2.80	0.208	0.0175
11.93	0.197	0.0185
21.80	0.190	0.0191
31.67	0.184	0.0197

Temperature (°C)	Thermal Conductivity (W/m·K)	Total Thermal Resistance (m^2·K/W)
2.23	0.216	0.0169
11.97	0.196	0.0186
21.74	0.189	0.0192
31.62	0.181	0.0201

Results (Berg – Heat Transfer Fluid Analysis)

Performance Evaluation of the System with Implementation of Selected Nanofluids





100 W & 200 Avg. Power with Measured k heat transfer nanofluid

Max Semiconductor Temperature					
Test	**PSF k CFD**	**Theoretical k CFD**	**Measured k CFD**	**Experimental**	**% Improvement compared with PSF**
100 W	54.7	54.36 ℃	46.67 ℃	57.5 ℃	18.8
200 W	99.0	90.18 ℃	83.49 ℃	98.2 ℃	14.9

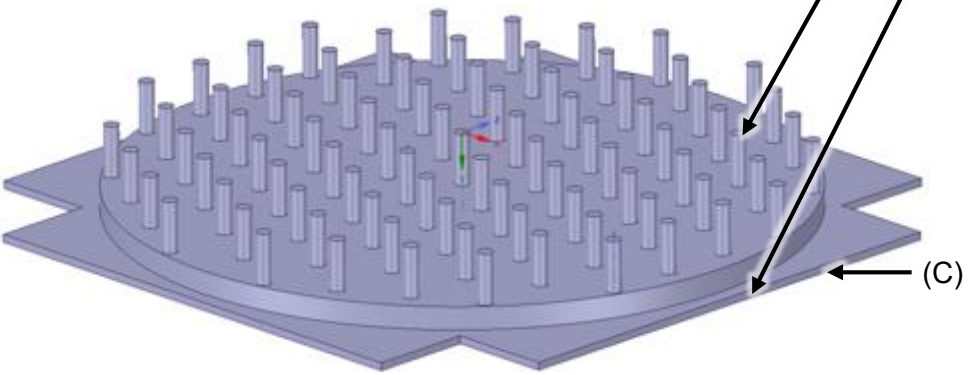
Phase III: UC-TMS (Sisk)
February 2022-September 2022

Primary Problem: The ambitious end goal is to create an ultra-compact cooling unit with the ability to remove 1 kW/cm^2 of heat in a short time frame. To achieve such high heat flux, a turbulent flow profile must be achieved. The objective will be reached as the micron scaled cooling unit is to be integrated onto a semiconductor device, allowing more heat extraction to occur.

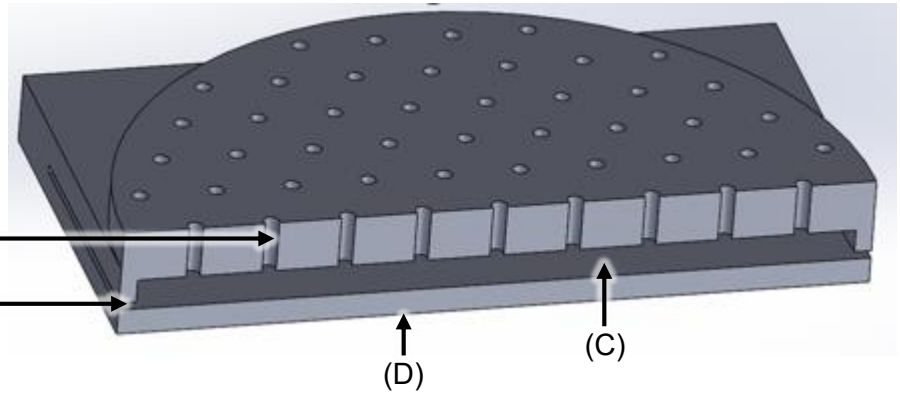
Solution Space: In recent literature, over 1 kW/cm^2 has been achieved with minimal pumping power. The pumping power will be kept to a minimum since the unit to be prototyped will represent 1 cm^2 surface area. This enables less power to be consumed to create a turbulent flow. An array of micro-sized jet nozzles will provide a turbulent flow onto a microchannel section directly on the semiconductor device. The ultra-compact TMS (UC-TMS) design will reach turbulency at a faster rate while requiring less energy consumption.

Ultra Compact Thermal Management System (UC-TMS)

- Array of over 80 nozzles;
- Triangular array pattern;
- 4 Outlet Ports;



Cross Sectional View of Fluid Domain Geometry



Cross Sectional View of Solid Geometry

A), Nozzles	C),Heated Surface
B),Outlet Port	D), Semiconductor Attachment Point

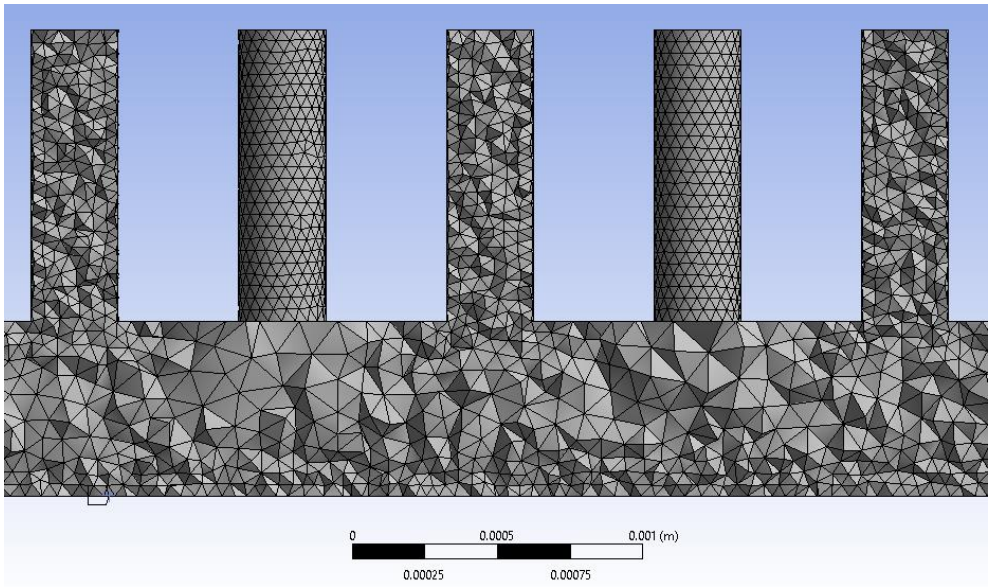
Technical Background and Approach (Sisk)

Meshing Set Up

- Tetrahedron mesh elements;
- Maximum skewness < 0.9;
- Orthogonal quality > 0.1;
- Mesh sizes from 2.5M Elements and 500k nodes;
- Fluid dynamics and heat transfer equations solved at each node.

Simulation Set-Up

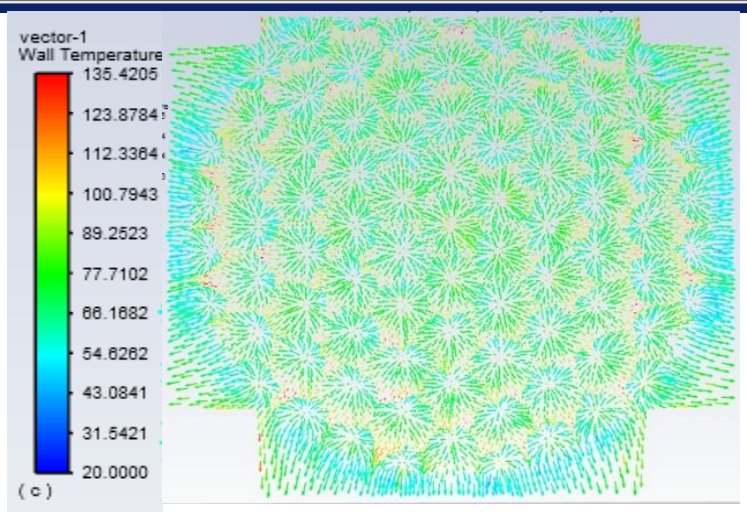
- Standard k-epsilon physics model for focus on turbulency
- Heat Flux of 1 $\frac{kW}{cm^2}$ on Heated Plate
- Over 80 nozzles diameter of .3 mm
- Fluid outlet cross sectional area is equivalent to the sum of nozzles surface area
- Incoming fluid is set to 40 m/s at a flow rate of 3.1 GPM

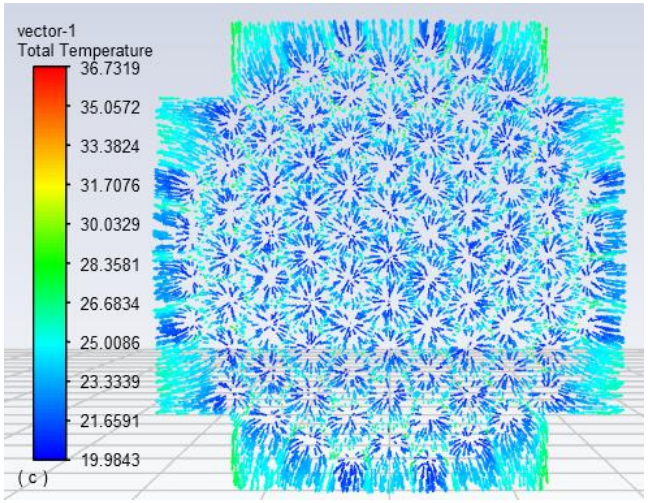


Cross sectional view of meshing in fluid domain

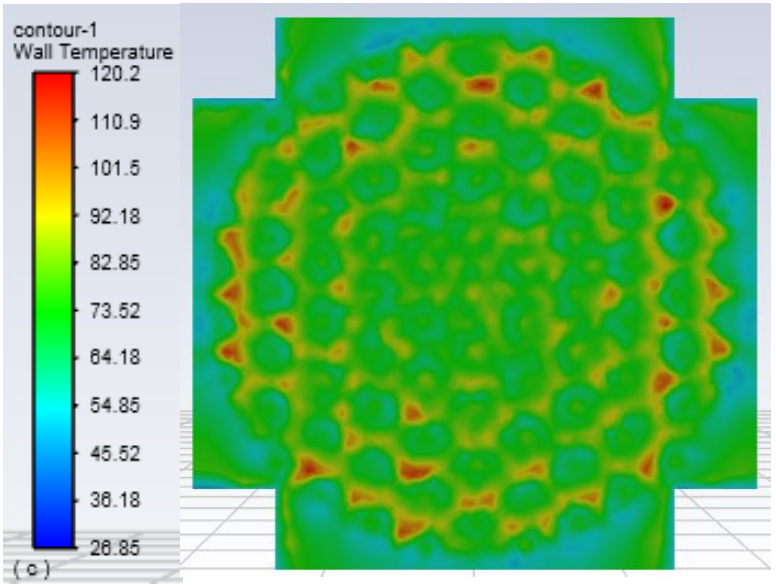
Results (Samual Sisk - Simulation)

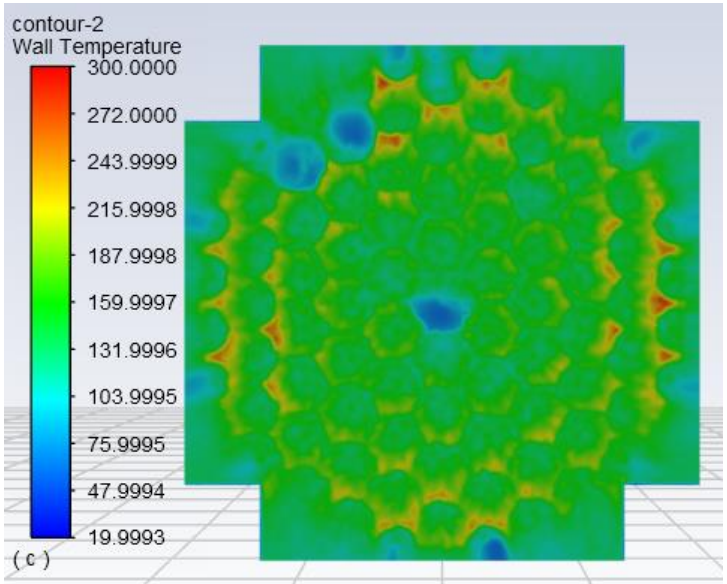
A.





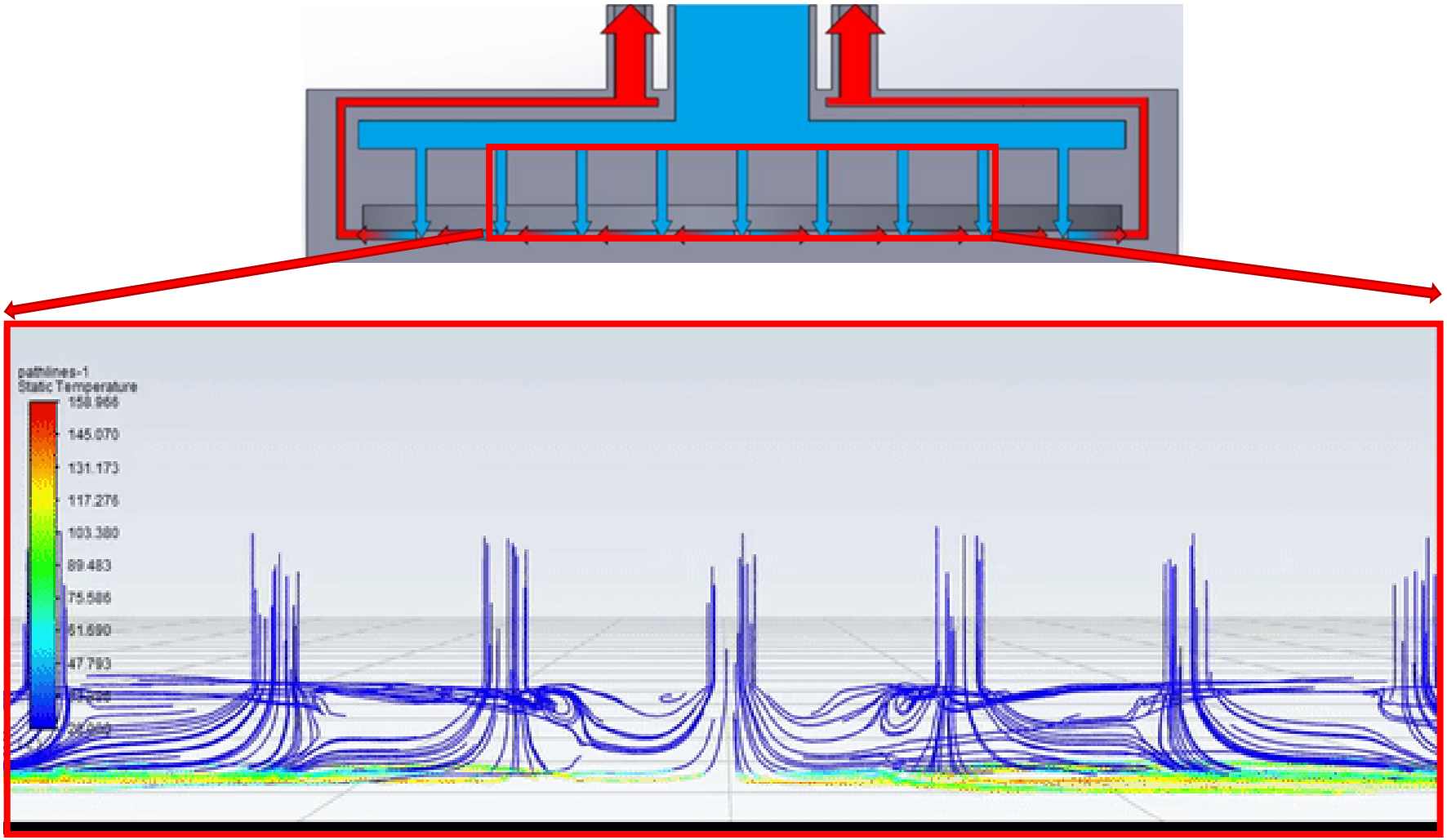
Top view of JI contact displaying contour plot of velocity vector colored by temperature. (A) Fluid is Water (B Fluid is pure Si Fluid





Top view of JI contact displaying contour plot of temperature. (A) Fluid is Water (B) Fluid is pure Si Fluid

Results (Sisk - Simulation)



Visualization of fluid flow from jet inlet and target surface
(cross sectional view)

Results (Sisk - Simulation)

- **Summary of achievements in Phase-III:**

- A water-cooled, cross-flow microchannel cooling system with various microchannel widths etched into GaN and Al/GaN monolithically. An experimentally achieved heat flux of 1.7 kW/cm^2 using 0.056 W of pumping power. Although the cross-flow design is not the best fit under manufacturing constraints, the theory of using channels is remarkable and further analyzed.

- A water-cooled hybrid of microchannels with impinging jets. This design implemented the idea of having jets confined in their own individual spaces reaching up to 900 W/cm^2 with 0.83 W of pumping power.

- A hybrid consisting of multiple jet arrays with microchannel draining ways produced up to 1200 W/cm2 using 1.52 W of pumping power.

Outputs

- **Students Graduated:**
  - Jordan Berg, MS, Spring 2021 (now at MRI Global)
- **Theses and Dissertations:**
  - Jordan N. Berg, "Development of a Jet Impingement Thermal Management System for a Semiconductor Device with the Implementation of Dielectric Nanofluids," MS Thesis in Mechanical Engineering, University of Missouri-Kansas City, **2021** [mospace].
- **Students Contributions:**
  - Sam Sisk (Spring 2022-Present)
  - Justin Clark (Spring 2021-Fall 2021)
- **Journal Publications:**
  - J. N. Berg, R. C. Allen, and S. Sobhansarbandi, "A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation," *International Journal of Thermal Sciences*, 172, 107254, **Feb 2022** [doi].
- **Full-length Peer-Reviewed Conference Articles:**
  - J. Berg, and S. Sobhansarbandi. "CFD Modeling of Thermal Management Systems for a Silicon Semiconductor Switch." *ASME 2020 Heat Transfer Summer Conference collocated with the ASME 2020 Fluids Engineering Division Summer Meeting and the ASME 2020 18th International Conference on Nanochannels, Microchannels, and Minichannels*, Virtual, July 13–15, 2020, American Society of Mechanical Engineers Digital Collection [doi].

Outputs

- **UMKC SUROP symposium, September 2022:**
  - S. Sisk, and S. Sobhansarbandi, “In-Chip Cooling Technology within Semiconductor Switches”, (Poster Presentation).
- **Directed Energy Professional Society, Directed Energy Systems Symposium, Washington DC, October 25-29 2021:**
  - J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation” (Poster).
  - J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures” (Poster).
  - J. Clark, R. C. Allen, and S. Sobhansarbandi, “Ultra-Compact Integrated Cooling System Development” (Poster).
- **UMKC SUROP symposium, September 2021:**
  - J. Clark, and S. Sobhansarbandi, “Ultra-Compact Integrated Product Cooling Technology, (Poster Presentation).
- **UMKC OSPRES Grant Biannual Review, May 2021:**
  - J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “A Novel Method of Cooling a Semiconductor Device through a Jet Impingement Thermal Management System: CFD Modeling and Experimental Evaluation” (Poster Presentation).
  - J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “Heat Transfer Enhancement of a Jet Impingement Thermal Management System: A Comparison of Various Nanofluid Mixtures” (Poster Presentation).
- **DEPS Posters and Presentations, Virtual, December 9, 2020:**
  - J. N. Berg, R. C. Allen, and S. Sobhansarbandi, “Heat Transfer Potential and Pragmatism from Jet Impingement” (Presentation).
- **UMKC OSPRES Grant Biannual Review, September 2019:**
  - J. N. Berg, and S. Sobhansarbandi, “Thermal Design and Development of Cooling System for SiPCSS” (Poster Presentation).

Summary

- The CFD results for the JI-TMS show that device temperature is well maintained below the desired operating temperature at 100 W with great margin, but exceeds the target temperature during the 200 W simulation;
- Validation of the design is performed with the same boundary conditions experimentally to ensure the accuracy of the CFD results; showing an average error of 5.89% with the numerical data;
- To further increase the performance of the system, nanofluid samples were created using various nanoparticles and surfactants; a 0.25 wt% mixture of silicon carbide with surfactants was found to have the most significant heat capacity reduction with the greatest thermal conductivity increase of all the sample;
- Using the new thermophysical property values, CFD models were run. The nanofluids showed a 12.6% and 13.3% maximum temperature reduction for the 100 W and 200 W average power simulation, respectively.
- A water-cooled, cross-flow microchannel cooling system with various microchannel widths etched into GaN and Al/GaN monolithically. An experimentally achieved heat flux of 1.7 kW/cm^2 using 0.056 W of pumping power. Although the cross-flow design is not the best fit under manufacturing constraints, the theory of using channels is remarkable and further analyzed.

Recommendations & Future Work

- **Reduce the size of the JI-TMS by a factor of 10**
  - Integrate into semiconductor (thermal resistance reduction)
  - Reduction in flow rate (L to mL)
  - Literature suggests a 10-fold increase in heat extraction ability
  - No known research on chip-integrated JI
- **Implement nanofluids in new geometry**
  - Increase HTF thermal conductivity without compromising the dielectric property
- **Exceed the 1 kW heat extraction ability**

Contact

Thank You for your attention!

For any possible questions that you may have, please contact:

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