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NOVEL DEEPLY SCALED FIN HETEROJUNCTION BIPOLAR TRANSISTORS (FinHBTs) FOR THz MIXED SIGNAL APPLICATIONS

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Final Report

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14. ABSTRACT

A novel lateral SiGe FinHBT has been proposed. Utilizing the advanced lithography technology of ultra-scaled VLSI, the lateral scaling of base width can greatly enhance the RF performance of FinHBT. A FinFET compatible fabrication process has been designed and developed. With a 100nm base width and 15% peak Ge composition, the maximum measured DC gain is 6.5. The simulation predicts that the fT/fMAX > 750GHz can be achieved with base width scaling.

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1 SUMMARY

FinFET has become the mainstream technology on the VLSI platform for logic applications since the 22nm node. With layout and parasitic resistance/capacitance optimization, the f_T/f_{MAX} of 300GHz/450GHz has been demonstrated on Intel 22nm Si FinFET [1]. However, it is still insufficient for terahertz sensing and high bandwidth communications. Though capable of THz operations [2]-[4], III-V-based devices are limited by the integration level. A device solution that encompasses both the density and the THz capability will lead to a major leap in SoCs by enabling the reduction of form factor, the decrease in power consumption, the reduction of interconnect latency, and the improvement in high-frequency performance. In the past, BiCMOS technology has been the go-to solution for RF/mixed-mode applications. Vertical SiGe HBT on 130nm node has demonstrated f_T/f_{MAX} up to 505GHz/720GHz [5], which shows potential for THz operations. However, implementing the conventional vertical HBTs on the FinFET platform is extremely challenging.

To solve this issue, a novel lateral SiGe FinHBT has been proposed. Utilizing the advanced lithography technology of ultra-scaled VLSI, the lateral scaling of base width can greatly enhance the RF performance of FinHBT. A FinFET compatible fabrication process has been designed and developed. The lateral base region is created by SiGe SEG. A T-shape extrinsic base structure is used to reduce the base resistance. A test device has been successfully fabricated and characterized. With a 100nm base width and 15% peak Ge composition, the maximum measured DC gain is 6.5. The simulation predicts that the $f_T/f_{MAX} > 750$GHz can be achieved with base width scaling.

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2 INTRODUCTION

2.1 2.1 T-base FinHBT Design

The 3D structure of a Lateral SiGe T-base FinHBT is shown in Figure 1. A cross-section schematic is illustrated in Figure 2. The device architecture resembles a FinFET, but with a wider fin because the narrow fin is not needed to suppress short channel effects. The "source" and "drain" of the FinFET are replaced by a highly doped emitter and collector region of the HBT. The "channel" region is replaced by a lateral-graded SiGe base region. Instead of the high-k metal gate stack in FinFET, a highly doped T-shaped extrinsic p+ base (T-base) is formed on the top of the intrinsic SiGe base. By using the T-base, the base contact area can be significantly increased. Since the T-base can have a higher in-situ doping concentration than the intrinsic base, the contact resistivity can also be improved. This can greatly reduce R_{base} and improve the f_{MAX} of the device. The devices are fabricated on SOI wafers with a 25nm-thick BOX, which is used to eliminate the emitter-base leakage path through the substrate.

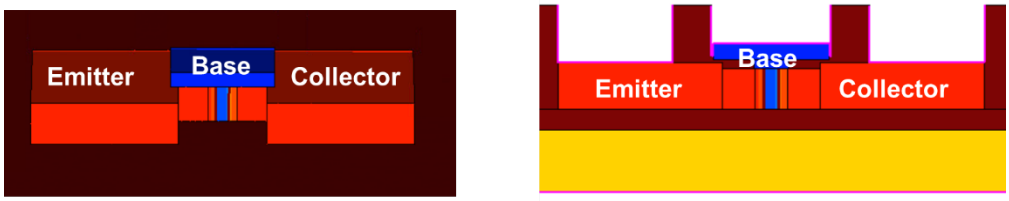

Figure 1. 3D Structure of Lateral SiGe T-base FinHBT

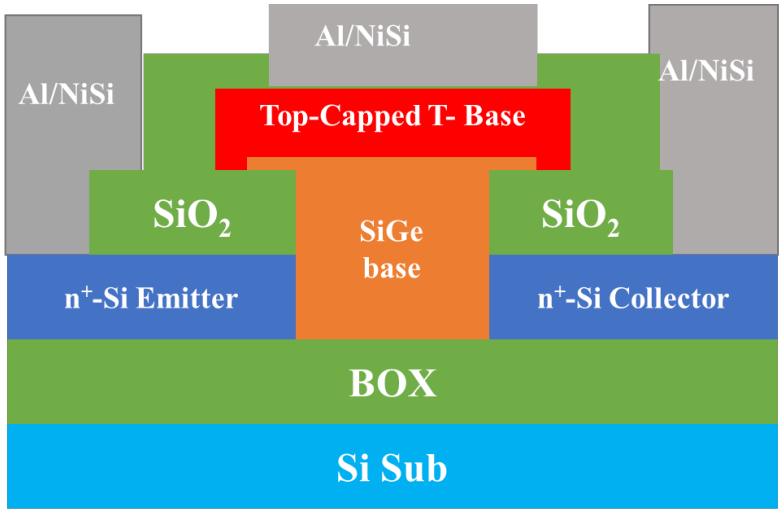

Figure 2. Cross-Section Schematics of a T-base FinHBT

2.2 T-base FinHBT Process Flow

The key steps of the T-base FinHBT fabrication process are illustrated in Figure 3. The width of the SiGe base region is defined by the trench created by e-beam lithography and dry etching. SiGe with lateral grading is then selectively grown inside the trenches. A highly doped extrinsic base is grown on top of the intrinsic SiGe base. By using a longer epitaxy growth time, the extrinsic base extends outside the trench, forming a T-shaped extrinsic base structure. After that, an e-beam

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lithography step followed by a dry etch is used to define the desired width of the T-base. With the T-base, the base contact area is no longer limited by the base width. At the same time, the in-situ doped extrinsic base can reach a doping concentration > $1x10^{20}$ cm^{-3}, further reducing the base resistance.

After the epitaxial growth, dry etch is used to etch the fin structure. A test structure is used to ensure good isolation is achieved before proceeding to the next step. ALD is then used to passivate the exposed Si surface during the fin etch. Contact openings are created with dry etch. The area emitter and collector openings are 1μm x 1μm. The base is contacted right on top of the T-base region for the reduction of base resistance. The width of the base contact opening is 300nm. This is followed by the NiSi formation to reduce the contact resistance. For metallization, the 100nm Al metal wires and landing pads are deposited using single-layer PMMA lift-off. Figure 4 summarizes the flow chart for the complete SiGe FinHBT process flow. The comparison between FinHBT and the standard FinFET process is shown in Table 1. Extra steps include base patterning, base SEG, and extrinsic base growth.

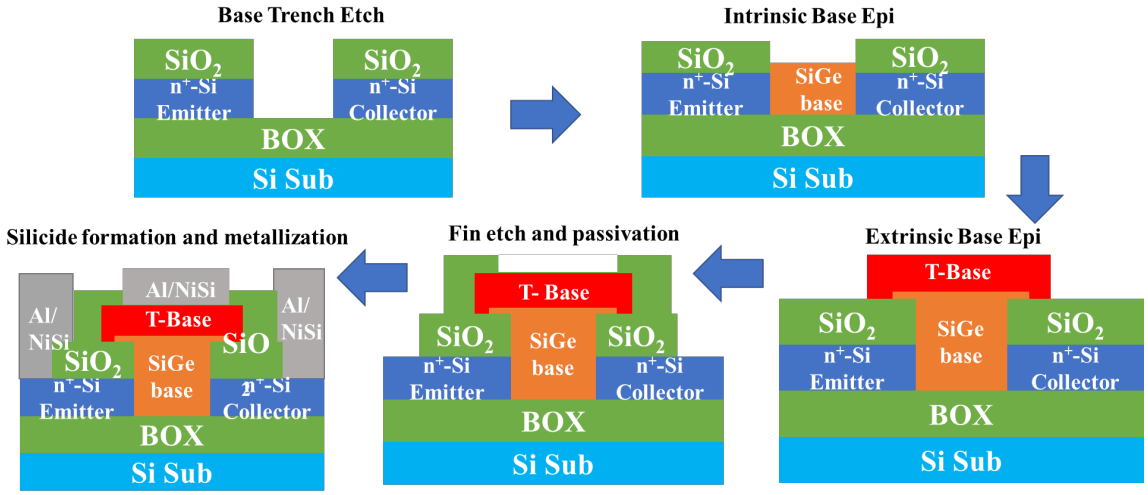

Figure 3. Key Process Steps of T-base FinHBT

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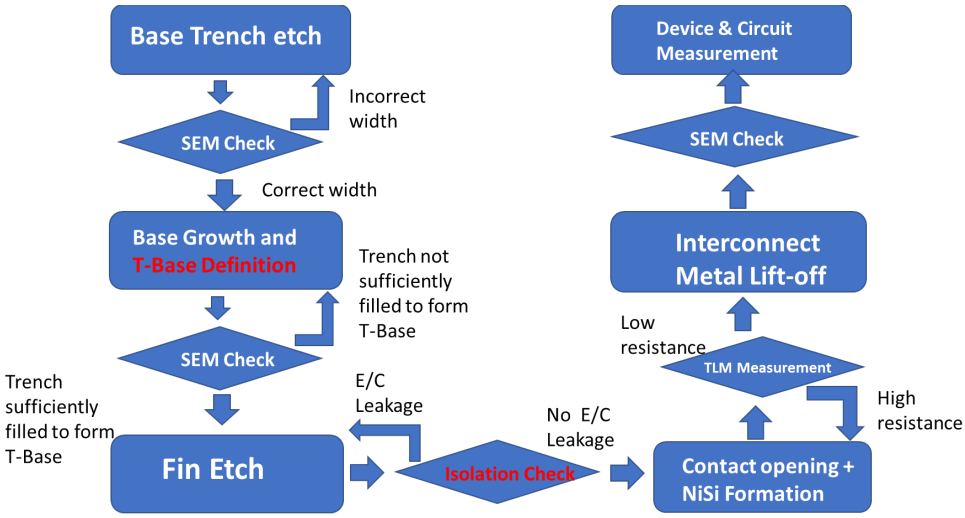

Figure 4. Flow Chart of T-base FinHBT Process

Table 1. FinHBT vs. FinFET Process

SOI FinFET	FinHBT
SOI Substrate	SOI Substrate
	E/C doping → Base Epi → Extrinsic base Epi
Fin pattering	Fin patterning
Dummy gate	Dummy gate
Spacer	Spacer
SD regrowth	EC regrowth
Remove dummy	Remove dummy
HKMG	
Contact	Contact

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3 METHODS, ASSUMPTIONS, AND PROCEDURES

In order to fabricate SiGe FinHBT on SOI substrate, key process modules have been developed. The selective epitaxy growth (SEG) technique is used to create the SiGe base region on a Si SOI substrate. E-beam lithography (EBL) and dry etch are then used to pattern the fin architecture, which is aligned to the base region with sub-10nm accuracy. The contact module includes creating the contact opening using EBL, forming NiSi in the contact openings, and metal deposition. The implementation and integration of the modules on silicon SOI substrate were done at UCLA Nanofabrication Laboratory (Nanolab) and Stanford Nanofabrication Facility (SNF).

3.1 Selective Growth of SiGe in Trench

SiGe epitaxy growth is done using the Applied Materials Centurion Epitaxial System at Stanford SNF. It is a reduced-pressure chemical vapor deposition (RPCVD) system in which dichlorosilane (DCS) and germane were used as source gas in a reduced-pressure environment [6]. In order to find the optimal growth condition, SiGe blanket growth was done on bare silicon wafers. The growth rate and Ge composition versus the mass flow ratio between DCS and germane at 650°C and 700°C are shown in Figure 5(a). The AFM imaging (Figure 5(b)) indicates that a conformal SiGe layer can be obtained after the blanket growth. By introducing doping precursors in the growth process, in-situ doped SiGe can be formed. For growing the base of an NPN transistor, 1% B_2H_6 is used as the precursor. The doping concentration between $1x10^{19}$ and $1x10^{20}$ cm^{-3} can be reached by controlling the B_2H_6 mass flow.

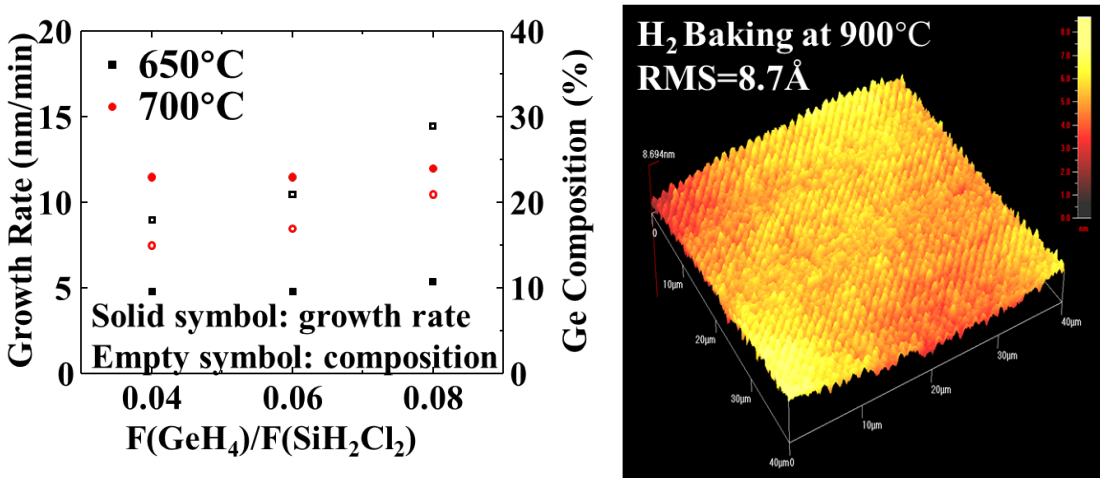

Figure 5. (a) SiGe Blanket Growth Rate and Ge Composition vs. Germane/DCS Mass Flow Rate (b) AFM Imaging of SiGe Grown at 650°C

Selecting an appropriate Ge composition for the SiGe growth is crucial for building a functional FinHBT. According to [7], the SiGe layer grown on Si substrate can suffer from significant interface dislocation due to strain relaxation. This effect can happen with high growth temperature, low pressure, and high Ge composition. A large amount of dislocation at the Si/SiGe interface can cause significant leakage in the n+-p+ heterojunction, and thus lead to the failure of the FinHBT device. Also, strain relaxation can also happen if the layer thickness is larger than the critical value, as described in [8]. To examine this, n+-p+ Si/SiGe heterojunction diodes are made as a test

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structure. The structure of the heterojunction diodes is shown in Figure 6. A p+ SiGe layer is grown on an n+ silicon substrate. Dry etch is then used to isolate the junction, creating the mesa for the diode. Metal is then deposited by lift-off to create the contact for measurement. The growth conditions and the diode measurement data are shown in
Table 2, Figure 7, and Figure 8.

For germane flow of 1 sccm and 2 sccm, diode characteristics can be observed (Figure 7 and Figure 8). The extracted diode V_{th} is 0.64 and 0.67 V, respectively, which is in agreement with the band structure of Si/SiGe heterojunction diodes. For germane flow of 3 sccm and 4 sccm, the measurement shows a large leakage current for both forward and reverse bias. Therefore, the V_{th} cannot be extracted. This is possibly due to a large amount of dislocation at the Si/SiGe interface caused by the strain relaxation. For higher Ge compositions, the lattice mismatch between Si and SiGe is higher, and it is more likely that dislocation will be formed due to the strain relaxation. Therefore, 15% germanium composition will be used in the test device. The process temperature/pressure will be further optimized to increase the base germanium composition and improve the performance of the device.

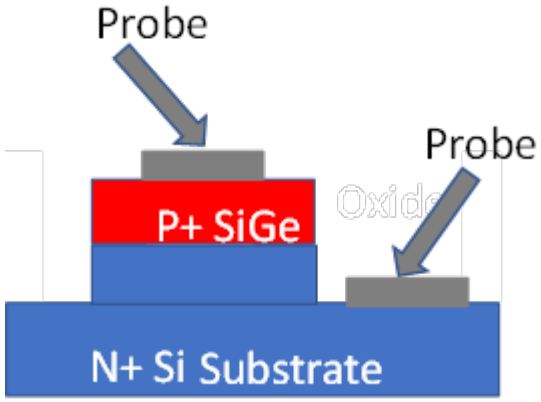

Figure 6. N+-P+ Si/SiGe Diode Test Structure

Table 2. SiGe Growth Conditions

DCS flow (sccm)	Germane flow (sccm)	Ge %	Diode Vth
75	1	12	0.67
75	2	15	0.64
75	3	24	X
75	4	29	X

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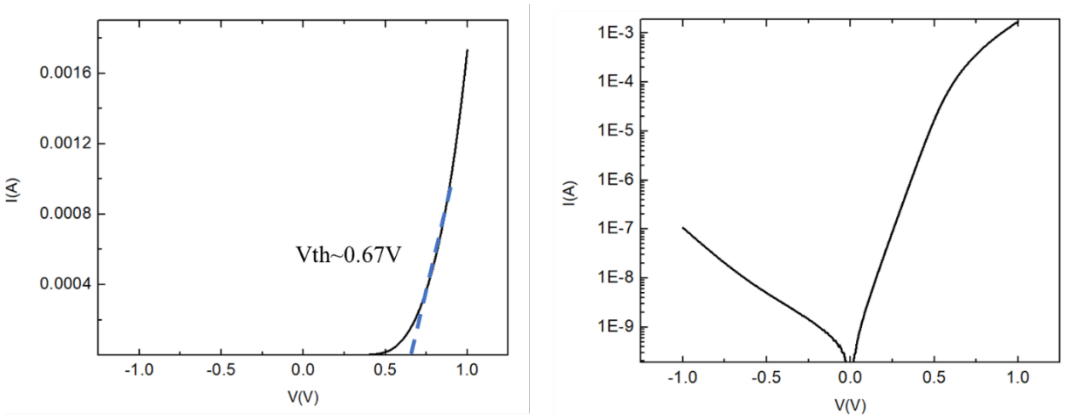

Figure 7. Diode I-V. Ge Composition of p+ SiGe is 12%.

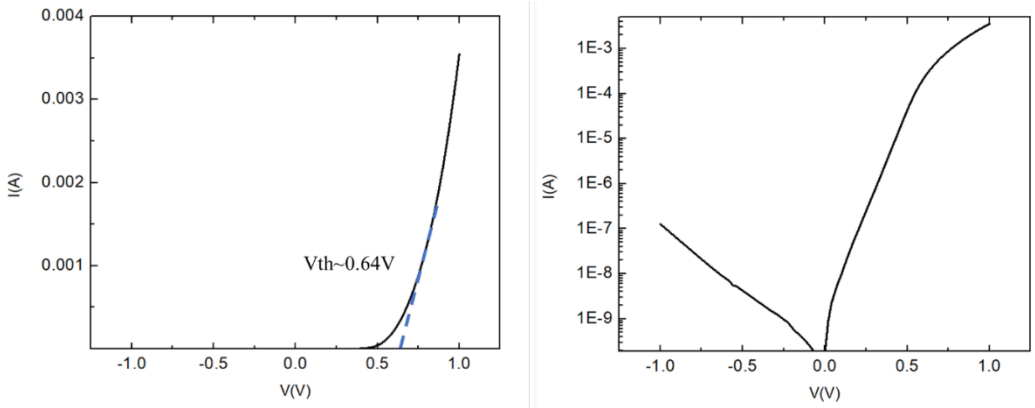

Figure 8. Diode I-V. Ge composition of p+ SiGe is 17%.

To form the highly scaled SiGe base region, SiGe SEG is done in small trenches. An SiO_2 layer is deposited on the silicon device layer using PECVD. Trenches are then created using e-beam lithography (EBL). A JEOL JBX-6300FS e-beam writer is used to pattern the narrow trenches that will be used to define the base region. With EBL, the width of the trenches can be defined down to 20nm Figure 9. Dry etch is used for pattern transfer. All the 50nm of silicon device layer in the trench is etched. The BOX serves as an etch-stop layer.

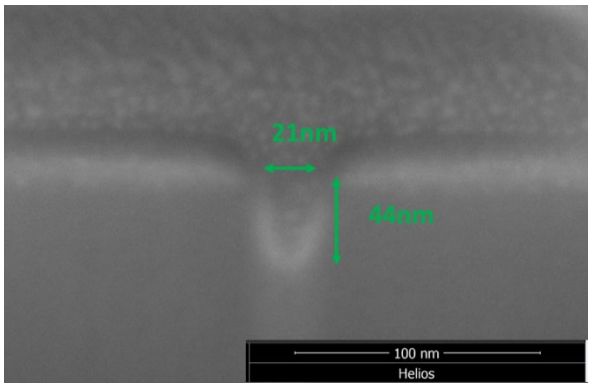

Figure 9. 20nm Trench Defined by E-Beam Lithography

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After patterning the base trench, the SiGe growth process is performed. Since all of the silicon in the trench is etched, there will be no seeding layer at the bottom of the trench. Therefore, SiGe will only grow from the sidewalls, enabling better control of the desired Ge composition profile. The growth of the intrinsic SiGe base region is followed by a p+ T-base growth. The T-base is then patterned by EBL to achieve the desired T-base width. As shown in Figure 10, a T-base with a width of 300nm is formed on the top of a 50nm intrinsic base. The cross-section of a 100nm trench and T-base after epi and is shown in Figure 11. The SEM shows a boundary in the middle of the base. This indicates the potential grain boundary or void in the base.

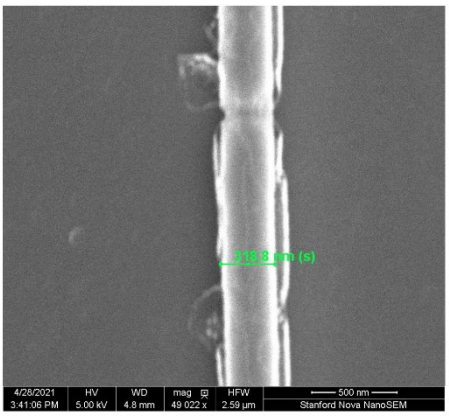

Figure 10. SEM of a 300nm T-base

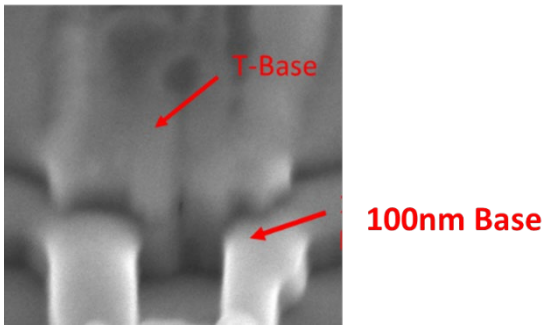

Figure 11. Cross-Section of 100nm SiGe Base and T-base

3.2 Fin Patterning and Contact Opening

Fin structure was created using EBL and chlorine etch. The layout is shown in Figure 12(a) and the cross-section of the fin after the etch is shown in Figure 12(b). An average fin width of 55nm is achieved, with a 77° taper angle.

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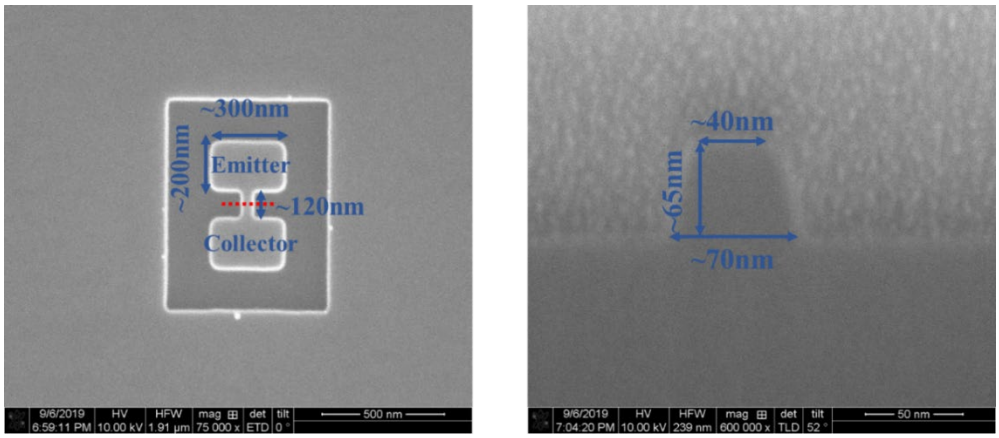

Figure 12. (a) Top view of the Fin Pattern and (b) Cross-Section SEM of the Fin

To create the desired device structure, the fin structure needs to be aligned to the SiGe base region. Two-step alignment (with global alignment and chip alignment) was used to make sure the alignment error was minimized. The alignment marks were cross-shaped, 1μm deep trenches in order to cause good enough contrast in the back-scatter detector of the EBL system. This experiment was done in Stanford SNF using key tools in Table 3. The error of the alignment is less than 10nm, which is good enough to achieve desired device structure.

Contact openings are created using EBL and RIE oxide etcher. The base is contacted right on top of the T-base region for the reduction of base resistance. With two-step alignment, minimal alignment error can be reached. To reduce the contact resistance, an enlarged emitter and collector are used for the test device. This allows for larger contact openings at the emitter and collector. The extrinsic emitter and collector size is 1μm x 1μm. This can potentially reduce the contact resistance at the emitter/collector to 20Ω, which is less than 10% of the total series resistance of a 20nm-base FinHBT.

Table 3. Key Equipment Used in Process Development

Process	**Equipment**
SiGe SEG	Applied Materials Centurion Epitaxial System
EBL	JEOL JBX-6300FS
Oxide dry etch	Applied Materials Precision 5000 Etcher
Silicon dry etch	Lam Research TCP 9400 Poly Etcher

3.3 NiSi Formation at Emitter/Collector(n-Si) and Base(p-SiGe)

Due to the small size of the FinHBT, it is crucial to have small contact resistivity for high f_T and f_{MAX}. Therefore, the self-aligned nickel silicide process is chosen to reduce the contact resistivity. The NiSi process on SOI wafer reported in [9] has been reviewed. In [9], 11nm to 41nm Ni is deposited on a 100nm SOI substrate for NiSi formation. The RTA temperature varies from 450°C to 700°C. It was reported that contact resistivity depends heavily on the depth of silicidation. When forming NiSi, Ni and Si consume at a rate of 1:1.84. The contact resistivity is the lowest ($1x10^{-7}$ $\Omega \cdot cm^2$) when 60% of Si is consumed. Based on this understanding, different silicide thicknesses are tested. Also, RTA temperatures of 400°C to 700°C are tested.

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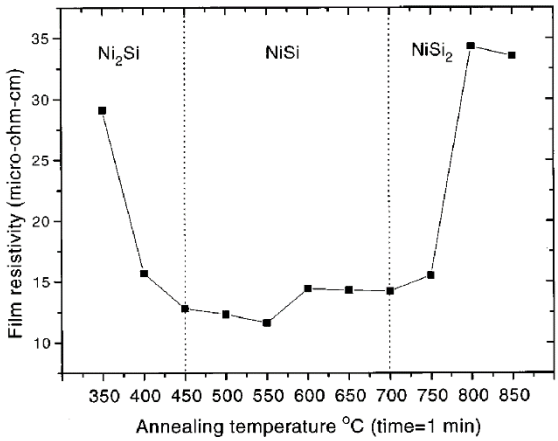

Figure 13. NiSi Film Resistivity vs. RTA Temperature

In our experiments, Ni thickness from 6nm to 20nm on 50nm Si (n-type 9x1019 cm-3) were deposited on SOI samples, as shown in Table 4. Different RTA temperature of 450°C to 700°C and different Ni evaporation base pressure (1x 10-6 torr and 1.2x 10-7 torr) have also been studied. Figure 14 shows the contact resistivity is the lowest (3.11x10-6 Ω ·cm2) when 60% of Si is consumed (RTA = 600 °C and base pressure = 1x 10-6 torr), which is similar to the result in [9].

Table 4. Ni Thickness and Si Consumption in NiSi Formation on 50nm SOI Samples

Ni (nm)	6	10	16	20
Si (nm) consumed	11(22%)	18.4(37%)	30(60%)	37(74%)

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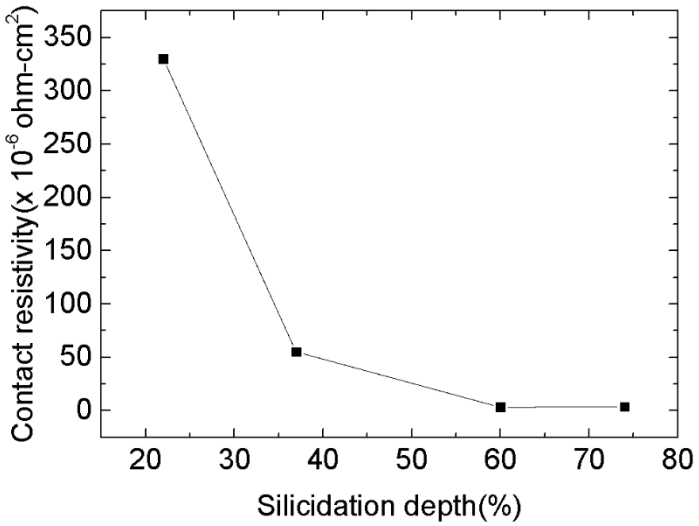

Figure 14. Contact Resistance vs. Silicidation Depth

Different RTA temperatures of 450, 500, 550, 600, 650, and 700°C have also been tested under the same Ni thickness (16nm) and base pressure (1x 10^{-6} torr). Figure 15 shows the lowest contact resistivity 9.11x10^{-7} Ω ·cm^2 is achieved at RTA = 500°C

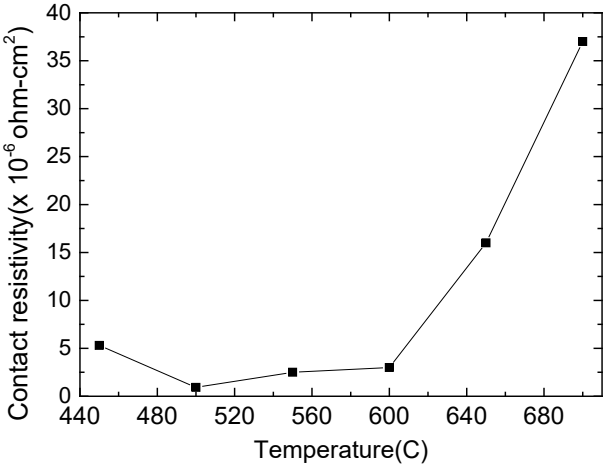

Figure 15. Contact Resistivity vs. RTA Temperature

Different Ni evaporation base pressures (1x 10^{-6} torr and 1.2x 10^{-7} torr) also have been used with the same Ni thickness (16nm) and RTA temperature. The lower evaporation base pressure (1.2x 10^{-7} torr) gives lower contact resistivity 3.1x10^{-7} Ω ·cm^2, as shown in Figure 16.

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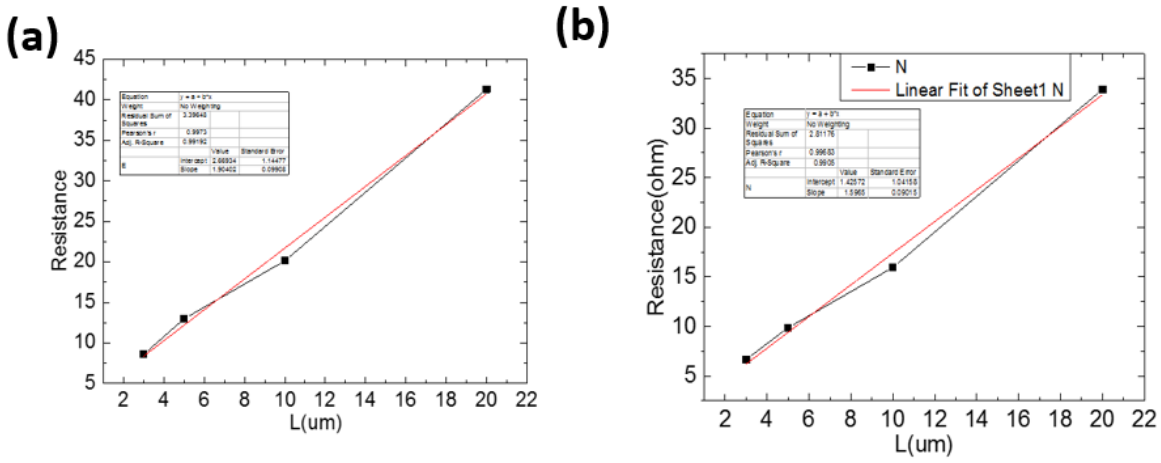

ρ_c =9.3X 10^{-7} Ohm cm^2 ρ_c =3.1X 10^{-7} Ohm cm^2

Figure 16. (a) Base Pressure = 1 x 10^{-6} torr. (b) Base Pressure = 1.2 x 10^{-7} torr.

The contact resistivity of nickel silicide on P-type SiGe ($8x10^{19}$ cm^{-3}) has also been tested (Ni = 16nm, RTA = 500°C, and base pressure = 1.2 x 10^{-7} torr). The contact resistivity is $3.83x10^{-6}$ Ω ·cm^2. The contact resistivity is higher on P-type SiGe than on N-type Si substrate. This is due to the rough interface and nickel germanosilicide agglomeration on the surface of P+ SiGe, as described in [10].

After the silicidation process, PMMA lift-off is used to form the metal wires and pads. The lift-off resist is a 200nm PMMA layer patterned by EBL. The 100nm Al layer used for metal pads and wires is deposited by e-beam evaporation. The source region of a FinHBT test device after metal deposition is shown in Figure 17. The evaporation step has enough step coverage to ensure that the metal strip is continuous across the isolation trench.

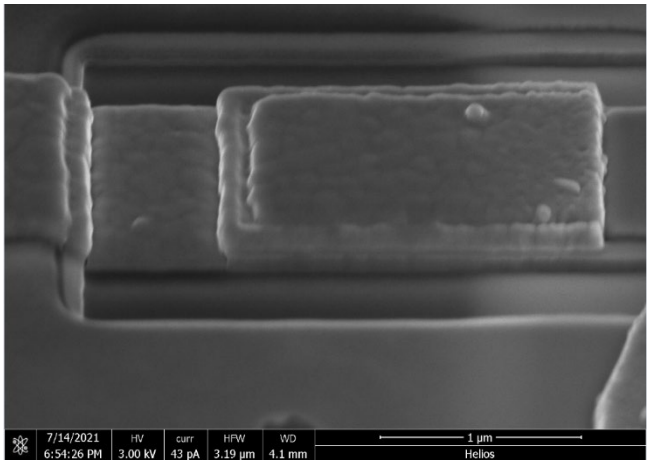

Figure 17. Device After 100nm Al Deposition

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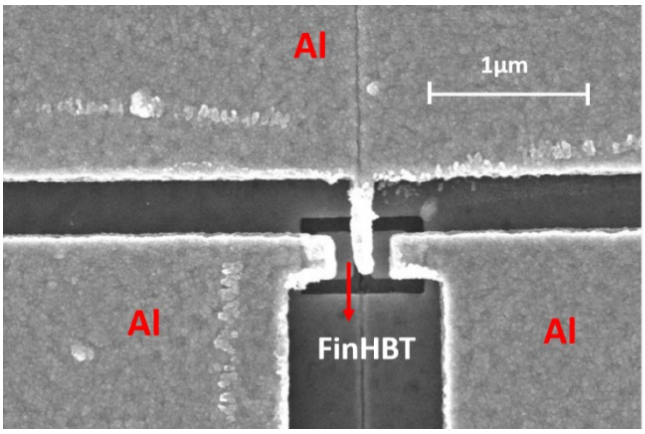

Figure 18. Device After Metallization (Negligible Alignment Error).

3.4 DC/RF T-FinHBT Characterization Procedure and De-Embedding Structures

Both DC and RF performances of FinHBT devices are characterized after fabrication at the end of Phase 1. The procedure of achieving DC and RF figure-of-merit plots will be discussed in the following section. First, the FinHBT DC performance metrics including DC current (I_C and I_B), current gain (β), and transconductance (g_m) can be obtained by Gummel plot. The detailed measuring procedure is as follows:

1. Set up the V_{CE} = 1.25 V
2. Sweep the V_{BE} from 0 to 1 Volt
3. Record the base current and collector current for each V_{BE}
4. Plot the I_B and I_C (log scale) versus V_{BE}
5. Repeat for different V_{CE}

To realize the DC performance measurements, metal pads with 100x100 μm^2 area are designed and fabricated for DC probing as shown in Figure 19.

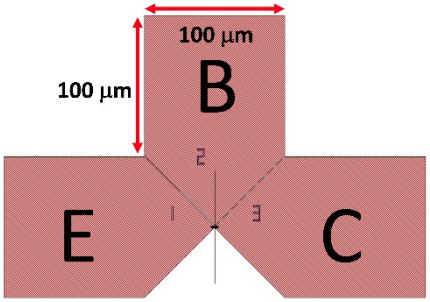

Figure 19. The Layout of DC Probing Pads

For RF applications, cut-off frequency (f_t) and maximum oscillating frequency (f_{max}) are two critical figures-of-merit to be measured and determined. The two parameters directly impact the operating frequency limit of an RF circuit. The f_t is determined from the short-circuit current gain (h_{21} parameter), which is defined as

$$h_{21} = \frac{\Delta I_2}{\Delta I1} \; when \; V_2 = 0 \text{ and } h_{21} = 1 \text{ when } f = f_t. \quad (1)$$

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Typically, an f_t versus bias current I_C or biasing voltage V_{BE} will be plotted to explore the optimal biasing point. Therefore, the f_t measurement procedure is discussed in the following. First, a proper V_{BE} and V_{CE} (1.25V) are set. Next, the h_{21} is measured at a different frequency (e.g., 10 to 50GHz). Assuming a single pole, a -20dB/dec will be obtained plotting h_{21} versus frequency. The f_t is extrapolated to the frequency such that $h_{21} = 1$.. This will be recorded, and the measurement will be repeated for different biasing conditions.

The f_{max} can be related to unilateral gain (U). The condition for f_{max} is defined as

The maximum available gain (MAG) = 1 when $f = f_{max}$ (2)

To explore the optimal biasing point, f_{max} versus bias current I_C or biasing voltage V_{BE} will be plotted. Therefore, the f_{max} measurement procedure is discussed in the following. First, a proper V_{BE} and V_{CE} (1.25V) are set. Next, the source (Z_s) and load impedance (Z_L) will be adjusted to provide a conjugate match for every frequency (e.g., 10 to 50GHz). The MAG will also be recorded for a different frequency. Assuming a single pole, there will be a -20dB/dec slope plotting MAG versus frequency. The f_{max} is extrapolated to the frequency such that MAG = 1. This will be recorded, and the measurement will be repeated for different biasing conditions.

To realize RF measurement for the fabricated FinHBTs, de-embedding structures are important to extract the intrinsic parameters accurately. Short-Open-Thru is built for de-embedding calibration, and the designed structures are shown in Figure 20. The input and output GSG are separated for 250μm to avoid interference between two GSG probes. The track width is 20μm and the gap is 12μm, which provides a characteristic of 50 Ohm.

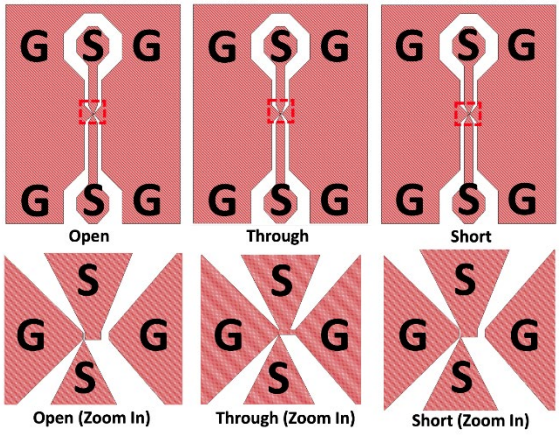

Figure 20. The Layout of De-embedding Structures

Figure 21 shows a typical de-embedding model. The goal is to subtract the additional components – $Y_{1\text{-}3}$ and $Z_{1\text{-}3}$ – and obtain the intrinsic FinHBT performances. The de-embedding procedure is discussed in the following. First, measure the S parameters of all the structures including the device under test (DUT), open and short structure. Next, subtract out the parasitic of pads by using the Y parameters ($Y_{no\_pad} = Y_{DUT} - Y_{open}$) and obtain the Y parameters without pads. Then, subtract out the parasitic of wires by using the Z parameters ($Z_{intrinsic} = Z_{no\_pad} - Z_{short}$) and obtain the

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Z parameters of the intrinsic FinHBT. Finally, transform the Z parameters into H parameters and obtain the h_{21} component.

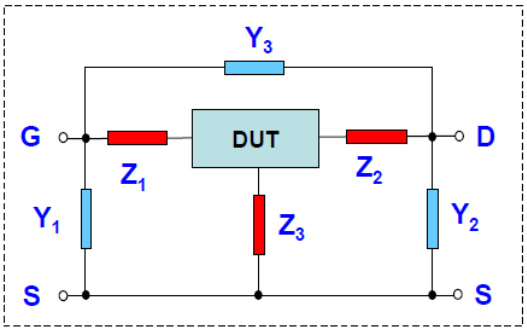

Figure 21. Typical Two-Port Model for De-embedding

3.5 3.5 T-FinHBT Frequency Dividers Design & Layout

To realize the circuit application of the FinHBTs, a Miller divider is implemented to demonstrate the pre-scaler circuit. The block diagram of a typical Miller divider is shown in Figure 22. The Miller divider is composed of three main blocks: a mixer, an amplifier, and a low-pass filter (LPF). The entire system is targeted to operate at 600GHz or near transistor f_{max}.

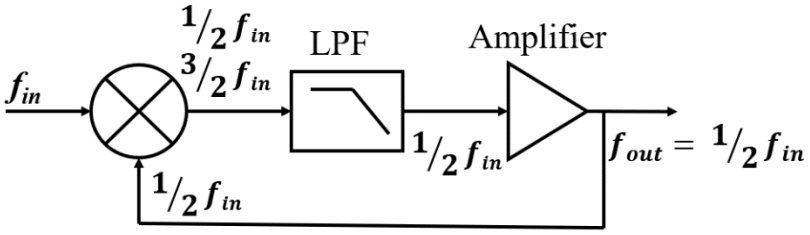

Figure 22. Block Diagram of a Typical Miller Divider

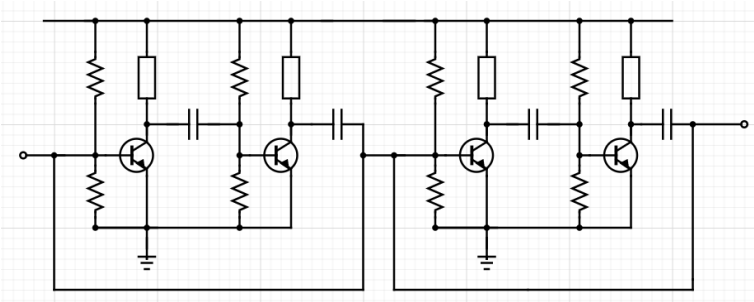

Figure 23. Circuit Diagram of Implemented ¼ Prescaler

Figure 23 shows the actual implementation of the divider. Since the goal is to demonstrate a 1/4 prescaler, a cascaded Miller divider is implemented. This circuit consists of two Miller dividers, and each stage can produce half of the input frequency. The design philosophy of the first stage Miller divider is discussed. The same design procedure is applied to the second stage.

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First, the mixer is designed to operate at a frequency of around 600GHz. With the presence of both the 600GHz signal from the input and the 300GHz signal from the feedback path at the base terminal, the mixer will produce the collector current with 300GHz, 600GHz, and 900GHz frequency components. Detailed calculation is shown below:

$$I_c = I_S exp^{\frac{V_{BE}+V_{in}+V_{out}}{V_T}} = I_Q e^{\frac{V_{in}}{V_T}} e^{\frac{V_{out}}{V_T}} = I_Q \left(1 + \frac{V_{in}}{V_T}\right)\left(1 + \frac{V_{out}}{V_T}\right)$$

$$= I_Q \left(1 + \frac{V_{in}}{V_T} + \frac{V_{out}}{V_T} + \frac{V_{out}}{V_T}\frac{V_{in}}{V_T}\right)$$

$$= I_Q \left(1 + \frac{V_{IN}}{V_T} cos\,(\omega_{in}t) + \frac{V_{OUT}}{V_T} cos\,(\omega_{out}t) + \frac{V_{OUT}}{2V_T}\frac{V_{IN}}{V_T}(cos\,cos\,((\omega_{out} - \omega_{in})t) + cos\,cos\,((\omega_{out} + \omega_{in})t))\right) \quad (3)$$

A quarter-wavelength transmission line is tuned around 300GHz and is implemented between the supply and the collector node. It is a coplanar structure, with L = 250 μm, stripe width = 5 μm, gap width = 3μm, and Z_0 = 50 Ohm. With this transmission line implemented, the 300GHz current component will see an open, and therefore all the power will flow into the next stage.

Typically, an LPF will be implemented to filter the 600GHz and 900GHz signals. However, the 900GHz signal power will be automatically surpassed by the transistor since it already exceeds f_{max}. The 600GHz signal will also be surpassed due to the transmission line. Note that a quarter-wavelength transmission line for 300GHz is a half-wavelength transmission line for 600GHz. Therefore, a RF short will be transformed to the collector node and terminate the 600GHz signal. The DC blocking capacitor is designed to be 220fF with an impedance = 1 Ω at 300GHz. Since the purpose of this capacitor is to provide isolation between the mixer stage and amplifier, the designed capacitor impedance only occupies less than 5% of the amplifier input impedance. Followed by the DC blocking capacitor, an amplifier is designed to amplify the 300GHz signal. The transistor will be biased around the f_{max} region, which will provide a gain of 2 for the 300GHz signal.

$$I_c = I_S exp^{\frac{V_{BE}+V_{in}}{V_T}} = I_C e^{\frac{V_{in}}{V_T}} = I_C \left(1 + \frac{V_{in}}{V_T}\right) = I_C + \frac{I_C}{V_T} V_{IN} cos\,(\omega_{in}t) \quad (4)$$

Passive components such as resistor and capacitor are also designed for integration in the Miller circuit. Resistors (illustrated in Figure 24) are designed to have $Rsq = 150\ \frac{\Omega}{square}$. It is located at the silicon wafer level and is done by implantation. Capacitors are designed to be interdigitated with a capacitance of 0.035fF/μm (illustrated in Figure 25). It is made of aluminum and SiO_2. The spacing and height of the metal interconnect is 300 nm, and the finger width is 500 nm.

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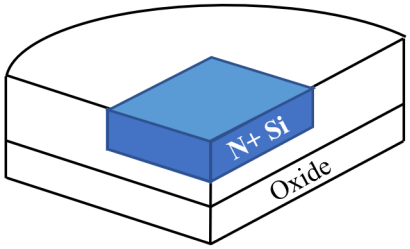

Figure 24. Illustration of the Resistor Structure

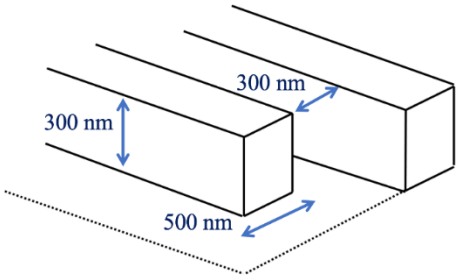

Figure 25. Illustration of the Capacitor Structure

A complete layout for the 1/4 prescaler is also shown in Figure 26. The layout consists of two stages divide-by-2 Miller divider. The area is 800 x 800 μm^2. The DC pads are located on the north/south side of the design. Four individual DC pads are created to provide the flexibility of individual supply adjustments. The input comes from the west GSG pads while the output can be taken out through the east side GSG pads. The inactive area is covered by a metal plate to provide a solid connection to the ground. A complete chip layout for phase 1 demonstration is shown in Figure 27. The chip includes a DC DUT array, RF DUR array, de-embedding structure, frequency dividers and other test structures.

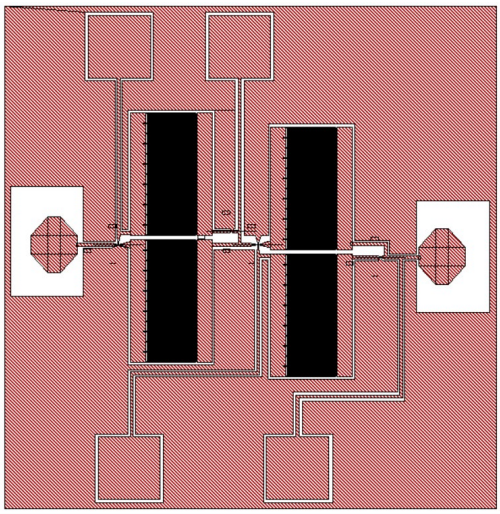

Figure 26. Layout of the Miller Divider

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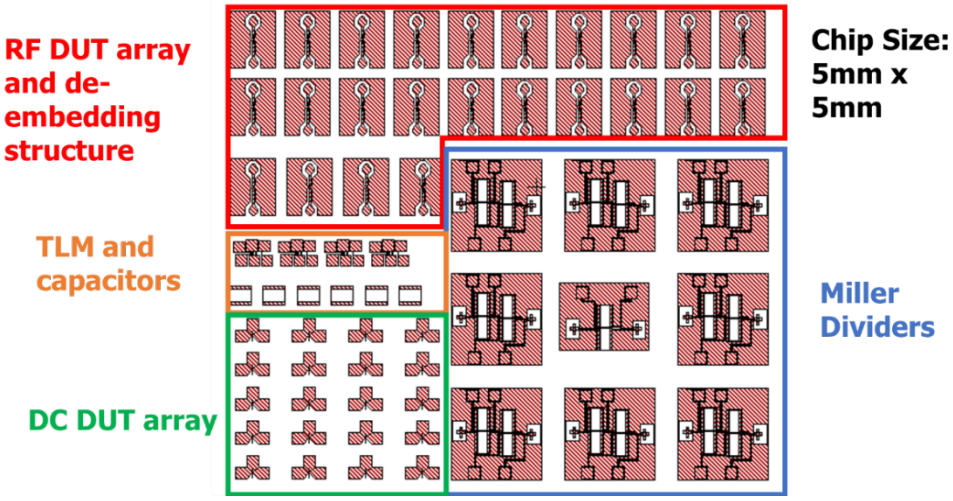

Figure 27. T-base FinHBT Mask Layout for Phase I

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4 RESULTS AND DISCUSSIONS

4.1 FinHBT DC Measurement

T-base FinHBT with a base width of 100nm is successfully fabricated. The estimated parameters of the device are shown in Table 5. The average doping concentration is measured by sheet-resistance calculation and the base Ge% is measured by an ellipsometer.

Table 5. Parameters of the Fabricated FinHBT

Base Width	100nm
Fin Width	100nm
Fin Height	50nm
Emitter/Collector size	1μm/1μm
Extrinsic base width	300nm
Base Ge%	15%
Emitter/Collector Doping	$8x10^{19}cm^{-3}$
Base doping	$2x10^{19}cm^{-3}$

The measured device DC characteristics are shown in Figure 28 through Figure 30. The device's Gummel plot is given in Figure 28(a). While the turn-on slope of I_C is close to the ideal 60mV/dec, the ideality factor of I_B is larger than 1, especially with a small V_{BE}. This is likely due to the existence of defects or vacancies in the base region. During the SiGe growth in the base trench, grain boundaries will form in the middle of the base when the SiGe grown from the base trench sidewalls merge in the middle. For the CVD process, it is possible that the top of the trench is filled without completely filling the bottom of the trench. This will result in vacancies in the base. Although annealing done after the growth can potentially suppress the defect density, it still causes notable Shockley-Read-Hall Recombination (SRH) recombination. This leads to the <1 gain at small V_{BE}. While the defect density can be suppressed by annealing, the vacancies may still exist after the annealing. This can be proved by the reverse emitter-collector Gummel plot in Figure 28(b). The I_C is reduced, and the gain is also smaller. The possible reason for this is the existence of voids in the base. The void will decrease the effective base width. When the void is not located in the middle of the base, asymmetric behavior can be observed when swapping the emitter and collector, like in Figure 28(b). Further optimization of the SiGe epitaxial process is necessary to eliminate the void and asymmetric device behavior.

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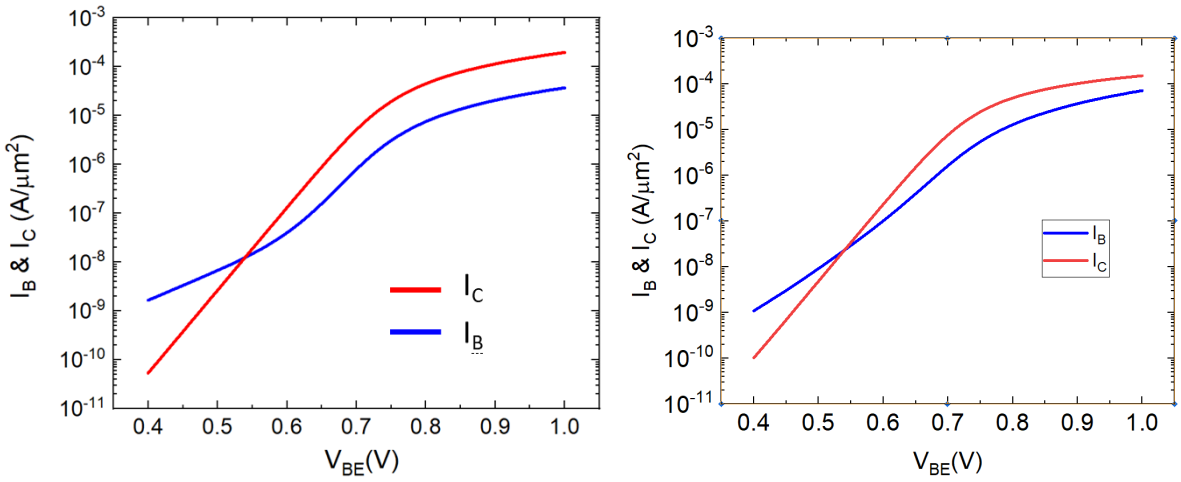

Figure 28. Measured Gummel Plot of the FinHBT (a) and (b) Swapping Emitter and Collector

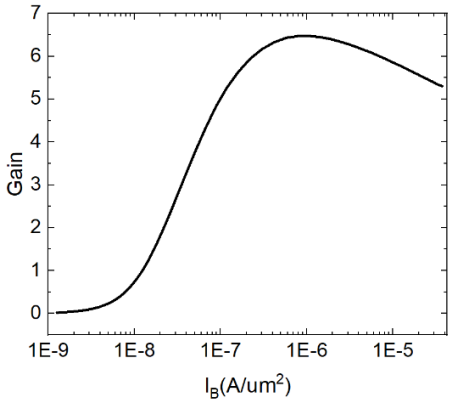

Figure 29. Measured Gain vs. I_B of FinHBT

The gain vs I_B is shown in Figure 30. The peak DC gain is about 6.5 at $I_B = 2.5\mu A/\mu m^2$. Measured common-emitter characteristics. Current saturation can be observed. There is an asymmetric 0.015V V_{CE}-offset that can be caused by the asymmetric device behavior due to the void in the base. The measured open-base breakdown voltage is 1.5V.

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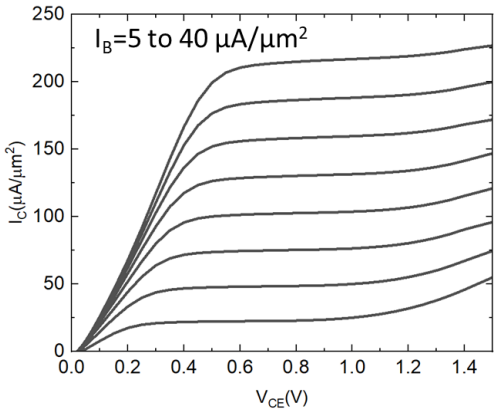

Figure 30. Measured Common-Emitter Characteristics of FinHBT

4.2 FinHBT RF Performance Simulation

Based on the measured data of 100nm base FinHBT, the RF performance of further scaled FinHBT can be predicted by TCAD. Like in the FinFET and FinHBT study, the Sentaurus TCAD platform is used for the FinHBT study. The calibrated hydrodynamic model [11] is adopted to capture the velocity overshoot in the deeply scaled device. In addition, high field mobility saturation, doping-dependent mobility, Auger recombination, Shockley-Read-Hall recombination, and bandgap narrowing have been enabled.

The FinHBT with parameters in Table 5 is simulated. The emitter/collector and base contact resistance are used to fit the measured results. The result of the fitting is shown in Figure 31. Simulated and measured Gummel plot of FinHBT. The fitted contact resistance is 1.1 kΩ for the emitter and collector and 4.5 kΩ for the base. Although the base contact region has been enlarged by the T-base structure, the base resistance is still substantially higher than the emitter and collector. This is likely due to the relatively smaller contact area and larger silicide resistance on p-type SiGe.

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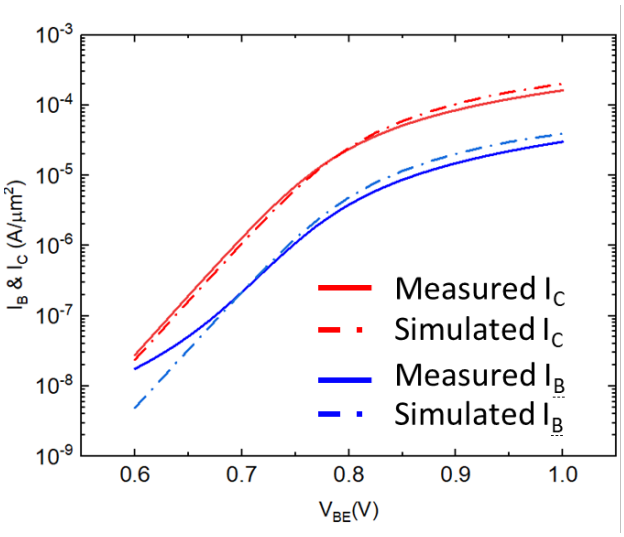

Figure 31. Simulated and measured Gummel plot of FinHBT

Based on this result, the T-base FinHBT structure with scaled base width has been designed and simulated. The 3D structure and the cross-section of the simulated T-base device with 20nm W_{base} are shown in Figure 32. The doping and Ge profile is shown in Figure 33. The parabolic-shaped Ge profile is fitted to the SIMS profile of a vertical SiGe HBT in [12]. The doping profile in the emitter/collector resembles the doping profile in the source/drain and spacer region of a FinFET [13]. Enlarged emitter/collector regions are used to mitigate the effect of emitter/collector contact resistivity. The T-base structure is adopted to reduce base contact resistivity. The doping concentration in the T-base is $1x10^{20}$ cm^{-3}. The intrinsic SiGe base doping concentration is $8x10^{19}$ cm^{-3}.

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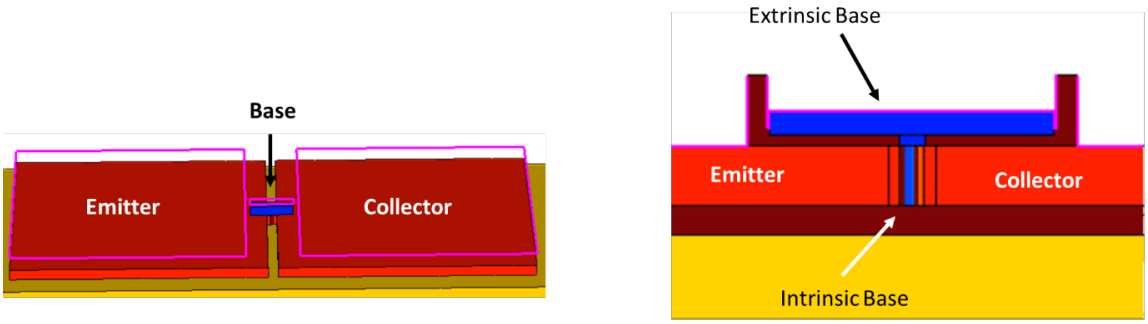

Figure 32. Simulated T-base FinHBT

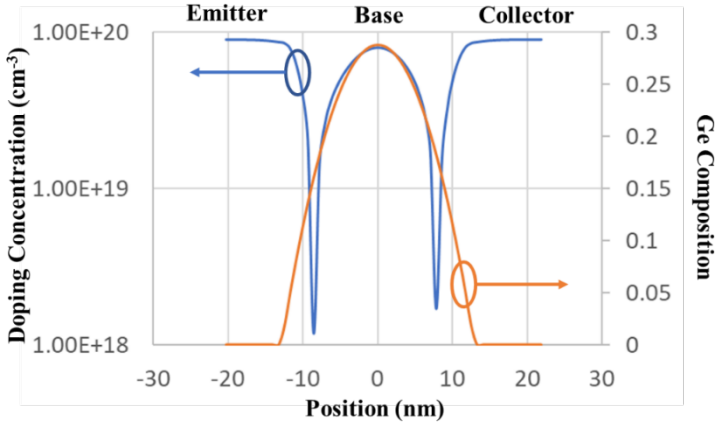

Figure 33. Doping and Ge Profile in the Simulated FinHBT with a Base Width of 20nm

The detailed parameters and simulated device characteristics are shown in Table 6. Two types of scale FinHBT are proposed. Device 2 has a base width of 20nm, which is similar to the channel width of a 10nm FinFET. In Device 1, the base width is further scaled to 10nm, which can be defined by the EUV technology in sub-5nm technologies. The contact resistance is $1x10^{-8}$ Ω-cm^2 for Device 1 and further improved to $1x10^{-9}$ Ω-cm^2 in Device 2. With the narrow base width, the base doping concentration needs to be increased to prevent base punch-through. The Ge composition of the base region is also increased to 30% to boost the current gain and f_T/f_{MAX} by enhancing the carrier transport in the base with the built-in electric field.

Table 6. Simulated Characteristics of T-base FinHBT

	Device 1	**Device 2**	**DC Test Device**
Base width	10nm	20nm	100nm
Contact resistivity	$1x10^{-9}$ Ω-cm^2	$1x10^{-8}$ Ω -cm^2	$1x10^{-6}$ Ω -cm^2
Ex-base width	100nm	100nm	300nm
Base Doping	$8x10^{19}$cm^{-3}	$8x10^{19}$cm^{-3}	$2x10^{19}$cm^{-3}
Base Ge%	30%	30%	15%
f_T	814GHz	600 GHz	
f_{MAX}	751GHz	620 GHz	
DC gain	220	169	6.5

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The simulated Gummel plot and f_T & f_{MAX} vs I_C for Device 1 and Device 2 are shown in Figure 34 and Figure 35, respectively. Peak f_T /f_{MAX} and I_C increase as the base width scales down. As W_B reduces from 20nm to 10nm, f_T/f_{MAX} increases from 600/620GHz to 814/751GHz. The delay components are extracted in Figure 36. The forward transit time (τf) of ~156fs is extracted from Figure 36(b) based on:

$$\frac{1}{2\pi f_T} = \left[\tau_f + \frac{kT}{qI_C}(C_{be} + C_{bc}) + C_{bc}(R_e + R_c)\right] \qquad (5)$$

where kT/q, I_C, C_{be}, C_{bc}, R_e, and R_c are thermal voltage, collector current, base-emitter capacitance, base-collector capacitance, emitter resistance, and collector resistance, respectively. The extracted $\tau_F + \tau_C$ and capacitance charging delay is shown in Table 7. The results show that τ_F and τ_C are the main contributors to the reduction of delay time as base width scales down. This is a result of increased carrier velocity and decreased base width. Therefore, τ_F decreases as the base width scales down, leading to the increased f_T.

Table 7. Delay Components of Device 1 and Device 2

	τF + τC	**Charging Delay**
Device 1	156 fs	42 fs
Device 2	203 fs	60 fs

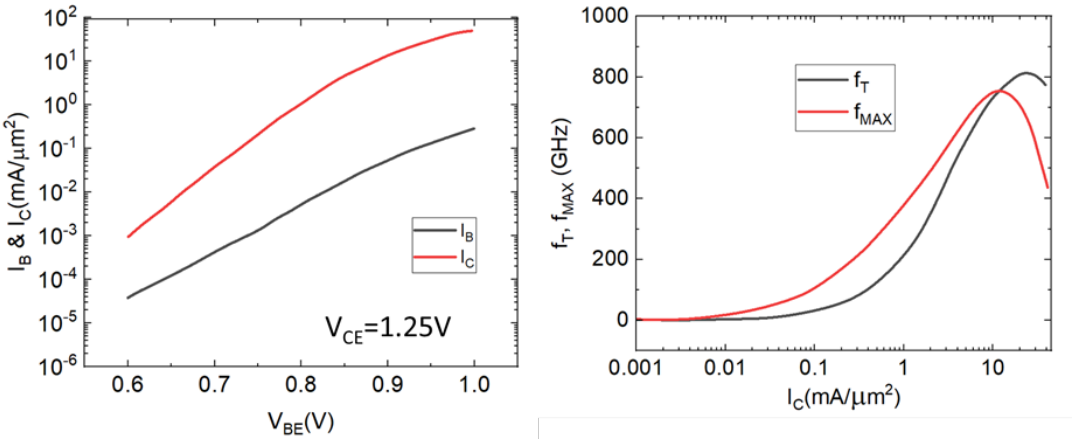

Figure 34. Simulate Gummel Plot and f_T/f_{MAX} of Test Device 1

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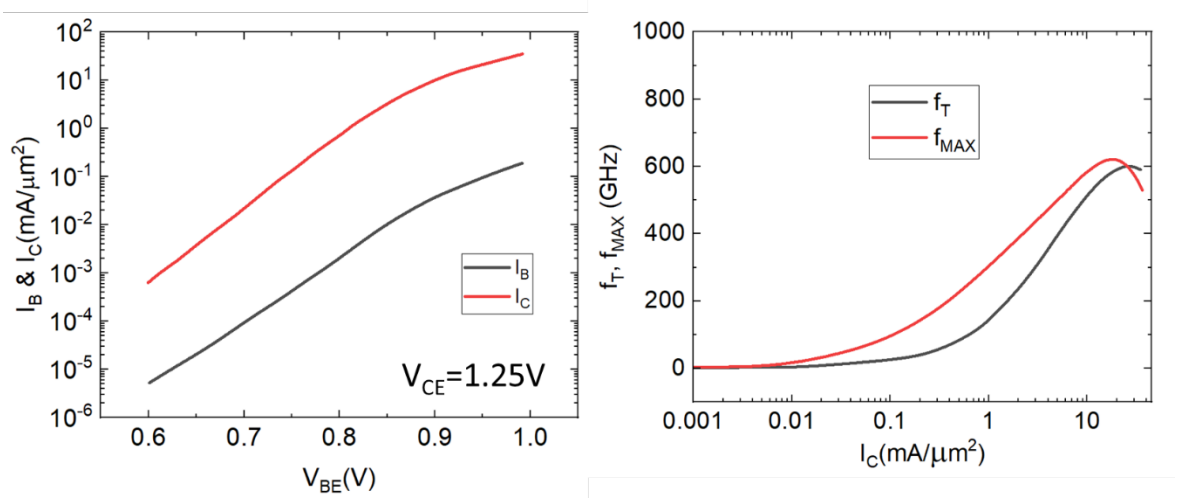

Figure 35. Simulate Gummel Plot and f_T/f_{MAX} of Test Device 2

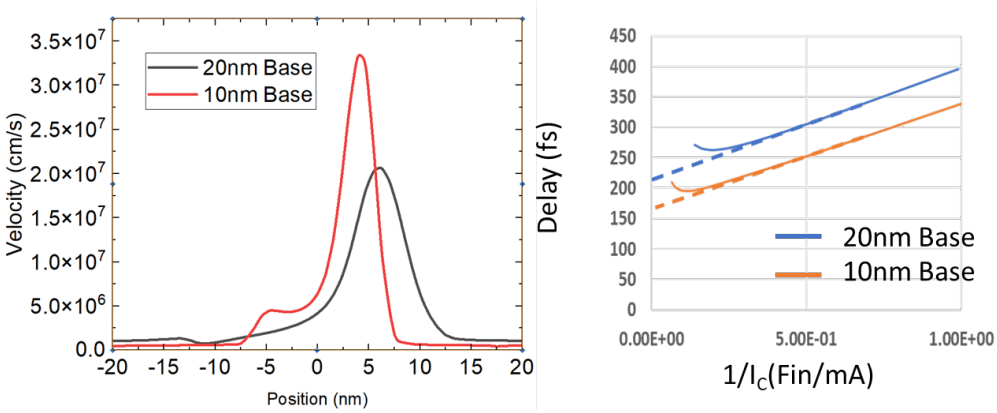

Figure 36. Carrier Velocity Profile and Delay Components Extraction

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5 CONCLUSION

The process modules for T-base FinHBT fabrication on SOI substrate are developed with individual process module validated as well. A test device has been successfully fabricated and characterized. With a 100nm base width and 15% peak Ge composition, the maximum measured DC gain is 6.5. Asymmetric device characteristics are observed in the slightly uneven 0.015 $V_{CE\text{-}Offset}$ values measured between active/reverse-active operation modes as shown in Figure 37. This may be caused by the existence of asymmetric voids grown in the base region. The voids can also lead to an increased defect density in the base region, which degrades the I_B. To resolve this issue, further optimization of the RPCVD process is necessary. This problem can also be alleviated by using the atomic-layer RPCVD epitaxial process. The performance of the FinHBT can also be improved by raising base Ge content to a higher level (~30%). With higher Ge content, the band misalignment will be increased, which will suppress the leakage current and improve the gain.

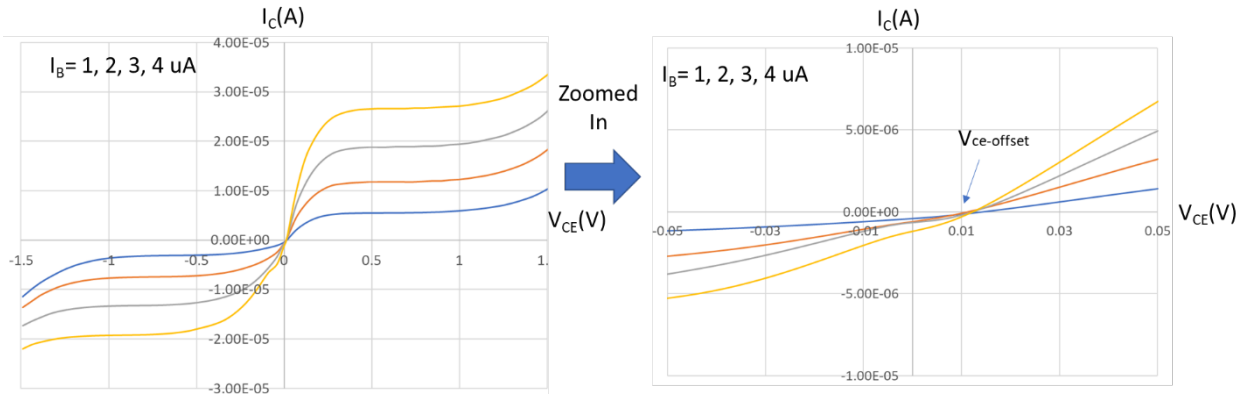

Figure 37. Asymmetric $V_{CE\text{-}offset}$ in the two directional common-emitter measurement

Based on the experiment result, the T-base FinHBT structure with scaled base width has been designed and simulated. The Ge content in the SiGe base is assumed to be 30% to improve the RF performance. The simulations predict that as W_B reduces to 20nm, the f_T/f_{MAX} can reach 600/620GHz. Further decreasing W_B to 10nm can further push the f_T/f_{MAX} to 800/750 GHz. This shows that with further lateral scaling, the FinHBT can potentially approach f_T/f_{MAX} close to THz.

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LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS

ACRONYM	DESCRIPTION
ALD	Atomaic layer deposition
AFM	Atomic force microscopy
BiCMOS	Bipolar CMOS
CMOS	Complementary Metal-Oxide-Semiconductor
DCS	Dichlorosilane
EBL	Electron beam lithography
FinFET	Fin Field Effect Transistor
GSG	Ground signal ground
HBT	Heterojunction bipolar transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
RF	Radio Frequency
RIE	Reactive-ion etch
RPCVD	Reduced-pressure chemical vapor deposition
RTA	Rapid thermal annealing
SEG	Selective epitaxial growth
SEM	Scanning electron microscope
SoC	System on Chip
SS	Subthreshold Swing
TCAD	Technology Computer-Aided Design
VLSI	Very-Large-Scale Integration

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