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MILLIMETER-WAVE ULTRA-WIDEBAND LINEAR FRONT-END INTEGRATED CIRCUIT (MULFI)

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14. ABSTRACT

This project explored the design of wideband mm-wave CMOS transceivers with enhanced linearity, applicable to modern highly linear front-end modules. The enhanced linearity is particularly needed when interfacing these circuits to front-end modules to enhance the output power, the sensitivity, or to address a particular frequency band.

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CMOS, transceiver, linearity, mm-wave, wideband

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1 INTRODUCTION

This research project aimed to advance the state-of-art design of CMOS transceivers to address emerging applications in digital beamforming, as highlighted from our "vision" figure of Fig. 1.1. The overarching goal has been to maximize the linearity and bandwidth of a CMOS receiver and to maximize the linear output power of a wideband transmitter. The aim of the project is to provide a "common module" realized in low cost CMOS technology that can be placed behind a high performance front-end module designed for a specific band or application, as shown in Fig. 1.2. As such, the "common module" should be as flexible as possible, accommodating different LNA gain requirements and PA output power, modulation schemes, and other transmitter specifications.

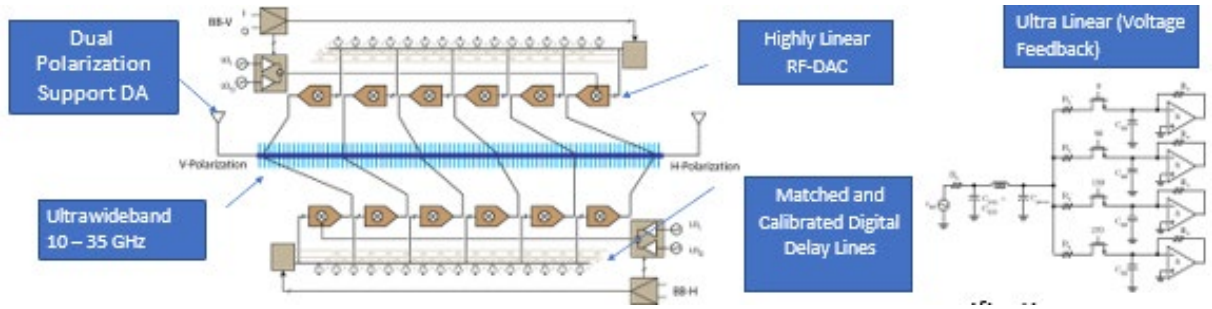

Figure 1.1: High Level Vision for the Berkeley MIDAS Project

In the receiver, we favor linearity over noise performance, since the front-end module will provide gain and set the sensitivity, whereas linearity is of utmost importance, since the signals presented to the digital beamformer are not spatially filtered and are gained up by the LNA gain. We explored "mixer first" receivers, typically used at lower RF frequencies, since they provide excellent linearity, set by the switch on-resistance, and naturally provide a tunable bandpass response around the LO frequency. Our efforts focused on advancing N-path mixer techniques from sub-5 GHz RF domains up to mm-wave frequencies, up to 35 GHz in this project.

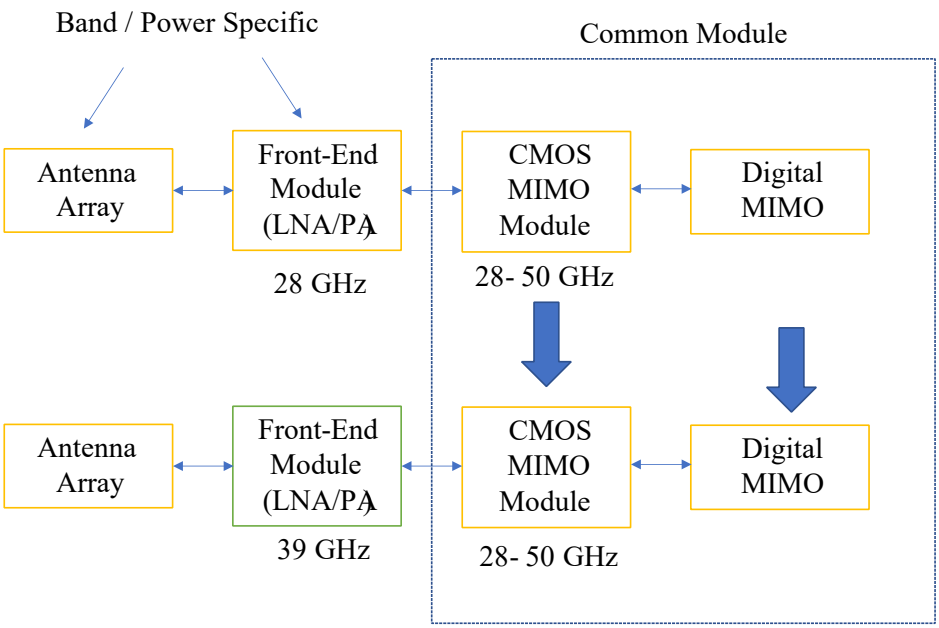

Figure 1.2: Proposed Wideband "Common Module" Covers 28-50 GHz RF Bandwidth at the Input with 200 MHz Baseband Bandwidth and can Interface to Many Different Front-end Modules to Realize Different Functionality

The design of a prototype in 28nm technology is described in detail in Ch. 2. This prototype was fabricated, tested, and published both as a conference paper [21] and a journal paper [18]. While this prototype demonstrated excellent performance, with an input bandwidth from 10-35 GHz and a baseband bandwidth of 200 MHz (I + Q), an excellent record high in-band IIP3 of +14.1 dBm, it suffered from relatively high noise of 12.5 dB. While acceptable in applications where the front-end gain is sufficiently large, in some applications this design may fall short on the sensitivity specification.

An improved second generation design has been investigated and fabricated using the same CMOS 28nm technology, but with much better noise performance. This second generation prototype is described in Ch. 3.

On the transmitter side, our goal was to design a flexible architecture that could work with many different modulation schemes. An RF-DAC topology utilizing distributed combining was investigated, combining a baseband DAC, analog filters, and distributed up-conversion mixers that drive different points on a transmission line to combine I and Q signals and to boost the output power compression point. The prototype is described in great detail in Ch. 4.

To further enhance output power, Ch. 5 details our investigation into CMOS power amplifiers that could provide high output power with good back-off efficiency, such as a Doherty power amplifier. A novel scheme was proposed to control the bias point of a Doherty PA dynamically, and a prototype modest bandwidth 28 GHz amplifier was designed, fabricated (Global Foundries 45nm-SOI), and we are awaiting fabricated die to begin testing.

To improve the bandwidth and flexibility of the design, we also investigated a novel configuration of a Load Modulated Balanced Amplifier (LMBA), described in Ch. 6. Traditionally balanced amplifiers provide excellent bandwidth but suffer from back-off efficiency. The power amplifier back-off efficiency can be improved by using load modulation inherently provided by the balanced architecture. Our goal was to utilize the balanced architecture for power combining, load modulation, and VSWR robustness. A proof-of-concept prototype has been designed and is in fabrication in 28nm CMOS.

2 DESIGN OF HIGH LINEARITY MIXER-FIRST RECEIVERS FOR MM-WAVE DIGITAL MIMO ARRAYS

A 10–35GHz mixer-first receiver is proposed for use in digital MIMO arrays. Techniques are proposed to enhance the linearity of such receivers, both at baseband and the RF mixer switches. Techniques to mitigate charge sharing due to LO overlap are also proposed. Detailed simulation results are provided to illustrate the benefits of these techniques. An integrated circuit prototype is fabricated in 28nm bulk CMOS and fully characterized. The receiver has built-in programmability to trade-off gain for linearity. The receiver achieves a peak in-band IIP3 of +14.1dBm, a peak gain of 14.5dB and a noise figure of 12.5dB, in its nominal setting.

2.1 Introduction

The next generation of mobile wireless promises to offer enhanced user experience with 100x end user data rates and lower latency, by exploiting spatial dimension of communication using multiple antennas at the transmitter and receiver [6, 33]. To serve multiple users (K) simultaneously, massive MIMO (Multiple-Input Multiple-Output) systems have base-stations with large number of antennas M, with $M \gg K$ [25]. MIMO systems with a small number of concurrent beams [27, 17, 34] have used RF phase shifters for spatial filtering, in an attempt to save LO and baseband power. However, for massive MIMO arrays which serve a larger number of users, higher degree of spatial flexibility is desired. The $K \times M$ number of phase shifters required in multi-user MIMO systems makes the implementation of vector interpolator based active RF phase shifters [27, 17] prohibitively power hungry. Use of passive transmission line based phase shifters [34] results in loss and a large area penalty.

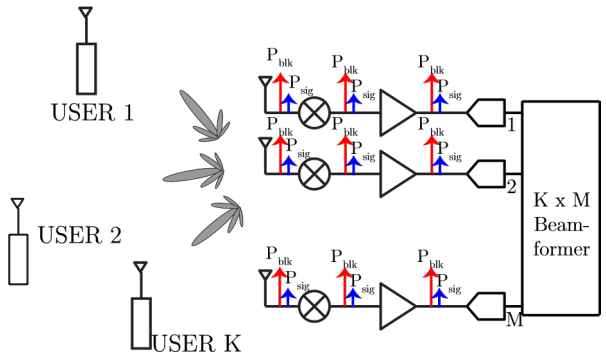

Figure 2.1: Digital beamforming receiver array for massive MIMO systems

To this end, it is desirable to have massive digital beam-forming arrays for systems with high spatial flexibility. Since the noise of the receiver front-ends is mostly uncorrelated across the array, the beamforming operation results in a $\sim 10\log(M)$ boost of the signal-to-noise ratio (SNR) due to noise averaging, where M is the number of antennas in the array. As a result, in massive arrays, the noise figure requirement of each individual receiver can be relaxed [30]. On the other hand, digital beamforming architectures mandate high linearity requirements. As spatial

filtering of outof-beam, in-band interferers is performed at the baseband, the RF front-end needs to be highly linear to handle these interferers (see Fig. 2.1).

The mm-wave 5G spectrum covers a wide range of bands, including bands ranging from 24–40GHz. Traditional circuit techniques, using tuned front-ends [27, 17, 34], cannot support the entire band with a single transceiver. It is desirable to have a single integrated circuit solution to support operation across the entire mm-wave 5G band. This mandates the need for wideband highly linear receiver front-ends.

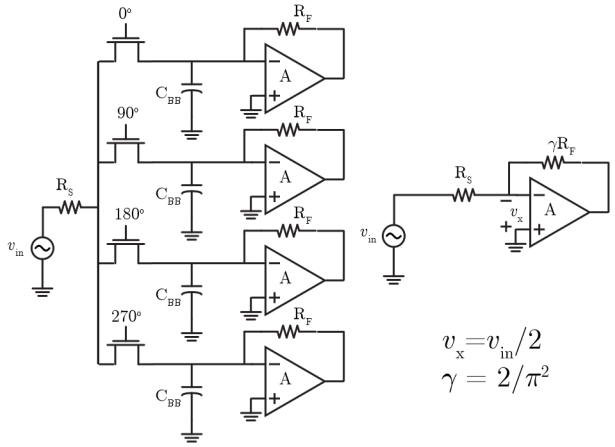

Figure 2.2: Conventional N-path Filter and its LTI Equivalent

Passive mixer-first receivers or N-path-filter-based receivers (see Fig. 2.2) have been used at lower RF frequencies for high linearity across a wide band of operation. A lot of focus of the research at lower RF frequencies has been to improve the resilience to out-of-band interferers. The impedance translational property of N-path filters has been used to synthesize tunable high-Q band-pass filters. While passive mixer-first receivers and their enhancements [5, 36, 20] have made strides towards improving out-of-band IIP3, the in-band linearity of such receivers is still limited by the linearity of the baseband amplifiers.

N-path filters at RF frequencies use *N* non-overlapping square-wave LO phases (usually *N* =4) to drive the mixer switches. Today, such an LO waveform cannot be synthesized at mm-wave frequencies even in the most advanced process nodes. A common solution in mm-wave mixerfirst receivers like [13] is to use pseudo non-overlapping sine-wave LO drive, at the cost of reduced mixer switch linearity. In [22], we proposed a broadband highly linear mixer-first receiver frontend exploiting feedback linearization, which addresses the aforementioned issues.

Compared to [22], this work provides greater detail on the benefits and limitations of feedback linearization. It also delves into great detail about enhancing linearity of mixer switches and provides simulation results supporting the superior mixer IIP3 of our architecture compared to others. It also describes the challenges associated with LO waveform generation for N-path filters at mmwave frequencies, and provides solutions. Additionally, it provides more extensive

measurement results compared to [22]. Finally, this work demonstrates why this architecture is a good candidate for an LNA-based receiver front-end driving a passive mixer.

The content of this chapter is organized as follows. Section 2.2 describes the architecture and circuit design details. It provides simulation results to highlight the various salient features of this work. Section 2.3 presents the measurement results, and Section 2.4 compares this work against the state-of-the-art and provides the key takeaways of the work.

2.2 Feedback Linearization

Fig. 2.2 shows the architecture for a conventional passive mixer-first receiver driven by a 4-phase non-overlapping square wave LO drive, and its LTI equivalent, where the baseband impedance is scaled by a factor $\gamma = 2/\pi^2$ [4].[1] As detailed in [4], the impedance translational property of these N-path filters is used for input matching. An explicit shunt termination resistance at baseband would yield a 3dB noise figure penalty. Therefore, input matching is performed in these receiver front-ends through a resistor R_F in feedback around an amplifier of gain A. In addition to reducing the noise figure, increasing the gain A and R_F of the amplifier also helps in achieving higher closed loop gain, given by

$$\begin{aligned} A_{CL} &\approx 1 - \frac{\gamma R_F}{R_S} \\ &\approx -\frac{\gamma R_F}{R_S} \\ &\approx A \quad \text{Under constraint of input match} \end{aligned} \tag{2.1}$$

The input impedance looking into the amplifier input is $R_F/(1+A)$. Therefore, to maintain input match, as the amplifier gain A is increased, the feedback resistance R_F also needs to be increased. This implies that the amplifier input always processes a signal equal to $v_{in}/2$, and does not benefit from feedback linearization. We will show this by analyzing the non-linearity arising from the output conductance ($g_o = 1/r_o$) of the amplifier.

The main sources of non-linearity in transistors are the transconductance non-linearity g_{m3} (V_{GS} limited), output conductance non-linearity g_{d3} (V_{DS} limited) and cross-modulation terms. However, for a transistor in saturation region, the cross-modulation terms may be neglected [16]. Additionally, when the output conductance is low, like in an inverter, the output conductance nonlinearity g_{d3} is the main source of non-linearity. This was also verified by the extraction of the

[1] Note that the shunt re-radiation resistance has been neglected in the LTI equivalent for simplicity. It will be considered while analyzing the noise figure.

parameters g_{o3} and g_{m3} of the actual inverter-based amplifier used in this work. Therefore, we restrict our analysis to V_{DS} limited non-linearity.

The drain-source current is given by $i_{ds} = g_o v_{ds} + g_{o3} v^3_{ds}$. It can be shown that the in-band IIP3 and OIP3 due to the non-linearity of the output conductance are given by

s

$$V_{IIP3} \approx \frac{1}{A}\sqrt{\frac{8g_o}{3g_{o3}}} \qquad (2.2)$$

$$V_{OIP3} \approx \sqrt{\frac{8g_o}{3g_{o3}}}$$

Consider the term g_o/g_{o3} in equation (2.2).

In order to enhance open loop gain A, if g_o is reduced, while maintaining the same g_m, g_{o3} is assumed to scale down by the same amount.[2] Now, this means that, as g_o is changed, the term g_o/g_{o3} remains constant and is a function of the bias. From the equation for in-band IIP3 and OIP3, it is seen that the in-band IIP3 degrades with increasing loop gain A and the in-band OIP3 remains a constant. This assumes that the mixer switches are perfectly linear. The linearity of the mixer switches will be dealt with in a subsequent section. Clearly, that the in-band IIP3 and OIP3 (due to output conductance non-linearity) of a conventional mixer-first front-end of Fig. 2.2 do not benefit from feedback linearization under the constraint of input match.

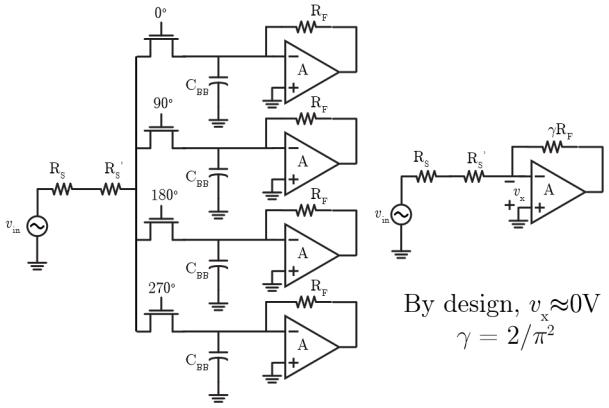

Figure 2.3: N-path filter exploiting feedback linearization and its LTI equivalent.

Now consider the architecture proposed in Fig. 2.3. Here, the input match is performed using an explicit series termination resistance R'_S. Compatibly with the digital massive MIMO requirements discussed in Section 2.1, this topology targets enhanced linearity at the cost of higher noise figure, by using an explicit series termination resistance R'_S for input match. The R_F

- [2] If g_o is decreased by increasing channel length, while maintaining same g_m, g_{o3} may not scale proportionally. However, such an assumption serves to illustrate the benefits of higher A for feedback linearization.

and gain A are chosen such that $\gamma R_F/(1+A)$ is considerably smaller than R'_S. The closed loop gain, under input-match constraint, is now given by,

$$A_{CL} \approx -\frac{\gamma R^F}{R_S \text{Node}} \tag{2.3}$$

v_x is a virtual ground whose magnitude is given by

$$\begin{aligned} \frac{v_x}{} &= \frac{\gamma R_F}{(1+A)(R_S+R'_S)+\gamma} \\ &= \frac{}{v_{in}R_F} \\ &= \frac{\gamma R_F}{2(1+A)R_S} \end{aligned} \tag{2.4}$$

For the circuit in Fig. 2.3, where input match is performed through an explicit series resistor, the feedback resistance R_F need not be changed with A to maintain input match (under the previously stated assumption $\gamma R_F/(1+A) \ll R'_S$). However, as A is increased, the virtual ground voltage v_x becomes smaller. To analyze the non-linearity of the circuit due to the output conductance, we inject a third order voltage non-linearity (equal to $g_{o3}r_oA^3v^3_x$) at the output node of the LTI equivalent circuit shown in Fig. 2.3, and compute the amount by which the negative feedback loop attenuates it. The third order non-linearity injected $v_{nl3,go}$, and the resultant output third order non-linearity $v_{o3,go}$ are given by,

$$\begin{aligned} v_{nl3,go} &= g_{o3}r_o \frac{v_{in}}{2(1+A)R_S}{}^3 \\ v_{o3,go} &= \frac{v_{nl3,go}}{1+\frac{(R(sR+sR+sR's)A}{'})+\gamma R_F} \approx \frac{v_{nl3,go}}{1+\frac{2R_S^S ARF}{\gamma}} \end{aligned} \tag{2.5}$$

Consequently, the in-band IIP3 and OIP3 are given by

$$\begin{aligned} V_{IIP3} &\approx \sqrt{\frac{8g_o}{3g_{o3}}}\frac{s}{A_{CL3}}\sqrt{\frac{s}{A}} \\ V_{OIP3} &= A_{CL}V_{IIP3} \approx \frac{}{}\sqrt{\frac{}{}}(2.6)\sqrt{\frac{s}{8g_o}}\,r\,A \end{aligned}$$

$$3g_{o3} \quad A_{CL}$$

As discussed previously, the first term $\sqrt{8g_o/3g_{o3}}$ in equation (2.6) does not vary with increasing open loop gain A and is purely a function of the bias. If the closed loop gain $A_{CL} = \gamma R_F/R_S$ is kept constant, and the open loop gain of the amplifier A is increased, the OIP3 and IIP3 increase as A, illustrating the benefit of higher linearity with increased open loop gain A. This is verified by simulation results shown in Fig. 2.4. The open loop gain A of the amplifier is swept, but the feedback resistance R_F is kept constant as the matching is performed through the explicit series resistor R'_S. Therefore, the closed loop gain A_{CL} remains constant as the open-loop gain A is swept.

However, the in-band IIP3 and the OIP3 increase as $A^{1/2}$, as seen from the slope of 0.5 in the log scale plot in Fig. 2.4.

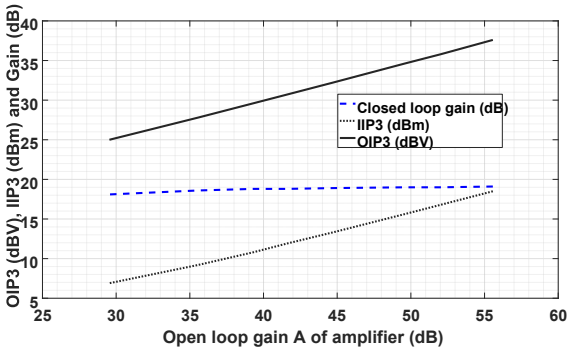

Figure 2.4: Simulated in-band IIP3, Differential OIP3 and Closed Loop Differential Gain of Proposed Architecture Versus Amplifier Open Loop Gain *A*

For the plot in Fig. 2.5, we consider the actual implementation of our circuit, where the open loop gain A of the amplifier is fixed. The feedback resistance R_F is programmable to trade-off gain for linearity. It can be seen from equation (2.3) that for a fixed open loop gain A of the amplifier, the closed loop gain A_{CL} is proportional to R_F. The IIP3 is proportional to $A_{CL}^{-3/2}$ and the OIP3 is proportional to $A_{CL}^{-1/2}$. This well-studied effect of feedback linearization is verified by the simulation plot in Fig. 2.5.

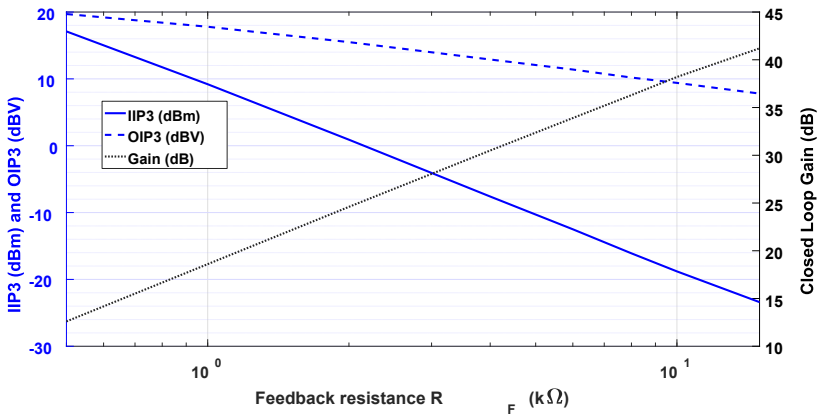

Figure 2.5: Simulated in-band IIP3, Differential OIP3 and Closed Loop Differential Gain of Proposed Architecture Versus R_F, for Amplifier Open Loop Gain A Equal to 60

Importantly, the use of shunt feedback also increases the instantaneous bandwidth of the receiver front-ends, an important requirement to support the high data rates of next generation wireless devices. To ensure high open-loop gain A for the amplifier and good common mode rejection, a current starved differential inverter-based amplifier was used. Devices with a channel length of 200nm were used to obtain a higher $g_m r_o$. However, the parasitics limit the achievable RF bandwidth to around 600MHz, for the choice of transistor widths. A higher bandwidth may be obtained with a lower channel length with a lower $g_m r_o$ at the cost of reduced IIP3.

2.2.1 Mixer Switch Linearity

It was seen in Fig. 2.5 that for a gain of ~ 18dB and ~ 12dB, an IIP3 of 9dBm and 17dBm respectively, may be achieved. However, this holds true only if the mixer switches are perfectly linear. Considering the non-linearity of the mixer switches as well, the overall IIP3 is given by the well-known cascade IIP3 formula[3],

$$\frac{1}{V_{IIP3}^2} = \frac{1}{V_{IIP2\,3,mix}} + \frac{a2mix}{V_{IIP2\,3,BB}} \tag{2.7}$$

The conversion gain of a 4-phase passive mixer is approximately unity. Therefore, to achieve the desired IIP3 of Fig. 2.5, $IIP3_{mix} \gg IIP3_{BB}$. That is, we need to build highly linear passive mixers with IIP3 much higher than 9−17dBm. Otherwise, the mixer-switch non-linearity will limit the cascade non-linearity. This is quite challenging at mm-wave frequencies. In this section, we look at various techniques to achieve high in-band linearity for passive mixers at mm-wave frequencies.

[3] Neglecting second order interaction.

Consider the proposed architecture of Fig. 2.3 with an explicit series resistor R'_S for matching. Now, there are three possible locations for the placement of R'_S. One is shown in Fig. 2.3, where there is a series resistor common to all four paths of the N-path mixer. For a 4-phase nonoverlapping LO, this is equivalent to placing one series resistor R'_S in each of the four paths, as shown in Fig. 2.6(a). The distinction between these two cases will be made subsequently. However, for now, we compare the two circuits shown in Figs. 2.6(a) and (b), where there is an explicit R'_S in each path. In Fig. 2.6(a), R'_S is placed before the mixer switch towards the RF input. In Fig. 2.6(b), R'_S is placed after the mixer switch towards the baseband amplifier.

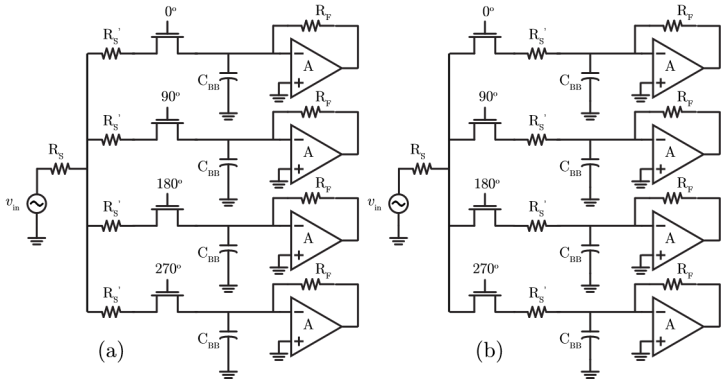

Figure 2.6: Two Variants of Proposed N-path Filter Architecture with Series Resistor R'_S (a) Before the Mixer Switches (b) After the Mixer Switches

To compare the linearity of the mixer switches in the two cases, the mixer is simulated without the baseband amplifier by terminating the mixer baseband output with a resistance equal to the input impedance ($\gamma R_F/(1+A)$) looking into the amplifier. Additionally, this resistance is terminated with a DC voltage equal to the bias point of the inverter in the desired mode of operation. The gates of the mixer switches are driven at f_{LO} = 20GHz, with a 4-phase non-overlapping square wave LO swinging from 0 to V_{DD} = 1.2V. The size of the mixer switches is swept such that R_{SW}, the mixer switch ON resistance, varies from 7.2Ω to 36Ω.[4] IIP3 of the mixer switches is plotted versus R_{SW} for the two placements of R'_S in Fig. 2.7. Clearly, the IIP3 of mixer switches is significantly higher (more than 10dB higher for ON resistance equal to 7.2Ω) if the series resistor R'_S is placed before the mixer switch as compared to placing it after the mixer switch.

Analytical expressions to compare the linearity performance of the circuits in Fig. 2.6 are cumbersome. Hence, we resort to explaining the simulation results through approximate calculations which are more insightful. Consider the source node of the NMOS mixer switch shown in Fig. 2.6(a). The voltage swing at this virtual ground node is approximately given by equation (2.4). However for the circuit in Fig. 2.6(b), the source node swings by an amount approximately equal to

[4] R'_S is also swept to ensure that input match happens with the series combination of R'_S and R_{SW}, that is R'_S+R_{SW} is maintained constant.

$$v_{\text{mix,source}} = v_{in}\frac{R'_S + A_\gamma R_F}{2R_S} \approx \frac{v_{in}}{2} \tag{2.8}$$

The approximation in the second line is valid when the mixer switch resistance $R_{SW} \ll R_S$. Equation (2.8) tells us that the source node swings by an amount equal to $v_{in}/2$ for the circuit in Fig. 2.6(b). During the ON phase of the LO, the gate voltage V_G of the mixer switches is constant, equal to V_{DD}, except during the finite rise and fall times of the LO waveform. However, the source voltage swing is significantly lesser in case of the circuit in Fig. 2.6(a) than for the circuit in Fig. 2.6(b). Therefore, there is significantly smaller V_{GS} modulation of ON resistance of the mixer switches in Fig. 2.6(a). This reduction of V_{GS} modulation of ON resistance of mixer switches is very similar to the effect of bottom plate mixing demonstrated in [24]. If the source of the mixer switch were a perfect ground, the in-band IIP3 of the mixer switches may be derived similar to the derivation of out-of-band IIP3 in [40], and it can be shown that the IIP3 is proportional to

$$V_{IIP3,mix} \propto \rho^{-\frac{3}{2}} \qquad \rho = \frac{R_{SW}}{R_S + R'_S + R_{SW}} \tag{2.9}$$

However, as seen from the log scale plot of IIP3 versus R_{SW} in Fig. 2.7 (in case of optimal R'_S placement), the slope of IIP3 versus R_{SW} is less than 1.5. This could be because, while our architecture reduces the V_{GS} modulation to a large extent due to the virtual ground, it does not completely eliminate it.

Thus far, we have shown simulation results using a 25% duty-cycled non-overlapping square wave LO to illustrate the benefits of reduced V_{GS} modulation of ON resistance of mixer switches. However, it is extremely challenging to synthesize such a waveform at the desired frequency of operation (10−35GHz). A commonly used technique to drive the gate of the mixer switches at mm-wave frequencies is to use pseudo non-overlapping sinusoidal LO drive. However, with such a drive, while the source voltage of the mixer switch is held approximately a constant due to the virtual ground at the input of the baseband amplifier, the gate voltage varies throughout the ON phase of the LO. Therefore, there still exists V_{GS} modulation of ON resistance of mixer switches. Fig. 2.8 illustrates that the IIP3 and P1dB of the mixer switches drop significantly when driven by a sine wave LO (with same rail-rail swing), with a reduced slope for IIP3 versus R_{SW} as compared to the 25% non-overlapping square wave LO drive.

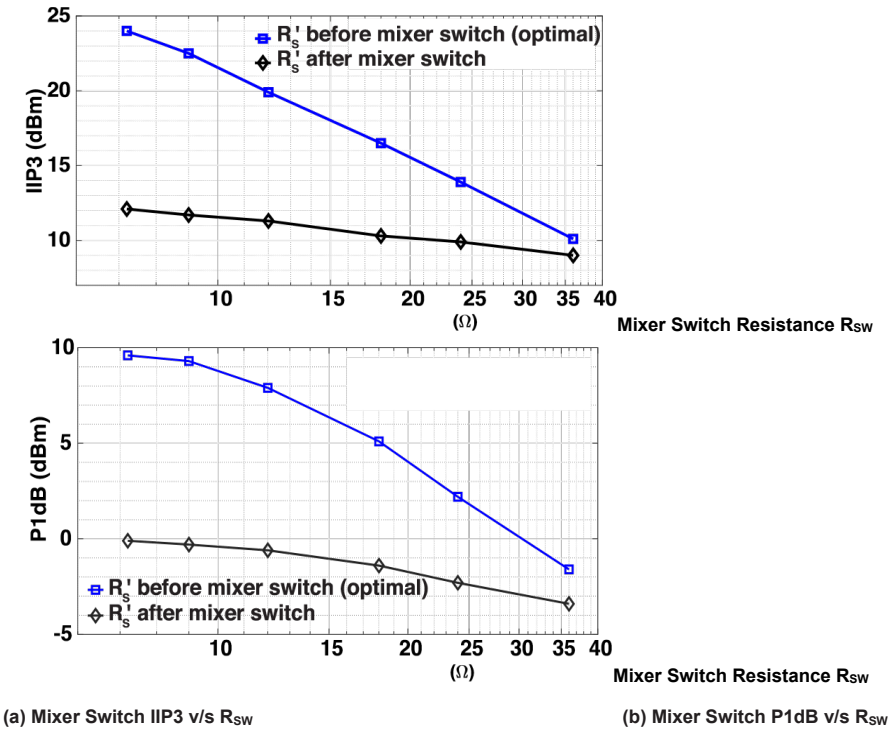

Figure 2.7: Simulated IIP3 and P1dB (f_{LO} = 20GHz) of mixer switches for the two circuits shown in Figs. 2.6(a) and (b). The series resistor is placed before and after the mixer switch, in the two cases. The baseband is assumed to be perfectly linear for this simulation.

While it may not be possible to synthesize a 25% duty-cycled non-overlapping LO waveform at mm-wave frequencies, it is definitely possible to synthesize 50% duty-cycled overlapping LO waveforms in the desired 10 − 35GHz band, in the 28nm bulk CMOS node used in this work. The charge sharing issues associated with an overlapping LO [2] are dealt with subsequently. Fig. 2.8 shows the IIP3 and P1dB of the mixer switch versus mixer switch ON resistance for different LO drives: 25% duty-cycled non-overlapping LO with 1ps rise and fall times, 50% duty-cycled overlapping LO with 1ps rise and fall times, 50% duty-cycled overlapping LO with 5ps rise and fall times, and finally a pseudo-non-overlapping sine-wave LO with the same peak swing. The IIP3 is approximately the same for 25% and 50% duty-cycled LO drive, with the same rise and fall times (1ps). Therefore, there is no linearity penalty for using a 50% duty-cycled LO compared to a more conventional 25% duty-cycled LO, which cannot be synthesized at these frequencies. As the rise and fall times of the LO waveform increase, the IIP3 starts reducing, as the V_{GS} modulation of ON resistance occurs for a larger fraction of the ON period. Therefore, it is desirable to make the transitions as sharp as possible, while designing the LO chain, to maximize IIP3.

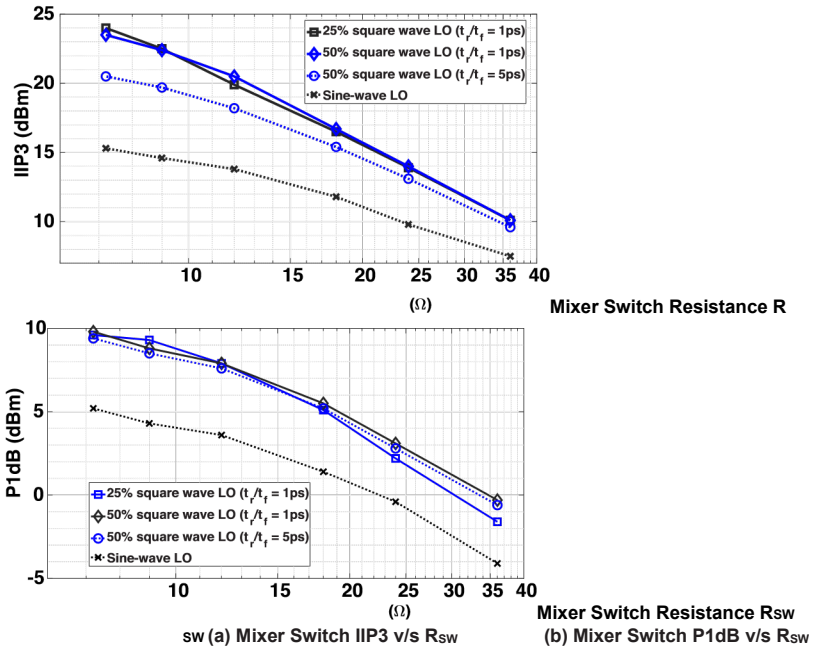

Figure 2.8: Simulated IIP3 and P1dB (f_{LO} = 20GHz) of mixer switches for the circuit shown in Fig. 2.6(a), for different LO drives. The different cases are 25% non-overlapping LO, 50% overlapping LO and pseudo non-overlapping sine wave drive. The LO swings from 0 to V_{DD} = 1.2V in each case. The baseband is assumed to be perfectly linear for this simulation.

Due to issues encountered with respect to convergence and the BSIM4 model discontinuities [43], the IIP3 was simulated using transient simulations with relatively high input powers (> −10dBm) as the discontinuity would form a smaller fraction of the waveform at higher power levels [43, 23]. For completeness, P1dB simulation results are also provided. The P1dB simulation results exhibit similar trends as the IIP3 simulations, re-affirming the various concepts discussed in this section.

2.2.2 Noise and Charge Sharing

To analyze the noise figure of the traditional and proposed circuit and understand the various tradeoffs, consider the LTI equivalent circuit shown of [40] in Fig. 2.9, which shows both the shunt re-radiation resistance R_{sh} and the overlap resistance R_{OL}. R_{OL} is used to capture the effects of charge-sharing due to LO overlap. While deriving this LTI model, [40] makes some assumptions on the leakage current during the overlap, which do not hold for this work. Like in [40], we assume that the voltages on the baseband capacitors are approximately constant throughout the LO overlap period. Unlike [40], the leakage current is also assumed to be constant for the entire duration of the overlap period while deriving the overlap resistance. In this case, the LO waveform is a 4-phase square wave with duty-cycle D. D varies between 0.25 and 0.5 depending on whether the the LO waveform is completely non-overlapping or has a quarter LO period overlap. The amount of LO overlap is given by

$$\tau_{OL} = T_{LO}\left(D - \frac{1}{4}\right) \tag{2.10}$$

The noise figure (without considering amplifier noise) is given by

$$F = 1 + \frac{R_{SW}}{R_S} + \frac{R'_S + R_{SW}}{R_S}\left(\frac{R_S + R'_S + R_{SW}}{R_{sh}}\right)^2 + \left(\frac{R_S + R'_S + R_{SW}}{R_{OL}}\right)^2 \tag{2.11}$$

$$R_{OL} = \frac{8}{\pi^2 - 8} R_S$$

$$R_{sh} = R_S + R'_S + R_{SW}$$

It can be derived that the overlap resistance R_{OL} is given by,

$$R^{OL} = \frac{8}{\pi}\frac{R_{path}}{\sqrt{4D-1}} \tag{2.12}$$

where R_{path} is the resistance per path of the N-path mixer. Equation (2.12) reduces to $R_{OL} = \infty$ for a 25% duty-cycled non-overlapping LO, which makes sense since the effect of LO overlap is not seen in the 25% duty-cycled non-overlapping LO.

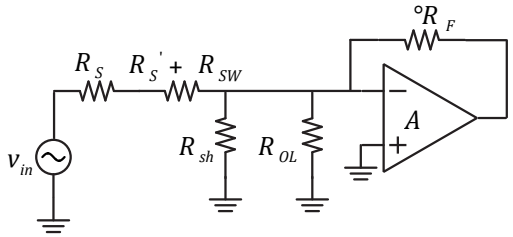

Figure 2.9: LTI equivalent circuit of the circuits in Figs. 2.2 and 2.11, showing shunt re-radiation resistance R_{sh} and overlap resistance R_{OL}. The values of R_{OL} are different for each of the circuits, depending on the nature of the LO driving the mixers.

First, the evolution of the architecture is illustrated using simulation results of actual extracted transistors (see Fig. 2.10). Then, some of the trade-offs are discussed using equations (2.11) and (2.12). Simulation results using ideal switches and resistors are used to validate some of the trends illustrated by the LTI model in Fig. 2.9. First consider the noise figure of the traditional N-path filter based architecture of Fig. 2.2 with $R_{SW} = 12\Omega$ (using transistors of dimension 27μm/30nm), driven by a 25% duty-cycled non-overlapping square wave LO ($R'_S = 0\Omega$ for the circuit in Fig. 2.2). The overlap resistance $R_{OL} = \infty\Omega$ for mixers driven by non-overlapping LO waveforms. A simulated DSB (double side-band) noise figure of $\sim$ 6.7dB is observed. The simulated noise figure includes contributions from the switch parasitics and the

baseband noise which are not included in equation (2.11). Now, consider the circuits of Figs. 2.11(a) and (b), where an explicit series resistor R'_S is added for input matching. First, let us consider the scenario where the circuits in Fig. 2.11 are driven by a 25% duty-cycled non-overlapping LO, as opposed to the 50% duty-cycled LO shown in the figure. The circuit in Fig. 2.11(a) has one common R'_S for all the four paths, whereas the circuit in Fig. 2.11(b) has one R'_S in each path. Simulations show an increase in NF of 3.1dB for the circuit in Fig. 2.11(a) compared to the circuit in Fig. 2.2. This increase is due to the noise contribution of resistor R'_S, as well as additional losses that arise at high frequency from the RC network created by R'_S and the switch parasitic capacitance. Neglecting switch parasitics, an equal increase in noise figure is expected for both circuits when driven by a non-overlapping 25% dutycycled LO. However, simulations show a further 0.3dB increase for the circuit in Fig. 2.11(b). This is due to the difference in the network formed by the series resistor R'_S and the parasitics in the two cases.

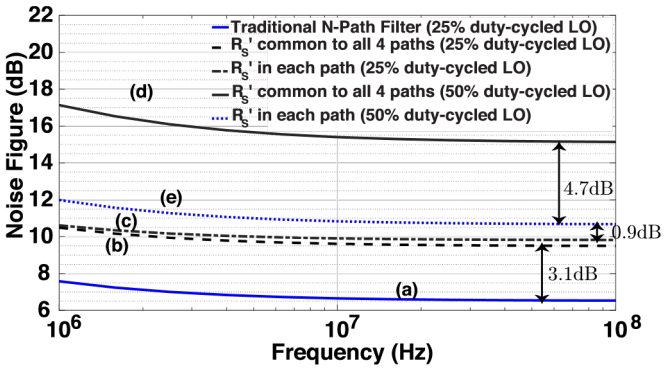

Figure 2.10: Simulated Noise Figure (f_{LO} = 20GHz)

For the following cases (a) The circuit in Fig. 2.2 driven by non-overlapping 25% duty-cycled LO(b) The circuit in Fig. 2.11(a) driven by nonoverlapping 25% duty-cycled LO. (c) The circuit in Fig. 2.11(b) driven by non-overlapping 25% duty-cycled LO. (d) The circuit in Fig. 2.11(a) driven by overlapping 50% duty-cycled LO. (e) The circuit in Fig. 2.11(b) driven by overlapping 50% duty-cycled LO.

As discussed previously, it is extremely challenging to generate a 4-phase 25% duty-cycled non-overlapping square wave LO, but it is possible to generate a 4-phase 50% duty-cycled overlapping square wave LO for the desired 10–35GHz frequency of operation. When the mixers are driven by the LO waveform thus generated, there is I/Q charge sharing, which degrades the noise figure [2].

The two circuits shown in Fig. 2.11(a) and (b) are indistinguishable when driven by a 25% duty-cycled non-overlapping LO, if the parasitics are neglected. However, when driven by a 50% duty-cycled overlapping LO, the noise figure of the circuit in Fig. 2.11(a) degrades by as much as 4.7dB (see Fig. 2.10) compared to 25% duty-cycled non-overlapping drive. By judiciously placing the explicit series termination resistance R'_S (see Fig. 2.11(b)), the degradation may be reduced from 4.7dB to just 0.9dB. This mitigation is due to the reduced overlap leakage current, which in turn leads to a reduction of the charge sharing effect. For the circuit in Fig. 2.11(a), the

overlap leakage current is proportional to $1/R_{SW}$, whereas for the circuit in Fig. 2.11(b), it is proportional to $1/(R_{SW}+R'_S)$.

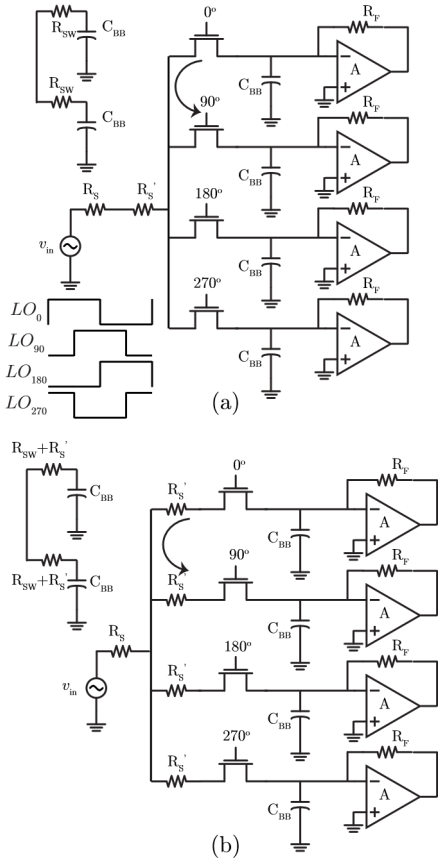

Figure 2.11: Charge Sharing Problem Due to LO Overlap When Driven by a 50% duty-cycled LO (a), (b) Mitigating Charge-sharing

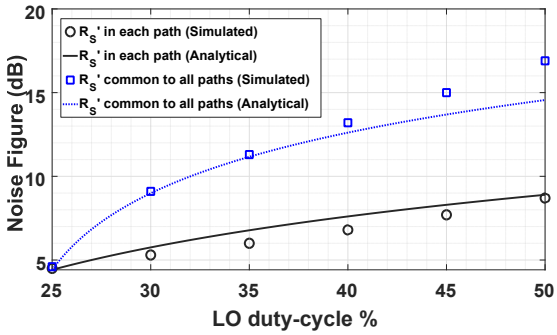

Figure 2.12: Simulated and Analytic Noise Figure of the Circuits in Figs. 2.11(a) and (b) Versus Duty Cycle of the 4-phase LO Waveform

For these simulations, the switch ON resistance is equal to 12Ω) and the explicit series resistance is equal to 50Ω). The switch parasitics are not included in this simulation.

Another way of looking at some of these results based on equations (2.11) and (2.12) and the results of [40] is by using overlap resistance R_{OL} to denote the charge-sharing losses. The expression for R_{OL} is given by equation (2.12). $R_{path} = R_{SW}$ for the circuit in Fig. 2.11(a) and increases to $R_{path} = R_{SW} + R'_S$ for the circuit in Fig. 2.11(b). Fig. 2.12 shows the plot of simulated noise figure versus duty-cycle for a fixed value of switch ON resistance and explicit series resistance for the circuits in Figs. 2.11(a) and (b). It shows the benefit of having a series resistance in each path as opposed to having one series resistor common to all four paths. Clearly, for a series resistance in each path, the R_{path} is higher, and consequently, the overlap resistance R_{OL} is higher, reducing overlap losses. The trends regarding overlap losses, illustrated by the analysis in equations (2.11) and (2.12), are verified by the simulation results (Fig. 2.12).

For a 25% duty-cycled non-overlapping LO, $R_{OL} = \infty$. Therefore, the noise figure increases with increasing R'_S as given by equation (2.11) and the results of [4]. However, with overlapping LO drive, there exists an optimum value of $R'_S + R_{SW}$ in terms of noise figure. Increasing series resistance increases the noise contribution from R'_S, but also increases R_{OL}, thereby decreasing the noise contribution due to the overlap. This is observed from the simulation plots in Fig. 2.13, where ideal switches (with an appropriate ON resistance), but no C_{par} were used. The existence of an optimum $R'_S + R_{SW}$ for noise is similar to the existence of an optimal switch resistance in conventional N-path mixers with narrow-band input matching networks [4].

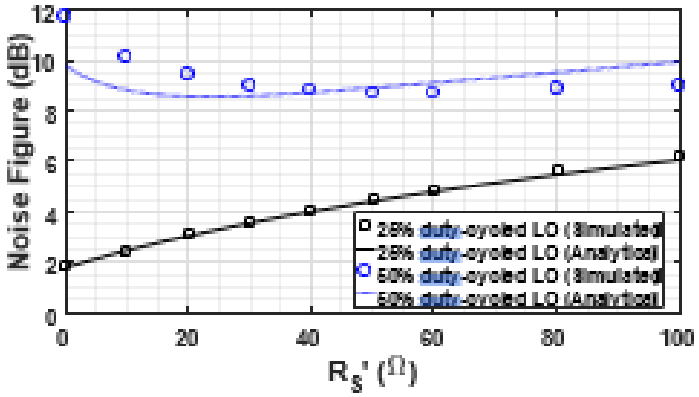

Figure 2.13: Simulated and Analytic Noise Figure of the Circuit in Fig. 2.11
(b) versus series termination resistance R'_S for different cases of LO drive. For these simulations, an ideal switch with ON resistance equal to 12Ω is used. The switch parasitics are not included in this simulation.

This reduction of charge sharing due to LO overlap is quite similar to the technique with series inductors proposed in [2]. However, the technique proposed in this work has a frequency invariant R'_S and occupies less area due to the use of an explicit resistance rather than an inductor as in [2].

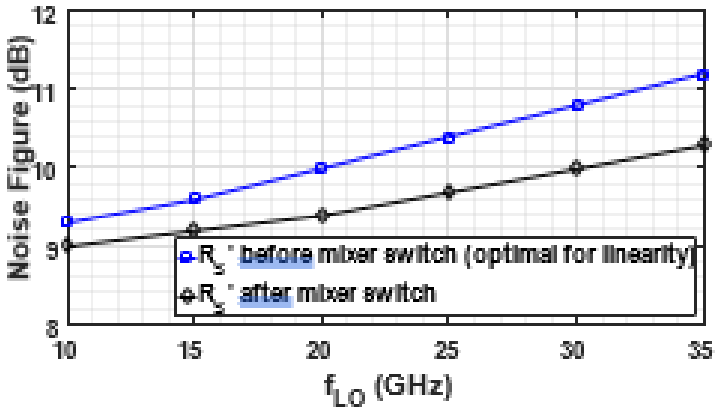

Figure 2.14: This plot compares the simulated noise figure v/s f_{LO} for two different placements of the series termination resistance R'_S with respect to the mixer switch (Figs. 2.6 (a) and (b)). For these simulations, an ideal switch with ON resistance equal to 12Ω is used. Switch parasitics of 30fF per switch are included in this simulation.

In Section 2.2B on mixer-switch linearity, it was seen that placing the explicit series resistance before the mixer switch was optimal for linearity (Fig. 2.6(a)). However, the RC network formed between the series resistor and the mixer switch parasitics lead to worse noise figure for the circuit in Fig. 2.6(a) compared to the one in Fig. 2.6(b). This is illustrated by the simulation plot of Fig.2.14, where switches with appropriate ON resistance and switch parasitics were used.

2.2.3 Effects of LO Overlap on Baseband Non-Linearity

In the previous section, we discussed the issue of gain and noise figure degradation due to charge sharing arising out of LO overlap, and solutions to mitigate the same. In a similar vein, LO overlap also degrades the baseband non-linearity due to leakage between the I and Q channels [26], due to lack of reverse isolation in the mixer. Fig. 2.15 plots the simulated OIP3 of the two circuits in Figs. 2.11 (a) and (b) versus the duty-cycle of the LO drive, for a value of feedback resistance R_F = 1kΩ.[5] 25% duty-cycle implies zero LO overlap. The extent of LO overlap becomes higher with larger duty-cycle. To illustrate the effect of LO overlap on baseband non-linearity alone, ideal mixer switches are used in the simulation. Clearly, the LO overlap leads to a significant degradation in baseband non-linearity (more than 8dB degradation from 25% duty-cycle to 50% duty-cycle) for the circuit in Fig. 2.11(a), where R'_S is common to all four paths. The technique used for mitigation of charge-sharing also mitigates the baseband non-linearity degradation since the explicit series resistance improves the reverse isolation. For the circuit in Fig. 2.11(b), where R'_S is placed in each of the four paths, the degradation in baseband non-linearity is reduced significantly (see Fig. 2.15).

[5] Note the OIP3 is plotted instead of the IIP3 to normalize for the front-end losses which arise due to charge sharing.

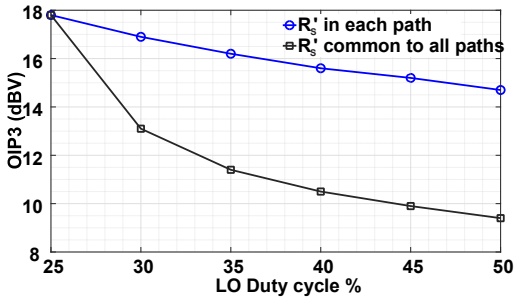

Figure 2.15: Degradation of baseband non-linearity due to LO overlap for the circuits in Figs. 2.11(a) and (b). The model used for the baseband amplifiers is the same as the one used for the simulation plot in Fig. 2.5, and is derived from the actual transistor implementation of the amplifier used in this work. The OIP3 is shown for R_F = 1kΩ. In each case, an ideal mixer of switch ON resistance equal to 5Ω is placed in each of the four paths.

2.2.4 Input Matching Network

The parasitic capacitance of the mixer switches, bonding pad and ESD diodes degrade the noise figure [29], with greater degradation at higher frequencies. In this section, we discuss the input matching network to mitigate this degradation. Assuming that the mixer switch resistance R_{SW}, series resistance R'_S and the baseband resistance have been chosen appropriately to match to the input resistance R_S, Fig. 2.16 gives an approximate representation of the input matching network. The noise figure simulations thus far have included the effect of C_{par}, the parasitic capacitance (~ 110fF) of the mixer switches. Fig. 2.17 shows the insertion loss of the input matching network with C_{par} alone, and also with the capacitance of the probe pad (C_{PAD}) and the ESD diodes (C_{ESD}), in addition to C_{par}. C_{PAD} = 40fF and C_{ESD} = 120fF cause a further degradation in the insertion losses, which are reflected in the 1.7dB degradation in noise figure at f_{LO}=20GHz (see Fig. 2.18). To mitigate the losses due to C_{PAD} and C_{ESD}, a matching network using an artificial 50Ω transmission line may be created by inserting L_{match} between the pad and mixer. Obviously, this is a second order transfer function with a steep roll-off beyond the 3-dB bandwidth. Therefore, while it minimizes the insertion losses up to ~ 38GHz compared to not having L_{match}, the losses are worse at higher frequencies (see Fig. 2.17). This improvement is also reflected in the improved noise figure at f_{LO}=20GHz (see Fig. 2.18).

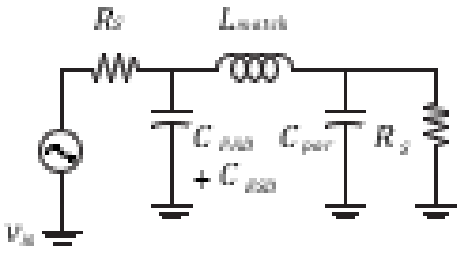

Figure 2.16: Schematic of the Input Matching Network

The matching network includes pad and ESD capacitance and an additional inductor L-match added to reduce front-end loss, by forming a π-section T-line.

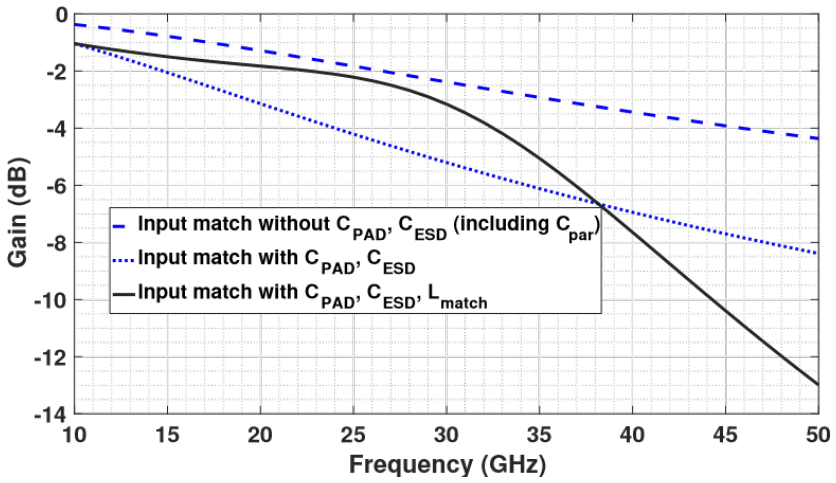

Figure 2.17: Input Matching Network Losses

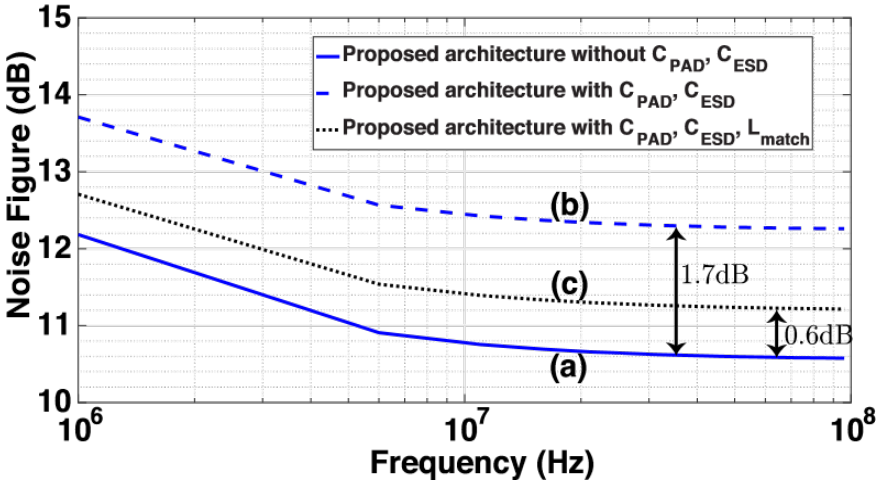

Figure 2.18: Simulated Noise Figure at f_{LO} = 20GHz (a) with only C_{par} (b) with C_{par}, C_{PAD}, C_{ESD} (c) with Entire Input Matching Network Including L_{match}.

2.2.5 LO generation

The LO chain shown in Fig. 2.19 is used to generate the four-phase 50% duty-cycled overlapping LO required to drive the mixer switches. A single-ended off-chip LO input (nominally 0dBm) is converted to a differential signal using an on-chip balun. To compensate for the losses of the balun and the transmission line routing, an inverter based buffer is used.[6] A lumped implementation of a differential quadrature hybrid [12, 13] is used to generate the I/Q signals. In the differential quadrature hybrid implementation shown in Fig. 2.19, most of the capacitance comes from the parasitic capacitance of the inductors and the buffers before and after the quadrature hybrid. The quadrature hybrid is followed by an inverter chain to ensure rail-to-rail LO swing at the mixer gate input. To ensure low quadrature phase error across the entire

[6] Note that this buffer may not be necessary if the LO input power is higher or if a differential on-chip local oscillator with sufficient output swing is used to synthesize the LO.

bandwidth of interest, a small tunable capacitor bank is implemented. While this helps correct for phase error at different frequencies, there exists an amplitude mismatch between the four differential I/Q signals as seen from the small signal gain from the input to the four different LO outputs (see Fig. 2.20). However, our target is to have square wave LO drive for the mixer switches. The gain of the entire LO chain to all four I/Q mixer gates is high enough in the 10–35GHz frequency range to ensure that the LO swing "rails out" for a 0dBm input LO power, ensuring square wave drive. Fig. 2.21 shows the simulated amplitude imbalance and phase difference between the differential I and Q outputs for the small signal conversion gain from the RF input to the baseband output. For each f_{LO}, the capacitor bank of the quadrature hybrid was suitably adjusted to ensure phase difference as close to 90° as possible. With suitable settings, it is observed that the simulated I/Q phase error is less than ±1° across 10–35GHz and the amplitude imbalance is less than 0.15dB.

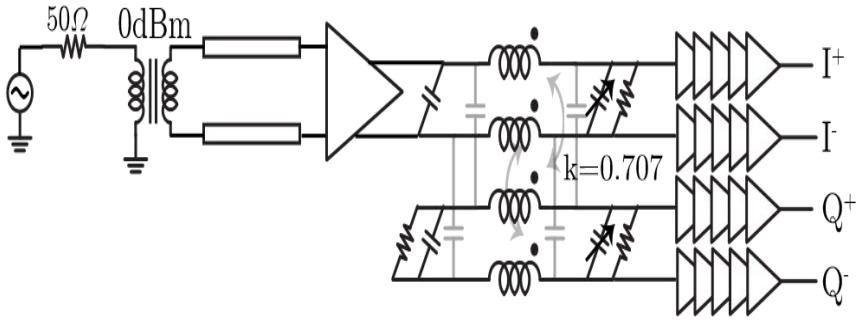

Figure 2.19: Schematic of LO Chain

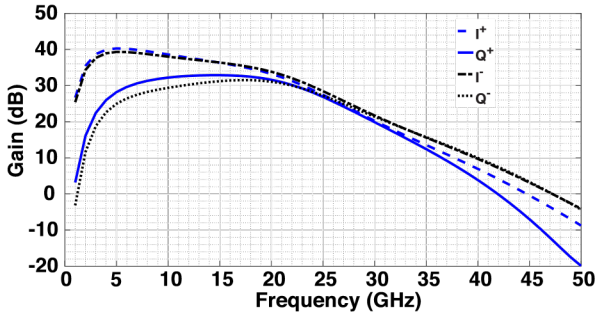

Figure 2.20: Simulated Small Signal Gain of the LO Chain from LO Input to the Four Gates of the I/Q Mixer Switches

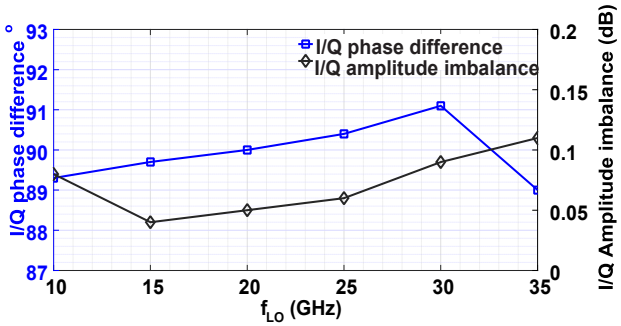

Figure 2.21: Simulated I/Q Amplitude and Phase Imbalance for Differential Baseband Outputs

2.3 Measurement Results

A test chip was fabricated in a 28nm bulk CMOS process and wire-bonded directly onto PCB (see Fig. 2.23). The RF and LO inputs were probed using GSG probes. A detailed schematic of the fabricated chip and the test setup is shown in Fig. 2.22.

The feedback resistance R_F in Fig. 2.11 is programmable, so that the chip may be used over a wide range of gain and linearity settings. Fig. 2.24 shows the measured voltage conversion gain and input matching for f_{LO} varying from 15GHz to 30GHz in steps of 5GHz, for a setting of R_F = 1kΩ. An RF bandwidth of 400MHz was achieved for this gain setting. The s_{11} is less than −10dB across f_{LO}, and is largely flat across frequency due to the use of an explicit series resistor R'_S for matching.

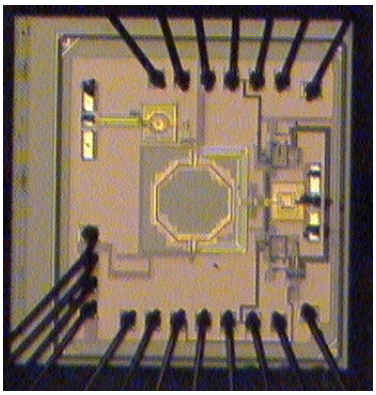

Figure 2.23: Die Micrograph of 28nm Bulk CMOS Prototype of Receiver Front-end

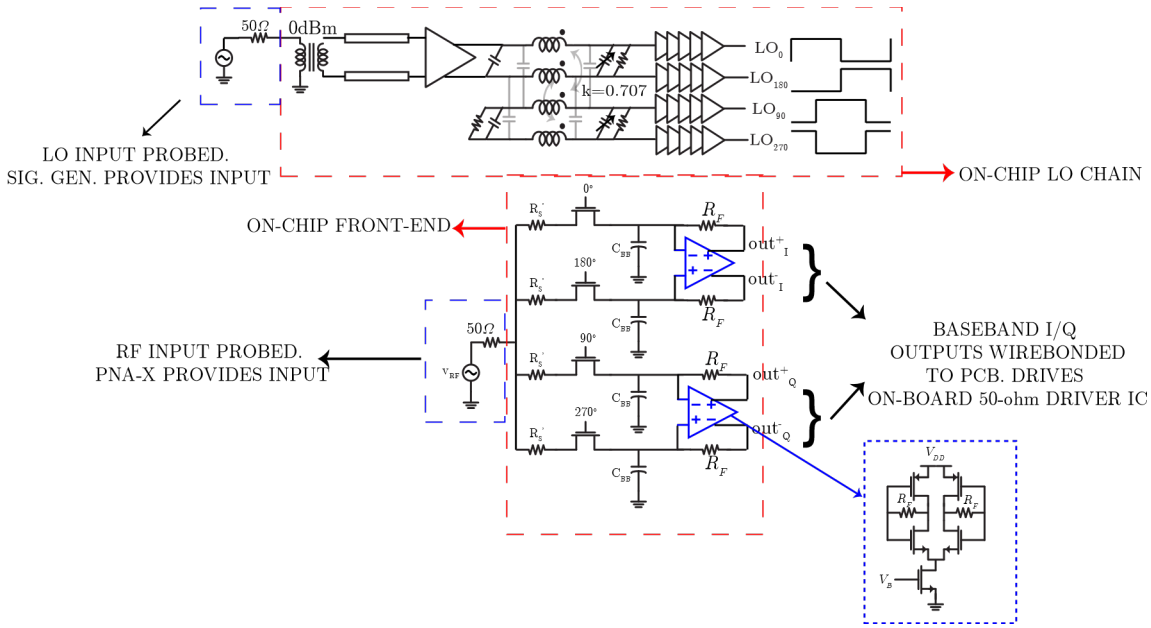

Figure 2.22: Block diagram Summarizing the Entire Receiver Front-end and the LO Chain

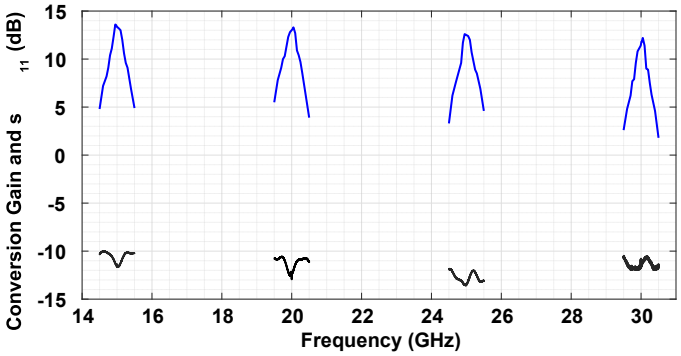

Figure 2.24: Measured conversion gain and input match for R_F = 1kΩ versus frequency for four different f_{LO}

Figure 2.25: Measured and simulated gain versus f_{LO} for R_F = 1kΩ and R_F = 2kΩ.

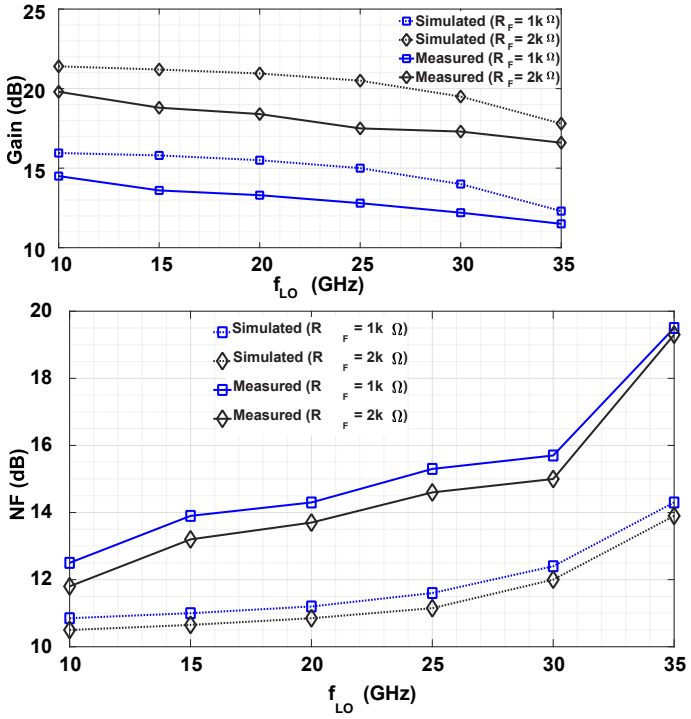

Figure 2.26: Measured and Simulated Noise Figure Versus f_{LO} for R_F = 1kΩ and R_F = 2kΩ

Fig. 2.25 and Fig. 2.26 show the measured conversion gain and noise figure for f_{LO} varying from 10–35GHz, for two different settings of feedback resistance R_F, 1kΩ and 2kΩ. As expected, conversion gain for R_F = 2kΩ is around 5dB higher than that for R_F = 1kΩ, and drops with f_{LO}. The increased conversion gain at R_F = 2kΩ comes at the cost of RF bandwidth reducing from 400MHz to 240MHz. Also, there is a discrepancy of >1.5dB between the simulated and measured conversion gain, which may be explained by probe losses and underestimation of input parasitic capacitance. For the higher linearity setting of R_F equal to 1kΩ, a NF of 12.5 to 15.7dB was measured for f_{LO} varying from 10–30GHz. The noise figure is lower by about 0.4dB for R_F = 2kΩ. The simulated NF for R_F = 1kΩ varies from 10.8 to 14.3dB for f_{LO} varying from 10–35GHz. The discrepancy of >1.5dB may be explained by probe losses and inaccurate noise models. The steep jump in measured noise figure from 30 to 35GHz may be attributed to higher parasitic capacitance. Fig. 2.17 shows the input matching network loss as a function of frequency, and the higher order transfer function of the input matching network leads to a steeper roll-off with frequency. For higher parasitics than simulation, the roll-off starts at a lower frequency, explaining the bigger discrepancy between simulated and measured noise figure at f_{LO} = 35GHz.

A 2-tone test was performed to characterize the IIP3 of the receiver front-end (for R_F = 1kΩ), with one tone at f_{LO} + f_{OS} + 40MHz and another tone at f_{LO} + 2f_{OS} + 40MHz, with the IM3 tone falling at f_{LO} +40MHz. Fig. 2.27 plots the IIP3 as a function of tone offset. In traditional

mixer-first receivers, which are used to enhance out-of-band RF selectivity, the IIP3 increases considerably for tones at higher offset from f_{LO} [20]. However, in this case, the IIP3 is almost constant for f_{OS} within the baseband bandwidth (that is, for in-band blockers), due to the use of an explicit resistor for matching. There is a slight drop for f_{OS} outside the band, which may be explained by the reduction of loop gain in the baseband amplifier, and hence reduced benefits of feedback linearization. IIP3 numbers as high as +14dBm show that we have indeed derived benefit both from feedback linearization and the improved mixer switch linearity.

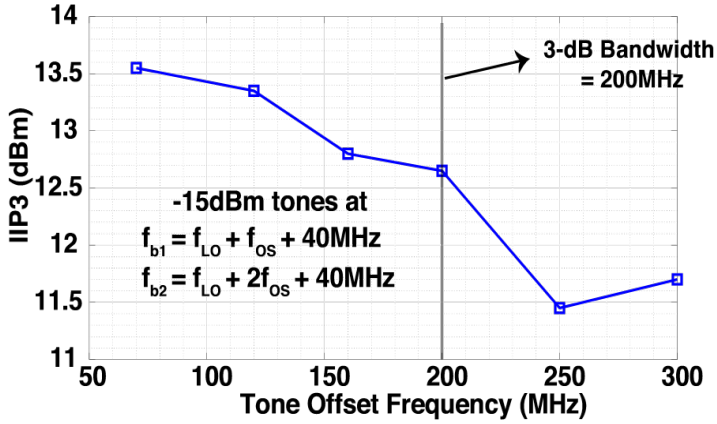

Figure 2.27: Measured IIP3 as a Function of Tone Offset for f_{LO} = 20GHz for R_F = 1kΩ

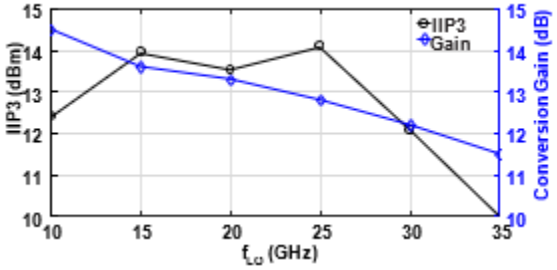

Figure 2.28: Measured Conversion Gain and In-band IIP3 Versus f_{LO} for R_F = 1kΩ

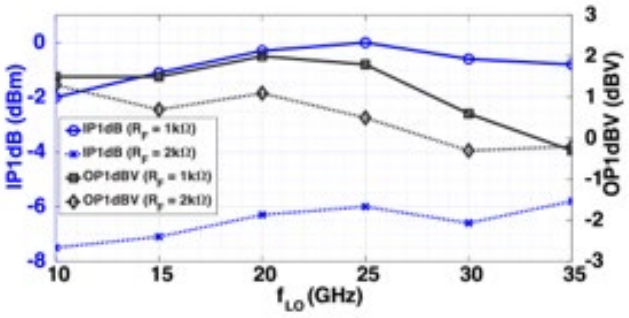

Figure 2.29: Measured IP1dB and OP1dBV Versus f_{LO} for R_F = 1kΩ and R_F = 2kΩ

Fig. 2.28 shows the conversion gain and in-band IIP3 across f_{LO} for R_F = 1kΩ. The inband IIP3 is largely flat up to f_{LO} = 30GHz, varying between +12dBm and +14dBm. The drop to +10dBm at 35GHz is likely due to less "square" LO drive, and hence reduce mixer linearity. Figs. 2.29 and 2.30 show P1dB measurements. Measured input P1dB and output OP1dBV are plotted versus f_{LO} for R_F equal to 1kΩ and 2kΩ in Fig. 2.29. The higher OP1dBV for R_F equal to 1kΩ (lower closed loop gain) illustrates the benefit of feedback linearization and shows that we are not just giving up closed loop gain for P1dB dB for dB. Fig. 2.31 illustrates the trade-offs between P1dB, gain and NF as the feedback resistance R_F is changed. The benefit of feedback linearization may be inferred from the following observations. In Fig. 2.31, when R_F is reduced from 9kΩ to 5.4kΩ, the gain drops by less than 3dB, but the P1dB increases by more than 4dB. The increase in P1dB by a factor approximately 1.5× the gain shows that we are benefitting from feedback linearization. Additionally, while R_F is reduced from 15kΩ to 667Ω, the gain drops by around 20dB, while the P1dB increases by 26dB. It may be noted from the plot that for R_F as low as 667Ω, the P1dB (+3dBm) continues to increase without trailing off. This shows that the mixer P1dB is higher than +3dBm, validating our techniques to increase mixer switch linearity. Of course, the noise figure does increase with reducing R_F, but the penalty is quite low up to values of R_F equal to 1kΩ, as R_F is not the dominant noise source.

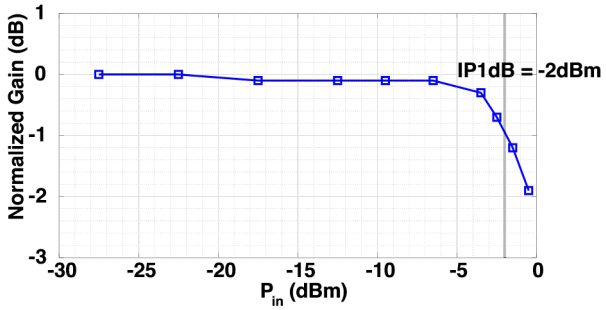

Figure 2.30: Normalized Measured Gain Versus Input Power P_{in} for R_F = 1kΩ at f_{LO} = 10GHz

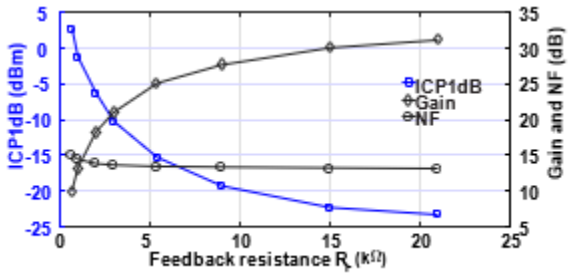

Figure 2.31: Trade-off between P1dB, Gain and NF versus Feedback Resistance R_F. (Measured)

2.4 Conclusion

Table 2.1 compares this work against the state-of-the-art mixer-first receivers operating at greater than 10GHz. While the modest noise figure of our receiver was a choice based on utilization in massive digital MIMO arrays, it may be seen that the IP1dB of 0dBm is an order of magnitude better than the next best receiver. While most previously publications do not directly report IIP3, +14dBm of in-band IIP3 is achieved in this work and is 16dB higher than the state-of-the-art. Also, the OP1dBV is significantly better than the state-of-the-art mixer-first receivers operating at greater than 10GHz. Finally, the broadband operation from 10–35GHz is among the highest fractional bandwidth reported in mm-wave mixer-first receivers.

Table 2.2 compares this work against other works intended for the 28GHz band. Most of the work in Table 2.2 have LNA front-ends, and are RF-phase-shifter-based systems. Therefore, while they do achieve considerably lower noise figure, they are not capable of broadband operation. Also, [41, 17, 27] have significantly lower linearity due to the use of vector interpolator based active phase shifters. [34], which uses transmission line based passive phase shifters, also shows lower linearity. The receiver front-end presented in this work could also be re-purposed for use in smaller sized phase arrays, in which case an LNA-based front-end is required. To illustrate this point, we consider the LNA from [27] driving the passive-mixer front-end described in this work. The LNA in [27] had a post-layout simulated gain of 25dB, noise figure of 3.6dB and ICP1dB of -3.2dBm at 28GHz. The last column of Table 2.2 shows the calculated performance specifications of the aforementioned LNA driving the front-end proposed in this work. The competitive performance metrics of such a front-end indicate that our work is suitable for use in an LNA-based front-end for arrays with lower number of elements.

To summarize, this work demonstrates a wideband highly linear mixer-first receiver front-end for massive digital arrays. As the array relaxes the noise requirement, feedback linearizaton at baseband was proposed to enhance linearity at the cost of noise. The limitations of feedback linearization were also highlighted. Techniques were proposed to enhance the linearity of mixer switches at mm-wave frequencies using overlapping square wave drive, and solutions were proposed to address the issue of charge sharing arising from the use of the same.

Table 2.1: Comparison with Mixer-first Receivers Greater Than 10GHz

	Moroni [28] RFIC 2012	Wilson [39] RFIC 2016	Ying [42] ESSCIRC 2017	Iotti [13] JSSC2020	Boynton [8] RFIC2020	Ahmed [1] CICC2020	This work
Technology	65nm CMOS	45nm SOI	130nm HBT	28nm CMOS	65nm CMOS	22nm FD-SOI	28nm CMOS
f_{RF} (GHz)	49 – 67	20–30	0.3 – 12	70 – 100	9 – 31	43 – 97	10 – 35
Voltage gain (dB)	13	8 – 20.6	3 – 5	19.5 – 25.3	45	12 – 15	10 – 31 (20GHz)*; 11.5 – 14.5 †
IP1dB (dBm)	-12	-9.3 – -13	-20 – -40	-16.8 – -24	-45	-5.6 – -8	-2 – 0 †
Best case OP1dBV	-10	-3.4	-26	-8.3	-11	-4	1.5
In-band IIP3 (dBm)	-	-2.3 – -9.7	-	-	-	0 – +4	+10 – +14.1 †
NF (dB)	11–14	8	10	8 – 12.7	12.5 – 17.5	12.5 – 16.5	12.5 – 19.2 #
DC power (mW)	14	41 (at 24GHz)	1200 – 1300	12	72	36	22.8 (Baseband); 19 – 37 (LO)
Supply (V)	1.2	0.9/1.8	-	1	-	-	1.2

* Measured gain at 20GHz across different gain settings.

† Measurements reported at nominal setting (R_F = 1kΩ), across f_{LO}.

NF varies from 12.5 – 15.7 dB for f_{LO} = 10−30GHz.

Table 2.2: Comparison with Recently Published 28GHz Receiver Front-ends

	Yeh [41] RFIC 2016	Kibaroglu [17] RFIC 2017	Mondal [27] JSSC2019	Sadhu [34] JSSC2017	This work	This work with LNA front-end (calculated)
Technology	120nm SiGe	180nm SiGe	65nm CMOS	130nm SiGe	28nm CMOS	28nm CMOS
f_{RF} (GHz)	28-32	28-32	28/37	28	10 – 35	28
Voltage gain (dB)	9.4	20	33/26.5	34	11.5 – 14.5	37.5
IP1dB (dBm)	-16 – -13	-22	-30/-24	-22.5	-2 – 0	-25.5
Best case OP1dBV (dBV)	-14.6	-13	-8	-1.3	1.5	-3
NF (dB)	5.1	4.6	7.3	6	12.5 – 19.2#	3.8
DC power (mW)	136.5	130	52.5	103.1	22.8 (Baseband); 19 – 37 (LO)	66

#NF varies from 12.5 – 15.7 dB for f_{LO} = 10−30GHz.

3 WIDEBAND LINEAR RECEIVER

3.1 Wilkinson Divider in Mixer-First Receivers

This chapter explores the use of Wilkinson Dividers in mixer-first receivers. Two designs are analyzed, simulated, and compared to the linear receiver proposed in the previous chapter and in [19]. Interestingly, we find that we can hold the performance of the receiver constant with respect to conversion gain and linearity while improving the noise figure considerably, to below 8 dB across the frequency band from 25 GHz to 40 GHz.

3.1.1 Wilkinson Divider

Figure 3.1 shows the schematic of a Wilkinson divider. Wilkinson dividers are used as either power combiners or power dividers. They have the benefit of isolating $Port_2$ and $Port_3$ while providing impedance matching between $Port_1$ and the other two ports. The two quarter-wavelength transmission lines provide input matching and help with the isolation between $Port_2$ and $Port_3$.

Traditionally, the characteristic impedance of the transmission line is chosen to be 50Ω with

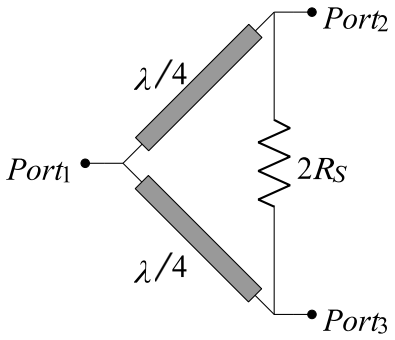

Figure 3.1: Wilkinson Divider

50Ω resistors at all ports. But since a quarter-wavelength transmission line can be used as an impedance transformer, the characteristic impedance of the lines can be changed to achieve matching with load resistors that are not equal to 50Ω. When used as a power divider, $Port_2$ and $Port_3$, which are the output ports, are isolated by current cancellation. This can be shown by calculating S_{23}. S_{23} can be calculated by applying a signal at $Port_2$ and using even and odd mode circuit equivalent to calculate the total current flowing through the load resistor at $Port_3$. The current through the bridge resistor will be 180 degrees out of phase with the current through the transmission lines. This means that no current will flow through the load resistor at $Port_3$. In order for the two output ports to be isolated, the bridge resistor value has to be equal to $2R_{sw}$.

3.1.2 Wilkinson Divider in Mixer-first Receivers

In the previous design, matching was achieved using a 50Ω physical resistor which added a 3dB penalty to the noise figure. In an effort to improve the noise figure of the receiver, this design proposes eliminating the 50Ω physical resistor and using a Wilkinson divider between the antenna and the mixers. Instead of a 50Ω resistor, the on-resistance of the mixers can be used for matching. And with the help of the quarter-wavelength transmission line, a small on-resistance of the mixer can be transformed to a larger value to match the antenna. In theory, the addition of a Wilkinson divider will provide isolation between the I and the Q paths of the receiver, which are $Port_2$ and $Port_3$ of the Wilkinson Divider. This means that that the charge sharing current that is caused by the overlapping LO waveform will be reduced. This design uses feedback linearization proposed in the previous section to mitigate the effect of the baseband distortion on receiver's overall linearity.

3.1.3 Input Matching

The impedance matching can be achieved by choosing the width of the transmission line such that its characteristic impedance is

$$Z_0 = \sqrt{2R_{sw}R_S} \tag{3.1}$$

This makes the impedance looking into one transmission line equal to

$$R_{sw} \quad Z_{Tline1} = \frac{Z_0^2}{R_{sw}} = \frac{2R_{sw}R_S}{R_{sw}} = 2R_S \tag{3.2}$$

and the input impedance looking into the receiver is

$$Z_{in} = 2R_S \| 2R_S = R_S \tag{3.3}$$

.

Figure 3.3 shows the difference between the simulated noise figure of proposed receiver compared to the design with 50Ω physical resistors. The design is simulated using ideal transmission lines from rfTlinelib library. The width of the line is found using an online calculator to achieve 270 matching to R_{SW} = 12Ω. The transmission line length is 1.8mm which is equal to equal to $\lambda/4$ at 20GHz. The baseband amplifier is an ideal differential amplifier with an open loop gain of 60dB, input capacitors at the input of the baseband amplifier, and a feedback resistor of 1kΩ. Ideal switches are used for the switches with an on-resistance of 12Ω. There's a 2.4dB improvement at 20GHz. The noise figure gets worse as operating frequency moves away from 20GHz shifts since the input matching would not be achieved at other frequencies.

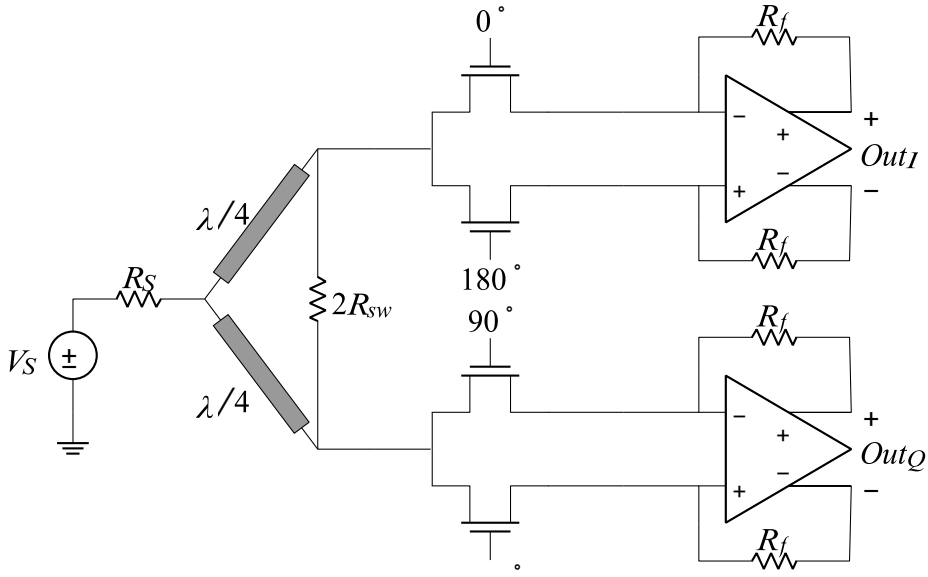

Figure 3.2: Mixer-first Receiver with Wilkinson Divider

3.1.4 Limitations

Using a Wilkinson Divider makes the design narrowband. The isolation between the two output ports is only valid for a single frequency, which is the frequency where the length of the transmission line is a quarter wavelength. Wideband designs of Wilkinson divider employing the use of tapered transmission lines can be used, but the use of a wideband Wilkinson divider will increase the charge sharing current and will degrade the noise figure of the receiver.

The narrow-banded nature of the Wilkinson divider is not only related to the input matching, it's also related to the isolation between the two output ports, $Port_2$ and $Port_3$. The two ports are only completely isolated if the signal applied at either $Port_2$ or $Port_3$ is at the same frequency. Since the use of the Wilkinson divider in this design is to prevent the charge sharing current from getting to the adjacent path, it would not be as effective. The charge sharing current is the result of the capacitor at the baseband input discharging and charging up the capacitor at the other baseband input. This means that the current sharing current is not a single tone and will not be fully suppressed by the Wilkinson Divider. The bridge resistor is providing more of a leakage path for the charge sharing current. The noise of the bridge resistor is also adding to the noise of the receiver.

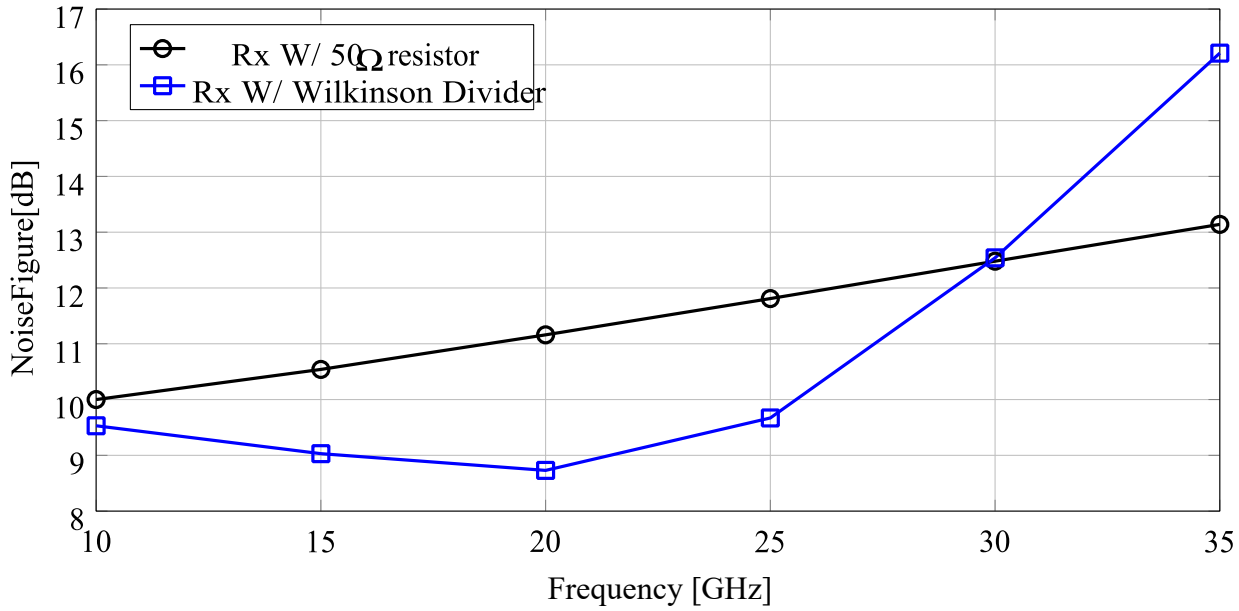

Figure 3.3: Noise Figure of a Receiver with a 50Ω Resistor and a Receiver with a Wilkinson Divider Designed for 20GHz with R_{sw} = 12Ω

3.1.5 Mixer-First Receiver with Modified Wilkinson Divider

The second proposed design uses a modified version of a Wilkinson divider between the antenna and the mixers. Common-mode analysis shows that the bridge resistor doesn't help with input matching since the bridge is an open in common-mode. The main purpose of the resistor is to provide isolation between the $Port_2$ and $Port_3$. The analysis above showed that the bridge resistor doesn't help with suppressing the charge sharing current, and it might be increasing the charge sharing between the I and the Q paths and impacting the noise figure. Hence, the bridge resistor can be omitted from the design. The rest of the design is not changed from the previous architecture. The quarter-wavelength transmission lines are still used to transform the on-resistance of mixers to 50Ω. Similar to the previous architecture, the on-resistance of the mixers is used for matching with the quarter-wavelength transformer included. This design uses feedback linearization proposed in the previous section to mitigate the effect of the baseband distortion on receiver's overall linearity.

The simulation setup is similar to setup of the simulation with the full Wilkinson Divider. The only difference is that the bridge resistor is removed from the schematics. Figure 3.5 shows the results of the simulated design. There is a 4.7dB improvement in the noise figure compared to the 270 previous design at 20GHz. The figure also shows the simulated noise figure values for mixer-first receiver with a transmission line designed for 30GHZ with a 6.1dB improvement in noise figure. The higher frequency means a shorter length for the $\lambda/4$ transmission lines, less loss in the signal path, and an improved noise figure.

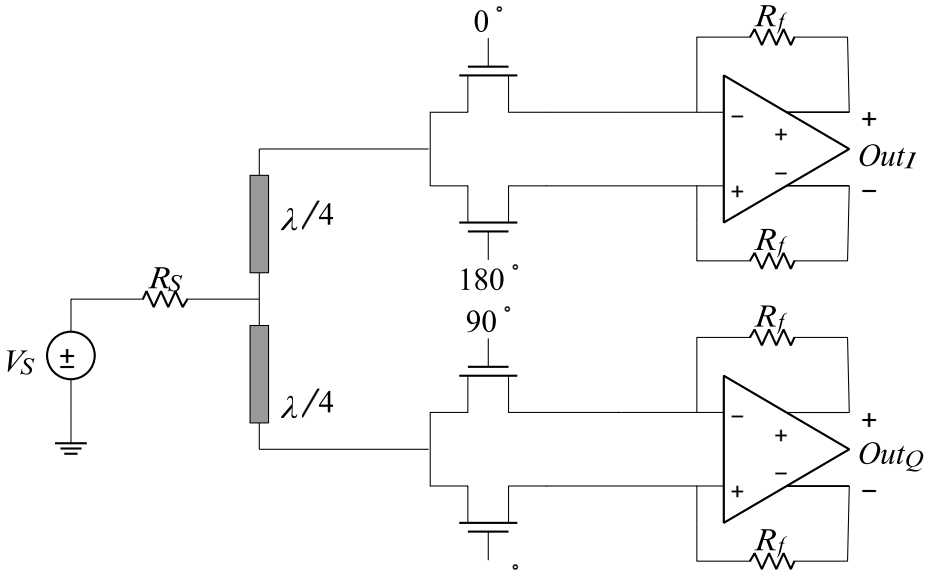

Figure 3.4: Mixer-first Receiver with a Modified Wilkinson Divider

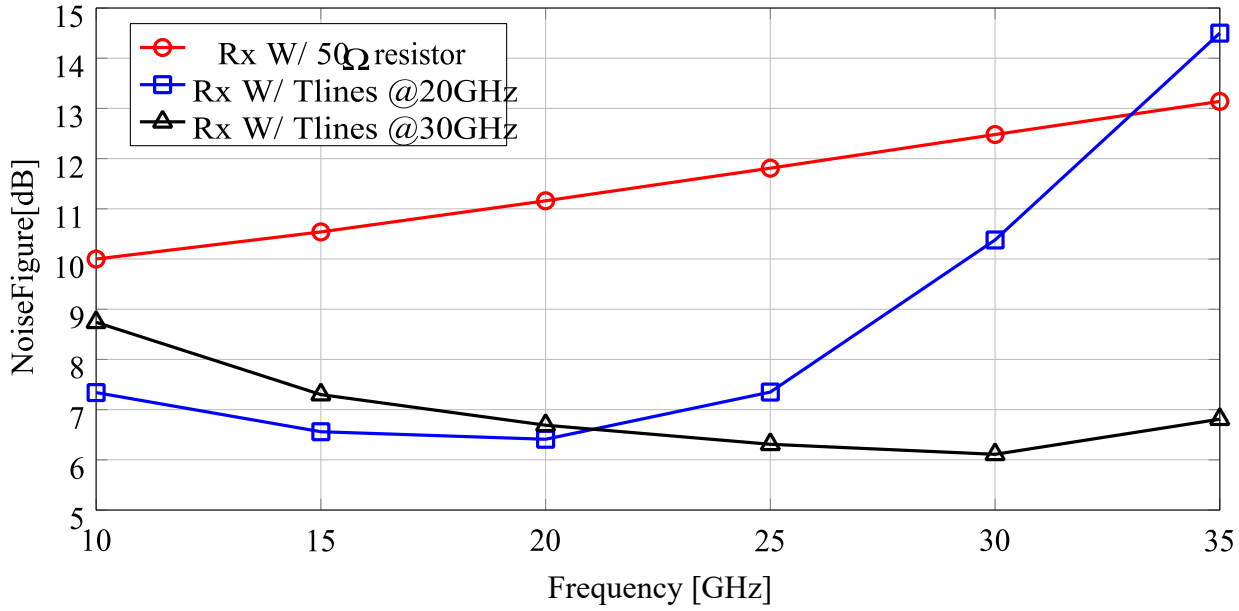

Figure 3.5: Noise Figure of a Receiver with a 50Ω Resistor, Receivers with a$\lambda/4$ Transmission Lines Designed for 20GHz and 30GHz

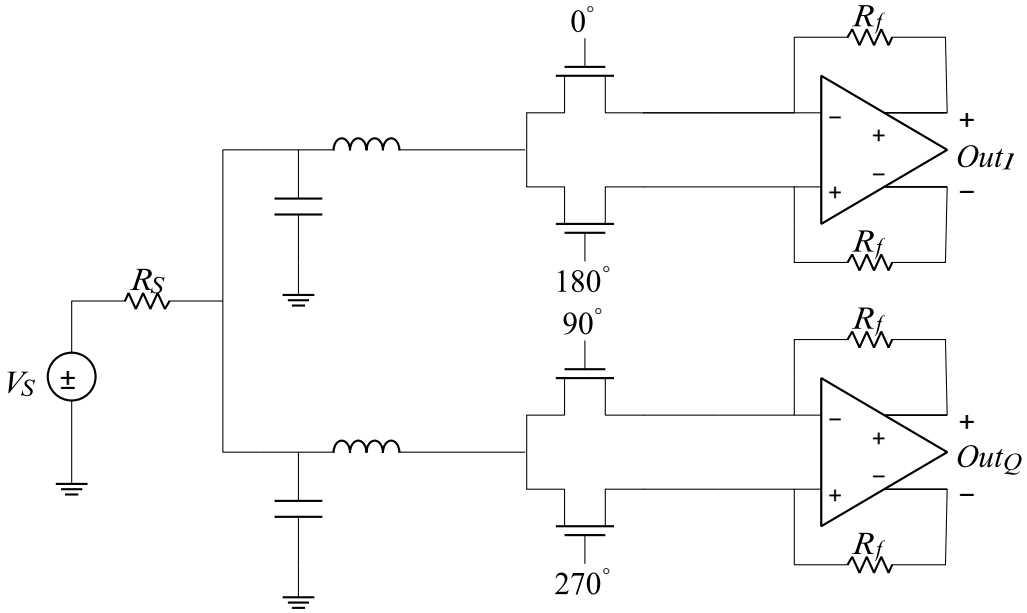

Figure 3.6: Mixer-first Receiver with L-matching Network

3.1.6 Limitations

Using a Wilkinson Divider in a mixer-first receivers provided an improvement in the noise figure. But their application is limited due to several factors. At 20GHz, the required length of a quarter wavelength transmission line at is about 2mm. This means that the design will consume large area and will not be practical. And although removing the resistor improved the noise figure significantly, the receiver is still narrowband.

3.2 Mixer-First Receiver with Tunable Matching Network

To overcome the area and the bandwidth limitation imposed by transmission line length in the designs proposed in the previous chapter, the quarter-wavelength transmission line can be replaced with a passive LC matching network. The matching network will behave as an artificial quarterwavelength transmission line and it will transform the on-resistance of the mixers' to a 50Ω. Figure 3.6 shows the receiver with the passive matching network. The matching network is used on both the I and the Q paths and it behaves as a low-pass filter to isolate the I and Q paths. It consists of a shunt cap at the input and a series inductor. This configuration is chosen as opposed to the capacitor in series and a shunt inductor because the series inductor would provide filtering to the charge sharing current, which is similar to the design described in [3]. This is an improvement from the previous design because a 2mm transmission line is not needed anymore, which puts less constraint on the area.

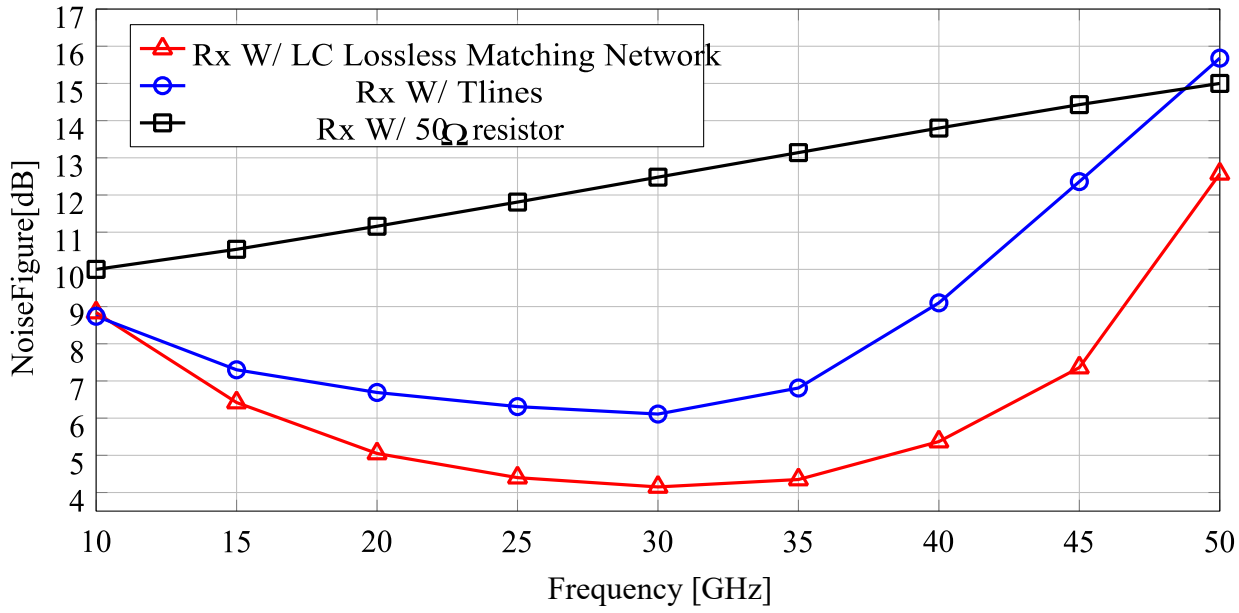

Figure 3.7: Comparison of NF Across Three Different RX Designs

3.2.1.1 Tunable Matching Network

In addition to the reduction in area, using passive components in the matching network will provide the possibility of making the receiver a wideband receiver. To achieve that, the matching network needs to be tunable.

This means that both the inductor and the capacitor need to be adjustable. The capacitor can be implemented with a varactor or capacitor bank. The tunability of the inductor is more difficult to realize since inductors occupy larger amount of area and implementing an inductor bank would be difficult. This means that the variable inductor needs to be implemented differently. In this design, the tunable inductor is implemented with an inductor in series with a capacitor bank. The impedance of that combination can be written as

$$Z_{series} = j\omega L + \frac{1}{j\omega C} = j\left(\omega L - \frac{1}{\omega C}\right) \quad (3.4)$$

By looking at Eq. 3.4, it can be shown that changing the value of the series capacitor has the same effect as implementing a tunable inductor. Decreasing the value of the series capacitor while keeping the inductor fixed will be the equivalent to decreasing the value of the inductor.

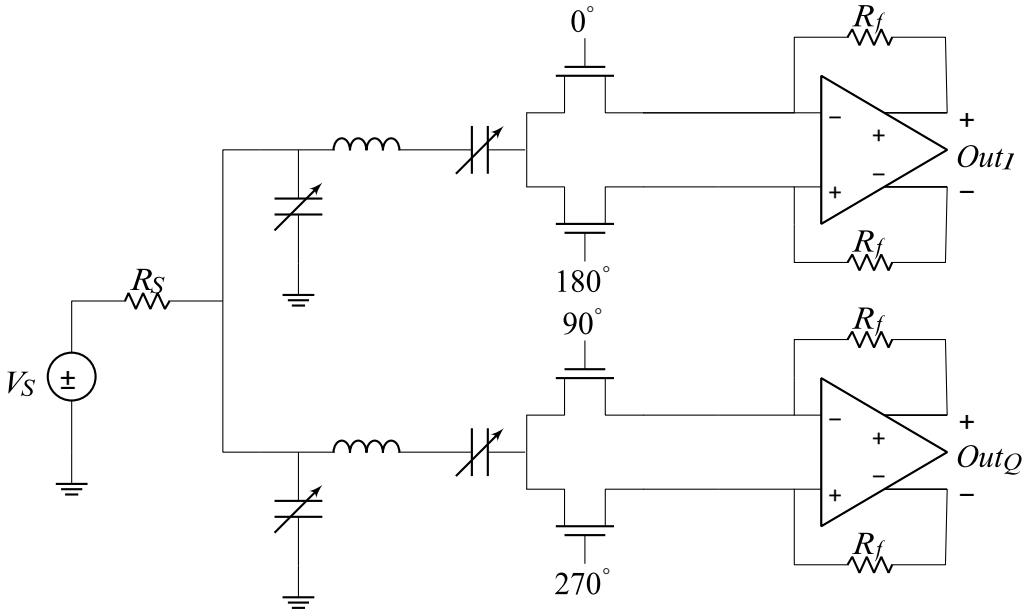

Figure 3.8: Mixer-first Receiver with Tunable L-matching Network

The shunt capacitor can be implemented with a varactor since its value varies slightly between different frequencies. The series capacitor, on the other hand, needs to be implemented with a capacitor bank.

3.2.2 Linearity

The linearity of the receiver is limited to the linearity of the mixers and the baseband amplifier. This can be seen by analyzing the overall IIP3 of the receiver which is given by the following equation:

$$\frac{1}{V_{IIP3}^2} = \frac{a_{2MN}}{V_{IIP2\,3,Mixer}} + \frac{a_{2MN}a_{2Mixers}}{V_{IIP2\,3,BB}} \tag{3.5}$$

The gain of a four-phase mixers is approximately 1. The voltage gain of the matching network is less than unity, which means that the IIP3 of the mixers is effectively increased. The linearity limit imposed by the baseband amplifier is mitigated by using feedback linearization, which is a technique previously proposed by our team [19]. By choosing a large open loop gain of the baseband amplifier for the matching with a physical resistor, the swing at the input of the baseband would be small and can be considered as a virtual ground. Making the input of the baseband amplifier's input a virtual ground means that input swing to the baseband amplifier is minimized, which limits the effect of the baseband non-linearity.

The linearity limit that the mixers impose is mitigated by stepping down the input voltage with the matching network and using a smaller on-resistance for the mixers. A smaller V_{ds} results in a

more linear mixer. The reduction of the V_{ds} swing across the mixer would not be the limiting factor in the receiver linearity.

3.2.3 LO Harmonic suppression

The proposed architecture offers LO harmonic filtering. The presence of high frequency LO harmonics means that interference at those frequencies will be down converted to baseband, degrading the signal-to-noise ratio at the output and the receiver's noise figure. The matching network between the antenna and the mixer acts as a low-pass filter. Interference at the LO harmonics will be attenuated before getting down-converted to baseband. This will improve the signal-to-noise ratio at the output and will improve the noise figure. The filtering effect makes this architecture a harmonic rejection receiver. Unlike conventional harmonic rejection receivers, the tunable nature of the matching network allows for wideband operation.

3.2.4 Charge sharing

In addition to being part of the matching network, the series inductor in the matching network offers another benefit. the inductor provides filtering to the charge sharing currents between the I and Q paths. This will consequently improve the noise figure of the receiver. The use of an inductor is also reported in [3] to reduce charge sharing.

3.2.4.1 Baseband Amplifier

The baseband amplifier is implemented with and inverter-based amplifier shown in figure 3.10. Open loop gain of the amplifier is 36dB and the feedback resistor is programmable.

3.2.4.2 LO Chain

The LO chain used is similar to the one used in the first chapter. The single-ended LO input is converted to a differential waveform using a balun. Using inverter-based buffers, the differential waveform is fed into a quadrature hybrid to generate the four-phase 50% LO Waveform. Inverterbased LO buffers are used after the quadrature hybrid to drive the mixers.

3.2.4.3 Mixers' Sizes

The choice of the mixers' size affects the performance of the receiver. Choosing a large device would make the on-resistance of the mixer smaller, improving the noise figure. The simulation results showed a 0.3dB improvement in the noise figure when using a switch with on-resistance 6Ω instead of 12Ω. The mixers are driven by an ideal voltage source with overlapping waveforms.

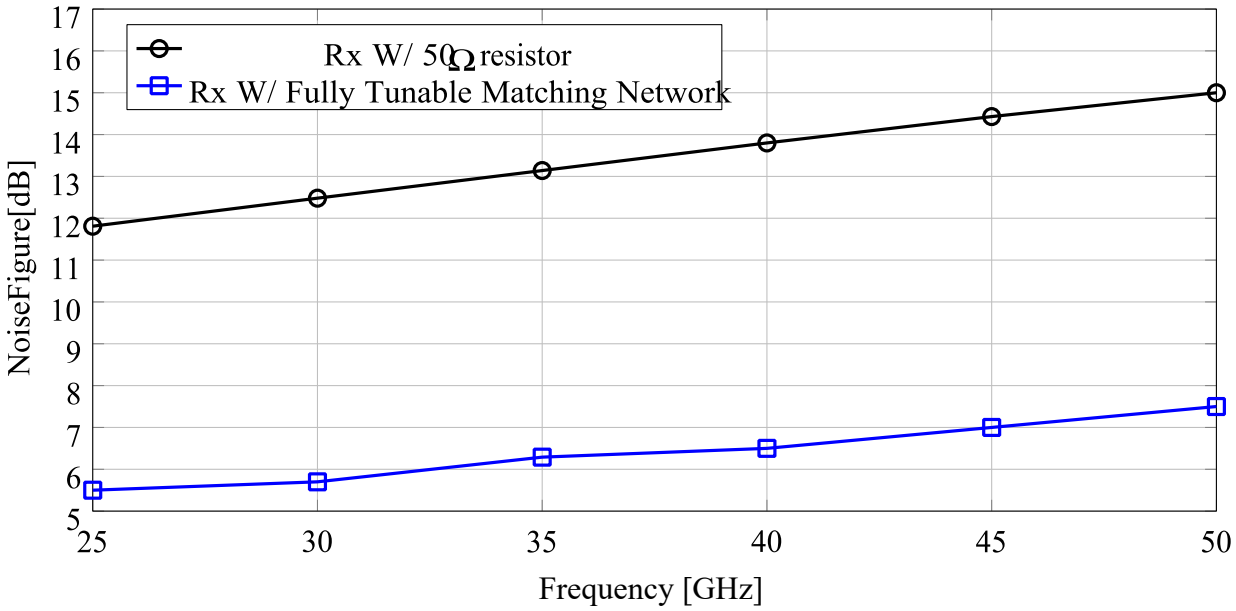

Figure 3.9: Noise Figure Values of the Proposed Linear Receiver Compared to the Design Proposed in the Previous Chapter

The simulations are with ideal LO, baseband amplifier, and R_{sw} = 6Ω.

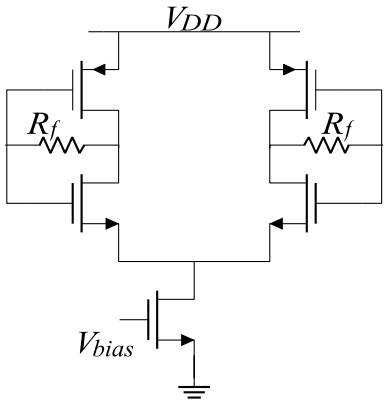

Figure 3.10: Inverter-based Baseband Amplifier

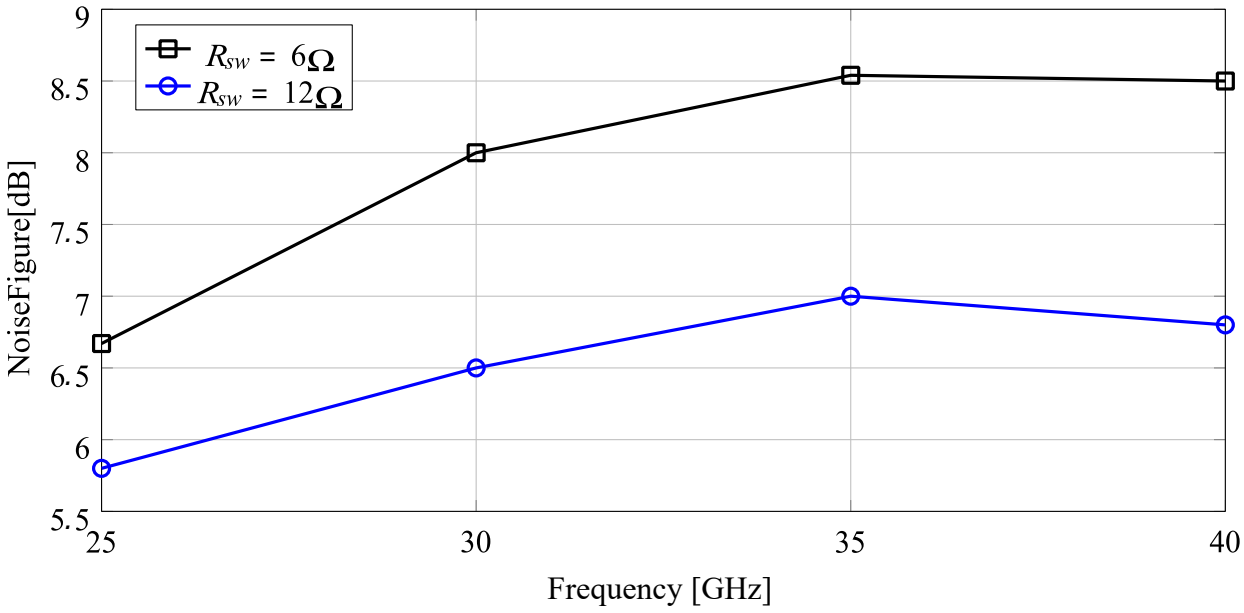

Figure 3.11: Noise figure of Rx with a fully tunable lossy matching network, transistor switches, and the transistor-level LO chain

The larger transistor size means that the gate capacitance of the mixers will be larger, making it more difficult to drive the mixers with a reasonable power consumption. The larger mixers also mean adding more parasitic capacitance to the input of the mixer, leading to more loss in the signal path and further degradation in the noise figure. Hence, the final design uses switches with W/L = 27µm/30nm instead of a larger device size, with on-resistance of 12Ω.

3.2.4.4 Matching Network Implementation

The pad and the parasitic capacitance at the input can be included to implement the shunt capacitor. The inductors are implemented with octagonal single-turn inductor to maximize the quality factor of the inductor. The series capacitor is implemented with a capacitor bank.

Figure 3.12 shows the final results of the post-layout simulated design. R_f = 1kΩ is used. Noise analysis in virtuoso shows that the noise of R_f contribute 30% of the overall receiver noise. Choosing a larger value will improve the noise figure but will degrade the linearity of the receiver. The well-know discontinuities in the BSIM4 [44] models made it difficult to simulate IP3 of the receiver. The source of the problem are transistors in the deep triode region, which in this case are the mixers. The mixers were replaced by ideal switches to simulate the IP3.

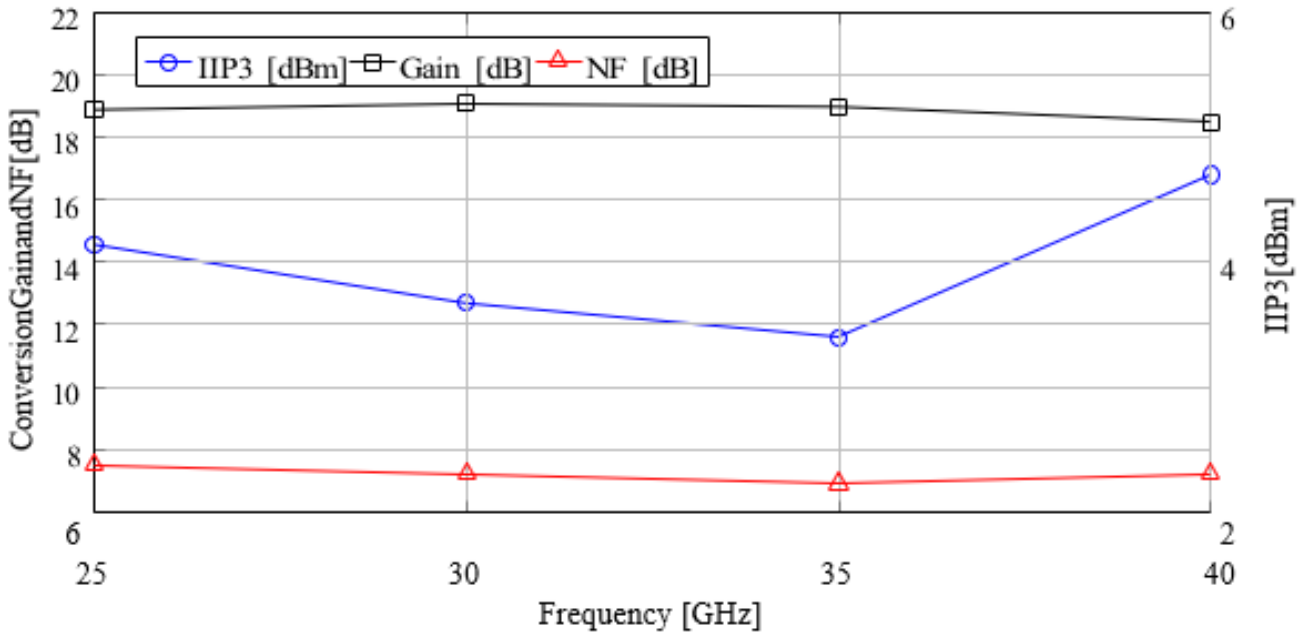

Figure 3.12: Post-layout Simulations of the Design

3.2.5 Measurement

Figure 3.13 shows the top level layout of the chip. The design was taped out in a 28nm bulk CMOS process and is awaiting completion of the fabrication. The expected performance is on par with our previous demonstrate with regards to conversion gain and linearity, but has markedly better noise figure, less than 8-dB across the band from 25 GHz to 40 GHz. These are simulation results but nevertheless even comparing simulations to previous simulations, we see improvements. We eagerly await the fabricated die to confirm these findings.

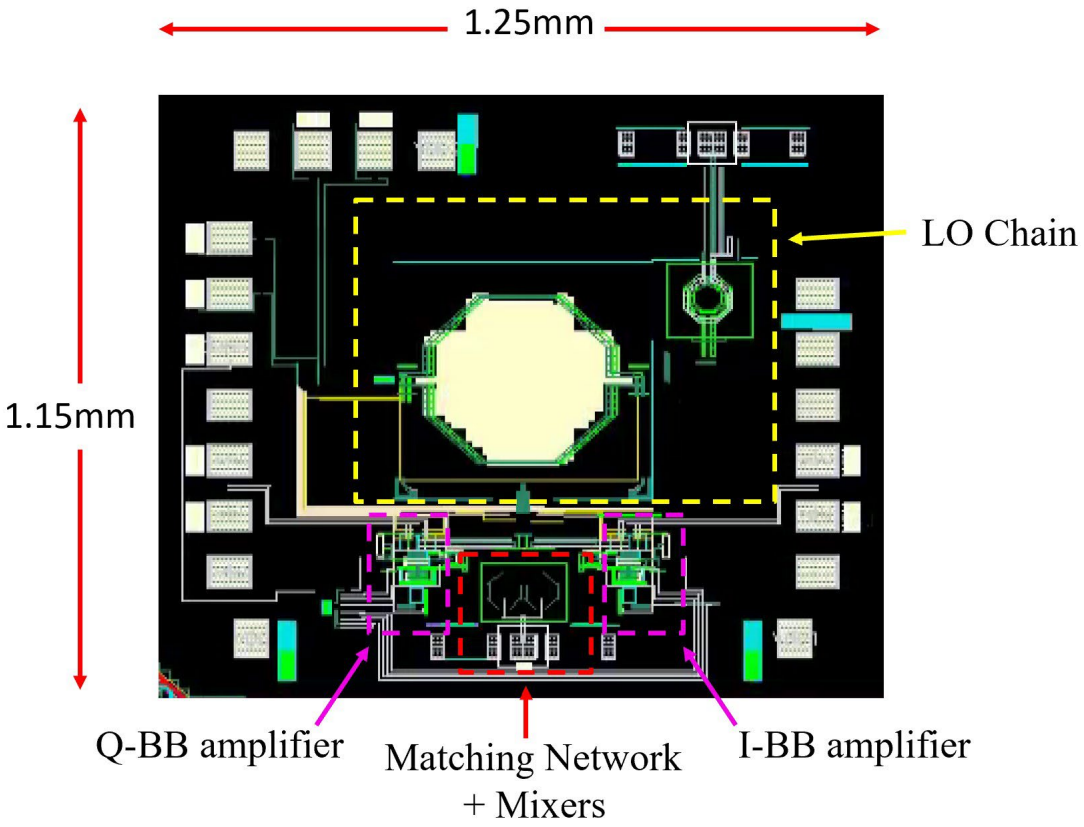

Figure 3.13: Top Level Layout of the Chip

Table 3.1: Comparison with Mixer-first Receivers Greater Than 25GHz

	Moroni [28] RFIC 2012	Wilson [39] RFIC 2016	Iotti [13] JSSC2020	Boynton [8] RFIC2020	Ahmed [1] CICC2020	This work
Technology	65nm CMOS	45nm SOI	28nm CMOS	65nm CMOS	22nm FD-SOI	28nm CMOS
f_{RF} (GHz)	49 – 67	20–30	70 – 100	9 – 31	43 – 97	25 – 40
Voltage gain (dB)	13	8 – 20.6	19.5 – 25.3	45	12 – 15	18 †
In-band IIP3 (dBm)	-	-2.3 – -9.7	-	-	0 – +4	+3.6 – +4.2 †
NF (dB)	11–14	8	8 – 12.7	12.5 – 17.5	12.5 – 16.5	6.8 – 7.5 ♯
DC power (mW)	14	41 (at 24GHz)	12	72	36	22.8 (Baseband); 19 – 37 (LO)
Supply (V)	1.2	0.9/1.8	1	-	-	1.2

† Simulated values reported at nominal setting (R_F = 1kΩ), across f_{LO}.

♯NF varies from 6.8 – 7.5 dB for f_{LO} = 25−40GHz.

Table 3.2: Comparison with Recently Published 28GHz Receiver Front-ends

	Yeh [41] RFIC 2016	Kibaroglu [17] RFIC 2017	Mondal [27] JSSC2019	Sadhu [34] JSSC2017	This work
Technology	120nm SiGe	180nm SiGe	65nm CMOS	130nm SiGe	28nm CMOS
f_{RF} (GHz)	28-32	28-32	28/37	28	25 – 40
Voltage gain (dB)	9.4	20	33/26.5	34	18
NF (dB)	5.1	4.6	7.3	6	6.8 – 7.5[#]
DC power (mW)	136.5	130	52.5	103.1	22.8 (Baseband); 19 – 37 (LO)

[#]NF varies from 6.8 – 7.5 dB for f_{LO} = 25−40GHz.

4 RF-DAC LINEAR TRANSMITTER

4.1 Introduction

5G communication utilizes a rich spectrum in millimeter-wave(mm-Wave) bands. In particular, the FR2 spectrum extends from a 26.5GHz all the way to 71GHz in different countries/regions. To support all these disparate bands, it usually requires different transceivers designed for a specific frequency range. It is not only costly, but also takes up a lot of valuable PCB area especially on mobile devices. Hence, it is highly beneficial to design a single transceiver that supports a wide RF frequency range, so that the system will support multiple applications, such as MIMO communication and mm-Wave radar, on a single platform. To achieve such versatility, the transceiver is required to have wide frequency bandwidth, high instantaneous RF bandwidth, low noise figure, as well as high linearity in both the RF-end and the baseband. This chapter will focus on the exploration of different architectures to realize these goals for a transmitter.

4.1.1 Traditional Transmitter vs Distributed RF-DAC

Traditional transmitter typically consists of the following stages: a Digital-to-Analog Converter (DAC), a baseband Filter, an up-converting Mixer, an RF Filter, and a Power Amplifier, as shown in Fig. 4.1. The LO distribution will be simpler in the traditional design compared to a distributed design. However, to achieve high linearity of the overall transmitter, each stage would have to be extremely linear by itself. Often we will see that the linearity degrades due to signal-dependent current through the mixer and finite output impedance of the DAC.

On the other hand, RF-DAC transmitter uses distributed design, as shown in Fig. 4.2, where each element consists of a DAC and a mixer with less output power than the traditional counterpart, but *N* of such element are combined together at the RF output. There is no explicit PA in the transmitter, as it is absorbed into the distributed element and the output sums up the power delivered by each cell using a power combiner such as a Transmission Lines (T-Line). To obtain higher linearity at the output, the architecture often becomes more complicated. The LO distribution network is required, and the matching between each element would limit the overall linearity of the system.

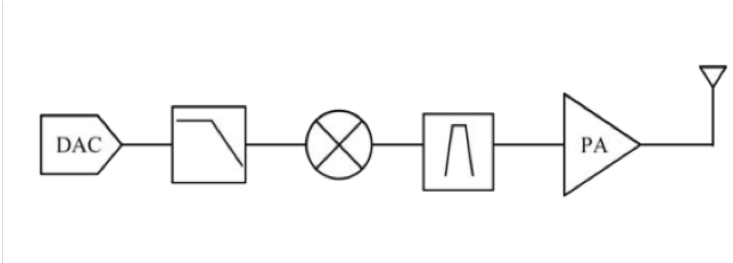

Figure 4.1: Traditional Transmitter Block Diagram

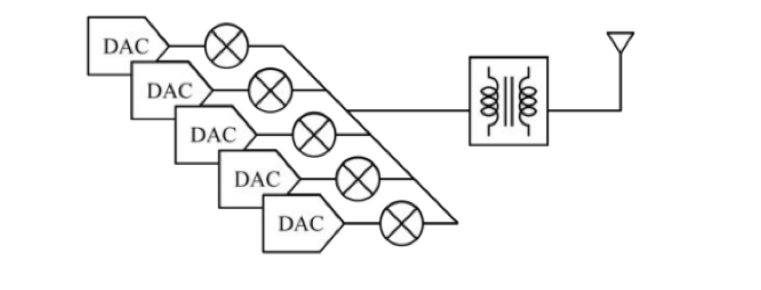

Figure 4.2: RF-DAC Block Diagram

In this project, we explored the potential and limits of both types of designs by taping out two high-linearity global mixers (active and passive), and a complete transmitter chain with I/Qchannel DACs, baseband filters, and distributed mixers along the T-Line.

4.2 High-Linearity Mixer Designs

The following mixers were taped out in October 2019 using TSMC 28nm Bulk CMOS. These mixers are assumed to be used in a traditional transmitter architecture as the global mixer, so the key design goal was to achieve high linearity with a single mixer. We took different paths and proposed two mixers: a passive mixer and an active mixer, both of which were aimed to achieve high linearity by reducing the signal-dependent quantities in the circuit.

4.2.1 Passive Mixer

The schematic of the taped-out passive mixer is shown below, in figure 4.3. It consists of the standard double-balanced mixer topology, with the addition of bootstrapping resistors from the IF input to the gate of the mixer transistors to further improve the linearity. These resistors cause the gate to track the (low frequency) IF port, keeping the transistors' V_{gs} independent of the IF signal, which reduces intermodulation (IM) products due to the IF signal [37]. The mixer itself is driven by a simple common source amplifier with a choke inductor load. To keep the structure broadband, asymmetric T-coils were used as output matching networks to the probe pads and their ESD diodes. The overall layout is shown in Fig. 4.4. The measured results are given in Fig. 4.1, and were within 1-2dB of simulation; the mixer showed a reasonable OIP3 for a low power consumption (8.4mW at 24GHz, 15.6mW at 40GHz), and was capable of operating across a wide bandwidth.

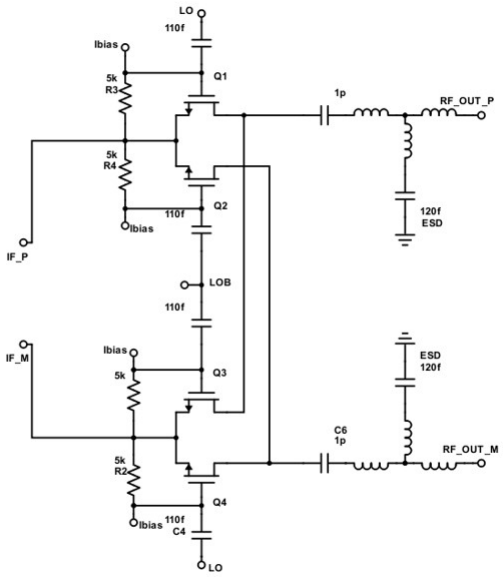

Figure 4.3: Passive Mixer Schematic

Note the output capacitors represent the ESD diodes. The output is matched via an asymmetric T-coil. The resistors bootstrap the IF signal to the mixer gates, to remove IF-dependent linearity effects.

Table 4.1: Simulated OIP3 of the Proposed Active Mixer

Frequency(GHz)	Measured P_{1dB}(dBm)	Measured OIP3(dBm)	Simulated OIP3(dBm)
24	-4.3	4.16	5.25
32	-9.1	1.89	3.1
40	-8.9	0.41	1.5

4.2.2 Active Mixer

In a differential amplifier with tail current I_{SS}, if the two input MOSFETs are different in size, the large signal transconductance G_m vs V_{GS} curve will shift to the left or to the right, as shown in

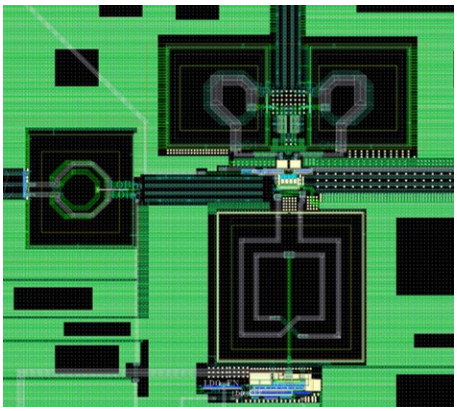

Figure 4.4: Passive Mixer Layout, Viewed in Cadence Virtuoso
The T-coil matching is at the top, the driver choke is below.

Fig. 4.5[32]. If the drains of the two opposite copies of such amplifier are combined, the overall G_m curve could be flattened.

Fig. 4.6 shows the current flow in a single-balanced active mixer. For analysis purpose, we simplify the IF input to be a current source with some finite conductance, G_0. At any given moment, the following equations describe the relationship between the current in different branches:

$$i_1 + i_2 = i_{in} + G_o V_s \tag{4.1}$$

$$i_1 \approx f\left(V_{G0} + \frac{V_{LO}}{2}, V_s\right) \tag{4.2}$$

$$i_2 \approx f\left(V_{G0} - \frac{V_{LO}}{2}, V_s\right) \tag{4.3}$$

If we write i_1 in terms of the DC term and the derivative of i_1 with respect to V_{G0} and V_{S0} times the differential quantities, we will get:

$$i_1 \approx f(V_{G0}, V_{S0}) + \frac{\partial f}{\partial V_s} v_{LO} + \frac{\partial f}{\partial V_G \partial v_S} v_{LO} \times v_S + \ldots \frac{\partial^2 f}{\partial V_G^2} v_{LO}^2 \tag{4.4}$$

$$\approx I_Q + G_{m1}(t) v_{LO} + \frac{\partial f}{\partial V_s} v_S + \frac{\partial^2 f}{\partial V_G \partial v_S} + \ldots \tag{4.5}$$

The first term is the DC current with no signal. The second is the LO-feedthrough term which will get cancelled in the double-balanced differential output. The third term, which is a little bit more complicated if we take the full derivative, is a non-linear and time-varying term (as the IF signal changes), which generates distortion and mixing. The fourth term is also non-linear and time-varying, and it also changes as the IF signal changes. This simple Taylor

Series expansion shows that the output current depends, in a non-linear way, on both the source (input) voltage and gate (LO) voltage. The LO controls the gates in a time periodic way, and the source varies due to the DAC and the second harmonic of the LO. At any given moment, the value of v_S, and consequently the current that flows into the differential pair versus the current that flows into the load G_o depends on the ratio between $G_o(t)$ and $G_m(t)$. Even if we have an ideal DAC whose output impedance is independent of signal, we still would suffer from non-linearity because $G_m(t)$ is changing in magnitude due to the source voltage varying. Therefore, if we flatten the G_m with respect to the LO port, the non-linear mixing term can be lowered in magnitude.

The architecture of the active mixer is shown in Fig. 4.7. It is a modified current-commutating mixer (Gilbert-type mixer). Instead of one current steering DAC (+ and – outputs), we use two, but each only burns half of the current. The topology is adapted from the amplifier by connecting the drains of the two G_m-linearized amplifiers together. By purposely introducing asymmetry between the $LO+$ and $LO-$ transistors, we can reduce the non-linear mixing term at the output.

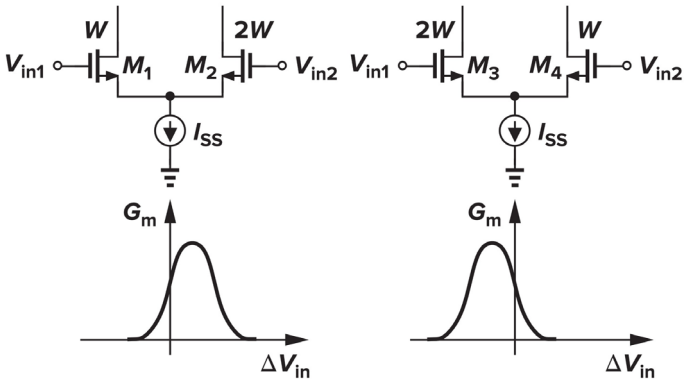

Figure 4.5: G_m curve Shifting Due to Asymmetric Differential MOSFET Pair

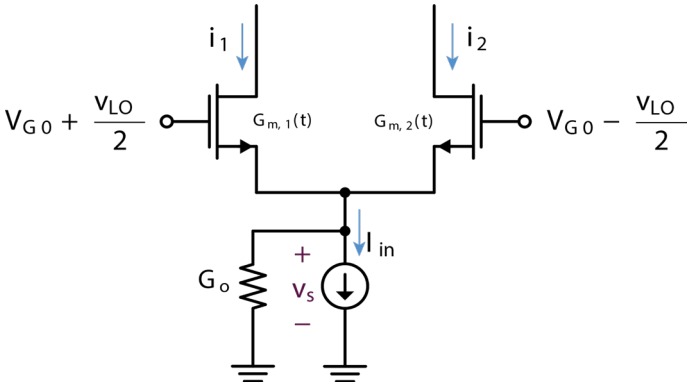

Figure 4.6: Simplified Model for Single-balanced Active Mixer

For testing purpose, we replaced the two DACs to be a common-gate input stage so we will have enough headroom for swing at the output. The schematic and layout floorplan is shown in Fig. 4.8 and Fig. 4.9. The DC current consumption of the mixer is 13.5mA, but this

current will be shared with the DAC. We simulated its performance at relatively high output power (non-linearity dominating the SINAD) in comparison with traditional double-balanced mixer at the same output power and total DC current consumption, and the result is shown in Fig. 4.10 and Fig. 4.10. It is worth noting that, because of more active MOSFETs being used in our design, the SINAD will be lower than traditional double-balanced mixer when the signal power is very low (such that the noise power dominates the SINAD). The OIP3 simulated at 25.6GHz with 200MHz bandwidth IF input using extracted transistors and ideal 50Ω source/load impedance is 10.96dBm, and it is 10.38dBm at 50GHz, as shown in Table 4.2.

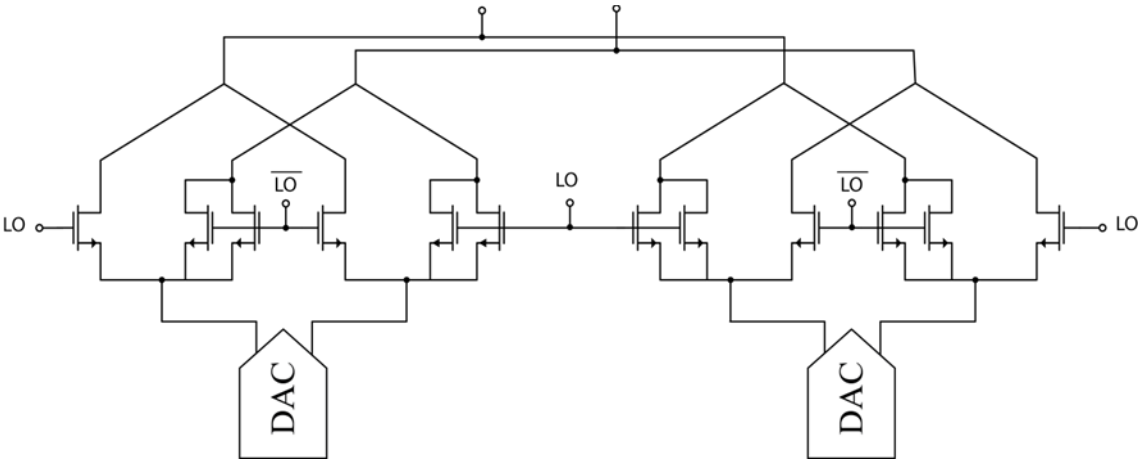

Figure 4.7: Linearity-improved Active Mixer

Table 4.2: Simulated OIP3 of the Proposed Active Mixer

Frequency	25.6GHz	50GHz
OIP3	10.96dBm	10.38dBm

The mixer was taped out in TSMC 28nm bulk CMOS technology. The output power at 24, 28, 32, and 36GHz with 200MHz bandwidth IF input was measured and shown in Fig. 4.12. Note that the OIP3 extrapolated at different points varies, as the slope of the third-order harmonics (in dB scale) is not constant as opposed to commonly seen 3dB/dB slope. Measured and simulated OIP3 are reasonably close demonstrating the validity of the approach.

4.3 High-Linearity DAC with Distributed Active Mixer

Following the high-linearity mixer, we taped out a transmitter in TSMC 28nm bulk CMOS with 10 bit I/Q and RF at 40-60GHz. Fig. 4.13 shows the system block diagram of the transmitter, which consists of both I and Q paths.

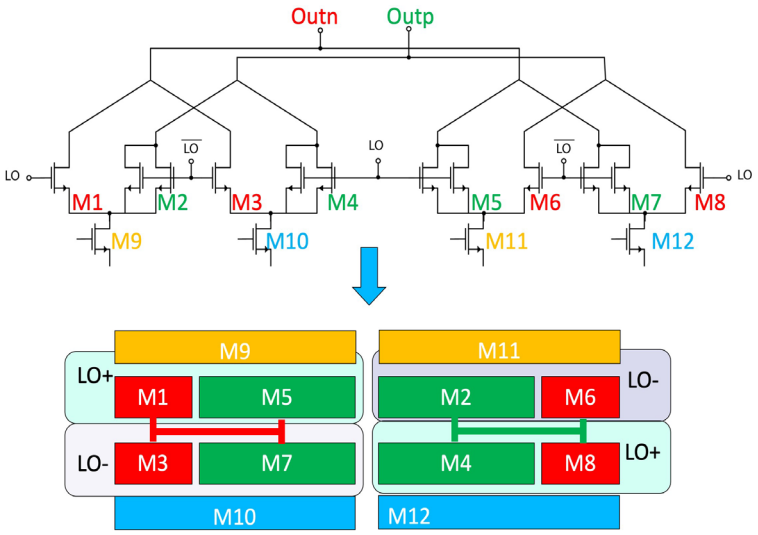

Figure 4.8: Schematic and Floorplan of the Linearity-improved Active Mixer

4.3.1 High-Linearity DAC

Traditional current-steering DAC, such as the one shown in 4.14, suffer from a number of problems. One of the top problems is the limited headroom. Usually the current source MOS are long channel devices because of pursuit of high output impedance for linearity reasons. Therefore, to generate certain required current, it requires larger V_{GS} bias than short channel devices, and consequently needs high source-drain DC voltage for operating in saturation. Therefore, the headroom voltage at the output node is reduced, which makes current sharing between the DAC and active mixer extremely difficult. Also, the swing at the output node will directly impact the bias of the current source. Cascoding the current source to boost its output impedance will result in the same situation, which makes mixer cascoding or low-supply voltage operation not an option.

Another issue is that, since there's no shielding between the input differential pair and the output node, charge feedthrough from the input to the output due to parasitic coupling between the gate node and the drain node could severely degrade the performance of the DAC, creating a series of spur tones on the output spectrum. One way to decouple the output node from the input node is to add a cascode transistor before the output node as shown in Fig. 4.15. However, this is only be feasible if the supply voltage is high enough, otherwise the headroom will still be an issue.

The DAC adopts a folded-cascode structure as shown in Fig. 4.16, a topology that was modified from the folded-cascode differential amplifier, first proposed by [31] which wasn't verified through silicon yet. $M_{5,6}$ provides constant bleeding current. By putting the input pair and current source on the separate branch, the V_{DS} of M_1 and M_2 can be set high independent of the output voltage bias. Because the headroom is no longer an issue (due to fewer stacking of transistors), we can keep $M_{7,8}$ as the shielding devices so the output node and the input gate no

longer have a direct coupling path, so the impact of charge feedthrough can be mitigated considerably.

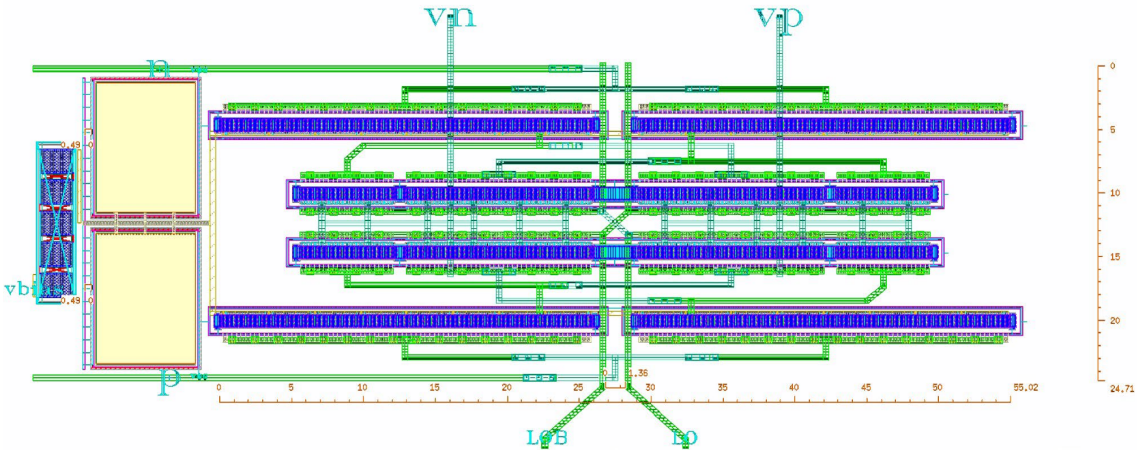

Figure 4.9: Layout of Linearity-improved Active Mixer

We used the 6-thermometer + 6-binary digits segmentation for the DAC. The binary cells share one folded branch (right hand side of the structure) as shown in Fig. 4.17. The size of each thermometer cell is 2^6 = 64×LSB size. The DC power consumption of the 10-bit DAC is 1.4mW, and the AC power (with the bit latches included) is 1.47mW.

4.3.2 High-speed FPGA-to-Chip SerDes Link

One of the big challenge for testing the DAC above is to send all the bits (10 differential pairs for I and Q-channel each) at 10GHz rate and align the phases, as the bits were not fully synchronized due to the limited bank size of FPGA and skews due to different transmission delays. For the high-speed bit generation and transmission to our chip as the input to the DAC, we are using Xilinx Ultrascale+ VCU-118 FPGA platform with its built-in 28GHz serial LVDS transmitters. Each bank is capable of driving four differential channels, so in order to drive the 20 differential I/Q bits, we need a total of five banks. Because each bank has a separate clock domain, the relative delay between the banks and the delay due to the routing need to be corrected on chip.

Fig. 4.19 shows the phase calibration loop that we designed to for bit-alignment. The loop will calibrate the delay of each bit by comparing the phase of the bit against the master clock that drives the latches of the DAC. Each bit will go through a digital delay line initialized with minimum delay, and the loop will detect if the rising edge of the master clock arrived earlier compared to the bit, and the delay will be added to that bit (with a step of 9ps each time), until the rising edge of that bit lags behind the clock. The calibration will be performed for all bits for I and Q channels, and then additional delay will be added to the DAC (via scan bits) to meet the setup and hold time requirement. The layout is shown in Fig. 4.20 and it consumes 110mA of current when operating with an activity factor α = 1.

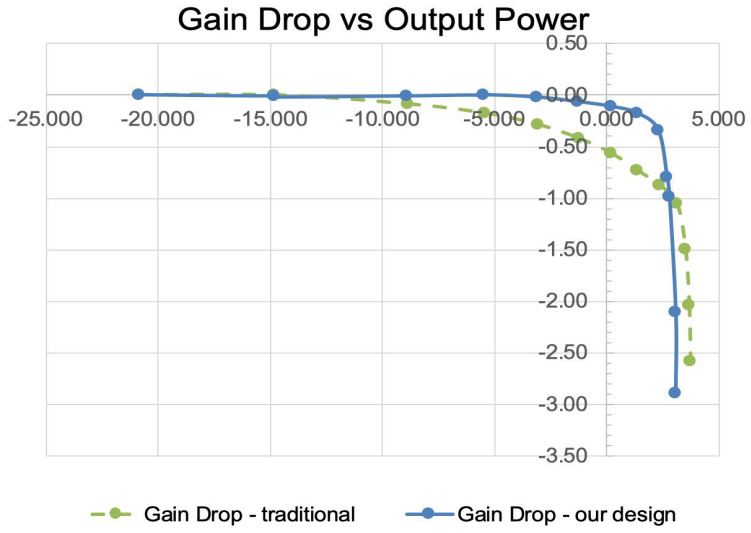

Figure 4.10: Comparison of Gain Compression of Traditional Mixer and the Proposed Mixer

4.3.3 Current Mirror Filter

The anti-alias filter schematic is shown in figure 4.21. The filter itself is a modified version of that shown in [15]. The input to the filter has a low impedance thanks to the negative feedback (akin to the super source follower or gain boosted stages), while the loop gain is not extraordinarily large (note the common source drives the source of the transistor above it), even with a moderate gain allows for a lower input impedance at no additional power cost. The (small-signal) impedance was designed and simulated at around 15Ω, with approximately 2mA of current consumption in the input branch (4mA total). The filtering action is created via a two, *m*-derived sections, as well as an output *RC* network. The *m*-derived sections provide both a sharp roll-off, as well as a notch, and were created using T-coils and variable capacitors (3 bit cap-DAC); the capacitor DAC adjusts the corner (and notch, though the ratio of corner:notch frequency remains constant) frequency. The Bode plot is shown in 4.22. The overall layout is shown in figure 4.23. Note that the signal is differential, so care was made to keep the layout symmetrical. Each filter consumes around 4mW of power.

With the filter knocking down the clock tone at 10GHz, the Effective Number of Bits (ENOB) is 9.05 bits when integrating the noise up to 50GHz, as shown in Fig. 4.24.

4.3.4 Distributed Active Mixer

To achieve high OIP3, we designed a distributed mixer by delaying the LO and RF signal by the same amount along the transmission lines. Because we used transmission lines, the delay is true time delay rather than phase delay, and the design is inherently broadband. To connect the

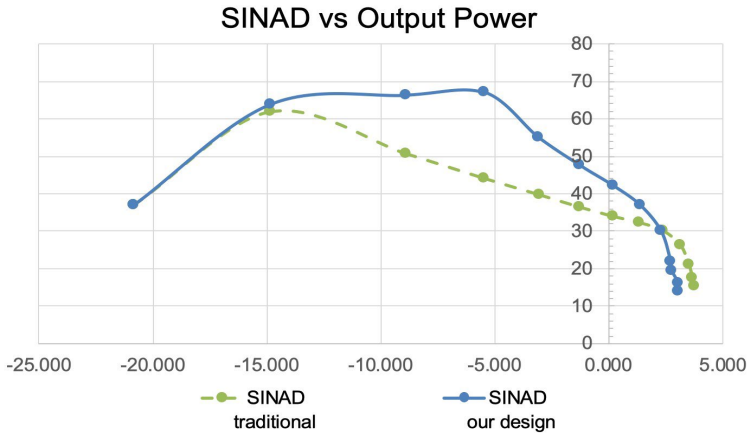

Figure 4.11: Comparison of Signal-to-Noise-and-Distortion Ratio of Traditional Mixer and the Proposed Mixer

gates of each sub-mixer as well as the drains, we designed a 125Ω differential high-impedance transmission line and the output capacitance of the mixers are absorbed in the design. The IF signal are injected into the sub-mixers using similar techniques, and the mismatch on the phase of the IF signal introduces little loss on the gain since the IF bandwidth is significantly less than the LO frequency. The simulated loss of gain with 500MHz filtered IF signal and 30GHz LO frequency is less than 0.1dB.

Fig. 4.25 shows the distributed mixer with output matching network to absorb the ESD and pad capacitance. The combiner for I/Q signals is also built-in by alternating the I-mixers and the Q-mixers along the output transmission line.

Because the mixers are distributed, the linearity requirement on each sub-element is not as high as in the traditional single-mixer designs. Shown in Fig. 4.26, we used the common source IF input at the bottom, and common gate LO input at the top. The IF port uses Class-A bias so the mixing gain is higher (compared to class-B) but the efficiency is lower. For better integration with the DAC-filter, we chose to bias the IF at 400mV V_{GS} with Class-A operation.

The RF output pad capacitance is simulated to be 40fF, and the ESD diodes contributes 80fF of capacitance. To absorb that, we designed an output matching network with artificial T-line that matches to the 50Ω output load. The other side of the transmission line was terminated with an RF choke with 150pH connected to the V_{DD}, so the output swing of the mixer is enhanced.

Fig. 4.27 shows the high-impedance transmission line with mixer loads distributed across the line. The unloaded line has Z_0 = 125Ω, and the loaded line has slightly lower impedance of 115Ω. The bandwidth of the line reduces with the addition of taps for gate LO and drain RF nodes.

The gain and linearity (P_{1dB}) of the mixer with the I/Q combining loss was shown in 4.29. It achieves a small-signal 3-dB bandwidth from 13-50GHz, with the peak P_{1dB} of -0.5dBm at 30GHz. The distributed mixer consumes a total of 33mA DC current when operated at P_{1dB} ($V_{DD} = 1.2V$). The entire transmission line with the taps, RF choke and inductors are EM-simulated, and all active devices are extracted from the layout including the metal stacks from M10.

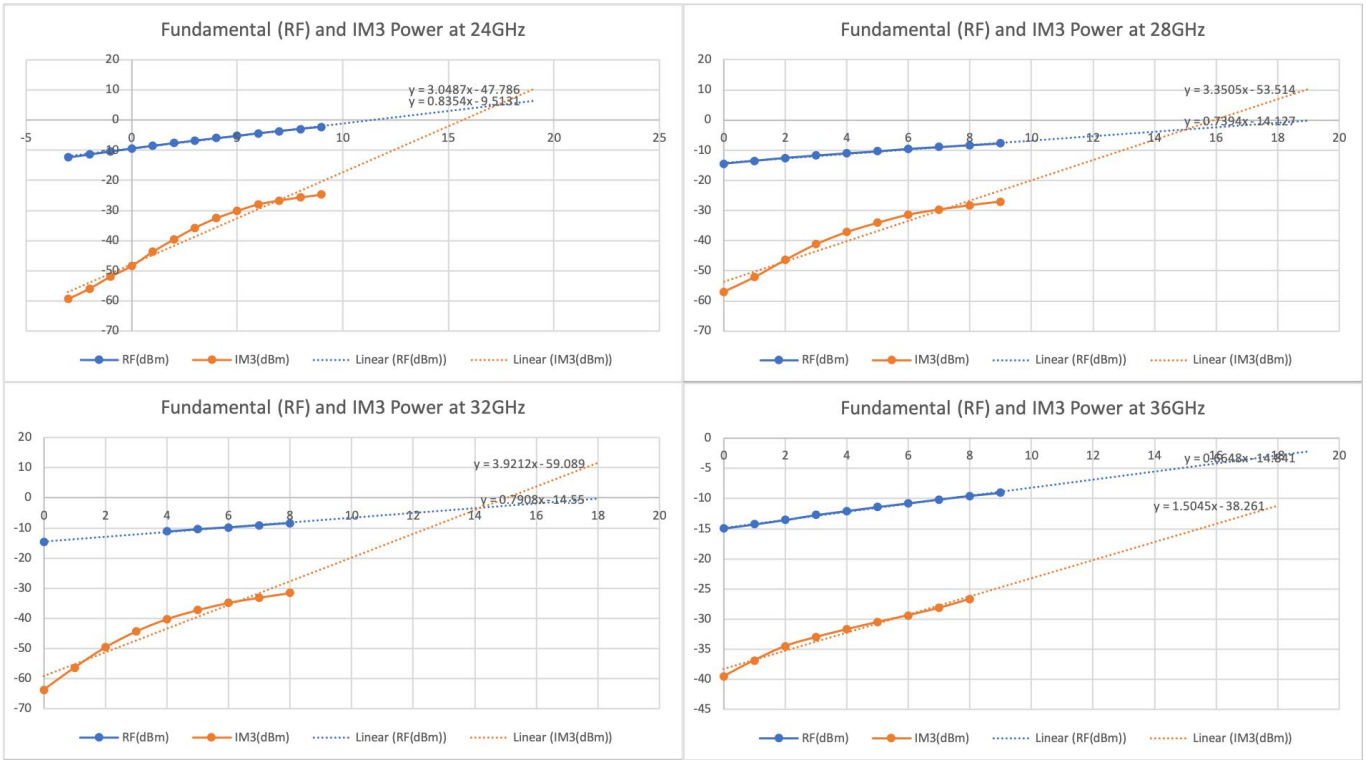

Figure 4.12: Fundamental and IM_3 output power measurements

The static EVM simulation was simulated with 16-QAM modulation scheme. Fig. 4.30 to Fig. 4.33 show one quadrant of the 16-QAM constellation. While operating at peak power = P_{1dB}, the EVM turns out to be -19.1dB with I/Q pulling, and -21.5dB without I/Q pulling, so the degradation in EVM due to I/Q pulling is 2.4dB when the mixer is at OP_{1dB} point. When the output power is backed-off to $OP_{0.5dB}$, the EVM is -22.5dB with I/Q pulling and -25.7dB without I/Q pulling, showing a 3.2dB degradation due to the I/Q pulling.
Table 4.3 summarize the performance of the distributed mixer.

4.3.5 Dual Mode Wideband LO Chain

A major challenge in the transmitter is providing LO power across the entire frequency regime, from around 18GHz to potentially 60GHz. As this is far more than an an octave, and thus out of range for a typical broadband matching network, a dual frequency drive chain was designed. The general idea is to have a high and low frequency amplifier chain, with a switch to decide between them, as shown in figure 4.34. Both the LO paths end in a two stage (with inter-stage low-*k* transformer matching) class A/B driver that drives the LO through the switch

network and into the transmission line mixer input. The gate bias voltages in the drivers were made to be fully re-configurable. This tune-ability will allow for increased LO drive power if necessary during testing (class A bias). The nominal setting has 15mA DC current, and a 1.2V supply for both stages combined, with higher power needed to overcome the lossy switch network.

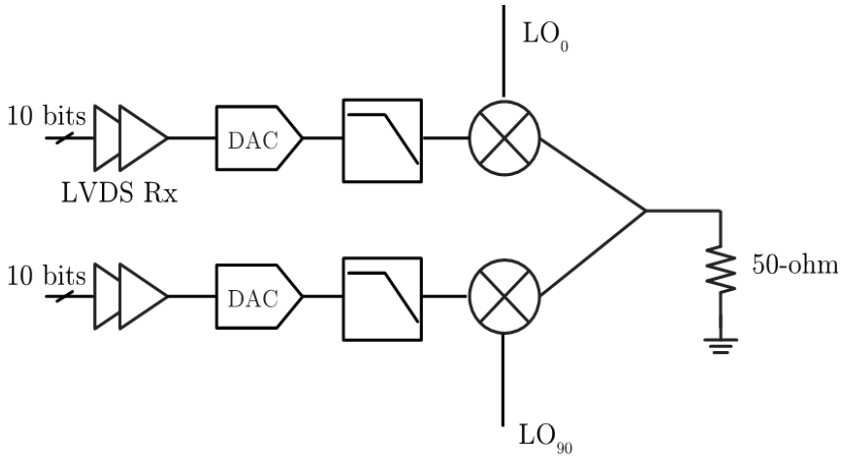

Figure 4.13: System Block Diagram of the Transmitter

Table 4.3: Summary of the Performance of the Distributed Mixer

Metric	Performance
Bandwidth	13-50GHz
P_{1dB} (w/o I/Q combining)	2.5dBm
P_{1dB} (w/ I/Q combining)	-0.5dBm
DC power (at OP_{1dB})	39mW
DC supply voltage	1.2V
Efficiency	2.3%
EVM (at OP_{1dB} with I/Q pulling)	-19.5dB
EVM (at $OP_{0.5dB}$ with I/Q pulling)	-22.5dB

Low Frequency Chain The low frequency chain operates from around 18 to 35GHz. The schematic is shown in figure 4.35. At these frequencies, an inverter-based chain is still viable, and hence used for simplicity. An artificial transmission line *LC* hybrid was used to provide I/Q signaling, based on [14], with tuning capacitors used to set the balance and center frequency. A balun provides on chip differential signaling as well as impedance matching. The entire low frequency chain consumes around 40mA, on a 1.2V supply, primarily due to the power hungry inverter chains.

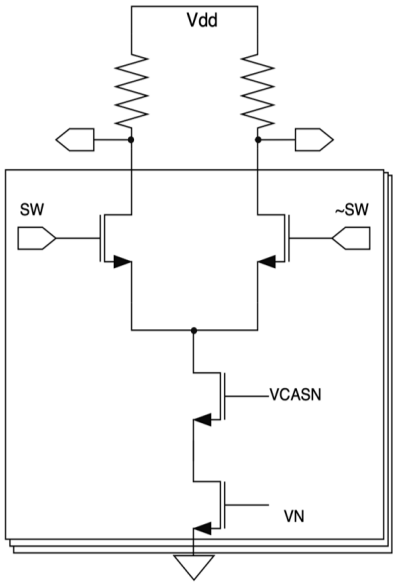

Figure 4.14: Conventional Current-steering DAC

High Frequency Chain The higher frequency chain operates from around 35 to 60GHz. The input probe pad and its ESD diodes are matched via a T-coil. The key feature in this part of the chain is the broadband 50Ω hybrid for I/Q signaling. This was accomplished through the use of a four-finger Lange coupler, shown in 4.36. The coupler achieves at worse 1.25dB of amplitude mismatch and 3 degrees phase imbalance across the 35-60GHz band, with about 1dB of insertion loss. The structure was designed and simulated in HFSS. From the hybrid, the signal is directly fed into a balun and matching network, to provide the required differential signaling and 50Ω match between the driver amplifiers and the hybrid. To provide a broadband match, a two stage network was used; the balun phase itself gave 10 degrees of phase imbalance across the entire band, which is not ideal, but still provides acceptable performance. The total power consumption here is simply that of the driver amplifiers, 15mA at 1.2V (18mW), though this can be adjusted higher if a larger LO drive is required.

The layout of the dual LO chain paths can be viewed in Fig. 4.37. The lumped and Lange hybrids are in the center of the chip, with the I/Q amplifier chains laid out symmetrically around the mixer. The signals are routed around the chip with grounded-co-planar waveguide transmission lines.

4.3.6 The Overall Transmitter

The architecture of each path is shown in Fig. 4.38. The output P1dB per-element with distributed architecture and I/Q combining is around -2dBm, and it consumes 71mW of power (including I/Q and excluding the power consumed by the high-speed SerDes link).

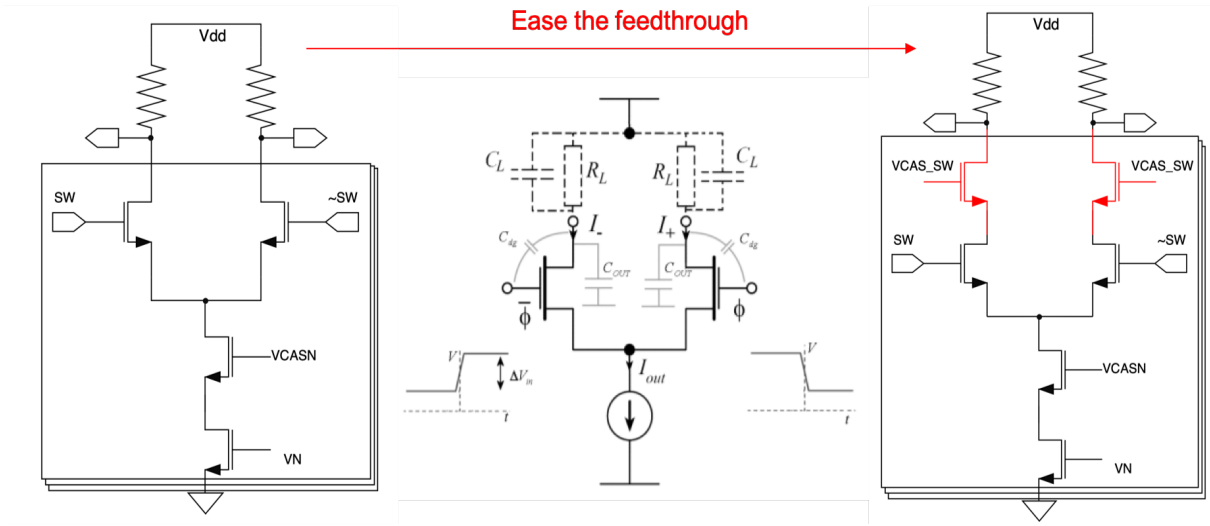

Figure 4.15: Conventional and Cascoded Current-steering DAC

4.3.7 Measurement

Fig. 4.39 shows the top level layout of the transmitter chip, which was taped out in TSMC 28nm bulk CMOS process (chip photo shown in Fig. 4.40) and is awaiting measurement. We are in the process of fabricating a PCB and assembling the entire system. Our first attempt at measurement failed due to PCB errors and lack of space for probing.

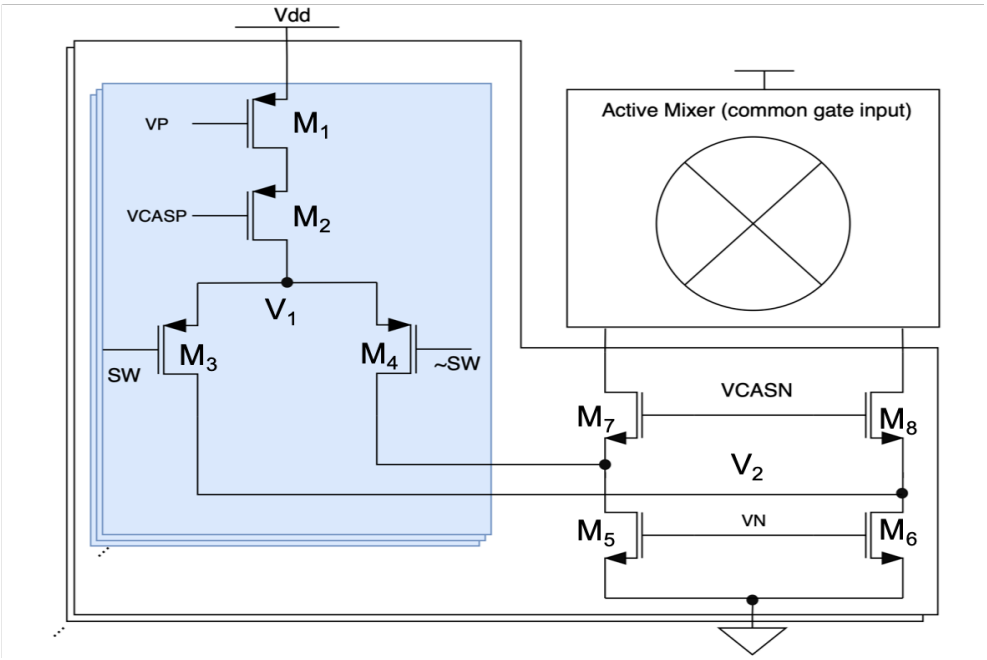

Figure 4.16: Folded-Cascode Current-Steering DAC

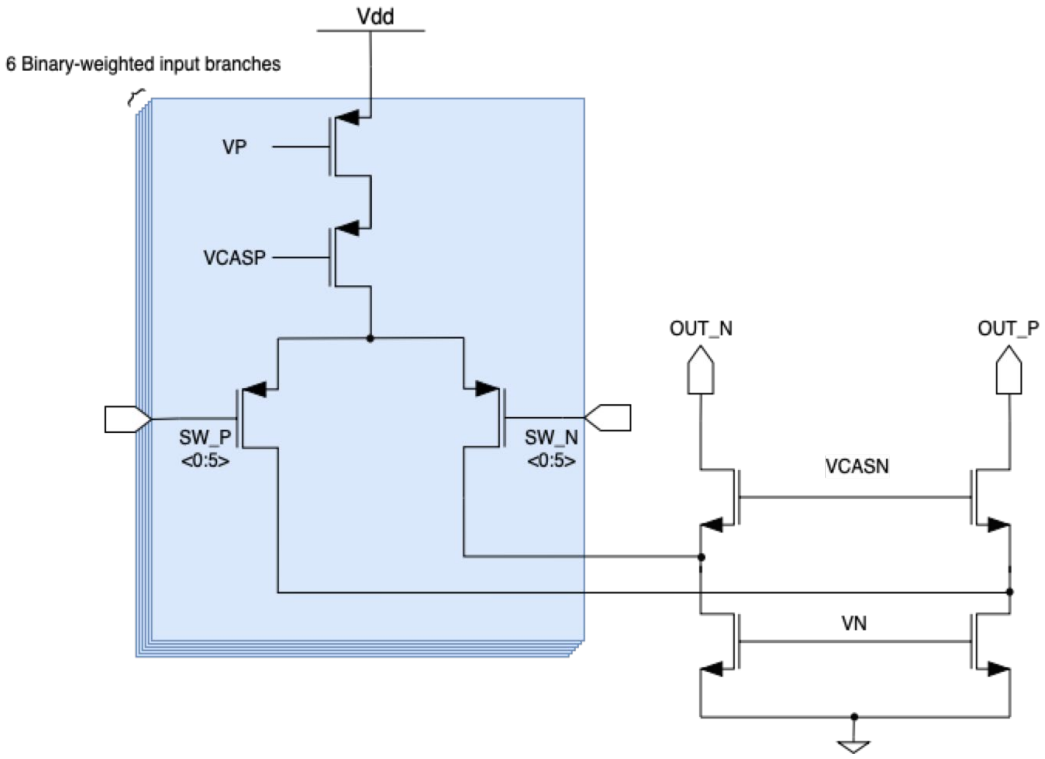

Figure 4.17: Six-bit Binary-weighted Input Branches are Connected to the Same Folded Branch

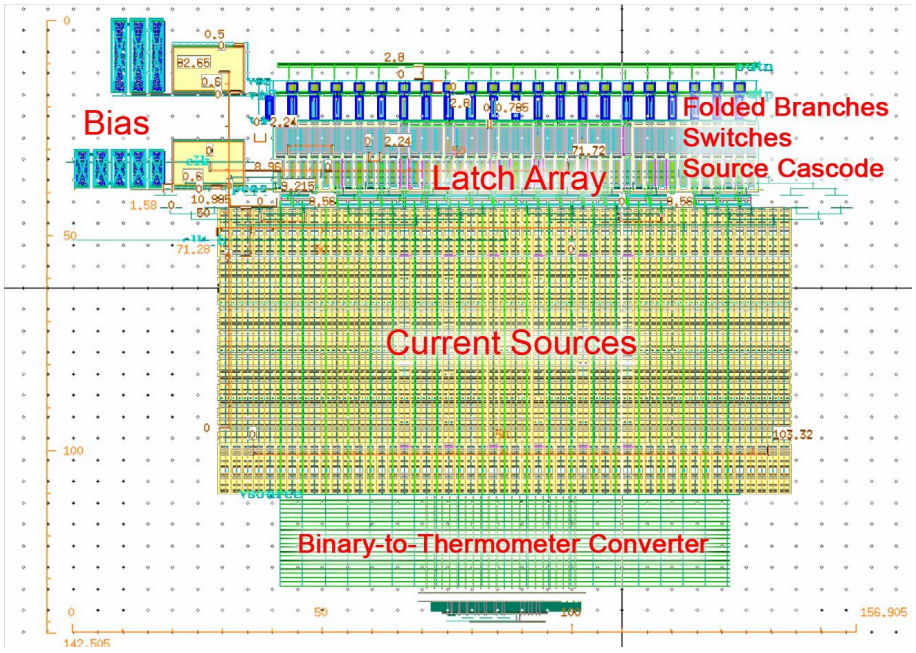

Figure 4.18: Layout of the Folded-cascode Current-steering DAC

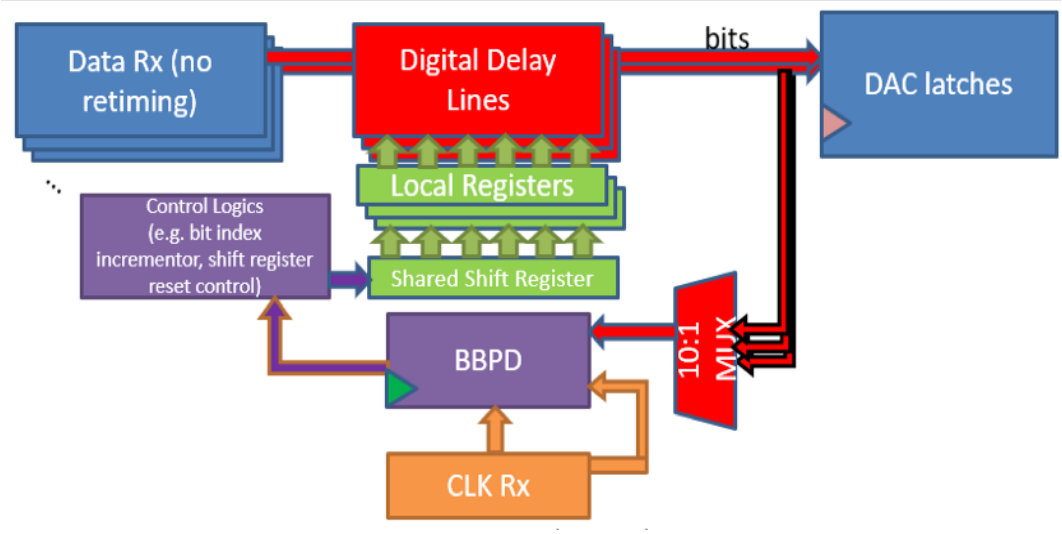

Figure 4.19: Block Diagram of Clock-Data Recovery (CDR) Circuit to Align the Bits

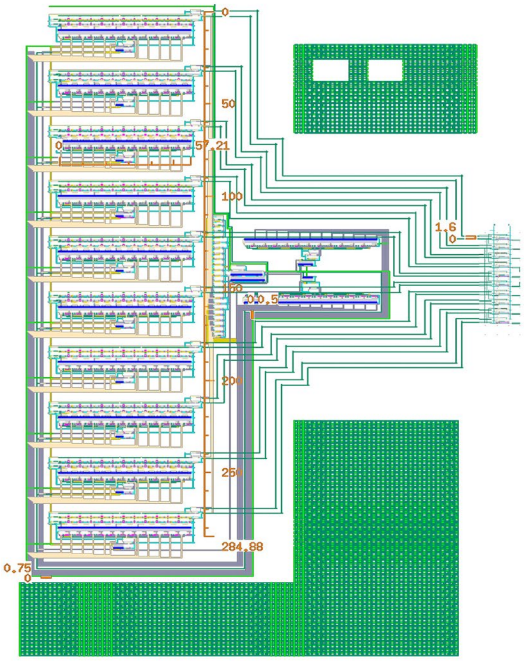

Figure 4.20: Clock-Data Recovery (CDR) Circuit to Align the Bits

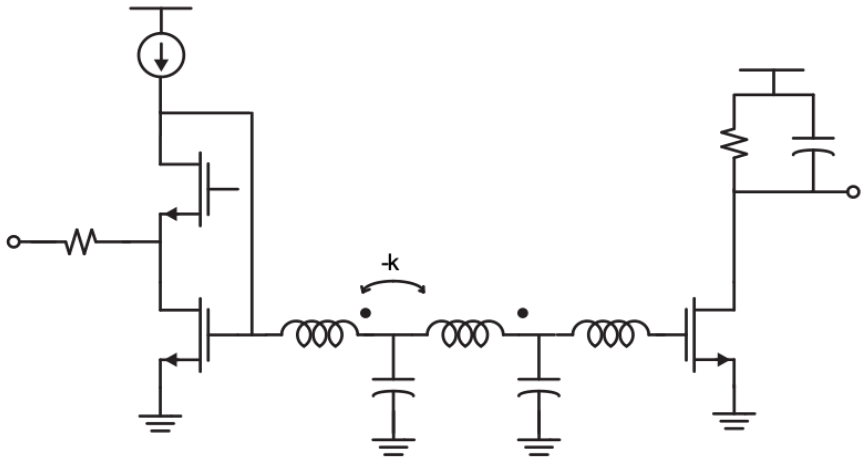

Figure 4.21: Current Mirror Filter Schematic.
The input is on the right-side, the output on the left.

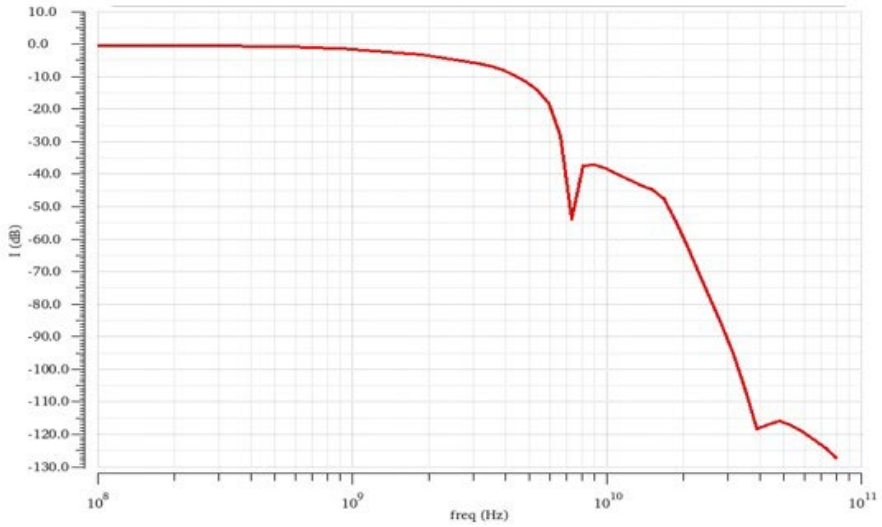

Figure 4.22: Current Mirror Filter Bode Plot
Note the zero from the m-derived sections.

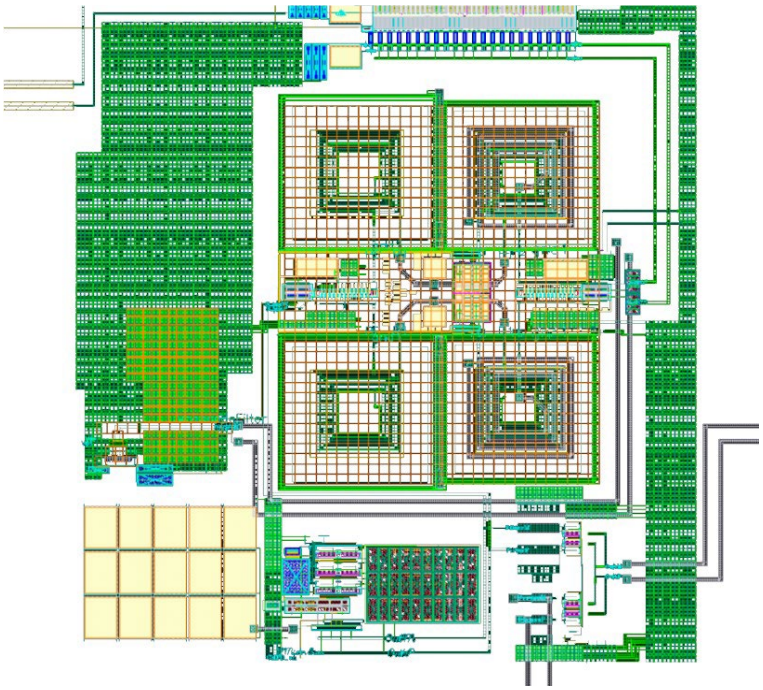

Figure 4.23: Layout of the Current Mirror Filter

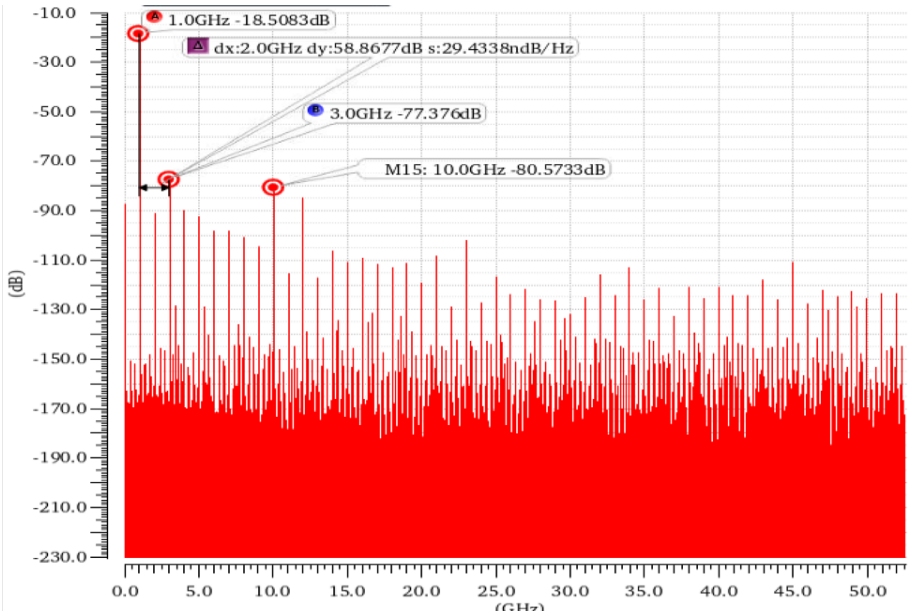

Figure 4.24: Simulation of the DAC with the Filter

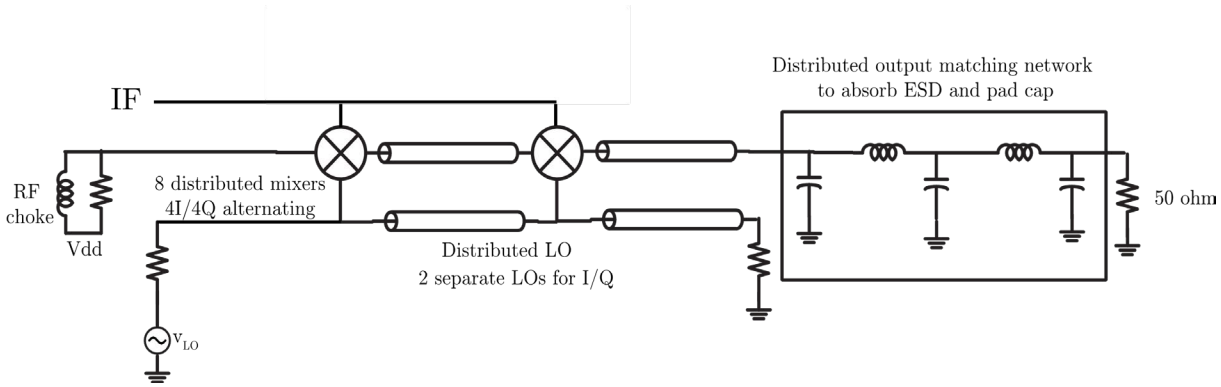

Figure 4.25: Distributed Mixer and Output Matching Network

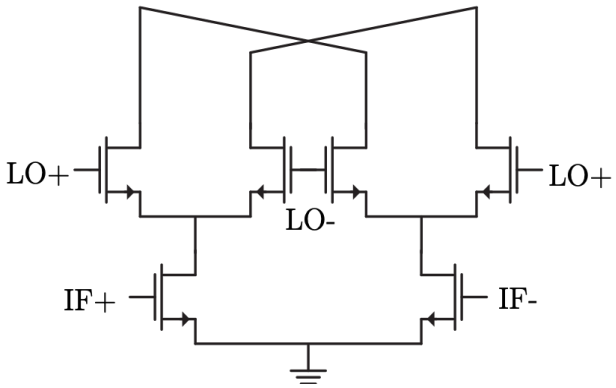

Figure 4.26: Double-Balanced Active Mixer Quad

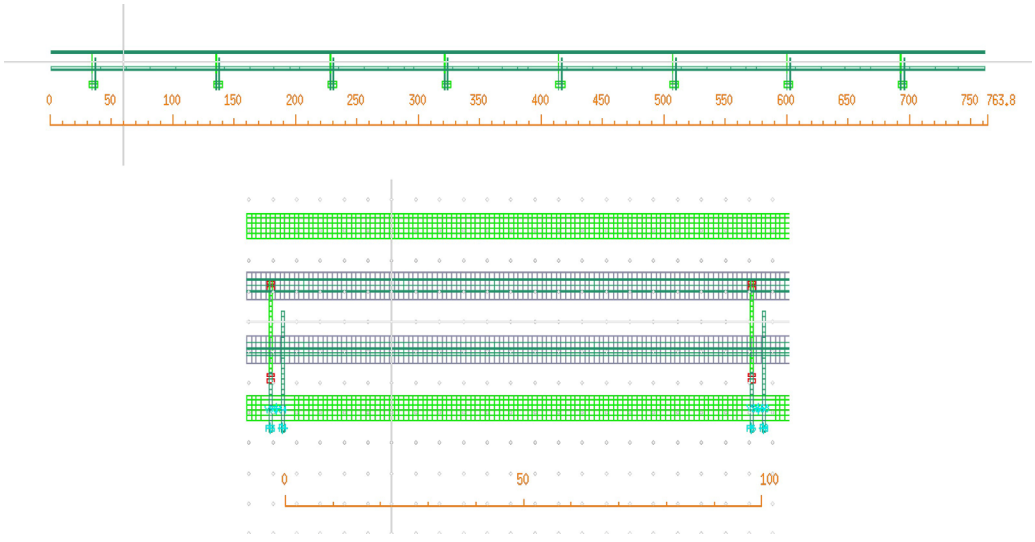

Figure 4.27: Distributed Mixer Layout

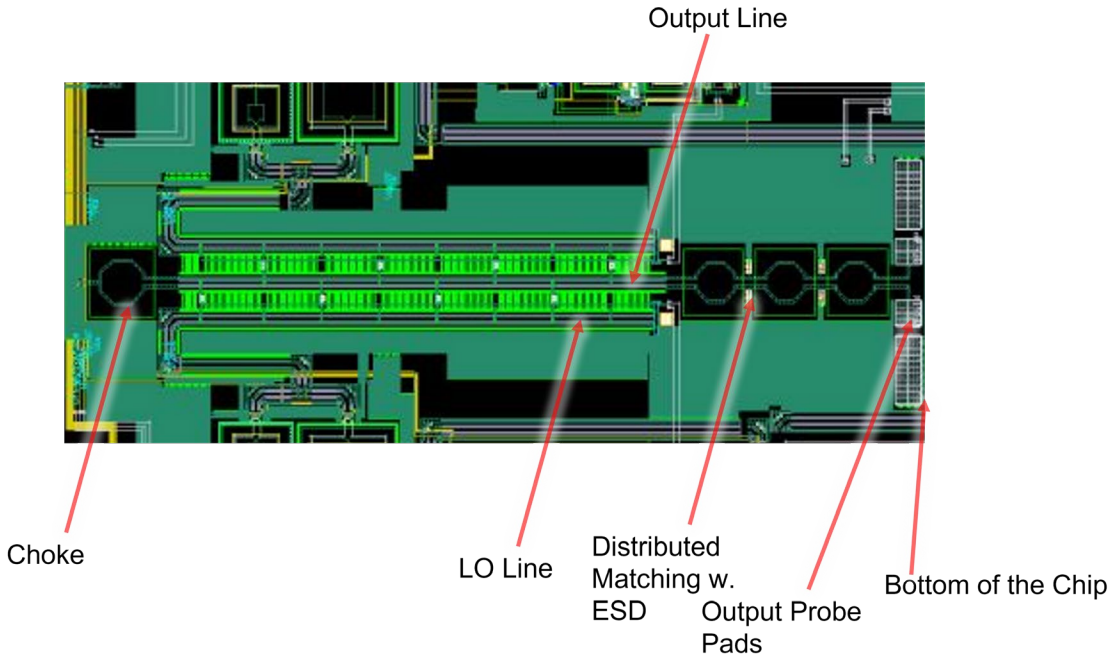

Figure 4.28: Distributed Mixer Layout on the Chip

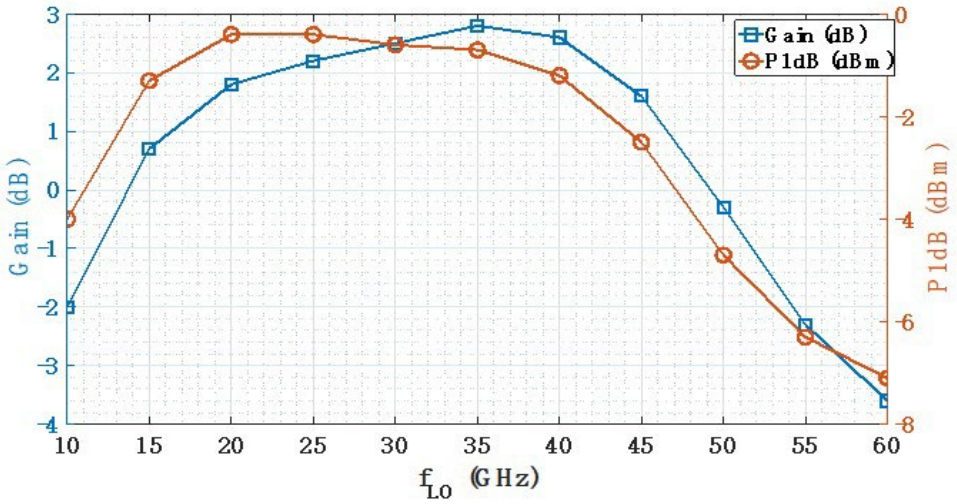

Figure 4.29: Simulated Distributed Mixer Gain

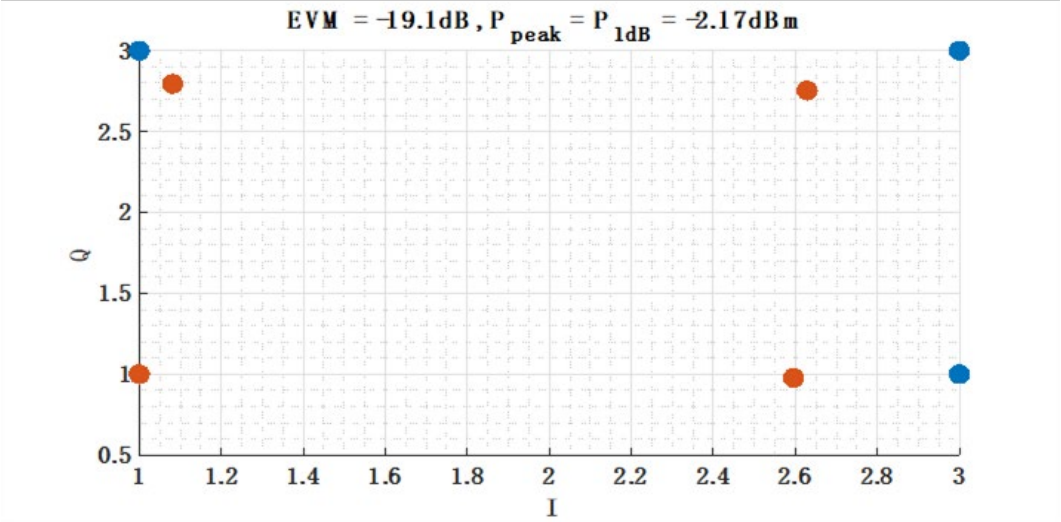

Figure 4.30: Distributed mixer with I/Q pulling at OP_{1dB}

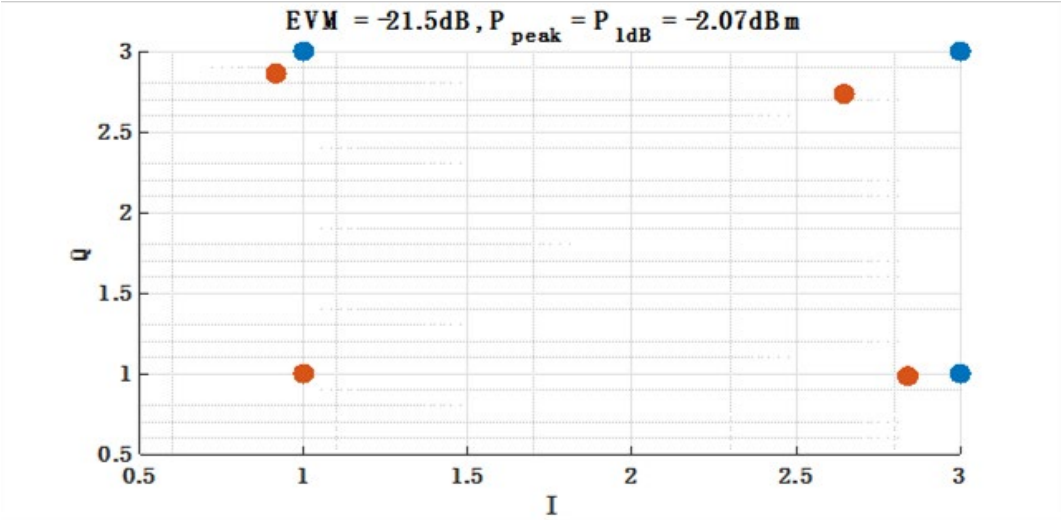

Figure 4.31: Distributed Mixer Without I/Q Pulling at OP_{1dB}

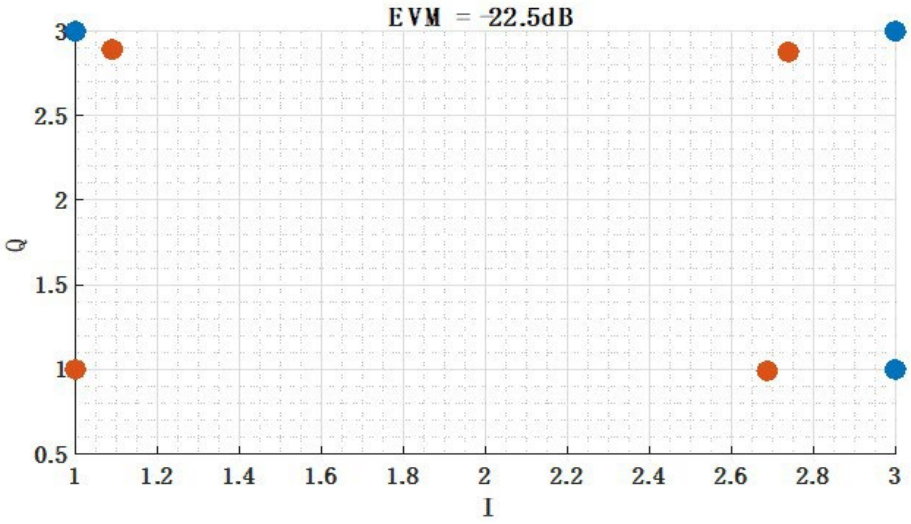

Figure 4.32: Distributed mixer with I/Q pulling at $OP_{0.5dB}$

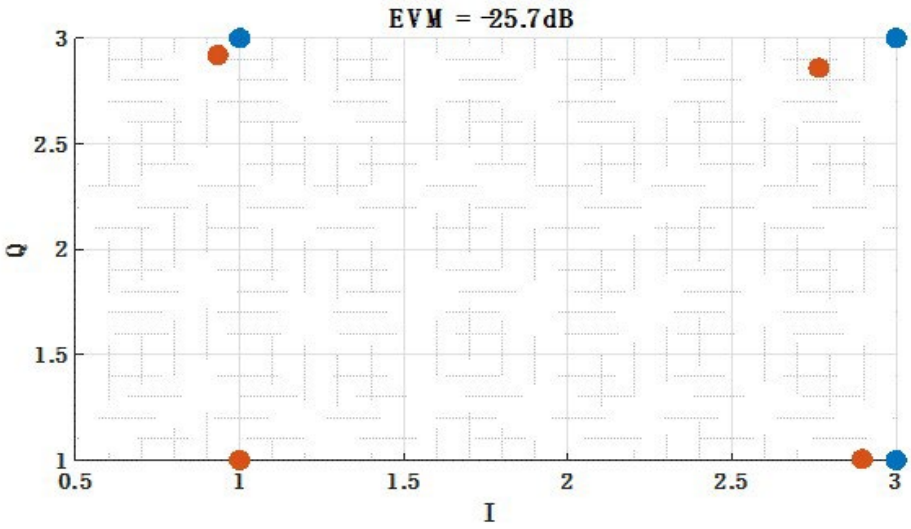

Figure 4.33: Distributed mixer without I/Q Pulling at $OP_{0.5dB}$

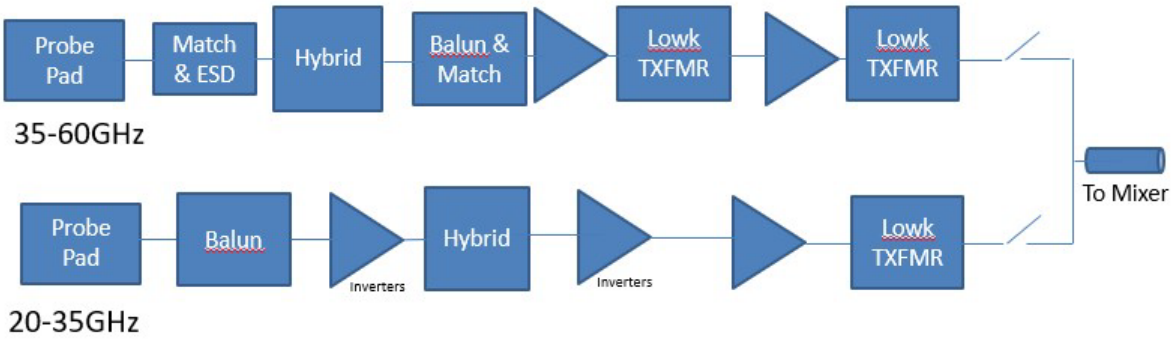

Figure 4.34: General Idea of the LO Chain

Low and high frequency amplifier paths, followed by a switch network to select the desired frequency band.The LO signal is then fed into the distributed mixer (the transmission line).

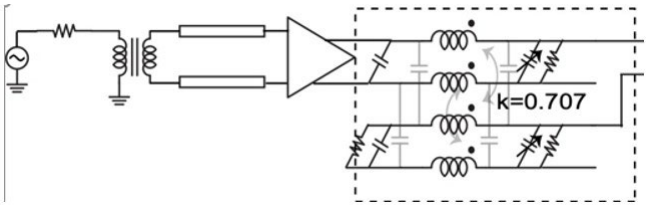

Figure 4.35: The Low Frequency LO chain, Prior to the Final Driver Stage

Note that the amplifiers are simply inverters). An artificial transmission line LC hybrid is based on [14], with 4 bit tuned capacitors.

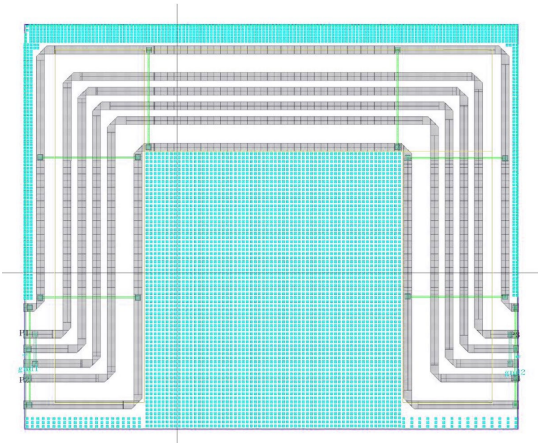

Figure 4.36: The Four Finger Lange Coupler

The dummy metal (blue) fills the surrounding regions to pass the difficult density DRC rules.

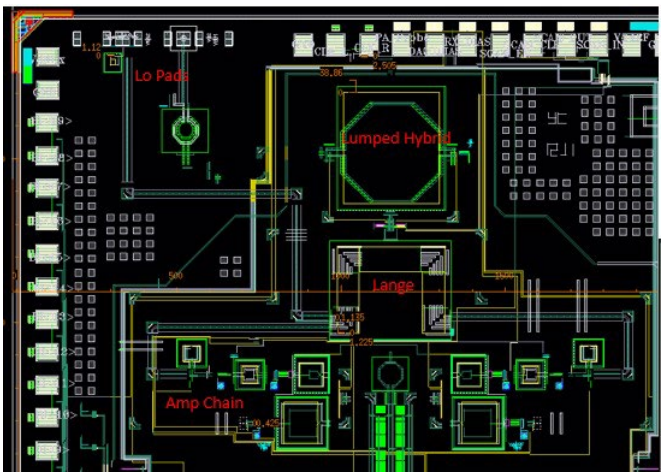

Figure 4.37: Complete layout of the LO Chains

The lumped and Lange hybrids are in the center of the chip, with the I/Q amplifier chains laid out symmetrically around the mixer.

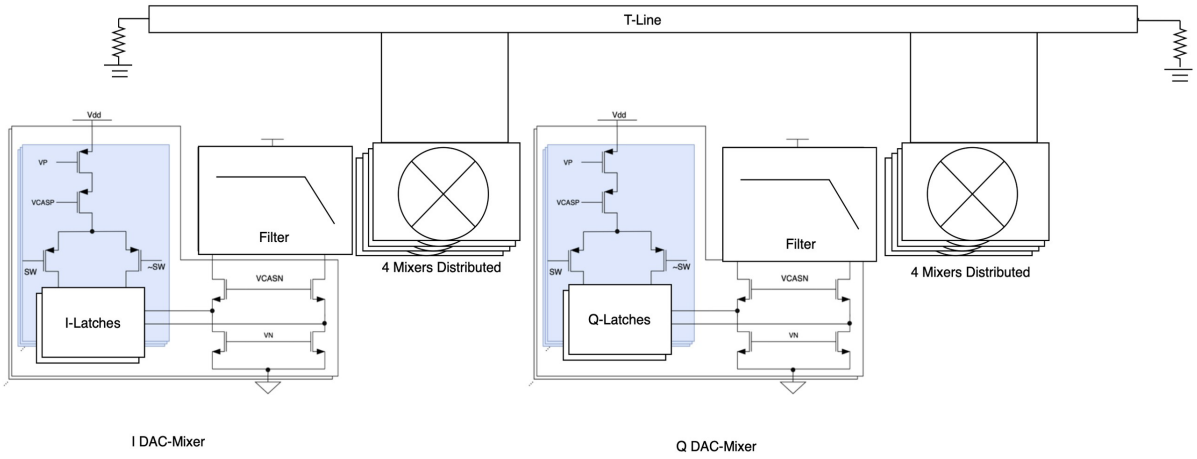

Figure 4.38: Architecture of the Transmitter

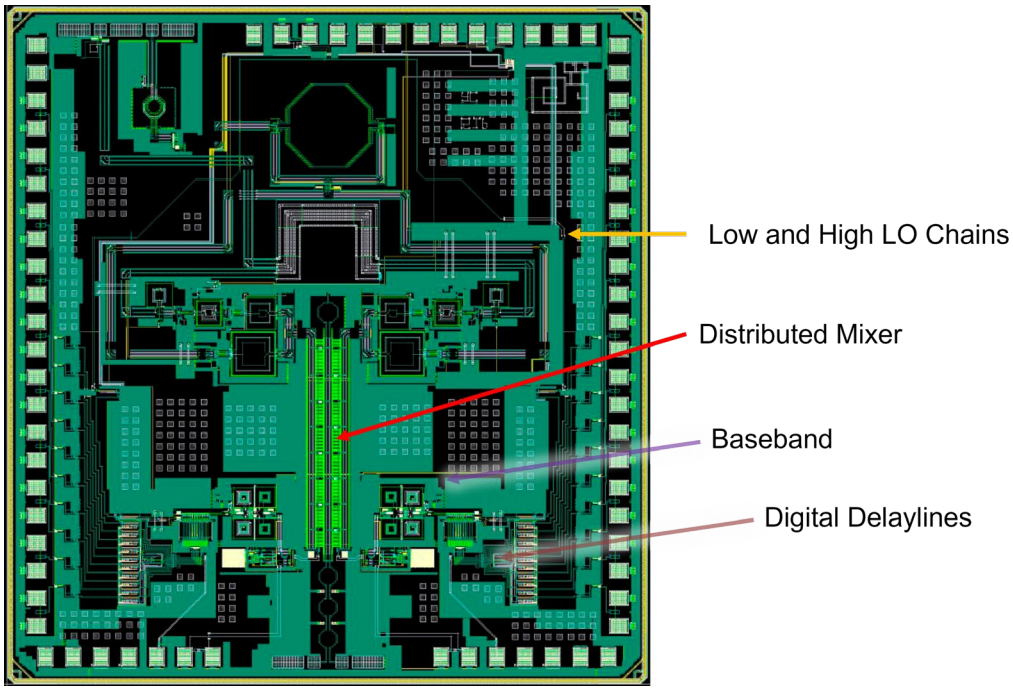

Figure 4.39: Layout of the Wideband Linear Transmitter

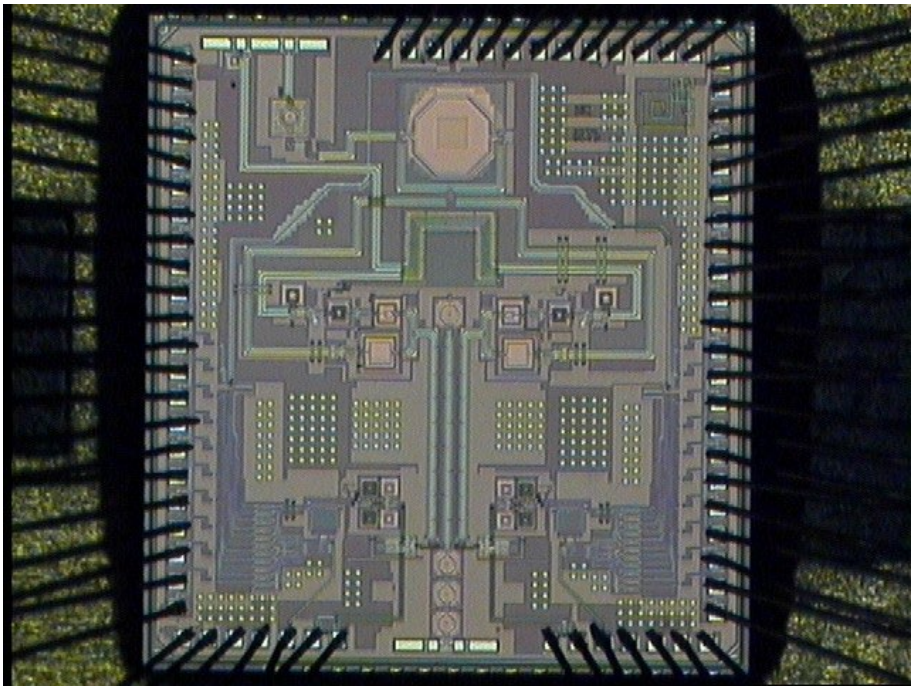

Figure 4.40: Die Photo of Wideband Linear Transmitter

5 COMPACT AND LINEAR DOHERTY POWER AMPLIFIER

5.1 Introduction

WiFi and 5G both use Orthogonal Frequency Division Multiplexing (OFDM) which has high peak to average power ratio due to the usage of multi-carriers in order to overcome the fading effects in the channel. Thus, the transmitters in general and the power amplifiers in particular operate most of the time at back-off power from it's saturated power. In order to decrease the average power consumption, the PA is required to have relatively high efficiency at this back-off power. Doherty PAs [38] use load modulation in order to achieve high back-off efficiency. Fig. 5.1 shows the block diagram of the conventional Doherty PA. It depends on power combining between two amplifiers, the main and the auxiliary, where at low input power the main amplifier will work and the auxiliary amplifier will be turned off. As the input power increases the auxiliary amplifier will start working and the impedance seen from the main amplifier will start to decrease due to the load modulation created by the quarter wavelength transmission line.

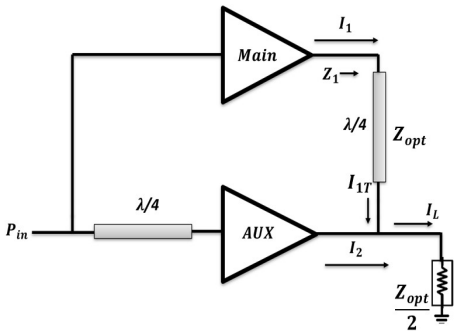

Figure 5.1: Block Diagram of the State of Art Doherty PA

The transmission line at the input of the auxiliary amplifier is required for in-phase power combining at the output. The high back off efficiency of Doherty PAs makes them good choice for 5G transmitters. However, there are many challenges that make Doherty PA not popular in today's 5G and mm-wave systems. First, Doherty PA requires a large area footprint for the two quarter wave length transmission lines and the two transformer baluns used for both the main and auxiliary amplifiers to have output matching and to transform the signal from differential to single ended at the output of each amplifier. In addition, the 90° phase shift created by the transmission lines is achieved at a single frequency, leading to the narrow band operation of the Doherty PA. Another big challenge is the non-linearities added to the system due to this load modulation. The proposed Doherty PA provides solutions for some of these challenges which will be discussed in the next sections.

5.2 Transformer Balun and Impedance Inverter

Fig. 5.2 shows the schematic of the proposed Doherty PA. Instead of using two baluns for each of the main and auxiliary amplifiers, a single balun is used and then the main and auxiliary amplifiers will combine differentially. After differential combining, differential impedance inversion is used for load modulation. The impedance inverter is composed of two stage LC sections (lumped transmission line model) in order to achieve the required 90° phase shift across a bandwidth higher than that of the distributed transmission line. The characteristic impedance of this lumped impedance inverter is designed to be Z_{opt}. Thus, if the impedance inverter has certain impedance Z_L at the inverter output, the impedance seen at the inverter input is:

$$Z_{seen} = \frac{Z_{opt}2}{Z_L} \tag{5.1}$$

The output balun will transform the load impedance from 50Ω to $Zopt/2$.

At low input power, the auxiliary amplifier is off, the impedance seen from the main amplifier will be:

$$Z_{main} = \frac{Z_{opt}2}{\frac{Z_{opt}}{2}} = 2Z_{opt} \tag{5.2}$$

As the input power increases beyond the back-off power, the impedance at the output of the impedance inverter will increase to Z_{opt} and the impedance seen from the main amplifier will be Z_{opt}.

Fig. 5.3 shows the layout view for the output transformer balun (imported into a 3D EM solver). The balun is 2:1 turns where the primary and secondary inductors are implemented at the top thick metal layers. The coupling between these inductors is maximized to decrease the loss of the balun which decreases the passive losses effect on the total efficiency for the PA. Fig. 5.4 shows the loss of the balun across frequency range from 20GHz to 30GHz.

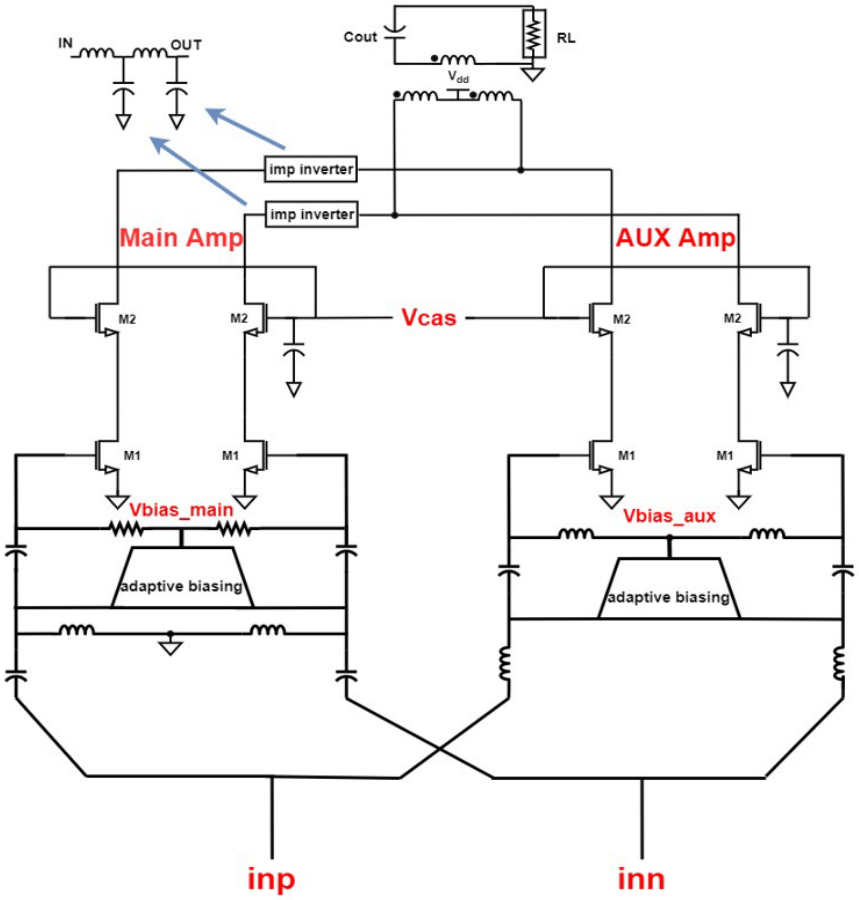

Figure 5.2: Schematic of the Proposed Doherty PA Output Stage

The main amplifier loadpull simulations show that in order to achieve the desired load modulation, the imaginary part seen from the main amplifier has to decrease with output power while the real part can be roughly constant across the Pout range. This is in contrast to lower frequency RF Doherty PA's where the real part of the load determines the output power. Fig. 5.5 shows the load modulation created by the impedance inverter. The impedance inverter is designed to allow the imaginary part seen by the main amplifier to decrease as the Pout is at 6dB back off from the maximum output power. The real part is almost constant until Pout of 20dBm which is close to the OP1dB of the PA.

5.3 Adaptive Biasing for EVM improvement

OFDM has high EVM requirements which requires the non-linearities of the Doherty to be improved. The main source of distortion in the Doherty PA is due to the variation of the gain of the auxiliary amplifier with the input power. In order to obtain a linear response for P_{out} against P_{in}, the Doherty PA should be designed in a way such that the summation of the P_{out} from both the main and auxiliary amplifier results in this linear P_{out} across P_{in}. To adjust the power contributions from both amplifiers, adaptive biasing should be used in both of them.

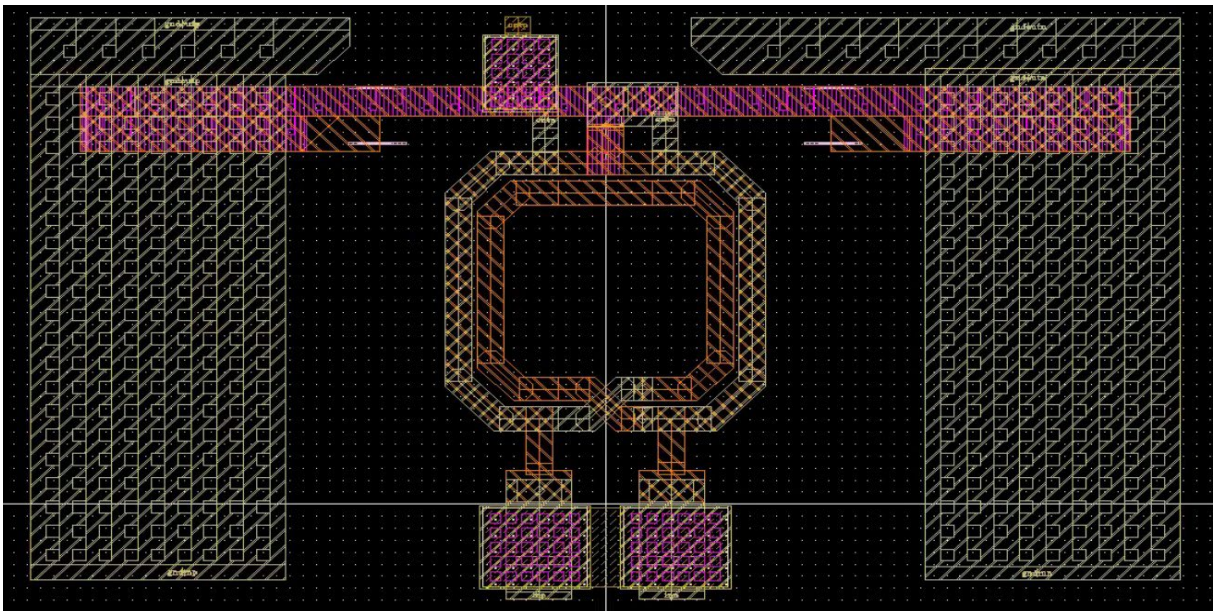

Figure 5.3: Layout for the Output Balun with Capacitors for Matching

5.3.1 Process Insensitive Power Detector for Adaptive Biasing

Fig. 5.6 shows the schematic of the proposed power detector which is based on the idea of having an amplifier in feedback to decrease the process variations. Transistors M1 and M2 in Fig. 5.6 are operating in triode region and are used as the sense resistors due to the process tracking requirements. The amplifier - as shown in Fig. 5.7 - has three terminals. The first two terminals

V_{detinp} and V_{detinn} are resistively coupled to the power amplifier inputs for power detection while the third terminal V_{inn} is the negative differential terminal. All three terminals are biased at V_{cm}. Devices M_{21} and M_{22} are both equally sized and the size of each device is half that of M_1. Thus, the currents I_1 and I_2 will be the same at low input power.

When the input power increases the DC components of current I_{21} and I_{22} will increase as shown in the following equation:

$$\frac{K}{2} I_2 = \frac{K}{2}(V_{cm} - V_{th} + A\cos(\omega t))^2 + (V_{cm} - V_{th} - A\cos(\omega t))^2 \quad (5.3)$$

$$2 I_{2,dc} = I_{cm} + K\frac{A}{2} \quad (5.4)$$

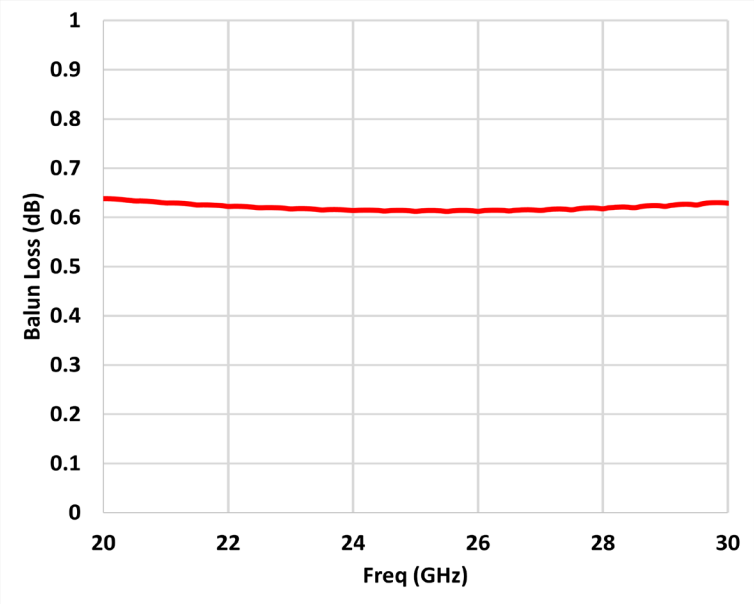

Figure 5.4: Balun Loss Across Frequency

where $K\frac{A_2}{2}^2$ is the small-signal AC current of I_2. Since the amplifier is in feedback, the currents I_1 and I_2 have to be equal.

$$I_{2,ac} = I_{1,ac} = K\frac{A_2}{2} \tag{5.5}$$

$$I_{1,ac} = g_m \times v_{inn} = K(5.6)\frac{A_2}{2}$$

$$v_{inn} = \frac{KA^2}{2g_{mn}} = \frac{A^2}{2(V_{gs} - V_{th})} \tag{5.7}$$

$$v_{detout} = \frac{A_2}{2(V_{gs} - V_{th})}(1 + \frac{R_2}{R_1}) \tag{5.8}$$

Since V_{gs} tracks V_{th}, the detector output will be process independent. Fig 5.8 shows that the detector output voltage has very low variations across Process/Voltage/Temperature (PVT).

Fig. 5.9 shows P_{out} from both the main and the auxiliary amplifiers. It can be shown that at low P_{in}, the output power contribution is mainly from the main amplifier only. However, the adaptive biasing role is to make the P_{out} slope for the auxiliary amplifier higher than the P_{out} slope for the main amplifier. As a result, the P_{out} from the main and auxiliary amplifier will be almost the same at maximum P_{in} leading to in-phase combining with equal contributions.

5.4 Driver Stage

In order to achieve the high gain requirements for a PA working for 5G system and to allow the required P_{in} to drive the Doherty output stage, a driver stage is needed. Unlike the Doherty PA, which works with 1.8V supply, the driver stage uses 1V power supply in order to enhance the overall efficiency. Fig. 5.10 shows the schematic of the driver stage which is composed of simple neutralized differential pair.

5.5 Post Layout Simulation Results

Fig. 5.11 shows the top level layout for the 2-stage Doherty PA fabricated in Global Foundaries 45RFSOI. The area of the chip is 400μm × 800μm excluding the pads area. A Ground-SignalGround (GSG) probe is used for the output while GSGSG probe is used for the input with 150μm pitch for each probe.

EMX, a 3D electromagnetic solver tool, is used for all the electromagnetic simulations. This PA achieves high bandwidth, from 23GHz to 28GHz, relative to published Doherty PAs for 5G applications. Fig. 5.12 and Fig. 5.13 shows that the PA achieves peak PAE greater than 35% across the entire BW in addition to PAE of 30% at the average Pout of 18dBm. Fig. 5.14 shows the power gain of more than 20dB across P_{out} for multiple frequencies. Fig. 5.15 shows that the proposed PA achieves P_{sat} of greater than 21 dBm and Op1dB of greater than 19 dBm. Finally, Fig. 5.16 shows the s-parameters of the PA, which shows flat gain response across the entire BW.

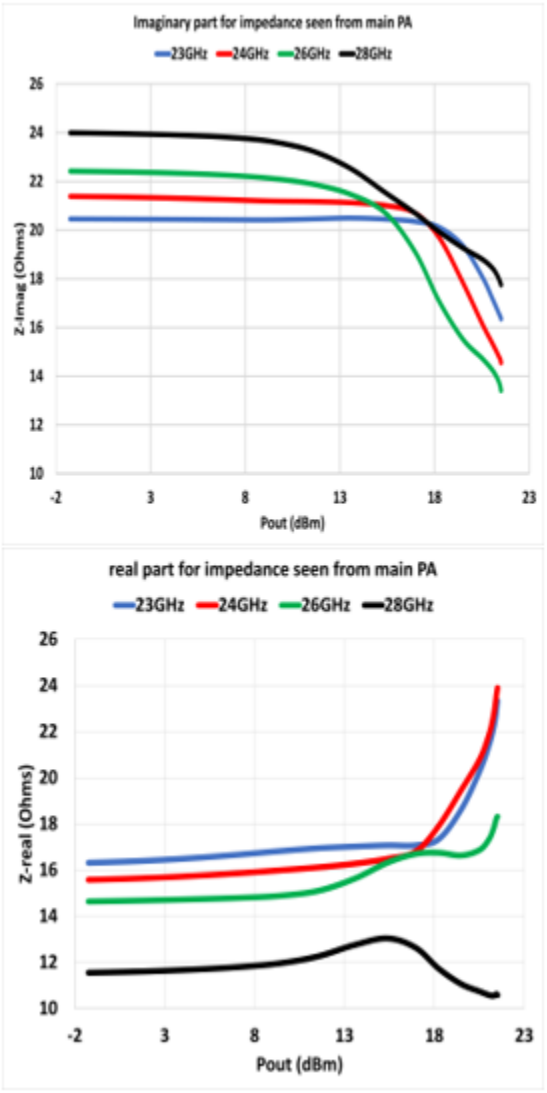

Figure 5.5: Imaginary Impedance Seen from Main Amplifier (a), (b) Real Impedance seen from Main Amplifier

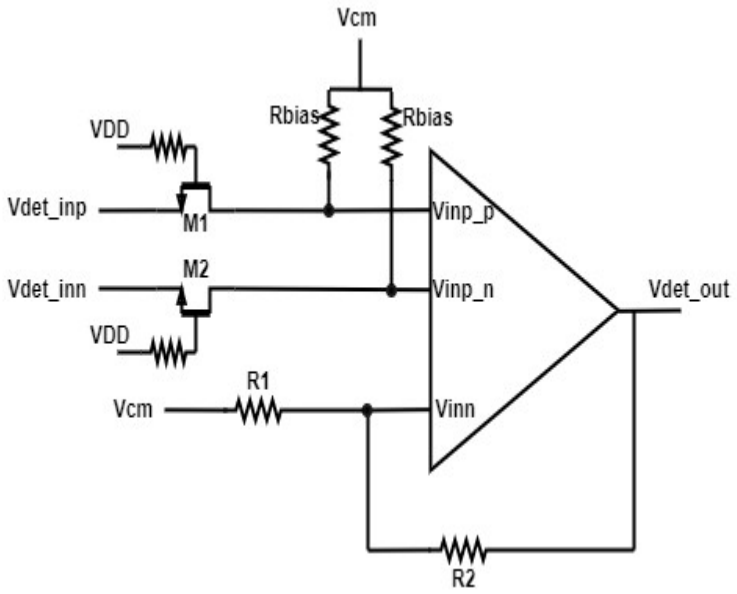

Figure 5.6: Power Detector Block Diagram

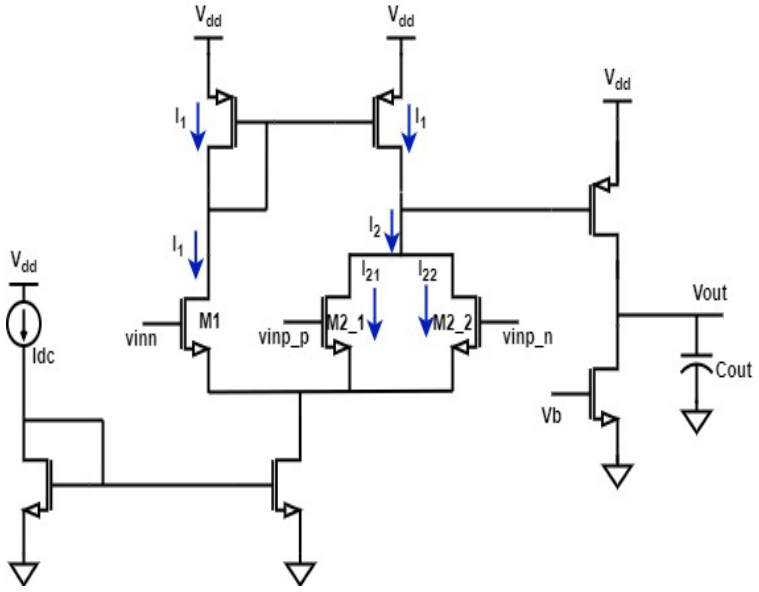

Figure 5.7: Three Terminal Amplifier for Power Detection

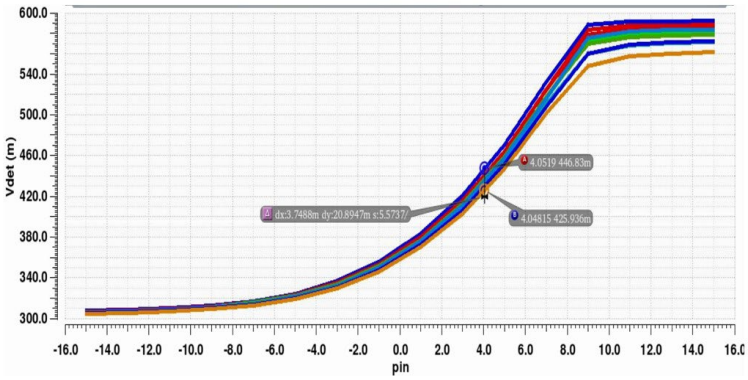

Figure 5.8: Detector DC Output Voltage Across P_{in} and PVT

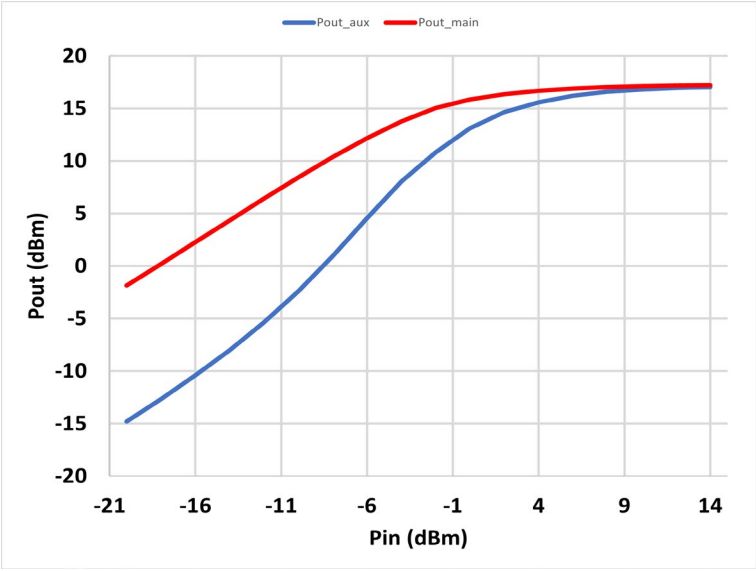

Figure 5.9: P_{out} from the Main and Auxiliary Amplifiers Across P_{in}

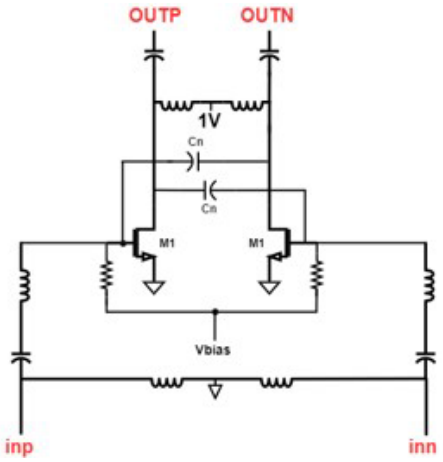

Figure 5.10: Schematic of the Driver Stage

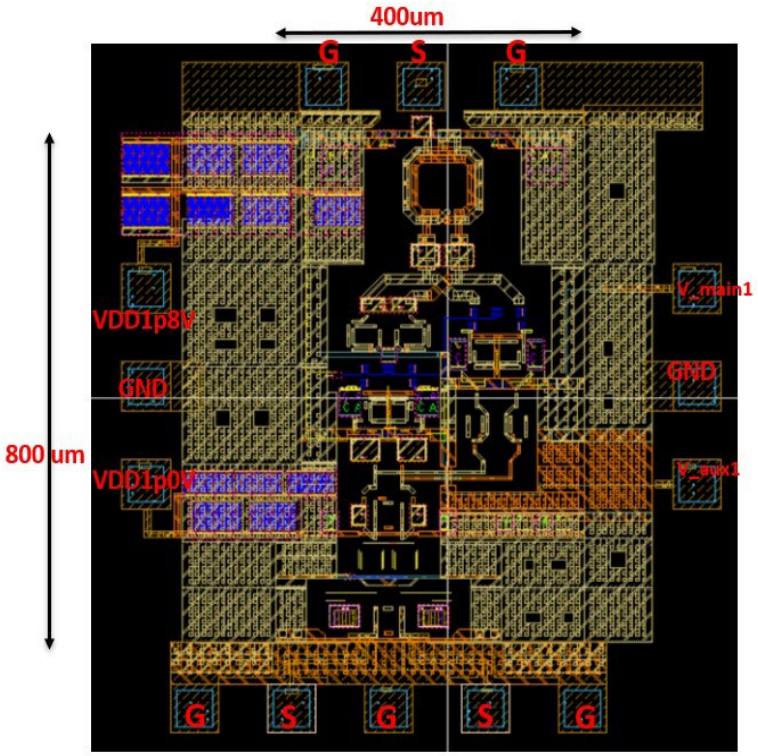

Figure 5.11: Layout View for the 2-stage Doherty PA

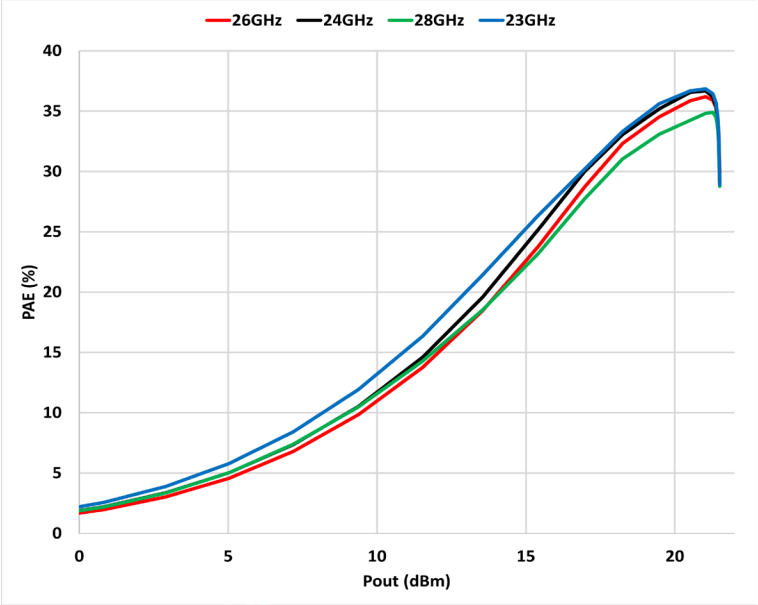

Figure 5.12: PAE Across P_{out} at Multiple Carrier Frequencies

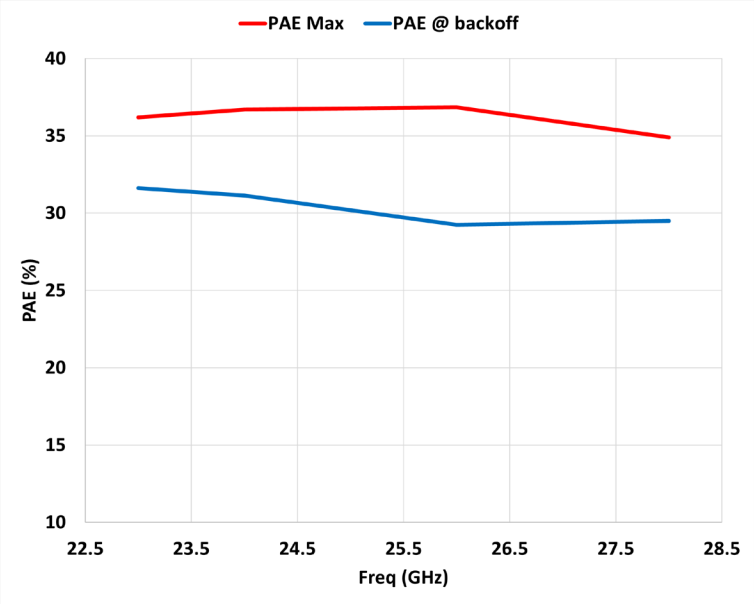

Figure 5.13: PAE at P_{sat} and at P_{avg} Across Frequency

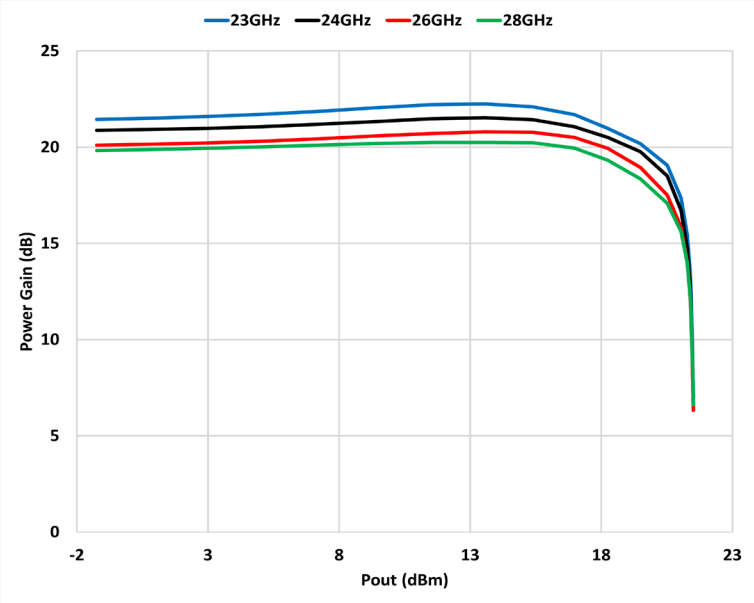

Figure 5.14: Power Gain Across P_{out} at Multiple Carrier Frequencies

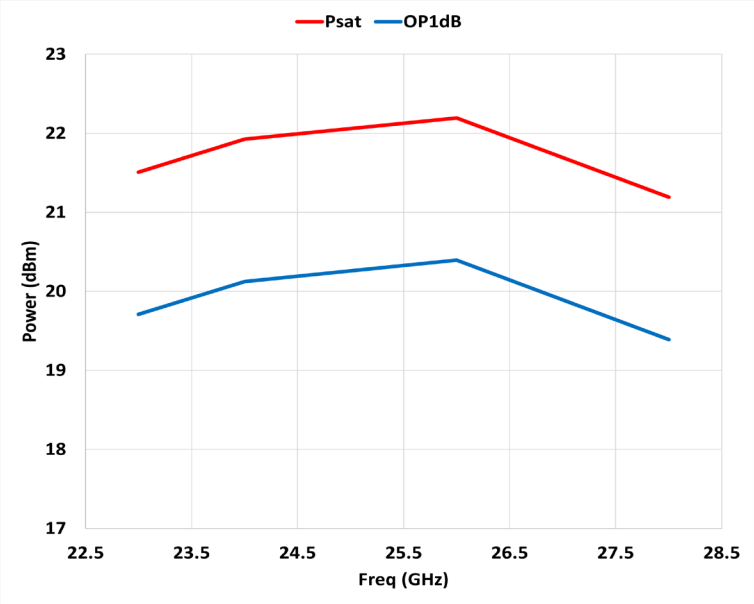

Figure 5.15: P_{sat} and OP1dB Across Frequency

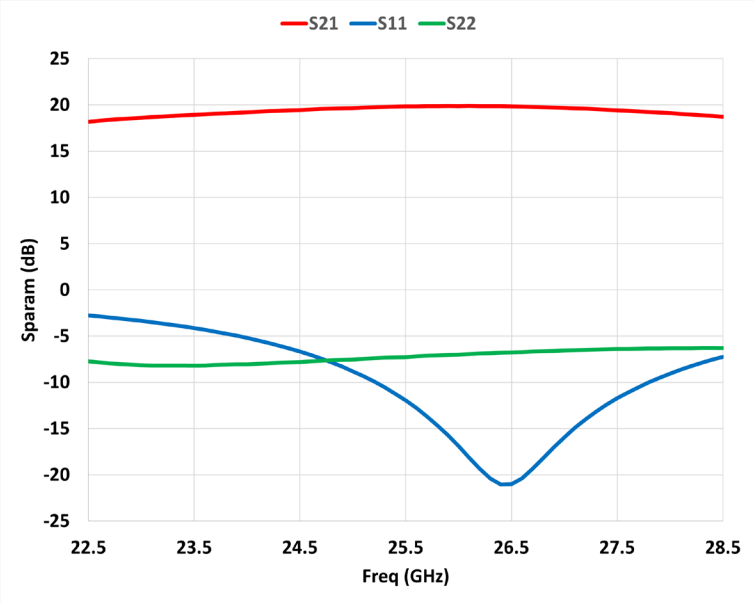

Figure 5.16: Small-signal S_{21}, S_{11} and S_{22} of the Doherty PA

6 SWR ROBUST WIDEBAND LOAD MODULATED BALANCED AMPLIFIER

In this section we investigated the Load Modulated Balanced Amplifier (LMBA) and its sensitivity to antenna VSWR variation when used as a PA. An alternative topology, the orthogonal load modulated balanced amplifier (OLMBA) is suggested as a more VSWR insensitive alternative. A prototype was then fabricated in August, 2022 in 28nm CMOS.

6.1 Introduction to the Load Modulated Balanced Amplfier (LMBA)

The LMBA topology is shown in figure 6.1. First published by Shepphard, Powell, and Cripps, the LMBA provides active load modulation over a wide bandwidth. The large bandwidth is easy to see: the use of coupled-line hybrids provides wideband performance. The load modulation is provided by the control signal at port (3) in Fig. 6.1. It can be shown [35] that the resulting impedance seen by each PA is given by:

$$Z_2 = Z_4 = Z_o\left(1 - 2\frac{\sqrt{I_c e^{(j\varphi)}}}{I_b}\right) \tag{6.1}$$

where Z_o is the hybrid's characteristic impedance, I_c is the control current, with phase φ relative to I_b, the current from each transistor. This is a useful feature of the LMBA as the control signal can be used either to help match the PA to the antenna across various settings, or as a means to change the PA load impedance over back-off conditions, similar to a Doherty PA, as seen in [9].

6.2 LMBA Sensitivity to Antenna VSWR

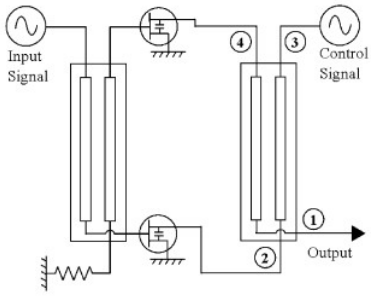

Figure 6.1: The LMBA [35]

For mobile communication, sensitivity to the antenna impedance variations is an important consideration, as the antenna can vary up to 2:1 VSWR. In this section we will consider the case where the antenna has an impedance Z_L, not necessarily equal to the Z_o of the hybrid. We will also account for the control port impedance, represented by Z_c. We will use the same port convention as Fig. 6.1. Assume an ideal hybrid, with Z matrix seen in figure 6.2. We can solve for the currents and voltages at each port with load Z_L with some algebra, as follows:

$$V_1/Z_o = -I_1 Z_L = jI_3 - j\sqrt{2}I_4$$

$$V_3/Z_o = jI_1 - j\quad 2I_2 = V_{ctrl} - I_3Z_c$$

$$\sqrt{}$$

$$-I_1Z_L = jI_3 - j\quad 2I_4$$

$$\sqrt{}\qquad Z_o$$

$$I_1 = [j\quad 2I_4 - jI_3]\ \frac{}{Z_L} \tag{a}$$

$$\sqrt{}$$

$$V_4 = Z_o[-j\quad 2I_1 + jI_2]$$

$$\sqrt{}\ \sqrt{}$$

$$V_4 = Z_o[-j\quad 2(\ 2I_4 - I_3)Z_o/Z_L + jI_2]$$

$$\sqrt{}\quad Z_o$$

$$= Z_o[(2I_4 -\quad 2I_3)\ \frac{}{Z_L} + jI_2] \tag{b}$$

Now solve for I_3 :

$$\text{p}\qquad\qquad \sqrt{}\qquad Z_o\quad \sqrt{}$$

$$V_3 = Z_o[jI_1 - j\quad (2)I_2] = Z_o[j(j\quad 2I_4 - jI_3)\ \frac{}{Z_L} - j\quad 2I_2] = V_{control} - I_3Z_C$$

$$\sqrt{}\qquad Z_o\quad \sqrt{}$$

$$Z_o[(-\ 2I_4 + I_3)\ \frac{}{Z_L} - j\quad 2I_2] = V_{ctrl} - I_3Z_c$$

$$\frac{-Z_o^2}{Z_L}\sqrt{2}I_4 + \frac{-Z_o^2}{Z_L}I_3 - Z_o\sqrt{2}I_2 = V_{ctrl} - I_3Z_c$$

$$Z_o2\qquad\qquad \sqrt{-}\quad Z_o^2\quad -\sqrt{}$$

$$I_3(Z_c + \quad) = V_{ctrl} + jZ_o\quad 2I_2 + \frac{}{\sqrt{Z_L}}\ 2I_4$$

$$Z_L\qquad\sqrt{}\qquad\sqrt{}$$

$$V_{ctrl} + Z_o[j\quad 2I_2 + \underline{ZZ_{Lo}}\ 2I_4]$$

$$I_3 = \qquad\qquad (Z_c + \underline{ZZ_oL2}) \tag{c}$$

We can find the impedance at port 4 by finishing up for V_4 and then plugging (c) into (b) :

$$\sqrt{}\qquad\sqrt{}$$

$$\sqrt{}\quad V$$

$$\underline{Z_o}\qquad -\quad 2(\underline{\ ctrl + Z_o[j\quad 2I_2 + ZZ_{Lo}\ 2I_4}]))+ jI_2]$$

$$V_4 = Z_o[Z_L(2I_4\qquad\qquad (Z_c + \underline{ZZ_oL}\ )$$

$$Z_o$$

Define $\chi = \frac{}{Z_L}$, and substitute in the values $I_4 = jI_B$, $I_2 = -I_B$

$$\sqrt{}\qquad\sqrt{}$$

$$\frac{V_4}{(Z_c + Z_o\chi)I_4} = 2\chi - 2\chi\left[\frac{\sqrt{}\quad V_{ctrl} + Z_o(j\quad 2I_2 + \chi\ 2I_4)}{}\right] + jI_2/I_4\, I_4 Z_o$$

$$= 2\chi - \quad 2\chi\left[\frac{\sqrt{\quad V_{ctrl} + Z_o j\quad 2I_B(\chi - 1}}{jI_B(Z_c + Z_o\chi)}\right] - I_B \qquad \text{(d)}$$

Now to solve for impedance at port 2:

$$V_2/Z_o = -j\quad \sqrt{\quad 2I_3 + jI_4}$$

$$\frac{V_2}{I_2} = Z_o\left[\frac{j\quad 2I_3}{-I_B} + 1\right], \qquad \text{(e)}$$

where I_3 is given by (3)

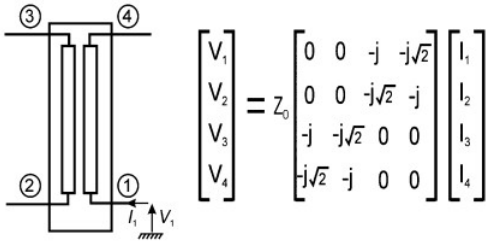

Figure 6.2: Ideal Hybrid Coupler Matrix

The impedance seen by each PA can be seen in equations (d) and (e) for ports 4 and 2 respectively. The exact solutions are not important so much as that it shows a dependence on the load matching for port 4. Interestingly, port 2 remains insensitive to load mismatch. Unfortunately the impedance seen in the other ports can become negative, leading to potential instability, as seen in Fig. 6.3. This limits the LMBAs possible impedance modulation properties to only a few select control conditions, greatly hampering its practical use.

6.2.1 The Balanced Amplifier

A look at how the traditional balanced amplifier fares over load mismatch is a worthwhile endeavour. It can be shown that in the balanced amplifier, the impedances seen by each PA vary as

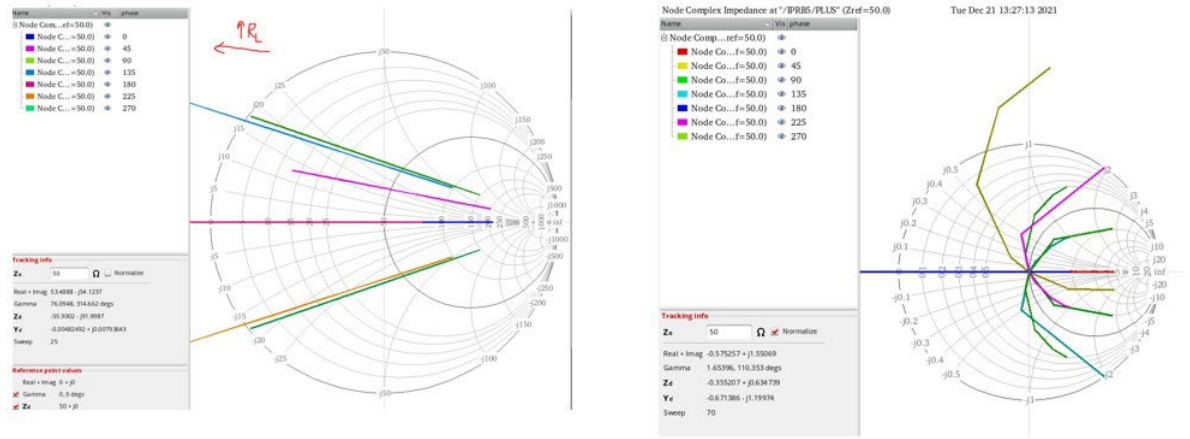

Figure 6.3: Impedance Variation seen by the PAs (left) and the Control Port (right), for Varying Antenna VSWR (from 1:2 to 2:1), Over Varying Control Conditions
Note the arising instability issues.

follows [11], where Z_1, Z_2 are the impedance seen by the balanced PAs:

$$Z^1 = \frac{\Gamma}{\Gamma - 1} \tag{6.2}$$

$$Z^2 = \frac{\Gamma}{\Gamma + 1} \tag{6.3}$$

The key thing to note here is that as the load VSWR varies, one PA sees a lower impedance, whereas the other sees a higher impedance; the net result is that the overall PA output power can be made relatively constant over various load mismatches, as the PA with the lower impedance at its output can supply more to compensate for the PA with a higher impedance at its output.

6.3 Orthogonal LMBA

The first paper on the orthogonal LMBA was published by Cripps et. al [10]. The schematic is shown in figure 6.4 [10].

In the OLMBA, the control signal is now applied to the input hybrid instead of the output hybrid. The output hybrid thus looks essentially like the balanced amplifier, except that instead of matching the isolation port to Z_o, a reactive load is applied. This reactive load provides active load modulation, as the control signal causes a slight imbalance to the balanced PAs, which then gets reflected at the reactive port, mimicking the LMBA. The load modulation can be seen in Fig. 6.5.

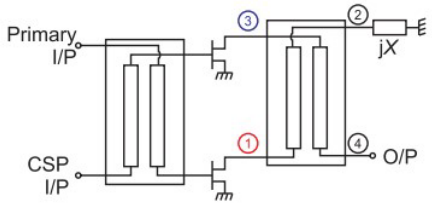

Figure 6.4: The Orthogonal LMBA [10]

Note it is similar to the normal LMBA, except that the control current is applied at the input hybrid, and the output isolation port is replaced with reactive load Jx.

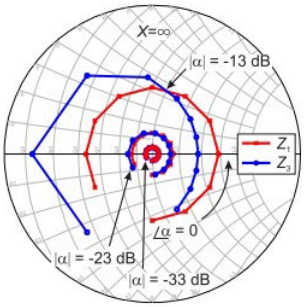

Figure 6.5: Example of Varying Control Power and Phase and its Affect on PA Drain Impedance

Note that because the control is added to the input, a lower control power is required since it gets amplified by the Pas.

6.3.1 OLMBA Outptut Power Over Load Variation

A balanced PA, and OLMBA with open/short loads (instead of the reactive load) was simulated to observe it's robustness to load impedance variation. The results for the OLMBA are seen in figure 6.6; for reference, when the Pas are placed in the standard balanced configuration, the output power remains fairly flat at 20dBm across the 2:1 VSWR change (figure 6.7). In figure 6.6, the output power is shown for two cases: open and short (on the output isolation port); we can see then that by switching between the open and short conditions, as the impedance we can choose the more optimal setting, while still providing the reflections needed for load modulation.

6.4 Implemented PA

We have seen that the orthogonal LMBA can provide a constant output power similar to the balanced 87tructure over load mismatches, while potentially also offering active load modulation for the individual Pas. The proposed schematic is shown below, in Fig. 6.8.
The overall PA contains two PA sub-blocks, two hybrids, a switch, ac-coupling capacitors, and an impedance transformer. The impedance transformer provides a 4:1 impedance match, translating the impedance from a nominal 50 ohms at the antenna to 12.5 ohms. The output hybrid is thus designed at a characteristic impedance of 12.5 ohms as well. The input hybrid is the standard 50 ohms. The switch provides the open/short isolation port load necessary for load modulation. Each PA block is a standard cascode-type PA cell.

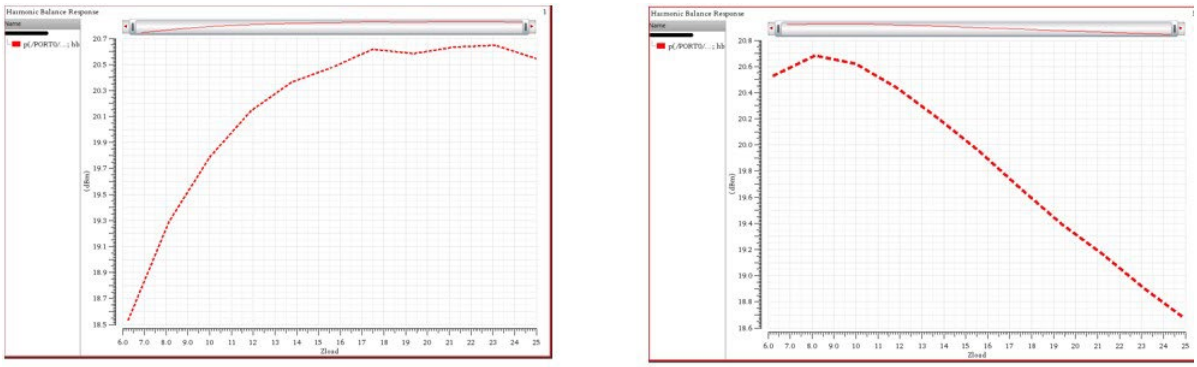

Figure 6.6: Power Gain of the PA when the Isolation Port of the Output Lange Coupler is Open (left) and Short (right)

A simple switch therefore will allow for more optimal performance based on the VSWR.

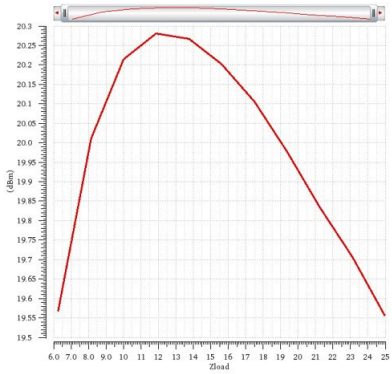

Figure 6.7: Output Power when the Pas are Placed in the Balanced Configuration

Note the output power varies by < 1Db across the full VSWR range.

6.4.1 Passives Design

We can see that the PA relies heavily on the passives. There are two important factors in the passive design to note: first that they must be wideband (as that is the primary benefit of the LMBA in the first place), and second, they need to meet electro-migration and other reliability concerns required for PA design. Obviously low loss is critical for 88tructure88 as well. In this section we will go over the design of the critical components.

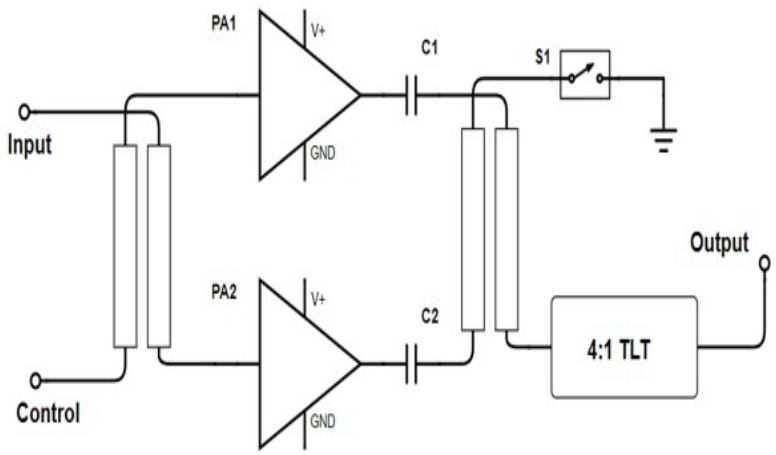

Figure 6.8: Top Level Schematic for the Overall PA

Output 12.5 ohm Lange Coupler The output hybrid was designed with the 6 finger Lange Coupler topology as well. First, a coplanar 89tructure was chosen over the microstrip equivalent, as the small height from the substrate to the top metal layers made it impossible to simultaneously achieve the low odd-mode impedance and high even-mode impedance in microstrip form. Coplanar-type structures provide a higher odd-mode impedance by lengthening the return path (effectively increasing the unit capacitance). Unfortunately these type of structures (with multiple fingers) need to be solved using EM simulators, as there are no closed-form equations. A six finger structure was used because the standard 4 fingers did not provide enough odd-mode capacitance to achieve the desired 3Db coupling-even with the 6 fingers, the traces are placed with near minimum DRC rule spacing, as seen in the layout Fig. 6.9. Increasing the numbers of fingers further would not only add additional area, but also cause a variety of DRC errors common to most digital CMOS processes, namely density and total "inductor" area limits. For lifetime considerations, the top two metal layers were used in parallel to handle the large PA currents (as well as increase coupling). The structure was simulated using a 3D EM simulator (EMX). The results are shown in figure 6.10, showing < 1Db amplitude mismatch from roughly 30 to 70GHz and around 1Db of insertion loss.

Ruthroff Impedance Transformer Two provide a broadband, 4:1 impedance transform, a Ruthroff transmission-line transformer structure was utilized. This is shown in the Fig. 6.11[7]. The operation of this structure can be thought of as follows: consider the coupled line as a coupled inductor; an applied input current through line *A* will produce a coupled current in the opposite direction on line *B*. This means the current through node 2 is twice as large as that through node 1. As this is a passive element, to maintain power balance, this means the impedance at node two must be 4 times smaller than that at node 1. The bandwidth of this structure is maximized with greater coupling between the two lines. To that end, a six finger Lange coupler is utilized (whose characteristic impedance is the geometric mean of the two ports, in this case 25 ohms). The layout can be seen in Fig. 6.12. Note that two thick metal traces and wide widths are utilized to meet EM requirements for ~200mA of AC current over ten years of operation (at a slight cost in performance).

The resulting *S*-parameters for the structure are shown in figure 6.13. The transformer provides $S_{11} < -10dB$ from 31 to 52GHz, with at worst S_{21} of -1.3dB (insertion loss is approximately 0.76dB). This compares favorably to the standard two-stage Chebyshev match, which for component Q of 10 and network Q of 1 gives a theoretical insertion loss of 0.85dB.

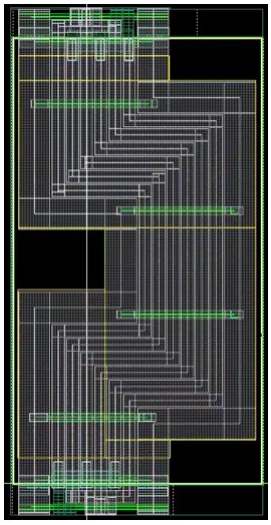

Figure 6.9: A six finger Lange Coupler with 12.5 ohm Characteristic Impedance

Input 50 ohm Hybrid The hybrid used previously in the wideband transmitter was re-used in this design.

AC coupling capacitors The AC coupling capacitors needed some care to minimize loss while simultaneously achieving a high enough breakdown voltage (approximately 3.3V). To do so, the standard "momcap" was modified to include the top-metals which essentially wrap around the capacitor, which helps reduce coupling to the lossy substrate and provides additional, low resistivity capacitance. The spacing of the momcap fingers was also increased to increase the breakdown voltage. The resulting 250fF (Fig. 6.14) capacitor had a simulated (in EMX) Q of 77 at 40GHz.

6.4.2 Actives

The individual PA schematic is shown in Fig. 6.15. It consists of two cascoded common source stages, with a low-*k* transformer and capacitive matching sections between each. Note that the PAs are single ended. Each stage also has a 100pH choke with multiple wide traces designed to provide the voltage supply and handle the large DC and AC currents. An example walkthrough of the inter-stage matching is shown in Fig. 6.16. The overall small-signal power gain of the combined stages is shown in Fig. 6.17, at class A/B, when driven by a 50 ohm source, into the 12.5 ohm load (the hybrid).

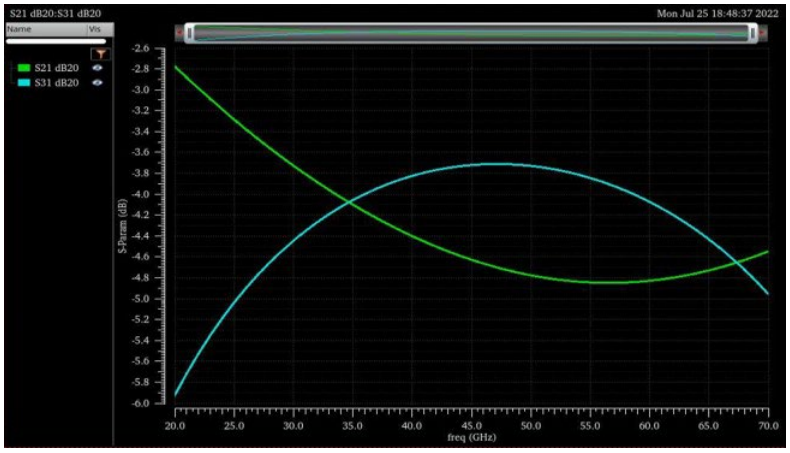

Figure 6.10: *S*-parameters for the 12.5 ohm Lange Coupler

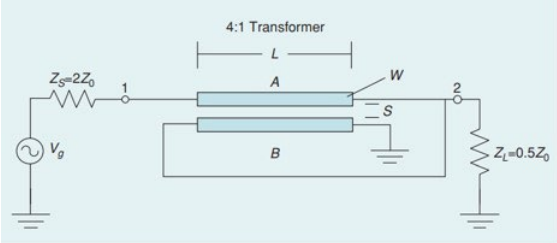

Figure 6.11: Ruthroff Transmission Line Transformer, *L* is about *λ/*8 [7]

6.5 Tapeout and Conclusion

The overall PA was taped-out in TSMC's 28nm CMOS process in late August, 2022. Figure 6.18 shows the top-level layout. Measurements will be done via probing (DC source provided via wirebond) upon receiving the chip, expected quarter 2 of 2023. This work thus explores the use of the OLMBA for applications (such as mobile handsets) with large load variations. The total structure is expected to deliver approximately 16dBm P_{sat}, at 18% efficiency from 30-50GHz. Future work will delve more in depth on utilizing the load modulation to either help load mismatch tolerance or improve other functions such as back-off efficiency or increased P_{sat}.

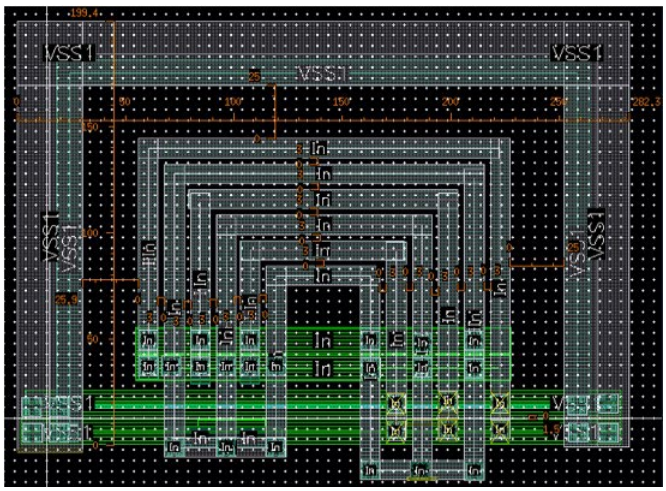

Figure 6.12: Layout of the 4:1 Ruthroff Transmission Line Transformer, Meandered to Reduce Area

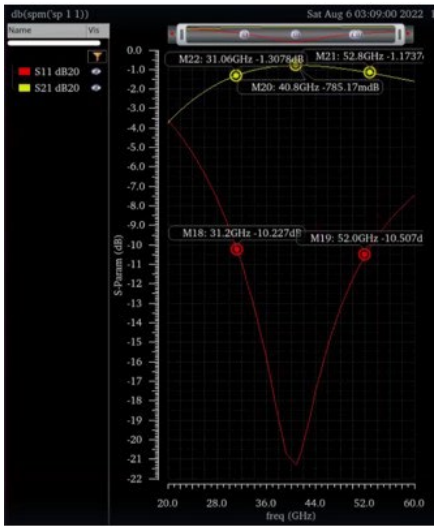

Figure 6.13: Ruthroff 4:1 Transformer *S*-Parameters, from 50:12.5 ohms

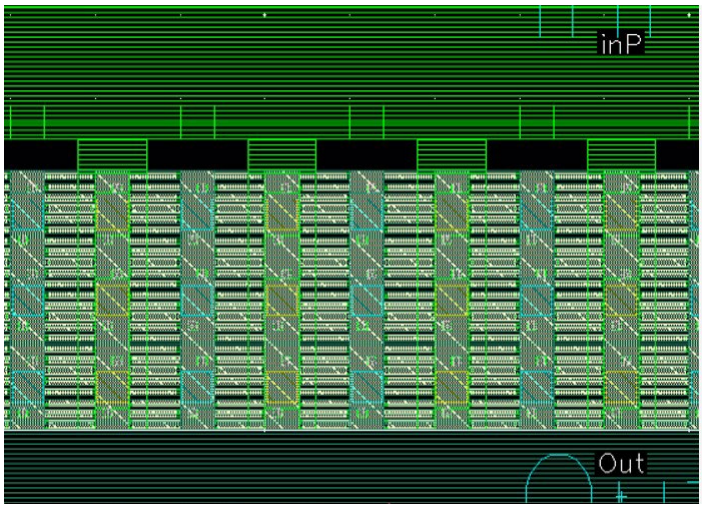

Figure 6.14: Momcap Modified with Top-metal Layers Above and on the Sides, and Wider Gaps to Achieve a Good Q at High Frequency and an Increased Breakdown Voltage

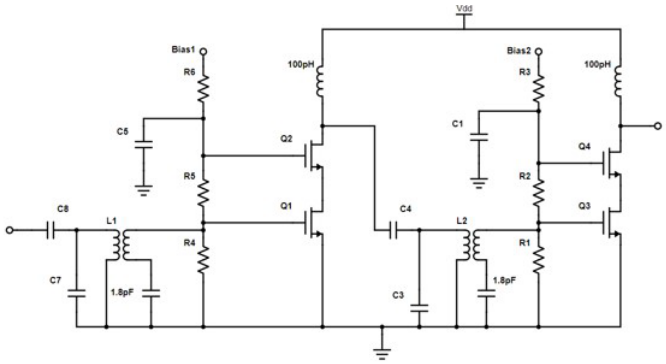

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Figure 6.15: Transistor Level Schematic of the Individual PA
Simple two stage, cascoded PA architecture, with matching sections in between.

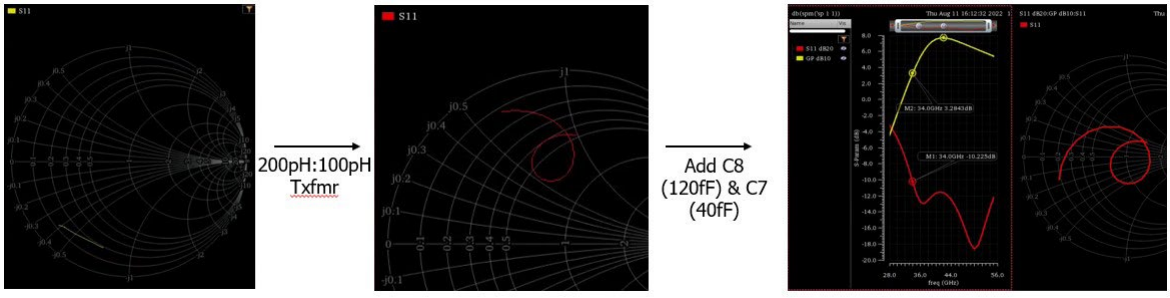

Figure 6.16: Matching Network Design, First the Low-*k* Transformer is Added, followed by a Capacitive Divider Match

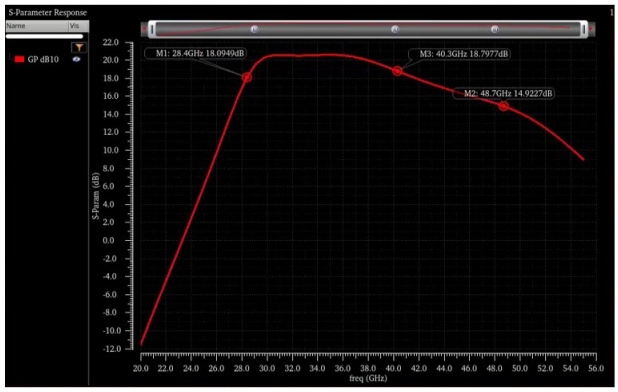

Figure 6.17: Overall Small-signal Gain of Each Individual Power Amplifier Chain

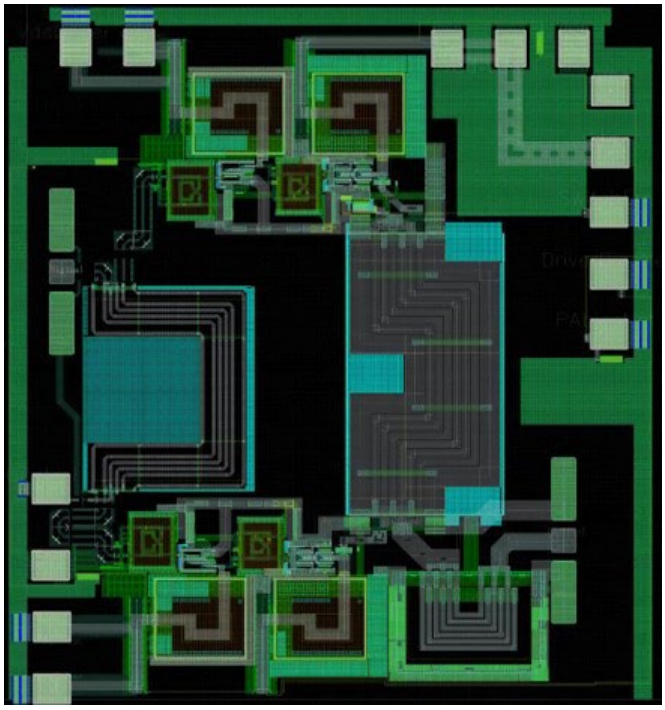

Figure 6.18: Top Level Layout Taped-out, as Seen in Virtuoso

7 CONCLUSION

This project explored the design of wideband mm-wave CMOS transceivers with enhanced linearity, applicable to modern highly linear front-end modules. The enhanced linearity is particularly needed when interfacing these circuits to front-end modules to enhance the output power, the sensitivity, or to address a particular frequency band.

Several techniques were proposed and demonstrated to improve the receiver linearity. We realized mixer-first passive mixers at mm-wave frequencies, and further demonstrated a new voltage mode baseband amplifier with feedback to realize very high in-band linearity, an order-ofmagnitude improvement over previous demonstrations. The design also places resistors in each arm of the quadrature I/Q mixer, mitigating charge sharing and improving the noise figure. This is important since non-overlapping 25% clocks are difficult to generate at mm-wave frequencies, whereas sinusoidal quadrature is practical. A measured prototype down-conversion receiver has record high linearity, achieving +14.1 dBm IIP3 and covers 10-35 GHz frequency range. The noise figure varies between 12.5 and 15.7 dB in the 10-30 GHz range.

We also proposed a new matching technique at the mixer input, which uses the resistance of the switch for matching rather than an explicit resistor. This greatly improves the noise figure and also combats charge sharing through series inductors in the matching network. The network is tunable to cover a wide bandwidth. Over a 25-40 GHz frequency range, the simulated noise figure is below 8 dB while the IIP3 is larger than +12 dBm (in-band), while maintaining a baseband bandwidth of 200 MHz. This down-conversion receiver has > 4dB lower noise figure, and represents state-ofthe-art performance if verified by measurements.

On the transmitter side, we have explored several broadband amplifier and transmitter architectures. We designed and taped out a complete transmitter chain consisting of a broadband baseband I/Q DAC, on-chip filters, and high OIP3 distributed mixers that power combine on a transmission line to realize I/Q combining and broadband performance. The chip includes a high-speed digital interface to feed 20 bits of I/Q data into the transmitter as well as LO generation and distribution. The fabricated chip has a bandwidth of 13-50 GHz and a compression point of 2.5 dBm while consuming 71mW on a 1.2V supply. The prototype has been fabricated in a 28nm bulk process and testing is in progress.

To boost the output power, we also investigated broadband PA topologies, such as Doherty combining, which is known to have superior back-off characteristics, 1but suffers from linearity at back-off due to the bias point of the auxiliary amplifier. To alleviate this issue, we introduced a dynamic biasing element that tracks the signal envelope in a process/temperature/supply voltage insensitive manner to generate a bias that can be programmed to ramp up the auxiliary amplifier in an optimal way to boost output power with a desired level of linearity. Despite using a quarter wave combiner, the design has good bandwidth compared to previous demonstrations. A 28 GHz prototype meeting strict OFDM linearity requirements of 5G has been sent for fabrication and we are awaiting the chip for

measurements. The design covers 23 GHz - 28 GHz and has a simulated output power of 18 dBm (average for OFDM) and an efficiency greater than 30% (peak 35%).

Finally, to build a truly wideband PA that is robust against load variations, we employed an Orthogonal Load Modulated Balanced Amplifier (O-LMBA), which has many interesting features. For one the load modulation can be used for back-off efficiency enhancement. In our design we utilize the structure as a wideband combiner, designed with a wideband Lange coupler, and use a controlled reactive termination to improve the output power under VSWR. The prototype has a simulated bandwidth covering 30-50 GHz and a output power of 16 dBm with 18% efficiency. It was sent for fabrication in a 28nm CMOS bulk process.

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LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS

ACRONYM	DESCRIPTION
CDR	Clock-Data Recovery
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-to-Analog Converter
ENOB	Effective Number of Bits
ESD	Electro-Static Discharge
EVM	Error Vector Magnitude
FPGA	Field-Programmable Gate Array
IM	Intermodulation
LMBA	Load Modulated Balanced Amplifier
LNA	Low-Noise Amplifier
LO	Local Oscillator
LTI	Linear Time-Invariant
LVDS	Low-Voltage Differential Signaling
MIMO	Multiple-Input Multiple-Output
NMOS	N-type Metal–Oxide–Semiconductor
OFDM	Orthogonal Frequency Division Multiplexing
OLMBA	Orthogonal Load Modulated Balanced Amplifier
PCB	Printed Circuit Board
RC	Resistor/Capacitor
RF	Radio Frequency
SNR	Signal-to-Noise Ratio
TSMC	Taiwan Semiconductor Manufacturing Company
VSWR	Voltage Standing-Wave Ratio