AFRL-RI-RS-TR-2023-041

FABRICATION TECHNOLOGIES FOR SUPERCONDUCTING OPTOELECTRONIC NEUROMORPHIC COMPUTING

SUNY POLYTECHNIC INSTITUTE

MARCH 2023

FINAL TECHNICAL REPORT

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REPORT DOCUMENTATION PAGE

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED START DATE	3. DATES COVERED END DATE
MARCH 2023	FINAL TECHNICAL REPORT	MARCH 2019	SEPTEMBER 2022

4. TITLE AND SUBTITLE

Fabrication Technologies for Superconducting Optoelectronic Neuromorphic Computing

5a. CONTRACT NUMBER	5b. GRANT NUMBER	5c. PROGRAM ELEMENT NUMBER
N/A	FA8750-19-1-0031	62788F
5d. PROJECT NUMBER	**5e. TASK NUMBER**	**5f. WORK UNIT NUMBER**
		R2RG

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8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Air Force Research Laboratory/RITB
525 Brooks Road
Rome NY 13441-4505

10. SPONSOR/MONITOR'S ACRONYM(S)

AFRL/RI

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

AFRL-RI-RS-TR-2023-041

12. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for Public Release; Distribution Unlimited. This report is the result of contracted fundamental research deemed exempt from public affairs security and policy review in accordance with SAF/AQR memorandum dated 10 Dec 08 and AFRL/CA policy clarification memorandum dated 16 Jan 09.

13. SUPPLEMENTARY NOTES

14. ABSTRACT

In this project, three critical circuit elements (superconducting nanowires, W-center 1.22 um emission centers, and Josephson junctions) for superconducting optoelectronic neuro-morphic computing (SONC) at 300 mm wafer scale using CMOS-fab compatible materials and processes. W-center photoluminescent emission (at a operating temperature of 25 K) of 1.22 μm light with <3% across-wafer non-uniformity was demonstrated. Physical vapor deposited TaN nanowires showed <4% across-wafer non-uniformity in room temperature resistance, and critical current density of 0.25 MA/cm2 for 20 nm thick nanowires. Cu-encapsulation showed non-hysteretic behavior in the nanowires. Josephson junctions with superconducting α-Ta electrodes and ALD TaN as the tunnel barrier showed resistance dependence that scaled precisely as inverse-squared with junction dimension, as expected. Junctions of 2 μm showed within wafer non-uniformity of ~4%, while junctions larger than 500 nm had non-uniformity better than 10%. Cryogenic measurements indicated that the tunnel barrier thickness of 9 nm was too thick for determination of Josephson junction critical current, but showed an I-V trace that was otherwise supportive of an SIS junction. Yield of the electrically tested structures exceeded 90%. The successful fabrication of these sub-components prepares the ground well for future integration of SONC systems.

15. SUBJECT TERMS

Neuromorphic, computing, nanowire, superconductor, Josephson junction, cryogenic

16. SECURITY CLASSIFICATION OF: a. REPORT	b. ABSTRACT	C. THIS PAGE	17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES
U	U	U	SAR	47

19a. NAME OF RESPONSIBLE PERSON	19b. PHONE NUMBER *(Include area code)*
JACK P. LOMBARDI	**N/A**

PREVIOUS EDITION IS OBSOLETE.

STANDARD FORM 298 (REV. 5/2020)
Prescribed by ANSI Std. Z39.18

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1.0 SUMMARY

This project is focused on the development of three critical device components of a superconducting optoelectronic neuromorphic computing (SONC) system at 300mm wafer scale. Such an SONC system will use Josephson junctions as an integral part of the neuron spiking circuits, Si-based cryogenic infrared photon emitters and superconducting nanowire single photon detectors for one neuron to signal hundreds of downstream neurons, with the neural weights being implemented as bias currents. Neurons in an SONC system have been designed to show spike-timing-dependent plasticity, integrate-and-fire, and other important characteristics of biological neurons [1]. NIST has demonstrated some elements of SONC [2] and published results of theoretical calculations [3] indicating that SONC could be several orders of magnitude faster than a human brain, while maintaining similar levels of energy efficiency as the human brain, measured as spikes/s/W. SONC systems have the advantage of enabling hundreds of synaptic connections between a neuron and its downstream neighbors, due to the use of superconducting single photon detectors that are integrated onto photonic waveguides. SONC systems that could mimic the visual cortex of the human brain have been envisioned.

This project was executed between March 1, 2019 and September 30, 2022, which included a six-month no-cost extension granted due to COVID-related delays in the thick of the pandemic. The project was carried out by a team led by Dr. Satyavolu Papa Rao with co-PI Prof. Nathaniel Cady. The team included the many process technology and metrology experts in the fab, who were guided by the process integration R&D conducted by Dr. Stephen Olson, Dr. Soumen Kar and Dr. Ekta Bhatia. The latter two joined the team in 2021.

The SONC components to be developed in this project (using advanced 300mm process tools, and existing 193nm lithographic masks as applicable) comprise of (1) Si-defect based infrared photon emitters operating at cryogenic temperatures (2) nanowire superconducting structures with fab-compatible tantalum nitrides for development of single photon detectors and (3) scalable Ta-based superconducting Josephson junctions (JJs) using tunnel barriers formed by atomic layer deposition (ALD) of TaN. Demonstration of superconducting TaN nanowires deposited by physical vapor deposition (PVD) across 300 mm wafers leverages the lower superconducting gap of TaN to increase sensitivity. This was coupled with in-situ integration of thin Cu layer, as a heat-sink, directly above the superconducting TaN layer to improve the reset time of superconducting nanowire single photon detectors (SNSPDs) that will be needed for SONC. The fabrication of superconducting JJs using alpha-Ta electrodes and an ALD TaN tunnel barrier is a world-first, and particularly important since it is done on 300 mm wafer scale, using CMOS fab-friendly processes from start to finish. Additionally, an initial version of the Ta CMP Design Rule Manual was developed.

For each of the three components, this project targeted a standard deviation of <3% in the corresponding device characteristic, with the threshold condition set at <10%. The project has successfully demonstrated performance characteristics for the three components: Si-based photon emission uniformity of 2.7% was observed across the 300 mm wafer, exceeding target. Across-wafer resistance uniformity of superconducting TaN nanowires was 4%, far exceeding threshold, and close to target. Ta-based JJs achieved 4% non-uniformity

across a 300 mm wafer for junctions of 2 µm size, increasing to 10% for 0.5 µm junctions, and ~15% for the smallest junctions tested (100 - 200 nm). Yield of the PVD TaN nanowires as well as Josephson junctions ranged between 90 to 100%. Selected devices were measured at cryogenic temperatures at partner sites (NIST-Boulder and AFRL-Rome) to build correlations to room temperature measurements.

The success of this project paves the way to build neurons in a following project that exhibits neuromorphic computing behaviors such as integrate and fire, spike-timing dependent plasticity, *en route* to building a large scale SONC processor on a single chip.

2.0 INTRODUCTION

The functioning of an SONC neuron can be described with reference to Figure 1 [1]. With reference to portion of Figure 1labelled ‘Synapse’, an incoming photon (from an upstream neuron, say), causes the SNSPD to be driven normal, causing superconducting current to be driven into the adjacent circuit across the resistor. Depending on the ‘neural weights’ encoded by biasing superconducting currents, further propagation of the current pulse can be controlled. In the portion of Figure 1 labelled ‘Transmitter’, the current signal emanating from the thresholding circuit switches the state of the n-tron [4], diverting current to the h-tron [5] further to the right in the circuit diagram. This results in a voltage pulse activating the Si-based light emitting diode.

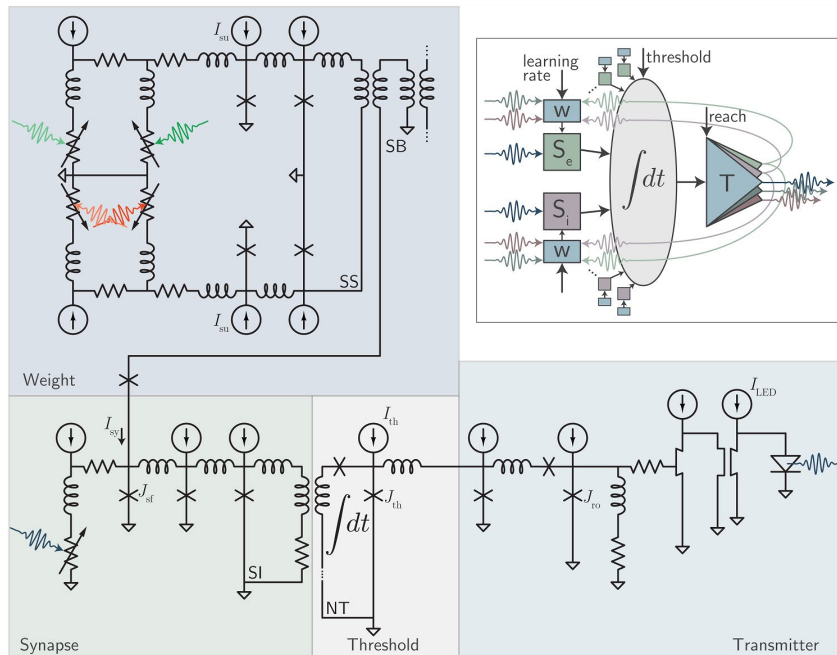


Figure 1: A superconducting circuit implementation of a single SONC neuron – the sub-circuit labelled Synapse shows the single-photon detector and firing junction; the sub-circuit labelled Transmitter illustrates how the current signal is transduced into an outgoing photon [1]

It can be observed that the circuit elements needed for implementing an SONC neuron include a number of Josephson junctions, SNSPDs, resistors, superconducting loops, an n-

tron and h-tron, a light-emitting diode and photonic waveguides. In this project, three crucial circuit elements were studied, for first time fabrication at 300 mm scale, using existing masks (at 100 nm minimum line/space rules, without optical proximity correction): Josephson junctions, superconducting nanowires and Si-based light emission. It should be noted that the resistor and superconducting loops are trivial adders, once a new mask with appropriate lithographic layers and layout is designed. The n-tron and h-tron require sub-100 nm lithography, necessitating a 193nm lithography reticle capable of smaller size features, which is eminently feasible, and widely practiced, in the CMOS industry. The implementation of n-tron and h-trons was hence moved to a future project when the entire neuron is constructed at 300mm scale, using a reticle-set specifically designed for it.

Josephson junctions consist of superconducting metal electrodes separated by a barrier across which tunneling of Cooper pairs occurs. Josephson junctions have been utilized in superconducting quantum computing and in superconducting single-flux quantum (SFQ) logic circuits that operate at speeds far higher than 10 GHz. Superconducting circuits have typically been fabricated using Nb as the interconnect material and a 'tri-layer' of Al/AlO/Al between Nb, with AlO functioning as the tunnel barrier. Recently, it was shown that qubits using Ta-based interconnects surpassed the performance of qubits using Nb interconnects [6]. Alpha-Ta (with a BCC crystal structure) is a particularly easy candidate for use in 300 mm wafer fabs since it has formed a part of copper interconnects in integrated circuits developed in the early 2000s. ALD TaN is also a friendly material for CMOS fabs, since it has been utilized as the preferred copper diffusion barrier in advanced interconnect with narrower critical dimensions (CDs). However, the ALD TaN that is used in CMOS ICs is designed to be as conductive as possible. Hence work was done in this project to develop a very high resistivity version for use as a tunnel barrier in the Josephson junction, along with alpha Ta as the material for junction electrodes as well as for the superconducting interconnect between the various circuit elements in a future SONC chip.

PVD TaN is the fab-friendly choice of material for SNSPDs. It can be patterned into nanowires by chemical-mechanical planarization (CMP), or by reactive ion etch (RIE). PVD TaN has a lower superconducting transition temperature than NbN, and hence would be more sensitive when integrated on top of a photonic waveguide as an SNSPD.

Since the neuron communicates with downstream neurons through photons generated and detected at cryogenic temperatures, the option of using silicon based photon emitters that operate at such temperatures can be taken advantage of. The advantage of using silicon based photon emitters is the avoidance of fabrication complexity introduced by III-V materials that are more typically used as light emitting materials. By implanting Si into Si, and annealing at chosen temperatures, a variety of light emitting defect centers can be formed [7]. In this project, the "W-center" was created using all 300 mm wafer processes, and studied using photoluminescence, since it has the required characteristics of a sharp 'zero phonon line' emission at 1.22 μm, which fits well within the transmission window of a silicon photonic waveguide. When the W-center region is coupled with adjacent n- and p- doped regions in silicon, it can form an LED.

Figure 2 shows a schematic cross-section of how such a circuit could be implemented in silicon, using the process technologies developed by this project. The W-center development ties into the LED shown on the right of Figure 2, while the PVD TaN nanowires

characterized in this project allow the design of SNSPDs shown on the left of Figure 2. The process technology developed in this project for Ta/TaN/Ta Josephson junctions is essentially ready for use in SONC circuits, with tweaks to the thickness of the ALD tunnel barrier to meet design needs.

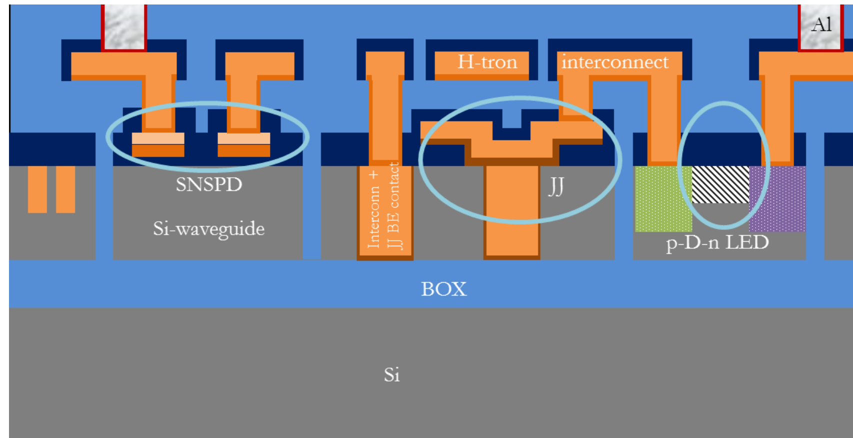


Figure 2: Schematic of SONC, with focal elements of this project highlighted

3.0 METHODS, ASSUMPTIONS, AND PROCEDURES

In this section, the process flows used for the 300 mm fabrication of the three focus areas of this project are described, with background information/results included where appropriate. The results of detailed characterization at room temperature and cryogenic temperatures (at partner sites like AFRL and NIST) are provided in the next section.

3.1. Fabrication of W-centers at 300 mm scale

Multiple experiments were conducted. Coupons from a 300 mm wafer, implanted with 5E15 of Si at 40 keV at Albany through 5 nm of silicon oxide, were annealed at NIST to study the effect of anneal temperature. This will be referred to, in the Results section as the Coupon study.

A set of 10 'blanket' (ie, no patterning) wafers were created to explore ion implantation conditions required to form the W centers. Si epitaxy was conducted on standard SOI wafers in order to ensure that the top Si thickness was 220nm – the thickness required for waveguides in an SONC system. It should be noted that the optimal thickness for the buried oxide (BOX) layer in the SOI wafers is 2 µm – to avoid 1.22 µm photon loss in the waveguides due to substrate coupling. However, initial experiments for implantation studies can be more cost-effectively conducted on 'standard' SOI wafers, which have a BOX layer thickness of 144nm – it also permits characterization of silicon modification towards the end of the implantation range in the silicon substrate under the BOX layer. The implant fluence was fixed at 5E13 Si atoms/cm^2. Implant energy was varied between 40 keV, 80 keV and 120 keV. The Si implant was conducted through a sacrificial oxide – whose thickness was varied between 120nm, 150nm, and 200nm. Each of the 10 wafers was annealed for 30 minutes in a single wafer anneal chamber held at 250°C, in a flowing N_2 ambient at 150mT. After annealing, the sacrificial oxide was etched using a dilute HF chemistry on a

300mm single-wafer platform. This experiment is referred to, in the Results section, as the Screening study.

Another set of 6 wafers were generated, where the screening oxide thickness was set at 150 nm, and the implant energy was set to 80 keV. The anneal temperature was varied, wafer by wafer, in 10°C increments from 230°C to 280°C, while anneal time was held constant at 30 minutes as before. The annealing ambient was nitrogen (with a constant flow of nitrogen through the chamber). As in the prior experiment, he screening oxide was stripped after annealing before shipping to NIST. This experiment is referred to, in the Results section as the "300mm-Anneal Study"

3.2. Fabrication of PVD TaN Nanowires

The fabrication of superconducting nanowires of PVD TaN was informed by work done first on blanket wafers. Blanket wafer tests were done early in this project, and repeated after the COVID pandemic had subsided, which allowed far deeper characterization at cryogenic temperatures than was possible with the first set.

3.2.1 Blanket PVD TaN film Deposition

A systematic study of PVD TaN films was conducted, using a reactive sputter deposition process (in a nitrogen/argon plasma ambient, using a pure Ta target) to deposit TaN on a 1 μm thick silicon oxide film. The silicon oxide was touch-polished to remove 30 nm of oxide and planarize the surface prior to PVD TaN deposition. During PVD TaN deposition, the chuck temperature was 300°C, or held at room temperature. In some tests the wafer was tightly coupled to the chuck temperature by capacitively pulling the wafer close to the chuck and flowing He gas between the chuck and the wafer, while in others, no active thermal coupling was used. Nitrogen content in the PVD TaN film was controlled through a change in the N_2 flow during the deposition step in the 300mm process chamber.

3.2.2 Patterning of PVD TaN Nanowires

The process sequence used to form the PVD TaN nanowires with Cu capping can be summarized as consisting of deposition of thermal oxide + SiN hardmasks, patterning openings in the hardmask to expose Si (100) of varying width, and trench formation in silicon with (111) sidewalls. This is followed by TaN and Cu deposition into these trenches. In a fashion akin to blanket PVD TaN deposition, the film properties were varied by altering the N_2 flow rate. Wafer temperature during deposition was also varied by capacitively pulling the wafer onto the 300 °C chuck and flowing He gas to ensure good thermal coupling between the chuck and the wafer, or leaving it unchucked, with a resultant (dramatic) decrease in thermal coupling. Cu was then deposited on the PVD TaN, without a vacuum break. The use of Cu has multiple benefits. It permits CMP of the PVD TaN/Cu stack to utilize well-known CMP processes that have been developed in the CMOS industry, and the presence of Cu above the TaN serves to act as an oxidation barrier that protects the superconducting PVD TaN film, and improves electrical contact during cryogenic characterization. Finally,

the Cu thin film that is in intimate contact with the superconducting nanowire provides an excellent heat sink for thermal hot-spots that will be generated during photon detection, reducing the reset-time of SNSPDs. In order to experimentally verify the heat-sink effect, and investigate superconducting proximity effects, some wafers were processed with an intervening layer of metallic, non-superconducting, ALD TaN between the superconducting PVD TaN and Cu.

The wafer with PVD TaN and Cu covering the surface is subjected to chemical mechanical planarization to remove the overburden and leave TaN/Cu in the trenches, as shown by the SEM image in Figure 3(a). With reference to Figure 3(b), it can be seen that an increase in the PVD TaN thickness will necessarily decrease the cross-sectional area occupied by copper. This will result in a higher resistance to be measured at room temperature, when copper is the predominant conductor. At cryogenic temperatures, when the PVD TaN becomes superconducting, current flows exclusively through the PVD TaN. The reticle set used for this study permitted 4 point resistance measurements of nanowires of widths ranging from 100 nm to 3 µm. Figure 3(c) shows a TEM cross-section of a 500 nm wide nanowire with 20nm PVD TaN as the superconducting layer, capped with Cu.

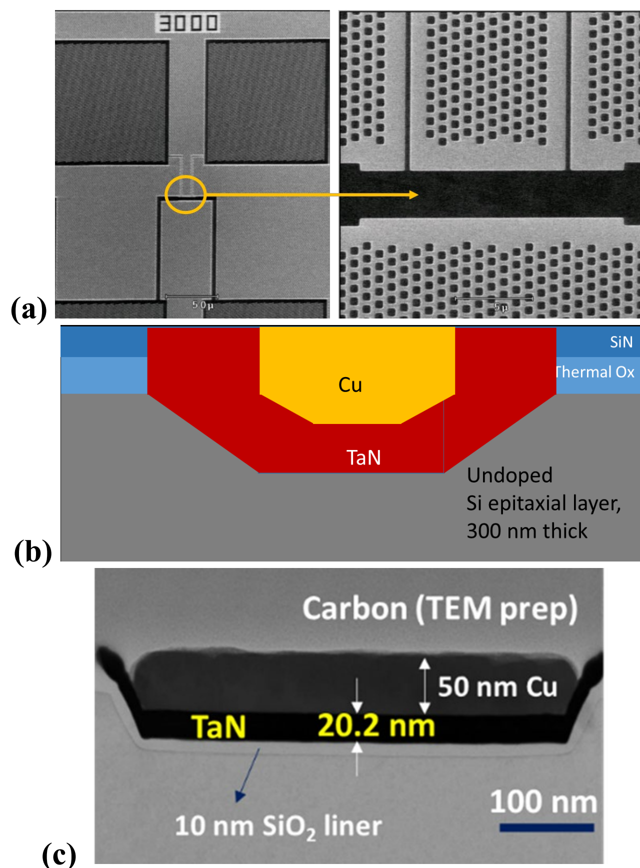


Figure 3: Diagram of nanowires with (a) SEM images of a 3 µm wide PVD TaN/Cu nanowire (b) schematic cross-section of the nanowire (c) TEM cross-section of a selected nanowire

3.3. Josephson Junction Fabrication with α-Ta Electrodes & ALD TaN Tunnel Barrier

The process flow for Josephson junction fabrication at 300 mm wafer scale involves about 40 individual steps, grouped into two major sections: those for creating bottom electrode features, followed by steps for creating JJs along with top electrodes. The process flow evolved significantly over the three years of this project.

3.3.1 JJ Fabrication using RIE-based Top Electrode Patterning

The first process flow followed a subtractive patterning scheme for top electrode patterning. It utilized a reticle at hand that permitted resistance measurements of only a few linewidths at the bottom electrode level, used 2 terminal measurements for junction resistance measurements (as shown in Figure 4) and had a degraded probability of success in aligning the top-electrode pattern to the bottom electrode features on the wafer.

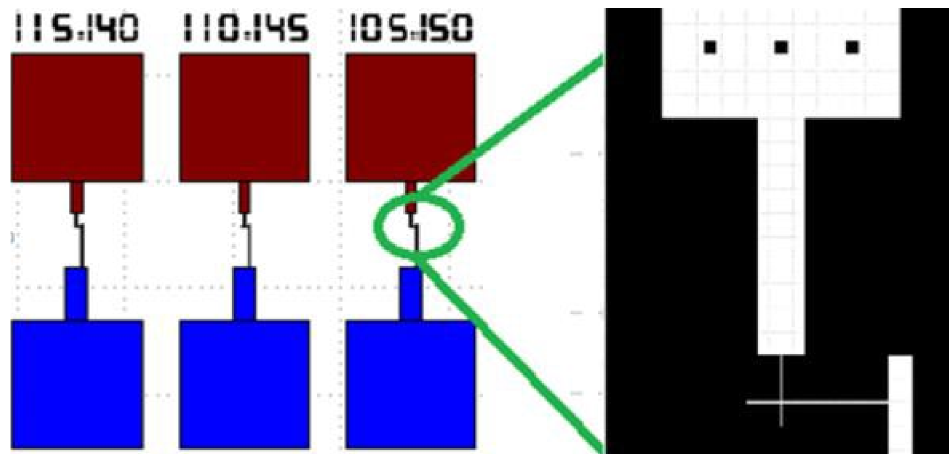


Figure 4: First reticle permitted only two-terminal measurements of Josephson junction resistance

As can be seen in Figure 5, the process flow involves lithography to create bottom electrode patterns, followed by RIE of the 30 nm thick thermal oxide hardmask to expose the silicon surface. Trenches with (111) Si faces on the sidewall are created using a hydroxide-based aqueous chemistry to accomplish the required anisotropic silicon etch. (The sloped sidewalls of the trench eliminate the likelihood of Ta seams forming at the corners during the subsequent physical vapor deposition of Ta). Trench formation is followed an oxidation step to create an insulating liner on the trench, followed by ALD TaN + Ta deposition. The ALD TaN is required to promote the formation of the alpha phase of tantalum (α-Ta), which is superconducting. This is followed by Ta CMP to remove the overburden of tantalum in the field areas, and leave the Ta in the trenches, creating the required damascene Ta features. Electrical test of the Ta features confirms good isolation between Ta lines, and measures the across wafer uniformity of Ta line resistance. This work enabled a “Rev0” Design Rule Manual for Ta CMP, as detailed in the Results section.

The next series of steps form the Josephson junction and top electrode connections. To accomplish this, the wafer surface (with damascene Ta lines) is sputter-cleaned and then

covered by the tunnel barrier (ALD TaN) of desired thickness, followed by PVD Ta (accomplished without an intervening air-break, since both processes are integrated into one 300 mm 'cluster tool' with high-vacuum transfer between various chambers). The Ta surface is then covered by a 30 nm thick Si oxide film deposited by room-temperature plasma-enhanced ALD. This layer serves as an oxide hardmask for Ta RIE. Due to the lack of an explicit "zero-layer" alignment mark (and associated process) in this reticle set, it was necessary to add a "no-alignment' 'mask-open' step that etched the (opaque) Ta above the alignment marks. This process exposed the alignment marks, so that the top electrode patterns could be aligned to the bottom electrode. As mentioned previously, this process still had >30% chance of failure, needing rework of the photoresist and multiple steps. When successful, top electrode patterns are created (by expose + develop) in the 193 nm lithography photoresist that is present above a spin-coated optical density layer (ODL) and a spin-coated anti-reflective coating (SiARC). The RIE process etches through the SiARC, the ODL, the SiOx hardmask, the Ta and the ALD TaN, ideally landing perfectly on the bottom Ta electrode surface, with minimal overetch into the Ta. The oxide hardmask above the top Ta is etched away in dilute HF, permitting low-resistance access to both the top and bottom electrode pads.

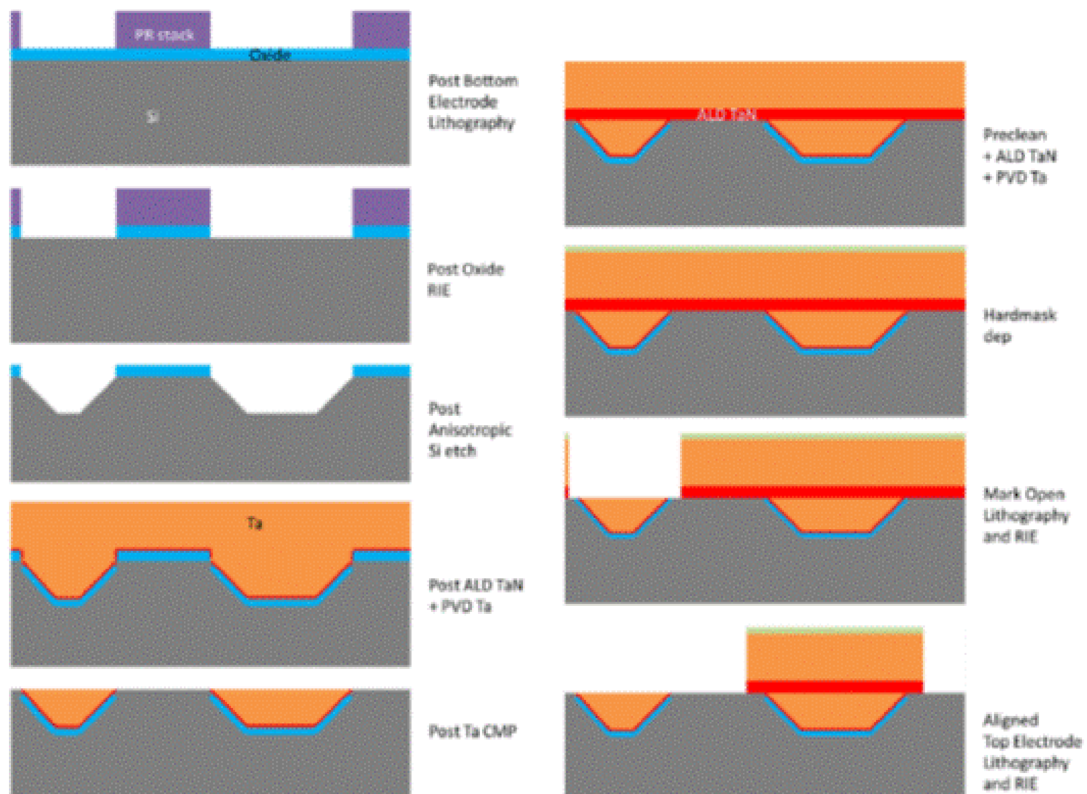


Figure 5: Process flow for JJ fabrication initially used, involving subtractive patterning for JJ definition

While it was possible to create a Ta RIE process to accomplish the above scheme, as can be seen in Figure 6, variability in the Ta RIE etch rate made across-wafer process control difficult, with good results as shown at left in Figure 5 also marred with areas on the wafer

where when the top Ta etch went too far and removed substantial portions of the bottom Ta (Figure 6a and 6b, on right). Metal RIE has inherently an edge-fast behavior, creating a condition where the wafer edge is always sacrificed (to some extent) in order to complete the RIE at the wafer center (in this process scheme). Additionally, separate monitors of the chamber Ta etch rate suggested that variability in Ta RIE etch rate over time will compound this difficulty. Images shown in Figure 6(a) and Figure 6(b) taken at different times illustrate this problem. Optical emission spectroscopy (OES) was feasible for the other steps in the RIE process (etching of organic photolithography stack layers, like ODL and SiARC, and the inorganic oxide hardmask layer). However, since the Ta to be etched in the top electrode and the Ta exposed by etch in the bottom electrode were the same, and > 50% of the wafer surface is exposed, it was not possible to create a reliable OES end point by leveraging changes in the optical emission from the plasma.

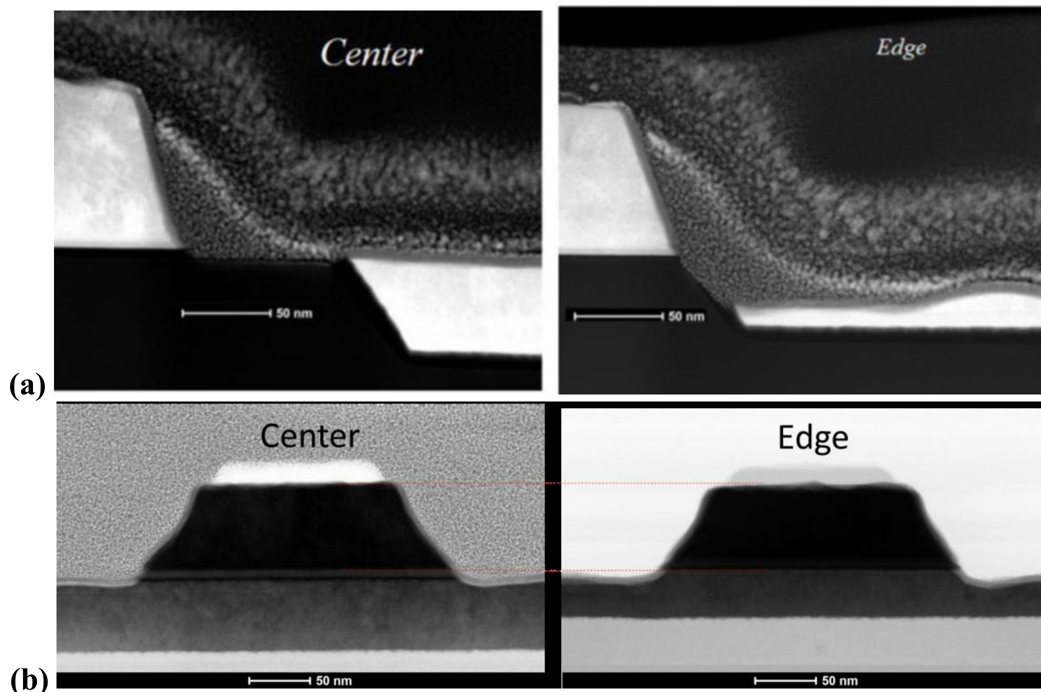


Figure 6: TEM cross-sections where (a) and (b) are images from two different wafers processed at different times through the RIE chamber. On left, images show good top Ta RIE, leaving bottom Ta largely intact after completion of RIE at wafer center. On right, removal of bottom Ta at wafer edge, with (a) and (b) showing the different amounts of remaining bottom Ta

In spite of these issues, significant progress was made on developing the Ta CMP process, formation of junctions and top electrode patterns, as well as initial, room-temperature, measurement of junction resistance. Cryogenic measurements of chips from these wafers were not possible because NIST Boulder was shut down for COVID, and the systems at the Innovare Advancement Center were yet to come online. Additionally, when the next reticle became available, the process flow evolved to the sacrificial oxide method of defining the top electrode, along with other improvements, as described in the next sub-section.

The improvement in process performance is so dramatic that this report will focus on the new scheme in the Results section.

3.3.2 JJ Fabrication Using Sacrificial Oxide Trench Patterning

In the second half of this project, coupled with the no-cost extension, another reticle set (designed for an AFRL STTR project on Fluxonium qubit fabrication) became available, which allowed for 4 terminal resistance measurements at all inline electrical test points. This improved data quality. In addition, the new reticle added a "zero-layer' pattern, and a separate lithography layer for trench formation in the sacrificial oxide.

The new reticle includes two types of Josephson junctions – a 'cross-junction' formed by the overlap of a bottom electrode by a top electrode line that runs perpendicular to the bottom electrode. This is shown in Figure 7(a). The second type is a 'bridge junction' formed by a via-like opening in the sacrificial oxide layer, into which the barrier and top electrode Ta are deposited, as shown in Figure 7(b). In this project, both types of junctions were compared, in terms of resistance targeting and across-wafer uniformity. The bridge junction has the advantage that the junction is completely planar, at the expense of layout complexity. It also has the advantage that junction geometry is set by one lithographic exposure (the MS level), rather than by two levels. The MS level is necessary under the TE level to ensure that Ta in the TE line is anchored to the silicon, and is separated from the Si only in small lengths where bridges are explicitly desired, as can be seen in the schematic cross-section in Figure 7(b)

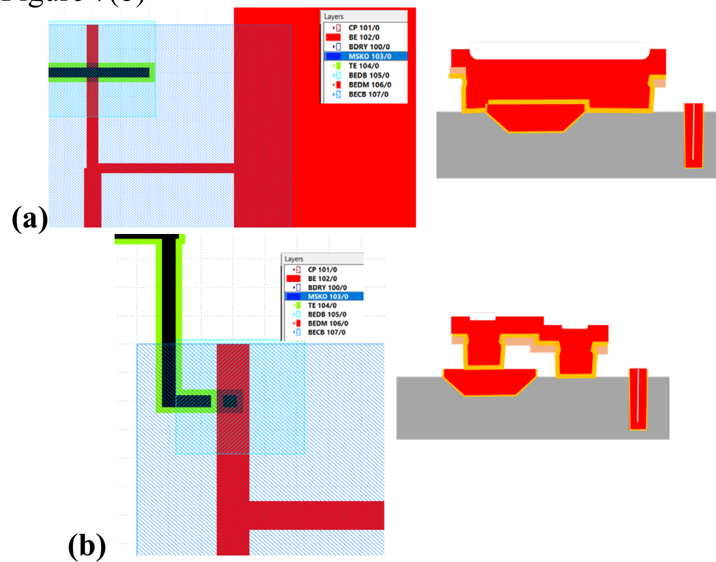


Figure 7: Junction layouts with (a) Cross-junction layout and schematic cross-section (b) Bridge junction layout and schematic cross-section

The new process flow can be easily explained with reference to Figure 8. This process flow uses a dual hardmask approach with 50 nm thermal oxide surmounted by a 20 nm RTCVD SiN layer – this allows for the formation of a 1.25 μm deep trench layer that can serve as zero-layer alignment mark (if needed). This deep trench layer also permits capacitor formation (required for qubits). The dual hardmask is etched to expose Si, which is followed by an anisotropic etch to create trenches in Si with sloped sidewalls that follow the (111)

planes of silicon (as was done in the prior process flow) – this is captured in the schematic cross-section marked “A” in Figure 8. The SiN hardmask is then selectively removed using a hot phosphoric acid chemistry. The trenches are filled with α-Ta and then CMP’ed (again in a process similar to what was described in the prior scheme).

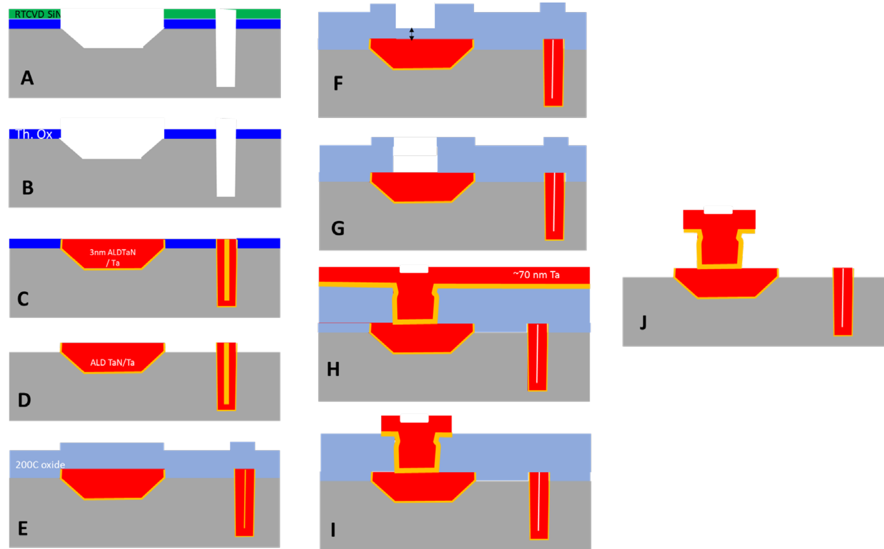


Figure 8: Process flow for JJ fabrication using sacrificial oxide

One of the differences in the current integration scheme is that the thermal oxide is now etched away with dilute HF, as shown in the schematic labeled “D”. This change, coupled with the use of shorter wavelengths in the lithographic alignment process, resulted in very high accuracy alignment of the next patterning steps to the bottom electrode pattern. This made the “zero-layer” mark optional, if deep capacitors are not required – the success of this change in improving alignment has been repeatedly verified, with < 30 nm of maximum misalignment on all wafers tested over multiple months. An example of the alignment feature is shown in Figure 9.

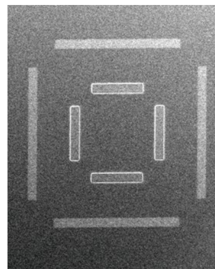


Figure 9: Alignment verification feature confirming excellent alignment to bottom electrode pattern

Returning to the process flow, after the oxide is etched, leaving damascene Ta features embedded in silicon, various surface treatments have been tested (in addition to leaving it as is, with no surface treatment): sputter clean and cover with PVD TaN, sputter-clean and cover with high resistivity ALD TaN. For the SONC case, such treatments are not needed, and a native oxide of Ta and Si can be left over the respective surfaces.

In schematics F and G of Figure 8, the next steps are shown – a sacrificial layer of oxide is deposited, and then a trench layer (called "MS") is patterned and etched. The etch process is designed to leave some amount of oxide at the bottom of the trench, so that the Ta surface underneath is not roughened by the energetic RIE process used to etch the trench in the sacrificial oxide. Figure 10 shows an example of the resultant structure with 20 nm of oxide left to protect the Ta, corresponding to schematic G. The image also shows residue-free surfaces, which was achieved after considerable experimental optimization.

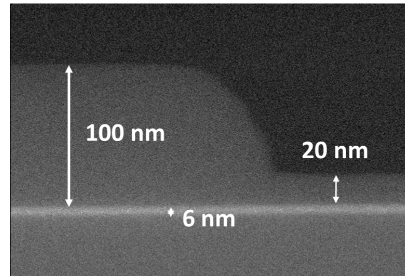


Figure 10: Cross-section post "MS" trench RIE

Schematics H, I and J of Figure 8 show the critically important steps of tunnel barrier and α-Ta deposition, patterning of the top electrode, followed by dHF etch of the sacrificial oxide. Figure 11 shows tilt-view scanning electron microscope images of finished junctions, as well as cross-sectional transmission electron microscope images of a 'bridge' junction.

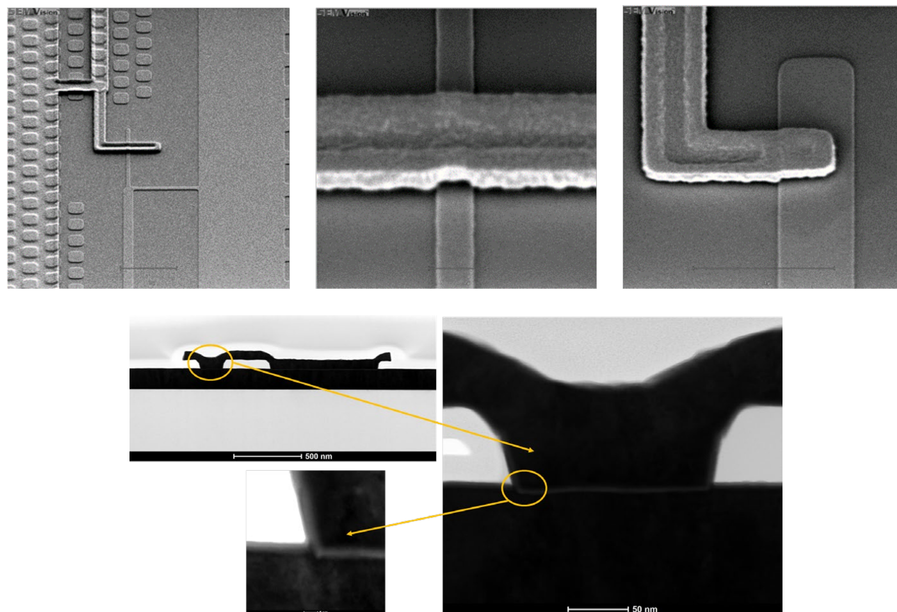


Figure 11: Top down SEM and cross-sectional TEM images of Josephson junctions fabricated using the sacrificial oxide approach

4.0 RESULTS AND DISCUSSION

4.1. Characterization of W-centers on 300 mm wafers

Cryogenic micro-photoluminescence measurements (at NIST Boulder) indicated that the sharply defined emission associated with the W-center at 25 K was approximately 300x brighter than the light emitted at the silicon band-gap energy (Figure 12). The W-center emits light at 1.22 µm (the zero-phonon line), and has weaker emissions in a satellite train at longer wavelengths, in a predictable pattern.

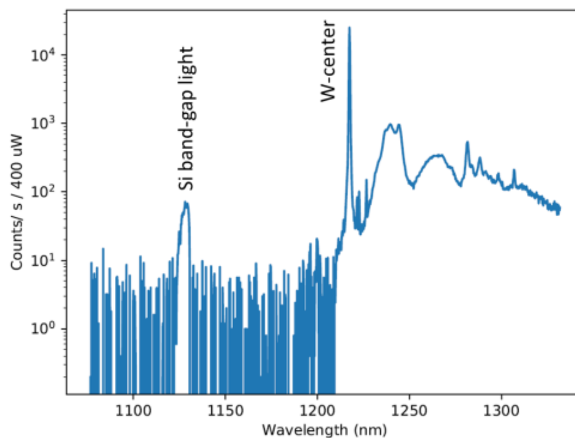


Figure 12: Micro-photoluminescence emission spectrum at 25 K, comparing the W-center with silicon band-gap emission

Measurements of the screening-oxide thickness/ implant energy splits ('Screening Study') indicated that highest emission intensity was observed with the 80 keV implant through a screening oxide thickness of 150 nm. (Figure 13). For a given implant condition, there is an optimal screening oxide thickness desired. If the screening oxide is too thin, more of the implant energy is deposited beyond the Si layer, and is hence 'wasted' since no W-center can be formed in the buried oxide layer. Similarly, if the screening oxide is too thick, the damage-region (where the W-centers are formed) can move into the sacrificial screening oxide. In Figure 13, the blue lines confirm that no photoemission is observed when the silicon layer above the buried oxide (BOX) layer is removed – hence, in all conditions, no W-centers were created in the bulk silicon substrate under the BOX layer. As it has the highest photoluminescence counts, 80 keV Si implant through 150 nm of screening oxide is hence set as the 300 mm process of record.

In the '300mm-Anneal Study', the thermal process conditions for W-center activation were varied from 230°C to 280°C, (503 K to 553 K), in steps of 10 Kelvin, in an ambient of flowing nitrogen, for 30 minutes. The results of the measurements at NIST from these wafers are shown in Figure 14(a). In Figure 14(b), multiple locations across a wafer were measured multiple times. The error bars represent 3 standard deviations. The highest variation from a single area had a standard deviation of about 2.8%, giving a 3-sigma interval of about 8.3% for the measurement error. This is significantly higher than the maximum variation in means between any two different locations, ~3.5%, allowing the team to conservatively conclude that the total variation across the wafer is less than 8.3%. Hence one-

standard deviation variation across the 300 mm wafer is less than 3.0%, under the 300 mm 'Process of Record' (POR) conditions that have been developed, in this project, for W-center formation. The POR is: a screening oxide of 150 nm thickness, a Si fluence of 5E15 atoms/cm^2, an anneal temperature of 543 K, in a flowing pure N_2 ambient, held at a pressure of 150 millTorr.

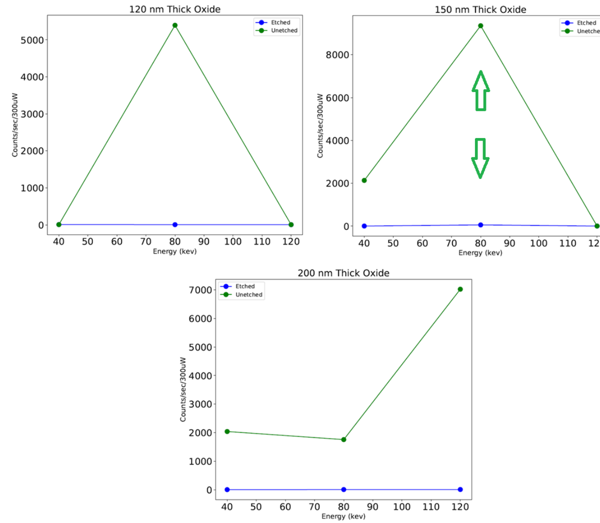


Figure 13: Photoluminescence Results for the 'Screening study'

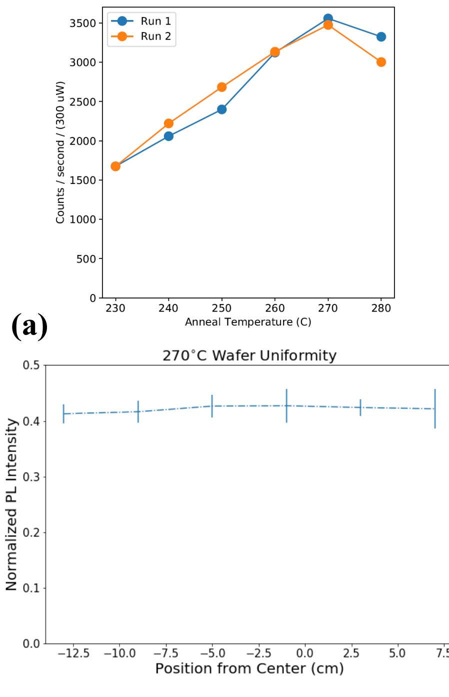


Figure 14: Plots of photoluminescence results with (a) Micro-photoluminescence characterization as a function of annealing temperature in 300 mm process tool (b) W-center emission uniformity characterization at NIST Boulder

4.2. Characterization of PVD TaN films and Superconducting Nanowires

4.2.1 Characterization of Blanket wafers with PVD TaN

Blanket PVD TaN films were characterized by X-ray Photoelectron Spectroscopy (XPS) in order to identify the N to Ta ratio in the “bulk” of the film (away from the top surface that would be subject to oxidation upon exposure to the atmosphere). The results are shown in Figure 15.

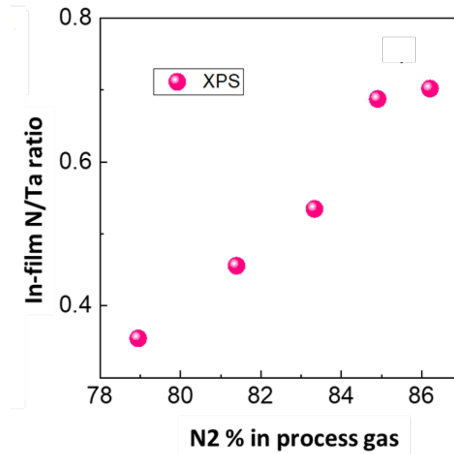


Figure 15: XPS characterization of films deposited with different plasma ambients

These films were also studied by X-Ray Reflectometry (XRR) and 4-pt sheet resistance measurements. In Figure 16(a), the within wafer non-uniformity for sheet resistance (Rs) and for thickness are plotted versus the N/Ta ratio. It can be seen that the thickness uniformity stays roughly constant over the process space explored, while the Rs non-uniformity stays constant initially, but rises sharply for films with the highest N content studied. Thickness and sheet resistance measurements are combined to determine the influence of N/Ta ratio on film resistivity, as shown in Figure 16(b). This shows the sigmoidal transition in resistivity (from metallic to insulating) due to in-film N content, as has been reported by many studies [8]. Figure 16(c) shows the in-plane glancing incidence X-ray diffraction (GIXRD) spectra as a function of in-film N content, as well as the out-of-plane XRD spectra. There is a clear change in the spectra when moving from the film with lowest nitrogen content (N/Ta = 0.35) to other films. With N/Ta = 0.35, the peaks ((111), (200), (220) and (311) in order of increasing 2-theta) can be matched well to a face-centered cubic structure, with a lattice constant of 4.32 Å. Films with higher nitrogen content cannot be matched well by cubic structures, but to a body-centered tetragonal cell with a = b = 4.32 Å, c = 5.15 Å or c = 5. 25 Å, with peaks assigned to (002), (200), (220) and (222), in order of increasing 2-theta. Residuals are less than 1%, which could be explained by in-film elastic strain.

Superconductivity of PVD TaN films with N/Ta ~ 0.53 was confirmed by NIST Boulder, as shown in Figure 16(d), with a superconducting transition temperature of 3.3 to 3.5 K at various points on the wafer (this wafer was processed separately from the wafer-set that has been described here, but with process conditions as prescribed). This gave confidence to move ahead with patterned nanowires, for characterization at room temperature and at cryogenic temperatures.

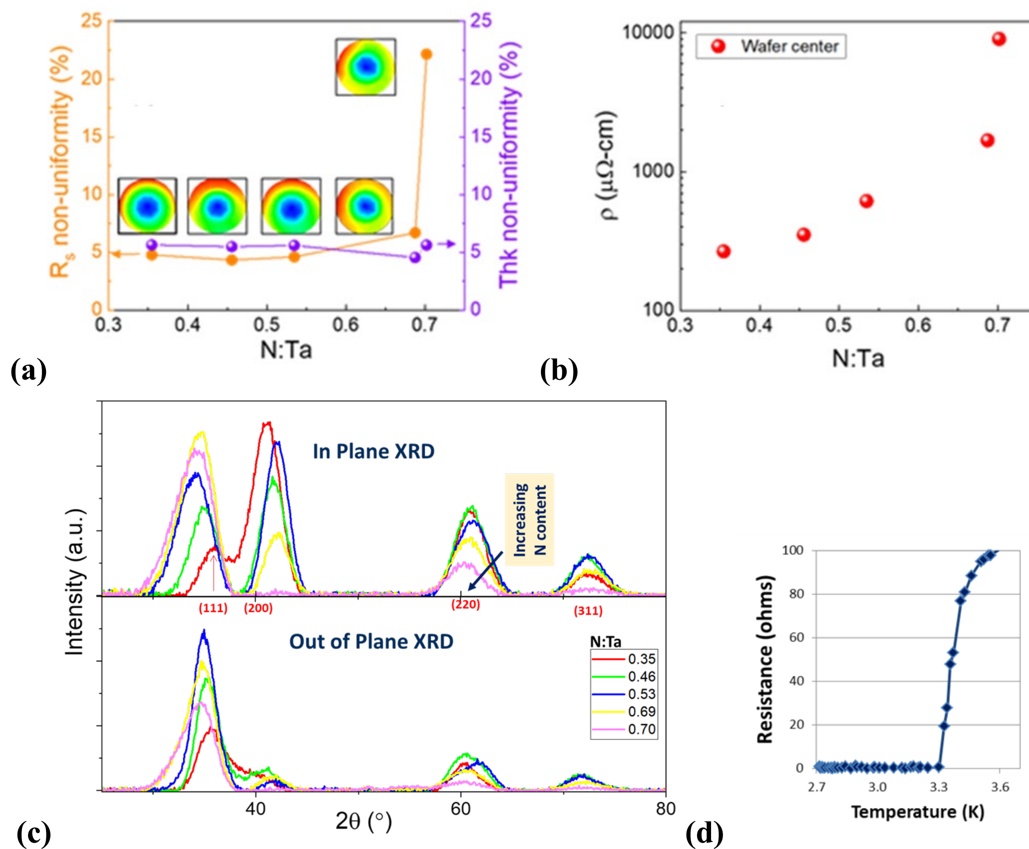


Figure 16: Diagram of TaN PVD characterization with (a) Within wafer non-uniformity of sheet resistance and thickness as a function of in-film nitrogen content (b) film resistivity as a function of in-film nitrogen content (c) In-plane and out of plane XRD spectra, also as a function of in-film nitrogen content (d) Superconducting transition confirmed at NIST Boulder

In addition to the uniformity characterization of blanket films, it is important to verify that the nanowire structures show uniformity in sheet resistance measurements at room temperature. This is a good proxy for uniformity of cross-sectional area of the superconductor, which will imply uniformity of critical current (thereby reducing the number of measurements to be made at cryogenic temperatures). Since the patterned nanowires have both PVD TaN and Cu, it is necessary to remove the Cu using dilute sulfuric acid, prior to measuring line resistance at room temperature. Figure 17 shows the result of such measurements, confirming that within wafer non-uniformity of PVD TaN sheet resistance is around between 3 to 4%, for PVD TaN nanowires with N/Ta ratio of 0.53, and film thickness of 35 nm.

30s 46JOI050SJC2	B120S	B150S	B200S	B120SL	B150SL	B200SL
Average (kΩ)	29.11	26.91	24.71	38.85	34.96	30.84
Stdev (Ω)	1094.5	1039.1	992.1	1390.2	1271.2	1172.1
Stdev %	3.76%	3.86%	4.01%	3.58%	3.64%	3.80%
40s 46JOI049SJG4	B120S	B150S	B200S	B120SL	B150SL	B200SL
Average (kΩ)	20.80	19.34	17.79	27.78	25.09	22.18
Stdev (Ω)	714.5	688.0	643.7	910.4	829.2	765.1
Stdev %	3.43%	3.56%	3.62%	3.28%	3.30%	3.45%
50s 46JOI048SJC2	B120S	B150S	B200S	B120SL	B150SL	B200SL
Average (kΩ)	17.65	16.35	15.02	23.66	21.33	18.78
Stdev (Ω)	597.8	562.4	532.4	757.6	691.0	617.2
Stdev %	3.39%	3.44%	3.54%	3.20%	3.24%	3.29%

Figure 17: Room temperature sheet resistance of PVD TaN nanowires of varying width showing within-wafer non-uniformity is between 3 and 4 %

Wafers processed at Albany were diced at the AIM Photonics TAP facility in Rochester, NY, with help from Peter McGarvey. The chips were packaged using designs by Dr. Jack Lombardi, and with help from his team-members at AFRL-Rome. Characterization of packaged chips with PVD TaN nanowires (of various compositions, and thicknesses, and linewidths) was performed in the Blue Fors XLD dilution fridge at the Innovare Advancement Center, Rome, NY, jointly with Dr. Jack Lombardi, with help from Dr. Mike Senatore, Dr. Dan Campbell and Dr. Matt LaHaye.

Figure 18(a) provides an example of the I-V traces obtained, while Figure 18(b) is a plot of the critical current density of nanowires of various widths. PVD TaN (N/Ta ~ 0.53) of 20 nm and 35 nm thicknesses showed superconductivity. Using area estimated from TEM, the critical current density of 20 nm nanowires is ~ 0.25 MA/cm^2, while that for 35 nm nanowires is ~ 0.8 MA/cm^2. Figure 18(c) shows that nanowires with PVD TaN thickness of 5 nm (nominal) did not show any superconducting transition even down to millikelvin temperatures.

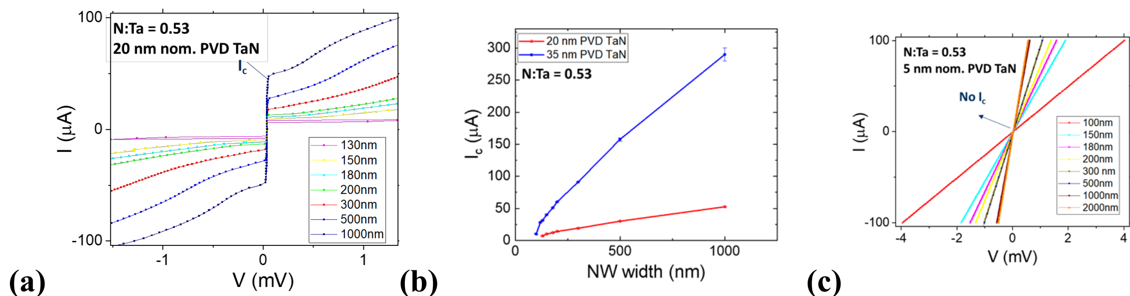


Figure 18: I-V plots for TaN nanowires with (a) I-V traces for 20 nm thick nanowires (b) Critical current for 20 nm and 35 nm thick PVD TaN nanowires of varying width (c) I-V traces for 5 nm thick TaN

The lack of superconductivity for the thinnest film could potentially be ascribed to the reverse proximity effect, due to the intimate contact of a 5 nm thin superconductor with a

>10x thicker layer of copper. Since Cooper pairs diffuse from TaN into the Cu, and unpaired electrons diffuse from copper into the superconductor – these processes can impact the superconductivity of PVD TaN films of thicknesses close to the coherence length of PVD TaN. It could also be due to compositional differences in the initial few nanometers of PVD TaN deposition. Further work will be required to understand this better.

As mentioned previously, as the PVD TaN thickness increases, the Cu thickness decreases in a linear fashion. This translates directly into the ability of the Cu layer to transport heat away. Due to the ability of Cu to transport heat away, the 20 nm nanowires showed a single value for critical current, and no hysteresis. But, as Figure 19(a) shows, a 35 nm PVD TaN nanowire shows hysteresis, with distinctly different values for the critical current and for the 'retrapping' current, seen during the reverse sweep from normal state back into the superconducting state. The variation of critical current and retrapping current with temperature (Figure 19(b)) has features reminiscent of a modified version of the Skocpol-Beasley-Tinkham (SBT) model [9]. For SNSPDs, this observation suggests, for example, that a 20 nm PVD TaN nanowire with a Cu encapsulation can demonstrate better reset times, since the heat is dissipated much faster.

The effect of introducing a thermal resistance was experimentally studied by adding a 25 nm thick metallic ALD TaN layer in between the superconductor and the Cu layer in the nanowire. As can be seen in Figure 19(c), hysteresis increases dramatically – and the retrapping currents are far smaller than the critical current, and the temperature dependence of these currents is shown in Figure 19(d). These measurements on PVD TaN with varying heat-sinks are in opposition to Dane *et al* [9] on NbN nanowires with different substrates (to modify heat sink capabilities), since the Ic, Ir dependance does not fit a common value of their exponent (n), as their data does. Further theoretical modeling and measurements are needed.

Cryogenic characterization of the PVD TaN nanowires down to 100 nm linewidth provides us the values for design of SNSPDs that can be incorporated into future designs of SONC circuits. In addition, the experimental confirmation that hysteresis can be completely suppressed by a suitable choice of PVD TaN and Cu thicknesses bodes well for the design of faster response SNSPDs. Finally, this work provides experimental evidence that PVD TaN SNSPDs with better than 5% variability can be fabricated with high yield across a full 300 mm wafer. The low Tc (3.3 K to 3.5 K on blanket films, and possibly as low as 2.6 K in Cu-encapsulated nanowires could also help improve the sensitivity of SNSPDs to the relative ease with which Cooper pairs can be broken by an incoming photon.

In addition to measurements at AFRL-Rome, chips from the same wafer are being characterized at Brookhaven National Lab, using a Physical Property Measurement System (PPMS) capable of reaching 1.5 K, and equipped with the ability to sweep magnetic fields up to 9 tesla. Such measurements on the 35 nm PVD TaN (N/T ~ 0.53) have shown that the coherence length is about 6 nm, with Hc (T=0) estimated at 6.5 tesla, through fitting of the data acquired to date.

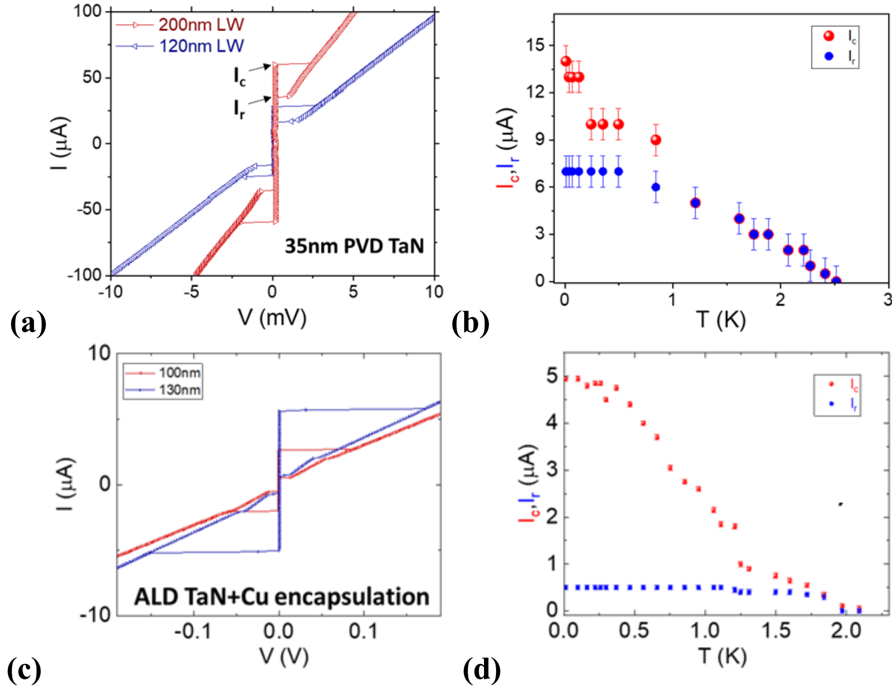


Figure 19: Comparison of encapsulated and unencapsulated TaN nanowires with (a) Hysteritic effects seen with 35 nm nanowires, with critical current and retrapping currents marked (b) Dependence of critical current and retrapping current on operating temperature (c) Critical current and retrapping currents when a thick metallic ALD TaN layer separates Cu from the PVD TaN (d) Dependence of the currents on operating temperature for nanowires with intervening ALD TaN

4.3. Characterization of Josephson Junctions at 300 K and mK temperatures

4.3.1 Blanket α–Ta films and ALD TaN films

For operation of a Josephson junction, it is necessary that the electrodes on either side of the barrier be superconducting. For tantalum to be the material used, it is imperative that Ta be present in the bcc phase. This is readily accomplished, even with room temperature sputter deposition on silicon by leveraging a TaN underlayer, which is well-known in the IC industry for Cu interconnects. A very thin layer of TaN (deposited by PVD or ALD) can be used to promote the formation of α-Ta. α-Ta is the thermodynamically stable phase at room temperature, has a bcc crystal structure, and a bulk superconducting transition temperature of 4.2 K. This team has previously confirmed superconductivity for thin films generated at Albany, with a transition temperature of 3.8 K (with thanks to Prof. Michael Hamilton of Auburn University). Figure 20 shows the XRD patterns obtained from a 200 nm thick PVD Ta film on 3 nm ALD TaN on a 300 mm high-resistivity Si wafer, confirming a bcc crystal structure for Ta.

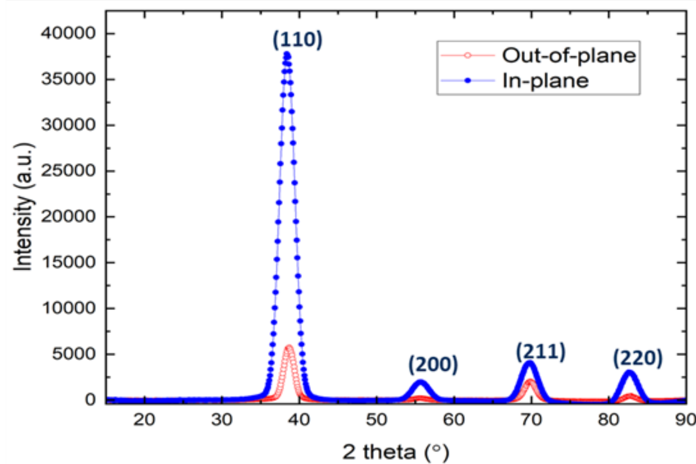


Figure 20: XRD spectrum of alpha-phase tantalum (formed by deposition of Ta on 3 nm ALD TaN on Si)

Another requirement for a Josephson junction of the Superconductor-Insulator-Superconductor type ('SIS' type) is that the tunnel barrier should be insulating at operating temperatures. The ALD TaN film that is needed in the IC industry is designed to have as high a conductivity as possible while still serving as a good diffusion barrier for copper. Hence, this team had to redevelop a new 'Quantum POR' for ALD TaN – with high resistivity, good defect performance, and without any disruption to the CMOS POR process that needs to run on the same chamber. This was accomplished by a careful study that explored lower and lower chamber temperatures, which resulted in steadily increasing resistivity of the ALD TaN film (deposited on thermal oxide of silicon to permit thickness and sheet resistance measurements). The 'Quantum POR' condition was set at 50 °C below the CMOS POR temperature, as shown by the green star in Figure 21(a) – this results in a resistivity approximately 40x higher than the CMOS POR film. Figure 21(b) shows how the resistivity of the film is not uniform across the entire wafer, but shows a central region of higher resistivity. Such a non-uniformity is present even in the CMOS POR condition, and is due to the specifics of the gas flow through the shower head. However, the deviation stays roughly the same when expressed as a percentage of the median resistance at any given temperature. Figure 21(c) shows how an 'idle' ALD chamber can be conditioned to give repeatable performance by running 6 depositions (of 25 nm for each) – these depositions can be done on a single wafer, in order to economize on wafer usage. After an equivalent of 150 nm, the resistivity distribution across wafer is stable, as shown in Figure 21(d). The particle performance is also stabilized by such conditioning, as Figure 21(e) illustrates.

The resistivity ALD TaN is sensitive to the surface chemistry of the film it is deposited on – this is the subject of a patent disclosure that is in the process of being filed by this team and co-inventors, through RF-SUNY.

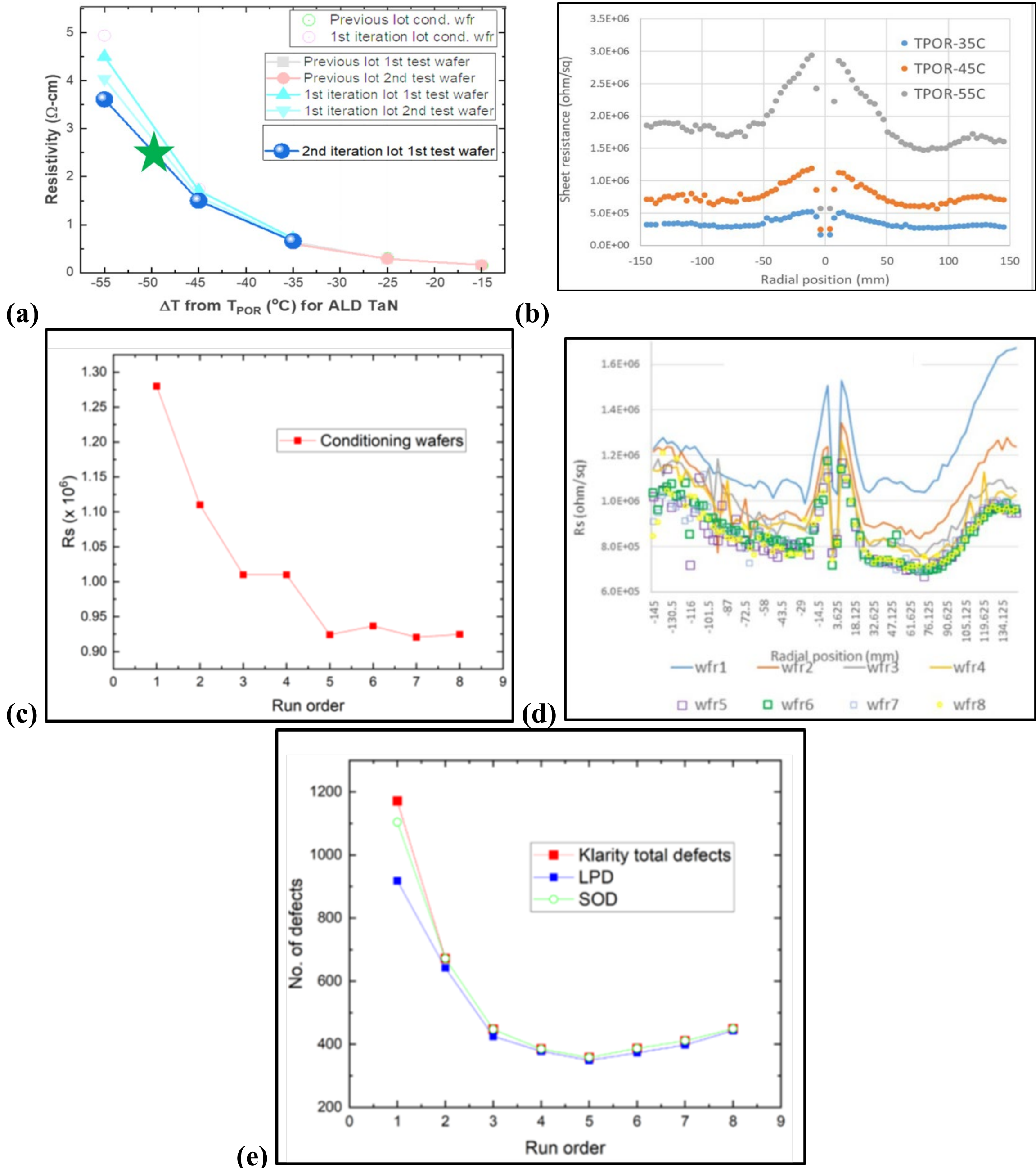


Figure 21: Plots of ALD TaN resistivity with (a) Resistivity of ALD TaN as a function of deposition temperature (b) Resistivity as a function of radial position on wafer at chosen deposition temperatures (c) Stabilization of deposition characteristics by using ' chamber conditioning' wafers at the 'Quantum POR' temperature (d) Resistivity profile over the wafer diameter is stable with conditioning (e) Defectivity stabilization with conditioning

4.3.2 Bottom Electrode Ta CMP Design Rules

One of the important results of this project, in addition to the three deliverables, was the development of a ‘Rev 0’ Design Rule manual for Ta CMP. The Process of Record (developed through multiple iterations using two different reticle sets) was successfully tested on multiple lots to confirm repeatability, along with polish time variations to confirm the process window. This POR process was confirmed to produce high quality factor coplanar waveguide resonators (>200,000) of alpha-tantalum, embedded in a silicon matrix. The POR process is equally applicable to Ta CMP conducted in a silicon oxide matrix – and can hence be used for SFQ logic circuits as well.

The POR process needs a trench depth of ~90 nm, filled with a 200 nm thick PVD Ta layer. CMP is accomplished with a combination of a hard-pad step, followed by a soft-pad step. The hard-pad step includes a reflectance based endpoint scheme that allows for the bulk removal to be less sensitive to the exact removal rate (which depends on pad age, and the concentrations of slurry constituents in the blend being used on that day). The endpoint scheme is shown in Figure 22. This is followed by a fixed time polish on a softpad, which serves to buff away scratches present after the hard-pad polish, and to address local regions of remaining metal on the field surface, since the soft-pad has a much shorter planarization length than the hard-pad (which has a much higher flexural modulus).

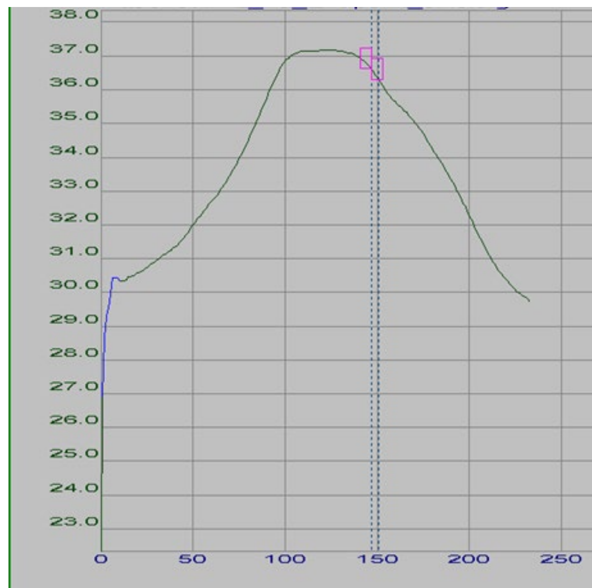


Figure 22: Ta CMP optical endpoint in hard-pad step

Electrical characterization of the Ta damascene lines created by the process of record show (Figure 23) good uniformity in resistance, and leakage across the surface of the 300 mm wafer. The resistance variation is driven by CD variation The Ta CMP design rule manual now includes tested values for the permissible area without dummy fill, and the data supporting the choice of 3 µm as the distance from a line edge where cheesing can be blocked without serious detriment to nearby features. Figure 24 shows gds images of the test structures used to gauge this effect – where varying widths of a Ta feature without any cheese

are placed immediately next to a 100 nm wide 'canary' line separated from the cheese-blocked line by 100 nm. Measurements of topography post CMP show local topography variation is less than 5 nm (Figure 25).

All of this data provides a designer with quantitative data on Ta line resistance, its variation across the 300 mm wafer, the dependence of linewidth, along with topography, leakage and other information critical for a new layout.

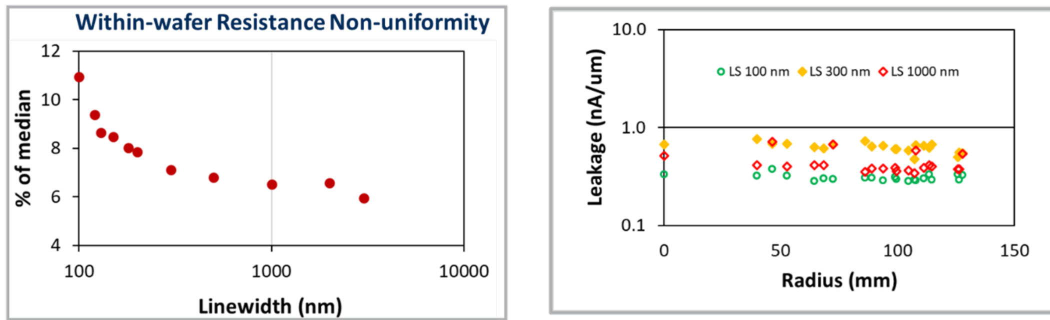


Figure 23: Plots of wafer uniformity with within wafer resistance uniformity (1 standard deviation as a % of median) on left, and leakage current per unit length as a function of radial position on the wafer on the right

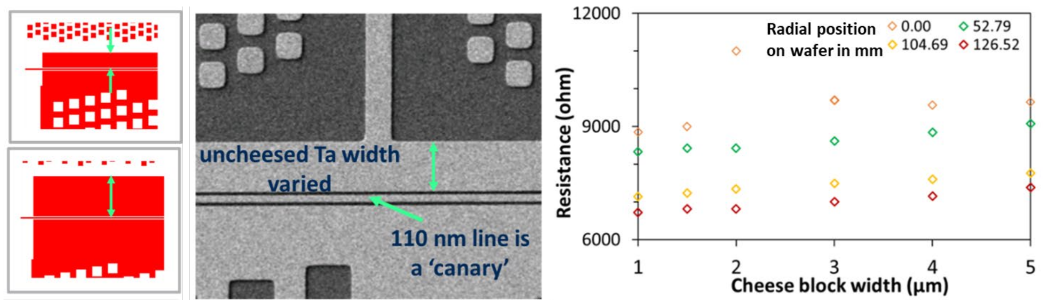


Figure 24: Effect of cheese block on resistance of a 'canary' line, when cheesing is blocked to ever greater distances from line edge

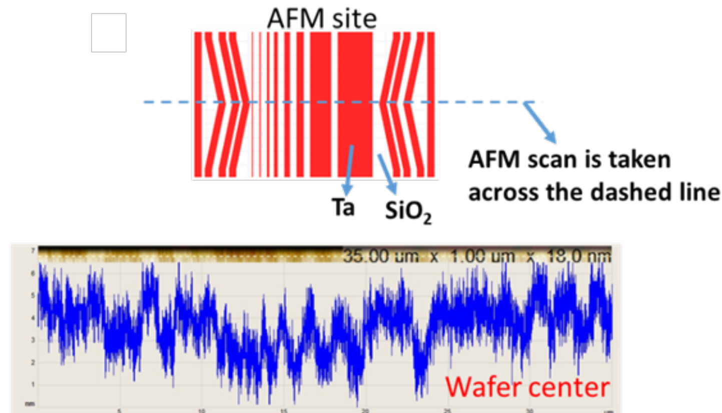


Figure 25: Atomic Force Microscope (AFM) trace showing local topography

4.3.3 Characterization of Josephson junctions at 300 K and ~10 mK

Based on learning from blanket wafers and through integrated device wafers using the new reticle (FLXNM1), Josephson junctions with a hybrid barrier composed of native oxide of tantalum and a 9 nm thick high-resistivity ALD TaN layer were fabricated. A companion wafer was fabricated, with just the native oxide of tantalum along with a low-resistance 3 nm thick ALD TaN present between the top and bottom electrodes of Ta. The 3 nm ALD TaN is metallic, and 40x *more conductive* than the tunnel barrier, and promotes the formation of alpha-Ta for the top electrode. Data from this companion wafer served to further correct for parasitic effects in resistance measurements and improve the quality of the data corresponding to the tunnel barrier – 9 nm of high resistivity ALD TaN. Yield of the junctions is well above 90%, with spec range defined 1st quartile minus 1.5*IQR to 3rd quartile + 1.5*1QR.

Figure 26(a) shows the cumulative probability distributions for cross junctions formed by the perpendicular intersection of a top electrode and bottom electrode. In the sacrificial oxide approach being used, this is accomplished by a perpendicular intersection of a nested pair of "MS" and "TE" lithographic features, with a "BE" line, as shown in Figure 26(b). Junction resistance increases monotonically as the junction size is reduced. The distributions shown in this figure are from the measurements made at 25 dies distributed across the wafer, as shown in Figure 26(c).

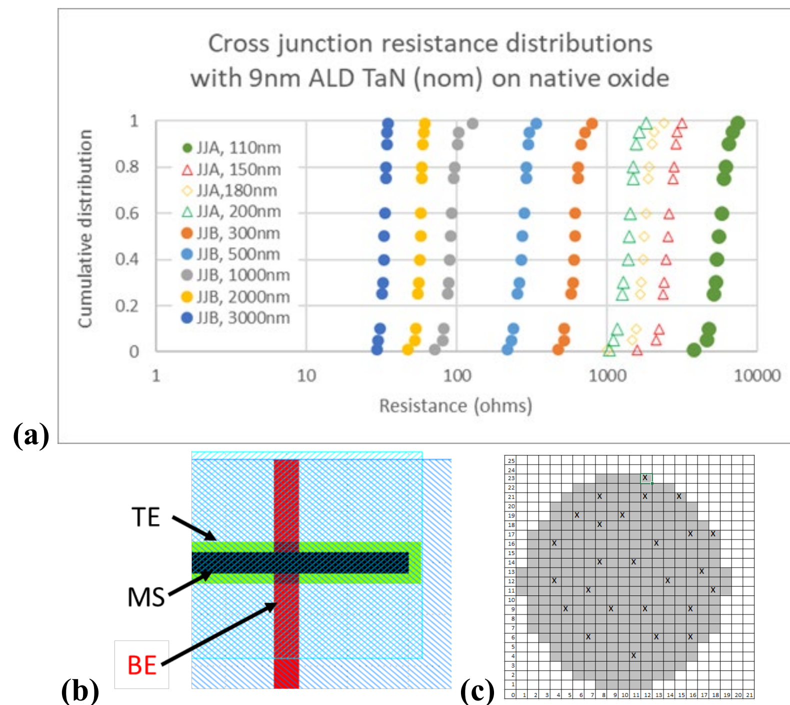


Figure 26: Diagram of results for cross junctions with (a) Cumulative probability distributions of cross junction resistance at room temperature (b) layout of a cross junction (c) Inline electrical test positions

The resistance of ‘bridge’ junctions, measured by a similar inline electrical test program is shown in Figure 27(a), in the form of a cumulative probability distribution. Figure 27(b) provides a schematic of the junction, illustrating how the MS level alone is used to form the junction. The MS level forming the junction is a island (rectangle, square, or a more complex feature as will be described later in this section). The island is placed on top a BE line, and is connected to the rest of the circuit by a TE-only ‘bridge’. This ‘architecture’ ensures that the tantalum top electrode line, defined by the TE pattern is always anchored to silicon (or to bottom electrode Ta) by the MS trench, except in those carefully-controlled areas where the MS pattern is deliberately cut away to form a TE-level ‘bridge’. Bridge length in this reticle was limited to ensure that no wholesale ‘liftoff’ of the TE pattern occurred, causing particle problems in the processing and metrology tools. Bridge length was varied from 100 nm in the JJC and JJD macros, to 200 nm in the JJE and JJF macros, to 400 nm in the JJG and JJH macros (not included in Figure 27(a) for clarity – trends in these macros are similar to those shown). It is heartening to note that the junction resistance is largely independent of bridge length, as it should be – differences are less than ~10%. As mentioned previously, bridge junctions have the advantage that the Cooper pair tunneling occurs only across a planar geometry – while the cross-junctions have a corner at the edge of the Ta line where potential risks for reliability might exist.

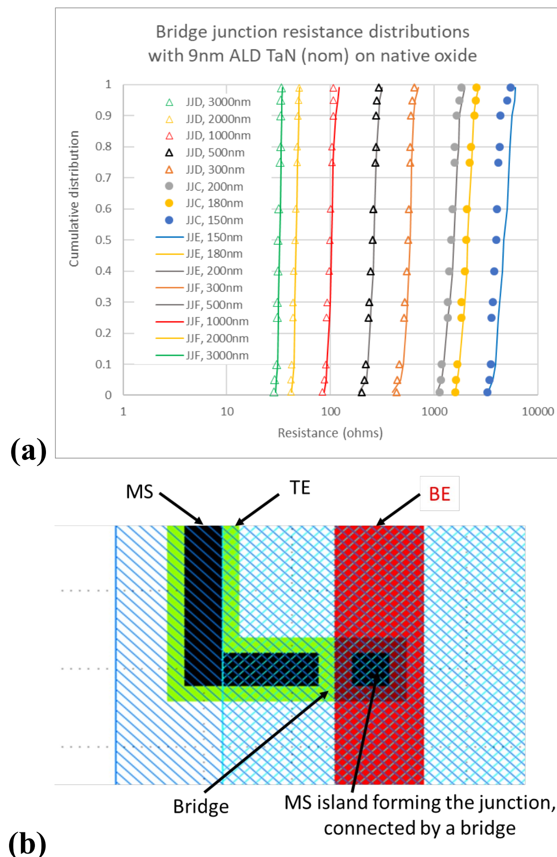


Figure 27: Diagram of results for bridge junctions with (a) Cumulative probability distribution of bridge junction resistances for varying geometries (b) layout schematic of bridge junctions

In order to see if bridges of greater length could be safely formed, a single test macro that explored bridges of 1000 nm length was included – as can be seen in Figure 28, structural integrity of the bridge is good (and verified across multiple locations on multiple wafers). There is relatively little 'sag' of the 1000 nm long bridge – suggesting that it can be used for such 'air-bridges', with applications such as connecting ground-planes across a resonator line in qubit architectures to improve coherence times. Such features are not needed in SONC circuits where connections can be made with oxide supporting the Ta lines, but having a process flow that can serve multiple needs with simple modifications makes a future Process Design Kit/Design Rule Manual more adaptable and useful.

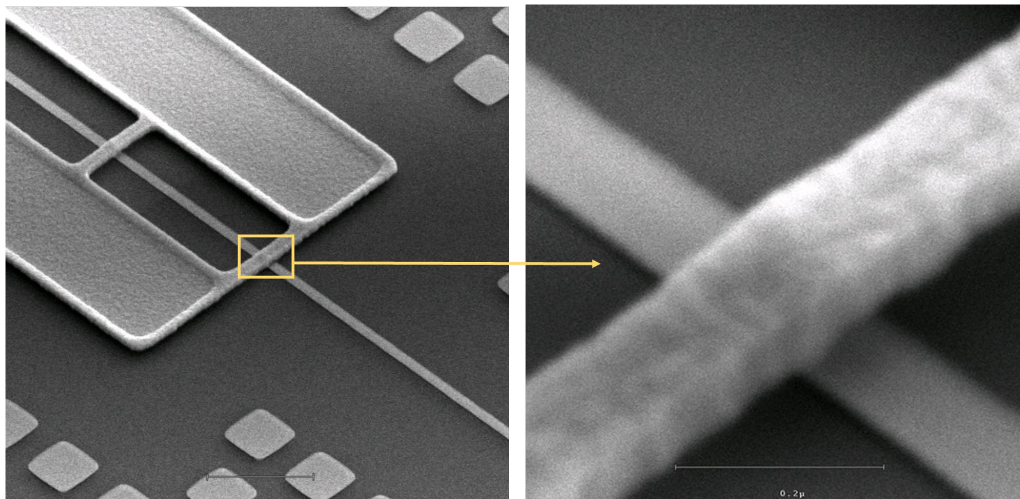


Figure 28: Test structure to check bridge integrity at longer lengths

In Figure 29 below, the very important criterion of within-wafer junction resistance uniformity is characterized. For both cross and bridge junctions, the within-wafer nonuniformity follows a similar pattern, reaching values lower than 4% for large junctions, and increasing to 15% for the smallest junctions.

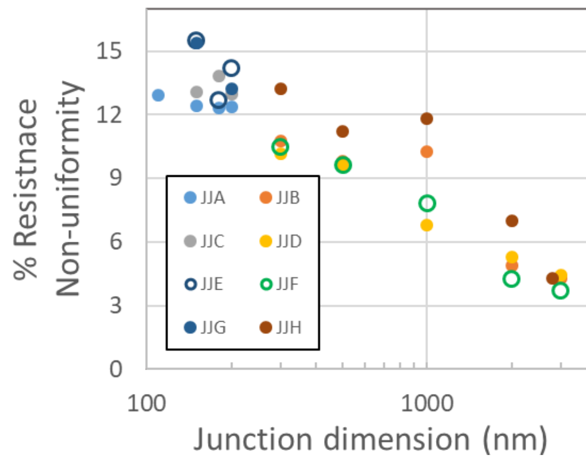


Figure 29: Junction resistance non-uniformity as a function of junction size and for different architectures (cross junctions, and bridge junctions of different bridge lengths)

This indicates that, for junctions larger than 300 nm on a side, the threshold criterion of this project has been achieved. For junctions 3 µm on a side, the non-uniformity is close to the target value of 3%. Through improvements in RIE-induced CD variation across the wafer and improving the line-edge roughness power-spectrum in lithography, it should be possible to further improve the non-uniformity of the smaller junctions.

The reticle also included linear series of junctions of varying lengths – 6 junctions, 30 junctions and 78 junctions. Such an array of JJs in series is an excellent test for JJ-opens. As Figure 30 indicates, several thousand junctions have been successfully tested against the opens metric. Shorted junctions would reveal themselves more clearly in series tests of 6 JJs, and again, Figure 30 shows that such junctions are well behaved. The numbers in red indicate the junction size. The cause of high resistances in the 500 nm junction arrays needs to be investigated – such high points are found exclusively along two columns of die (5 die to the left and 5 die to the right of wafer center). Notwithstanding this effect, the data indicates excellent yield.

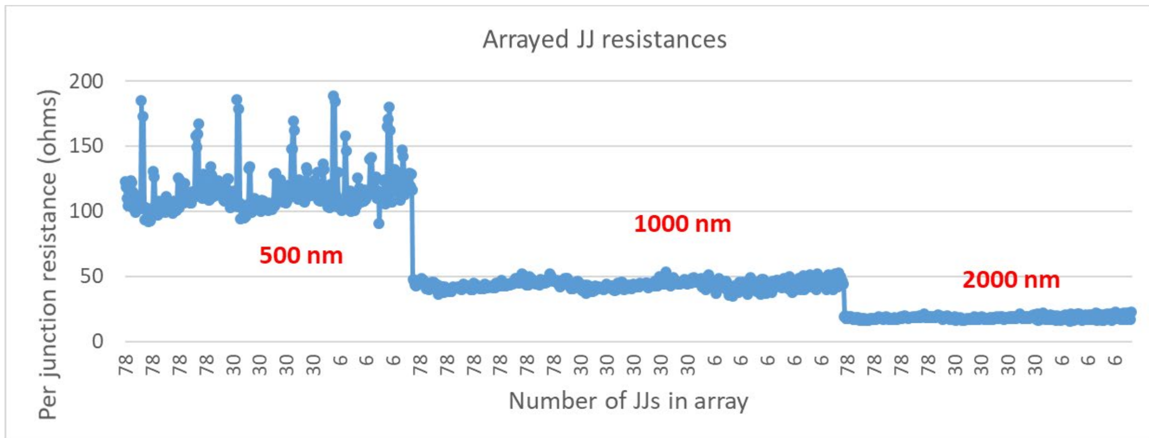


Figure 30: Per junction resistance of arrays of junctions connected in series, with varying numbers of junctions in each array; the numbers in red correspond to junction size

In order to separate the potential effect of the edge of the junction from the area of the junction, a macro was designed with the same nominal junction area, but with greatly increased perimeter, as shown in Figure 31(a). The areas that are 'cut-out' in each case are the same, just grouped together into fewer 'cuts' to reduce the resulting perimeter. The measured resistance of the junctions with different perimeters is shown as a cumulative probability distribution plot in Figure 31(b), indicating that increasing perimeter does not change the resistance of the junction. Hence current flowing (at room temperature) across the junction flows uniformly over the area of the junction, rather than preferring the edge.

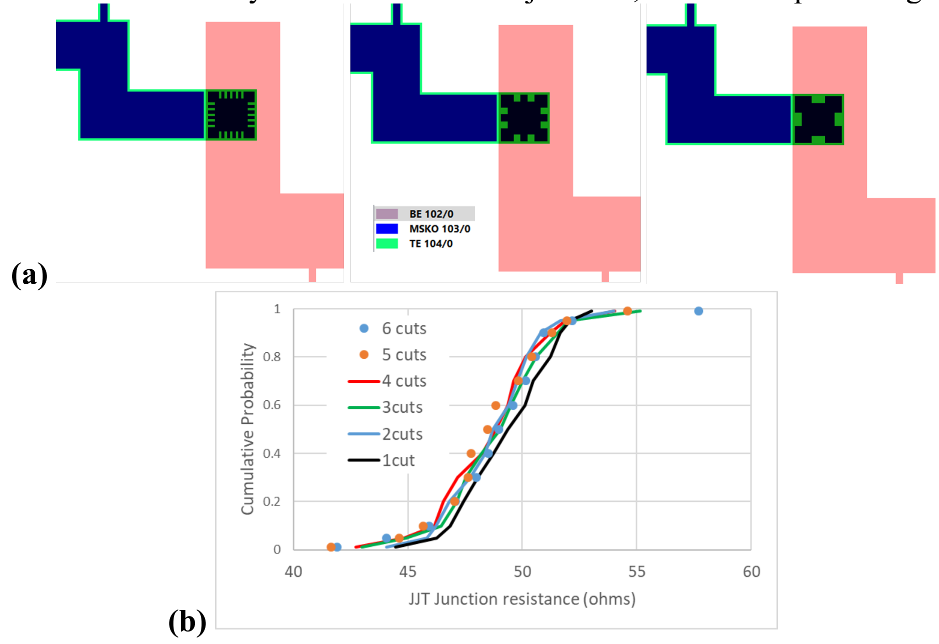
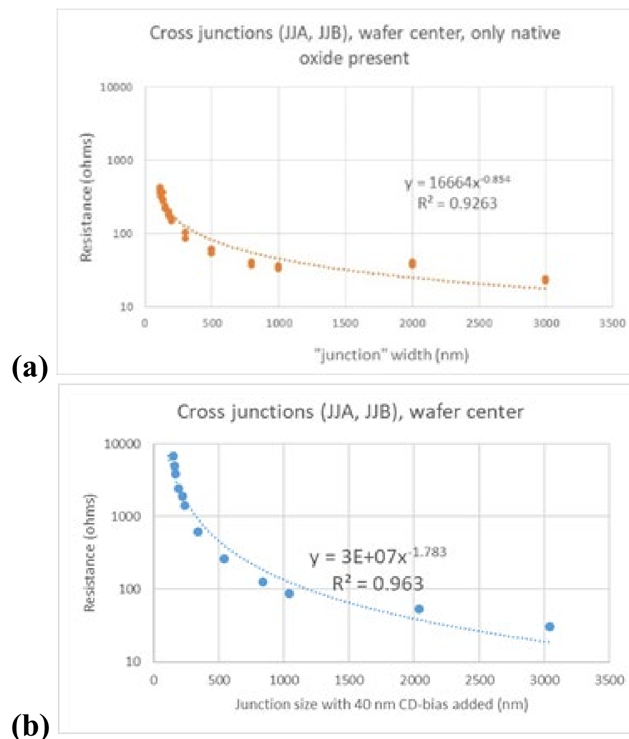


Figure 31: Results of junction edge vs area investigation with (a) Layout of the junctions to explore influence of junction edge vs area (b) Cumulative probability distributions of resistance for the junctions with different perimeters, but the same nominal area

We now tackle the (small) effect of the native oxide that is present in the hybrid junction that is used in these JJs, which contributes to room temperature resistance. We note that the small remaining lengths of lead wire form a part of the measured junction resistance. To first order, subtracting the resistance contributions of the native oxide and few micron long lead wires, and the metallic ALD TaN should sharpen the understanding of the hybrid junction resistance behavior.

Using a wafer that was run with no ALD TaN, but with only the native oxide, measurements of the "junction resistance" were made. The results are shown in Figure 32(a), showing resistance as a function of junction size for the wafer center die, for cross junctions. In Figure 32(b), the corresponding resistances for the full hybrid junction are shown (cross junctions, at wafer center die). It can be seen that while the native oxide resistance is smaller than the full hybrid junction (from 5% for the smallest junctions to 70% for the largest junctions where overall resistances are already small), the variation as a function of size is substantial enough that subtracting its effects will yield useful information. Figure 32(c) focusses on the resistance of bridge junctions of varying sizes for the native oxide-only wafer, while Figure 32(d) provides the corresponding data for the full hybrid junction, again for the die at the wafer center alone, for clarity. In all cases, a power law fit is included, and it can be seen that the resistance does not scale as length ^-2, as would be expected if the measured junction resistance depended solely on junction area.



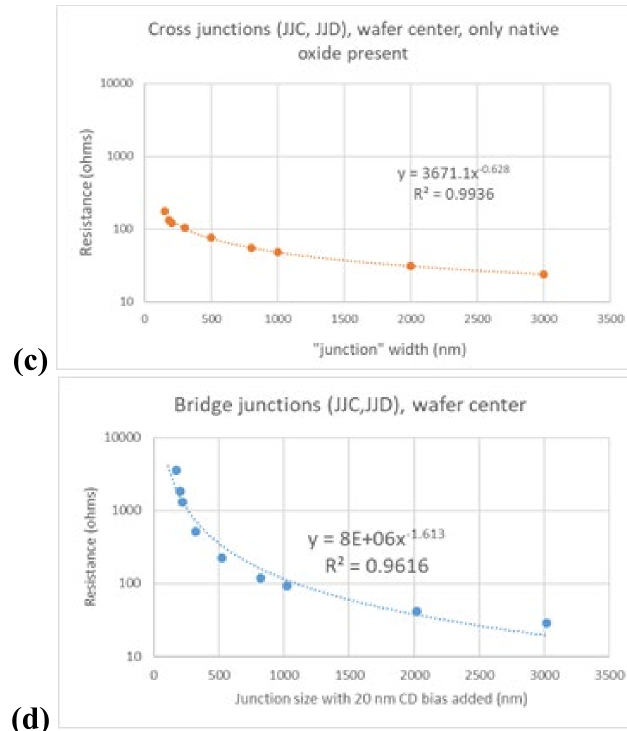


Figure 32: Plots of cross and bridge junction resistance with (a) cross junction resistance vs junction size, wafer center, native-oxide only (b) cross junction resistance vs junction size, wafer center, full hybrid barrier (c) bridge junction resistance vs junction size, wafer center, native-oxide barrier only (d) bridge junction resistance vs junction size, wafer center full hybrid barrier

While acknowledging that the native oxide-only data comes from one wafer, and the full hybrid barrier data (necessarily!) comes from a different wafer, it is possible to subtract one from the other. Most of the remaining processes for these two wafers were run together (when the wafers were run as one “lot” through the line), which makes other effects less significant, and supports such a subtraction. In Figure 33, the result of such analyses is shown for both cross junctions and bridge junctions. In both cases, the power-law fit with an exponent close to -2 is remarkably tight. This is a result that has been achieved for the first time, in the late days of this project, and bodes well for cryogenic operation of such devices.

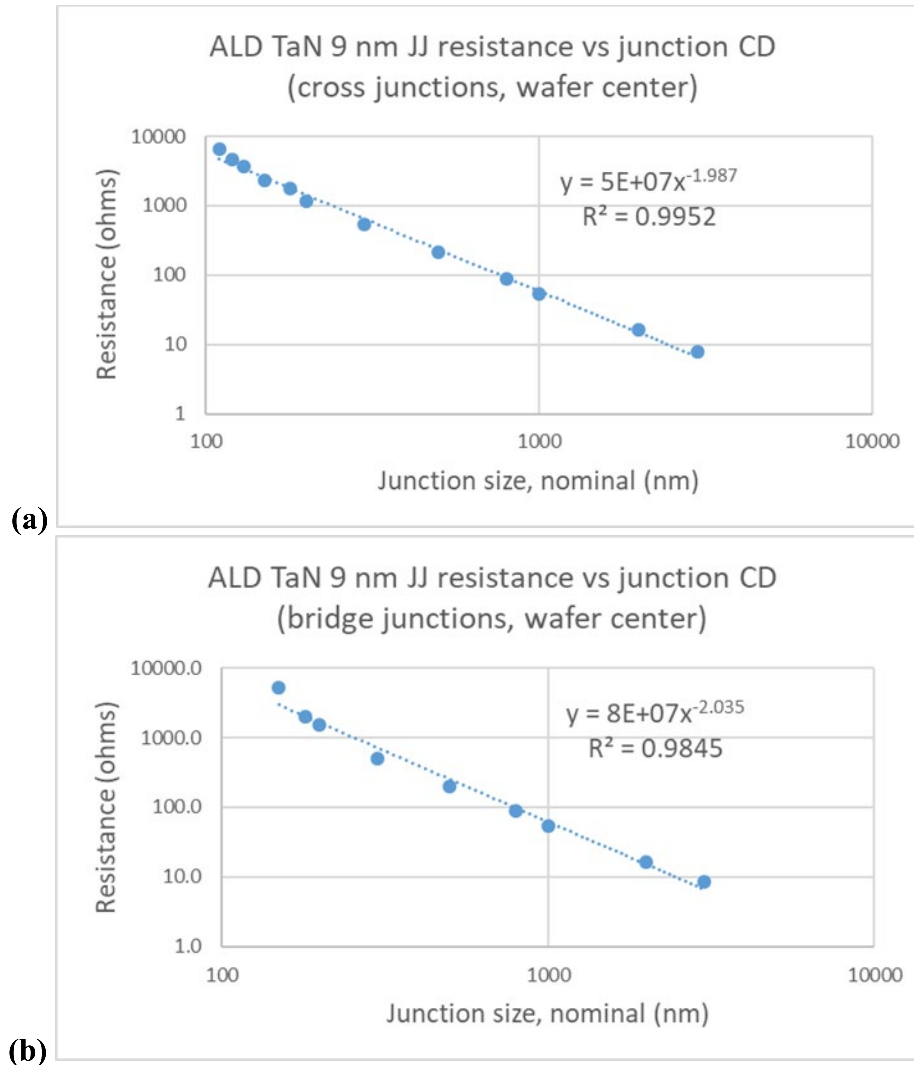
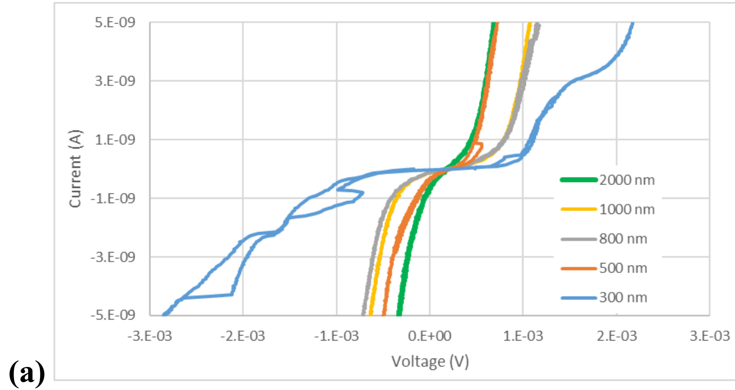


Figure 33: Plots of corrected junction resistances to reflect the influence of the ALD TaN barrier for (a) cross junctions and (b) bridge junctions in the die at the wafer center

The hybrid junction was packaged by Dr. Lombardi and tested in the dilution fridge at the Innovare Advancement center. Cross junctions in the JJB macro were tested. The I-V curves obtained are shown in Figure 34(a), and show that the critical current of the junction is too small to be measured. These 'clean' measurements of I-V traces were made possible by the use of high-quality passive filtering schemes at cryogenic temperatures (via QDevil® QFilter). Previous attempts to make DC measurements of JJs (at multiple sites) were bedeviled by noise.

The junction shows normal resistance at higher voltage values. Such rounded I-V curves for low Ic junctions are expected [10], as shown in Figure 34(b), due to the ratio of Ic*h/kT being low, where Ic is the critical current, h is the Planck's constant, k is the Boltzmann constant and T is the junction temperature.

(a)



(b)

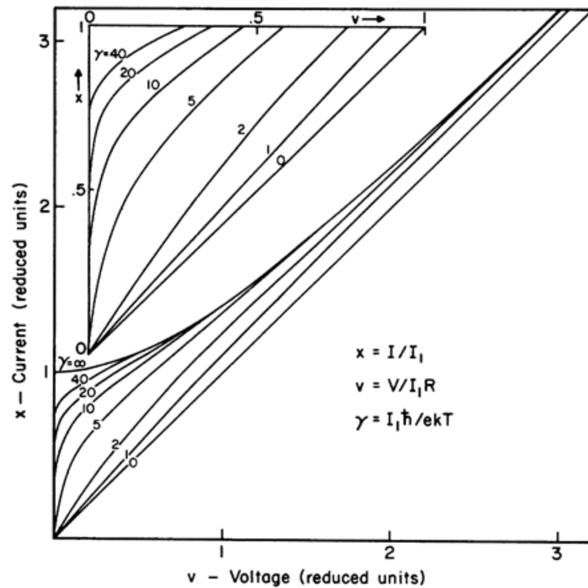


FIG. 1. Current-voltage characteristic of Josephson junction, including average noise voltage, based on Eq. (9). The inset contains an expanded version of the region $0 < x < 1$, $0 < v < 1$.

Figure 34: Plots for I-V characteristics of the tested JJs with (a) I-V characteristics of various JJs in the JJB macro, with 9 nm ALD TaN on native oxide of Ta, measured at millikelvin temperatures. (b) I-V characteristics predicted for low Ic junctions (from [10])

It is interesting to note that the resistance of these junctions (when driven normal) at millikelvin temperatures is between 10 kiloohms and 40 kiloohms. In contrast, at room temperature, these junctions had much lower resistance (between 100 and 3000 ohms). This additional observation can help explain why the Ic of the JJs was so low. The resistance of the ALD TaN tunnel barrier, when measured at room temperature, is much lower than its resistance at cryogenic temperatures because the energy barrier that the Cooper pairs must tunnel through is much lower than is the case with Al/AlO/Al junctions. Wilt *et al.*[11] report that the energy barrier for Al/AlO junctions is the order of 1 to 1.4 eV. In the case of ALD TaN, the energy barrier (the difference between the conduction band-edge of ALD TaN and the Fermi level of the Ta) is possibly lower. Hence, by targeting room temperature resistance, the thickness of the tunnel barrier was increased to 9 nm. In order to have the

desired normal resistance for the junction at cryogenic temperatures, we would need to have much thinner ALD TaN films (say 1 to 4 nm). These will be targeted in work (outside this project) that is anticipated to be completed in Jan 2023, and will be measured by partners in dilution fridges if possible by Q1 2023. The jumps in I-V curves visible in the 300 nm JJ (and to a lesser extent in some other junctions) were confirmed in repeated measurements– and may be an indication of phase slips [12,13] – though, clearly, further measurements at millikelvin temperatures with targeted values of JJ resistance will need to be done to confirm that hypothesis.

5.0 CONCLUSIONS

In this project, we developed three critical circuit elements (superconducting nanowires, W-center 1.22 µm emission centers, and Josephson junctions) for superconducting optoelectronic neuromorphic computing at 300 mm wafer scale using CMOS-fab compatible materials and processes. Project criterion specified a target non-uniformity of 3% and a threshold non-uniformity of 10%. The target value was reached for W-center emission at 25 K, while room temperature resistance variation of superconducting nanowires came close at ~4%. Josephson junctions of large area reached 4%, while meeting the threshold non-uniformity of 10% for junctions of 500 nm size. Cryogenic measurements of superconducting nanowires provided values of critical current density (~0.25 MA/cm^2 for 20 nm thick nanowires, and 0.8 MA/cm^2 for 35 nm thick nanowires). Due to in-situ capping with copper, interesting observations were made of conditions where the retrapping current was the same as the critical current – leading to non-hysteretic behavior and (future) faster response in SNSPDs. Cryogenic measurements of JJs showed that Ic was unmeasurably low, likely due to excessive thickness of ALD TaN used (9 nm). It is expected that thicknesses ~ 1 to 4 nm ALD TaN will show the requisite hysteretic I-V curves, with measurable values of Ic, in the near future. This is anticipated to be completed in the near term (Jan/Mar 2023). The project also saw the development of a design rule manual for Ta bottom electrodes that can be used for multiple SONC levels (and for qubits). Yield for fabricated devices that were compatible with electrical test (JJs and nanowires) was well above 90%.

The success of this project can be used in the future for the design of an SONC reticle set to demonstrate functional neurons that demonstrate integrate-and-fire, spike-timing-dependent plasticity, and responsivity to external input of 'learning weights'. This can be followed by increasingly more complex SONC circuits, leading to a visual cortex or similar systems of utility.

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APPENDIX A – PUBLICATION (INCLUDING MANUSCRIPTS IN PREP)

1) Sonia M. Buckley, Alex N. Tait, Galan Moody, Stephen Olson, Joshua Herman, Kevin L. Silverman, Satyavolu Papa Rao, Sae Woo Nam, Richard P. Mirin, Jeffrey M. hainline, "Optimization of photoluminescence from W centers in silicon-on-insulator", *Optics Express*, **28** (11) pp. 16057-16072 (2020)
2) Ekta Bhatia, Jack Lombardi, Soumen Kar, Michael Senatore, Steve Olson, Tuan Vo, Sandra Schujman, Jakub Nalaskowski, Hunter Frost, John Mucci, Brian Martinick, P. Y. Hung, Ilyssa Wells, Thomas Murray, Corbet Johnson, Aleksandra Biedron, Vidya Kaushik, Dan Campbell, Matthew LaHaye, Satyavolu Papa Rao, " Ul-tra-thin TaN Damascene Nanowire Structures on 300 mm Si Wafers for Quantum Applications", (manuscript in prep, for Quantum Sci. & Technol.)
3) Ekta Bhatia, Soumen Kar, Jakub Nalaskowski, Tuan Vo, Steve Olson, Hunter Frost, John Mucci, Brian Martinick, P. Y. Hung, Ilyssa Wells, Sandra Schujman, Satyavolu Papa Rao, " Chemical Mechanical Planarization for Ta-based Superconducting Quantum Devices" in (*manuscript in prep, for Jour. Vac. Sci & Tech. B)*

APPENDIX B – PRESENTATIONS

1) Meeting name: Single Photon Workshop
   Purpose: Public Conference
   Location: Milan, Italy
   Date: Oct 21-25, 2019
   Attendees from this project: None
   Author list: S. M. Buckley, A. N. Tait, G. A. Moody, K. L. Silverman, S. Olson, J. Herman, S. Papa Rao, S. W. Nam, R. P. Mirin, and J. M. Shainline
   Presentation: "Optimization of Si emitters for cryogenic light sources"

2) Meeting name: American Vacuum Society 66th International Symposium and Exhibition
   Purpose: Public conference
   Location: Columbus, OH.
   Date: Oct 20-25, 2019
   Attendees from this project: Satyavolu S. Papa Rao
   Author list: S. Olson, C. Hobbs, H. Chong, J. Nalaskowski, H. Stamper, J. Mucci, B. Martinick, M. Zhu, K. Beckmann, I. Wells, C. Johnson, V. Kaushik, T. Murray, S. Novak, S. Bennett, M. Rodgers, C. Borst, N. Cady, M. Liehr, and Satyavolu S. Papa Rao
   Presentation: "Materials and Fabrication Challenges for Neuromorphic and Quantum Computing Devices"

3) Meeting name: Q4I
   Purpose: Public conference
   Location: Rome, NY
   Date: July 12-14, 2022
   Attendees from this project: Ekta Bhatia, Soumen Kar, Satyavolu S. Papa Rao
   Author list: E. Bhatia, S. Kar, H. Frost,S. Olson,B. Martinick, D. Ashworth, J. Mucci, W. Collison, T. Vo, H. Chong, J. Nalaskowski,I. Wells, P.Y. Hung, K. Beckmann, M. Liehr, C. Johnson, T. Murray, S. Schujmann, A. Biedron, N. Cady, V. Kaushik, C. Borst, S. Papa Rao
   Presentation: "R&D of Scalable Quantum Technologies at NY CREATES"

4) Meeting name: Foundations of Superconducting Digital Logic (SDL)
   Purpose: Private Meeting with Dr. Rory Perkins (LPS) re: future BAA on SDL
   Location: Albany, NY
   Date: Sept 6, 2022
   Attendees from this project: Satyavolu S. Papa Rao
   Author list: Ekta Bhatia, Soumen Kar, Satyavolu Papa Rao
   Presentation: "imec/NY CREATES/Jefferson NL/Cornell Univ Joint SDL Proposal to LPS"

5) Meeting name: American Vacuum Society 68th International Symposium and Exhibition
   Purpose: Public conference
   Location: Pittsburgh, PA

Date: Nov 6-11, 2022

Attendees from this project: Ekta Bhatia

Author list: Ekta Bhatia, Soumen Kar, Stephen Olson, Tuan Vo, Sandra Schujman, Jakub Nalaskowski, Hunter Frost, John Mucci, Brian Martinick, P. Y. Hung, Ilyssa Wells, Thomas Murray, Corbet Johnson, A. Biedron, Vidya Kaushik, Satyavolu Papa Rao

Presentation: "Ultra-thin TaN Damascene Nanowire Structures on 300 mm Si Wafers for Quantum Applications"

APPENDIX C – ABSTRACT

In this project, three critical circuit elements (superconducting nanowires, W-center 1.22 µm emission centers, and Josephson junctions) for superconducting optoelectronic neuromorphic computing (SONC) at 300 mm wafer scale using CMOS-fab compatible materials and processes. W-center photoluminescent emission (at an operating temperature of 25 K) of 1.22 µm light with <3% across-wafer non-uniformity was demonstrated. Physical vapor deposited TaN nanowires showed <4% across-wafer non-uniformity in room temperature resistance, and critical current density of 0.25 MA/cm^2 for 20 nm thick nanowires. Cu-encapsulation showed non-hysteretic behavior in the nanowires. Josephson junctions with superconducting α-Ta electrodes and ALD TaN as the tunnel barrier showed resistance dependence that scaled precisely as inverse-squared with junction dimension, as expected. Junctions of 2 µm showed within wafer non-uniformity of ~4%, while junctions larger than 500 nm had non-uniformity better than 10%. Cryogenic measurements indicated that the tunnel barrier thickness of 9 nm was too thick for determination of Josephson junction critical current but showed an I-V trace that was otherwise supportive of an SIS junction. Yield of the electrically tested structures exceeded 90%. The successful fabrication of these sub-components prepares the ground well for future integration of SONC systems.

7.0 LIST OF SYMBOLS, ABBREVIATIONS, AND ACRONYMS

AFRL	Air Force Research Lab
ALD	Atomic Layer Deposition
BOX	Buried Oxide (layer)
CD	Critical Dimension
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Planarization
GIXRD	Glancing Incidence X-Ray Diffraction
IC	Integrated Circuit
JJ	Josephson Junction
LED	Light Emitting Diode
NIST	National Institute of Standards and Technology
OES	Optical Emission Spectroscopy
POR	Process of Record
PVD	Physical Vapor Deposition
R&D	Research & Development
RF-SUNY	Research Foundation for the State University of New York
RIE	Reactive Ion Etch
RTCVD	Rapid Thermal Chemical Vapor Deposition
SEM	Scanning Electron Microscopy
SFQ	Single Flux Quantum
SNSPD	Superconducting Nanowire Single Photon Detector
SOI	Silicon On Insulator

SONC	Superconducting Optoelectronic Neuromorphic Computing
STTR	Small Business Technology Transfer
TEM	Transmission Electron Microscopy
XPS	X-ray Photoelectron Spectroscopy
XRD	X-Ray Diffraction
XRR	X-Ray Reflectometry