Silica Based Inorganic Composite for Heterogenous Integration

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Abstract— **Currently, there is strong demand across government and commercial sectors for high densification of microelectronic systems. Wafer level packaging and heterogenous integration strategies provide a potential solution for tighter integration and higher densification of electronics. However, conventional packaging materials are limiting the ability of these techniques to address the advanced needs of microelectronics fabrication. These limitations predominately stem from the organic-based chemistries that traditional packaging materials are composed of. These organic-based packaging materials have high coefficients of thermal expansion, complex deposition processes, and have low compatibility with further microfabrication steps. Due to the organic nature of these materials, they also outgas, have low thermal stability, and poor mechanical stability. In this work, we describe a new inorganic-based silicate composite material that can be deposited in thick layers (10-20µm) through air spray, casting, and spin coating. This material is synthesized with clean room grade starting materials ensuring insertion into existing microfabrication process flows. After cure, this material has thermo-mechanical, chemical and RF properties comparable to a quartz silica. Broadly, we find that this material will be of significant use for high density CMOS compatible systems, and also specifically high-density phased arrays.**

Keywords—CMOS, Wafer level packaging, microelectronics, RF.

I. Introduction

Lower size weight and power (SWaP) microelectronics are continuously evolving for advanced devices. One significant challenge in reducing SWaP constraints of advanced microelectronic systems is through wafer level packaging and heterogenous integration strategies. Traditionally improvements in densification of microelectronics have been driven through improvements of advanced tooling to produce higher resolution features within devices. Although there are constraints with only utilizing 2D or one layer fabrication for next generation microelectronics.[1] Heterogenous integration in three dimensions has emerged as an attractive approach for achieving superior active component density, higher efficiencies due to shorter electrical interconnects, and greater complexity through the combination of a wide range of devices [2].

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Commonly utilized 3D integration approaches are a mixture of through silicon-vias, die bonding, and packaging/molding [3]. Packaging compounds are predominately utilized in fan-out wafer level packaging (FOWLP) in order for encapsulation of commercial off the shelf (COTS) components within high density devices. Molding materials allow for assembly of 3D microsystems with flexible geometric layouts. Currently conventional mold compounds are limited due to outgassing, CTE mismatch, and low thermal stability for conventional CMOS processing [4]. In addition, conventional mold compounds are difficult to process, and in general are too thin (<2 µm) to perform as a structural component required for 3D integration [5]. Overall there is a need to develop a mold compound that can overcome these traditional challenges.

In previous work, we developed a novel inorganic composite molding material for heterogenous 3D integration. The material composition was composed of a liquid alkali sodium silicate binder with silica particles. Creating an inorganic glass composite with a thermal stability above 1000°C after a 250°C cure, a CTE of 4.9 ppm/°C, minimal outgassing, and the ability to readily make thick films [6]. These meet the requirements needed for a next generation mold compound. For a wide applicability in CMOS compatible cleanrooms, trace element reduction is required.

Our current work addresses the sodium contamination issue in the binder chemistry, by utilizing clean room grade materials to synthesize a novel binder and particle composite. This approach utilizes polydiethoxysiloxane polymer which has been synthesized from tetraethyl orthosilicate precursor. This polymer has been synthesized from clean room grade materials while targeting similar properties as the sodium silicate-based material.

As shown in Fig. 1, the nanoparticles are dispersed into a solution with hydrolyzed (acid treated) polydiethoxysiloxane in water and alcohol. As water and alcohol evaporate during the molding process, the metastable silicate molecules condense

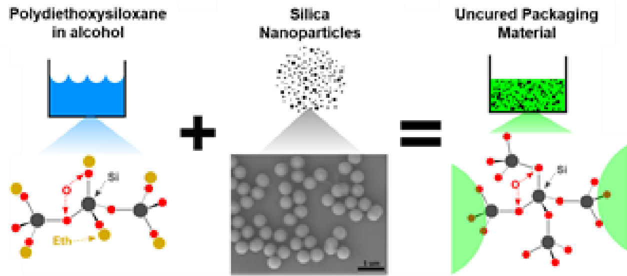


Fig 1. Hydrolysate PDS and incorporation of monodispersed Silica nanoparticles from the Stöber process to fabricate the uncured packaging material

around the nanoparticles and components on the wafer to form a solid composite matrix as depicted in Fig. 1. The nanoparticle fillers within the molding material serve multiples roles. First, the nanoparticles can be used to alter the viscosity of the molding fluid allowing for a wide variety of processing methods. Such as spray coating, spin coating, casting, compression molding and 3D printing. Second, the particles can be used to alter the CTE and electromagnetic characteristics of the molding material. Finally, the nanoparticles serve a structural role within the composite and reduce the shrinkage of the molding material by limiting the water content in the solution. We describe here how this versatile material system can be tailored for a wide range of 3D integration applications.

II. Microfabrication Compatibility

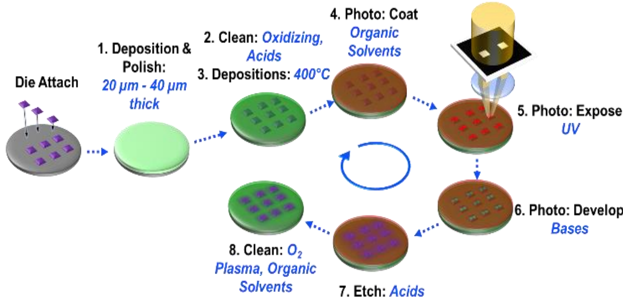
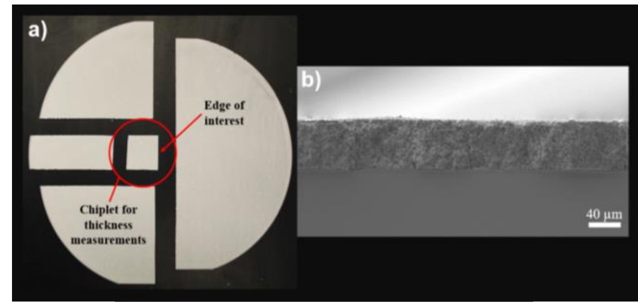


Fig 2. Process flow of microfabrication process where dies are required for fabrication.

The traditional process flow for microfabrication processes where dies are required can be consolidated into eight steps, this is noted in Fig 2. With a wafer, dies are adhered and applied to a wafer. After the dies are deposited, deposition of the material can occur on top of the wafer. Planarization of the material is required followed by cleans oxidizing environments and depositions which require the material to have robust thermal stability. After these steps traditional photolithography and development steps can occur to pattern the material for required features and integration for an additional layer. This process flow can be repeated to enable 3D integration.

A. *Thick Film Processing*



Substrate Material	Blade Height (mm)	Thickness (µm)	
		Avg	*Std*
Silicon	3.75	17.7	0.4
	3.775	26.2	0.7
	3.80	34.8	0.5
	3.825	48.5	0.8
	3.85	61.4	0.8
	3.90	81.4	2.4

Fig. 3 Thick film processing of PDS + Silica composite to produce thick and uniform films on various samples.

Ideal molding materials can be formed into thick layers (10sto 100s of µm) in order to completely embed die and afford the next surface for the following microfabrication processes. Figure 3 demonstrates the processing of the silicate composite material into thick films using precision doctor blade casting of a 60 % w/w PDS loaded with silica nanoparticles produced individual films with strong adhesion to silicon. By adjusting the blade height, we can increase the thickness of the film from 17.7-81.4 µm.

B. *Gap Fill*

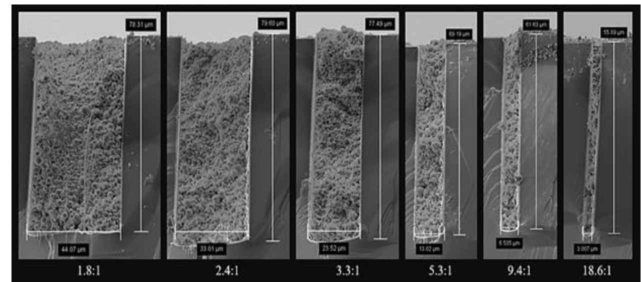


Fig. 2. SEM micrographs depicting PDS composite gap fill at various aspect through compression molding.

During the 3D integration process, gaps between assembled components can be a major source of structural failures in devices. Molding materials should completely fill gaps (<10 µm wide and >50 µm deep) between die components so that there are no voids or air pockets exist in the device. In Fig 3 we utilized compression molding to fill multiple vias with various aspect ratios. A 80w/w% PDS loaded with Si800 particles was loaded onto a silicon wafer with high aspect ratio vias. Pressure

was applied to the wafer with a ½'' thick Teflon plate was put into a vacuum chamber to pull at -14 psi. Overall even the highest aspect ratio vias were filled with this approach.

C. Photolithography and Patterning

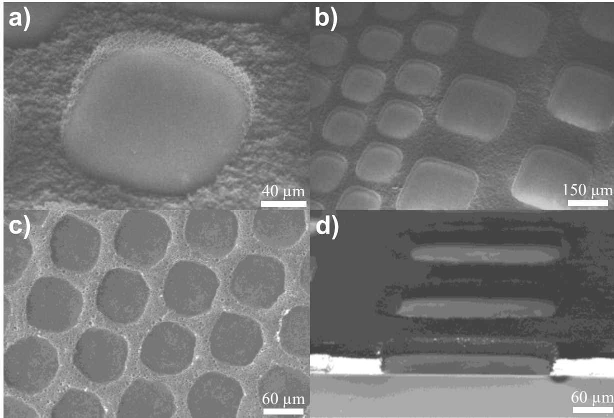


Fig. 3. SEM micrographs describing the ability of the composite to go through photolithography processes in order to pattern various squares at different dimensions.

Patterning of molding materials allows for more tightly integrated designs. In Fig 4. We demonstrate the ability to apply photoresist on top of film of silicate composite, pattern squares at various sizes and etch with an HF buffer etchant. We see that we can successfully pattern and etch features of squares with dimensions ranging from 50-200 µm in length. And can control the wet etch to resolve features to the silicon substrate. In Fig 4c consists of 50 µm squares, and there is a noticeable change in the resolution of the etch. This is most likely due to the photoresist chosen.

III. Tailoring of Materials Properties

A. Coefficient of Thermal Expansion

Data Pairings		**CTE (ppm/°C)**		
GaAs	*Silicon*		*Avg*	*Std*
Sample 1	Sample 1	3.016	2.968	0.054
Sample 1	Sample 2	3.013		
Sample 2	Sample 1	2.923		
Sample 2	Sample 2	2.918		

Fig 5. CTE measurements from 60 wt% Silica Particles with PDS composite on GaAs and Silicon wafer bow testing

The CTE of molding material must be tunable to prevent stress build up and potential cracking or delamination when integrated with substrate materials such as silicon, gallium arsenide, etc.. Commonly, the CTE should be lower than 10 ppm/°C to effective serve as a molding material. We chose silica nanoparticle fillers to modifying the CTE of the composite to attempt to closely match the CTE of silicon. Fig. 5 depicts results generated from stress-temperature curves of the silicate composite on silicon and gallium arsenide substrates. These values were used to estimate the CTE of the composite to be approximately 2.968 ppm/°C. These data indicate that the CTE is viable for heterogeneous integration in silicon-based microsystems.

B. RF Properties at 110 GHz

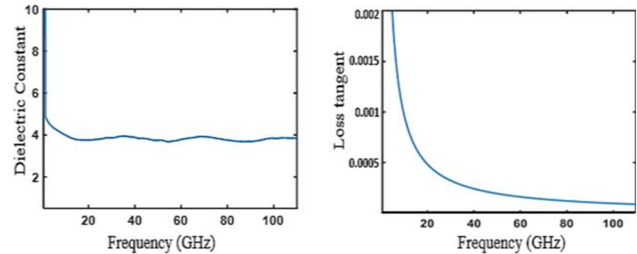


Fig 6. RF Properties of Silicate Composite for the Dielectric and Loss Tangent of the material up to 110 GHz.

The dielectric constant or relative permittivity and loss tangent of a material are significant quantities to determine the suitability of a material for packaging of highly densified RF antennas or phased arrays. Next generation RF devices are desired to operate at high frequencies. Pushing operation to 110 GHz. The PDS composite at a 60w/w% with 800nm silica particles was casted onto a silicon wafer. Co-planar waveguides were fabricated onto the silicate packaging material in order to utilize probe testing of a 110 GHz. We demonstrate those results in Fig 6. Where across the frequency range, the material holds a constant dielectric constant of 4, which is similar to a PECVD SiO_2 film. Also, the loss tangent of the material drops as the frequency increases ranging from 0.002-0.0005.

IV. Conclusions

In conclusion, we have demonstrated the PDS silica composite is stable choice in a way to make clean room compatabile mold compounds. The material is chemically, thermally, and mechanically stable, mimicking properties of a quartz silica. Furthermore, it was shown to be compatible with common microfabrication techniques, such as photolithographic patterning. The material can be processed via a number of deposition techniques ranging from spray coating, casting, molding to 3D printing dependent on the identity and concentration of filler materials. The silicate composite has been processed into thick films ranging from 10s to 100s of microns. It has demonstrated the ability to conformally fill high aspect ratio gaps (13:1), another important feature necessary for the encapsulation of high density components. Finally, the materials properties of composite were shown to be tailorable as demonstrated through the modification of the thermal expansion coefficient. The RF properties of the co-planar waveguide demonstrate similar RF properties to a PECVD $Si0_2$ film. Future work will investigate this material for wafer level packaging and integration into 3D microelectronics.

References

[1] M. Lundstrom, "Moore's Law Forever?," *Science*, vol. 299, no. 5604, pp. 210–211, Jan. 2003, doi: 10.1126/science.1079567.

[2] J. A. Burns *et al.*, "A wafer-scale 3-D circuit integration technology," *IEEE Trans. Electron Devices*, vol. 53, no. 10, pp. 2507–2516, Oct. 2006, doi: 10.1109/TED.2006.882043.

[3] D. Choudhury, "3D integration technologies for emerging microsystems," in *2010 IEEE MTT-S International Microwave Symposium*, Anaheim, CA, USA, May 2010, pp. 1–4. doi: 10.1109/MWSYM.2010.5514747.

[4] L. S. Sinev and V. T. Ryabov, "Reducing thermal mismatch stress in anodically bonded silicon–glass wafers: theoretical estimation," *J. Micro/Nanolith. MEMS MOEMS*, vol. 16, no. 1, p. 015003, Jan. 2017, doi: 10.1117/1.JMM.16.1.015003.

[5] D. Q. Tan, "The search for enhanced dielectric strength of polymer-based dielectrics: A focused review on polymer nanocomposites," *J Appl Polym Sci*, vol. 137, no. 33, p. 49379, Sep. 2020, doi: 10.1002/app.49379.

[6] J. C. McRae *et al.*, "Sodium Metasilicate-Based Inorganic Composite for Heterogeneous Integration of Microsystems," *IEEE Trans. Compon., Packag. Manufact. Technol.*, vol. 11, no. 1, Art. no. 1, Jan. 2021, doi: 10.1109/TCPMT.2020.3043367.