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Raytheon BBN Technologies Corp.
10 Moulton Street

Cambridge, MA 02138 -1119

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RPPR Final Report
as of 14-Feb-2022

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INVESTIGATOR(S):

Name: Mohammad Soltani
Email: mo.soltani@raytheon.com
Phone Number: 6178735009
Principal: Y

Organization: **Raytheon BBN Technologies Corp.**
Address: 10 Moulton Street, Cambridge, MA 021381119
Country: USA
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Submitted By: Richard Lazarus Email: rich.lazarus@raytheon.com
Phone: (617) 873-2181
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Major Goals: To address the challenges of the IARPA SuperCables program, we pursued the following goals in this project:
1- Design a scalable cryogenic PIC architecture for massive transfer of data from cryogenic electronic to room temperature over optical fiber
2- Develop a PIC material platform operating at 4K with high-speed EO modulators operating with < 5mVpp modulation voltage and low energy per bit consumption.
3- Develop a robust fiber to PIC packaging for operation at 4K.
4- Test of cryogenic EO modulator with a cryogenic superconducting stimulus module that provide electric data stream with Vpp < 5mV.

Our detailed study has shown that our CRISP approach, heterogeneous InP-on-Silicon, is the most promising for satisfying the SuperCables metrics. InP quantum well (QW) modulators show a strong modulation effect due to several mechanisms including quantum-confined stark effect (QCSE), bandfilling, and free-carrier plasma dispersion effect. The QCSE and bandfilling in particular are quite strong (at least 10x better than Si modulators). Integration of such InP modulators on Si photonics has several advantages:

1- We overcome the weak modulation effect of Si by integrating InP modulators on Si leveraging that silicon photonics is the most promising scalable PIC platform.
2- InP quantum well modulators with their QCSE effect have significant modulation enhancement at 4K as the exciton spectrum becomes sharper and where applying a small voltage can dramatically shift its spectrum compared to its width.
3- Silicon is the main substrate for SC electronics and hence, essentially both SC electronics and InP-on-Si photonics can be monolithically integrated.

Accomplishments: In the CRISP project, we have designed a scalable PIC architecture for massive data transfer from SC electronics at 4K temperature to room temperature over an optical fiber. As part of this effort, we have demonstrated a cryogenic modulator with sub-5 mV driving voltage and gigabits/sec data rate, with ultralow electric energy consumption less than 5 atto-joules/bit. We achieved this record performance by designing a compact optical ring resonator modulator in a heterogeneous InP-on-Silicon platform, where we optimized a multi-quantum well layer of InAlGaAs to achieve a strong EO effect at 4K while benefitting from high-carrier mobility and minimal free carrier freezing of III-V compounds at low temperatures. Our demonstrated modulators with their included advantage of silicon photonics scalability can pave the path for massive data transmission between superconducting processors and room-temperature electronics.

Design of InP QW epi material with their associated III-V alloys for modulation enhancement at 4K: We developed a systematic method for the design of QW epi for maximum modulation enhancement and optimal lattice matching between the stacks at 4K.

Design of InP-on-Si resonator modulators with efficient waveguide-resonator coupling at 4K and with high intrinsic Q: The Si and InP dimension were optimized for maximum modal overlap between the Si and InP section. The resonator radius and the coupling waveguide dimension were optimized for minimum radiation leakage and maximum coupling.

Demonstration of InP-on-Si QW resonator modulators with <5mVpp modulation at Gbps data rates: Our indicated that there is room for further improvement over this record achievement.

Verification and demonstration that InP minimally suffers from free-carrier freezing: The contact resistance of our modulators showed similar results for 300K and 4K for a moderate doping level.

Demonstration of InP-on-Si resonator modulators with loaded Q resonances of 100,000 and intrinsic Q of 200,000: This demonstration verified that the InP-on-Si platform can provide high Qs and so a low loss platform.

Demonstration of InP-on-Si bulk resonator modulators with 100 mV modulation at Gbps data rates: Our investigation showed that there is room for further improvement.

Developing and troubleshooting InP-on-Si fabrication to meet the cryogenic operation: Some aspects of fabrication such as a thicker oxide cladding or facet etching was not pursued at this stage. These added fab steps can improve fiber to chip coupling.

Development of a fiber-to-chip packaging for operation at cryogenic (4K) temperatures: The packaged devices were tried at different temperature cycles and then were sent to the Government site for the verification.

Microwave and optical packaging of our modulators and testing with SC stimulus module: We successfully tested the packaged auxiliary Si resonators at 40K. The stimulus module was placed at 4K stage while the packages PIC modulator at 40K. The packaging of the InP-on-Si modulators and testing with the stimulus module.

In our CRISP test setup, we demonstrated an implementation of phase modulation which, unlike intensity modulation, requires much lower energy-per-bit for the same BER level, and has the capability to meet the SuperCables program metrics. Pulse position modulation (PPM) is another promising technique, though at the cost of requiring large bandwidth, hence does not show a scalability path to higher data rates. Also, PPM receivers are more complicated and require phase noise stability especially at higher rates.

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Paolo Pintus, Anshuman Singh, Weiqiang Xie, Leonardo Ranzani, Minh A. Tran, Martin V. Gustafsson, Chao Xiang, Jonathan Peters, John E. Bowers, Mohammad Soltani. (2021). "Attojoule Scale Cryogenic High-speed Electro-Optic Modulator with sub 5 mV Operation." submitted to Nature Photonics.

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1- NSA/Laboratory for Physical Sciences (LPS)
2- Navy Information Warfare Center (NIWC) Pacific

RPPR Final Report
as of 14-Feb-2022

PARTICIPANTS:

Participant Type: Faculty
Participant: John Bowers
Person Months Worked: 1.00 **Funding Support:**
Project Contribution:
National Academy Member: N

Participant Type: Other Professional
Participant: Richard Lazarus
Person Months Worked: 1.00 **Funding Support:**
Project Contribution:
National Academy Member: N

Participant Type: PD/PI
Participant: Mohammad Soltani
Person Months Worked: 3.00 **Funding Support:**
Project Contribution:
National Academy Member: N

Participant Type: Co PD/PI
Participant: Paolo Pintus
Person Months Worked: 6.00 **Funding Support:**
Project Contribution:
National Academy Member: N

Participant Type: Staff Scientist (doctoral level)
Participant: Anshuman Singh
Person Months Worked: 4.00 **Funding Support:**
Project Contribution:
National Academy Member: N

Participant Type: Staff Scientist (doctoral level)
Participant: Martin Gustaffson
Person Months Worked: 2.00 **Funding Support:**
Project Contribution:
National Academy Member: N

Participant Type: Staff Scientist (doctoral level)
Participant: Leonardo Ranzani
Person Months Worked: 2.00 **Funding Support:**
Project Contribution:
National Academy Member: N

Participant Type: Postdoctoral (scholar, fellow or other postdoctoral position)
Participant: Weiqiang Xue
Person Months Worked: 2.00 **Funding Support:**
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National Academy Member: N

Partners

,

I certify that the information in the report is complete and accurate:
Signature: Richard Lazarus
Signature Date: 12/28/21 4:24PM

Raytheon
BBN

Title of the Project:	Cryogenic InP-on-Si Photonic Integrated Circuits (CRISP)
Contract Number:	W911NF19C0060
Contractor Name and PI:	Raytheon BBN Technologies; Dr. Mo Soltani 10 Moulton Street, Cambridge, MA 02138
Subcontractor Name and PI:	University of California, Santa Barbara; Dr. John Bowers
Report, CDRL 0003	Final Technical Report, CDRL
Project period of performance	13-May-2019 to 17-Dec-2021

Subject: Final Technical Report, CDRL 0003

Attention: Dr. William Harrod, IARPA; Dr. T.R. Govindan, ARO

In accordance with the referenced requirement of the subject contract, Raytheon BBN Technologies (BBN) hereby submits its Final Technical Report, CDRL 0003, for the Cryogenic InP-on-Si Photonic Integrated Circuits (CRISP) project. Please do not hesitate to contact Mr. Richard Lazarus at 617.873.2181 (email: rich.lazarus@raytheon.com) or Dr. Mo Soltani at 617.873.5009 (email: mo.soltani@raytheon.com) if you would like to discuss this report or have any other questions.

Sincerely,

Richard Lazarus

Richard Lazarus
Senior Program Manager
Raytheon BBN Technologies

Table of Contents

1 Introduction and Summary of Achievements

A major bottleneck in next generation computing and sensing systems is transferring their large amounts of data (tens of terabit to petabit) through interconnect channels at high-speed and with low power consumption[1,2]. This problem is exacerbated in emerging cryogenic (T~<4K) computing and sensing systems where interconnect channels are required between high-speed superconducting (SC) circuits and room-temperature electronics for subsequent access and processing[3,4]. Bulky copper cables do not provide a scalable path for such interconnects due to their limited communication bandwidth, and large heat load. As the system scales, this heat load can reduce the performance of the cryogenic circuits and potentially exceed the cooling power of the cryogenic system. To overcome these limitations, a promising solution is to use integrated electro-optic (EO) modulators in a photonic integrated circuit (PIC) platform to up convert and multiplex data from the electrical to the optical domain and transmit to room temperature via optical fibers[1,5-7]. This approach provides wide data bandwidth, extremely low loss, and negligible heat transfer all enabled by the photonic and fiber technology, which have an aggregate data capacity of petabit/s and beyond[1,2].

The key enabling PIC component to achieve this goal is an electro-optic (EO) modulator that can operate at ~4K temperature, and can respond to low-voltage, high-speed SC digital signals, which are typically below 5 mV[3,4,8–11], and with low energy consumption. The energy consumption is ruled by the aggregate data rate to be transferred and the heat load that it will generate at 4K. For example, for a petabit aggregate data rate transfer, an energy per bit consumption of < 1 femto Joule/bit is acceptable for an EO modulator at 4K.

Despite a variety of demonstrated cryogenic PIC platforms and their associated EO modulators[7, 12-16], not all can operate efficiently at low temperatures nor can they provide a functional EO modulator sensitive to such small SC voltage levels and low energy consumption. The driving voltages of the existing modulators are significantly large (several hundred mV to few V) compared to the small voltage levels required for superconducting circuits, typically below 5 mV[3,4,8-11]. Common EO materials such as polymers and Lithium Niobate are prone to photorefractive instability at low temperatures, making them unreliable for interfacing with SC circuitry[17,18]. Long-established silicon EO modulators based on free-carrier plasma dispersion become inefficient below a few tens of Kelvin due to free-carrier freezing[7,19]. Although this effect can be compensated to some degree by increasing the doping concentration in the silicon, it does not improve the voltage sensitivity of the modulator[7,16] nor does it address increased insertion loss due to excess free carriers. Plasmonic slotted waveguide modulators infiltrated with EO polymer[20,21] have been demonstrated at room temperature with high-speed and small electric energy consumption at sub-100 aJ/bit [20,21], but they operate at several hundred millivolt modulation and suffer from large optical material loss and coupling loss. Additionally, the material stability of EO polymers at 4K temperature is not quite known and susceptible to degradation over time. More recently, 2D material-based modulators have been investigated at 4K, but the modulation voltage is still more than two orders of magnitude higher than what is required to interface with SC circuitry[14].

In the CRISP project, we have designed a scalable PIC architecture for massive data transfer from SC electronics at 4K temperature to room temperature over an optical fiber. As part of this effort, we have demonstrated a cryogenic modulator with sub-5 mV driving voltage and gigabits/sec data rate, with ultralow electric energy consumption less than 5 atto-joules/bit. We achieved this record performance by designing a compact optical ring resonator modulator in a heterogeneous InP-on-Silicon platform, where we optimized a multi-quantum well layer of InAIGaAs to achieve a strong EO effect at 4K while benefitting from high-carrier mobility and minimal free carrier freezing of III-V compounds at low temperatures. Our demonstrated modulators with their included advantage of silicon photonics scalability can pave the path for massive data transmission between superconducting processors and room-temperature electronics.

1.1 Our Goals in the CRISP Project and a Summary of our Achievements

To address the challenges of the IARPA SuperCables program, we pursued the following goals in this project:

1- Design a scalable cryogenic PIC architecture for massive transfer of data from cryogenic electronic to room temperature over optical fiber
2- Develop a PIC material platform operating at 4K with high-speed EO modulators operating with < 5mVpp modulation voltage and low energy per bit consumption.
3- Develop a robust fiber to PIC packaging for operation at 4K.
4- Test of cryogenic EO modulator with a cryogenic superconducting stimulus module that provide electric data stream with Vpp < 5mV.

We have developed a Cryogenic InP-on-Si Photonic (CRISP) platform and in it we have designed and demonstrated ring resonator modulator which achieves sub-5 mV modulation with gigabits-per-second (Gbits/s) data rate, and electrical energy consumption below 5 attojoule-per-bit (aJ/bit)

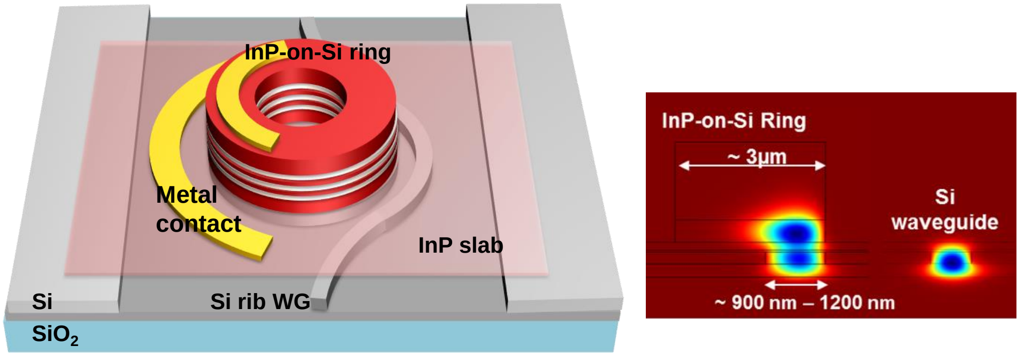


Fig. 1: **CRISP modulator overview**: (Left): A schematic of our InP-on-Si resonator modulator with stacks of III-V quantum wells (QW) to enhance the EO modulation. The epi QW material stack is optimized for 4K operation. (Right) Cross section of the simulated resonance optical mode of the InP-on-Si resonator with a radius of ~ 40 micron and a waveguide that is laterally coupled to it as shown in the left panel.

at 4K temperature. The CRISP modulator (see Fig. 1) is fabricated in a heterogeneous platform which combines the strong EO properties of InP ─ with its associated III-V alloys ─ with the scalable and compact silicon photonic circuitry[22–25]. Unlike silicon modulators, the CRISP modulator suffers minimally from free-carrier freezing at low temperatures allowing it to operate efficiently with moderate doping levels in the InP layer. We design the modulators for operation at a wavelength within ~ 1500-1600 nm. Table 1 shows the major challenges of the SuperCables Program, and our CRISP platform innovations to meet these challenges.

Table 1: Major SuperCables challenges with associated CRISP platform innovations.

Challenges to achieving SuperCables metrics	CRISP solutions and innovations
Developing a cryogenic (4K) EO modulator sensitive to small (<5 mV) voltages.	Use InP-on-Si modulators with quantum confined Stark effect (QCSE) effect, as well as Franz-Keldysh effect providing ultra-sensitive modulation at 4K.
Achieving low BER with high speed (>10 Gbps) and low energy per bit (<5 aJ/bit) for exascale and <5000 aJ/bit for petascale	Using compact InP-on-Si resonator phase modulators with small capacitance, and using binary phase shift keying (**BPSK**) and differential PSK (**DPSK**) modulation schemes.
Scalability of a PIC platform with many modulators to petascale and potentially exascale	Compact EO modulators can be multiplexed on the same channel increasing bandwidth per channel. Si PIC platform has efficient coupling of fiber to chip and is compatible with superconducting circuit fabrication.

Our detailed study has shown that our CRISP approach, heterogeneous *InP-on-Silicon*, is the most promising for satisfying the SuperCables metrics. InP quantum well (QW) modulators show a strong modulation effect due to several mechanisms including quantum-confined stark effect (QCSE), bandfilling, and free-carrier plasma dispersion effect. The QCSE and bandfilling in particular are quite strong (at least 10x better than Si modulators). Integration of such InP modulators on Si photonics has several advantages:

- We overcome the weak modulation effect of Si by integrating InP modulators on Si leveraging that silicon photonics is the most promising scalable PIC platform.
- InP quantum well modulators with their QCSE effect have significant modulation enhancement at 4K as the exciton spectrum becomes sharper and where applying a small voltage can dramatically shift its spectrum compared to its width.
- Silicon is the main substrate for SC electronics and hence, essentially both SC electronics and InP-on-Si photonics can be monolithically integrated.

In addition to InP-on-Si QW modulators, we also investigated InP-on-Si bulk modulators. Table 2 shows the modulator devices we employed to achieve the program goals. Since the design and the fabrication period of our ultimate modulator structure (e.g., QW InP-on-Si resonator modulator) was lengthy, we employed auxiliary modulators (Si modulator) to help accelerate the cryogenic packaging as well as testing the SC stimulus module.

Table 2: EO modulators used and demonstrated in the CRISP project

EO Modulators we developed or used in this project	Comments
InP-on-Si QW resonator modulators with QW epi optimized for 4K operation	We designed these during the SuperCables Program. These modulators provide the maximum modulation sensitivity and depth to an applied small voltage. The stack of QW epi layers are optimized for 4K enhanced modulation. This optimized QW stack may not necessarily work at other temperature e.g. room temperature. The dominant modulation mechanism is bandfilling and QCSE. We were able to experimentally achieve modulation voltage as small as 5 mVpp at Gbps data rates at 4K with on chip laser power within 50-100 µW.
InP-on-Si Bulk resonator modulators	We designed these during the SuperCables Program. These modulators provide moderate modulation sensitivity yet stronger than silicon modulators. Can operate over a wide temperature (4K-300K). The modulation mechanism is Franz-Keldysh and Free-carrier dispersion. We were able to achieve modulation voltages as small as 100 mVpp at Gbps data rates at 4K.
Silicon ring resonator modulators	We designed these modulators on our internal research effort and fabricated them in AIM foundry. These modulators allowed us accelerate fiber-to-chip packaging and test of the SC stimulus module at the intermediate stages. These modulators operate based on free-carrier plasma dispersion. We were able to experimentally achieve 400mVpp modulation at Gbps data rates but at much higher temperature (40K).

Table 3 shows a summary of our achievements during the execution of the CRISP project. These achievements cover the broad aspects of our CRISP platform including the resonator modulator design, QW material design for operation at 4K, fabrication, record performance demonstration at 4K, and fiber-to-chip packaging for stimulus module integration at 4K.

Table 3: A summary of our achievements

Achievements	Comments
Design of InP QW epi material with their associated III-V alloys for modulation enhancement at 4K	We developed a systematic method for the design of QW epi for maximum modulation enhancement and optimal lattice matching between the stacks at 4K.
Design of InP-on-Si resonator modulators with efficient waveguide-resonator coupling at 4K and with high intrinsic Q	The Si and InP dimension were optimized for maximum modal overlap between the Si and InP section. The resonator radius and the coupling waveguide dimension were optimized for minimum radiation leakage and maximum coupling.
Demonstration of InP-on-Si QW resonator modulators with <5mVpp modulation at Gbps data rates	Our investigation showed that there is room for further improvement.
Verification and demonstration that InP minimally suffers from free-carrier freezing.	The contact resistance of our modulators showed similar results for 300K and 4K for a moderate doping level.
Demonstration of InP-on-Si resonator modulators with loaded Q resonances of 100,000 and intrinsic Q of 200,000	This demonstration verified that the InP-on-Si platform can provide high Qs and so a low loss platform.

Demonstration of InP-on-Si bulk resonator modulators with 100 mV modulation at Gbps data rates.	Our investigation showed that there is room for further improvement.
Developing and troubleshooting InP-on-Si fabrication to meet the cryogenic operation	Some aspects of fabrication such as a thicker oxide cladding or facet etching was not pursued at this stage. These added fab steps can improve fiber to chip coupling.
Development of a fiber-to-chip packaging for operation at cryogenic (4K) temperatures.	The packaged devices were tried at different temperature cycles and then were sent to the Government site for the verification.
Microwave and optical packaging of our modulators and testing with SC stimulus module	We successfully tested the packaged auxiliary Si resonators at 40K. The stimulus module was placed at 4K stage while the packages PIC modulator at 40K. The packaging of the InP-on-Si modulators and testing with the stimulus module.

1.2 CRISP Datalink System Architecture

Our CRISP system architecture demonstrated an implementation of phase modulation which, unlike intensity modulation, requires much lower energy-per-bit for the same BER level, and has the capability to meet the SuperCables program metrics. Pulse position modulation (PPM) is another promising technique, though at the cost of requiring large bandwidth, hence does not show a scalability path to higher data rates. Also, PPM receivers are more complicated and require phase noise stability especially at higher rates.

We pursued two phase modulation schemes that use the same modulator design and PIC platform:

1. Coherent binary phase shift keying (BPSK) employs a laser LO arm for coherent homodyne detection. This scheme lowers the energy consumption at 4K by moving it to the LO arm at 300K, at the expense of increased receiver complexity (see Fig. 2a). This scheme can meet the threshold and the objective milestones and show a path toward stretch goals (for the latter more complex phase modulations such as QPSK might be needed which is not the scope of this proposal).
2. Differential binary phase shift keying (DPSK) is the simplest coherent detection scheme where the receiver uses interference between adjacent symbols without the need of an external reference laser local oscillator (LO) arm. While this scheme uses the same PIC modulator chip of Fig. 1a, it allows lower architecture complexity in the receiver (see Fig. 2b) to meet the intermediate milestones.

Figure 2a shows a simplified schematic of our proposed scalable BPSK. An array of laser sources with different wavelengths are multiplexed in a WDM device at room temperature and then sent over an optical fiber and split in two paths. The 1st path containing a very small percentage of the power (~<1%) is sent into the cryocooler and coupled to a Si waveguide on the PIC chip at 4K. The 2nd path contains the remaining higher power stays at room temperature and is sent to the room temperature receiver.

On the 4K PIC chip is an array of InP-on-Si resonator modulators with different resonance wavelengths corresponding to the wavelengths of the laser array. Each resonator responds to the corresponding laser wavelength and phase modulates the laser light in response to the signal

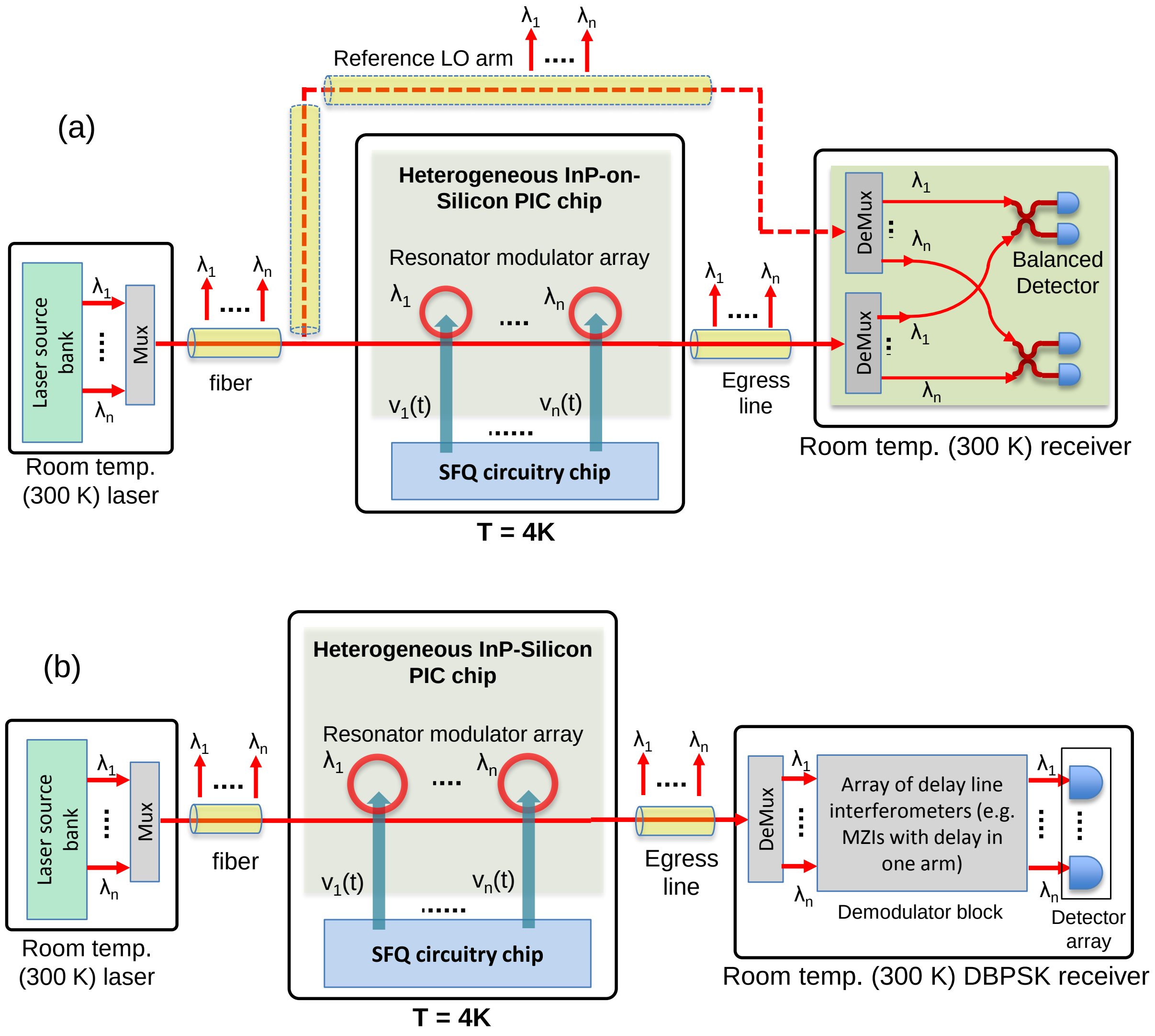


Fig. 2: Our scalable CRISP architecture based on coherent communication schemes. (a) A coherent BPSK scheme: InP-on-Si resonator phase modulator arrays with different operation wavelengths, corresponding to each wavelength data channel, and coupled to a Si bus waveguide. A RT multiplexed laser source is launched to the PIC chip inside the cryocooler via an optical fiber, and each laser wavelength addresses its corresponding resonator modulator. There is a reference LO path arm to carry the majority of laser power at RT in addition to further improving the BER. The receiver is a balanced receiver. In this project we only demonstrate one or few modulators per channel. (b) A DPSK scheme: the modulator PIC chip is the same as the one shown in Fig. 2(a). The RT receiver includes a demux to separate wavelength channels and send them to demodulator circuit (that includes Mach-Zehnder interferometer (MZI) with delay in one arm), and detector.

coming from the SFQ chip. Except for the modulator region in InP, all the photonic routing as well as coupling of light in and out of the chip is designed on a silicon photonic circuit. Note that the SFQ circuitry can in principle be made on the same PIC chip as both have silicon as their substrate platform. After data modulation, the information is sent out of the PIC chip over an optical fiber to room temperature. At the receiver the reference and signal paths which contain many wavelength channels are first demultiplexed, and then the reference and the signal for each wavelength channel are combined and detected in balanced receivers.

Figure 2b shows our scalable DPSK architecture. Note that the 4K PIC chip is exactly the same as the one shown in Fig. 2a, and there is no LO laser arm. At the receiver, a demultiplexer separates different wavelength channels and sends them to a demodulator circuit and then to the detector array. The DPSK demodulator circuit comprises a delay line interferometer and a detector to recover the phase difference between a current symbol and the previous symbol.

Since we use phase modulation in both of the above architectures, the resonator modulators are designed to operate in the electro-refraction regime. For such phase modulators, the resonator is overcoupled to the waveguide with minimal amplitude distortion (i.e., only phase change). As discussed in the next section, a BPSK modulator keeps most of laser power in the reference arm and reduces the energy per bit consumption and heat load in the cryocooler. In addition, BPSK improves the BER while responding to a small modulation voltage. While the BPSK scheme (Fig. 2a) allows low energy consumption (5 aJ/b) with small voltages ~5 mV (see next section), the DPSK allows us testing modulator chips at early stages with lower experiment complexity but at higher voltages (10-100 mV).

In the next section, we perform a link budget analysis and discuss the system parameters of the cryogenic PIC chip including the modulator as well as the receiver in the above architectures with respect to SuperCables metrics. While the architecture in Fig. 2a and 2b scales to large number of channels with aggregate higher data rates, we will demonstrate only one or few resonator channels.

1.3 CRISP Link Budget Analysis for SuperCables Milestones

Figure 3a shows a simplified system diagram of the CRISP architecture. The laser light is launched into the 4K fridge via an optical fiber and coupled to a PIC modulator chip. The light modulated

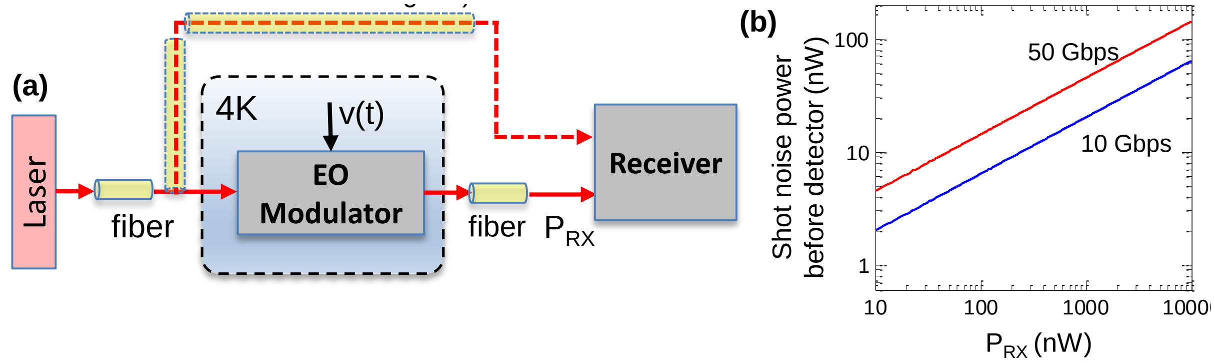


Fig. 3: (a) A simplified and generic system diagram of CRISP for either architectures in Fig. 1a or Fig. 1b with only one modulator. For the case of coherent BPSK (i.e. Fig.1a) the LO arm is needed, and the receiver consists of a directional coupler and two balanced detectors. For the DPSK case (i.e. Fig. 1b), the LO arm is not needed, and the receiver includes an MZI with a symbol delay in one arm followed by a single detector. (b) Plot of the inherent shot noise of laser light for different data rates. The received power at the detector needs to be above this noise level.

by SC circuitry voltage is coupled out of the PIC chip into an optical fiber and sent out to the receiver at RT. Starting from the diagram shown in Fig. 3a, and knowing that the signal light with power P_{RX} at the receiver needs to be above the photon shot noise, we calculate the specifications of the modulator such as maximum capacitance and modulator V_π (the applied voltage to induce a π phase shift for light).

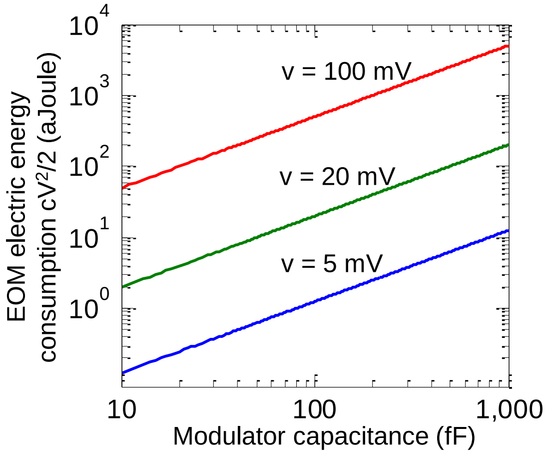


Fig. 4: The electric energy consumption of a lumped EO modulator for different modulator capacitance and for three different modulated

The maximum allowable modulator capacitance: For a lumped modulator, the RF energy consumption per bit is $CV^2/2$, where C is the modulator capacitance and V is the voltage applied to the modulator. Figure 4 shows a plot of this energy consumption versus the modulator capacitance for three different voltages of 5 mV, 20 mV, and 100 mV. The energy per bit constraint puts a limit on the maximum allowed value for the modulator capacitance which is linearly related to the modulator length. From Fig. 4 we see that for 5 mV modulation voltage (our goal) and a modulator capacitance of less than 80 fF, the RF energy consumption is < 1 aJ/bit. Since our resonator modulator has small capacitance (~<50-100 fF), its RF energy consumption is quite small, and therefore, the majority of energy dissipation is in the optical domain (i.e. modulator optical insertion loss, coupling loss to chip, etc.). The results in Fig. 3 also indicate that to meet the energy consumption metric, a modulator with a small V_π is needed to reduce the RF energy dissipation. While increasing the modulator length lowers V_π, it also increases its capacitance resulting in higher energy dissipation as well as lower modulator bandwidth. In this proposal we aim to lower our current V_π from 0.2V.cm to ~0.02-0.1 V.cm.

Modulator $V\pi$: A phase modulator with a smaller V_π, for a given modulator length, provides a larger extinction at the receiver for a given applied RF voltage V_{RF}, thereby improving the BER. Though a larger modulator length provides a smaller V_π, this comes with a tradeoff in bandwidth and insertion loss. Hence, minimizing modulator V_π for a given length is important as the sensitivity of the modulator is defined by V_{RF}/V_π. Here, we determine the minimum V_π to achieve desired BER values, for 5 mV RF signal and given 4K energy per bit consumption.

To find the required V_π, we start from the energy constraint budget and use standard formulas to determine the required energy per bit at the receiver. The energy per bit dissipated at 4K sets an upper limit to the optical power at the receiver and it includes the insertion loss of the modulator (including fiber-to-chip coupling) and the RF energy dissipated ($1/2CV^2$). We determine the minimum required SNR at the receiver for a given BER and modulation scheme and from the extracted SNR we can find the minimum modulator V_π for a modulation RF voltage of 5 mV. We assume the receiver noise floor is limited by photon shot noise and the detector dark current.

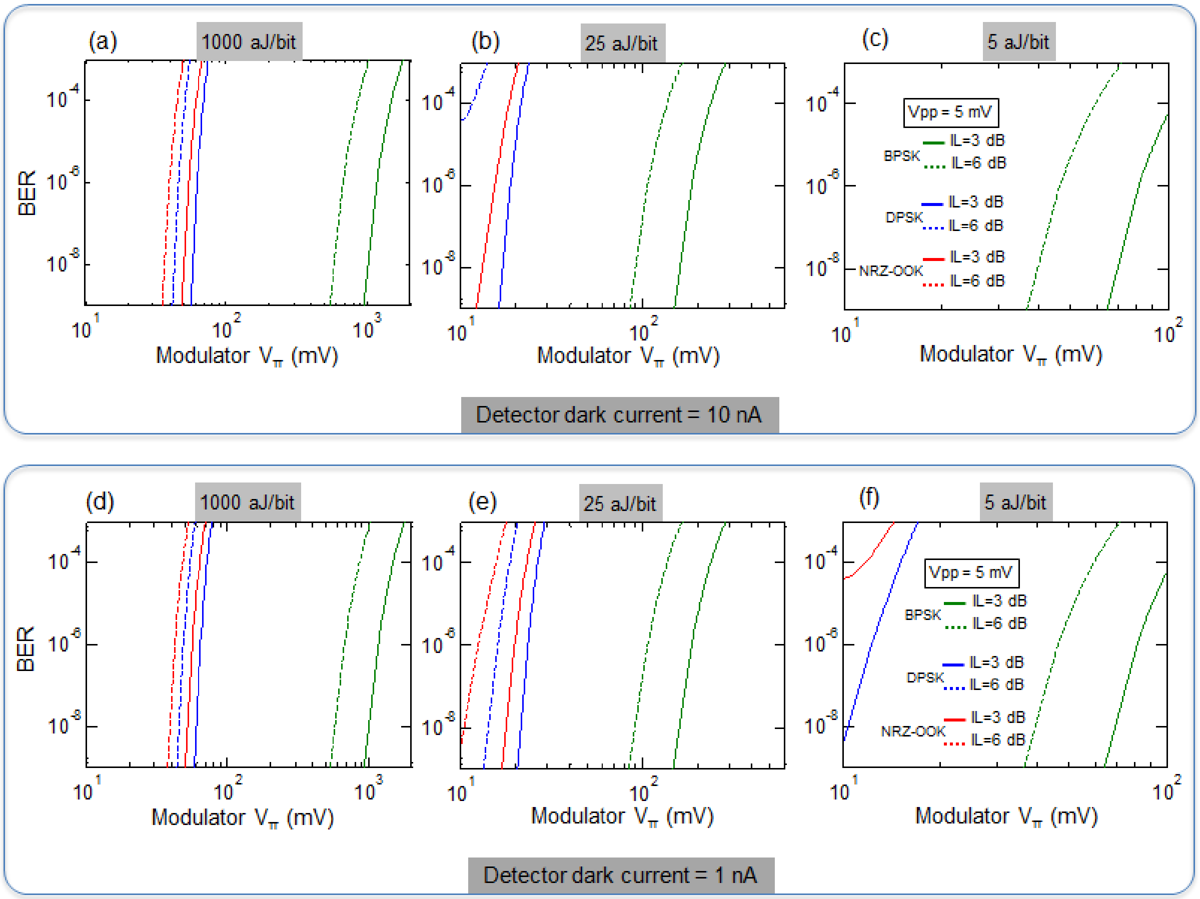


Fig. 5: Calculated BER vs. the modulator required $V\pi$ for energy per bit consumptions of 1000 aJ/bit, 25 aJ/bit, and 5 aJ/bit, respectively as specified in the figures, for detector dark currents of 10 nA (a-c), and 1 nA (e-f), respectively, and for three modulations schemes of NRZ-OOK, DPSK, and BPSK and two optical insertion losses (IL) of 3dB and 6dB as specified in the figure. The IL includes the fiber-to-chip coupling loss (both input and output) and the modulator insertion loss. For this analysis both the photon shot noise and the photodetector dark current noise have been considered. For the photodetector, we have assumed a detector responsivity of 0.8 A/W. We have also assumed a 5 mVpp voltage at 20 Gbps for the modulation signal. For the BPSK analysis, we have neglected laser RIN noise and the balanced detector common mode rejection ratio (CMRR).

Figure 5 shows the simulation of BER vs. the required modulator V_π for an applied 5 mV RF voltage, and for three modulation schemes of BPSK, DPSK, and NRZ-OOK. The simulations are for two detector dark currents of 10 nA and 1 nA, with nominal PIC chip insertion losses of 3 dB and 6dB. From Fig. 5 we can conclude:

- BPSK and DPSK have substantial advantage over NRZ-OOK in term of providing much lower BER for the same modulator $V\pi$. BPSK is in fact essential to reach and surpass the objective energy consumption metric (5 aJ/bit) as well as relaxing the required modulator $V\pi$ for the applied 5 mV RF voltage.
- Comparing Figs. 4c and 4e, we see that BPSK can meet the objective 5 aJ/b, but DPSK can meet initial program milestones. The reason for superior performance of BPSK is the

presence of LO arm that sets the noise floor at the signal photon shot noise.

- Also from Fig. 5 we see that, in order to meet the SuperCables metrics, the modulator Vπ needs to be ~< 100 mV.

How our CRISP modulator can meet small V_π (<0.1 V): As shown in Table 4, an InP-on-Si modulator has a typical room temperature V_π~0.2 V.cm (i.e. with 0.2 V voltage and an optical traveling length 1 cm, a phase of π is acquired). Since we use a resonator modulator, and light does many roundtrips in it a large optical length can be achieved. Table 3 shows the total traveling length of light in a resonator phase modulator for different modulator bandwidths. For a 10 GHz BW modulator, the optical traveling length is 0.75 cm meaning that such resonator provides an equivalent Vπ~0.2-0.3 V, sufficient to meet the threshold (25 aJ/bit)., traveling length is 0.75 cm meaning that such resonator provides an equivalent Vπ~0.2-0.3 V, sufficient to meet the threshold (25 aJ/bit).

Table 4: Calculation of the total traveling optical length (L_{TOL}) in a ring resonator phase modulator, for different resonator bandwidths (BW). We use the expression $L_{TOL}=c/(n_g.BW)$.

Resonator Modulator BW	10 GHz	20 GHz	50 GHz	Comment
Total optical traveling length for n_g = 4 (InP-on-Si)	0.75 cm	0.375 cm	0.15 cm	For such traveling lengths, an EOM with V_π in the range of 0.02-0.1 V.cm is needed depending on the modulation BW.

2 Details of the CRISP QW Resonator Modulator Structure and the Experimental Results

A schematic of the CRISP modulator is shown in Fig. 6a where the stack of III-V compounds sits on a silicon ring which is evanescently coupled to a silicon rib waveguide. Two strong modulation mechanisms are present in the III-V alloys used in the modulator: band-filling[26] (Burstein-Moss) and quantum confined Stark effects[27] (QCSE), with some contribution from plasma dispersion[26]. We design a multi quantum well (QW) layer to spatially confine electrons and holes, enhancing those EO effects and leading to large modulation. To further increase the modulation sensitivity to millivolt-scale voltages, we take advantage of a ring resonator configuration with its sharp resonance spectrum. This enables intensity modulation of the light with sub-5 mV modulation.

A key aspect of our CRISP modulator is the design of the multi QW layer to achieve high-sensitivity modulation at 4K. The QW layer doping is optimized to achieve large band-filling and plasma effects with negligible optical absorption, while the III-V alloy composition and the geometry of the QWs are engineered to maximize the QCSE. Specifically, the QCSE is the interaction of light with exciton quasiparticles (electron-hole bound state) and it becomes significantly stronger at lower temperatures due to the sharper exciton spectrum[28].

A simplified InP-on-Si cross-section of the modulator is shown in Fig. 6b, where the EO layer consists of a fifteen alternate stacks of QWs and quantum barriers (QB). Each well has a thickness of 8 nm sandwiched between 5 nm thick barriers. This multi-QW/QB layer is also sandwiched between two 125 nm thick separate confinement heterostructures (SCH) that confine electrons and holes in the EO layer. Such a design allows for a large overlap between electron and hole wave functions (Inset in Fig. 6c), so the QCSE effect is maximized. The layers of QW, QB and SCH are made of In_xAl_{1-x-y} Ga_yAs, which provides a larger bandgap offset — useful for energy band engineering[29] — and higher fabrication yield than $In_{1-x}Ga_xAs_{1-y}P_y$.

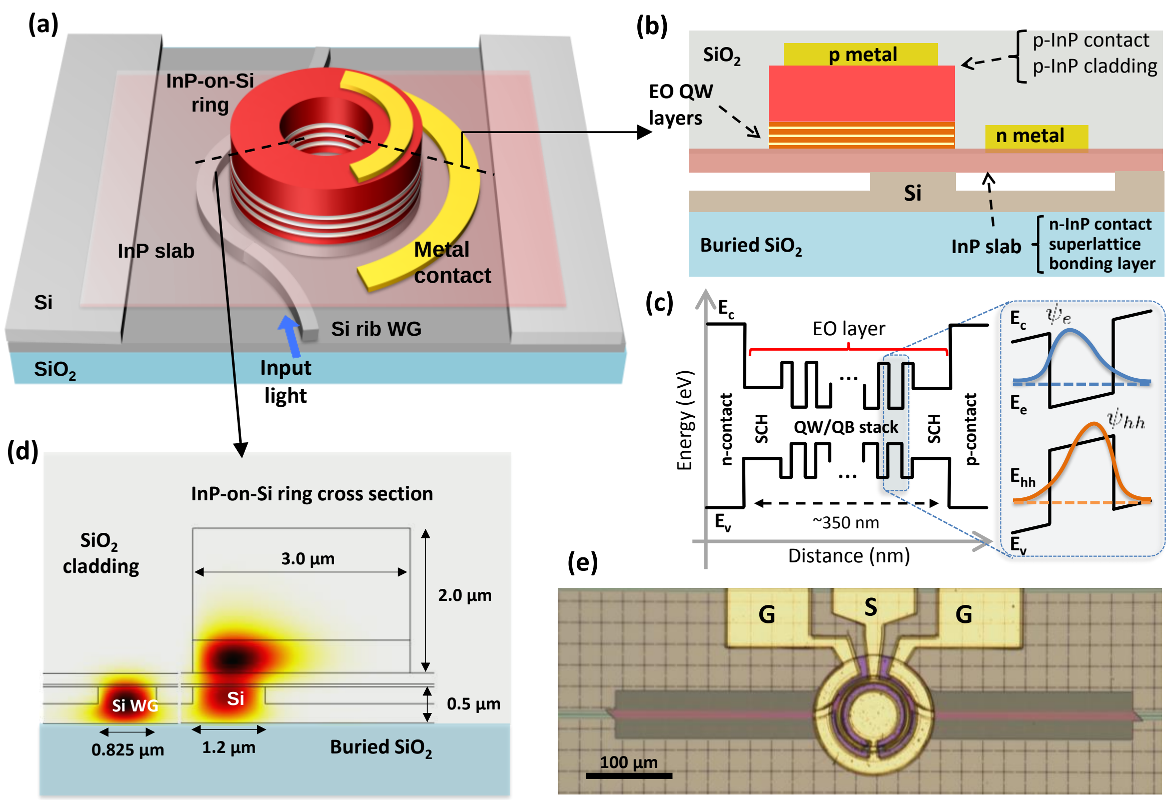


Fig. 6: **Heterogeneously integrated InP-on-Si resonator modulator for operation at 4K**. (a) InP ring resonator with stack of QW on a silicon resonator coupled to a silicon waveguide. (b) A generic cross section of the stack of materials for the InP-on-Si modulator with metal contacts. (c) Energy band and size of the EO layer which contains stacks of QWs and QBs in alternative manner and buried between two SCHs. Inset shows the wave functions of electrons and holes in conduction and valence bands, respectively. Doping of the layers is optimized to achieve large band-filling and plasma effects, while QW geometry is engineered to maximize electron-hole interaction (exciton) to perform large QCSE. (d) Cross section of optical mode profiles for the InP-on-Si resonator with a nominal external radius of 42 µm, and for the silicon waveguide, showing the mode overlap between the waveguide and resonator modulator. (e) An optical microscope image of the fabricated ring modulator, showing metallic pads in ground-signal-ground (GSG) configuration for electric signals and silicon waveguide in pulley coupling arrangement with the ring resonator. QW: Quantum well, QB: Quantum barrier, SCH: Separate confinement structure, EO: Electro-optic, E_c: Conduction band energy level, E_v: Valence band energy level.

The quaternary composition of QW, QB and SCH is chosen to maximize the EO effect in our modulators for 4K operation according to the following considerations: (i) the lattice constants match the one of InP to avoid undesirable strain when the device is cooled down to 4K, (ii) the exciton energy (i.e., photoluminescence) in QWs is ~100 meV larger than the energy of the operating wavelength (λ~1500 - 1600 nm), i.e., ~800 meV to prevent the optical absorption[30], (iii) the energy gap and bandgap offset of QW and QB are designed to better confine electrons and holes in the QW to maximize QCSE as well as band-filling and the free carrier dispersion effect[31,32]. By considering all these aspects, the alloy composition $In_xAl_{1-x-y}Ga_yAs$ used for QW, QB and SCH are ($x = 0.5296$, $y = 0.4512$), ($x = 0.5296$, $y = 0.3130$) and ($x = 0.5296$, $y = 0.3365$), respectively (see Supplementary Section S1 for more details). In addition, the three regions are lightly n-doped with a concentration of $\sim 1 \cdot 10^{17}/cm^3$ in order to obtain a large change in the refractive index of $In_{1-x-y}Al_xGa_yAs$ caused by plasma and band-filling effects[33].

We optimize the dimensions of the silicon and the InP layer for maximum optical modal overlap (Fig. 6d). For this purpose, we choose a silicon layer with a thickness of 500 nm, and etch it down to 260 nm to produce a rib type waveguide for maximum optical index matching to the InP layer. For device fabrication, we designed a ring with an external radius of 42 μm and a Si ring width of 1.0 μm and 1.2 μm. A microscope image of the final device is shown in Fig. 6e, where the top view of the gold electrodes and the rib waveguide bus are clearly identifiable.

We characterize the electro-optic performance of the CRISP modulator at 4K in a cryogenic probe station. Figure 7a shows the optical spectrum of the modulator, around 1600 nm, when the voltage

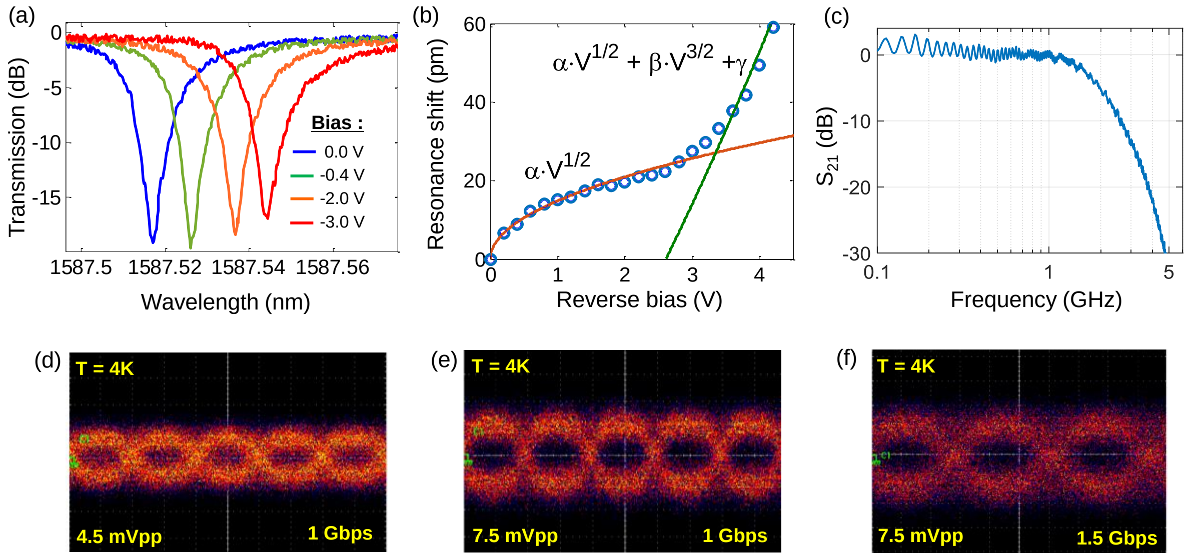


Fig. 7: **CRISP modulator optimized for sub-5 mV and attojoule/bit scale operation at 4K**. (a) The spectrum of the modulator at different reverse biases, with a full-width at half maximum (FWHM) for the resonance linewidth of ~16 pm. (b) The wavelength shift of the modulator resonance is plotted with respect to the reverse bias voltage. The fit (lines) of measured data (circle) highlights the contributing modulation mechanisms. The shift is proportional to $V^{1/2}$ for the band-filling and the plasma effects, while it varies with $V^{3/2}$ for the QCSE. The constants $\alpha=14.79\ pm/\sqrt{V}$, $\beta=12.45\ pm/\sqrt{V^3}$, and $\gamma = -76.36$ pm are the fitting parameters. (c) The electro-optical frequency response (S_{21} coefficient) of the modulator, shows a 3 dB bandwidth of ~1.5 GHz. (d)-(f) Demonstration of millivolt scale and high data rate modulation by sending PRBS 2^7-1 data stream to the modulator. The insets in (d)-(f) show the applied peak-to-peak modulation voltage and the data rate. The modulator bias voltage for these experiments is -0.3 V, with a resonance shift sensitivity of $d\lambda/dV \sim 14$ pm/V.

sweeps between 0 V and -3.0 V. The resonator modulator has a loaded quality factor of ~100,000 corresponding to a resonance linewidth of 16 pm (~1.8 GHz). With this small resonance linewidth, a minimal applied voltage is sufficient to lead the ring out-of-resonance. This large sensitivity to an electrical signal is shown in Fig. 7b, where the resonance shift is plotted with respect to the applied reverse bias voltages. When the magnitude of the reverse bias is small, the spectrum shifts mainly because of the band-filling and the carrier depletion effects ($\Delta\lambda \propto V^{1/2}$). However, for much lower bias voltages, the QCSE becomes the dominant contribution ($\Delta\lambda \propto V^{3/2}$), explaining the non-uniform shift of the spectrum as a function of the applied voltage[33]. From Fig. 7b we choose the optimal voltage bias point to provide large modulation sensitivity with optimum optical performance. Though the resonance shift is much stronger in the QCSE regime, we biased the modulator such that the band-filling and plasma effects are dominant since we observed negligible absorption and no resonance linewidth broadening in this region. An optimal future design can potentially bring the QCSE to a region of lower absorption while providing large resonance shift.

Our experiments show gigabit per second modulation rate with sub-5 mV modulation signal and 2 attojoule per bit energy consumption. The EO frequency response is shown in Fig. 7c and indicates a modulation bandwidth of around 1.5 GHz. This value is limited by optical resonance bandwidth of ~1.8 GHz due to the large quality factor of the ring resonator (Q ~100,000). For the modulator data rate measurement, we send to the device electrodes a pseudo-random non-return-

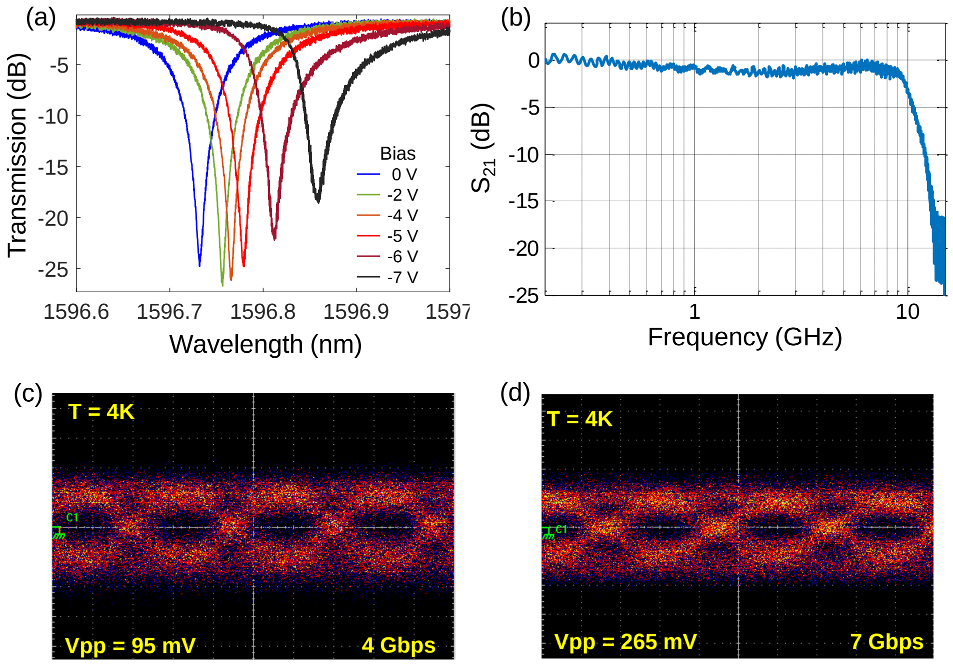


Fig. 8: CRISP modulators at higher speed data rates and modulation bandwidth at 4K (a) Spectrum of a resonator modulator with large resonance linewidth (~100 pm) and its shift at different bias voltages shown in the inset. (b) The measured modulator frequency response shows a 3 dB bandwidth of ~9 GHz. (c)-(d) The eye diagrams at 4K for data rates (modulation voltages) of 4 Gbps (V_{pp} = 95 mV) and 7 Gbps (V_{pp} = 265 mV). respectively. The modulator is biased at -6 V, operating dominantly in the QCSE regime, with a resonance shift sensitivity of $d\lambda/dV \sim 50$ pm/V.

to-zero (NRZ) bit sequence of length of 2^7-1, and peak-to-peak voltage amplitude (V_{pp}) at the millivolts scale. Fig. 7d-7g show the measured eye diagrams for data rates within 1-1.5 Gbps, and different V_{pp} values as small as 4.5 mV. The total electric energy per bit consumption of the modulator is equal to $\frac{CV_{pp}^2}{4} + |V_{bias}I_{bias}|/r_b$, where C is the modulator capacitance, V_{bias} and I_{bias} are the bias voltage and the leakage current of the modulator, and r_b is the data rate. We measure a capacitance of C ~ 406 fF at different bias voltages, which results in $\frac{CV_{pp}^2}{4} \sim 2.1\ aJ/bit$, when Vpp = 4.5 mV. We also perform the I-V curve characterization to find the leakage current of the modulator. For different modulator devices we observe a static leakage current within 0.1 nA-7 nA, resulting in an energy consumption within 0.03-2.1 aJ/bit for a bias of - 0.3 V and a data rate of 1 Gbps. Therefore, we estimate a total electric energy per bit E_b = 2.13-4.2 aJ/bit. We believe that sub-aJ/bit electric energy consumption can be reached by reducing the electrode size and introducing an intrinsic region between the p and n doped area that lowers the diode capacitance as well as the energy per bit[34].

To verify that our modulators minimally suffer from free carrier freezing and are able to operate at higher modulation data rates, we repeat the experiments with a lower Q resonator that exhibits a larger resonance linewidth, and thereby a wider modulation bandwidth. For this experiment, we select a ring resonator with Q ~16,000 corresponding to a resonance linewidth of ~100 pm (Fig. 8a). Such a wider resonance linewidth requires a larger modulating voltage. Fig. 3b shows the EO frequency response with a 3 dB bandwidth of ~9 GHz, which is much wider than the results shown in Fig. 2c. Figures 3c-3d show the measured eye diagrams at different data rates and driving voltages. For this device, the electric energy-per-bit is ~$CV_{pp}^2/4$ = 935 aJ/bit for a voltage V_{pp} of 95 mV (Fig. 8c).

2.1 Summary of CRISP QW Modulators

Table 5 summarizes the major results for the CRISP QW modulator devices in Fig. 2 and Fig. 3 that have resonance linewidths of 16 pm (Q~100,000) and 100 pm (Q~16000), respectively. While a narrower resonance linewidth enables modulation at smaller voltage and lower energy electric consumption, it limits the modulator bandwidth and data rate. Therefore, for a high data rate design, a wider resonance linewidth is required. In a future design and with a more optimal III-V material stack to enhance the band-filling and the QCSE effect, one can expect to achieve much stronger resonance shifts with small voltages (e.g., <5 mV) while using a wide-resonance linewidth (e.g., > 100 pm) modulator.

For these experiments, we fabricated resonator modulators with a radius of ~ 40 µm, though our simulation showed that resonators with radii within 25-30 µm can provide mode confinement with negligible radiation leakage. Making a more compact resonator can further reduce the energy consumption. Though in this work we demonstrate a single resonator modulator, our platform allows making a large array of such compact modulators and their data multiplexing for the promise terabit to petabit data transmission.

For any EO modulator, the total energy consumption which is the sum of electric energy and optical energy should be taken into account. For our CRISP modulator experiments, we used on-chip laser power within 50-100 µW due to limitations from the fiber-to-chip coupling loss (~12 dB/facet), as they were far from their optimal design point (2.5 dB/facet). With a proper fiber-to-chip coupling and modulation format, we expect to bring the on-chip laser power to be within 1-10 µW. With such laser power and a nominal data rate of 10 Gbps, we expect the optical energy consumption to be at 100-1000 aJ/bit.

Table 5: A summary of CRISP QW resonator modulator at 4K for two different resonance linewidths

Device	Resonance linewidth	Resonance shift sensitivity (dλ/dV)	Modulator BW	Bit rate / Vpp	Electric energy consumption (aJ/bit)*
#1 (Fig. 2)	16 pm (~2 GHz)	~14 pm/V @ -0.3 V bias (dominantly band-filling region)	1.5 GHz	1 Gbps / 4.5 mV	~2.1
				1.5Gbps / 7.5 mV	~5.7
#2 (Fig. 3)	100 pm (~12.5 GHz)	~50 pm/V @ -6V bias (dominantly QCSE region)	9 GHz	4Gbps / 95 mV	~916
				7 Gbps / 265mV	~7130

*: For this calculation we only estimate $CV_{pp}^2/4$ and neglect the static contribution (I_{bias}×V_{bias})/r_b, since I_{bias} is

2.2 Characterization of CRISP bulk InP-on-Si resonator modulators

As described at the beginning, we also investigated bulk InP-on-Si resonator modulators. These modulators have the advantage of operating over a wider temperature range and wavelength range with almost similar modulation sensitivity.

The bulk modulator is designed to maximize the Franz-Keldysh which is the analogous effect of the quantum confined Stark effect in quantum well. The epitaxial layer stack is similar to the multi-QW one but where the 16 QWs/QBs are replaced with an InAlGaAs p-n junction. The epi design of the bulk modulators has been described in our earlier work[34]. The composition of the InAlGaAs is set to have a bandgap of 1280 nm at 4K (1376 nm at 300K), while the thickness (p-200 nm and n-100 nm) and the doping (p-2.0×10^{17} and n-4.0×10^{16}) of the p and the n layers are chosen to maximize the electro-optic index variation. To reach large field confinement, InP is used to replace the top and bottom separated confinement heterostructure (SCH) of the multi-QW stack, since it holds a smaller optical refractive index.

For a similar modulation sensitivity (i.e., similar value of V_π), the bulk modulator suffers from larger optical absorption, as we demonstrated in the device characterization between 77 K and room temperature. At 4K the bulk modulators do not provide the modulation sensitivity performance of QW modulators. Figure 9 shows the experimental results for the bulk modulators. As seen from the eye diagrams in Fig. 9b-c, the best modulation voltage with an open eye diagram was at ~150 mVpp while for the QW modulators we could achieve open eye for a modulation voltage < ~5-10 mVpp.

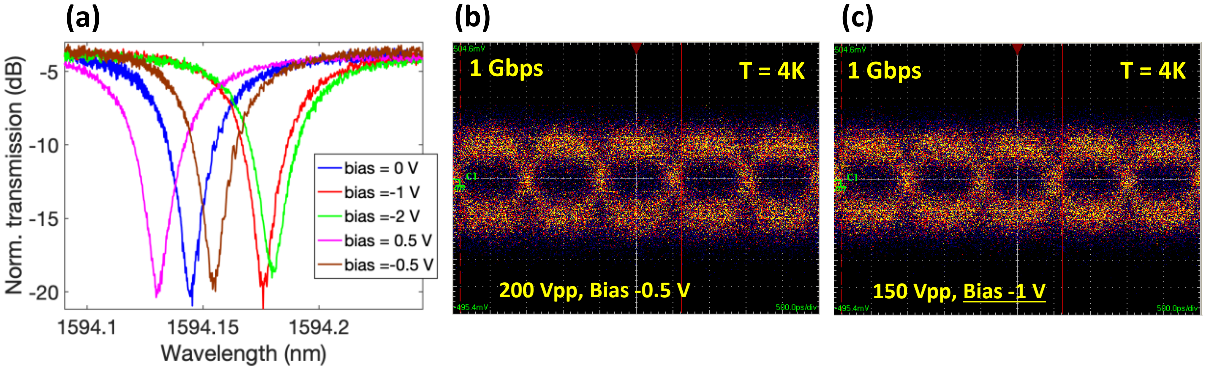


Fig. 9: (a) Resonance spectrum of a bulk InP-on-Si resonator modulator at 4K and for different applied voltages. The resonator has a geometry and dimensions and radius similar to the QW modulator shown in Fig. 6a. (b)-(c) Measured eye diagram of the modulator at 1Gbps data rate and for modulation voltages of 200 mVpp and 150 mV, respectively. Unlike the QW modulator results (Fig. 7), the bulk modulators could not operate at much smaller modulation voltages.

To increase the sensitivity, we must reduce the band-gap paying the price of a larger propagation loss. Based on these observations, we focused mostly on the QW modulators for the experiments. The fabrication steps of the bulk modulators are similar to that of QW modulators.

3 Heterogeneous InP-on-Silicon fabrication process

The major fabrication steps of heterogeneous InP-on-Si modulator is depicted in Fig. 10. It consists of silicon patterning and etching, III-V bonding and processing, followed by metal deposition and rapid thermal annealing for the contacts. All lithographic steps are performed using a 248 nm deep-ultra violet (DUV) stepper. The entire fabrication takes place at a wafer scale (4” SOI wafer), which demonstrates the potential scalability of the process.

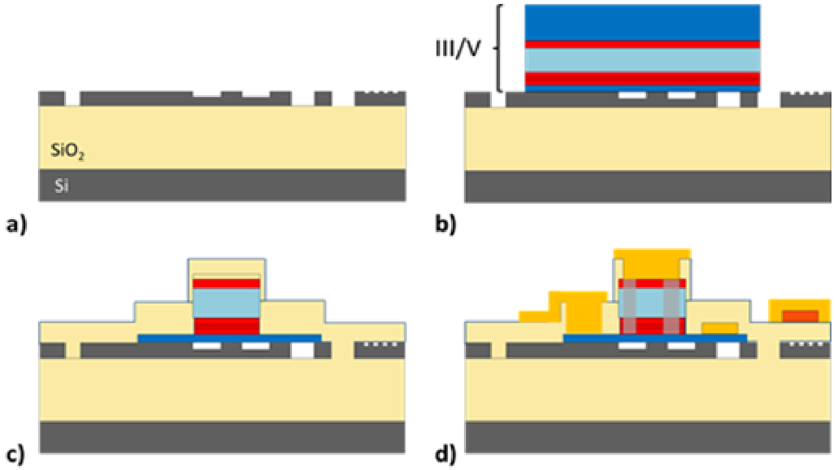


Figure 10. Major steps of the InP-on-Si modulator fabrication (a) Silicon fabrication, (b) InP-on-Si bonding, (c) InP patterning and cladding, (d) Metallization and defining the contact electrodes.

The first part of the process consists on the patterning of the silicon layer for the fabrication of the silicon waveguide, ring resonator and edge couplers. Due to the multiple silicon etching steps with different etch depths, a SiO_2 hard-mask is used to define the waveguides. The etching process is then carried out with the shallowest etch (240 nm) for defining the ring and waveguide. A second deep etch step is used to remove the left silicon to define the edge coupler (500 nm). Since the hard-mask is used to define the waveguides during the entire process, it ensures that the transitions between waveguides with different etch depths are self-aligned and not subject to lithographic misalignment in the stepper.

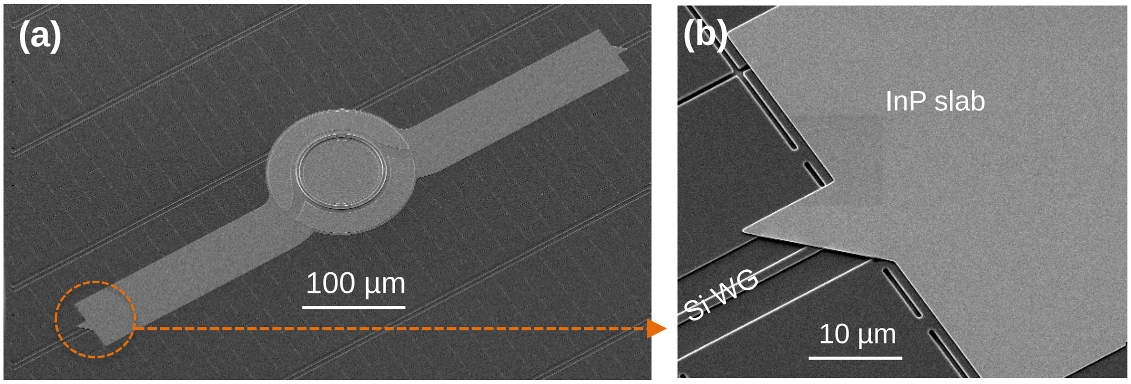


Figure 11. (a) Scanning electron microscope image of the InP-on-Si ring before the stapes of metallization. (b) A zoomed view of the transition region from the Si waveguide to the InP-on-Si region. The transition region has been designed in that shape to minimize back reflection and improve the mode conversion from the silicon waveguide to the heterogeneous cross-section[35]

The III-V die is bonded using an O_2 plasma activated direct bonding procedure, and the bulk of the InP substrate is removed using a combination of lapping and wet etching, leaving the III/V epitaxial layers used for the cryogenic modulator The modulator mesas are etched using a series of both $CH_4/H_2/Ar$ dry etches and wet etches containing HCl or H_3PO_4. Figure 11 shows the SEM images of the InP-on-Si resonator device before adding the oxide cladding and the metallization process. After the III-V processing is complete, SiO_2 is sputtered, and vias are opened to expose the n and p-contacts. The last part of the fabrication is deposition of the various metals for n-(Pd/Ge/Pd/Au/Ti) and p-contacts (Pd/Ti/Pd/Au), and probe pads (Au/Ti). More details on the fabrication of heterogeneous silicon photonic devices are discussed in M. Davenport[34]. A schematic overview of the main step of the heterogeneous fabrication is shown in Fig. 12.

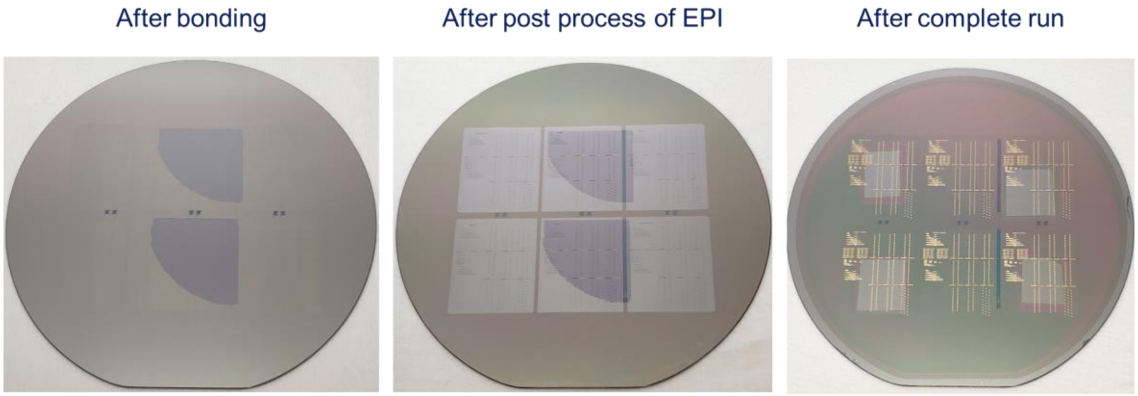


Figure 12. Fabrication run overview

3.1 Results summary of the 3 fab runs

During the project we had 3 full fabrication runs during which we optimized the fabrication yield, metal contacts, the fiber-to-chip coupling, and reduced the propagation loss in the silicon waveguides. The details of the improvements are reported in the following.

3.1.1 First fabrication run (April-May 2020)

One of the major challenges of the first fabrication run was the low fabrication yield (10%). The circular shape of the device and the tiny features make the fabrication of our device difficult to resolve all the features, as shown in Fig. 13 for a sample device.

The poor fabrication yield of the metal contact was also responsible for the high resistance of the p-contact. This

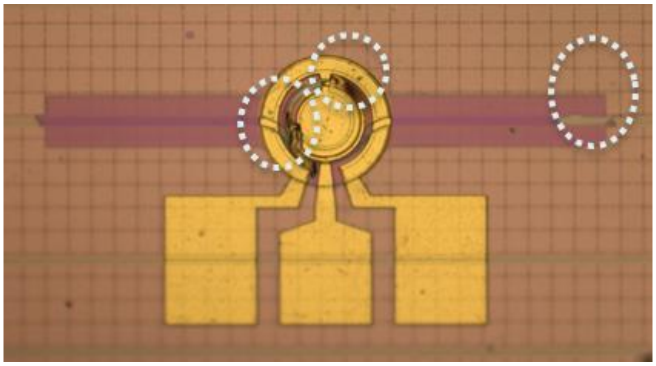


Figure 13. A sample device fabricated in the first run. The metal contacts were not fully resolved and part of the n-III-V layer was partially removed. The unresolved features are highlighted in the micrograph.

large value contributes to increasing the total resistance of the modulator, limiting the electro-optical bandwidth at low temperature and inhibiting the operation at 4K.

The semiconductor-metal contact resistances are characterized using the transfer length method (TLM). The TLM test pattern consists of an array of identical contacts with various spacings[36]. The measured resistances between neighboring contacts are shown in Fig. 14, for both n- and p-type contacts, respectively. The contact resistance is the y-intercept divided by 2 of the line that fit the experimental data. As shown in the figure, the value of the p-contact resistance is significantly larger than the n-contact resistance.

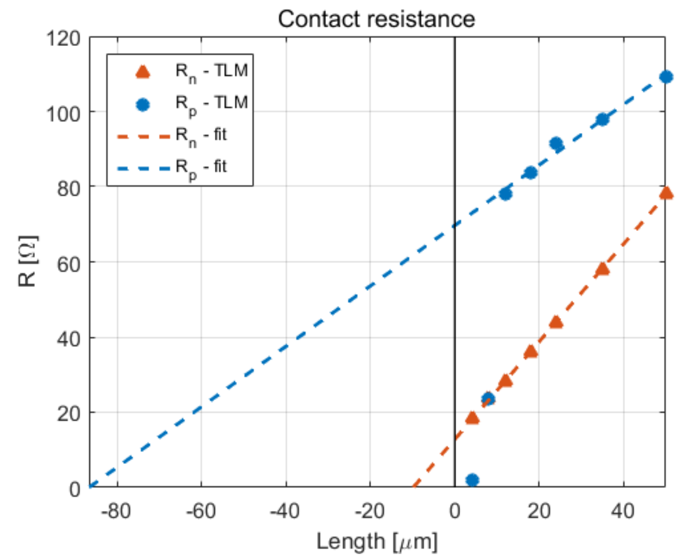


Figure 14. TLM characterization of the n- and p- contacts at room temperature (run 1).

Fiber-to-chip coupling is a central task of the CRISP project. During the first fabrication run investigated two strategies to achieve large fiber-to-chip coupling: flare taper and inverse taper.

The flare taper consists in widening the waveguide in order to match the mode in the fiber. This strategy is optimal when the buried oxide (BOX) is thin, because the mode is mainly confined in the waveguide and does not leak into the silicon substrate. However, the large refractive index contrast causes large reflections and limits the fiber-to-chip coupling.

The inverse taper design consists in reducing the waveguide cross-section such that the mode expands in the silica cladding. In this manner, the mode in the waveguide can match the mode in the fiber. The main disadvantage of this approach is the strong leakage in the silicon substrate, and a BOX of 2 µm or thicker is needed.

In the first fabrication run we consider 1 µm-thick BOX, which is the standard used at UCSB for the heterogeneous silicon photonic platform. Table 6 shows the results when 5 different flare tapers were tested. In this case, the minimum coupling loss is below 6.5 dB/facet.

Table 6. Tapered lensed fiber 2.0um spot / CHIP #3

Dev. no.	Tip. Width (µm)	Angle (deg)	Input Power (mW)	Output Power (µW)	Total Coupling Loss (dB)	Wavelength
75	3	0	4.36	123	**15.5**	1550.230
76	4	0	4.36	217	**13.0**	1550.240
77	5	0	4.36	186	**13.7**	1550.280
78	6	0	4.36	140.4	**14.9**	1550.240
79	7	0	4.36	92	**16.8**	1550.230

Table 7 shows the result of the inverse taper design. We tasted 5 tapers with different tip width: from 155 nm up to 235 nm, with a step of 20 nm, while the silicon thickness is about 270 nm. As show the total coupling loss is very large due to large mode leakage into the substrate. In this case, the minimum coupling loss is about 10 dB/facet but can be further reduced by consider a thicker BOX layer.

Table 7. Tapered lensed fiber 2.0um spot / CHIP#1

Dev. no.	Tip. Width (µm)	Angle (deg)	Input Power (mW)	Output Power (µW)	Total Coupling Loss (dB)	Wavelength
0	0.155	7	4.36	1.13	**35.7**	1550.230
1	0.175	7	4.36	3.37	**31.1**	1550.230
2	0.195	7	4.36	7.17	**27.8**	1550.230
3	0.215	7	4.36	24.06	**22.6**	1550.230
4	0.235	7	4.36	41.10	**20.3**	1550.230

3.1.2 Second fabrication run (Sept-Oct 2020)

In the second fabrication run, we significantly improved the fabrication yield. We evaluated that about 98% of the ring modulators were successfully fabricated and have consistent IV characteristics and optical spectra. A micrograph of a device fabricated in the second run is shown in Fig. 15. As it appears clear from the micrograph, all the features of the device look clearly resolved.

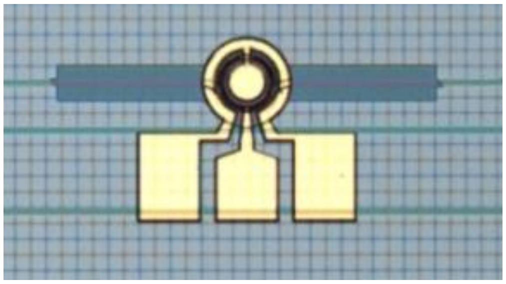


Figure 15. A sample device fabricated in the second run. Metal contacts and all semiconductor layers are clearly resolved.

The yield improvement was also observed in the contact resistances. The p-contact resistance was reduced by ~30x while the n-contact improved by ~1.5-2x, as shown in Fig. 16.

In order to improve the fiber-to-chip coupling, we focused our design optimization on the inverse taper and repeated the fabrication run with a 2 μm-thick BOX SOI wafer.

The results in Fig. 17 show the fiber-to-chip coupling for different taper tip cross-section. The tip width sweeps from 155 nm up to 275 nm with a step f 20m, while the silicon thickness is about 270 nm. The characterization of the fiber-to-chip coupling shown that the best taper is 215 nm wide and it can perform fiber-to-chip as low as 3.5dB/facet at a wavelength of 1550 nm. However, in the second run we selected a 185 nm wide tip, which limits the coupling coefficient to 5.5dB/facet at the same wavelength.

3.1.3 Third fabrication run (May-July 2021)

During the second run we observed a large propagation loss in the silicon waveguide, which was caused by the III-V fabrication process. After some test, we observed that the loss can be reduced by adding a wet etching step and limiting the dry etching to the area in the proximity of the device.

The third fabrication run is performed including all the previous optimization, which includes yield improvements, contact optimization, fiber-to-chip coupling, and reduction of the silicon propagation loss. Figure 18 shows an observed an improvement larger than 20 dB between the second the third run. Table 8 shows a comparison of the three fabrication runs.

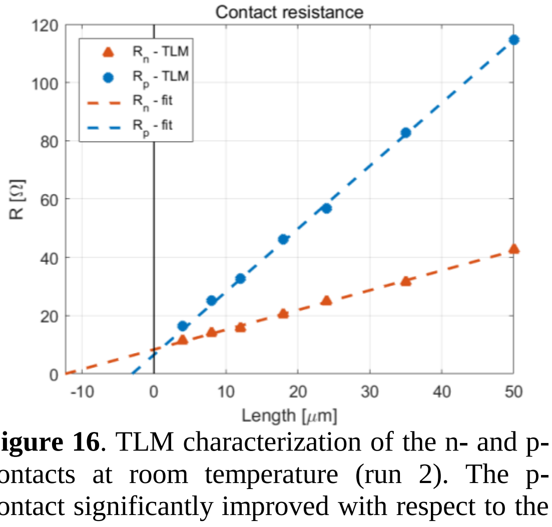


Figure 16. TLM characterization of the n- and p-contacts at room temperature (run 2). The p-contact significantly improved with respect to the previous fabrication run.

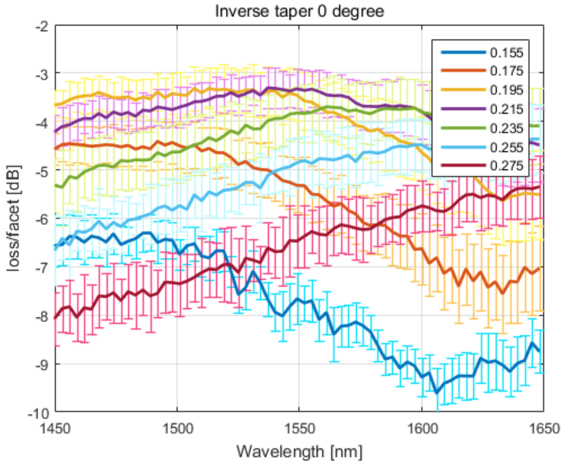


Figure 17. Fiber-to-chip coupling loss for the inverse tapers in the waveguide test-structure.

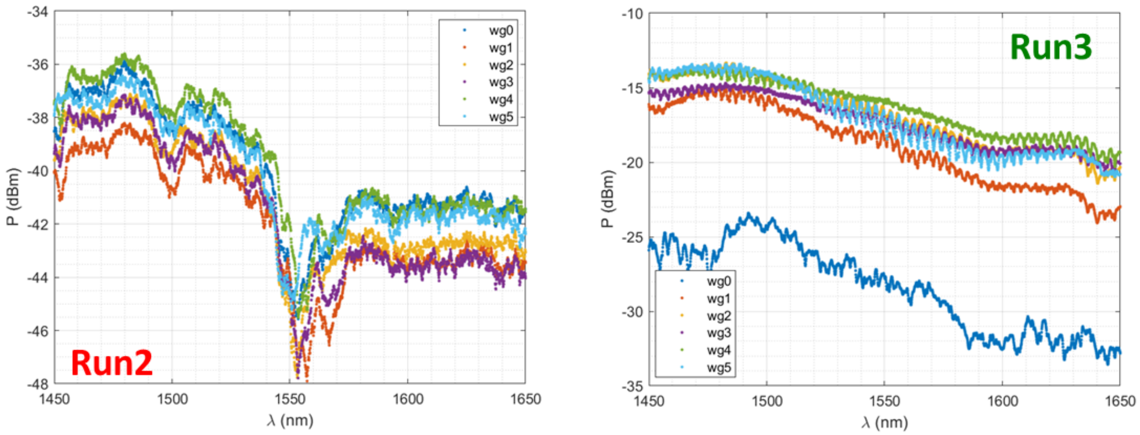


Figure 18. Insertion loss of 7 mm long passive waveguide. The optical input power is 1W. The coupled power consists of the fiber-to-chip coupling loss and the propagation loss. We observed an improvement larger than 20 dB between the second the third run.

Table 8. Fabrication Run Comparison. In the table we highlight in red the results that did not meet the metrics, in light orange the mid-term achievement, and in green the final results that meet the metrics by implementing all the improvements

Fab. run	Yield	p-contact resistivity $[\Omega*cm^2]$	n-contact resistivity $[\Omega*cm^2]$	Fiber-to-chip coupling (dB/facet)	Silicon prop. loss (dB/cm)	Comments
Run 1	**10%**	**$3.03\cdot10^{-3}$**	**$6.33\cdot10^{-5}$**	**10.0**	N/A	• Low yield • High-resistance contacts • Large fiber-to-chip coupling (values refer to inverse taper design)
Run 2	**98%**	**$1.01\cdot10^{-5}$**	**$5.18\cdot10^{-5}$**	**5.5**	**~20**	• High Yield • Low metal-semiconductor contact resistance • Good fiber-to-chip coupling because of 2μm BOX • Large propagation loss
Run 3	N/A	**$1.73\cdot10^{-5}$**	**$5.62\cdot10^{-5}$**	**3.5**	**~2**	• Improved fiber-to-chip coupling (better taper tip aspect ratio) • Low propagation loss

4 Quantum well: material stack design

A central aspect of our work is in designing the III-V alloy to perform the largest electro-optic (EO) phase shift with minimal optical absorption at 4K. In a III-V multi QWs, the dominant electro-optic effects that contribute to change of the refractive index are either due to free carriers or due to changing the energy bands when applying an external electric field as described below:

1- The EO effects caused by free carrier are the band-filling (Burstein-Moss) effect, the plasma dispersion effect, and the band-shrinkage effect[37]. Among them, the band-filling is the strongest, while the band shrinkage is the weakest and becomes considerable only at much higher doping concentrations than the one in our case[38].
2- The EO effects due to change of energy band is Quantum Confine Stark effect[39] (QCSE) when applying an electric field.

Note that the III-V alloy also has the Pockels EO effect[40]. However, the contribution of the Pockels effect is small, and in particular in a ring configuration becomes negligible, since all phase shift acquired for propagation around one-half of the ring is reversed during propagation around the other half.

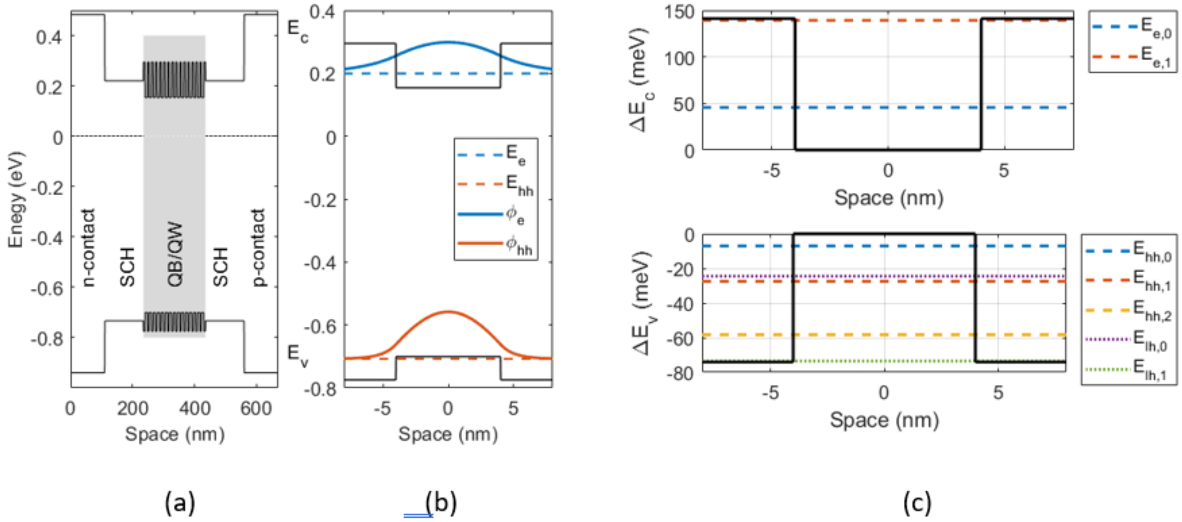


Figure 19. (a) Energy band diagram of the III-V alloy stack, which includes the n- and p-contacts (i.e., InP), the SCH and the multi QW layer (i.e., InAlGaAs). (b) Energy level and wavefunction of the electron and hole in the fundamental energy state. (c) Energy levels of the electron in the conduction band (top), the heavy-hole (dashed) and light-hole (dotted) in the valence band.

A challenge is in designing the III-V alloy material composition for 4K operation knowing that the low temperature optoelectronic properties of III-V alloys are neither fully characterized nor theoretically modeled in the literature. A significant problem in the theoretical modeling is the sharp transition in the Fermi-Dirac distribution function making numerical calculations prone to instabilities. To overcome these issues, we design the III-V alloy material composition for 4K operation based on experimental data on modulator devices that were optimized to operate at room temperature[41] and employ the empirical expressions exists for the variation of bandgap energy and lattice constants versus temperatures to optimize the material for 4K operation.

We design the alloy composition of the epitaxial stacks of QW/QB to maximize both the QCSE and the free carrier effects. Figure 19(a)-(c) show the energy band diagram and the energy levels of QW/QB as well as the electron and hole state. More consideration on the energy band gaps of the heterogeneous silicon/III-V phase modulator can be found in H.-W. Chen[42]. To achieve large

QCSE, electrons and holes must be confined in the QW layer by optimizing the band offset in the conduction (ΔE_c) and valence (ΔE_v) bands. The band offsets are temperature independent[43,44] and changes solely with the alloy composition. Their values are chosen high enough that both electrons and holes are confined when in their ground states with energy $E_{e,0}$ and $E_{hh,0,}$ respectively.

When an external voltage is applied, it is desirable to deplete the QW/QB area from electrons and holes, maximizing the refractive index variation due to free carriers. If ΔE_c and ΔE_v are too large, the excited states exist and the carriers will stay in the QW rather than being depleted. Since free carrier energy levels depend on the band offset and the QW, we fix ΔE_c and the well thickness such that only the ground state is occupied by electrons. As a result, ΔE_c equals to the energy of first excited state ($E_{e,1}$) and the QW thickness is set to 8 nm. On the other hand, the barrier thickness is set equal to 5 nm to make QWs independent.

The value of ΔE_v and energy level of holes are defined from the previous constraint. Minimizing the optical absorption is another important design goal in the modulator. Significant absorption occurs when the photon energy of the injected light approaches the exciton binding energy of the QW, $\Delta E_{PL}=E_{e,0}-E_{hh,0}$. To minimize the optical absorption, the exciton binding energy (i.e., photoluminescence) is set ~100 meV larger than the energy of operating wavelength[45] ~800 meV (λ~1550 nm). From those consideration, the optimal band gaps (in wavelength) for the SCH, QW and QB are $\lambda_{g,SCH}=1.3$ µm, $\lambda_{g,QW}=1.16$ µm, $\lambda_{g,QB}=1.46$ µm, respectively.

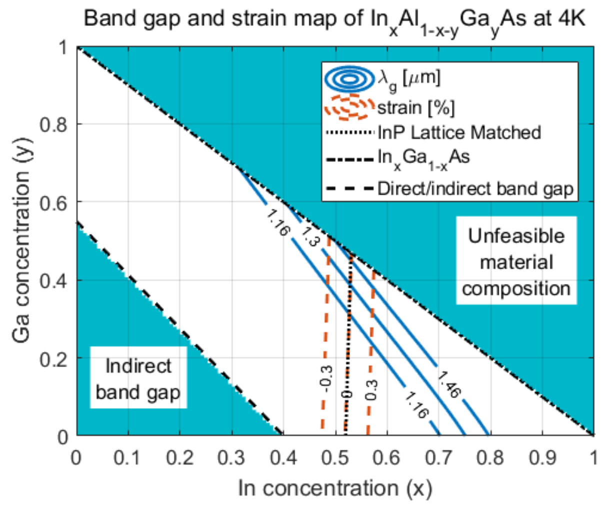


Figure 20. Band gap in wavelength (blue solid line) and lattice strain relative to InP (red dashed line) for InAlGaAs with respect to indium (x) and gallium (y) concentrations. The feasible alloy compositions are those where the cumulative concentration of indium and gallium are below 1 (black dot dashed like). In the same plot, we indicated the transition between direct and indirect band gap (black dashed line), and the alloy composition that matches the lattice of InP (black dotted line).

The material composition of QW, QB and SCH are determined from Fig. 20, which shows the band gap and the strain at 4K of InAlGaAs as a function of the indium (x) and gallium (y) concentrations in the alloy. The domain of the feasible material composition is $0 \le x \le 1$, $0 \le y \le 1$ and $0 \le 1 - x - y$. The area above $1 - x - y = 0$ is unfeasible since the concentration of aluminum becomes negative (dash dot line in the figure). For low concentrations of In and Ga, the bandgap of InAlGaAs is indirect, which is undesirable (dashed line). Thus, the region of interest falls between the dashed and the dot-dashed black line. The black dotted line indicates material compositions that match the lattice of the underlying InP, which is preferred in order to avoid stress in the material at cryogenic temperatures.

The contour lines of constant band gap energies (blue solid lines) for a temperature T=4K are computed interpolating the bang gap energies of InAs, AlAs and GaAs at the same temperature[46,47]. Specifically, the energy gap at 4K of such binary compounds is calculated using the Varshni's empirical equation

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{1}$$

$$\lambda_g(T) = \frac{hc}{E_g(T)} \tag{2}$$

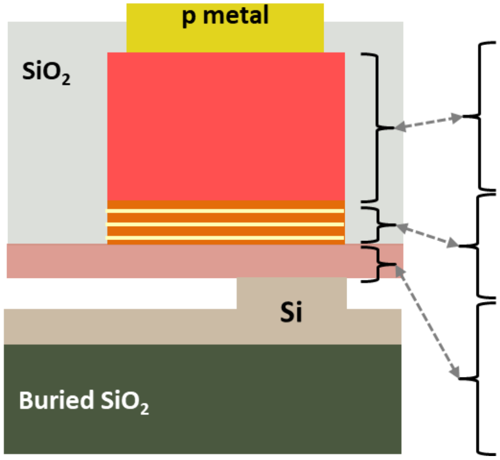
where $E_g(T)$ is the temperature dependent band gap, $\lambda_g(T)$is the corresponding wavelength, $E_g(0)$, α and β material constants, h the Plank constant, and c the speed of light in the vacuum. For InP, InAs, AlAs and GaAs the constants, $E_g(0)$, α and β by are reported in Table 9.

Table 9: Fitting parameters of the Varshni's empirical equation for the alloy used in CRISP modulator[42]. From Eq. (1), the energy band gap at 4K can be easily computed.

Material	$E_g(0)$	α	β
InP	1.4236	$0.363 \cdot 10^{-3}$	162
InAs	0.417	$0.276 \cdot 10^{-3}$	93
AlAs	3.099	$0.885 \cdot 10^{-3}$	530
GaAs	1.519	$0.541 \cdot 10^{-3}$	204

The lattice mismatch between InAlGaAs and InP native substrate is shown in the same figure (red dotted line in Fig. 20). We seek a material composition with minimal strain at room temperature, which can be exacerbated at low temperature and diminish the performance of the material. As a result, we obtain the following material composition for the SCH (Ga= 0.386, In=0.529), the QW (Ga= 0.449, In=0.530) and the QB (Ga= 0.312, In=0.527), which are determined by the intersection of the three blue lines and the black dot curve in Fig. 20.

The epitaxial layers are grown one after the other on the same substrate using metal organic chemical vapor deposition (MOCVD) technique. If the concentration of all the elements (i.e., In, Al, and Ga) are varied during the growth process, it is difficult to control the growth conditions, and the final composition may deviate from the original design. Since the concentration of indium does not change significantly, we set the In concentration equal to the average value 0.5296, while the concentrations of Ga and Al are adjusted to achieve the desired energy gap. The final stack and alloy composition are reported in Fig. 21. Beyond the SCH, QW and QB, the composition of the other layers is similar to the one used for other heterogeneous III-V/silicon photonics[35, 43, 48].



Layer	Material	Thickness [nm]	Doping [1/cm^3]
p-contact	$In_{0.53}Ga_{0.47}As$	100	p-1.5 $\cdot 10^{19}$
smoothing	$In_{0.586}Ga_{0.414}As_{0.888}P_{0.112}$	25	p-3.0 $\cdot 10^{18}$
	$In_{0.729}Ga_{0.271}As_{0.587}P_{0.413}$	25	p-3.0 $\cdot 10^{18}$
p-cladding	InP	1000	p-1.5 $\cdot 10^{18}$
	InP	200	p-8.0 $\cdot 10^{17}$
	InP	250	p-5.0 $\cdot 10^{17}$
SCH	$In_{0.5296}Al_{0.3339}Ga_{0.3365}As$	125	n-1.0 $\cdot 10^{17}$
well (×15)	$In_{0.5296}Al_{0.0192}Ga_{0.4512}As$	8	n-1.0 $\cdot 10^{17}$
barrier (×16)	$In_{0.5296}Al_{0.1574}Ga_{0.3130}As$	5	n-1.0 $\cdot 10^{17}$
SCH	$In_{0.5296}Al_{0.3339}Ga_{0.3365}As$	125	n-1.0 $\cdot 10^{17}$
n-contact	InP	110	n-2.0 $\cdot 10^{18}$
superlattice	$In_{0.85}Ga_{0.15}As_{0.327}P_{0.673}$	7.5	n-1.0 $\cdot 10^{18}$
	InP	7.5	n-1.0 $\cdot 10^{18}$
	$In_{0.85}Ga_{0.15}As_{0.327}P_{0.673}$	7.5	n-1.0 $\cdot 10^{18}$
	InP	7.5	n-1.0 $\cdot 10^{18}$
bonding layer	InP	10	n-3.0 $\cdot 10^{18}$

Figure 21. III/V epitaxial layers used for the cryogenic QW based modulator

5 Fiber-to-PIC Packaging

Packaging PIC devices for cryogenic operation (< 10 K) is not a mainstream technology, and it comes with new challenges on top of the ones present at room temperature. First, the relative alignment between the fibers and the chip needs to be maintained to below a micrometer of precision in spite of the thermal contraction and warping of the materials. Second, the constituent materials have to maintain their physical properties at low temperature. This is particularly challenging for adhesives such as epoxies, which are integral to most packaging techniques and tend to crack or delaminate upon cooldown.

The samples developed under CRISP use silicon waveguides that are thicker than in most PIC devices. This renders them unsuitable for grating coupling, which is otherwise attractive for low temperature operation because of its relaxed requirements on fiber-chip alignment. Instead, the scheme we have developed uses edge coupling, where cleaved fiber facets are pressed against the polished waveguide facets on the chip and fixed in place permanently with epoxy. Because of constraints set by the silicon waveguides and the thickness of the cladding on the chips, the optical mode of the waveguide is small, which reduces the tolerance for alignment error. To match a fiber mode as well as possible to this small mode, we use fiber with ultra-high numerical aperture (UHNA-7 from NuFern).

The assemblies fabricated in this way all look similar to the one shown in Fig. 22, with the PIC chip mounted on a large, rigid base. The fibers are aligned to the on-chip waveguide and secured with epoxy ("A-joint"). Some distance away from each A-joint, a second epoxy joint is applied to provide stability and strain relief. We refer to this as the "B-joint". We found that a few millimeters of separation between joints A and B is required to allow the fibers to take up stress due to mismatched CTEs in the assembly. For most of our work, the base and B-joint supports consisted of silicon chips, assembled with the same epoxy used for the fibers. In later experiments, we have improved on this, as will be discussed below.

The techniques and setup have undergone continual development and improvement over the course of the program. Below, we present the current process and the development that led to it, along with lessons learned along the way.

5.1 Choice of adhesive

Epoxy based adhesives are the only ones that form sufficiently stiff joints in the cured state to maintain alignment between fiber and chip. However, this stiffness also makes the epoxy prone to cracking or delaminating from the surfaces it adheres to due to different rates of thermal contraction. Epoxies that are able to withstand cryogenic conditions tend to have high elasticity and CTE, which is detrimental to the integrity of the joints.

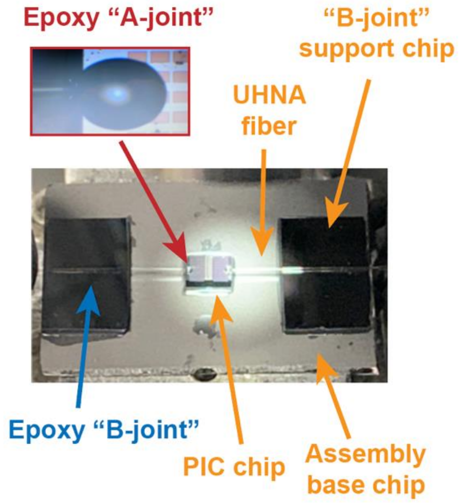


Figure 22. Packaging assembly consisting of several silicon pieces that support the fibers and the PIC chip. Epoxy is used to adhere the fiber facet to the PIC chip after alignment ("A-joint") and to stabilize the fiber and provide strain relief ("B-joint").

Early in the program, we experimented with UV-curable epoxies, since these allow the A-joints to be established rapidly once the optical elements are in good alignment. However, we found that the heat produced during the curing is substantial, and sufficient to disrupt the alignment. We also applied epoxy droplets of several kinds to bare silicon chips and cooled them to 4K to see how well they fared mechanically, and found that several of them tended to crack and delaminate. We eventually settled on EP29LPSP from Masterbond as a suitable adhesive. This is a thermally cured epoxy that came recommended by the T&E teams, and our tests showed that its sturdiness at low temperature, optical transparency, and low viscosity in the uncured state made it suitable for the task. As the EP29LPSP epoxy approached the end of its specified shelf life, we observed negative effects on the quality of the joints we could make. To prolong the life of the epoxy and use our time efficiently, we now mix the epoxy in batch and portion it into single-use syringes which are kept uncured by immersion in liquid nitrogen until they are thawed and used.

5.2 Mechanical alignment

The station used for packaging is shown in Fig. 23. Each of the two fibers is mounted on an XYZ stage with piezoelectric actuation option using magnetic clips. During fiber alignment, we use a power meter and a tunable laser with a manual polarization controller to monitor the optical transmission from one fiber to the other one. For rough alignment and diagnostics, we use an overhead microscope setup with two cameras, one for visible light and one for IR light at the target wavelength for the PIC chip.

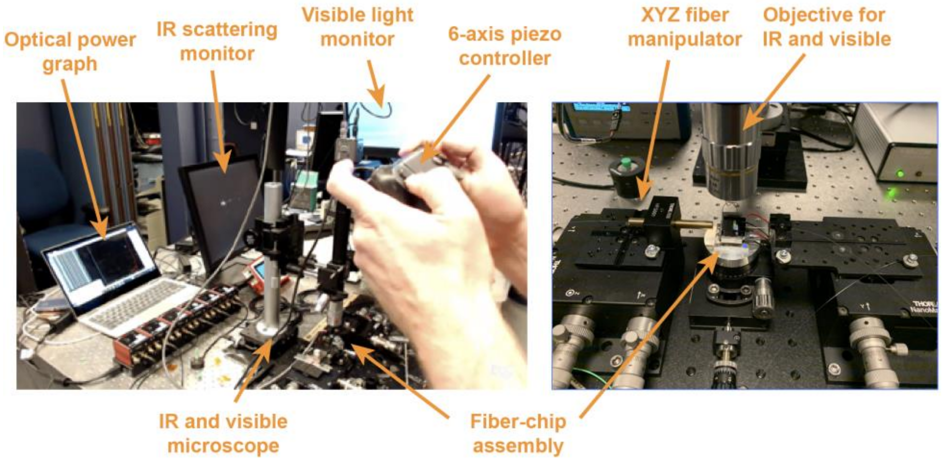


Figure 23. Packaging station at BBN, where the optical alignment and assembly is done.

We found that observation of scattered IR light is essential for quickly achieving sufficiently good alignment to get a measurable optical transmission. After that point, we adjust the positions of both fibers to optimize the optical transmission.

We initially used manual micrometer screws to actuate the XYZ stages and later wrote software to control the fiber movements through a computer interface. This interface allows us to move the two fibers with a video game controller while monitoring the transmission on-screen. We found that the alignment can be done quickly and with great precision in this way, without introducing vibrations. However, later in the project, we also found that the optical transmission tended to degrade during curing and attributed this to slow drift in the piezo elements. For this reason, we have returned to manual actuation, using the computer interface only to passively plot the optical transmission.

Since the core of the fiber has to press against the facet of the waveguide with micrometer separation or less, it is essential that the cleaved edge of the fiber is flat and clean. To keep the edges of the cleaved fiber from protruding beyond the core and preventing good coupling, we have experimented with rounding the edge by manual polishing. We found that it is possible to produce a rounded corner in the cladding without damaging the fiber core (Fig. 24), and that this is helpful for achieving a good fiber-to-chip interface. However, debris from the polishing can interfere with the coupling, so the rounded fibers need to be cleaned carefully. After some experimentation with this technique, we believe that the main benefit of rounding the fiber corners is to improve the quality of the epoxy joints (see below).

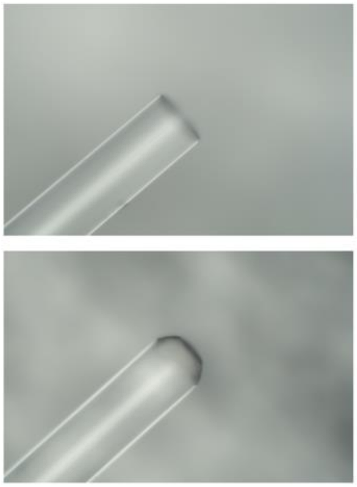


Figure 24. UHNA-7 fiber before and after rounding

Once the fibers are well aligned with the PIC chip waveguide and lightly pressed against the chip facets, we secure the tips of the fibers to the PIC chip with epoxy (A-joints in Fig. 22)

5.3 Epoxy application and curing

EP29LPSP is a thermal epoxy that requires a temperature of about 60°C to cure overnight. To this end, the sample stage that holds the assembly contains a Peltier element that can maintain a constant temperature using closed-loop control. In early experiments, we aligned the fibers and applied the A-joint epoxy at room temperature, but found that the heating required to cure the epoxy tended to bring the fibers out of position. Therefore, we moved to a procedure where the sample remains at a temperature of 58°C throughout the alignment, epoxy application, and curing. It was clear from early on that the forces on the fibers during application and curing of B-joints are sufficient to ruin the alignment unless the A-joints have already been fully cured. The full assembly process thus includes two overnight rounds of epoxy curing.

We found that large amounts of epoxy tend to disrupt the joints mechanically and also scatter light optically, particularly on PIC chips with thin SiO_2 cladding. To keep the epoxy localized, we initially used a syringe mounted on a micromanipulator, actuated through a flexible hose to reduce accidental movement and vibration (Fig. 25). To achieve still higher precision and use smaller droplets for the A-joints, we replaced the syringe with a short length of fiber and used that as a brush for the epoxy. This allows us to use very minimal amounts of epoxy and have good control of its placement.

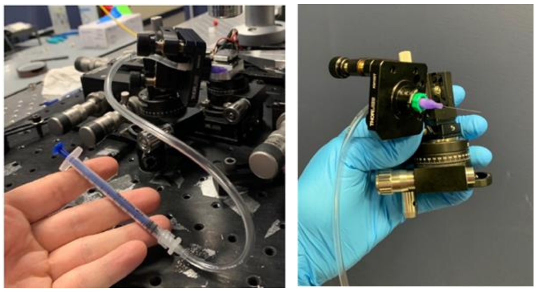


Figure 25. Micromanipulator equipped with a syringe for epoxy application.

Using a small amount of epoxy for the A-joint helps maintain the optical coupling, but it also makes the assembly fragile. To prevent the finished assemblies from breaking, we attempted to reinforce the A-joints with a second application of epoxy. However, we found that this extra epoxy was difficult to apply in a controlled manner and degraded the optical transmission.

By rounding the cladding of the fibers, as described above, we create a larger and rougher surface area for the epoxy to adhere to, compared to using fibers that have only been cleaved. We tried to also roughen the fiber cladding further away from the facet to increase the area on the fiber that the epoxy is able to wet, but found that this made the fibers so fragile that they would snap during handling.

5.4 Assembly materials and designs

We initially used assemblies consisting of several Si chips as shown in Figs. 22 and 26, left. As we moved from samples with lower sensitivity to misalignment to less forgiving ones, we found that the transmission degraded strongly during cooldown. This was sometimes, but not always, accompanied with visible damage. We attributed this to high CTE of silicon relative to the glass

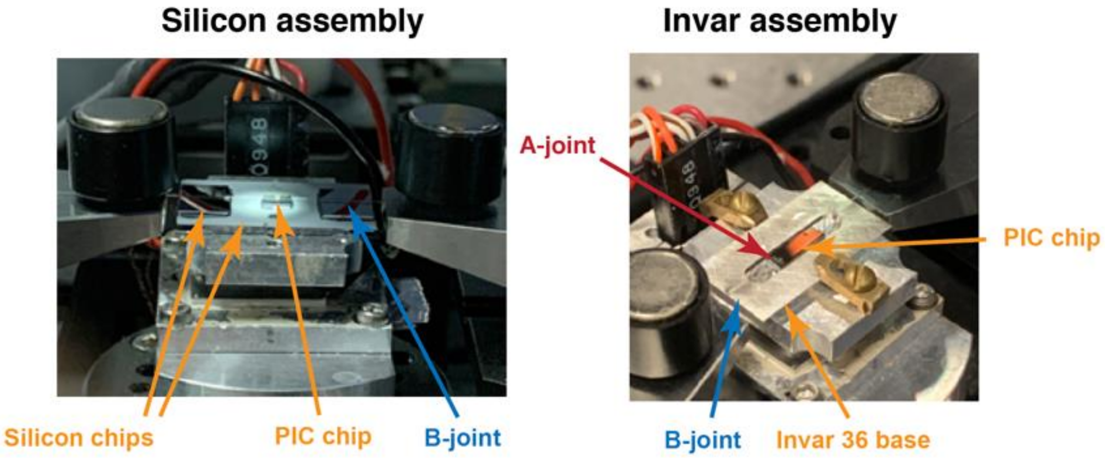


Figure 26. Comparison between an assembly using silicon chips (left) and one using a machined Invar 36 base (right).

fibers, the multiple large epoxy joints between chips, and the possibility for non-uniform contraction in the silicon base chip warping the assembly and stressing the fibers and joints.

To solve this problem, we moved away from assemblies made from silicon chips and opted instead to fabricate monolithic sample mounts from Invar 36 (Fig. 26, right). Invar 36 is a specialty alloy with very low CTE and low propensity to warp due to thermal stress. It is similar in strength to stainless steel and can be cut by standard machine tools. In samples with low tolerance for misalignment, we saw an immediate improvement in how well the assemblies could withstand cooling to 4K when moving from stacked-silicon bases to monolithic Invar bases.

5.5 Device specifics and post-fabrication improvement

During the development of the cryo-packaging, we used samples from different sources and fabrication runs and noticed important differences between them.

Much of the initial process development was done with test chips from Sandia, which use thin silicon with thick cladding. This creates a large optical mode at the facet that is relatively easy to match to the UHNA-7 fiber, and the thick cladding keeps epoxy on top of the chip from interfering with the optical transmission. Using these chips, we achieved a stable process where the assemblies worked at a temperature of 4K.

Moving the process to a first batch of UCSB-made CRISP chips (Fab #2) presented a new challenge, partly because the tolerances of the fiber-chip interface were smaller as a result of the thick silicon. Later, we also found that the 1 µm thick cladding on these chips was insufficient to fully confine the light inside the slim waveguide section near the chip facet, which gave rise to severe scattering when we applied epoxy. Because of these factors, we were unable to make these assemblies work at 4K.

Using a batch of CRISP samples with thicker cladding (1 µm; Fab #3 passives), we were again able to achieve a working packaging process, with ~50-70% estimated yield and total loss of 7 and

13 dB per facet for the two assemblies tested at 4K. While other changes to the packaging procedure also mattered for this improvement, we could determine through experiment that the thicker SiO_2 cladding played an important role.

All active modulator samples have thinner cladding than the Fab #3 passives (1 µm versus 2 µm), and to achieve good coupling to these devices, we did a series of experiments where we deposited an extra layer of SiO_2 on finished chips and re-polished the facets. Using our epoxy application manipulator to move a small droplet of epoxy along the waveguide and monitoring the optical transmission, we could determine that the extra oxide strongly reduces the amount of scattered light, thus facilitating low-loss packaging. We conducted such tests with 1 µm and 2 µm thick SiO_2 and found that the thicker oxide yields the best results. We also found that it is possible to remove as much as 2 µm of oxide from the contact pads by mechanical means and get good electrical connection by wire bonding. We have since used this procedure on pre-tested active modulators which are to be packaged and sent to T&E teams for evaluation.

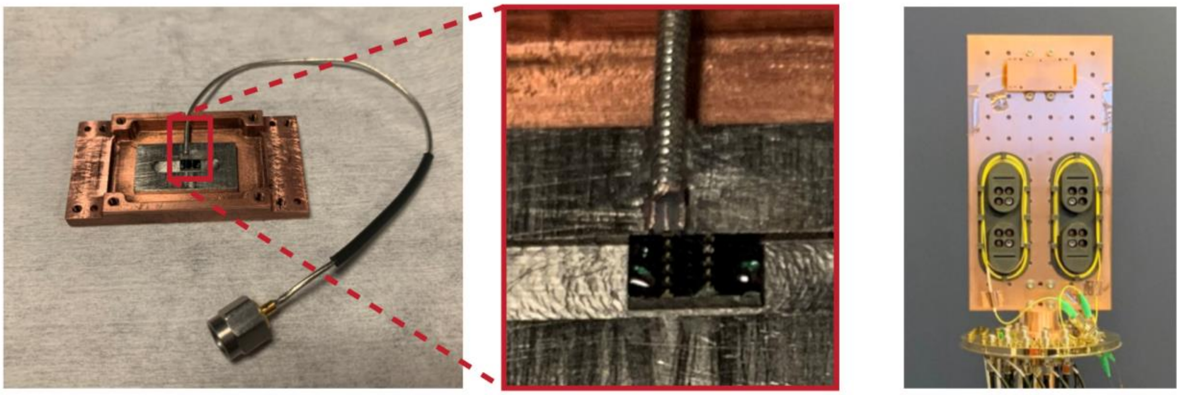


Figure 27. Left, Invar 36 assembly base with coaxial RF connection. The 1.2 mm cable is connected to the contact pads of the CRISP modulator by low-inductance wire or ribbon bonds. Here, the invar base is placed inside a copper box that protects and thermalizes the sample, and provides added strain relief for the fibers when fully assembled**. Right,** cryo-package ready for cooldown. The protective sample enclosure at the top contains the CRISP chip. This photo does not include the coaxial cable. The fibers are spooled below the sample box, and the whole copper back plate can be shipped to T&E teams after in-house testing

5.6 Electrical coupling and cryogenic hardware

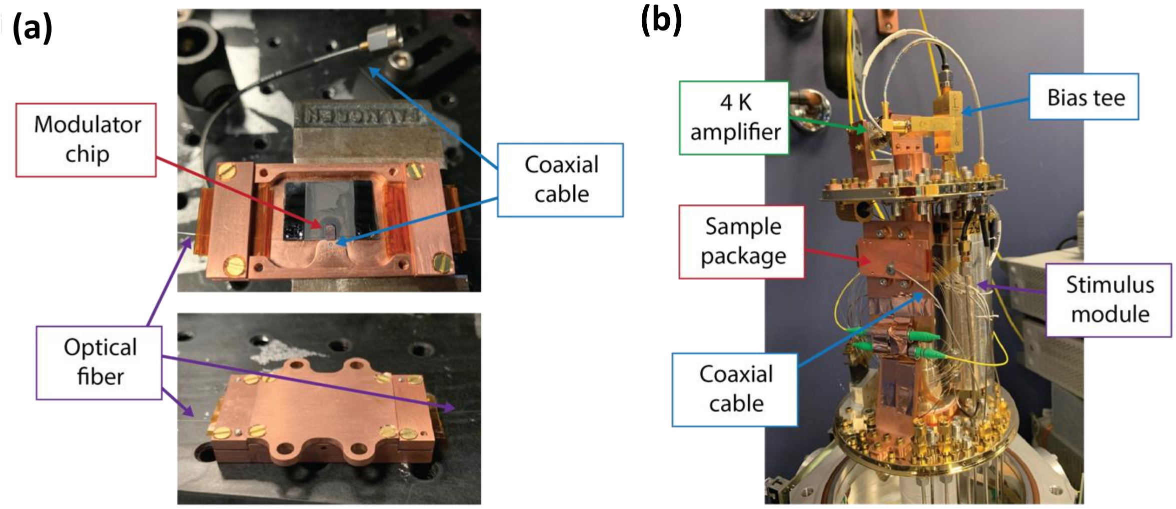
To keep the finalized assembly from breaking during handling and transport, and to provide a high-bandwidth electrical connection, we mount it in a custom box as shown in Fig. 27. The electrical pads on the modulator samples are bonded with gold wire or ribbon directly to the center conductor of a 1.2mm hand-formable coaxial cable. This allows the connections to have low inductance and thus support high data rates (>10 GSPS).

The copper box includes additional strain reliefs which squeeze the fibers gently between Kapton tape buffers, so as to not damage the fibers or reduce their optical performance. The box is attached to a large copper plate, along with custom 3D-printed spools for the fibers. The whole plate can be mounted in the cryostat supplied by NIST for the SuperCables project (Fig. 27, right), and afterwards be shipped out for independent T&E team testing with minimal risk of mechanical disruption.

6 Integration and Test of Packaged Modulator with Stimulus Module

As we discussed in the last report, since we had issues in the fabrication of InP-on-Si modulators and they didn't operate at low temperatures, we decided to package our existing auxiliary Si resonator modulators that we already had in our lab. These Si modulators operated at T = 40 K rather than T = 4K and required an externally amplified input signal. While this setup differs from the one we ultimately seek to demonstrate, experiments with the Si modulator allow us to accomplish the following goals:

1. Demonstrating operation of the Stimulus Module (SM) in our laboratory, using the fridge supplied by NIST as part of the project.
2. Demonstrating that the electrical and optical packaging of modulator devices at our lab works under realistic conditions.
3. Showing that the complete electro-optical signal chain is functional and ready to be used with upcoming CRISP devices.
4. Preparing for experiments using the SM in combination with BBN's test equipment.



Note: We changed the bias tee from the one shown to a model with better low-frequency performance for the experiments.

Fig. 28: (a) Si PIC modulator packaged with optical fiber and RF cables. (b) The cryogenic setup used for testing the packaged modulator and the stimulus module.

A packaged Si PIC is shown in Fig. 28a.The details of the device fiber and electric packaging was described in the previous report, and the packaging design was approved by LPS for calorimetric testing. We make electrical connections to the PIC by wire-bonding the on-chip contacts to a coaxial cable, in a process identical to the one used for CRISP devices.

The cryogenic part of the experimental setup is shown in Fig. 28b, and a schematic of the full setup is shown in Fig. 29. The diagram is intended as a general illustration, where different parts of the circuit are active for the different experiments presented below. Some connections differed from the diagram for certain tests as described in the text.

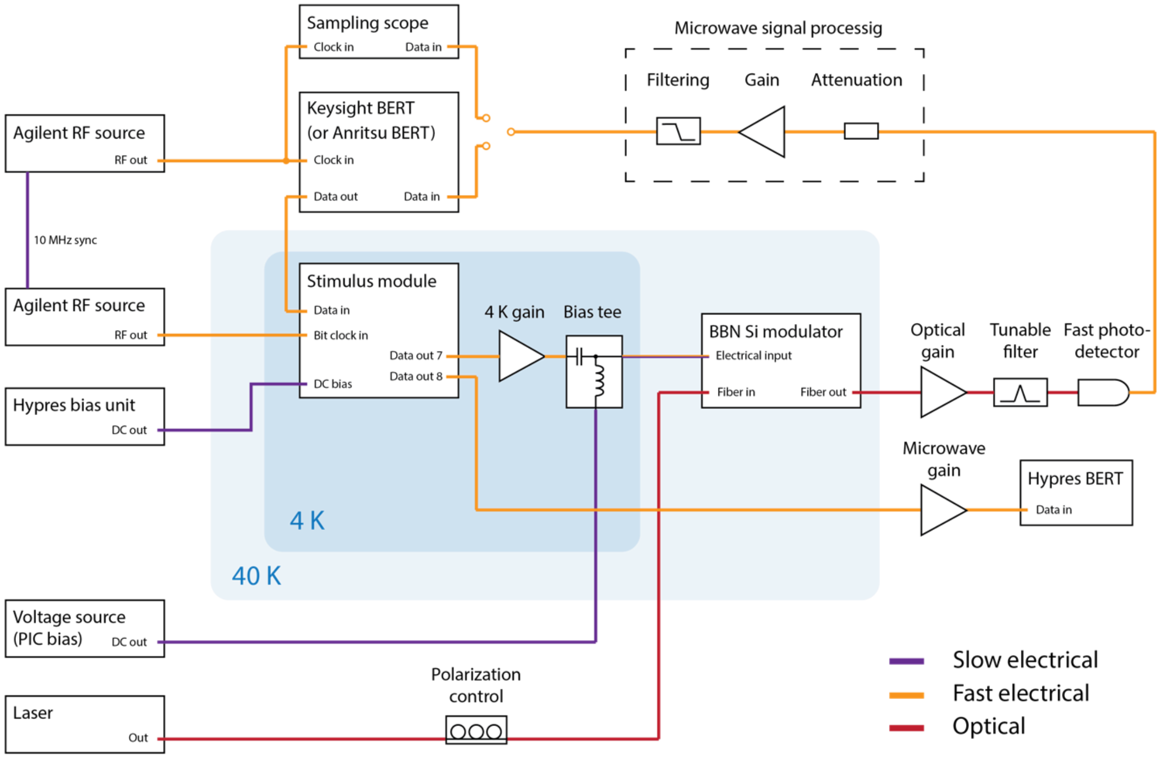


Fig. 29: Schematic diagram of the experimental setup used for test and integration of packaged PIC modulator with the Stimulus Module.

Testing the stimulus module: We tested the direct output of the stimulus module (Output 8) with the Hypres Bit Error Rate Tester (BERT). An Agilent RF source supplied the clock signal to the SM at a fixed frequency of 10.16 GHz to match the data rate expected by the BERT.

We found that the Bit Error Rate (BER) of the SM had a clear dependence on SM temperature, and found the best results when the fridge temperature was regulated to 4.75 K. Without active control, the temperature is below 3 K with the SM and the cold amplifier under power. The BER also depends to some extent on the amplitude of the SM clock, and we found input powers to the fridge around -23 dBm to give the best results. For externally supplied data, the phase between SM clock and PG clock had to be adjusted with care to achieve the highest possible BER.

After optimizing these parameters, we were able to achieve error free operation over long timescales (BER < 1e-13) for the SM-generated PRBS7 pattern, the SM-generated PRBS15 pattern, and the externally supplied PRBS15 pattern.

Testing the modulator with the stimulus module: For this experiment, we coupled Output 7 of the SM to the (AC-coupled) input of the cryogenic amplifier, which was also mounted at the base temperature stage of the fridge. The amplifier output connects to a bias tee at 4K which is necessary to reverse-bias the modulator diode.

The optimization of the BER involves the adjustment of many experimental parameters. The most important ones are shown in Table 10. While no definite set of parameters consistently resulted in error-free operation, we were always able to fine tune the parameters within the ranges shown in the table and reach error free operation for PRBS-7 (internally generated by the SM) at a data rates of 4 GBPS. The lowest BER measured for PRBS15 was in the range of 1e-10 at 3 GBPS, with values of 1e-6 and lower being straightforward to achieve.

Table 10: The experiment setting parameters for the BER characterization

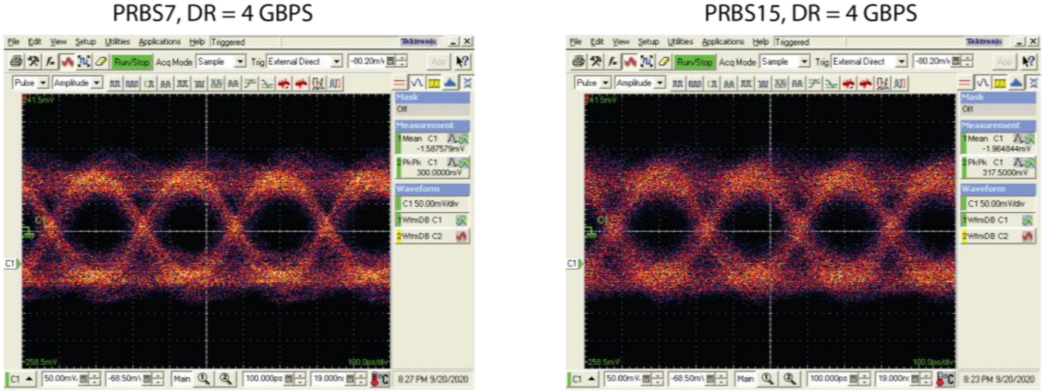
Parameter	Representative values
Laser power	5-8 mW. Limited by saturation of the optical amplifier
Laser wavelength	1552.9 nm, dependent on modulator bias
Modulator bias	-0.1 V to -0.5 V. Does not strongly affect the BER in this range
4K amplifier gain	36-40 dB, estimated based on spec. and applied DC power
Polarization	Not measured. Subject to drift during and between experiments
Microwave gain at room temp.	3 – 6 dB, using Bluebird amp. and pre-attenuation

Because the cryogenic amplifier used to drive the Si PIC has a specified lower frequency limit of 10 MHz, the PRBS15 bit sequence is more difficult to bring to low BER than PRBS7, since it carries more information at low frequencies. This constraint is specific to the Si PIC, since the CRISP modulators are intended to operate directly with the output from the SM without pre-amplification. Apart from the amplifier, the essential components in the signal chain have low-end frequency cut-offs well below 1 MHz. Fig. 30 shows eye diagrams for PRBS7 and PRBS15 at a data rate of 4 GBPS.

Testing the SM with the BBN BERT: Future CRISP devices will be tested with BBN BERT (Anritsu) instead of the NIWC BERTs (Hypres and Keysight). To confirm that we are ready for such experiments, we tested the BER of the SM and the modulator using BBN's Anritsu BERTWave.

The BERTWave does not in its current configuration support direct input clocking at the data rate frequency, and it also does not provide an output clock at this frequency. This complicates the synchronization with the SM, which requires a clock signal at the data rate. We tried synchronizing the Anritsu BERT by a 10 MHz clock supplied from the RF source used to clock the SM, but found that this approach yielded inadequate results. Instead, we used the BERTWave's ability to accept a clock at a sub-multiple of the data rate, and supplied this clock from a second Agilent RF source. The two RF sources (for SM clock and BERT clock) are synchronized through a 10 MHz reference clock. This setup works well for testing the sequences generated internally by the SM (PRBS7 and PRBS15) using the Anritsu BERTWave.

When feeding the high-quality signal from the SM directly to the BERTWave through the Hypres Bluebird amplifier, we can easily achieve virtually error-free operation using the arbitrary data rates between 0.125 GBPS and 6 GBPS. Using the optical modulator and the rest of the optical signal chain, measured BER < 1e-9 with the BERTWave with PRBS7 data at 4 GBPS.



PRBS7, DR = 4 GBPS

Acq Mode Sample
Trig External Direct -80.20mV
Mean C1 -1.587579mV
PkPk C1 300.0000mV
C1 50.00mV/div
C1 50.00mV -68.50mV 100.000ps 19.000ns
8:27 PM 9/20/2020

PRBS15, DR = 4 GBPS

Acq Mode Sample
Trig External Direct -80.20mV
Mean C1 -1.964844mV
PkPk C1 317.5000mV
C1 50.00mV/div
C1 50.00mV -68.50mV 100.000ps 19.000ns
8:23 PM 9/20/2020

Fig. 30: Measured eye diagrams of the packaged PIC modulator driven by the Stimulus Module, for PRBS7 and PRBS15 at a data rate of 4 GBPS.

More details can be found in the report to Brad. Given that we can adjust the parameters to achieve BER < 1e-9 already without such optimization, our conclusion from this experiment is that the setup is adequate for testing CRISP devices.

7 Conclusion and the Remaining Work (see also Table 2 and Table 3 in Section 1)

In summary, we have demonstrated a cryogenic (4K) QW InP-on-Silicon photonic integrated circuit platform with high-speed electro-optic modulators with record low modulation voltage – as low as 4.5 mV with an electric energy consumption of less than 5 aJ/bit, and with on chip laser power within 50-100 µW. We achieve this performance by employing the two strong EO mechanisms of band-filling and QCSE in the InP QW alloys, and by optimizing the design of the QW stacks to enhance these EO effects at 4K. To our knowledge, this is the first demonstration of a heterogeneous InP-on-Si photonics operating at such low temperatures as well as record achieved performance. Our CRISP modulators combine the benefits of InP for enhanced cryogenic EO functionality, and silicon for low-loss scalable photonic circuitry to realize a scalable EO modulator platform. They demonstrate the ability to provide seamless integration with micro-electronics and superconducting integrated circuits, which can strongly benefit emerging cryogenic classical and quantum information systems and pave the way for efficient, high-bandwidth optical data-links between 4K and room temperature environments.

Also in this project, we investigated bulk InP-on-Si resonator modulators at 4K, and achieved modulation voltages as small as 150 mVpp which is still much lower than the demonstrated Si modulators. However the modulation voltage of the bulk InP-on-Si was much higher than the QW modulators.

For modulator packaging and integration with the SC stimulus module, we started with our existing Si resonator modulators with a modulation driving voltage of ~0.4Vpp to achieve operation at a temperature of 40K. These auxiliary devices allowed us develop fiber-to-chip packaging recipes for cryogenic operation as well as systematic experimentation with the SC stimulus module. The packaging of our CRISP modulator and integration with the SC stimulus module is still an ongoing effort in our group as we aim to demonstrate direct modulator to SC stimulus module integration without the need for cryogenic amplification.

To achieve the ultimate scalability goals of the SuperCables program, there are a few aspects of our CRISP modulator and packaging work that requires more improvement and investment:

- The top cladding oxide of the CRISP modulator was only 1 micron, which was somewhat thin and degraded fiber to chip coupling efficiency. As a result of this degradation, we measured a 12dB/facet loss. However, in both theory and experiment with other passive devices using thicker cladding, we observed only about 3-3.5 dB/facet loss. The thin top cladding also affected the fiber-to-chip packaging performance. A future fabrication improvement would be to use a thicker cladding oxide (e.g., >2.5 micron).
- During CRISP, we had a limited number of epi growth (1) and device fabrication runs (3) and these limitations did not allow us perform a wider range of design variations and optimizations, especially as one fabrication run did not yield any working devices. We believe there is significant room for improvement of the modulator performance both through the material epi design and the modulator design to increase the modulation sensitivity, speed, and lower the energy consumption.
- To increase the yield of the CRISP fabrication, we need to transition this effort to a professional foundry. We are currently investigating this.
- The cryogenic PIC experiments were by nature slow. Nevertheless, we were able to achieve significant understanding and insights on the optimal design and performance of these devices as well as their packaging. A future investment in the CRISP modulator could yield a dramatic performance improvement in these devices.
- Most of our experiments were limited to using intensity modulation techniques. In a future effort with more optimized devices and measurement time, we can focus on using phase modulation schemes (DPSK, BPSK) to dramatically reduce energy consumption and required laser power.

8 References

1. Rumley, S. *et al.* Optical interconnects for extreme scale computing systems. *Parallel Comput.* **64**, 65–80 (2017).
2. Miller, D. A. B. Attojoule optoelectronics for low-energy information processing and communications. *J. Light. Technol.* **35**, 346–396 (2017).
3. Holmes, D. S., Ripple, A. L. & Manheimer, M. A. Energy-Efficient Superconducting Computing—Power Budgets and Requirements. *IEEE Trans. Appl. Supercond.* **23**, 1701610–1701610 (2013).
4. Mukhanov, O. *et al.* Scalable Quantum Computing Infrastructure Based on Superconducting Electronics. *Tech. Dig. - Int. Electron Devices Meet. IEDM* **2019-Decem**, 2019–2022 (2019).
5. Grutter, K., Salter, T. & Horton, T. Findings of the 2nd Photonics and Electronics Technology for Extreme Scale Computing Workgroup (REPETE) - Design Challenges for Socket Level Photonic I/O. (2020).
6. Lecocq, F. *et al.* Control and readout of a superconducting qubit using a photonic link. *Nature* **591**, 575–579 (2021).
7. Gehl, M. *et al.* Operation of high-speed silicon photonic micro-disk modulators at cryogenic temperatures. *Optica* **4**, 374–382 (2017).
8. Mukhanov, O. A. *et al.* Superconductor digital-RF receiver systems. *IEICE Trans. Electron.* **E91-C**, 306–317 (2008).
9. Mukhanov, O. A. Energy-Efficient single flux quantum technology. *IEEE Trans. Appl. Supercond.* **21**, 760–769 (2011).
10. Tanaka, M., Ito, M., Kitayama, A., Kouketsu, T. & Fujimaki, A. 18-GHz, 4.0-aJ/bit operation of ultra-low-energy rapid single-flux-quantum shift registers. *Jpn. J. Appl. Phys.* **51**, 0–4 (2012).
11. Tanaka, M., Kitayama, A., Koketsu, T., Ito, M. & Fujimaki, A. Low-energy consumption RSFQ circuits driven by low voltages. *IEEE Trans. Appl. Supercond.* **23**, 4–7 (2013).
12. Youssefi, A. *et al.* A cryogenic electro-optic interconnect for superconducting devices. *Nat. Electron.* **4**, 326–332 (2021).
13. Eltes, F. *et al.* An integrated optical modulator operating at cryogenic temperatures. *Nat. Mater.* **19**, 1164–1168 (2020).
14. Lee, B. S. *et al.* High performance integrated graphene electro-optic modulator at cryogenic temperature. *Nanophotonics* **10**, 99–104 (2021).
15. Chakraborty, U. *et al.* Cryogenic operation of silicon photonic modulators based on DC Kerr effect. *Optica* **7**, 1385–1390 (2020).

16. Gevorgya, H. *et al.* Cryo-Compatible, Silicon Spoked-Ring Modulator in a 45nmCMOS Platform for 4K-to-Room-Temperature Optical Links. *Opt. Fiber Commun. Conf.* 4–6 (2021).

17. Zhao, X. & Suo, Z. Electromechanical instability in semicrystalline polymers. *Appl. Phys. Lett.* **95**, 93–96 (2009).

18. Xu, Y. *et al.* Photorefraction-induced Bragg scattering in cryogenic lithium niobate ring resonators. *Opt. Lett.* **46**, 432–435 (2021).

19. Sze, S. M. & Ng, K. K. *Physics of semiconductor devices*. (2006).

20. Melikyan, A. *et al.* High-speed plasmonic phase modulators. *Nat. Photonics* **8**, 229–233 (2014).

21. Heni, W. *et al.* Plasmonic IQ modulators with attojoule per bit electrical energy consumption. *Nat. Commun.* **10**, 1–8 (2019).

22. Hiraki, T. *et al.* Heterogeneously integrated III-V/Si MOS capacitor Mach-Zehnder modulator. *Nat. Photonics* **11**, 482–485 (2017).

23. Han, J. H. *et al.* Efficient low-loss InGaAsP/Si hybrid MOS optical modulator. *Nat. Photonics* **11**, 486–490 (2017).

24. Komljenovic, T. *et al.* Photonic integrated circuits using heterogeneous integration on silicon. *Proc. IEEE* **106**, 2246–2257 (2018).

25. Roelkens, G. *et al.* III-V-on-silicon photonic devices for optical communication and sensing. *Photonics* **2**, 969–1004 (2015).

26. Bennett, B. R., Soref, R. A. & Del Alamo, J. A. Carrier-induced change in refractive index of InP, GaAs, and InGaAsP. *IEEE J. Quantum Electron.* **26**, 113–122 (1990).

27. Chuang, S. L. *Physics of photonic devices*. (2009).

28. Franciosi, A. & Van De Walle, C. G. Heterojunction band offset engineering. *Surf. Sci. Rep.* **25**, 1–140 (1996).

29. Guden, M. . & Piprek, J. Material parameters of quaternary III - V semiconductors for multilayer mirrors at 1.55 μm wavelength. *Model. Simul. Mater. Sci. Eng.* **4**, 349–357 (1996).

30. Ohe, H., Shimizu, H. & Nakano, Y. InGaAlAs multiple-quantum-well optical phase modulators based on carrier depletion. *IEEE Photonics Technol. Lett.* **19**, 1816–1818 (2007).

31. Mendoza-Alvarez, J. G. *et al.* Analysis of Depletion Edge Translation Lightwave Modulators. *J. Light. Technol.* **6**, 793–808 (1988).

32. Chen, H.-W. High-Speed Hybrid Silicon Mach-Zehnder Modulator and Tunable

Microwave Filter. (University of California Santa Barbara, 2011).

33. Li, G. L. & Yu, P. K. L. Optical intensity modulators for digital and analog applications. *Jounral Light. Technol.* **21**, 2010–2030 (2003).

34. P. Pintus, Z. Zhang, S. Pinna, M. A. Tran, A. Jain, MJ Kennedy, L. Ranzani, M. Soltani, and J. E. Bowers, "Characterization of heterogeneous InP-on-Si optical modulators operating between 77 K and room temperature," APL Photonics, Special Topic on Hybrid Integration Beyond Silicon Photonics, vol. 4, pp. 100805, 2019

35. Davenport, M. L. Heterogeneous Silicon III-V Mode-Locked Lasers. (University of California Santa Barbara, 2017).

36. Schroder, D. K. *Semiconductor material and device characterization*. (John Wiley & Sons, 2006).

37. Bennett, B. R., Soref, R. A. & Del Alamo, J. A. Carrier-induced change in refractive index of InP, GaAs, and InGaAsP. *IEEE J. Quantum Electron.* **26**, 113–122 (1990).

38. Botteldooren, D. & Baets, R. Influence of band-gap shrinkage on the carrier-induced refractive index change in InGaAsP. *Appl. Phys. Lett.* **54**, 1989–1991 (1989).

39. Chuang, S. L. *Physics of photonic devices*. (2009).

40. Yariv, A. & Yeh, P. *Optical waves in crystals*. (1984).

41. Chen, H. W., Kuo, Y. H. & Bowers, J. E. A Hybrid Silicon-AlGalnAs Phase Modulator. *IEEE Photonics Technol. Lett.* **20**, 1920–1922 (2008).

42. Chen, H.-W. High-Speed Hybrid Silicon Mach-Zehnder Modulator and Tunable Microwave Filter. (University of California Santa Barbara, 2011).

43. Vurgaftman, I., Meyer, J. R. & Ram-Mohan, L. R. Band parameters for III-V compound semiconductors and their alloys. *J. Appl. Phys.* **89**, 5815–5875 (2001).

44. Franciosi, A. & Van De Walle, C. G. Heterojunction band offset engineering. *Surf. Sci. Rep.* **25**, 1–140 (1996).

45. Guden, M. . & Piprek, J. Material parameters of quaternary III - V semiconductors for multilayer mirrors at 1.55 µm wavelength. *Model. Simul. Mater. Sci. Eng.* **4**, 349–357 (1996).

46. Williams, C. K., Glisson, T. H., Hauser, J. R. & Littlejohn, M. A. Energy bandgap and lattice constant contours of iii-v quaternary alloys of the form Ax By Cz D or ABx Cy Dz. *J. Electron. Mater.* **7**, 639–646 (1978).

47. Glisson, T. H., Hauser, J. R., Littlejohn, M. A. & Williams, C. K. Energy bandgap and lattice constant contours of III-V quaternary alloys. *J. Electron. Mater.* **7**, 1–16 (1978).

48. Tran, M. A. Heterogeneous Silicon/III-V Photonic Integration for Ultralow Noise Semiconductor Lasers. (University of California Santa Barbara).