AFRL-RY-WP-TR-2023-0016

DISCRETE-TIME mm-WAVE PROCESSORS FOR SCALABLE DIGITAL ARRAYS

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University of Southern California

MAY 2023
Final Report

AIR FORCE RESEARCH LABORATORY
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1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED	
		START DATE	END DATE
May 2023	Final	9 October 2018	10 January 2023

4. TITLE AND SUBTITLE

DISCRETE-TIME mm-WAVE PROCESSORS FOR SCALABLE DIGITAL ARRAYS

5a. CONTRACT NUMBER	5b. GRANT NUMBER	5c. PROGRAM ELEMENT NUMBER
FA8650-19-1-7996	N/A	62716E

5d. PROJECT NUMBER	5e. TASK NUMBER	5f. WORK UNIT NUMBER
N/A	N/A	Y1WP

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8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)		10. SPONSOR/MONITOR'S ACRONYM(S)	11. SPONSOR/MONITOR'SREPORT NUMBER(S)
Air Force Research Laboratory, Sensors Directorate Wright-Patterson Air Force Base, OH 45433-7320 Air Force Materiel Command, United States Air Forces	Defense Advanced Research Projects Agency (DARPA) 675 North Randolph Street Arlington, VA 22203	AFRL/RYDI	AFRL-RY-WP-TR-2023-0016

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14. ABSTRACT

The program is to develop and demonstrate wideband mm-wave element level digital array technology employing the discrete time processing units at mm-wave and data conversion at sub-harmonic frequencies to reduce system cost. The advantages of discrete-time processing over conventional analog processing, in the context of digital arrays, include the ability to perform more complex functions in smaller footprints (e.g. frequency conversion, filtering, and data conversion in one block), reconfigurability, and performance improvement with technology scaling.

15. SUBJECT TERMS

discrete time processing circuits, filtering, data conversion

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES
a. REPORT	b. ABSTRACT	C. THIS PAGE		
Unclassified	Unclassified	Unclassified	SAR	18

19a. NAME OF RESPONSIBLE PERSON	19b. PHONE NUMBER *(Include area code)*
Tony Quach	N/A

PREVIOUS EDITION IS OBSOLETE.

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Table of Contents

Section **Page**

List of Figures

Figure **Page**

1 SUMMARY

The University of Southern California (USC) has worked on mm-wave receivers and transmitters towards fully digital array architectures.

This research provided full or partial support for 6 Ph.D. students and 1 postdoctoral scholar. Two of the Ph.D. students have graduated: Dr. Ayonag Zhang is currently a postdoctoral scholar at Harvard University, and Dr. Pingyue Song is currently an ASIC design lead at the Twenty/Twenty Therapeutics. Dr. Shiyu Su, who was a postdoctoral scholar partially supported through this effort, is currently an Assistant Professor at the University of Waterloo.

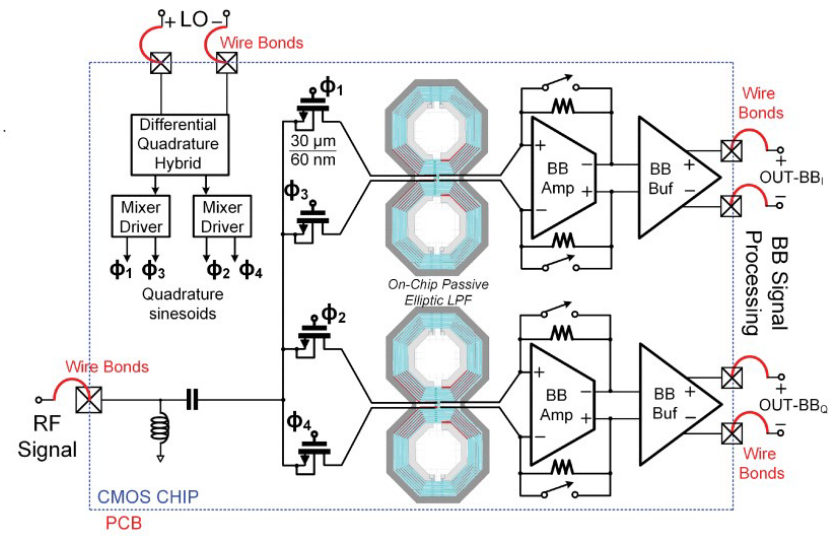
This report summarizes the major results and includes references to the publicly available peer-reviewed publications that include further technical details.

While the contract has officially ended, the students are still working on (1) writing papers that result from their research, (2) conducting measurements, and (3) taping out chips. These efforts, all partially supported through this contract up to the end of the contract, are now supported by other mechanisms.

1.1 mm-Wave Mixer-First Receiver with Selective Passive Lowpass Filtering

This effort demonstrated a mm-wave mixer-first receiver where the passive switching mixer is followed with an on-chip selective passive low-pass filter (LPF). The footprint of the passive LPF is small due to the large channel bandwidth that is associated with mm-wave applications. The main advantage of a passive mixer-first receiver over the conventional receivers that include a frontend low-noise amplifier (LNA) is the lower power consumption for the same linearity requirement. The downside of this scheme is a higher noise figure (NF). This higher NF may be acceptable in large-scale arrays, and in scenarios where the wireless link is limited by unwanted blockers/jammers, given that in a phased array the signal-to-noise ratio improves with the array size.

A proof-of-concept prototype in TSMC 65nm CMOS covers the 21-29 GHz RF input frequency range and provides a 0.5 GHz instantaneous single-sideband (SSB) bandwidth. Thanks to the application of passive mixers and onchip selective LPF, the passband to stopband rejection is over 49 dB, the in-band ICP_{-1dB} is -6 dBm, and the out of band B_{-1dB} is 3.4 dBm. Details of the design, analyses, simulations, and measurements are reported in [1][2].



Tuning Range (GHz)	21 ~ 29	
Instantaneous SSB-BW$_{3dB}$ (GHz)	0.5	0.8
DSB NF (dB)	12.0 ~ 14.5	17.3 ~ 20.8
RF-to-BB Gain (dB)	3 ~ 6	-15 ~ -12
ICP$_{1dB}$ (dBm)	-6.0	3.0
B$_{1dB}$ (dBm)	3.4 (Δf/BW = 2) 6.5 (Δf/BW = 12)	4.1 (Δf/BW = 1.2) 7.2 (Δf/BW = 7.5)
Stop-Band to Pass-Band Rejection (dB)	49	34
Transition Band BW (GHz)	1.2	1.1
Power (mW)	Mixer-Driver: 13.2 BB Amp: 9.6 22.8	Mixer-Driver: 13.2 BB Amp: 0 13.2
Supply Voltage (V)	1.2	
Active Area (mm^2)	0.63	
Technology	65 nm CMOS	
Architecture	Baseband Amp ON	Baseband Amp OFF
	Mixer-First RX with Passive Elliptic LPF	

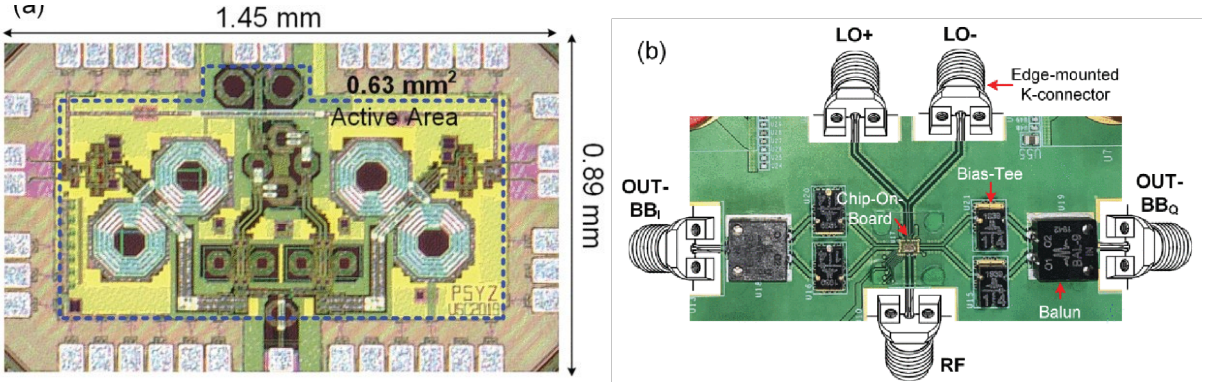
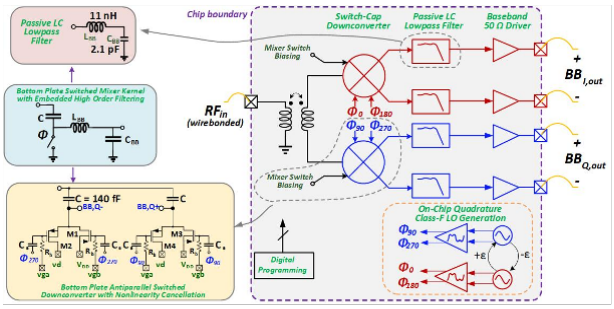
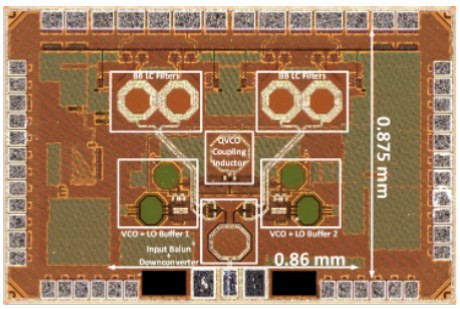


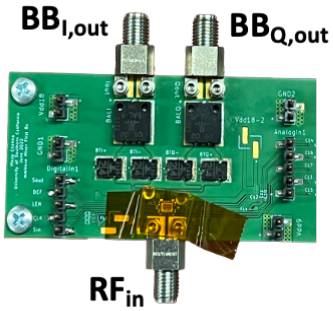
Figure 1. (a) Top Level Schematic Diagram of the mm-Wave Mixer First Receiver, (b) Measured Performance Summary, (c) Chip Photo, (d) Test Board Assembly for Connectorized Measurements

1.2 Improving the Linearity of mm-Wave N-Path Receivers

The objective of this effort was to improve the dynamic range of mm-Wave N-Path structures by attempting to resolve the key bottlenecks associated with high frequency switching structures, namely, switch linearity and LO generation. Towards this end, we proposed two key ideas: (a) Antiparallel nonlinearity cancellation of FET switches to improve switch linearity and, (b) Doubly tuned on-chip Class-F LO generation to generate flat switching waveforms at mm-Wave frequencies, to further increase the dynamic range. The chip was implemented in the TSMC 28nm CMOS technology and placed inside a cavity drawn within the printed circuit board (PCB) to shorten the wire-bonds at the mm-wave input. Furthermore, the wire-bonds at the inputs were designed to ideally resemble a 50 Ω CPW line using uniformly space ribbon bonds.







	Simulations	Measurements
Tuning Range (GHz)	24.5 – 29.6	23.4 – 27.0
BW_{BB} (GHz)	1.2	0.9
NF_{DSB} (dB)	< 11	TBD
Conversion Gain (dB)	-1	-12*
IIP3 (dBm)	> 21 (IB And OOB)	> 19 (In band)
Power Consumption (mW)	46	44.6

Figure 2. (a) Top Level Schematic Diagram of the mm-Wave Mixer First Receiver with Antiparallel Nonlinearity Cancelled Switches and Doubly Tuned LO, (b) Chip Photo, (c) Chip-on Board Assembly for Connectorized Measurements, (d) Measured Performance Table

We noticed a significantly lower conversion gain in measurements compared to simulation. We attribute this to the improperly assembled wire-bonds at the input and the output path on the PCB. We suspect that the wideband on-PCB baluns are loading the baseband drivers on chip in an unintended way.

Based on the measurement results described above, we are working on performing probed measurements at the input and the output to solve issues with conversion gain. Once the conversion gain issue is fixed, we will perform the noise figure measurements and redo the linearity measurements.

1.3 Non-Uniform Sub-Sampling Receiver Front-End Enabling Spectral Alias Spreading

This work introduces a non-uniform sub-sampling (NUSS) technique to relax the analog anti-aliasing filter design for mm-Wave receiver applications. By applying pre-designed periodic perturbation to the sub-sampling time instants, the unwanted spectral aliases, i.e., the integer multiples of the sampling frequency other than the carrier frequency, are spread out; hence undesired blockers aliasing at specific bands are significantly reduced. The NUSS technique effectively creates frequency notches during the sampling process that can be reconfigured simply by changing the NU perturbation sequence. A proof-of-concept NUSS receiver front-end is implemented in 28nm CMOS with 26.88 GHz carrier frequency [3]. Through spectral alias spreading, NUSS technique achieves 33 dB alias rejection with 29 mW power dissipation, which effectively creates notch filtering during sampling. The measured EVM is -25 dB using a 200 MHz 64-QAM modulated signal in the presence of a 0 dBc blocker.

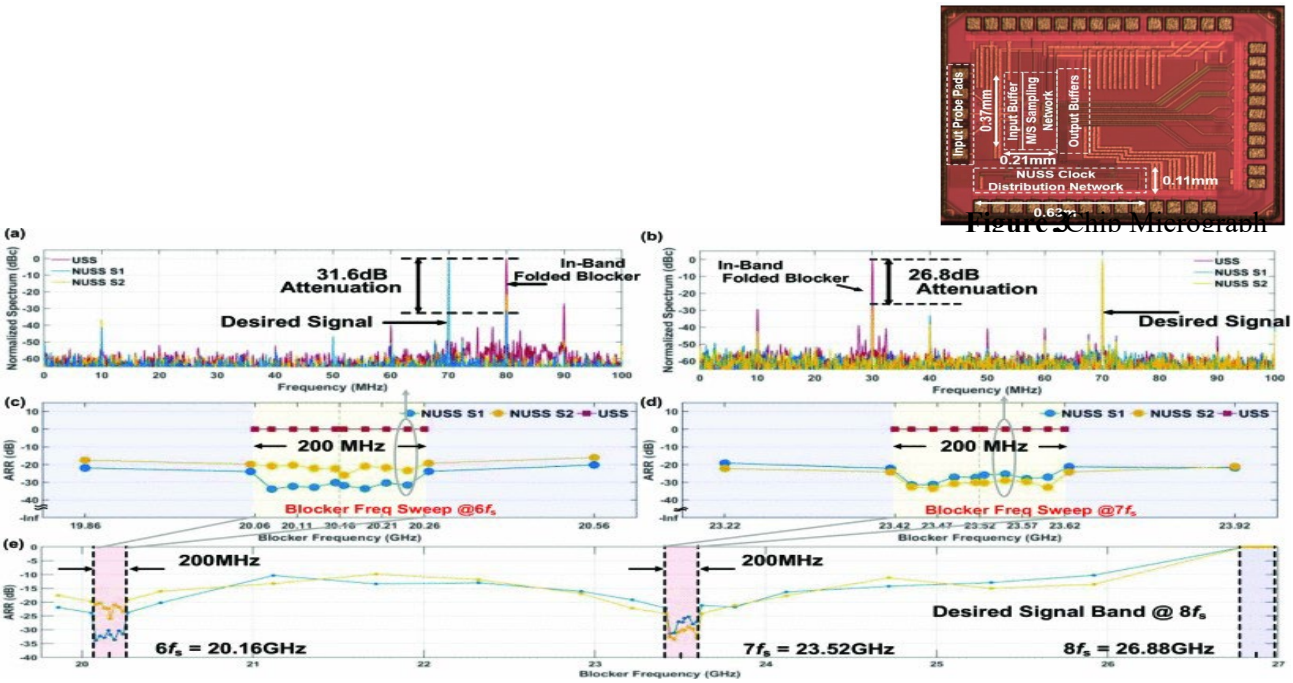


Figure 3. A Comparison of the Measured Spectra Using USS and NUSS for a Single-tone Input Signal (at 26.88GHz+70MHz) with a Single-Tone Blocker at Different Frequencies
(a) 20.16GHz (6fs) +80MHz; (b) 23.52GHz (7fs) +30MHz; (c) ARR(fBlk) around 20.16GHz (6fs); (d) ARR(fBlk) around 23.52GHz (7fs); and (e) ARR(fBlk) from 20 to 27GHz

Highlights:

1. The first non-uniform subsampling (NUSS) mm-Wave receiver front-end.
2. A novel sampling-embedded filtering technique (Spectral Alias Spreading).
3. The proposed blocker-tolerant front-end achieves 33 dB of alias blocker

1.4 Current-Mode Subharmonic Switching Digital Power Amplifier for Enhancing Power Back-Off Efficiency

This work proposes a current-mode subharmonic switching (SHS) power amplifier (PA) architecture to reduce conduction loss and minimize output impedance variation by toggling more PA branches at subharmonic frequencies in the power backoff (PBO) region. The proof-of-concept prototype achieves 27dBm peak output power at 5.7GHz and 40.1% drain efficiency at 5.4GHz [4]. The implementation leverages a proposed coupledinductor-based subharmonic trap to derive the optimal load impedance at the carrier frequency (f_c) and high impedance at the subharmonic frequency ($f_c/3$), and magnetic field cancellation for improved common-mode rejection. Due to the current-mode SHS operation, the efficiency peak at -9dB PBO is 29.2% at 5.4 GHz, which is a 2× improvement over that of the conventional current-mode digital PA. The real-time SHS operation achieves more than 28% average efficiency with 20/40/80MHz modulation signals.

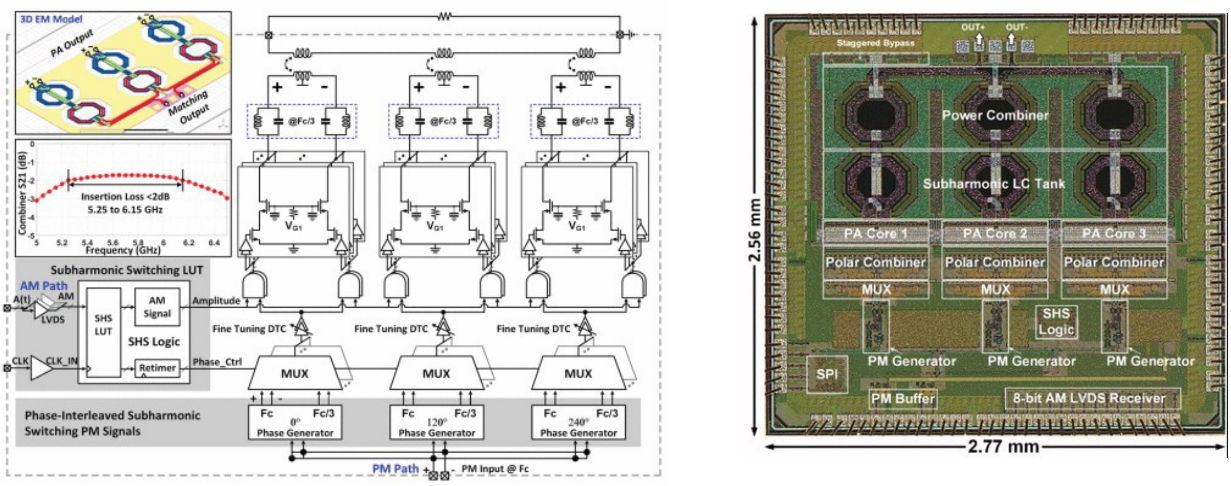


Figure 4. Schematic and Chip Photo of the Subharmonic Switching RF Power Amplifier

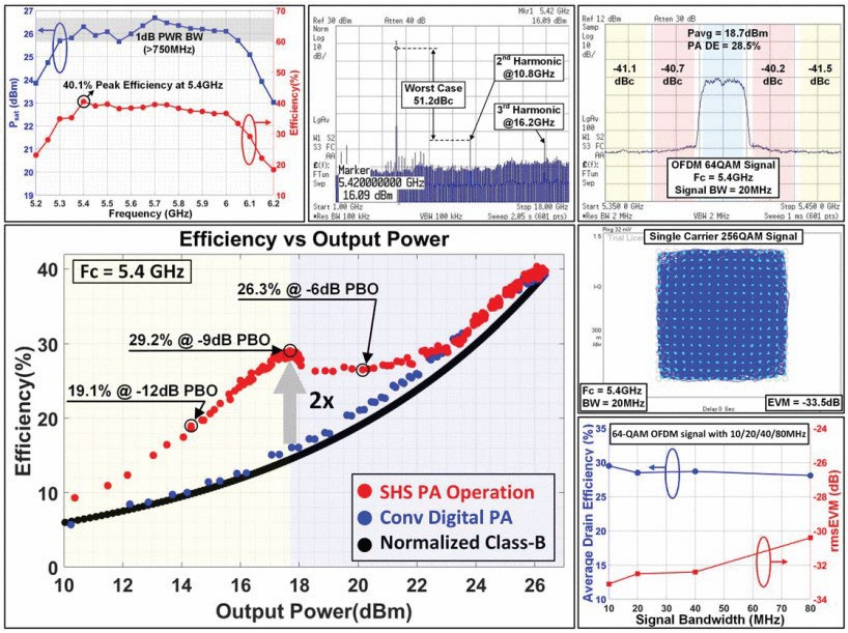


Figure 5. Representative Measurement Results

1.5 Concurrent Harmonic and Subharmonic Tuning Class E/F2,2/3 Subharmonic Switching Power Amplifier Achieving Peak/PBO Efficiency Enhancement

This work proposes a concurrent harmonic and subharmonic tuning Class E/F 2,2/3 SHS PA for mm-wave operation that: 1) utilizes both harmonic and subharmonic tuning to reduce I/V overlap (i.e., conduction loss) for both peak and PBO operation and 2) allows the PA cells to toggle at a much lower frequency (i.e., subharmonic frequency) in PBO, which facilitates square switching waveform and reduces the loss of highfrequency clock routing. At the circuit level, we propose an on-chip concurrent harmonic and subharmonic tuning matching network that can simultaneously provide optimal load impedance of the fundamental (f_c), 2nd harmonic ($2f_c$), subharmonic ($f_c/3$), and 2nd harmonic of the subharmonic ($2f_c/3$) with a compact footprint without involving any tunable switches and elements. The proof-of-concept prototype achieves 40.5% PAE at Psat and 24% PAE at -9 dB PBO. It largely enhanced deep PBO efficiency enhancement at mm-wave frequency bands [5].

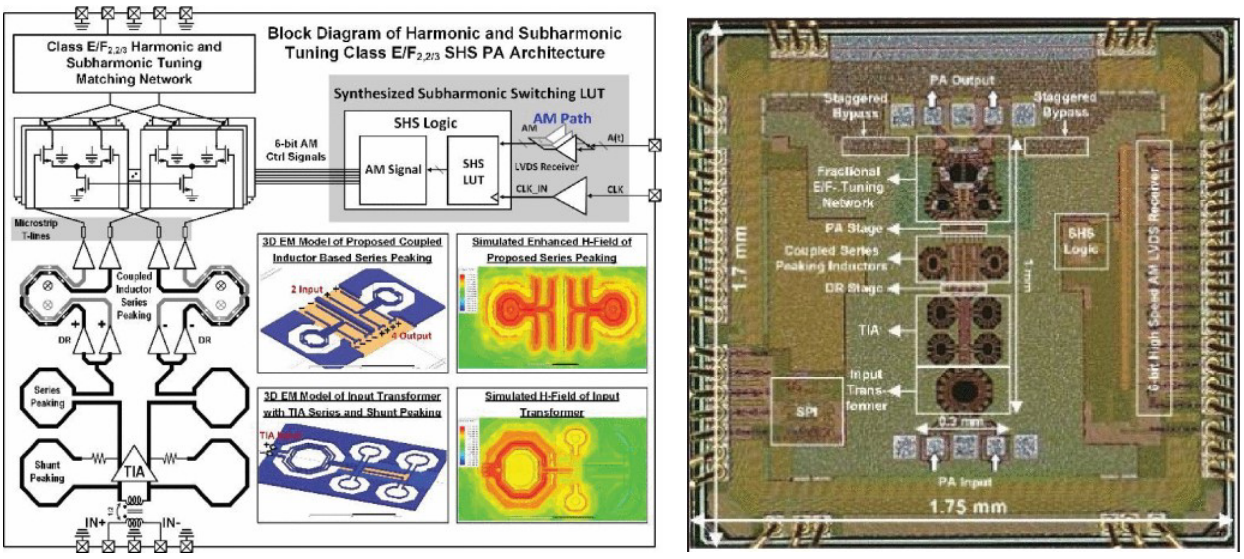


Figure 6. Schematic and Chip Photo of the Subharmonic Switching mm-wave Power Amplifier

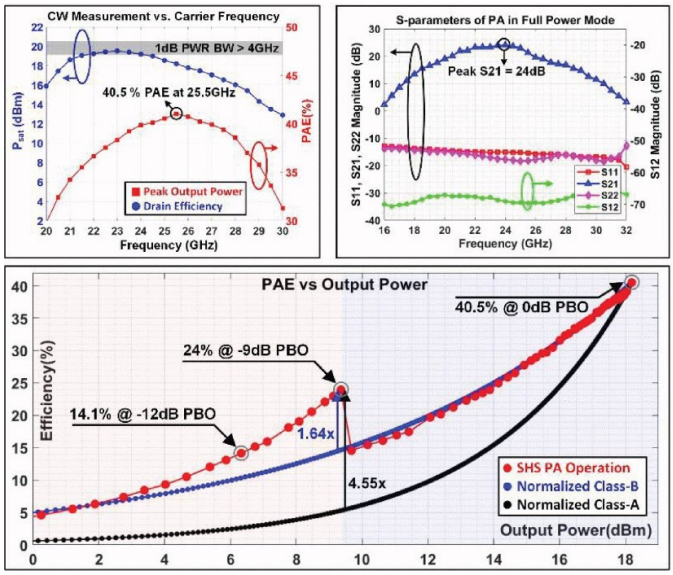


Figure 7. Representative Measurement Results

1.6 Non-Uniform Time Approximation Filter (NU-TAF) mm-Wave Receiver

This work presents a non-uniform (NU) time-approximation filter (TAF) technique for a wireless receiver (RX) to reject unwanted blockers. The proposed NU TAF leverages the alias-spreading property of NU sampling (NUS) and a TAF that approximates a finite impulse response (FIR) filter response in the time domain, achieving an overall flexible filter response with a higher attenuation factor. The filter response can be readily reconfigured by changing the NU sequence and/or the TAF waveform without adjusting the passive component value. A proof-of-concept millimeter-wave RX is implemented in the 28-nm CMOS process and achieves > 45-dB blocker rejection with a 33.7-GHz carrier frequency [6][7]. The EVM measures − 30.9 dB using a 100-MSymbol/s 64QAM signal in the presence of a 10-dBc out-of-band (OOB) blocker.

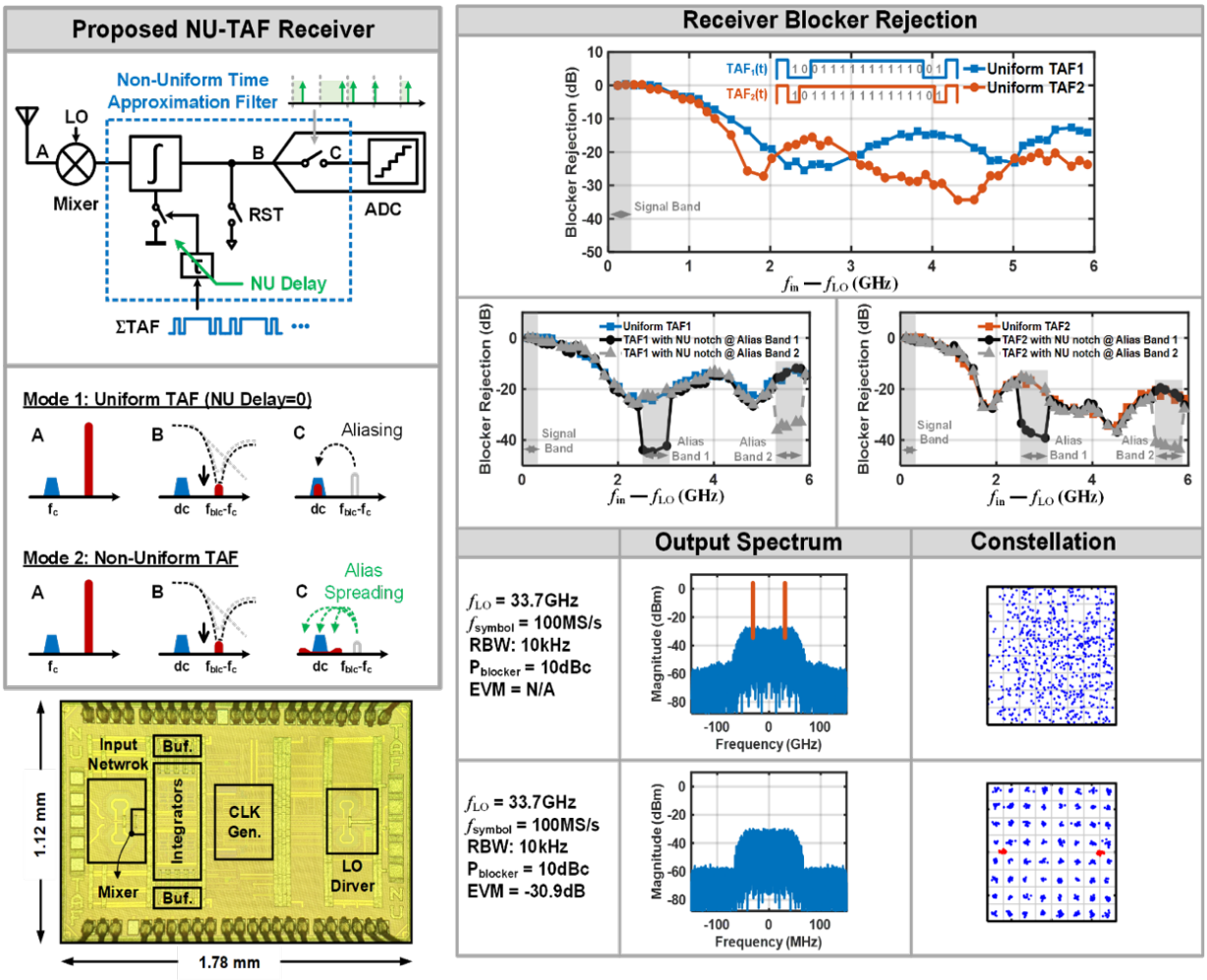


Figure 8. (a) The Proposed nu-taf Architecture and Operation Principle (b) Measured Receiver Blocker Rejection and Measured Spectra and Constellations at 64 QAM: Blocker Test with NU-TAF OFF and ON. (c) Chip Microphotograph

1.7 Non-Uniform Sub-Sampling mm-Wave Receiver with Non-Uniform DiscreteTime FIR Filtering

This work presents a mm-wave non-uniform subsampling receiver architecture featuring a non-uniform discrete-time filter that creates tunable frequency notches via judiciously designed non-uniform filter taps and attenuates both in-band and OOB blocker aliases hence, acting as a decimation filter to relax the subsequent ADC speed and dynamic range. The design incorporates a current-mode NU-DT FIR filter that re-uses the capacitive DAC of the subsequent SAR ADC and forms S/H network. It attenuates OOB blocker aliases, relaxing the subsequent ADC speed by 8X and dynamic range by 4X. A proof-of-concept prototype achieves 39 dB of blocker rejection with the worst-case B_{1dB} of -2.7 dB and measures -27.4 dB EVM for a 100 MS/s 64-QAM signal centered at 20 GHz. The results of this work will be published soon.

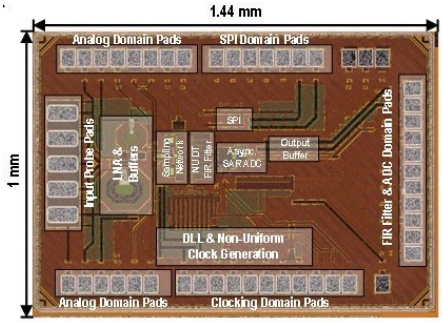


Figure 9. Chip Micrograph

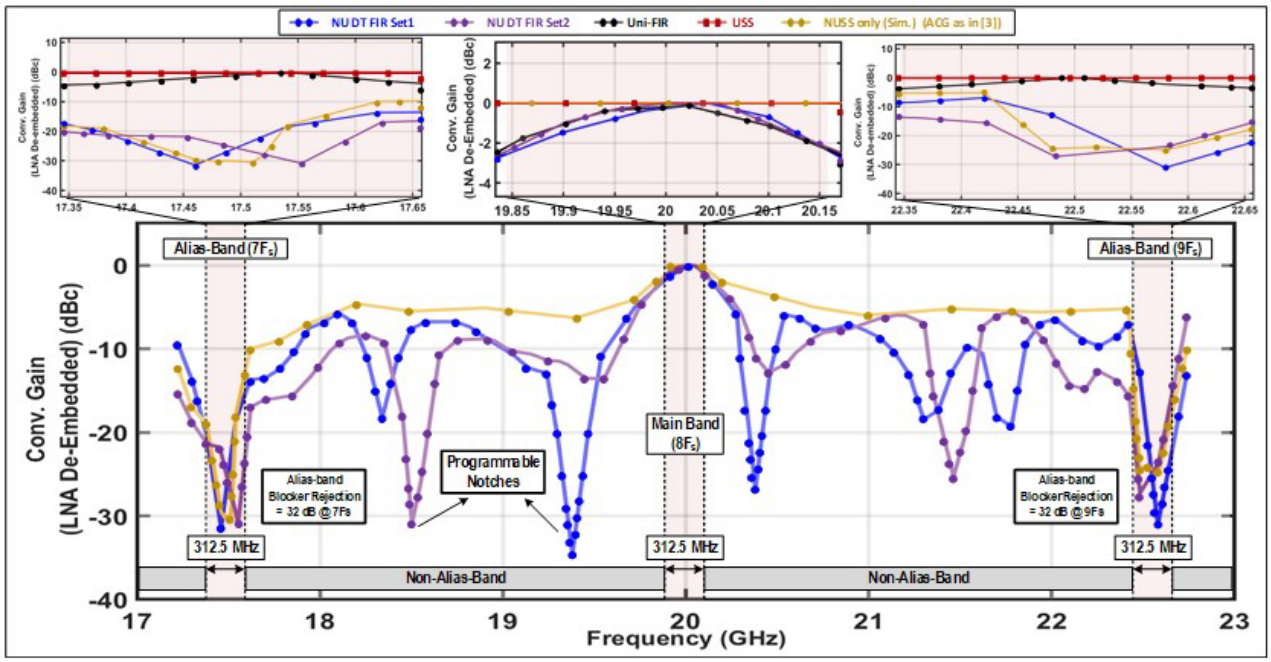


Figure 10. Measured Frequency Response for the NU DT FIR with Different Coefficient-Sets Showing Alias-bands Rejection and Non-alias Bands Programmable Notches
LNA gain is de-embedded, all points are measured after decimation

1.8 A SAW-Less Direct-Digital RF Modulator with Tri-Level Time-Approximation Filter and Reconfigurable Dual-Band Delta-Sigma Modulation

This work proposes a reconfigurable direct digital RF modulator architecture which is capable of high in-band dynamic range and/or low OOB noise floor at desired frequencies. A hybrid DAC with reconfigurable dual-band delta-sigma modulator (DSM) is used that can create in-band and/or out-of-band (OOB) spectral notches to support different communication scenarios. A tunable tri-level time-approximation filter (TAF) that further suppresses OOB noise to achieve higher reconfigurability and stopband attenuation than existing TAFs without increasing time resolution. A proof-of-concept prototype in 65nm CMOS, achieves -40 dB EVM and -169 dBc/Hz NSD at 68 MHz offset using a 17.4 dBm 256-QAM signal at 2.2 GHz carrier [8][9].

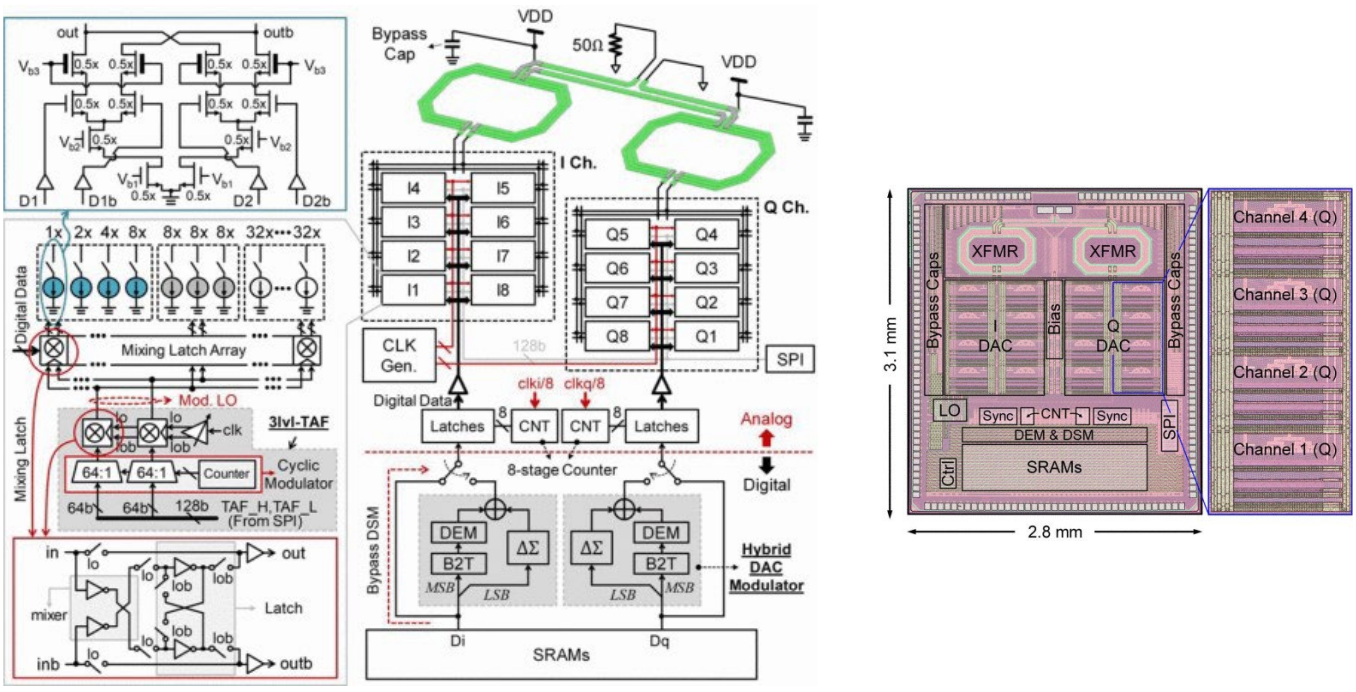


Figure 11. Schematic and Chip Micrograph

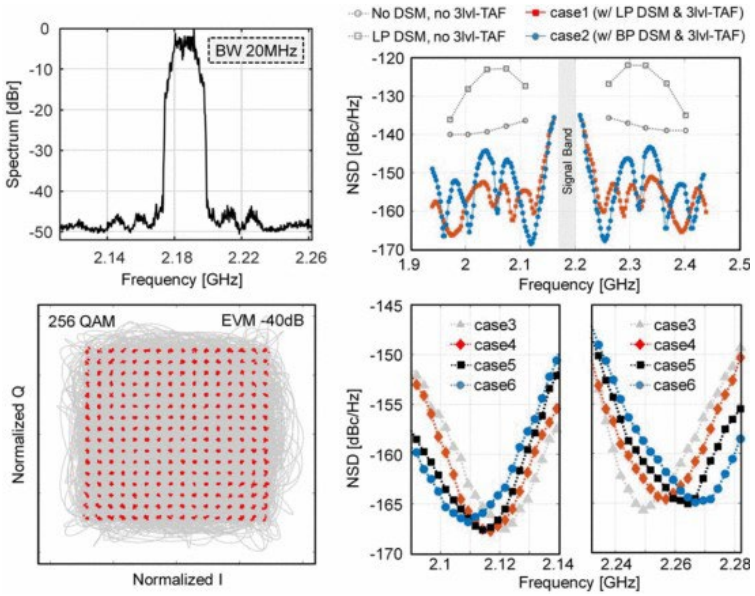


Figure 12. Measured Spectrum, Constellation, and NSD

1.9 Mm-Wave Subharmonic Switching I/Q Digital PA

This work proposes a mm-wave wideband quadrature digital power amplifier that leverages the sub-harmonic switching technique for enhancing the power-back efficiency, employs multi-phase I/Q summation for improving the peak efficiency and achieves in-band noise shaping by incorporating a hybrid delta-sigma modulator DAC. Time-approximation fltering aids in attenuation of the sub-harmonic component arising from SHS operation. Although polar digital PAs can achieve higher peak efficiency, they can only support narrowband signals owing to their

inherent bandwidth extension during modulation. Hence, their applicability at the mmWave band is limited which calls for quadrature digital PA architecture that doesn't suffer from this issue and hence, is a suitable choice for wideband applications. Based on simulation results, this PA achieves a peak power of 20.2 dBm with a peak efficiency of 33% and average efficiency of 20% for 400-MHz OFDM input. We plan to fabricate this chip and report the results in peer-reviewed publications.

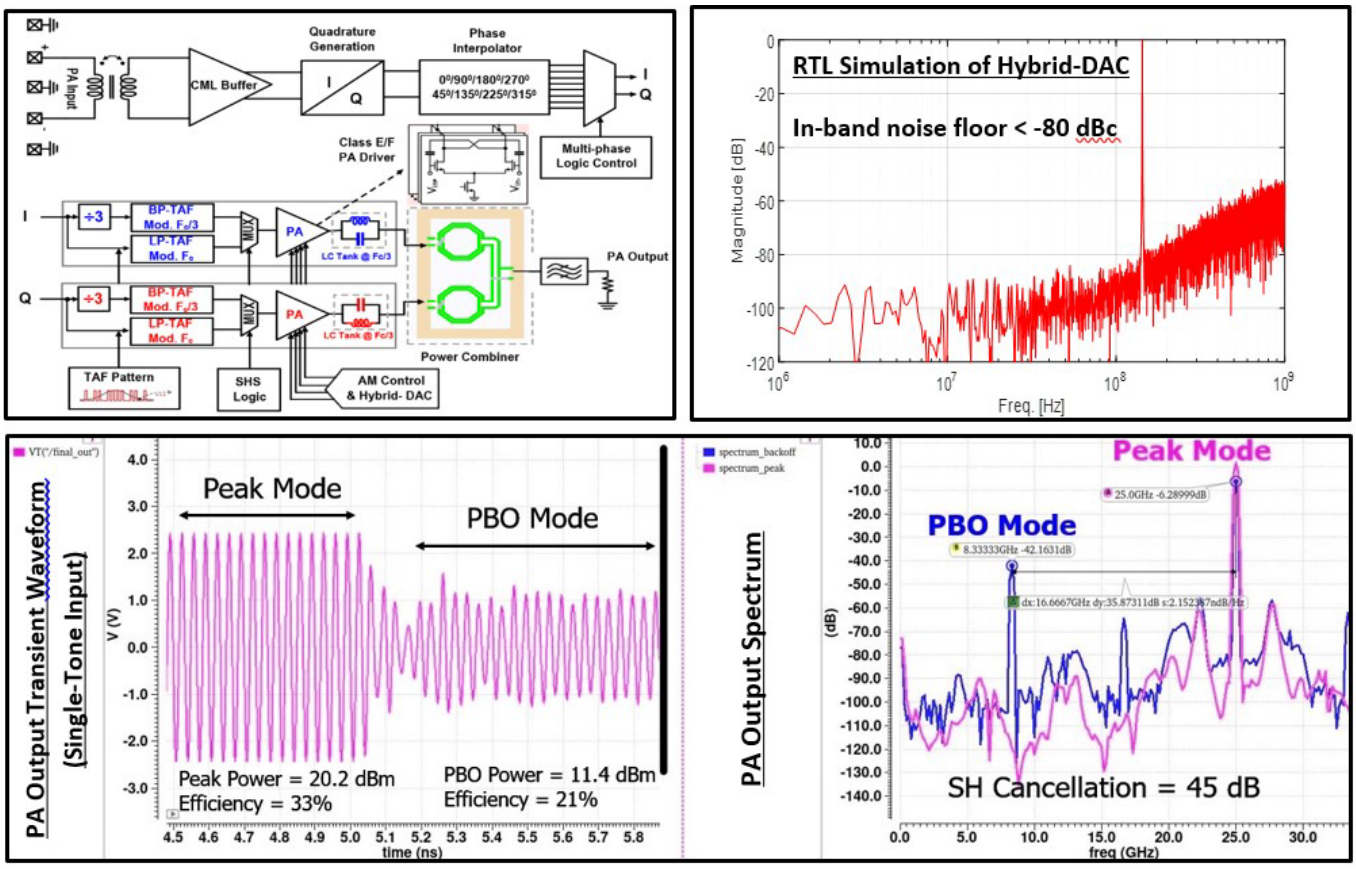


Figure 13. (a) Circuit Implementation. (b) Hybrid DAC Output Spectrum. (c) PA Transient Waveforms for Peak Mode and PBO mode. (d) PA Output Spectrum for Peak Mode and PBO Mode

2 PUBLICATIONS

[1] P. Song and H. Hashemi, “mm-wave mixer-first receiver with passive elliptic low-pass filter,” in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)* Digest, 2020.

[2] P. Song and H. Hashemi, “mm-wave mixer-first receiver with selective passive wideband low-pass filtering,” *IEEE Journal of Solid-State Circuits*, vol. 56, no. 5, pp. 1454-1463, May 2021.

[3] C. Yang, M. Ayesh, A. Zhang, T. -F. Wu and M. S. -W. Chen, "A 29-mW 26.88-GHz Non-Uniform Sub-Sampling Receiver Front-End Enabling Spectral Alias Spreading," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)* Digest, Los Angeles, CA, USA, 2020, pp. 87-90.

[4] A. Zhang, C. Yang, M. Ayesh and M. S. -W. Chen, "26.6 A 5-to-6GHz Current-Mode Subharmonic Switching Digital Power Amplifier for Enhancing Power Back-Off Efficiency," 2021 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA, 2021, pp. 364-366.

[5] A. Zhang, M. Ayesh, S. Mahapatra and M. S. -W. Chen, "A 24-28 GHz Concurrent Harmonic and Subharmonic Tuning Class E/F2,2/3 Subharmonic Switching Power Amplifier Achieving Peak/PBO Efficiency Enhancement," 2021 IEEE Custom Integrated Circuits Conference (CICC), Austin, TX, USA, 2021, pp. 1-2.

[6] C. Yang, S. Su and M. S. -W. Chen, "A Millimeter-Wave Mixer-First Receiver with Non-Uniform TimeApproximation Filter Achieving > 45dB Blocker Rejection," 2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Denver, CO, USA, 2022, pp. 3-6.

[7] C. Yang, S. Su and M. S. -W. Chen, "Millimeter-Wave Receiver With Non-Uniform Time-Approximation Filter," in IEEE Journal of Solid-State Circuits, 2023 (early access).

[8] S. Su and M. S. -W. Chen, "10.2 A SAW-Less Direct-Digital RF Modulator with Tri-Level Time-Approximation Filter and Reconfigurable Dual-Band Delta-Sigma Modulation," 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 174-176.

[9] S. Su and M. S. -W. Chen, "SAW-Less Direct RF Transmitter With Multimode Noise Shaping and Tri-Level Time-Approximation Filter," in IEEE Journal of Solid-State Circuits, vol. 57, no. 3, pp. 906-916, March 2022.

LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS

ACRONYM	DESCRIPTION
DSM	Delta-Sigma Modulator
FIR	Finite Impulse Response
LNA	Low-Noise Amplifier
LPF	Low-Pass Filter
NF	Noise Figure
NU	Non-Uniform
NUSS	Non-Uniform Sub-Sampling
OOB	Out-of-Band
PA	Power Amplifier
PCB	Printed Circuit Board
RX	Receiver
SHS	Subharmonic Switching
SSB	Single-Sideband
TAF	Time-Approximation Filter
USC	University of Southern California