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BROADBAND CONTINUOUS TIME DELTA SIGMA MODULATORS FOR MILLIMETER WAVE DIGITAL ARRAYS

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University of Michigan

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14. ABSTRACT

A fully integrated mm-wave, 16-element, 4-beam digital beamformer with 100MHz bandwidth was implemented in 40nm CMOS technology. In addition, a four-tile system with a custom substrate supports four chiplets. The four-chiplet substrate includes sixty-four 28GHz patch antennas and the power and digital infrastructure to support the chiplets. Furthermore, this work tackles the design of the frequency-offset bandpass modulators and introduces simple filters to efficiently suppress out-of-band quantization noise before combining modulator outputs. A proof-of-concept 2x frequency interleaved prototype doubles the conversion bandwidth with only a 3% power consumption overhead for the additional digital filtering circuity.

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digital beamforming, wireless, ADC, chiplet, packaging, phased array, antenna

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1 28GHZ 16-ELEMENT DIGITAL BEAMFORMER

We developed and demonstrated a fully integrated mm-wave, 16-element, 4-beam digital beamformer with 100MHz bandwidth implemented in 40nm CMOS technology. The IC employs bandpass ADCs plus bitstream processing (BSP) to reduce the power dissipation and silicon die area of digital beamforming. BSP saves power and area by implementing complex digital multiplication with simple multiplexers and reducing the number of decimators from the number of channels to the number of beams.

Fig. 1 shows the architecture for the prototype 28GHz single-tile digital beamformer IC. An RF frontend connects directly to the antenna array and amplifies and down-converts the received signal. Down-conversion is from 28GHz to the 1GHz center frequency of the IF beamformer. Each of the sixteen receive chains consists of a noise-cancelling single-ended-to-differential LNA, passive mixer, variable gain amplifier (VGA), and four bandpass CTDSM ADCs.

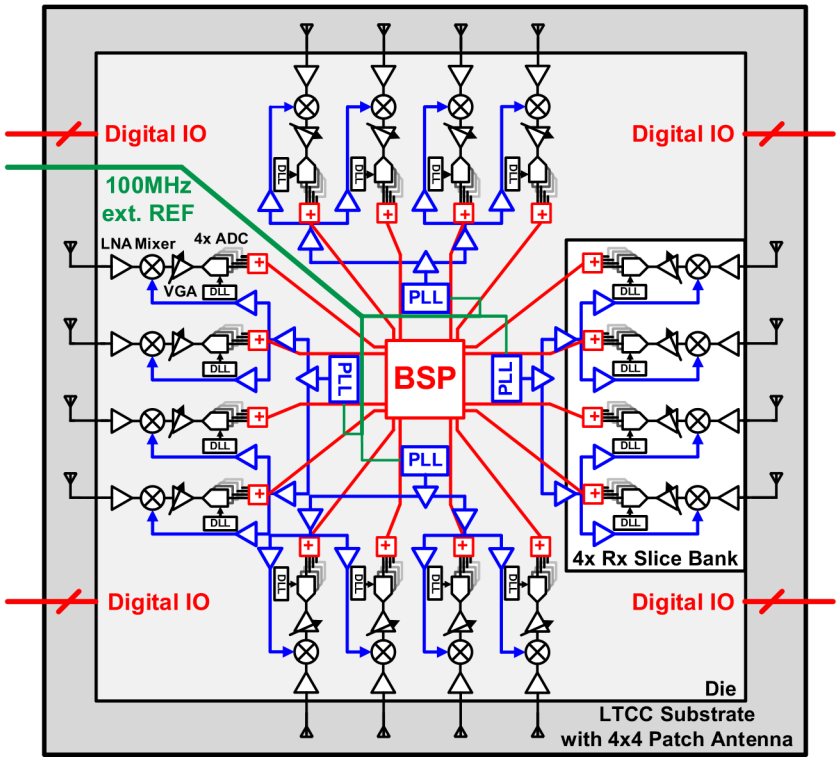

Fig. 1. Architecture of the 28GHz 16-Element Digital Beamformer IC

The LNA and mixer are broadband to avoid modeling issues and process variation, which might affect a narrowband design. Four 27GHz PLLs provide the LO for the down-conversion mixer. The use of four PLLs greatly simplifies LO routing on-chip. For this design, we use an integer-N PLL for simplicity and low-phase noise. The variable gain amplifier is digitally programmable via an SPI bus and directly drives the input of the ADC.

An array of four CTBPDSM sub-ADCs converts the IF signal to a 5-bit digital bitstream. The bandpass modulator samples the IF signal directly, moving I/Q mixing to the digital domain. Compared to analog I/Q mixing, digital I/Q mixing halves the power consumption and eliminates mismatch in the I/Q LO signals. The four sub-ADCs, clocked by four 90°-separated 4 GHz clock phases, implement four-phase sampling, cancelling the third harmonic in the ADC output and improving the HD3 by 9dB. The use of an oversampling architecture with short output bit-width allows for the area and power efficient BSP approach to the digital beamforming computation. The BSP in the digital core at the center of the chip generates four full beams of 250Mbps 12-bit data from the sixteen 4Gbps 5-bit ADC channel outputs.

The 16-element digital beamformer IC was fabricated in 40nm CMOS and measures 2.8mm x 2.8mm. The die is flip chip mounted on an 8-layer low-temperature ceramic substrate with a 4x4 array of patch antennas (Fig. 2). The top of the substrate has the 4x4 array of aperture-coupled microstrip patch antennas with a single-stub matching network. The patch antennas measure 3.6mm x 1.8mm with a 4.5mm pitch and a 300µm dielectric thickness. On the backside of the substrate, the die is flip chip mounted to bumps in the center of the substrate and a variable gain amplifier (VGA) around the perimeter mounts the substrate to the test PCB.

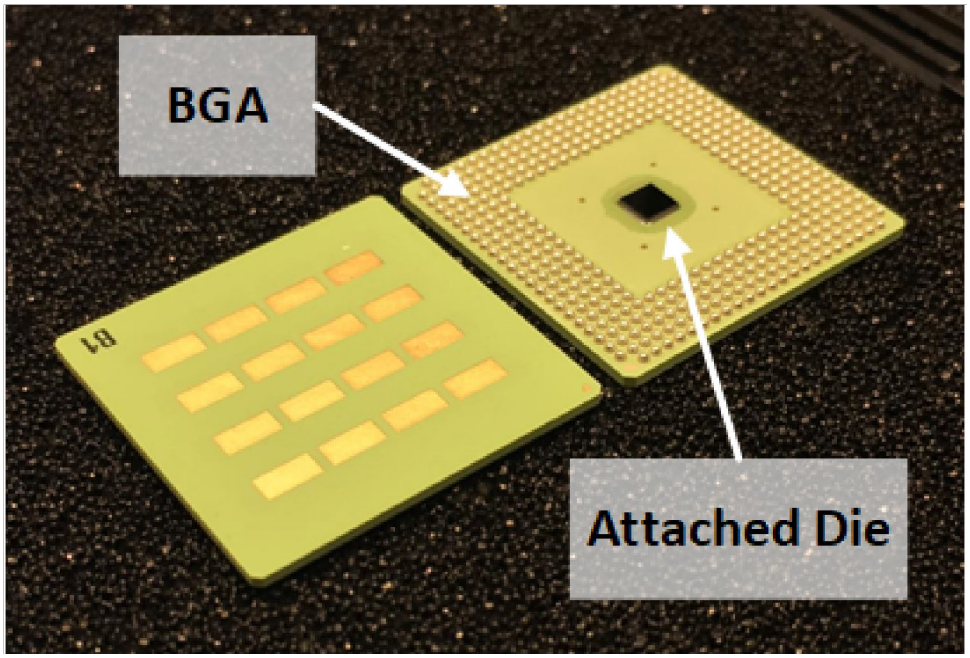

Fig. 2. Assembled Substrate

The sixteen-element beamforming array is BGA-mounted on the daughterboard, which in turn connects to a motherboard. The stack of PCBs provides power, programmable biasing references, reference clocks, and an SPI interface (Fig. 3).

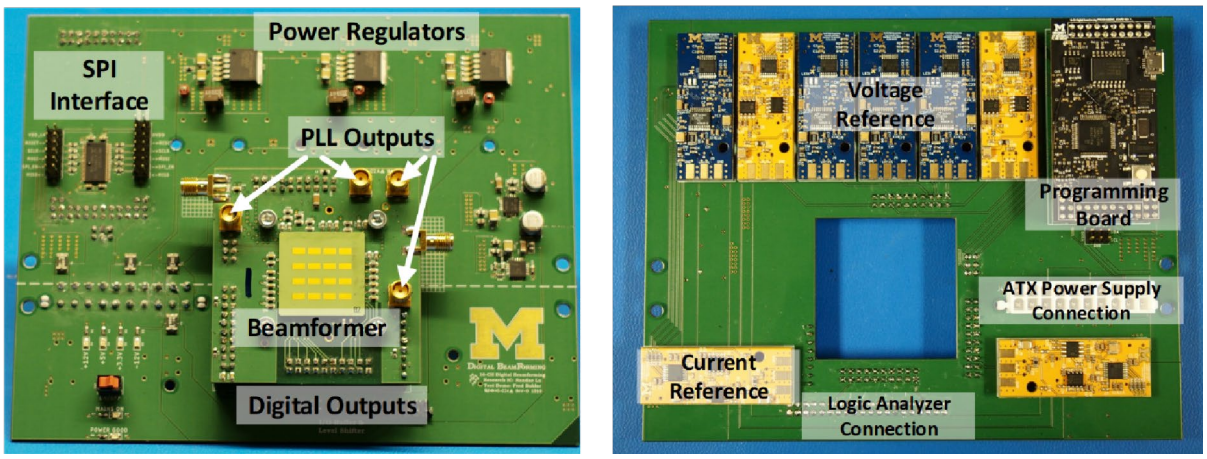

Fig. 3. Assembled Beamformer Mounted on PCB Stackup

The measurements were taken over-the-air in a 28GHz anechoic chamber (Fig. 4). A 28 GHz signal source is configured by the PC and its signal routed to a 28GHz horn antenna mounted on a wood and LEGO holder in the chamber. The motorized test fixture holds the stack of PCBs supporting the sixteen element array. A Raspberry Pi controls the servo motors in the test fixture, and an FPGA with a USB interface controls the SPI configuration of the chip. A logic analyzer reads the 12-bit 250Mbps digital data from the beamformer.

Fig. 4. Over-the-Air Measurement TEST SEtup

The 3-dimensional beampatterns were measured over-the-air using the setup shown above. The resulting 3D beampatterns when the beam is steered at boresight and at 15°/-15° ae shown in Fig. 5. The measured beampatterns closely match the ideal, simulated beampatterns.

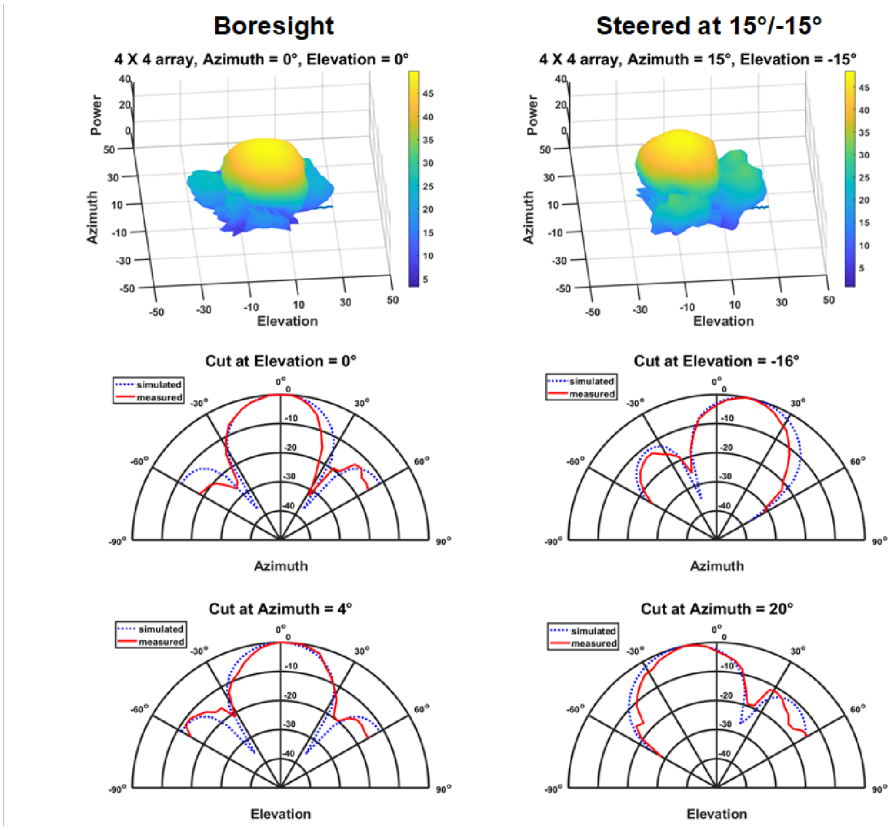

Fig. 5. Beampattern Measurements for a Beam Steered at 0°/0° (left) and 15°/-15° (right)

Fig. 6 shows the constellation diagram for the QAM4 over-the-air measurements. With a data rate of 5Mb/s, the measured EVM was -18-dB. Performance limitations in this measurement were from reflections between the horn antenna and the beamformer, which were placed more closely in this test, and from phase noise from pulling between the four on-chip PLLs.

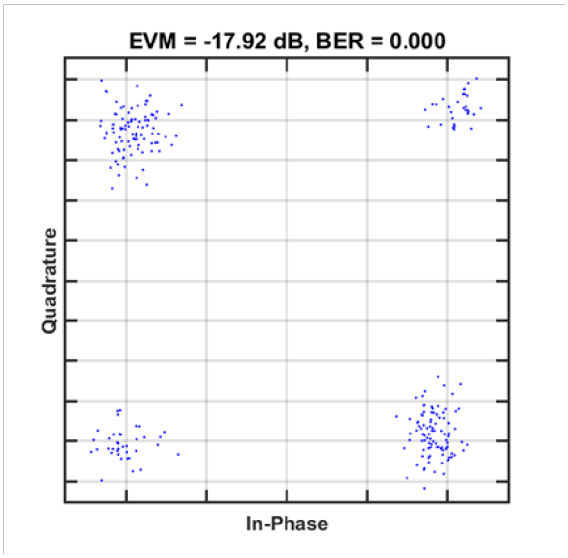

Fig. 6. QAM 4 Constellation Diagram

2 28GHZ 64-ELEMENT, MULTI-CHIP DIGITAL BEAMFORMER

In this phase, we significantly expanded the number of elements with a tileable, chiplet-based approach. In addition, we developed a four-tile system with a custom substrate supporting four chiplets. The four-chiplet substrate includes sixty-four 28GHz patch antennas and the power and digital infrastructure to support the chiplets.

Fig. 7 shows the tiling architecture we implemented for the multi-chip beamformer. To minimize lengthy routing on both the substrate and the PCB, each die passes its data to the next die in a spiral shape with each die rotating 90° relative to the previous die in the spiral. The combination of a spiral tiling geometry and diagonal I/O placement aligns the TX/RX pins between chips, allowing each chip to use the same I/O. To equalize computational load, we implement a distributed processing architecture that splits the beamforming processing between chiplets. Each chiplet accepts a partially processed beam from an adjacent chiplet and adds the phase-shifted signals for its channels. In turn, this partial beam is passed to the next chiplet and so on. This tiling architecture equally distributes the computational load throughout the array and is expandable to larger arrays at a small latency cost.

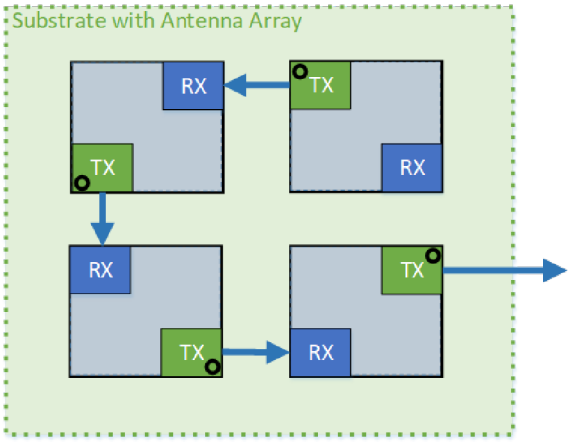

Fig. 7. Tiling Architecture between Chiplets

Each chiplet supports sixteen mm-wave frontends, 32 bandpass CTDSM ADCs, a 27 GHz PLL, LO distribution network, digital beamforming processing, digital clock generation, multi-chip clock synchronization, and digital chip-to-chip data communication. To conserve power across the larger, tiled array, this design uses two bandpass CTDSM ADCs per channel instead of the four used in the previous phase's work. The ADCs can be configured to turn on one or the other, for a low-power mode with redundancy, or to turn both ADCs on for a higher-performance mode with sampling frequency suppression. A single 27GHz Type II PLL is used to simplify calibration of PLLs in the larger array and to mitigate the pulling seen between the four PLLs in the previous version.

To implement the spiral tiling architecture described above, we designed a chiplet-to-chiplet digital communication interface as well as multi-chip clock synchronization. The digital communication interface between the chiplets consists of a 13-bit wide, 1Gbps digital bus

with the 1GHz data clock forwarded source synchronous with the data. A 1Gbps parallel bus achieves a good tradeoff between the power efficiency of a wide, parallel bus and routing limitations with the standard 162µm pitch bumps. Serializing the 250Mbps beam data allows four sets of data to be transmitted simultaneously with a configurable choice of two full quadrature beams or four half beams. A 250MHz clock forwarded as part of the multi-chip clock synchronization design is used to identify the starting transition of the data packet.

To synchronize the clocks between the four chips, a digital PLL measures the phase difference between forwarded and loopback 250MHz divided clocks. Adjusting the clock phase synchronizes the clock phase between chiplets, which in turn synchronizes the beamforming processing across chiplets.

The tileable, 16-element digital beamformer was fabricated in 40nm CMOS and measures 2.8mm x 2.8mm. Fig. 8 shows the assembled substrates for the prototype four-chip, 64-element 28GHz digital beamforming array. Four CMOS dies are flip-chip mounted on the backside of a 15-layer LTCC substrate. The four dies are positioned in the centers of the four 16-element quadrants of the 64-element array, minimizing the 28GHz RF routing distance from the antenna elements to the chips' RF inputs. The top side of the LTCC substrate is an 8x8 element array of 28GHz patch antennas.

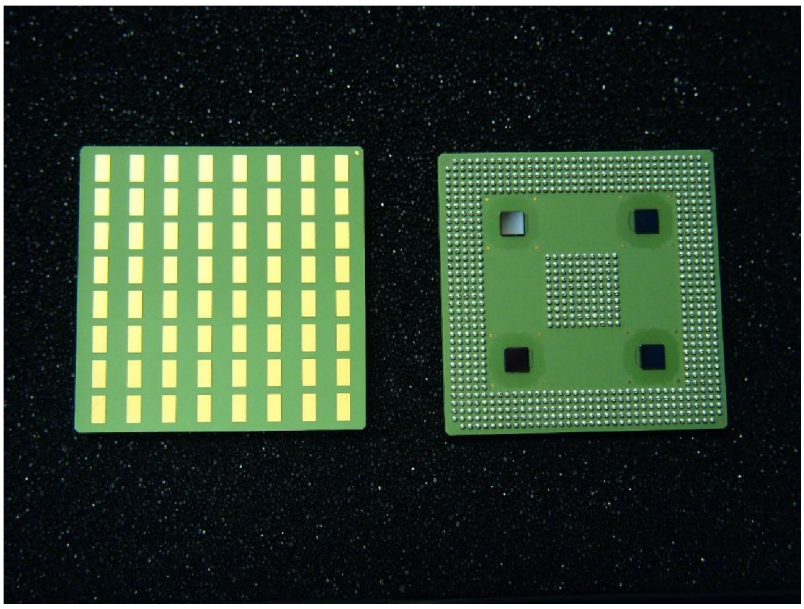

Fig. 8. Assembled Substrate with Four Chiplets
The substrate incorporates 64 28GHz antennas.

This substrate is BGA-mounted on a board that supplies power, biasing, and a reference clock to the substrate (Fig. 9). To read the 1Gbps data from the final chip, we designed a logic analyzer function for a Xilinx Ultrascale FPGA board. To minimize PCB routing distance between the beamforming array and the FPGA, we mount an Opal Kelly FPGA module onto the daughterboard with the beamforming array.

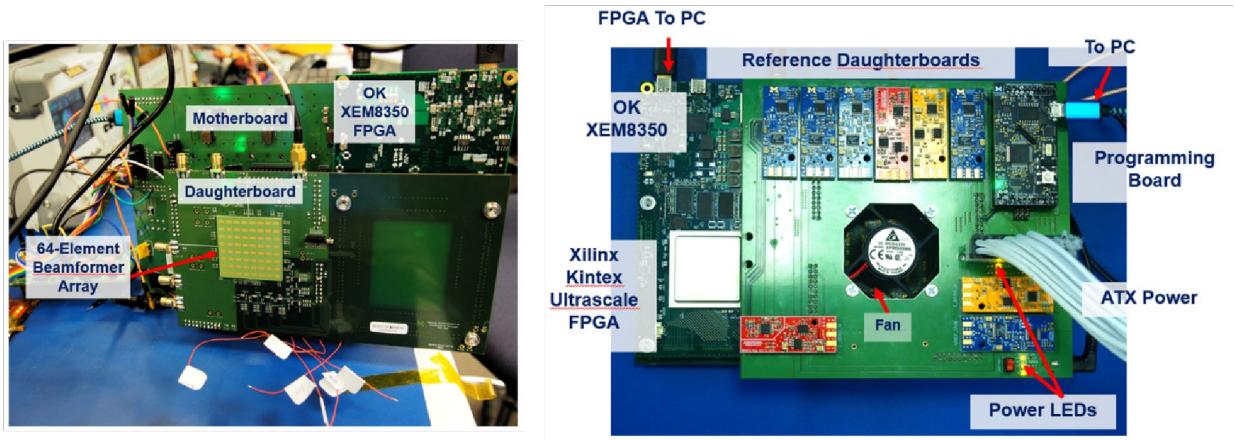

Fig. 9. Assembled Substrate on Support Boards

An initial version of this chip was taped out in May of 2021 and showed promising results. All systems on the chip powered up and were functional. However, the observed amplitude of the received signals was smaller than expected due to reduced LO distribution amplitude, digital timing skew, and low digital gain from using only 1x sub-ADC per channel.

A second version, taped out in September of 2022, improved the LO amplitude by using CML buffers in the first two stages of the LO distribution. This new version reduced digital timing skew between bit lines by optimizing manual routing of the digital I/O from the core to pad, instead of partially APRed routing the bit lines. Additionally, we expanded features and test modes to improve the calibration of the digital I/O, implemented a high-performance ADC mode with 2x sub-ADCs per channel, and added a TDC-based process monitor for calibration. An auxiliary boost path was added to the digital I/O output buffer so we can eliminate the external buffer chip when driving the high-capacitance FPGA input. This version also added a tri-state buffer to the SPI MISO to allow sharing of a multi-chip MISO line and improve SPI readback reliability.

Board assembly for the second version was completed in mid-February 2023. At the time of writing, we have finished power-up testing of the assembled system. Several functions have been verified. The SPI interface and control registers work well. The four 27GHz PLLs power up, operate, and lock (Fig. 10). Under control of the SPI interface, we also powered up different numbers of ADCs and measured the power consumption. As expected, power increases linearly with the number of ADCs (Fig. 11). Furthermore, the incremental increase in power consumption matches the simulated ADC power consumption. This measurement verifies bias and power distribution and suggests the correct operation of the ADCs. Digital data from the ADCs verifies the digital I/O interface, mm-wave front end, LO distribution, and ADC functionality. Fig. 12 shows an initial result from a full chain mm-wave to digital test for a single channel. The signal amplitude is close to what we expect for a single channel, and we can see evidence of noise-shaping from the ADC. Further SNDR improvement is expected with further ADC calibration. We are continuing chip bring-up, calibration, and beampattern testing to measure the chip's performance.

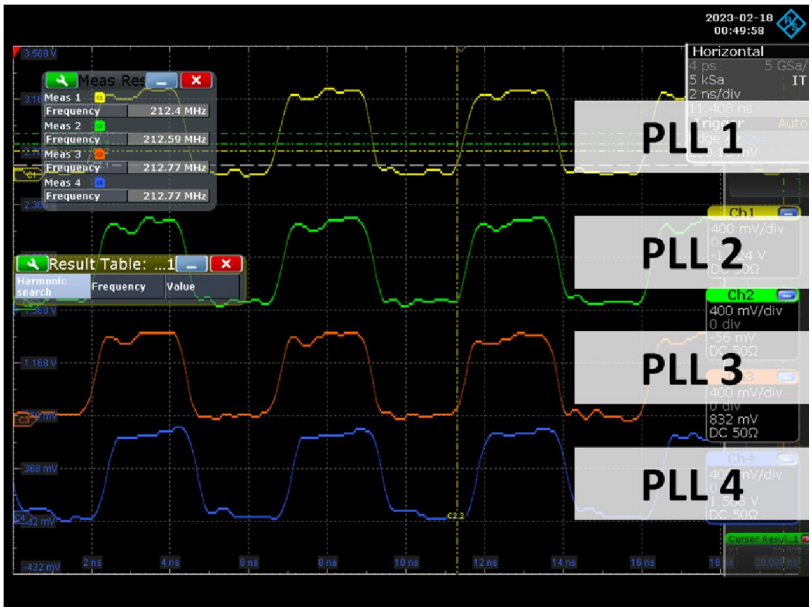

Fig. 10. Four LO PLLs Locking to the Same External Reference

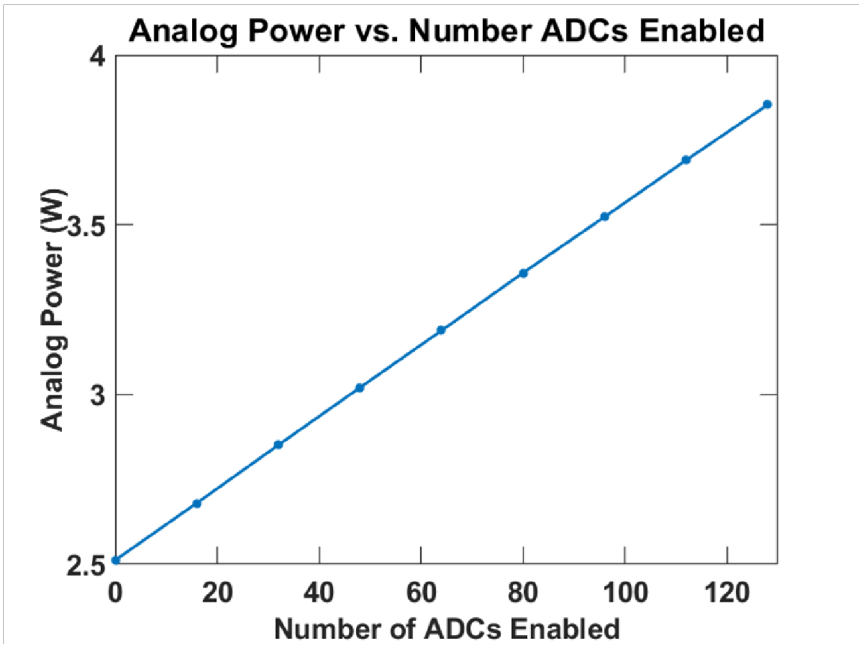

Fig. 11. Power Consumption Increases Linearly with Number of ADCs Enabled
This measurement is for all four chiplets assembled on the substrate and indicates correct biasing and power distribution to the mixed-signal circuitry.

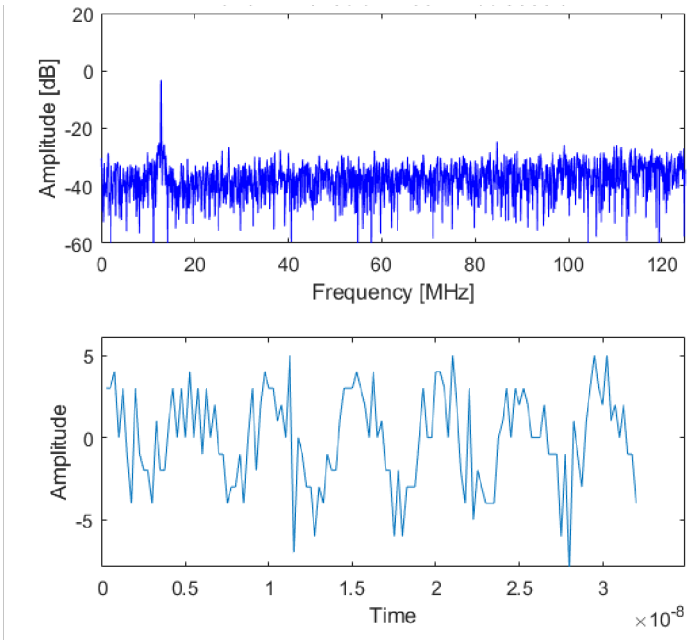

Fig. 12. mm-wave to Digital Measurement for One Channel in Frequency Domain (top) and Time Domain (bottom)

3 A DIRECT FREQUENCY-INTERLEAVING CONTINUOUS-TIME BANDPASS DELTA-SIGMA ADC

Wideband analog-to-digital converters are essential for emerging wireless communication schemes such as 5G and 6G. Time-Interleaving is a crucial tool for scaling the bandwidth of Nyquist analog to digital converters. However, noise-shaping and especially continuous time DSMs are very attractive for wireless communication systems but generally are not amenable to time interleaving. Critical advantages of continuous time DSMs include an easy-to-drive input, reduced need for anti-alias filtering, and suitability to SoC integration. This work considers the frequency interleaving of continuous time DSMs to extend bandwidth. We argue that frequency interleaving is a natural choice for bandpass CT DSMs and is less sensitive to sub-converter mismatch (e.g., timing mismatch) than time interleaving. However, direct frequency interleaving requires operating CT bandpass DSMs with differing center frequencies, combining the outputs, and efficiently suppressing overlapping quantization noise. This work tackles the design of the frequency-offset bandpass modulators and introduces simple filters to efficiently suppress out-ofband quantization noise before combining modulator outputs. A proof-of-concept 2x frequency interleaved prototype doubles the conversion bandwidth with only a 3% power consumption overhead for the additional digital filtering circuity.

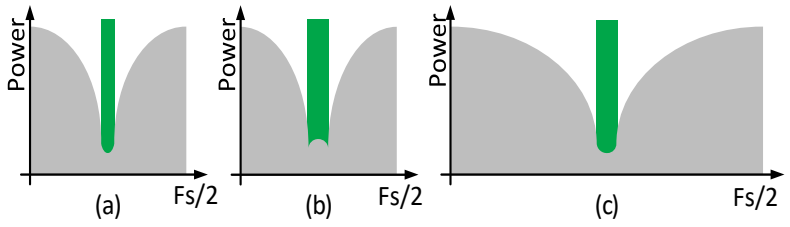

Fig. 13. Traditional Ways to Increase Delta-sigma ADC's Bandwidth
(a) baseline; (b) higher loop-order; (c) higher sampling frequency.

Despite their advantages, CT DSMs lack sufficient bandwidth for emerging arrayed applications, including 5G and radar. The signal bandwidth of recently-published state-of-the-art CT bandpass DSMs is usually less than 200MHz, whereas some Channel Aggregation (CA) schemes (e.g., 5G NR FR1) require up to 300MHz signal bandwidth at the user side. Conventionally, increasing a delta-sigma ADC's bandwidth involves either increasing the sampling frequency or loop order (Fig. 13). However, practical limits to loop order and sampling frequency lead to a performance wall. Among recently published GHz CMOS DSMs, empirically, the maximum sampling frequency is limited to around 9GHz, where the power consumption reaches 1W, which is a practical limit due to the power source, packaging, heat dissipation, etc. Moreover, we observe an exponential power increase with sampling frequency due to challenges in clocking, parameter sensitivity, resonator bandwidth, and loop compensation. This work explores the frequency interleaving of bandpass CT DSM modulators to break the bandwidth-power wall.

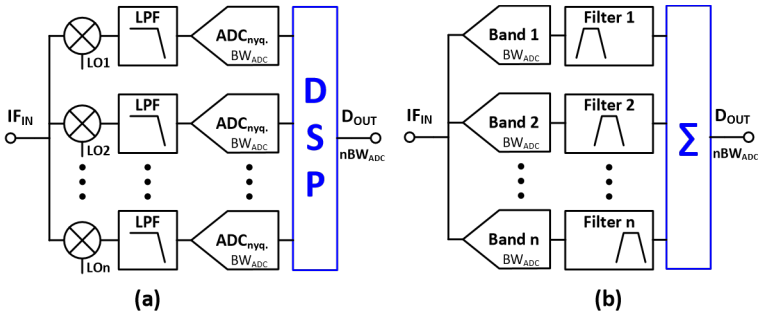

Fig. 14. (a) Mixer-based Frequency Interleaving for a Nyquist ADC; (b) the Concept of Direct Frequency-Interleaving for a Bandpass DSM

Frequency-interleaving is far less prevalent than time-interleaving; in fact, there are relatively few published works on this topic. As illustrated in Fig. 14, there are two general approaches to frequency-interleaving: 1) Mixer-based frequency-interleaving; and 2) Direct frequencyinterleaving. Mixer-based frequency-interleaving splits a broadband input signal into several narrow bands. Mixers down-convert these narrow bands to baseband, allowing digitization at a low conversion rate. The overall output is a combination of all the digitized signals. Although mixer-based frequency-interleaving achieves higher bandwidth and less sensitivity to timing jitter, it involves analog mixers and integrators at the input of each channel and an Inverse Fast Fourier Transform at the digital output for reconstruction, all of which increases the system complexity.

Direct frequency-interleaving eliminates analog mixers but complicates the ADC design as each sub-ADC must work with a different frequency band. Therefore, we cannot simply make identical copies of sub-ADCs as we do in time-interleaving. In direct frequency-interleaving of noise-shaping ADCs, as shown in Fig. 14 (b), multiple bandpass sub-ADCs sample the same analog input. An advantage of noise-shaping bandpass sub-ADCs is that we can avoid filtering the inputs, provided the sample rate and STF are appropriate. We can sum up the outputs of the bandpass sigma-delta modulators to produce the overall result, but we first need to consider the overlapping quantization noise. This is because the shaped quantization noise of a bandpass modulator overlaps the in-band region of the other modulator. Therefore, before combining, we should bandpass filter each modulator output to suppress this out-of-band quantization noise. Summing the n filtered outputs produces an overall output with n-times the sub-ADC bandwidth.

There are four challenges to making a high-bandwidth frequency-interleaving oversampling architecture practical: 1) As mentioned, we should not directly add the modulator outputs because the shaped quantization noise overlaps the useful frequency content of other modulators. In addition, the digital bandpass filters should be power and area efficiency so as not to degrade the overall ADC efficiency; 2) Each bandpass modulator has a different center frequency, and the differing center frequencies complicate loop synthesis and Excess-Loop-Delay (ELD) compensation; 3) Gain mismatch, although not as detrimental as in time-domain interleaving, limits the dynamic range of overall ADC. A particular challenge is to match the in-band SFTs for the different modulators; 4) Finally, the resonator quality factor significantly decreases at high frequency.

This work solves the challenges of efficiently combining multiple DSMs and building DSMs with differing center frequencies. In addition, we propose new techniques to increase the DSM sampling rate substantially. To summarize: 1) 3-tap mirrored FIR filters efficiently suppress the overlapping quantization noise; 2) A zero-insertion resistor in the resonator adds a degree of freedom in the loop transfer function, facilitating different bandpass DSM center frequencies and improving STF/NTF gain mismatch between sub-modulators; 3) Neutralization in the single-opamp resonator boosts the op-amp gain near the resonance frequency, and 4) the Q-enhancement capacitors around the positive feedback RC path form a fast feed-forward path to improve the Q factor of the resonator further.

A 28nm CMOS prototype frequency interleaves two modulators for a 300MHz BW at 1.5GHz with 37dB SNDR while consuming 38mW. Bandpass CT DSM ADCs provide essential advantages for RF and mm-wave systems, including the ability to directly process a high-IF input signal, facilitating digital I/Q mixing. In addition, moderate-resolution wideband bandpass DSMs are especially useful for digital beamforming systems. This practical demonstration shows the potential frequency-interleaving to break the bandwidth bottleneck of CT DSMs.

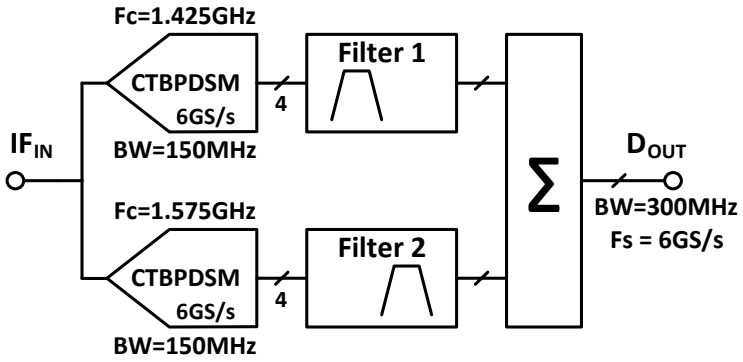

Fig. 15. 2′ Direct Frequency-Interleaving

Our proof-of-concept prototype is a 2x direct frequency interleaving scheme (Fig. 15) with two Continuous-Time Bandpass Delta-Sigma Modulator (CTBPDSM) sub-ADCs. Each sub-ADC has the same 6GS/s sampling frequency. This high sampling rate delivers a sub-ADC bandwidth of 150MHz. The overall 300MHz bandwidth input Intermediate Frequency (IF_{IN}) is centered at 1.5GHz – a high IF is very attractive for mm-wave systems. We offset the center frequencies of the two CTBPDSM sub-ADCs by half of their bandwidths (±75MHz) to produce an overall bandpass ADC frequency range of 1.35GHz-1.65GHz. Two digital bandpass filters with different center frequencies attenuate the quantization noise from each sub-ADC to avoid this noise overlapping the desired signal. Simply summing the filtered outputs of the sub-ADCs produces the final result. The overall signal bandwidth at the frequency-interleaved ADC output (DOUT) is 300MHz, which is twice the individual sub-ADC bandwidth.

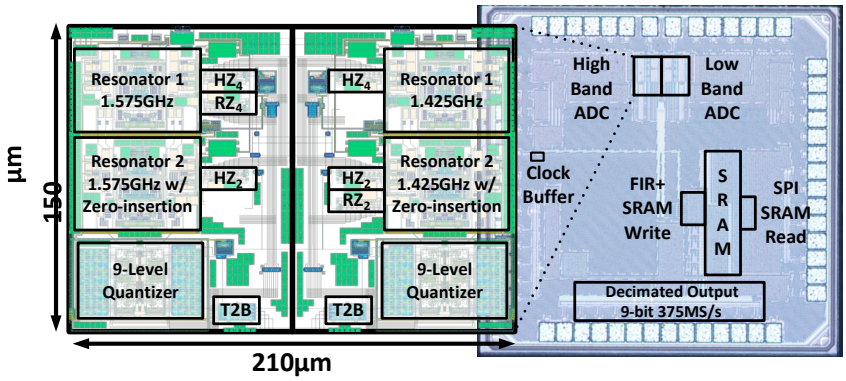

Fig. 16. Die Photo and Layout of the Higher/Lower-Band Sub-Modulator

The prototype (Fig. 16) is fabricated in 28nm CMOS and occupies an active area of 0.0255mm^2. The frequency-interleaving ADC consumes a total of 38mW from a 1.2V supply. The four active resonators contribute 54% of the total power consumption. The 6GS/s 9-level quantizer and the feedback RZ/HZ DACs consume another 43%. The digital FIR filter only takes 3% of the total power due to its simple coefficients and MUX-based operation, which benefit from the short output bit-width of the sub-modulators. Compared with the state-of-the-art, the prototype has a much smaller area and power consumption while supporting the highest input IF frequency of 1.5GHz, making it a very competitive choice for arrayed receiver systems.

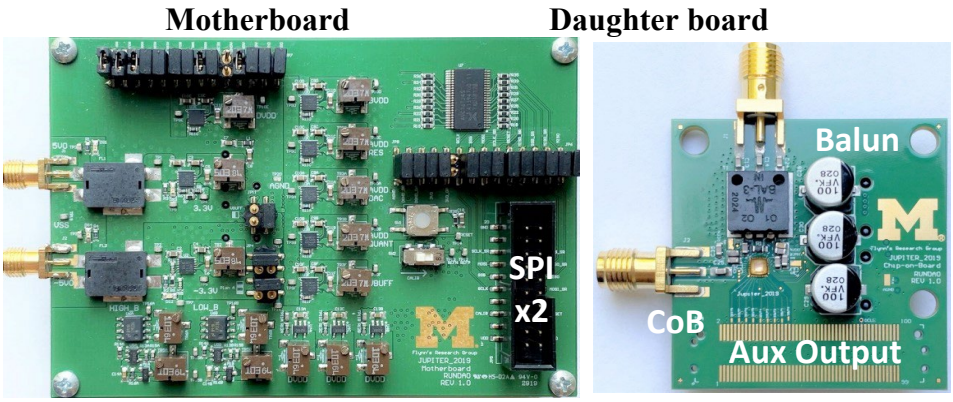

Fig. 17. Chip-on-Board (CoB) Test Set Up

The die is chip-on-board attached to a daughterboard to minimize bond-wire parasitics and facilitate 6GS/s testing. (Fig. 17). An onboard Marki balun (BAL-0003SMG) converts the single-ended signal source to the differential ADC input. The motherboard generates regulated power supplies and references. The daughterboard is mounted to the back side of the motherboard.

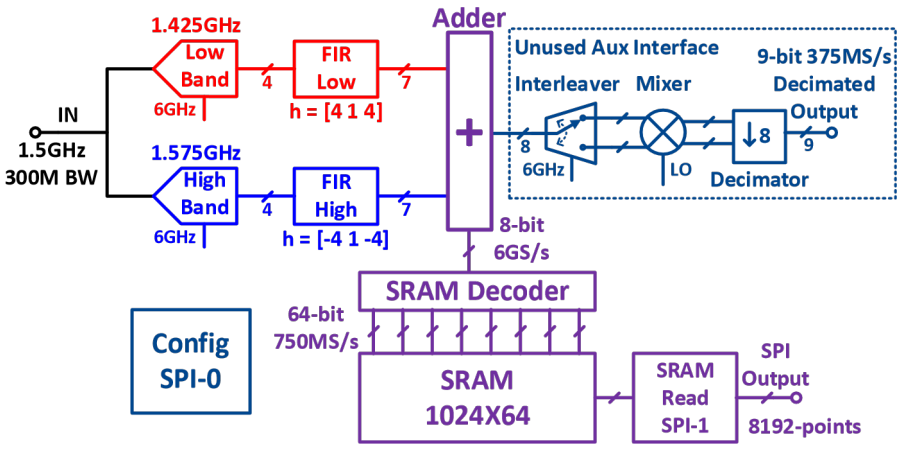

Fig. 18. Full-chip Block Diagram

On-chip SRAM stores the output of the frequency interleaved CT-DSM. Alternatively, the chip provides decimated I and Q streams.

Fig. 18 shows the full-chip block diagram. Due to I/O speed limitations, the prototype stores the 6GS/s high-speed output bit-streams in an on-chip SRAM. Later a low-speed SPI interface reads out the data. There is no off-chip calibration or filtering. The SRAM decoder parallelizes the 8bit 6GS/s ADC output stream to 750MS/s 64-bit words for moderate-speed SRAM writing. The SRAM has a word length of 64 and a depth of 1024 to support up to an 8192-point FFT (corresponding to a 732.4kHz resolution bandwidth).

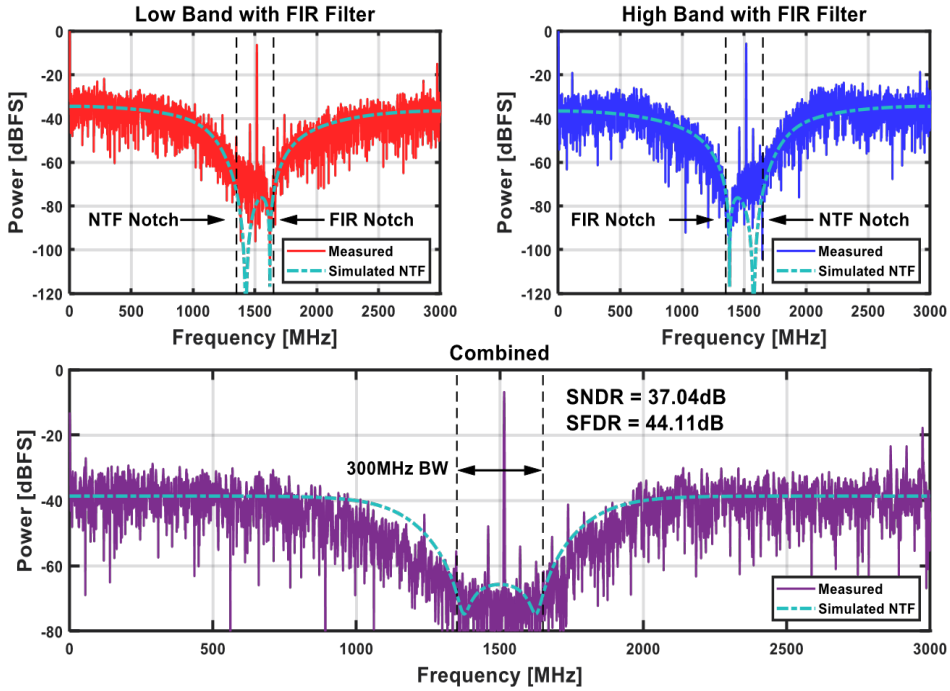

Fig. 19. Measured 8192-Point Power Spectra for Each Sub-Modulator with FIR Filter (top) and Overall ADC Power Spectrum (bottom)

Fig. 19 reports the measured 8192-point power spectra for each sub-modulator with the on-chip FIR filter enabled (top) and the on-chip combined power spectrum (bottom). The measured noise-shaping matches the simulated NTF (dashed line in Fig. 19). The measured SNDR and SFDR are 37dB and 44dB, respectively, for an input frequency of 1514.6MHz and input magnitude of -6dBFS.

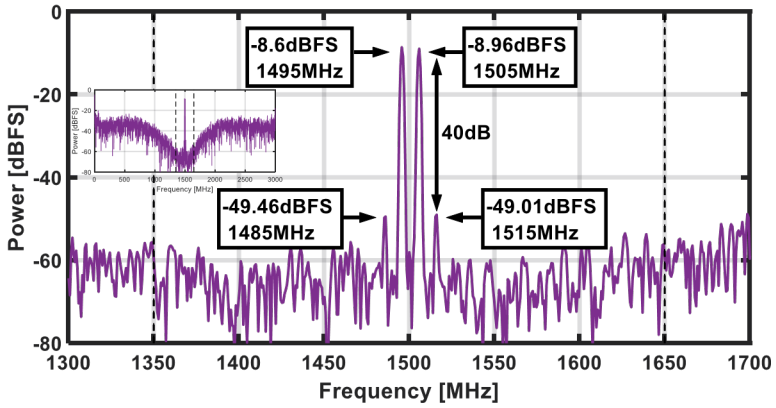

Fig. 20. Measured 8192-Point -9dBFS Two-Tone (1495MHz and 1505MHz) Spectrum

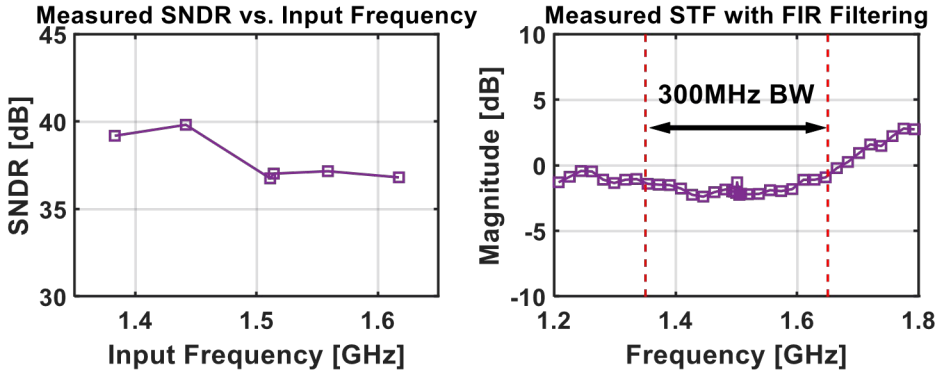

Fig. 21. Measured SNDR versus Input Frequency and Measured STF with FIR Filtering

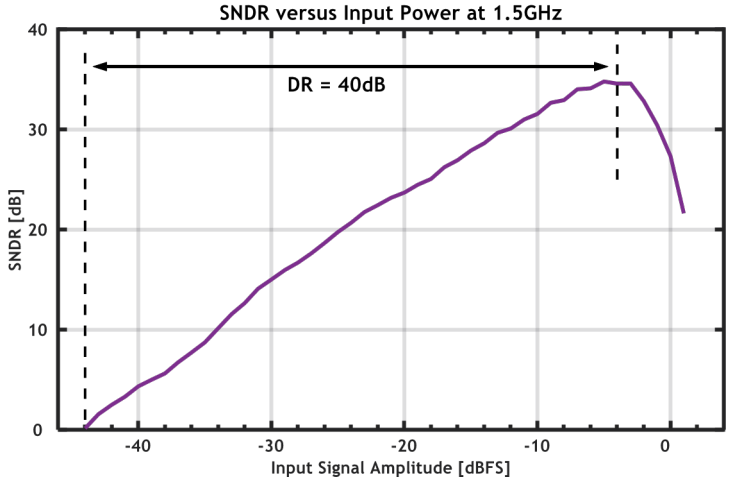

Fig. 22. Measured SNDR versus Input Power for a 1.5GHz Input

Table 1 State-of-the-Art GHZ DSMS WITH BW>100MHZ

	This Work			Wang ISSCC'19	Huang ISSCC'17	Dayanik VLSI'17	Dong ISSCC'16	Wu ISSCC'16
Architecture	**FI-CT-BP-ΔΣ**			CT-ΔΣ	CT-ΔΣ	CT-ΔΣ	CT-ΔΣ	CT-ΔΣ
Technology [nm]	**28**			28	16	40	28	16
Active Area [mm^2]	**0.0255**			0.019	0.217	0.45	1.4	0.155
Fs [MS/s]	**6000**			2000	2150	5000	8000	2880
Bandwidth [MHz]	**300**			100	125	156	465	160
IF Input	**Yes (1.5GHz)**			No	No	No	No	No
Order	**4**			4	4	3	3	4
OSR	**20**			10	8.6	16	8.6	9
Fin_hf [MHz]	**1383**	**1514**	**1617**	18	40	100	400	30
Fin_hf/Bandwidth	**4.61**	**5.05**	**5.39**	0.18	0.32	0.64	0.86	0.1875
SNDR [dB]	**40.16**	**37.04**	**37.33**	72.6	71.9	64.1	64.7	65.33
SFDR [dB]	**52.11**	**44.11**	**53.49**	83.6	85*	-	-	70*
Power [mW]	**38**			16.3	54	233	930	40

*: Estimated from figure.

Fig. 20 shows the measured 8192-point spectrum for a -9dBFS two-tone test. The measured IMD3 is about 40dB lower than the signal tone in the two-tone test. Fig. 21 shows the measured. SNDR versus input frequency and the measured STF with both sub-ADCs on and the on-chip FIR on. The SNDR is more than 37dB across the 300MHz signal bandwidth. Thanks to the mirrored FIR pair, the measured STF is flat from 1.2GHz to 1.8GHz. Fig. 22 reports SNDR versus input power at 1.5GHz - the measurements indicate a dynamic range (DR) of 40dB. Fig. 23 shows the power breakdown.

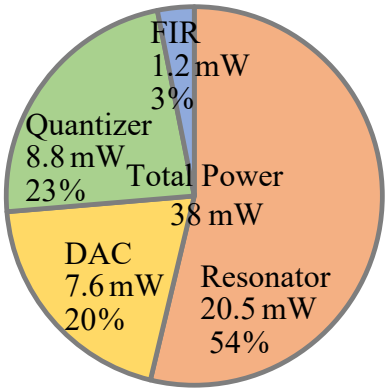

Fig. 23. Total Power and Breakdown

TABLE I compares with state-of-the-art GHz DSMs. The combination of small size, high IF, high BW, and moderate SNDR make this ideal for MIMO and beamforming applications. Furthermore, direct frequency-interleaving avoids the exponential increase of power and area with the increased ADC bandwidth. This work demonstrates that frequency-interleaving breaks the power-bandwidth barrier of CT DSMs.

LIST OF SYMBOLS, ABBREVIATIONS, AND ACRONYMS

ACRONYM	DESCRIPTION
ADC	Analog to Digital Converter
BSP	Bitstream Processing
CML	Current Mode Logic
CMOS	Complementary Metal-Oxide Semiconductor
CT	Continuous-Time
CTBPDSM	Continuous-Time Bandpass Delta-Sigma Modulator
DR	Dynamic Range
DSM	Delta-Sigma Modulator
FPGA	Field Programmable Gate Arrays
I/O	Input Output
I/Q	In-Phase Quadrature
IC	Integrated Circuit
IF	Intermediate Frequency
LO	Local Oscillator
MIMO	Multiple Input Multiple Output
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
SRAM	Static Random-Access Memory
TX/RX	Transmit Recieve
VGA	Variable Gain Amplifier