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**AN AUTONOMOUS AND RAPID-RESPONSE MIMO
DiGiTAL ARRAY RECEIVER FRONT-END
ARCHITECTURE WITH HYBRID SPECTRAL-SPATIAL
UNKNOWN SIGNAL SUPPRESSION AND EXTREME
BANDWIDTH (ARGUS)**

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JULY 2023

Final Report

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14. ABSTRACT The proposed project aims at designing and demonstrating next generation wireless frontend array system architectures what can support wideband communication links and be robust in increasingly complex and dynamic EM environment. The demonstrated system can also support the wireless communication links with "smart" front-end functionalities such as autonomous spatial filters and dynamic array operations. This is in response to the rapidly growing use of mm-Wave spectrum for next generation wireless systems, which requires enhanced wideband, high data rate, enhanced signal-to-noise ratio (SNR) and wireless link budget through array-based systems. These advanced applications impose stringent requirements on the array frontend circuits. To achieve this goal, this project will involve designing new circuits and system architectures to efficiently handle the signals and interferences, including ultra-wideband RX frontend, 2D autonomous beamforming, autonomous polarization alignment, and time-modulated array with concurrent steerable multi-beam MIMOs. The effectiveness of these proposed system is tested with state-of-the-art silicon IC implementations and is demonstrated through real-world experiments and measurements					
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Table of Contents

Section	Page
List of Figures	iii
List of Tables	vi
1 SUMMARY	1
2 INTRODUCTION	2
3 A 43-97GHZ MIXER-FIRST FRONT-END WITH QUADRATURE INPUT MATCHING AND ON-CHIP IMAGE REJECTION.....	4
3.1 System Overview	4
3.2 RF Coupled-Line-Coupler (CLC).....	5
3.2.1 Passive Mixer and LO Balun	8
3.2.2 If Amplifiers and if Transformer-Based Coupler	10
3.3 Experimental Results	12
3.3.1 Gain, Image Rejection and Matching	13
3.3.2 Modulation Testing.....	14
4 MMWAVE 2D 2X2 RECEIVER WITH AUTONOMOUS SPATIAL FILTER AND BEAMFORMING.....	18
4.1 System Overview	18
4.1 Circuits Implementation.....	22
4.1.1 Broadband mm-Wave Receiver Frontend	23
4.1.2 Autonomous Beamformer.....	24
4.1.3 Negative Feedback Loop of Autonomous Beamformer	25
4.2 Experimental Results	25
5 A TIME-MODULATED CONCURRENT STEERABLE MULTI-BEAM MIMO RECEIVER ARRAY WITH SPECTRAL-SPATIAL MAPPING USING ONE BEAMFORMER AND SINGLE-WIRE INTERFACE	32
5.1 System Overview	32
5.1.1 Time-Modulated Spectral-Spatial Mapping MB-MIMO RX.....	34
5.1.2 SNR Consideration in Time-Modulated MIMO RX	36
5.1.3 Time-Modulated MB-MIMO RX with Beam-Steering.....	37
5.2 Circuits Implementation.....	38
5.2.1 Experimental Results	40
5.2.2 Single Path RX Performance Characterization.....	41
5.2.3 Time-Modulated MIMO RX Array	42
5.2.4 Space Division Multiple Access Communication Using Time-Modulated Mimo Rx Array	43
6 A 26-32 GHZ DUAL-POLARIZATION RECEIVER FRONTEND WITH RAPID- RESPONSE MIXED-SIGNAL POLARIZATION ALIGNMENT FOR ULTRA-RELIABLE LOW LATENCY COMMUNICATIONS.....	46
6.1 System Overview	46
6.1.1 Analog/mixed-signal Computation Unit.....	46
6.1.2 Autonomous Control Voltage Generation	47
6.1.3 Feedback Loop Concept	48
6.2 Circuits Implementation.....	48

Section	Page
6.3 Experimental Results	51
6.4 PUBLICATIONS SUMMARY	52
7 CONCLUSION.....	55
8 REFERENCE.....	56
LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS	61

List of Figures

Figure	Page
Figure 1: Proposed Receiver Front-End	5
Figure 2: RF Coupled-Line-Coupler (CLC)	6
Figure 3: Simulated CLC	7
Figure 4: Simulated I/Q balance of the CLC	7
Figure 5: (a) Passive I/Q Mixer Implementation, (b) Normalized Gain at Different Harmonics, (c) Noise Figure Versus Bias Voltages, (d) Normalized Gain Versus Bias Voltages, (e) Normalized Gain Across IF Frequency ($f_{LO}=70\text{GHz}$), (f) Normalized Gain at the Antenna Interface ($f_{LO}=70\text{GHz}$)	9
Figure 6: (a) LO Marchand Balun and Matching Network, (b) EM Structure, (c) Gain Mismatch of the Differential Outputs, (d) Phase Difference of the Outputs	10
Figure 7: IF Section of the Font-End	12
Figure 8: Different Measurement Setups used for Chip Characterization.....	14
Figure 9: Measurement Results	15
Figure 10: (a) Noise Contributors at Different nodes, (b) Simulated Noise Figure Across IF Frequency for LO Frequency of 70 GHz.....	15
Figure 11: Modulation Performance.....	16
Figure 12: Operation Principle of the Proposed 2D MIMO RX Array	18
Figure 13: Autonomous Beamformer Operation Loop.....	19
Figure 14 (a) Simulated Control Voltage Response between the System with Only 2-X/Y AB and Proposed System (b) Simulated Waveform for Only 2-X/Y AB and Proposed System (c) Simulated Phase Shift Response Regarding to Control Voltage (d) Simulated Normalized Array Factor for Conventional Phased System (e) Proposed System with AB showing Full FoV Functionality (f) Operation Principle for both AB and Autonomous Spatial Filter(ASF)	20
Figure 15: Block Diagram of the Proposed 2D MIMO RX Array with Both Autonomous Beamforming and Spatial Filtering Functionalities.....	22
Figure 16 (a) Detailed Circuits Schematics of mm-Wave LNA (b) Detailed Circuits Schematics of Auxiliary Path to Extract the Strongest Signal (c) Detailed Block Diagram of Implemented 2-Stage Transformer Based I/Q Generation Circuits (d) Detailed Block Diagram of Implemented Autonomous Beamformer (e) Detailed Circuits Schematic of IF Amplifier (f) Detailed Block Diagram of Phase Shifter (g) Detailed Circuits Schematics of Doubly-Balanced Mixer.....	23
Figure 17 Measured Three Mode Operations of the Proposed 2D 2x2 MIMO Rx Array	26
Figure 18 Measured Wideband RX Array Element Conversion Gain (CG), Input Matching S_{11} , Noise Figure NF, Autonomous Spatial Discrimination of Concurrently Received Two-Tones Down to 1dB Power Difference for Different Incident Angles (the Stronger Tone is Automatically Identified by the Power-Aware Phase Detector in ASF and Subsequently Rejected), and In-band Blocker Pin1dB with the 1st-stage Spatial ASF being Turned on or Off	27
Figure 19 The Implemented mm-Wave RX MIMO Array with 2-stage ASFs Demonstrate Concurrent Autonomous Rejection of Blockers and Automatic Desired Signal Beamforming ..	28

Figure	Page
Figure 20 The mm-Wave RX MIMO Array with 2-stage ASFs Demonstrate Concurrent Autonomous Rejection of Blockers and Automatic Desired Signal Beamforming (the Blockers and Desired Signal are Co-channel with the Same Broadband Modulation and data-rate), Demonstrating Successful Receiving of the Desired Signal after Autonomous Spatial Suppression of One Spatial Blocker	29
Figure 21 Measured Closed-loop Response Time of the Autonomous Spatial Filter using a Real-time Oscilloscope and Breakdown of DC Power Consumption/per element and Chip Area.....	30
Figure 22 Operation Principle of the Proposed TM Spectral-spatial Mapping MB-MIMO RX Array	32
Figure 23 Time-modulated (TM) Sequence of an N-element Linear Array	34
Figure 24 Theoretical Normalized Array Factor of the N=2 and 8 TMA for MB-MIMO Beamforming	35
Figure 25 Simulated TM MB-MIMO RX Array with 30° Beam-steering	36
Figure 26 System Block Diagram and Detailed Schematic of the Proposed TM MIMO RX Array	38
Figure 27 Chip Micrograph of the Proposed TM MIMO RX Array and Measurement Setup for the mm-Wave TM MIMO RX Array for Both CW and Modulated Signals.....	40
Figure 28 Measured Wideband RX Array Element Conversion Gain (CG), Input Matching S ₁₁ , Noise Figure NF, Input-referred 1dB Compression Point IP _{1dB} , and Image Rejection.....	40
Figure 29 Measured Wideband Receiver With HIGH-Speed Complex Modulated Single Carrier Signal with Both 16-QAM and 64QAM.....	41
Figure 30 Measured Normalized Array Pattern of 4-element MIMO RX Array with Time Modulation to Achieve Concurrent Steerable 5-bands (n= 0, ±1, and ±2), while the Full FoV can be Covered by RX Array Beam Steering with a Much-Reduced Phase Shifting Range (-30°<θ<30°), Enabling Fast Array Beam Scanning Over the Full FoV	43
Figure 31 Measured Complex Modulation Performance of the 4-element MIMO RX Array with Time Modulated Spectral-spatial Mapping with Concurrent 5 Beams showing Incident Angles of 0° and 30° are Mapped to 0* FTM (3.5GHz) and 1* FTM (3.7GHz) IF Tones	44
Figure 32 Measured Complex Modulation Performance of the 4-element MIMO RX Array with TM Spectral-spatial Mapping with Concurrent 5 Beams Showing Two Concurrently Received Signals with -30° and 30° Incident Angles are Mapped to -1* FTM (3.3GHz) and +1* FTM (3.7GHz) IF Tones	44
Figure 33 Signal Cross Contamination Due to TX/RX Antenna Misalignment and Proposed Low Latency Analog/Mixed-Signal Computation Unit.....	47
Figure 34 Autonomous Control Voltage Generation Block Diagram	47
Figure 35 The Proposed mm-Wave Dual-Polarization Receiver RX Front Ends (RX _V and RX _H) with Autonomous Rapid Polarization Alignment.....	49
Figure 36 Circuit Details of (a) CMOS Power Detector Circuit (b) Op-amp (c) Hysteresis Comparator (d) Sine/Cos Generation Circuit	50
Figure 37 Measured RX S ₁₁ , Gain, P _{1dB} and NF Across Frequency Range, as well as the Measured Autonomous Polarization Alignment Performance Over the Entire -90° to +90° Polarization Mismatch Range	51

Figure**Page**

Figure 38 The Measured SNR(MER) for Outputs RXH and RXV with 1.8Gb/s 64QAM Modulation and the Measured Constellation of Outputs RXH and RXV with 1.8Gb/s 64QAM Modulation when Misalignment Angles θ vary from 15° to 90°	52
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List of Tables

Table	Page
Table I Results Comparison with The State-of-The-Art.....	16
Table II Results Comparison with The State-Of-The-Art	30
TABLE. III Comparison with Recently Reported State-of-the-Art mm-Wave MIMO RXs	45
TABLE. IV Comparison with recently reported state-of-the-art Designs.....	52

1 SUMMARY

The proposed project aims at designing and demonstrating next generation wireless frontend array system architectures what can support wideband communication links and be robust in increasingly complex and dynamic EM environment. The demonstrated system can also support the wireless communication links with “smart” front-end functionalities such as autonomous spatial filters and dynamic array operations. This is in response to the rapidly growing use of mm-Wave spectrum for next generation wireless systems, which requires enhanced wideband, high data rate, enhanced signal-to-noise ratio (SNR) and wireless link budget through array-based systems. These advanced applications impose stringent requirements on the array frontend circuits.

To achieve this goal, this project will involve designing new circuits and system architectures to efficiently handle the signals and interferences, including ultra-wideband RX frontend, 2D autonomous beamforming, autonomous polarization alignment, and time-modulated array with concurrent steerable multi-beam MIMOs. The effectiveness of these proposed system is tested with state-of-the-art silicon IC implementations and is demonstrated through real-world experiments and measurements.

2 INTRODUCTION

Millimeter-Wave spectrums have been extensively used for wireless communications. Its rich frequency spectrum resources can support multi-gigabits per second (Gbit/s) signals. Therefore, mm-Wave frequency is a great candidate for the emerging communication networks such as vehicle-to-everything (V2X) links, drone-to-everything (D2X) links, and intelligent transportation systems (ITS), which need to exchange a large amount of sensor data. In addition, there is a fast-growing trend to deploy mm-Wave wireless technologies for infrastructure, fixed-point, and mobile wireless communications. However, mm-Wave wireless links usually suffer from higher propagation loss compared to sub-6GHz counterparts such as high frequency bands include the V-band (40-75 GHz), E-band (71-76 GHz, 81-86 GHz, and 92-95 GHz) and W-band (75-110 GHz). Therefore, mm-Wave wireless links usually require a large array size to largely compensate for the millimeter-wave (mm-Wave) link loss; nevertheless, large arrays result in “pencil-like” sharp beams, which drastically complicates the beam alignment and poses challenges in the transmitter (TX) and RX array operations in practice. In existing methods, highly intensive DSP-controlled and AI/machine learning calibration [1] - [3] are required to align the sharp pencil-like beams of TX and RX. It not only causes high complexity but also brings a trade-off between accuracy and latency. [4] proposes the future of the 6G wireless communication systems supporting wireless links with <0.1ms latency. Therefore, future array-based mm-Wave wireless links will require fast and precise beamforming/-tracking to ensure high link reliability, enhanced data rate, and low latency.

In parallel, the future mm-Wave wireless links are expected to operate in complex and dynamic electromagnetic (EM) environments, exposed to unknown strong interferences with unknown angle-of-arrival (AoA), unknown frequencies, and modulation schemes. Some of the application examples include SATCOM-on-the-Move (SOTM) with satellite terminals mounted on cars, 5G mobile user terminals facing constant blockages, drones with mm-Wave data links, and HD AR/VR devices for immersive gaming.

The mm-Wave RX arrays are required to handle the complex and dynamic channel conditions and accommodate strong signals/blockers without compressions. Multiple analog beamformers [5] - [6] are reported to support spatial notches can and reject the blocker signals, but they typically exhibit limited FoV and are restricted to multiple-input single-output (MISO) systems. However, multiple analog beamformers for true MIMO operations will add substantial complexity. On the other hand, digital beamforming arrays can support full FoV and true MIMO capabilities with multi-stream/beams to support concurrent multibeam operations and improve spatial-spectral efficiency for multiple end users. With beamforming and spatial filtering all in the digital backend, digital beamforming arrays offer substantially more flexibility compared to their analog counterparts.

In practice, processing all the aperture information by the digital backend means that the RX downstream circuits such as the analog-to-digital converters (ADCs) need to handle all the in-band information including strong interferences, substantially increasing the linearity requirements. Recently, multiple beamformers with RF spatial filtering [7] - [8] are reported for digital RX phased arrays. The challenge is that their RF frontend designs require prior knowledge of the signals’/blockers’ AoA and frequency. Therefore, these hybrid RF filtering

digital arrays cannot respond to interference at the unknown frequency and/or from fast-varying AoA.

To address these problems, research on *self-steering arrays* is gaining increasing momentum recently, which can dynamically track the desired signals or unwanted blockers using analog closed loop beamformers. Existing self-steering arrays often use coupled PLL or VCOs that exhibit limited field-of-view (FoV) and array scalability and cannot process multi-beams [9]. Recently, a Delay-Lock-Loop (DLL) like topology for autonomous beam tracking is demonstrated [10], which achieves a complete analog/RF closed-loop for fast beamforming and spatial notching. However, its MIMO size decreases by two for every stage of its autonomous beamforming, and thus it supports true MIMO operation. On the other hand, an auxiliary-path base channel addition/subtraction is demonstrated in [11] that preserves the full array scale after autonomous beamforming for achieving true MIMO without compromising the MIMO dimension. On the other hand, this work is still limited to the 1D array operation intrinsically due to its autonomous beam acquisition circuit blocks. It is worth mentioning that both [10] and [11] use only one beamformer for all four elements, the outer channels alignment in the array only relies on architecture symmetry and pure analog signal computation. Thus, it will cause non-negligible and non-recoverable channel-to-channel phase errors, especially when being scaled to larger arrays. [12] utilizes a two-step mixed-signal phase alignment loop and bidirectional voltage-current converter to provide the desired spatial notch. It can provide a maximum of 40dB spatial rejection in full FoV. But its mixed-signal operation complicates the design and requires external digital hardware (MCUs) to perform beamforming which requires a long response time (latency). Moreover, its reported array architecture is also only 1D (in one dimension).

To address the aforementioned challenges and enable future mm-Wave wireless technologies in complex EM environments, we propose and demonstrate a ultra-wideband receiver frontend to fit multiple mm-Wave frequency standards and a 2D 2x2 MIMO receiver array to autonomously spatially filter out strong cochannel blocker signals. Furthermore, we proposed and demonstrated two interesting array systems for the future dynamic and smart frontends.

3 A 43-97GHz MIXER-FIRST FRONT-END WITH QUADRATURE INPUT MATCHING AND ON-CHIP IMAGE REJECTION

3.1 System Overview

To achieve a wideband receiver front-end while providing only the desired IF bandwidth at the early stage of operation and maintaining high intermodulation performance, this work presents a mixer-first front-end achieving an ultra-wideband frequency of operation from 43 to 97 GHz (77% fractional bandwidth) covering most of the high-frequency mmWave bands while maintaining a 1-GHz output IF bandwidth of operation with an IF frequency of 3.8 GHz. The topology used is low IF rather than zero IF to mitigate the effects of dc-offsets, flicker noise, and local oscillator (LO) leakage [13]. In addition, in our implementation, using higher IF frequency helps reducing the area of the image rejection transformer-based coupler.

The state-of-the-art mixer-first implementation includes [14], [15], where the RF port is matched with a high-order matching network and the output signal is connected directly to all the mixer switches while generating the quadrature signal at the LO. This implementation achieves a bandwidth from 70 to 100 GHz (fractional bandwidth of 35.3%) and low operation power. In the implementation presented in [16], coplanar T-lines are used instead of inductors for input matching and for splitting the RF signal for the mixers while the quadrature signal is generated at LO. This implementation achieves a bandwidth from 49 to 67 GHz (fractional bandwidth of 31%). Other RF signal splitting techniques include a power divider at RF to isolate the I/Q switches. This would induce 3 dB of loss (+ ohmic loss) at RF while still needing to generate quadrature LO signals.

The proposed chip (Fig. 1) generates quadrature signals at the RF domain rather than the LO domain [17] - [19], by incorporating RF 90° coupled-line coupler (CLC). This configuration is used because the characteristics of the CLC can be exploited to achieve wideband input matching without the need for additional high-order matching networks that will induce losses. In addition, and more importantly, at such high frequencies it is not possible to generate non overlapping I/Q LO phases, and hence, the choice of quadrature LO generation will cause crosstalk between mixer switches to occur, thus degrading the down conversion performance [20], [21]. Finally, this design decouples the input matching design from the mixer size choice. The generated quadrature signal is then down converted to IF frequency using passive mixers, designed with high linearity to reduce the effect of interferes' intermodulation products and to provide bandpass filtering for out-of-band blockers. The choice of the mixer switch size is determined by the NF and linearity requirements without worrying about the input matching performance. The mixer switches are driven by a differential LO signal generated with on-chip Marchand balun.

The IF section of the front-end consists of two-stage high linearity amplifiers incorporating multi-gated transistors (MGTRs) [22] - [27] to maintain high intermodulation performance (IP3), necessary when implementing beamformer or MIMO systems [28]. The second stage is loaded with a transformer-based coupler [13][29] - [33] to provide current mode on-chip image rejection.

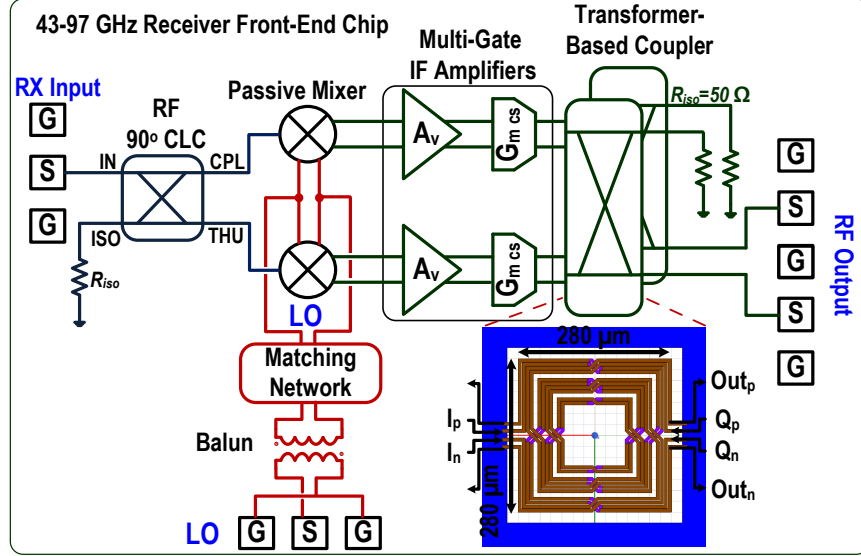


Figure 1: Proposed Receiver Front-End

3.2 RF Coupled-Line-Coupler (CLC)

The structure of the multi-section CLC is shown in Fig. 2. It is implemented using two or more small coupler-line-coupler sections with different coupling coefficients and frequency range of operation. When these sections are cascaded, the overall performance will cover a broader bandwidth of operation [34]. Figure 2(a) and 2(c) show the parameters and EM structure used, and Fig. 2(b) shows the flowgraph of an ideal coupled line coupler. The S-parameters of an ideal coupled-line-coupler is shown in (1) where C is the coupling coefficient[34] - [37].

$$\begin{aligned}
 S_{11} &= S_{22} = S_{33} = S_{44} = 0 \\
 S_{12} &= S_{21} = S_{34} = S_{42} = -j\sqrt{1 - C^2} \\
 S_{13} &= S_{31} = S_{42} = S_{24} = C \\
 S_{14} &= S_{41} = S_{23} = S_{32} = 0
 \end{aligned} \tag{1}$$

From Fig. 2(b), if port 4 is matched ($\Gamma_4 = 0$) and $\Gamma_{L2} = \Gamma_{L3} = \Gamma_L$, then the input reflection coefficient (Γ_{IN}) is calculated to be:

$$\begin{aligned}
 \Gamma_{IN} &= S_{21}S_{12}\Gamma_L + S_{31}S_{13}\Gamma_L \\
 &= (C^2 - 1)\Gamma_L + C^2\Gamma_L \\
 &= (2C^2 - 1)\Gamma_L \\
 &= 0 \quad \text{when } C = 1/\sqrt{2}
 \end{aligned} \tag{2}$$

This indicates that regardless of the load impedance presented at the coupled and through port (arbitrary Γ_L), the input matching is maintained as long as the input power is equally split between the coupled and through ports. This is demonstrated with simulating S_{11} of the CLC structure loaded with different impedances (Fig. 3(a)) and showing good matching performance. Figure 4b shows the overall gain and phase matching of the CLC when loaded with the actual mixer load. Figure 3(c) and 3(d) shows the actual parameters of the implemented CLC; namely the characteristic impedance (Z_0), the even mode impedance (Z_{0e}), the odd mode impedance (Z_{0o}) and the coupling coefficient (C). The equations relating these parameters are as follows [34]:

$$Z_0 = \sqrt{Z_{0e}Z_{0o}} \quad (3)$$

$$C = \frac{Z_{0e} - Z_{0o}}{Z_{0e} + Z_{0o}}$$

The choice of a multi-section CLC helps in extending the performance range of the I/Q balance of the structure [34]. Figure 4(a) shows the simulated I/Q balance of the coupler when loaded with 50Ω . The figure compares a plot for the multi-section coupler versus a family of plots for the single section coupler, where the length and width are swept, showing a wider performance bandwidth for the multi-section implementation. The equation used to generate the plot is:

$$I/Q \text{ Balance} = \frac{\varepsilon^2 + \Delta\theta^2}{4} \quad (4)$$

Where ε represents the amplitude mismatch and $\Delta\theta$ represents the phase mismatch.

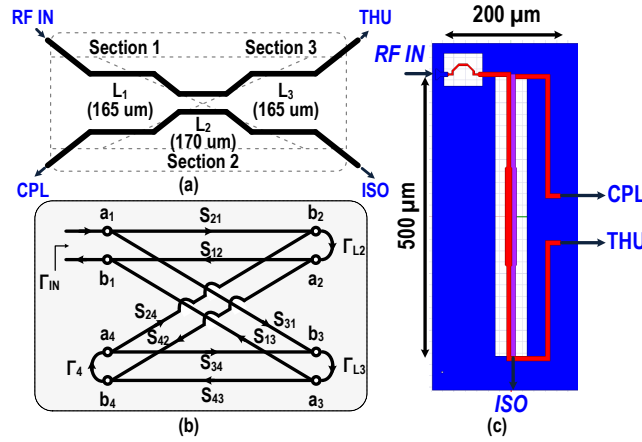


Figure 2: RF Coupled-Line-Coupler (CLC)

(a) Multi-section parameters, (b) Ideal signal flowgraph (c) EM structure.

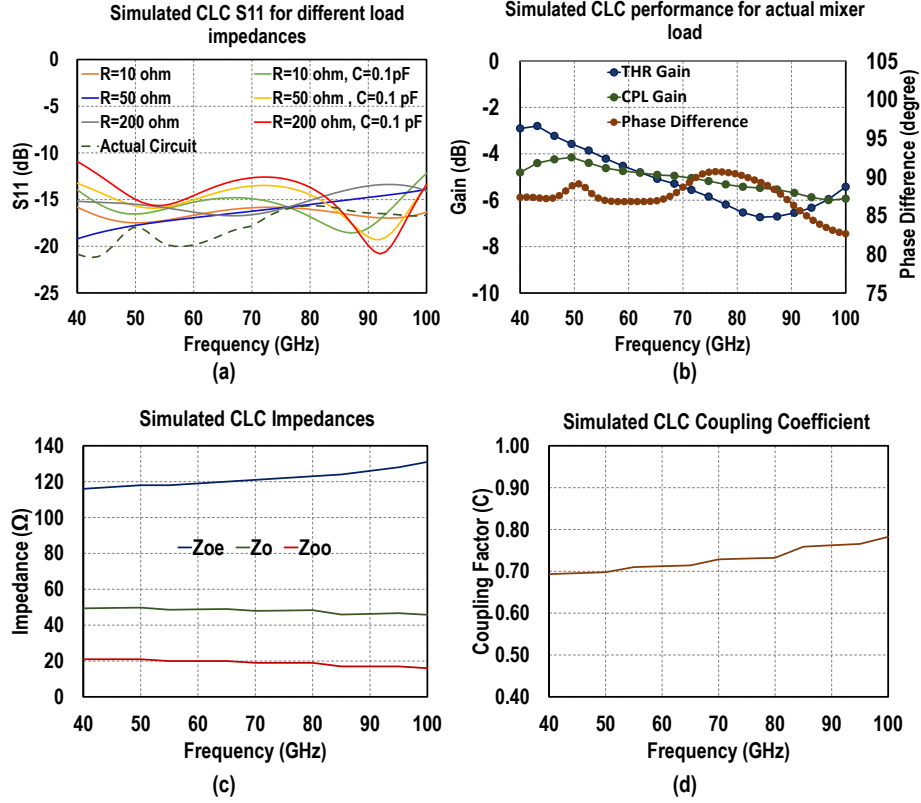


Figure 3: Simulated CLC

(a) S_{11} for different load impedances, (b) phase difference and gain of the coupled and through ports with mixer load, (c) even, odd, and characteristic impedances, (d) coupling coefficient.

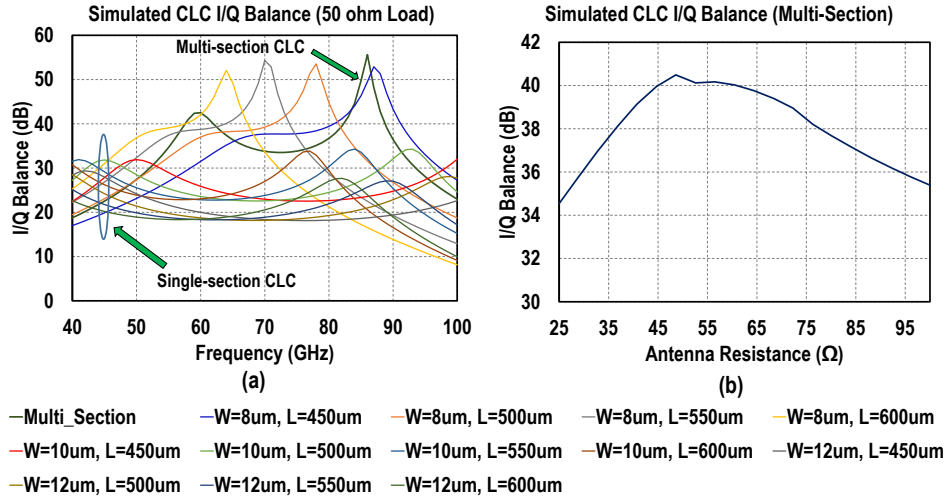


Figure 4: Simulated I/Q balance of the CLC

(a) With different sizes of a single section CLC as well as the chosen multi-section CLC, (b) Across antenna resistance variation.

Figure 4(b) shows the I/Q balance of the coupler with antenna impedance variations. For large antenna impedance variations, the I/Q balance can be degraded. It should be noted this I/Q imbalance can be mitigated by tuning the isolation resistance to match the antenna resistance.

3.2.1 Passive Mixer and LO Balun

The passive mixer implementation is shown in Fig. 5(a), it consists of a single-balanced implementation for each of the I/Q cells with a differential sine wave LO signal. The simulated conversion gain around the LO harmonics is shown in Fig. 5(b). The fact that the LO signal is a sinusoidal wave, ideally only the fundamental component of the LO should be present. However, because of the non-linearities and on-off-like operation of the transistors, RF signals around the third harmonic of the LO signal will be down-converted to the desired IF band. Several techniques are proposed in the literature to further reduce or cancel the third harmonic folding [38] - [41]. However, some of these techniques requires the use of driving frequencies at harmonics of the LO or generation of more than 4 LO phases. These techniques are either complex and cause degraded performance or not practical at such high frequencies. In this implementation, third order harmonic will always be outside the bandwidth of operation (43~97 GHz) and will be suppressed when the front-end is integrated with the corresponding antenna. Therefore, these techniques are not implemented to avoid performance degradation.

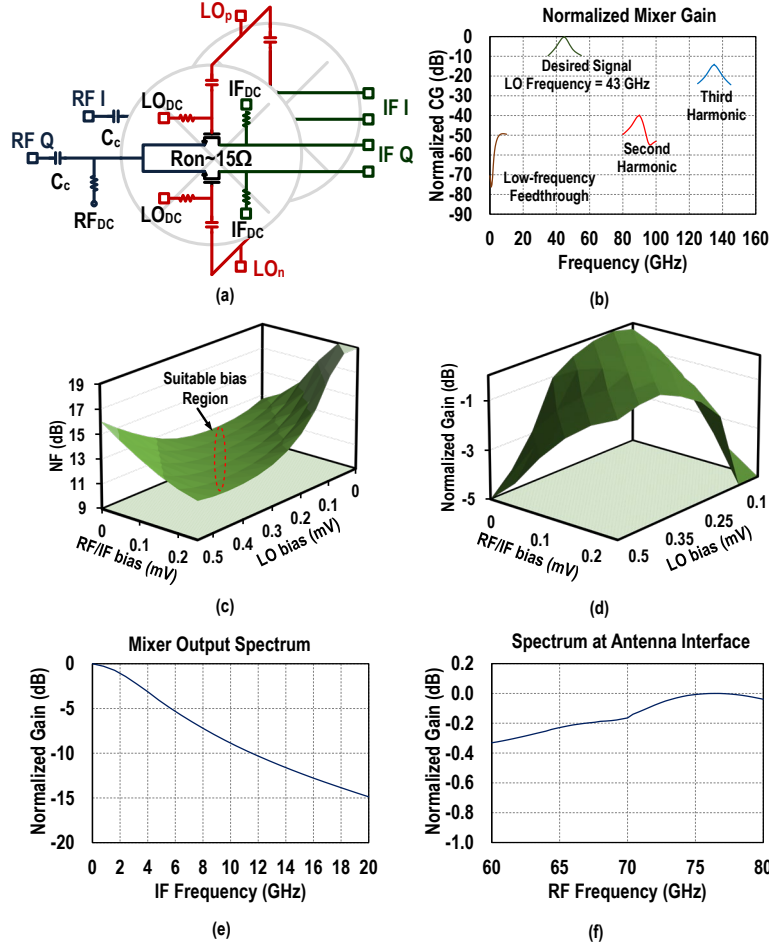


Figure 5: (a) Passive I/Q Mixer Implementation, (b) Normalized Gain at Different Harmonics, (c) Noise Figure Versus Bias Voltages, (d) Normalized Gain Versus Bias Voltages, (e) Normalized Gain Across IF Frequency ($f_{LO}=70\text{GHz}$), (f) Normalized Gain at the Antenna Interface ($f_{LO}=70\text{GHz}$)

Figure 5(c) and 5(d) shows the simulated noise figure and normalized gain versus the LO (gate) bias and RF/IF bias voltages. The optimum difference between the LO and RF/IF voltages is around 0.2 V. Finally, fig. 5(e) and 6(f) shows the normalized gain at the mixer output and at the antenna interface. Noting that because of the wideband matching provided by the CLC, the gain at the antenna interface has small variations.

The differential LO phases are generated with an on-chip Marchand balun [34][42][43] and a high order matching network (Fig. 6). The simulated gain mismatch between the signal is between -0.6 to 0.2 dB (Fig. 6(c)) and the phase difference is shown in Fig. 6(d).

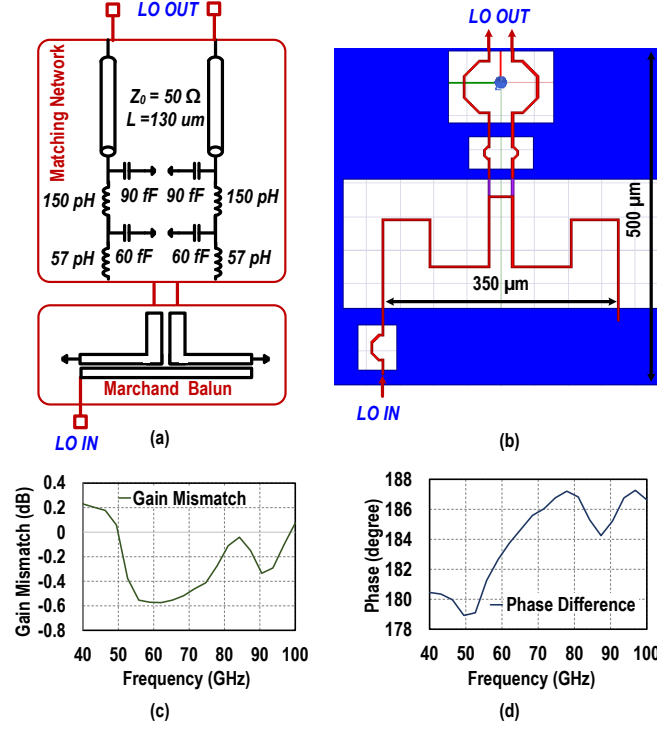


Figure 6: (a) LO Marchand Balun and Matching Network, (b) EM Structure, (c) Gain Mismatch of the Differential Outputs, (d) Phase Difference of the Outputs

3.2.2 If Amplifiers and if Transformer-Based Coupler

The IF gain section is composed of two stage amplifiers employing multi-gated transistors to achieve gm3 cancellation of the main transistor [22] - [29]. This technique is helpful in improving small signal non-linearity (IIP3) but not large signal non-linearity (P1dB). The first stage (Fig. 7(a)) is implemented as tuned cascode structure with one main transistor and three auxiliary transistors with different sizes and bias voltages. Figure 8b shows the gm3 of each of the four transistors as well as the overall gm3. Here, the auxiliary transistors (M2-M4) have a reduced bias voltage (compared to M1) allowing them to switch later on and shift their gm3 plots to the left. In addition, the gm3 values of the auxiliary transistors are scaled by sizing them differently from the main transistor. Hence, collaboratively equalizing the highly negative gm3 of the main transistor and achieving a flat overall gm3 performance. Since the auxiliary transistors need to be biased in class B or C (or AB), they are implemented as high threshold voltage transistors (hvt) as opposed to low threshold voltage transistor (lvt) used for M1. Choosing between hvt and lvt transistors to implement M2-M4 is arbitrary and both options can achieve similar performance. In Fig. 8(c), simulations for the transistor M3 with lvt and hvt flavors show indeed the gm3 value and current consumption is almost the same for both options with the correct bias values and sizes ($W = 30 \mu\text{m}$ for lvt and $24 \mu\text{m}$ for hvt). However, the lvt transistor requires 60mV lower bias voltage than the hvt transistors and hence impose more limitation on the usable bias voltage range of the main transistor when all the bias voltages should be positive (i.e. the M1 bias cannot be lower than 350mV when using hvt transistor and 410mV for lvt transistor). The second stage (Fig. 8d) is a gm stage implementing the same multi-gate transistors without the cascode transistor. The output current of the gm stages from the I and

Q paths are used to feed an IF transformer-based coupler [30]-[34] (Fig. 1) acting as a polyphase filter in order to reject the image signal.

The overall gm3 is simulated under process and temperature variations (Fig. 7(e)), showing that the flatness of the gm3 curve will be affected. Also, the simulated IIP3 of the first stage amplifier is shown in the small subfigure in fig. 8e. The flatness of the gm3 can be correct (Fig. 7(f)) by slightly changing the bias points of the auxiliary transistors (within ~30mV) to retrieve the flatness of the plot. In this work, this bias tuning needs to be done manually for each process and corner.

The simulated image rejection performance of the overall frontend is shown in Fig. 8. Here, the gate biases of the I/Q passive mixer transistors are independently swept from 50mV to 250mV such that the loading presented to the coupled and through ports of the coupler are made slightly different. Hence, rebalancing the coupled and through mismatches at different frequencies. This can be illustrated intuitively by writing down the power delivered to each port (with the help of Fig. 2b) as shown in (5). When the S-parameters of the coupler is not completely matched ($S_{31} \neq S_{21}$), then, this can be slightly corrected by making Γ_{L2} and Γ_{L3} not equal.

$$\begin{aligned}
 b_2 &= S_{21}a_1, & b_3 &= S_{31}a_1 \\
 P_2 &= |b_2|^2(1 - |\Gamma_{L2}|^2) \\
 &= |S_{21}a_1|^2(1 - |\Gamma_{L2}|^2) \\
 P_3 &= |b_3|^2(1 - |\Gamma_{L3}|^2) \\
 &= |S_{31}a_1|^2(1 - |\Gamma_{L3}|^2)
 \end{aligned} \tag{5}$$

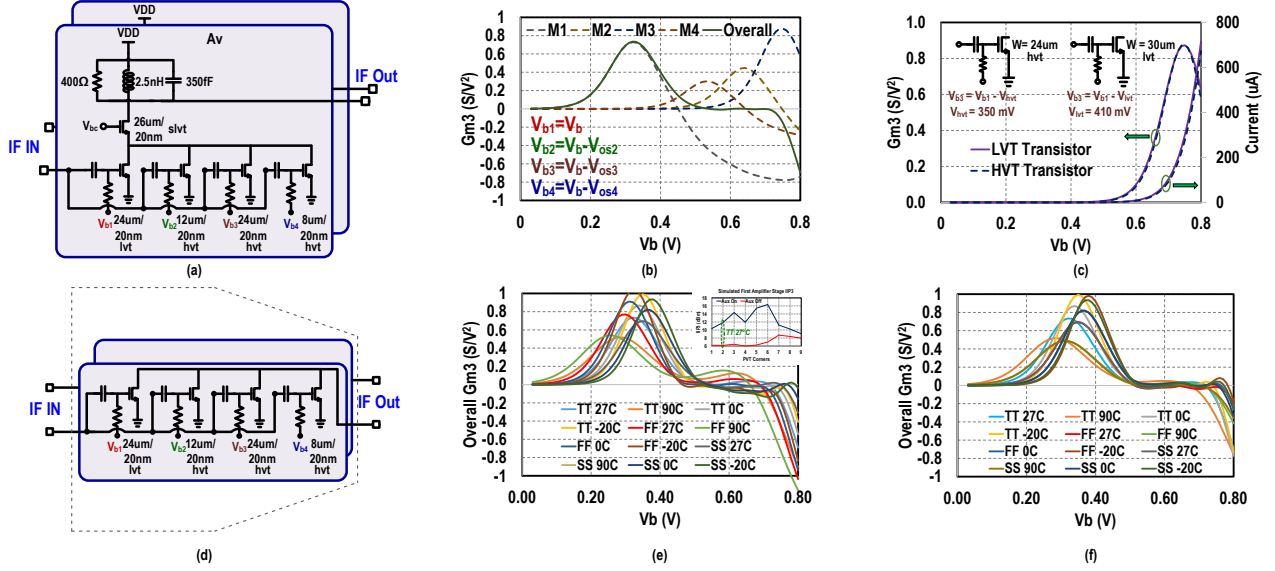


Figure 7: IF Section of the Front-End

(a) first gain stage, (b) gm_3 (second derivative of the transconductance), (c) gm_3 performance with different transistor flavors, (d) second gain stage, (e) gm_3 performance with different corners and temperature variations (IIP3 is shown in the small insert), (f) corrected gm_3 performance with different corners and temperature variations by slightly modifying the bias voltages.

The image rejection ratio (IRR) is calculated as the difference between the desired and image signals' gain. In this design, only two settings are chosen to cover the overall bandwidth (although using more than two setting regions can achieve higher performance in some frequency ranges). The final values chosen for the I and Q mixers' gate biases are 0.2V and 0.2V for the frequency range from 43 GHz to 73 GHz and 0.05V and 0.12V for the frequency range from 73 GHz to 97 GHz respectively.

3.3 Experimental Results

The ultra-wideband mixer-first front-end is fabricated in GlobalFoundries 22 nm CMOS FDSOI process and fully characterized using high frequency probes. All DC and biasing pads are wire-boned to the PCB. Some of the measurement setups are illustrated in Fig. 8. Signal generators are used to generate a continuous wave (CW) RF signal for the RF and LO ports. Since the signal generator cannot generate signals up to 100 GHz, different source modules (frequency extenders) are used across different frequency bands. For example, VDI WR15SGX module is used for the frequency range 50-75 GHz, VDI WR12SGX module is use for the frequency range 60-90GHz, and OML S10MS and Agilent 83558A modules are used for the frequency range 75-110 GHz. High frequency MPI probes (T110A-GSG100), with an attenuation of less than 1 dB up to 100 GHz, are used for the RF and LO signals for the whole frequency range (Fig. 8).

3.3.1 Gain, Image Rejection and Matching

A signal generator (E8257D-567) is used (along with the corresponding source module) to generate a continuous wave (CW) signal as an RF input to the chip for measuring the gain. The LO port is driven by another source module followed by a power amplifier to generate sufficient LO signal power. The chip frequency down-converts and amplifies the signal, then, the output signal frequency and power are measured using a signal analyzer (EXA-N9010A). The overall performance (Fig. 9) shows a state-of-the-art 3-dB gain bandwidth from 43 to 97 GHz (77.14% fractional bandwidth) with a peak gain of 15 dB. The gain versus frequency profile as measured at the IF output is shown in Fig. 9(a). The same setup is used to measure the image rejection capabilities of the chip. The desired followed by the image signals are used as the input to the chip and the output power difference is captured (Fig. 9(b)). As mentioned in Section I, only two settings are used to cover the whole bandwidth with image rejection ratio (IIR) of up to 32dB.

The matching performance is carried out using Anritsu 37397D VNA along with Anritsu transmission-reflection module at the RF port of the chip. The S11 is measured with the LO port of the chip both switched on and off and the results are shown in Fig. 9(b). The results indicate that the input matching using the coupled-line-coupler at the RF port is indeed resilient to the impedance presented to the coupled and through ports as can be observed by the good matching for both LO cases. The reason that the S11 (LO ON) not very smooth is because three different modules (and power amplifiers) are used to drive the LO signal at different frequency ranges causing some slight LO driving power differences. The intermodulation performance of the receiver front-end is characterized by measuring the input referred third order intercept point (IIP3). One way to generate the two RF tones required for testing the chip is to generate two IF tones and combine them in the IF domain then up convert the combined signal to the RF domain using up-conversion mixers. This method might impose some inaccuracy in the measurements due the low linearity of the available up conversion mixers specially at such high frequencies (~ -19 dBm OP1dB) which might dominate the non-linearity performance especially when measuring high linearity chips. Although this effect can be relaxed by using an RF amplifier following the mixer, the measurement setup used to characterize the chip adopts combining the two tones in the RF domain rather than the IF domain (Fig. 10). For example, in order to measure IIP3 at RF frequency at 75 GHz (with 3.8 GHz IF frequency), two signal generators followed by two source modules (VDI E-band module [60-90 GHz], and OML W-band module [75-110 GHz]) are used to generate two high frequency tones around 75 GHz frequency range, then power combiner (SWP-60390302-12-S1 [60-90 GHz]) is used for RF power combining. The output spectrum is observed using signal analyzer and the IIP3 value is calculated. Figure 11(c) shows the measured IIP3 versus two tone input separation with an in-band IIP3 of up to 5.2 dBm (in this measurement one tone is fixed at the center of the IF band and the other tone is frequency swept and the IM3 component closer to the first tone is used to calculate the IIP3). The IIP3 improves with two-tone frequency separation because of the increased attenuation the tones experience as they get out of the IF bandwidth. Figure 11(d) shows the output fundamental and IM3 components versus the input power. Finally, input compression point is measured with a setup similar to the gain measurement setup and the results are shown in Figure 11(b).

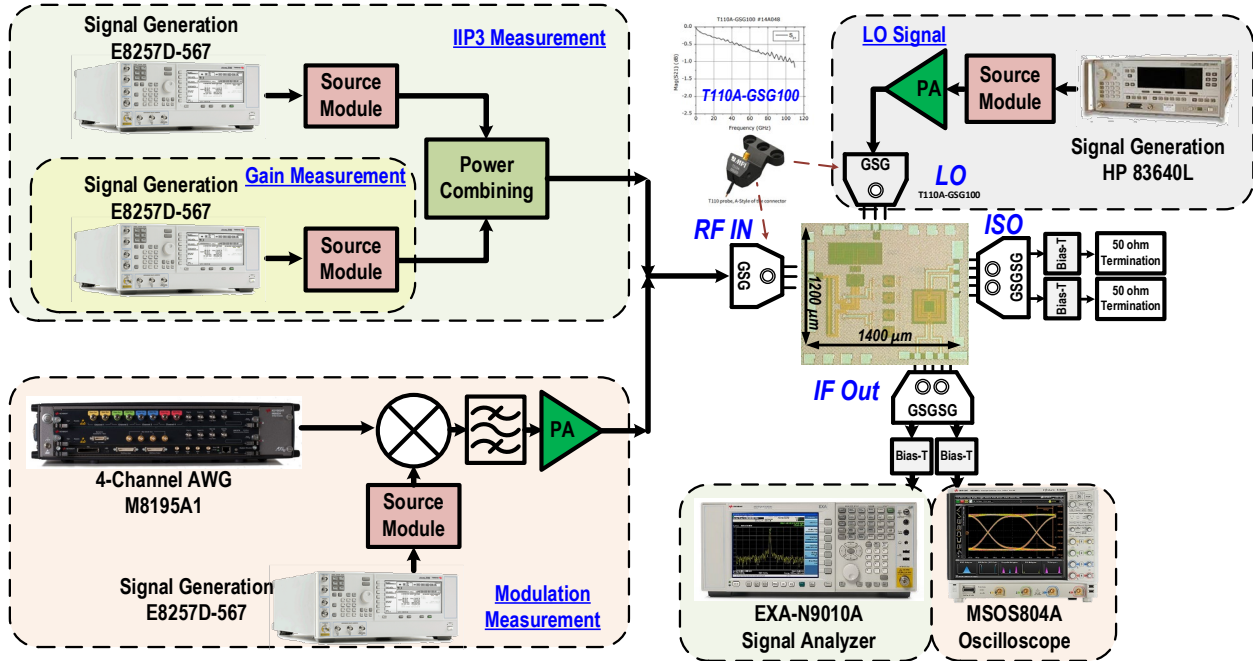


Figure 8: Different Measurement Setups used for Chip Characterization

Noise figure measurements are carried out using PXA signal analyzer (N9030A) with noise figure measurement capabilities and several noise sources for different frequency ranges. The noise sources used are Agilent (up to 50GHz), Quinstar QNS-FB15TV (50-75 GHz) and Quinstar QNS-FB12LW (75-110 GHz). The measurements show a noise figure performance between 12.5 to 16.5 dB across the frequency range (Fig. 11(b)). Simulations are carried out to investigate the noise figure after every stage of the frontend, this is shown in Fig. 12. After the CLC, the noise figure is equal to the noise of the coupler in addition to the noise contribution from the loading components. The noise figure of the coupler includes the coupler loss (Fig. 3) as well as the noise contribution of the resistance R_{ISO} . In this implementation R_{ISO} is 50 Ω , hence the noise figure of the coupler is theoretically limited to 3dB. After down conversion noise is added by the mixer switches in addition to folding of the image noise (and harmonics) to the desired frequency band. Next, the amplification stages add more noise, while after the image rejection operation, the folded image signal is rejected. In this implementation, the first stage amplifier has high noise contribution which can be enhanced in future implementations by reducing the number of auxiliary devices in the first stage and keeping 4 devices in the second stage to maintain linearity.

3.3.2 Modulation Testing

The implemented frontend supports high speed modulated signals (multi-Gbps data rate) required for future communication links. This is demonstrated by testing the chip with the modulation test setup shown in Fig. 8. The modulated signal is generated using an Arbitrary Waveform Generator (AWG) M8195A1 at low frequency (with an optional attenuator following the AWG), which is then upconverted to the desired RF frequency, bandpass filtered (to suppress the LO leakage and the up converted image signal) and finally amplified. This signal is applied as the input of the proposed frontend chip and the final output is demodulated using an

oscilloscope (MSOS804A). Figure 11(a) shows the demodulated signal's constellation and EVM performance for different bit error rates. The front-end is able to successfully frequency down convert and amplify 64QAM signals with data rates up to 6 Gbps with an EVM of better than -24.6dB. In addition to requiring high speed communication links, future EM environment will be congested and contested imposing a challenge on the frontend receivers to be able to successfully demodulate the desired signal in presence of blocker signals, especially in-band blockers with no out of band frequency rejection applied (blocker desensitization [31][44]). The case of large in-band blocker is demonstrated by applying the desired signal accompanied by an in-band blocker signal to the chip and demodulating the desired output signal. Figure 11(b) shows the EVM of the demodulated desired signal versus the relative input power level. The results show a successful demodulation even in a presence of blocker signal of up to 20 dBc and 0.3 GHz frequency offset from the desired signal.

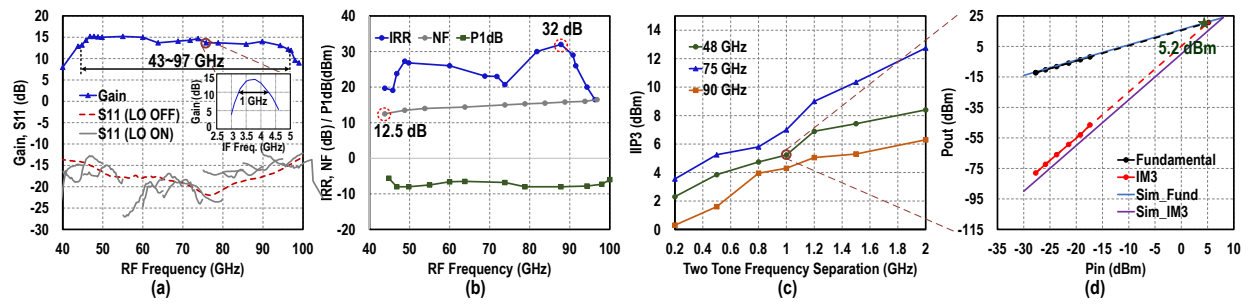


Figure 9: Measurement Results

(a) Gain and S11, (b) IRR, NF and P1dB, (c) IIP3 versus two tone separation, (d) fundamental and IM3 output versus input power

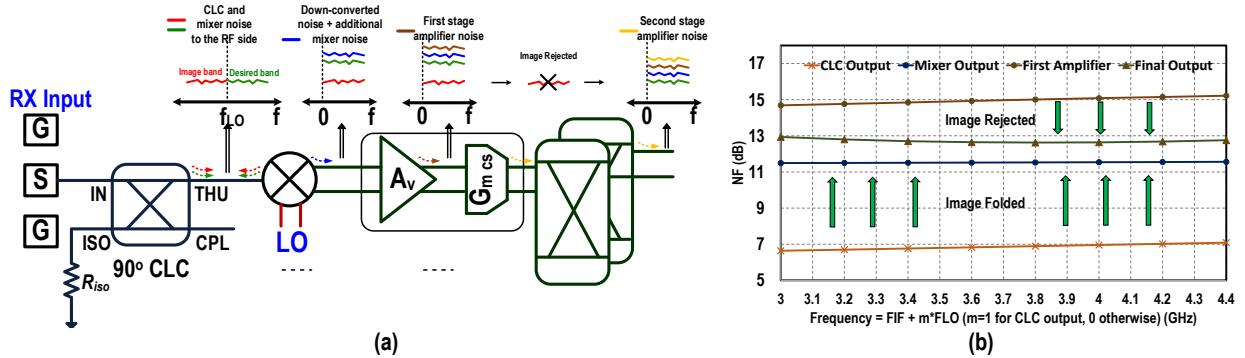


Figure 10: (a) Noise Contributors at Different nodes, (b) Simulated Noise Figure Across IF Frequency for LO Frequency of 70 GHz

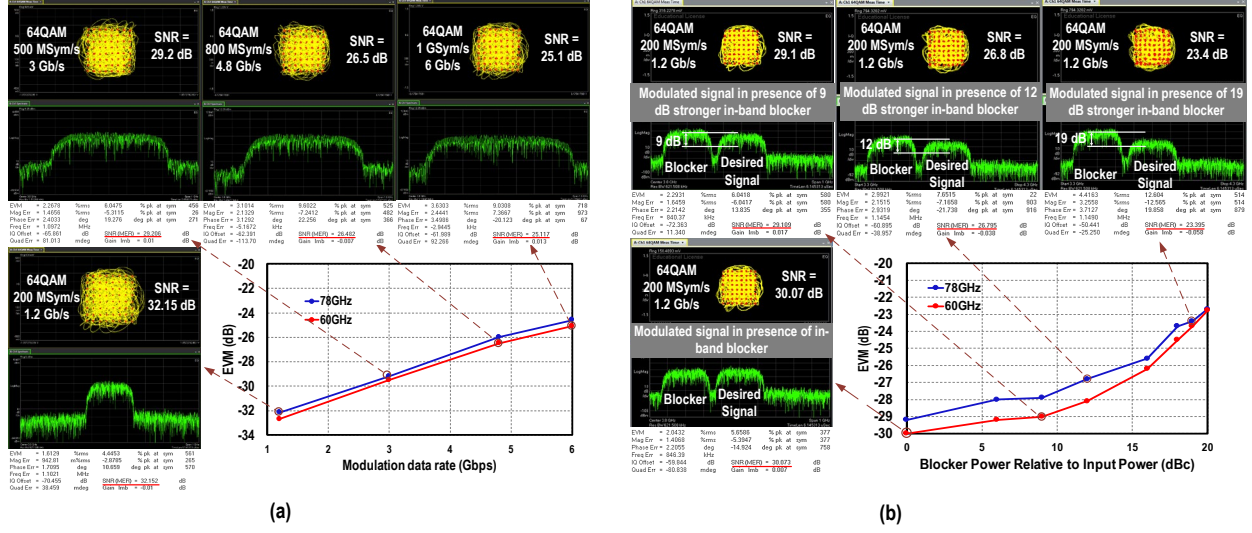


Figure 11: Modulation Performance

(a) for different data rates, (b) in the presence of blocker signal with an offset frequency of 0.3 GHz.

Table I Results Comparison with The State-of-The-Art

		CMOS Node	Center Freq. (GHz)	Operation Freq. (GHz) (Fractional BW %)	IIP3 (dBm)	Pin1dB (dBm)	Gain (dB)	NF _{dBSS} (dB)	Power (mW)	On chip image rejection (dB)	IF/Baseband BW (GHz)	Modulation	Architecture
Mixer	This Work	22nm FDX	70	43 ~ 97 (77.14%)	1.6 ~ 5.2 ⁴	-5.6 ~ -8	12~15	12.5 ~ 16.5	36	17~32	1	64QAM 1.2 to 6 Gbps (-32.7 to -24.6 dB) ⁵	Mixer-first low-IF down conversion
	L. Lotti [1-2] ISSCC '18 JSSC '20	28nm	84	74~94 (26.5%)	N/R	-26.5 ~ -18	21~26	8.2 ~ 10.8	8	N/A	1.5	N/R	Mixer-first direct conversion
	Moroni [3] RFIC '10	65nm	58	49 ~ 67 (31.0%)	N/R	-12	10-13	11 ~ 14	14	N/A	0.32	N/R	Mixer-first direct conversion
	Testa [45] EuMIC '19	22nm FDX	61	56~66 (16.4%)	N/R	-18	6.5	13.5 (SSB)	18	N/A	1	N/R	Inductorless down-conversion Mixer
LNA First Topology	Vigilante [5] JSSC '17	28nm	82.3	68.2~96.5 (34.4%)	-24 ~ -18 ¹	-28.1	29.6	6.4-8.2 ³	31.3	N/A	1.9	N/R	Sliding IF heterodyne
			81.1	65.8~ 96.5 (37.9%)	-18 ~ -12 ¹	-12.3	18	7.8-9.8 ³	11.7	N/A	1.9	N/R	
	Vigilant [7] ISSCC '18	28nm	75.1	68.85~81.75 (16.7%)	N/R	-25	28	8.3 ~ 10	77.3 ²	N/A	N/R	N/R	Coupled-RTWO-based subharmonic receiver
	Kundu [8] JSSC '15	45nm SOI	55.5	45~66 (37.8%)	N/R	-27	23.2-26.2	5.5 ~ 10 ¹	30	N/A	1.2	N/R	Active mixing direct conversion
			57.5	48~67 (33.0%)	N/R	-28	17.2-20.2	7.7 ~ 12 ¹	14	N/A	1.15	N/R	
	Khanpour [10] JSSC '08	65nm	83	75~91 (19%)	N/R	-16	13	5.5~7.5	89	N/A	9	N/R	Direct Conversion
	Guermandi [11] ISSCC '15	28nm	79	75~83 (10%)	N/R	-32.5	35	<7	59	N/A	>1	PMCW	Direct Conversion

NR: Not Reported, ¹ Estimated from figures, ² Receiver power, ³ Up to 90 GHz, ⁴ At 0.5GHz two tone offset, ⁵ With equalization

The overall result of the proposed ultra-wideband chip is compared with state-of-the-art high frequency CMOS designs and the comparison is shown in Table I. The proposed frontend achieves the highest carrier bandwidth (77.14% fractional bandwidth) amongst all CMOS ultrawide band designs. Additionally, the proposed design presents a state-of-the-art linearity performance achieving an IIP3 of 1.6dBm to 5.2dBm. Furthermore, on-chip image rejection capability is demonstrated by the proposed receiver frontend while not presented by any other

design. Besides, compared to state-of-the-art designs shown in Table I, this work is the only to demonstrate demodulation performance of the desired signal with and without the presence of large blocker signal.

4 MMWAVE 2D 2X2 RECEIVER WITH AUTONOMOUS SPATIAL FILTER AND BEAMFORMING

4.1 System Overview

A conventional uniform 2D phased array with a phase shifter on every element can steer the RX beam to an angle (θ_s, ϕ_s) by applying corresponding phase shifts to the elements according to the following equations:

$$a_{n,m} = e^{-j\vec{k} \cdot \vec{r}_{n,m}} = e^{-jk \sin(\theta_s)(nd \cos(\phi_s) + md \sin(\phi_s))} \quad (6)$$

where θ_s, ϕ_s are the signal incident angles. The array element spacing is assumed to be $\lambda/2$, where λ is the wavelength in the air. $a_{n,m}$ is the excitation of the element position at (n, m) in the array, k is the wavenumber and d represents the element spacing. Additionally, all the array elements are assumed to have the same amplitude weighting.

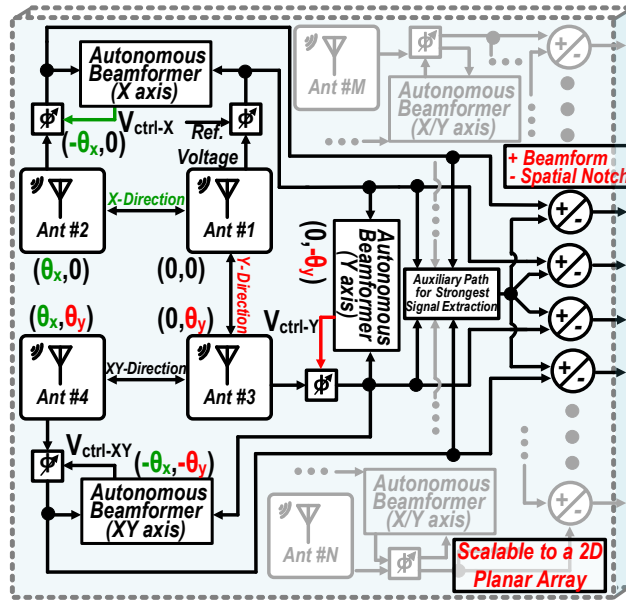


Figure 11: Operation Principle of the Proposed 2D MIMO RX Array

The array factor of a 2D $M \times N$ array is given as:

$$AF(\theta, \phi) = \sum_{n=0}^{N-1} \sum_{m=0}^{M-1} a_{n,m} e^{jk \sin(\theta_s)(nd \cos(\phi_s) + md \sin(\phi_s))} \quad (7)$$

Theoretically, to scan the 2D phased array to angle (θ_s, ϕ_s) , elements phase shifts $\theta_{n,m}$ is applied to each element according to the standard scanning equation:

$$\theta_{n,m} = nkd \sin(\theta_s) \cos(\phi_s) + mkd \sin(\theta_s) \sin(\phi_s) \quad (8)$$

where $n \times d$ and $m \times d$ are the x- and y-components of the vector from the $(n$ th, m th) element from the origin.

According to (6), in the 2D RX array, an incident wave can be decomposed into two orthogonal wavefronts in X and Y directions with an element-level phase difference of θ_x and θ_y . The received signal on this X-Y plane has a relative phase shift by the superposition of θ_x and θ_y . By properly adjusting the phase shift of individual elements, the 2D MIMO RX array can be steered to the direction with a maximized signal-to-noise ratio (SNR). However, large-scale look-up table based digital backend calculations are limited by array size because of the increasing complexity of the array architecture, accuracy, and latency.

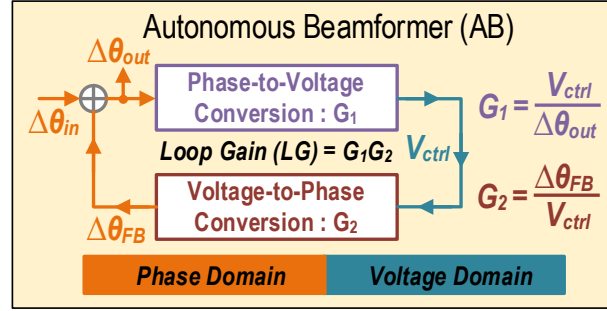


Figure 12: Autonomous Beamformer Operation Loop

To address the challenge of beam-alignment latency and accuracy, we propose a 2D 2×2 MIMO RX array (figure 12) with an autonomous beamformer and spatial filter. In the phased array system with the antenna on the $\lambda/2$ grid for minimum grating lobe levels, the progressive phase shift at each antenna/channel within the array can be calculated:

$$\Delta\theta_x = \pi \cdot \sin(\theta_s) \cos(\phi_s) \quad (9)$$

$$\Delta\theta_y = \pi \cdot \sin(\theta_s) \sin(\phi_s) \quad (10)$$

$$\Delta\theta_{xy} = \pi \cdot \sin(\theta_s) \cos(\phi_s) + \pi \cdot \sin(\theta_s) \sin(\phi_s) \quad (11)$$

To accurately achieve the corresponding phase shift (9)-(11) for each element, an autonomous beamformer (AB) with negative feedback is proposed in the system to provide the dynamic phase shifting to adjacent channels. The operation of the AB is explained in figure 13. The power-aware phase detector senses two phase mismatched signals and generates the corresponding DC control voltage (V_{ctrl}) with a gain of G_1 . Then V_{ctrl} is fed back into the phase shifter to generate the corresponding phase shift $\Delta\theta_{FB}$ with a gain of G_2 , and $\Delta\theta_{FB}$ is subtracted from the input signal to form a negative feedback loop. The residual output phase deviation $\Delta\theta_{out}$ can be expressed as

$$\Delta\theta_{out} = \Delta\theta_{in} / (1 + G_1 G_2). \quad (12)$$

With sufficient loop gain ($G_1 G_2$) and monotonic relationship between control voltage and phase shift, this phase-voltage domain negative feedback loop rapidly and autonomously aligns two varying incoming signals.

As it is shown in figure 12, the proposed system set the CH1 as the reference. An AB in two adjacent array elements (CH1 and CH2) detects the phase difference $\Delta\theta_X$ in the X-direction, and an AB in another two elements (CH1 and CH3) detects the phase difference $\Delta\theta_Y$ in the Y-direction. 2D autonomous beamforming requires two phase-domain negative feedback loops to independently track the two orthogonal plane wavefronts. Thus, the X-/Y-direction ABs generate

phase feedback DC control voltages V_{ctrl-X} and V_{ctrl-Y} . The control voltages are fed to their perspective phase shifters, such that CH1/CH2 are aligned to the X-direction plane wave-front, and CH1/CH3 are aligned to the Y-direction plane wave-front.

If all the circuits layout and the phase-shifters exhibit a fully identical/symmetrical and perfectly linear relationship between control voltage and phase shift, then CH4 (XY direction) can ideally be controlled $V_{ctrl-XY} = V_{ctrl-X} + V_{ctrl-Y}$ with analog open-loop computation by summing V_{ctrl-X} and V_{ctrl-Y} . In the [10][11], resistor voltage adder and multiplier are applied to generate feedback control voltage for the outer phased-array element with the assumption of fully symmetrical 1-D phased array architecture. However, in practical 2-D phased array architecture, the non-symmetrical system floorplan is inevitable. Moreover, in the real world's implementation, the phase shifter will demonstrate non-linear voltage-phase conversion, and the non-negligible phase shift error will be observed. To solve the abovementioned issues, an extra AB is included between CH3 and CH4. This additional phase-domain negative feedback loop autonomously aligns the phase between CH3 and CH4. Sequentially, CH4 is also phase-aligned to CH1 by leveraging the additional AB. Importantly, the control voltage $V_{ctrl-XY}$ for CH4 is dynamically aligned with reference channel CH1 due to high loop gain (12) and will not be affected by non-ideal effects.

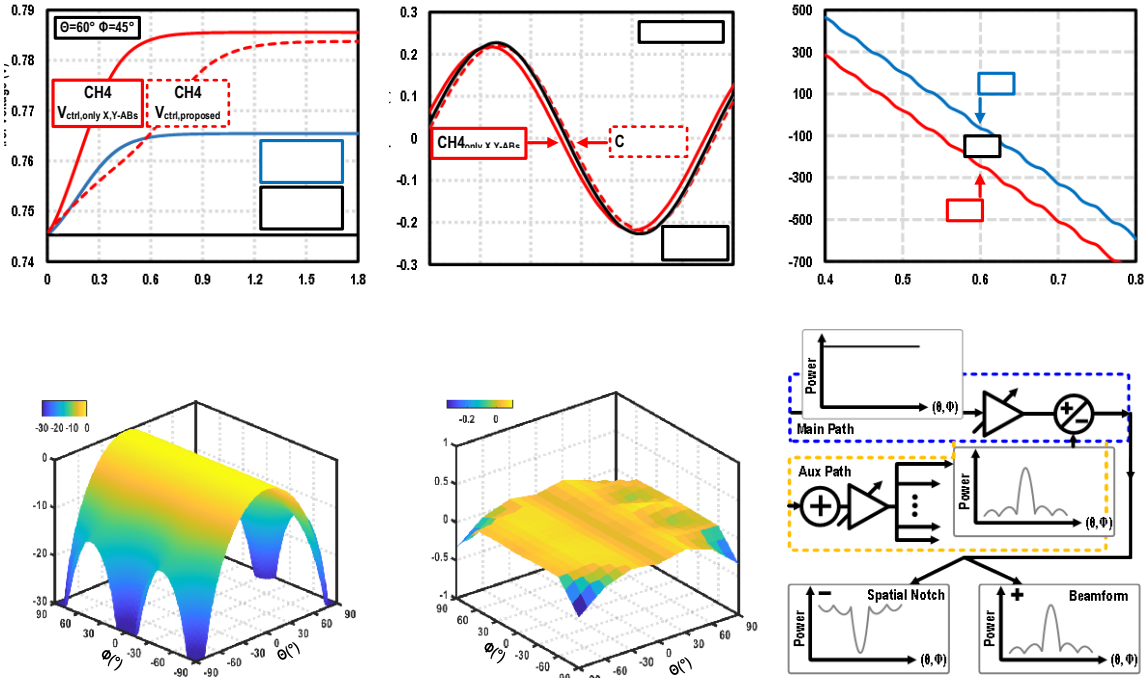


Figure 13 (a) Simulated Control Voltage Response between the System with Only 2-X/Y AB and Proposed System (b) Simulated Waveform for Only 2-X/Y AB and Proposed System (c) Simulated Phase Shift Response Regarding to Control Voltage (d) Simulated Normalized Array Factor for Conventional Phased System (e) Proposed System with AB showing Full FoV Functionality (f) Operation Principle for both AB and Autonomous Spatial Filter(ASF)

Figure 14(a) shows the simulated V_{ctrl} of four channels with receiving angles $\theta=60^\circ$ and $\Phi=45^\circ$. CH1 is the reference, so it stays constant. CH2/3 dynamically adjusts the V_{ctrl} based on the relative phase difference with respect to CH1. The red solid line in figure 14(a) describes the simulation using only two ABs in X-/Y-direction and the V_{ctrl} -XY for CH4 purely depends on analog open-loop computation. Due to the phase shifter non-linearity and system layout non-symmetry, there is a close 5-degree phase error compared to CH1-3 shown in figure 14(b). In our proposed system, an extra AB is connected between CH3 and CH4. Thus, the phase of CH4 will dynamically align to CH3 by the additional AB. As shown in figure 14(a), the red dashed line describes the behavior of V_{ctrl} -XY (for CH4) of the proposed system. V_{ctrl} -XY dynamically captures the phase information for X-/Y-direction. The phase error between CH4 and CH1-3 is smaller than 0.5 degrees in simulation as shown in figure 14(b). Figure 14(c) plots simulated the control voltage response of phase shifters. The simulated response shows non-linear voltage-to-phase conversion behavior.

Three ABs precisely align the phase of received signals in all channels. Figure 14(d) depicts the array factor of a 2D 2×2 RX array without element phase shifting and it's pointed to the broadside direction. After passing through the ABs, the four received signals are constructively combined with ~ 0 dB normalized array factor in FoV (figure 14(e)). Furthermore, the phase-aligned signal in each channel is split into two paths as shown in figure 12 and figure 14(f). An auxiliary (Aux.) path is introduced to sum all four channels together. This auxiliary path extracted signal provides the capability of beamforming of the strongest signal and other signals are suppressed due to the out-phase among channels. This extracted signal can be de-modulated at the baseband to verify if it's the desired signal or blocker. Moreover, the extracted strongest signal is feedforwarded to the main path in each channel (figure 14(f)). The combination of three ABs and the aux path is defined as a single-stage autonomous spatial filter (ASF). It is worth mentioning that more ASF stages can be further cascaded to handle multiple streams without having hardware overhead and high-power consumption.

Finally, our proposed 2D MIMO RX array with two ASF stages demonstrates an extremely fast response time which is suitable for mm-Wave 5G communications. Figure 15 depicts the system architecture of the entire proposed mm-Wave 2D MIMO RX array and different system operation modes. The broadband four-channel mm-Wave frontend with high image rejection is used to down-convert RF signals to IF frequencies. The aux path from each ASF stage can be extracted to verify if the received signal is desired or a blocker. Three different operation modes are introduced in this work. For Mode-I, only one unknown signal is received. In the first stage, ASF either beamforms the desired signal or spatial filters the blocker signal.

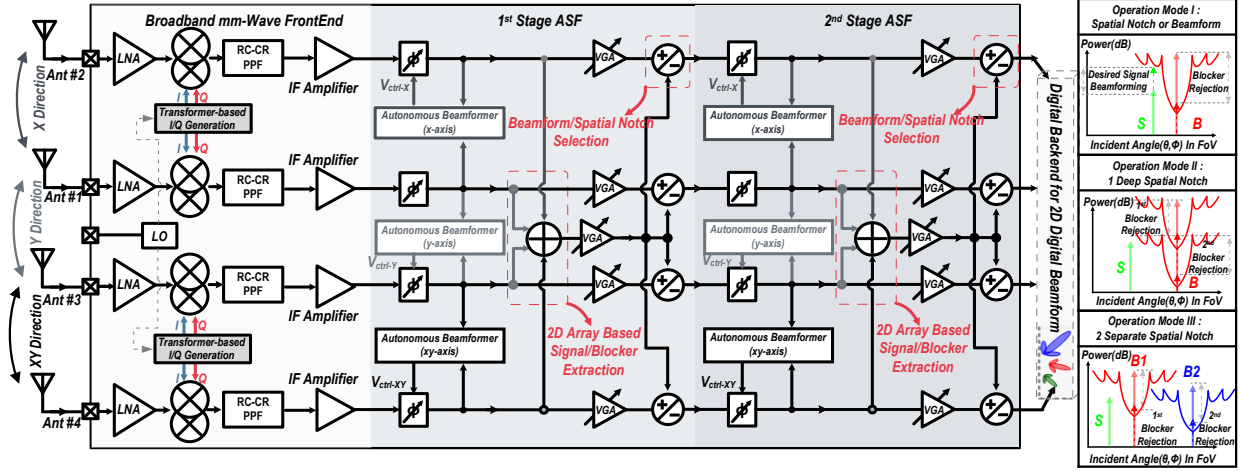


Figure 14: Block Diagram of the Proposed 2D MIMO RX Array with Both Autonomous Beamforming and Spatial Filtering Functionalities

In Mode-II, one large blocker is received. the 1st and 2nd ASF stages concurrently track this blocker and suppress it twice with a deep spatial notch. In Mode-III, two blockers with a similar power level are concurrently received. Two ASF stages sequentially suppress each blocker signal by two independent spatial notches.

It is worth mentioning that more 2D ASF stages can be cascaded to track more unknown signals/blockers depending on their received power levels and it can consequentially provide multiple spatial notches to blockers from various receiving angles or FoV autonomous beamforming. Thoracically, the proposed ASF stages can be designed and implemented with low DC power consumption, due to its non-linear phase-voltage loop gain which is shown in equations (14), (15), and (16).

4.1 Circuits Implementation

As a proof of concept, we implement a prototype design of an mm-Wave broadband 23-37GHz autonomous 2D MIMO RX array with two ASF stages in cascade for multi-beam spatial filtering and independent beam-steering. The proposed 2D RX array is designed and implemented in 45nm CMOS RF SOI with a 5.74×3.2 mm² area. Detailed circuit implementations for the broadband mm-Wave RX frontend, the proposed AB, and the following ASF stages are discussed and analyzed.

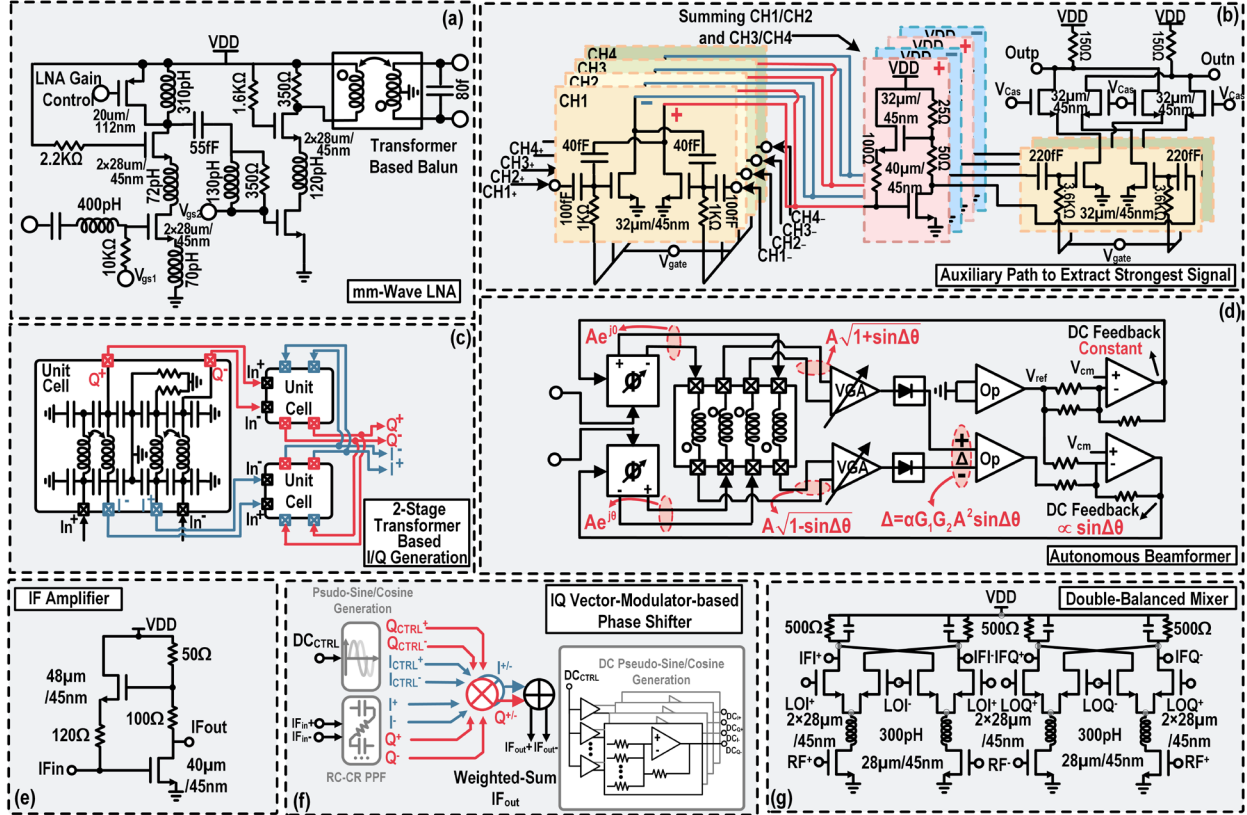


Figure 15 (a) Detailed Circuits Schematics of mm-Wave LNA (b) Detailed Circuits Schematics of Auxiliary Path to Extract the Strongest Signal (c) Detailed Block Diagram of Implemented 2-Stage Transformer Based I/Q Generation Circuits (d) Detailed Block Diagram of Implemented Autonomous Beamformer (e) Detailed Circuits Schematic of IF Amplifier (f) Detailed Block Diagram of Phase Shifter (g) Detailed Circuits Schematics of Doubly-Balanced Mixer

4.1.1 Broadband mm-Wave Receiver Frontend

The wideband MIMO RX frontend consists of mm-Wave broadband tunable low noise amplifiers (LNA)s and active mixers to achieve low noise figure and tunable gain for linearity improvement. The Hartley Image-Rejection RX architecture with LO I/Q generation and IF I/Q combining is chosen since the active mixer CG is less sensitive to LO driving amplitude mismatch [3][7][12][16]. The two-stage transformer-based I/Q generation network generates high-precision I/Q from 20-50GHz for mm-Wave LO generation. Additionally, to achieve a wideband image rejection ratio, a two-stage IF 2-5GHz RC-CR polyphase filter is chosen for image rejection IQ combining.

A two-stage LNA with wideband resonance loads is designed for providing broadband performance as shown in figure 16(a). The simulated standalone LNA achieves 25–40GHz 3-dB bandwidth and 3.1–4.2dB noise figure. The source degeneration technique is leveraged to optimize for both wideband noise and input matching. The two-stage LNA is simulated with a different gain setting for different practical receiving scenarios with linearity consideration. The

PMOS switch is properly designed and placed at the first-stage load for gain and noise figure trade-off. An output transformer-based balun absorbs the loading effect from following the differential I/Q double-balanced mixers and serves as a balanced differential signal generation.

The mm-Wave transformer-based I/Q network is designed to convert one differential LO input to two balanced well-matched differential I/Q LO outputs with compact size and low loss over an extremely wide bandwidth. The proposed transformer-based I/Q network is designed based on a two-stage cascaded self-similar 90° hybrid coupler as a one-inductor-footprint I/Q transformer. The phase/amplitude mismatch is highly suppressed by cascading multiple stages of transformer-based 90° hybrid coupler units. A proof-of-concept two-stage transformer-based I/Q is proposed to achieve high-accuracy I/Q generation over 20–50 GHz.

4.1.2 Autonomous Beamformer

The conceptual diagram of the AB stage is shown in Fig. 13. The circuit implementation (figure 16(d)) and more detailed theory of the AB are discussed in this sub-section. It ideally consists of two parts. The first part is converting phase-to-voltage (G_1). It detects the phase difference between adjacent channels and converts any phase mismatch into voltage. The second part of the AB is the voltage-to-phase (G_2) circuits. The circuit is able to read out the voltage information and delays the phase of the signals accordingly. In our proposed 2D 2×2 RX MIMO array, three ABs are placed between four adjacent channels to create three phase-voltage domain negative feedback loops as discussed in section II. For the implementation of G_1 , we implement a 2-5GHz differential 90° transformer low-loss coupler, IF VGAs, and high-order stage Dickson voltage rectifiers. The behavior of the phase-to-voltage converter can be explained by applying two RF incident signals with identical amplitude A and the phase difference $\Delta\theta_{out}$ into input and isolation ports of the 90° coupler. Based on the S-parameters matrix of the 90° coupler, we can further derive that the voltage amplitude of output signals at the thru and couple ports is a function of $\Delta\theta_{out}$ and gain α . α is determined by coupler loss and IF VGAs. Furthermore, after rectifying by the Dickson rectifiers with rectification efficiency β , the differential DC feedback voltage output is the following:

$$V_{ctrl} = V_{DC,thru} - V_{DC,couple} = 2\alpha^2\beta A^2 \sin \Delta\theta_{out} \quad (13)$$

By dividing V_{ctrl} by $\Delta\theta_{out}$, we can derive the G_1 mentioned in Fig.3.

$$G_1 = V_{ctrl}/\Delta\theta_{out} = 2\alpha^2\beta A^2 \sin \Delta\theta_{out} / \Delta\theta_{out} \quad (14)$$

This design leverages high gain IF VGA and high output load impedance at rectifiers for generating high V_{ctrl} and boosts the overall G_1 and loop gain over the full 2D FoV. Since the proposed receiver array is place within $\lambda/2$ grid, progressive phase shift $\Delta\theta_{in}$ between each adjacent channels are confined within $\pm 180^\circ$. Therefore, G_1 is sinc function with its peak at $\Delta\theta_{out} = 0^\circ$ and gradually decreases when $\Delta\theta_{out}$ approaches $\pm 180^\circ$.

After generating the feedback DC voltage V_{ctrl} , V_{ctrl} is sent back to the wideband vector modulation phase shifter. The feedback DC V_{ctrl} is firstly sensed by the DC pseudo-Sine/-Cosine generation circuit and then the DC pseudo-Sine/-Cosine generation circuit generates the corresponding I/Q control voltage for the differential I/Q vector modulator. The I/Q vector modulator generates compensation phase shift $\Delta\theta_{FB}$ accordingly based on the DC feedback voltage V_{ctrl} . Thus, we can list the corresponding equations:

$$G_2 = \Delta\theta_{FB}/V_{ctrl} \quad (15)$$

4.1.3 Negative Feedback Loop of Autonomous Beamformer

Based on G_1 and G_2 , we can further derive the loop equation of the AB as shown in figure 12. With the phase difference $\Delta\theta_{out}$ two adjacent channels,

$$\Delta\theta_{out} = \Delta\theta_{in} - \Delta\theta_{FB} = \Delta\theta_{in}/(1 + G_1 G_2) \quad (16)$$

Equation (16) elaborates on the behavior of the negative feedback loop for achieving two adjacent channels' phase alignment. With a high loop gain $G_1 G_2$, the residue phase $\Delta\theta_{out}$ can be fully canceled by the negative feedback behavior. Even in the end-fire case, the proposed AB can still maintain its large loop gain value by properly designing $G_1 G_2$. This essentially proves the 2D full-FoV phase alignment. The combination of three ABs and the Aux. path (figure 16) can be further built as a single-stage ASF. The close loop performance of the proposed beamformer can be analyzed as the following. Since the output phase error can be expressed as:

$$\Delta\theta_{out} = \frac{\Delta\theta_{in}}{1 + G_1 G_2} = \frac{\Delta\theta_{in}}{1 + \left(\frac{2\alpha\beta^2 A^2 \sin \Delta\theta_{out}}{\Delta\theta_{out}} \right) G_2} \quad (17)$$

It can be further simplified as the following:

$$\Delta\theta_{out} + k \cdot \sin \Delta\theta_{out} = \theta_{in} \quad (18)$$

where $k = 2\alpha\beta^2 A^2 G_2$. Since k is in a quadratic relationship with the input RF amplitude, this gain indicated the loop response as a function of input power. For $-180^\circ < \theta_{in} < 180^\circ$, $\Delta\theta_{out}$ has a one-to-one mapping to θ_{in} values, which results in non-zero loop gain, and autonomous beamforming is in operation. However, for $\theta_{in} = \pm 180^\circ$, equation (18) has a trivial solution, where the loop gain is zero regardless of the value of k , and the autonomous beamforming operation is stopped. For k less than 1, (18) never exceeds $\pm 180^\circ$, therefore there is only one solution for $\theta_{in} = \pm 180^\circ$ is $\Delta\theta_{out} = \pm 180^\circ$. However, when k exceeds 1, (18) has two trivial solutions. One is at $\Delta\theta_{out} = \pm 180^\circ$ and another is at $\Delta\theta_{out} < |\pm 180^\circ|$. A perturbation analysis can be performed to analyze the stability of the two possible solutions. For $\Delta\theta_{out} < |\pm 180^\circ|$, assuming there exists a small perturbation $\delta\theta$, such that $\theta_{in} = 180^\circ - \delta\theta$. Due to the negative feedback loop, $\Delta\theta_{out}$ will be forced to become smaller, and the autonomous beamforming loop is in operation. Therefore, this solution is stable. For $\theta_{in} = |\pm 180^\circ|$, $\Delta\theta_{out}$ will move to exceed 180 degrees region. Therefore, this is not a stable solution. Therefore, there exists one and only stable solution when $k > 1$.

4.2 Experimental Results

As a proof of concept, we demonstrated a broadband mm-Wave 23-37GHz autonomous 2D MIMO RX array with two ASF stages in cascade for multi-beam spatial filtering and independent beam steering.

Four-channel continuous-wave (CW) and modulated IF signals with variable phase and amplitude are synthesized by the Keysight arbitrary wave generator (AWG) 8195A to mimic the received signals with different incident angles. Then, the signals are up-converted to mm-Wave frequency using off-chip mixers. These signals generated by AWG can be programmed to mimic the multiple

signals and blockers concurrently injected into the proposed 2D MIMO RX array chip. For characterizing the CW results of the proposed design, Keysight spectrum analyzer UXA is used. All the connected cables used are matched cables to minimize both amplitude and phase errors. The Keysight oscilloscope MSOS804A is applied for high-speed de-modulation testing for different EM scenarios and loop response time testing of AB characterization. All the measurements including CW and modulations are based on-probe testing.

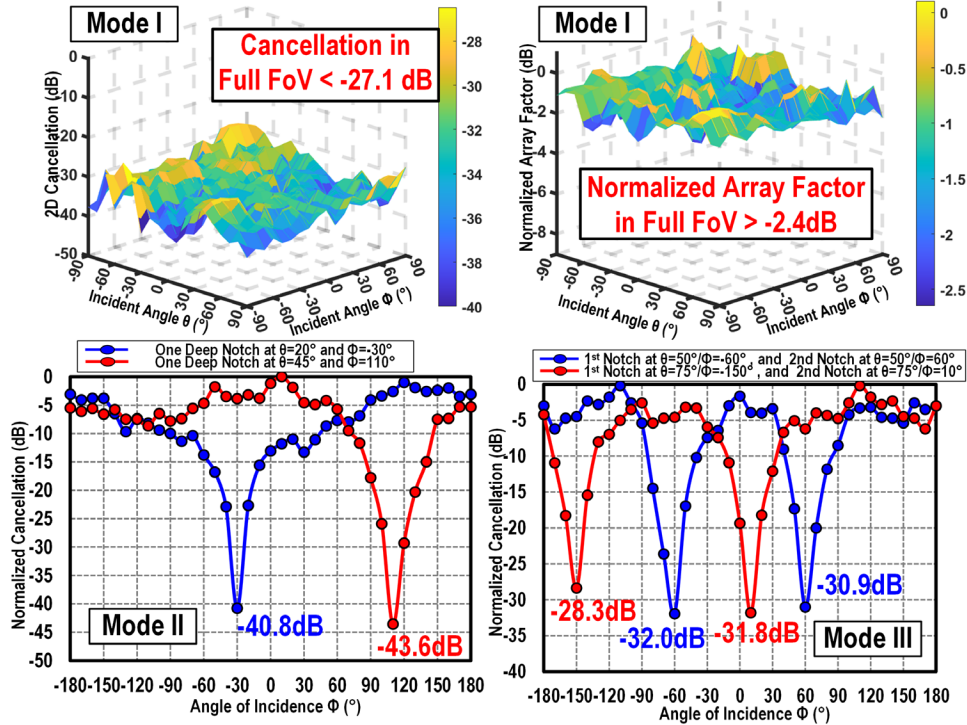


Figure 16 Measured Three Mode Operations of the Proposed 2D 2x2 MIMO Rx Array
Mode I: single-stage ASFs for autonomous spatial rejection on one dominant blocker or single-stage ASFs for beamforming on one desired signal. Mode II: Two-stages of ASFs for autonomous spatial rejection on one strong blocker for a deep notch. Mode III: 1st-stage ASF for autonomous spatial rejection of one blocker and 2nd-stage ASF for autonomous spatial rejection of second blocker

Autonomous beamforming and spatial notching measurements are tested by the on-chip 2-stage ASF without any external phase control and are shown in figure 17. We test the 2D MIMO RX array in several operation modes. For Mode-I, we characterize the performance of a single-stage ASF which can perform autonomous beamforming and spatial notching. Using only one single-stage ASF, a 27.1-to-39.9dB spatial blocker notching is achieved over the entire FoV. The one-stage ASF can also perform autonomous beamforming on the desired signal with a flat normalized array factor >-2.4 dB over the full FoV.

In Mode-II with one large blocker, the 1st and 2nd ASF stages concurrently track the blocker and suppress the blocker signal twice with a single deep spatial notch. We verify the functionality of multiple spatial notches with two different incident signals from $\theta=20^\circ/\Phi=30^\circ$

and $\theta=45^\circ / \Phi=110^\circ$, respectively. With the two-stage ASF performing as a spatial filter, the proposed system achieves -40.8dB and -43.6 dB deep spatial notch.

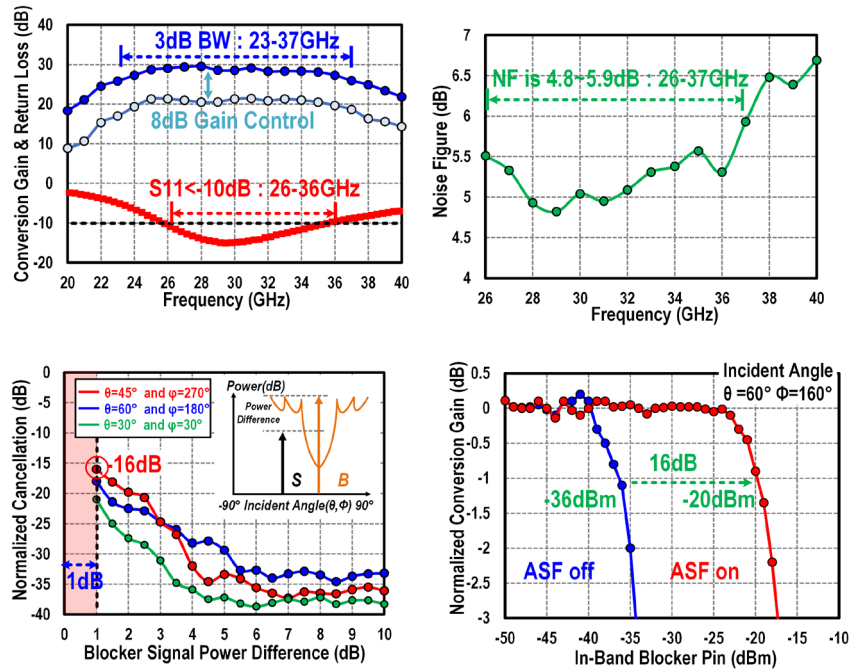


Figure 17 Measured Wideband RX Array Element Conversion Gain (CG), Input Matching S11, Noise Figure NF, Autonomous Spatial Discrimination of Concurrently Received Two-Tones Down to 1dB Power Difference for Different Incident Angles (the Stronger Tone is Automatically Identified by the Power-Aware Phase Detector in ASF and Subsequently Rejected), and In-band Blocker Pin1dB with the 1st-stage Spatial ASF being Turned on or Off

In Mode-III where two blockers with a similar power level are concurrently generated and received, the two ASF stages sequentially suppress each by two independent spatial notches. With two received blockers from both $\theta=50^\circ / \Phi=60^\circ$ and $\theta=50^\circ / \Phi=-60^\circ$, the two ASF stages suppress each by two independent spatial notches with a 32dB and 30.9dB cancellation. With two received blockers from both $\theta=75^\circ / \Phi=-150^\circ$ and $\theta=75^\circ / \Phi=10^\circ$, the two ASF stages suppress each blocker by two independent spatial notches with a 28.3dB and 31.8dB cancellation. Besides, cascading M ASF stages allows autonomous spatial suppression of M blockers, but front-end suppression of 1-2 major blockers is sufficient for practical mm-Wave digital arrays.

As shown in figure 18, the implemented autonomous 2D MIMO RX array demonstrates 23-to-37GHz wideband operation, 29.5dB conversion gain (CG) with 8dB gain control, and 4.8-to-5.9dB NF with 2-stage ASFs for spatial filtering to support mm-Wave multiband MIMO operations (figure 18). When the 1st ASF stage is on to perform spatial filtering, the measured in-band blocker $P_{in,1dB}$ achieves 16dB enhancement with 29.5dB conversion gain. When two spatial co-channel tones are concurrently received, as long as the two tones have ≥ 1 dB power difference, the Autonomous Beamformer can accurately discriminate the stronger one and achieve ≥ 16 dB suppression.

The implemented RX is also measured using concurrent multiple wideband modulated co-channel blockers and one desired signal (-47dBm) with different overlapping case (figure 19). All the desired signals and blockers are independently modulated, and various blocker/desired signal power level differences are assigned (3dBc to 5dBc) to produce a practical MIMO environment. With the 2-stage ASFs for spatial filtering, wideband modulated blockers are autonomously rejected, and the desired signal is successfully demodulated for 1.2Gb/s 64QAM with -26.16dB EVM_{rms} (25% spectrum overlap). The desired signal is swept across the incident angle Φ while maintaining the same incident angle θ . The desired signal is successfully demodulated until the difference between the incident angle Φ of the blocker and that of the desired signal is 25° (0.6GB/s 64QAM) and 30° (1.2GB/s 64QAM).

The proposed design with the 2-stage ASFs for performing spatial filtering also successfully rejects the wideband modulated blockers are demodulated the desired signal with 2.4Gb/s 64QAM (high speed) and -22.02dB EVM_{rms} (25% spectrum overlap) as shown in figure 20.

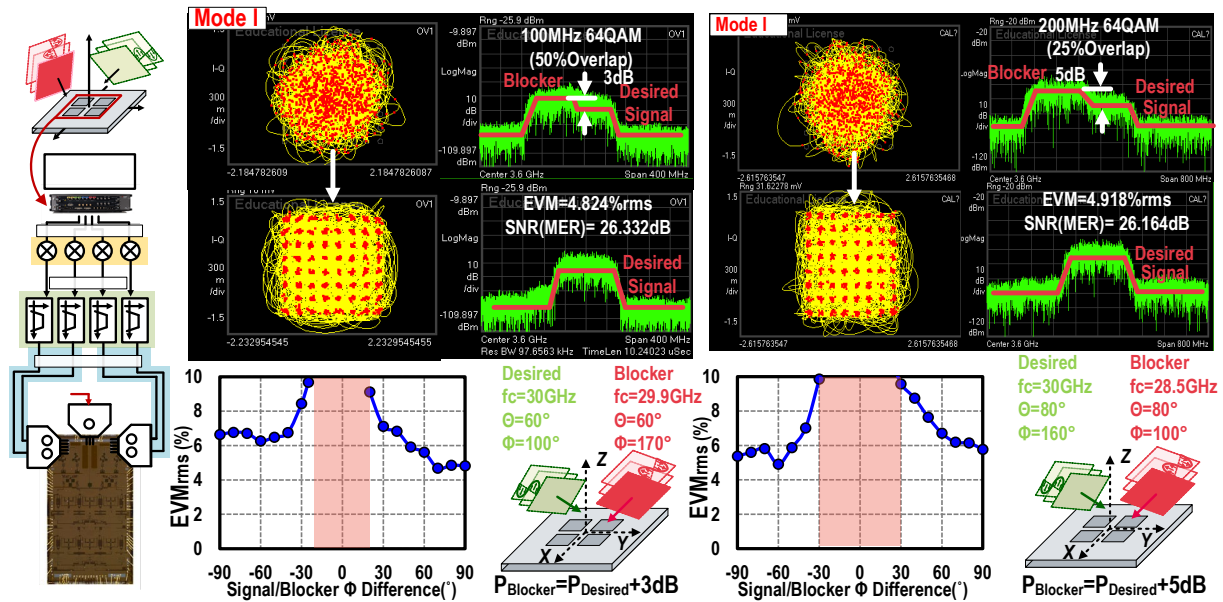


Figure 18 The Implemented mm-Wave RX MIMO Array with 2-stage ASFs Demonstrate Concurrent Autonomous Rejection of Blockers and Automatic Desired Signal Beamforming
The blockers and desired signal are co-channel with the same broadband modulation and data-rate, demonstrating successful receiving of the desired signal after autonomous spatial suppression of one spatial blocker. First test uses 100MHz 64QAM complex modulated signals and 50% overlapping on desired signal and blocker. Second test uses 200MHz 64QAM complex modulated signals and 25% overlapping on desired signal and blocker.

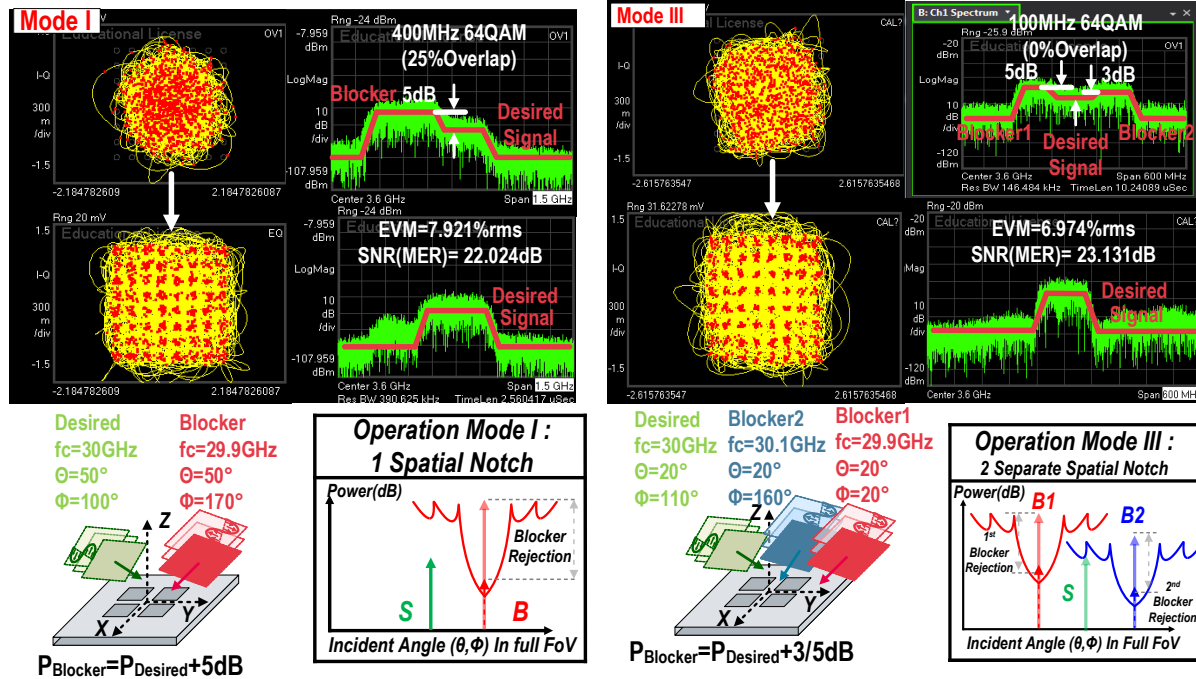


Figure 19 The mm-Wave RX MIMO Array with 2-stage ASFs Demonstrate Concurrent Autonomous Rejection of Blockers and Automatic Desired Signal Beamforming (the Blockers and Desired Signal are Co-channel with the Same Broadband Modulation and data-rate), Demonstrating Successful Receiving of the Desired Signal after Autonomous Spatial Suppression of One Spatial Blocker

First test uses 400MHz (high speed) 64QAM complex modulated signals and 25% overlapping on desired signal/blockers. Second test uses 100MHz 64QAM complex modulated signals and no overlapping on desired signal and two blockers.

Furthermore, the case with two different blockers is also measured. With the 2-stage ASFs for performing spatial filtering, wideband modulated blockers are autonomously rejected, and the desired signal is demodulated for 0.6Gb/s 64QAM with -22.13dB EVMrms (0% spectrum overlap).

We measured the response time of the autonomous beamformer using Keysight oscilloscope MSOS804A. With the received signal at $\theta=60^\circ$ and $\Phi=75^\circ$, we captured the closed-loop response time of the ASF with only $8.21\mu\text{s}$ as shown in figure 21. Due to the process variations and practical chip packaging issues, we capture the relatively slow response time compared to simulation, but it still sufficiently demonstrates the ultra-low latency for 2D MIMO RX array with autonomous beamforming and spatial filtering functionality. This is $>100\times$ faster than the existing DSP-controlled beamformers and it's suitable for next-generation mm-Wave wireless link applications. Moreover, the DC power consumption and chip area breakdown are also shown in Fig. 13, showing substantial low DC power consumption of the RF frontend and 2 cascaded ASF stages compared to power-hungry ADC. with wideband width for achieving high dynamic range. The chip area for each ASF stage is compact for large array scalability.

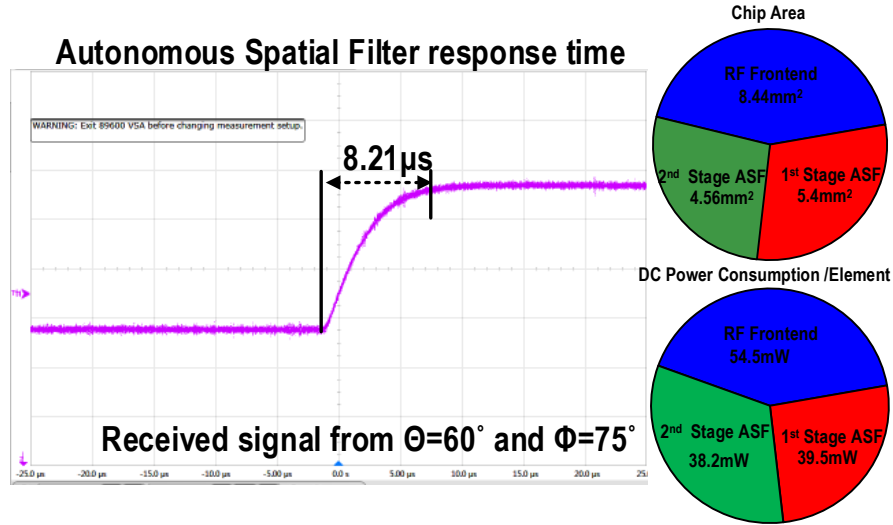


Figure 20 Measured Closed-loop Response Time of the Autonomous Spatial Filter using a Real-time Oscilloscope and Breakdown of DC Power Consumption/per element and Chip Area

Table II Results Comparison with The State-Of-The-Art

	This Work	Zhang JSSC 2017	Dunworth ISSCC 2018	Huang JSSC 2019	Pang ISSCC 2019	Huang TMTT 2019	Garg ISSCC 2020	Zhang ISSCC 2022
Technology	45nm CMOS SOI	65nm CMOS	28nm CMOS	45nm CMOS SOI	65nm CMOS	0.13μm SiGe	65nm CMOS	40nm CMOS
Frequency (GHz)	23-37	0.1-3.1	25-30.5	27-41	26.5-29.5	22-30	28	23-29
# of Inputs / Outputs	4 / 4 (2x2 2D Array)	4 / 4	24 / 2	4 / 4	8 / 2	8 / 2	4 / 1	4 / 4
Single Element Conversion Gain (dB)	29.5	43	34	36	11	33	>16	30
NF DSB,eq(dB) ¹	4.8-5.9	3.4-5.8	4.4-4.8	4.3-6.3	4.2	4.2-6.3	6-7.8	4.8
Spatial Blocker Rejection	2x2 4-Element 2-D Array-Based Frontend with Closed Loop Spatial Filter	Open Loop with Backend DSP	Open Loop with Backend DSP	4-Element Closed Loop with ASF	Open Loop with Backend DSP	2-Element Closed Loop with SSA Front-End BFs	Single-Wire Frequency Domain Multiplex	4-Element Closed Loop Notch Steer
Beamforming	2x2 4-Element Array-Based Frontend with Closed Loop Beamformer	Open Loop with Backend DSP	Open Loop with Backend DSP	4-Element Array-Based Frontend Closed Loop Beamformer	Open Loop with Backend DSP	2-Element Closed Loop with SSA Front-End BFs	Single-Wire Frequency Domain Multiplex	4-Element Closed Loop Notch Steer
Spatial Blocker Suppression Dimension	2D	2D	1D	1D	1D	1D	2D	1D
Spatial Blocker Suppression (dB) 1-/ 2-/ 3 Notches (dB)	43.6 / 39.9 / No	56 / 48.6 / 41.8	N/A	62 / 50 / 51	N/A	51 / 41 / No	37 / No / No	40 (IF)/35 (RF)
Blocker Modulation Scheme	0.6Gb/s 64-QAM and 2.4Gb/s 64-QAM	CW	N/A	3Gb/s 64-QAM and 0.8Gb/s 256-QAM	N/A	3Gb/s 64-QAM and 0.8Gb/s 256-QAM	*0.4Gb/s 16-QAM	0.6Gb/s 64-QAM
Desired Modulation Scheme	0.6Gb/s 64-QAM and 2.4Gb/s 64-QAM	*2Mb/s QPSK	*2.4Gb/s 64-QAM	3Gb/s 64-QAM and 0.8Gb/s 256-QAM	*6.4Gb/s 256-QAM	3Gb/s 64-QAM and 0.8Gb/s 256-QAM	*0.4Gb/s 16-QAM	0.6Gb/s 64-QAM
EVM of Desired Signal After Blocker Rejection	0.6Gb/s 64-QAM : 4.8% 2.4Gb/s 64-QAM : 7.9%	*2Mb/s QPSK : 20.5%	N/A	1.2Gb/s 64-QAM : 2.3% 3Gb/s 64-QAM : 3.7%	N/A	0.6Gb/s 64-QAM : 3.2% 3Gb/s 64-QAM : 4.7%	*0.4Gb/s 16-QAM : 5.96%	0.6Gb/s 64-QAM : 4.02%
Over the Air Measurement	No	Yes	Yes	No	Yes	No	Yes	No
Response Time	8.21 μs	NR	NR	1.47 μs	NR	< 1 μs	NR	NR
Power Consumption per Element (mW)	Frontend: 77.88/54.5 ^{2,3} 1st-Stage ASF: 54.75/39.5 ^{2,3} 2nd-Stage ASF: 67.65/38.2 ^{2,3}	28.5-36.75	42.5	70-85	112	70	112.5	56.1
Area (mm ²)	18.4	2.25	29 ⁴	23.4	12	21.6	10.6	2.8

NR: Not reported. * Far-field Measurement.

1. Equivalent Single-Element $NF_{DSB,eq} = NF_{DSB}$ measured with single-element excitation and output beamforming - log(number of elements).

2. DC Power consumption with 1.2V/1V supply voltage.

3. In contrast, a reported ADC DC power is 4.1 W for wideband ADC BW (200MHz), broadband carrier frequency (0.4-6GHz), and high dynamic range (71dB SNR) [6]. Therefore, enabling the front-end ASF suppresses the spatial blocker, relaxes required ADC dynamic range by >30dB, and substantially saves the ADC and total system power consumption.

4. It includes its T/R switches and Transmitter design.

Table II compares the proposed broadband mm-Wave MIMO RX array with state-of-the-art designs. By applying the proposed N-input–N-output cascaded multistage array-based autonomous beamforming MIMO architecture with spatial filtering functionality, the RX array demonstrates a full FoV operation with low-latency μ s response time per ASF stage and achieves state-of-the-art wideband modulated multi-Gb/s array-based high-order blocker rejection and

signal beamforming. Furthermore, by leveraging the multi-AB loops for both X-Y directions, the proposed work firstly demonstrates the autonomous beamforming/spatial filtering array can fully cover 2D FoV with low hardware complexity and dc power consumption.

In conclusion, this paper presents the world's first 2D scalable MIMO RX array with autonomous spatial filtering and individual beamforming functionality. The proposed work successfully implemented and demonstrated the RX system that can autonomously spatially filter out interferences and beamform desired signals without losing MIMO capability. Moreover, the proposed system is verified by 64-QAM co-channel modulation signal rejection and successfully demodulate Gb/s wideband signal supporting future mm-wave applications which are operating in complex and dynamic EM environment.

5 A TIME-MODULATED CONCURRENT STEERABLE MULTI-BEAM MIMO RECEIVER ARRAY WITH SPECTRAL-SPATIAL MAPPING USING ONE BEAMFORMER AND SINGLE-WIRE INTERFACE

5.1 System Overview

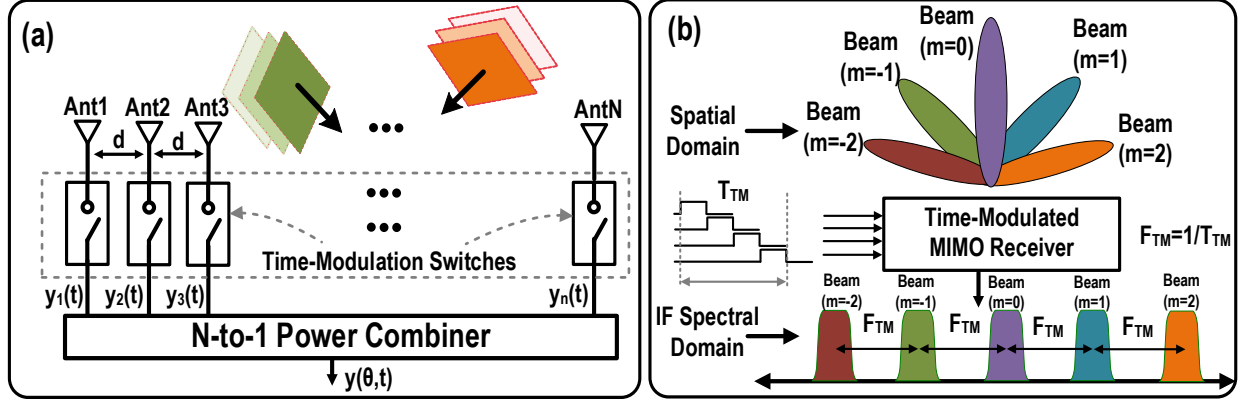


Figure 21 Operation Principle of the Proposed TM Spectral-spatial Mapping MB-MIMO RX Array

Figure 22(a) summarizes the basic TMA operation mode that is introduced in [44], [45] and [46]. For further understanding, a detailed derivation and discussion are presented here. Consider a 1-dimensional (1-D) TM linear array with N isotropic antenna elements with an element-to-element spacing “ d ” as shown in figure 22(a). The elements are labeled from 1 to N . The incident signals are assumed to be far-field plane-waves. Conceptually, a high-speed single-pole-single-throw (SPST) switch is connected to each array element with on-off switching. This “on-off time-modulation” is achieved by controlling the conduction time of each SPST switch in each TM sequence. The time-modulation sequence of the n^{th} SPST switch in Fig. 2 can be expressed as:

$$a_n(t) = \begin{cases} 1, & 0 \leq t_{n,on} < t < t_{n,off} \leq T_{TM} \\ 0, & \text{else} \end{cases} \quad (19)$$

where $t_{n,on}$ and $t_{n,off}$ are the switching on-off time periods of the n^{th} element, and T_{TM} is the entire TM sequence length.

In the following derivation, each element is activated for $t_n = T_{TM}/N$ and then switched-off for the remaining part of the period. With this periodical switching sequence across the N -element array, the corresponding excitation time of the n^{th} element can be written as:

$$\frac{nT_{TM}}{N} \leq t \leq (n+1) \frac{T_{TM}}{N} \quad (20)$$

The time-modulation waveform of each element is a periodic pulse. $a_n(t)$ can be further expanded by its Fourier series:

$$a_n(t) = \sum_{m=-\infty}^{\infty} \beta_{n,m} e^{jm\omega_{TM}t}, \quad (21)$$

where the TM sequence frequency $\omega_{TM} = 2\pi/T_{TM}$ ($F_{TM} = 1/T_{TM}$) that can be much lower than the carrier frequency ω . Note ω_{TM} should be at least greater than the bandwidth of the incident signal to avoid frequency aliasing. The coefficient m denotes the order of the generated fundamental and harmonic frequency components. Also, note the fundamental or harmonic frequencies here mean those for the TM sequence frequency ω_{TM} , not for the RF carrier frequency or LO frequency.

Within the period T_{TM} , (21) can be further derived for Fourier coefficients $\beta_{n,m}$ with each harmonic frequency component by substituting the periodic time-switching sequence (2) as:

$$\begin{aligned}\beta_{n,m}(\omega_{TM}) &= \frac{1}{T_{TM}} \int_0^{T_{TM}} a_n(t) e^{-jm\omega_{TM}t} dt \\ &= \frac{1}{T_{TM}} \int_{t_{n,on}}^{t_{n,off}} e^{-jm\omega_{TM}t} dt \\ &= \frac{1}{-jm\omega_{TM}T_{TM}} [e^{-jm\omega_{TM}t}] \Big|_{t_{n,on}}^{t_{n,off}} \\ &= \frac{\sin(\frac{m\pi}{N})}{m\pi} e^{-\frac{j2m\pi n}{N}} e^{-\frac{j\pi m}{N}}\end{aligned}\quad (22)$$

Equation (22) shows periodic TM switching effectively creates both amplitude and phase modulation for each channel at fundamental and different harmonics of the TM frequency ω_{TM} . With both amplitude and phase modulation, the TMA array factor can be accordingly resolved. Assume the TMA operates in the receiving mode with d as the antenna element spacing. A far-field incident plane wave of carrier frequency F_c is received with an incident direction θ and wavenumber k . Thus, the array factor $AF(\theta, t)$ can be expressed as:

$$AF(\theta, t) = e^{j\omega_c t} \sum_{n=0}^{N-1} a_n e^{jknd\sin\theta} \quad (23)$$

By substituting (21) and (22) into (23), the array factor $AF(\theta, t)$ with TM frequency ω_{TM} can be further derived as:

$$AF(\theta, t) = \sum_{m=-\infty}^{\infty} e^{j(\omega_c + m\omega_{TM})t} \sum_{n=0}^{N-1} \frac{\sin(\frac{m\pi}{N})}{m\pi} e^{-\frac{j\pi m(2n+1)}{N}} e^{jknd\sin\theta} \quad (24)$$

Equation (24) means each Fourier coefficient $\beta_{n,m}$ can translate a received signal from θ incidence to a specific harmonic frequency of ω_{TM} . With $d = \lambda/2$, (24) is further simplified as:

$$AF(\theta, t) = \sum_{m=-\infty}^{\infty} e^{-\frac{j\pi m}{N}} e^{j(\omega_c + m\omega_{TM})t} \sum_{n=0}^{N-1} \frac{\sin(\frac{m\pi}{N})}{m\pi} e^{j\pi n(\sin\theta - \frac{2m}{N})} \quad (25)$$

From (25), the maximum $AF(\theta, t)$ happens at $\theta = \sin^{-1}(\frac{2m}{N})$ for different TM harmonic frequencies $m \times \omega_{TM}$, and this is the fundamental concept of multi-arm harmonic beamforming in a TMA RX. This essentially means the received signals from different incident angles are

redistributed and multiplexed to different TM harmonic frequencies. Furthermore, isolation between signals with various spatial information is ensured.

It worth mentioning that there're few design concerns in the time-modulation frequency $\omega_{TM} = 2\pi/T_{TM}$ selection. Firstly, the time-modulated frequency F_{TM} at least needs to be twice of the signal bandwidth due to Nyquist sampling theorem, otherwise, strong aliasing between adjacent harmonics will happen. Thus, this is the lower bound of the time-modulated frequency. Secondly, the time-modulation frequency F_{TM} will be limited by the speed of the switch. In our design, we put the tail-current switch at the second stage of the LNA. The tail-current switch is widely used as the time-modulated system application at mm-Wave frequencies [47],[48],[49] and can support up to hundred megahertz. Thirdly, the time-modulated frequency F_{TM} at least needs to be within the receiver operation bandwidth. Thus, for example, in a 4-element time-modulated array receiver, $2*F_{TM}$ and $-2*F_{TM}$ should be within carrier signal's bandwidth for achieving proper receiver down-conversion.

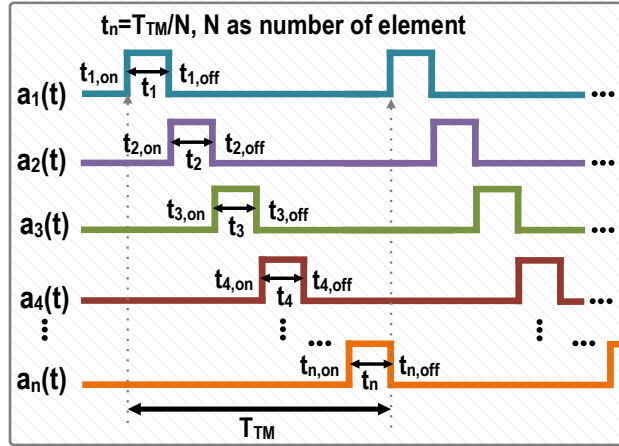


Figure 22 Time-modulated (TM) Sequence of an N-element Linear Array

5.1.1 Time-Modulated Spectral-Spatial Mapping MB-MIMO RX

Based on the fundamental concept of the TMA we propose a TM spectral-spatial mapping MIMO RX array with concurrent steerable multi-beams using only one beamformer. By using the periodic TM sequence on the four-element mm-Wave RX as shown in figure 22(b), the received signal at the carrier frequency F_c and incident from an angle $\theta = \sin^{-1}(\frac{2m}{N})$ is down-converted and mapped to one spectral component at the IF frequency of $F_m(\theta) = F_{IF} + m * F_{TM}$, where m is the time-modulation mode number (harmonic order) and $F_{IF} = F_c - F_{LO}$ for LO low-side injection receiving. Therefore, multiple concurrent incidents beam all at F_c can be mapped to different IF frequencies, achieving multi-beam MIMO operation over one single-wire interface. This spatial-to-spectral mapping property can be exploited for a multitude of applications such as harmonic sideband rejection[50][51], physical layer security[47][49], and angle-of-arrival estimation [52]-[54]. In this work, we target to leverage this spatial-to-spectral mapping property of TMA to achieve concurrent steerable multi-beams yet low-complexity MIMO system and fast beam scanning.

In an N -element TMA, $N+1$ concurrent beams can be generated corresponding to angles of incidence $\theta = \sin^{-1}(\frac{2m}{N})$ with the mode number $m = 0, \pm 1, \dots, \pm N/2$ for an even number N . Using the TMA operation together with the element phase-shifter-based beam steering steps, the RX array can cover a full field-of-view (FoV), supporting steerable multi-beams using one beamformer.

With minimal hardware complexity in our proposed TM MB-MIMO RX system, the beam scanning speed is also improved substantially. Further simulation results are included in figure 24, for different TM sizes. A 2-element/8-element array can simultaneously form 3/9 beams pointing to different directions (figure 25), with the number of concurrent TM beams ($N+1$) linearly increasing with array size N . Moreover, multiple beams incident from different angles are mapped to different IF spectral components and can be offloaded to the digital backend demodulated via a single wire interface. In addition, it is worth noting that the peak-to-null ratio between harmonic frequencies is theoretically maximized at each incident angle $\theta = \sin^{-1}(\frac{2m}{N})$ and the crossbeam isolation is then guaranteed. Thus, with a sufficient F_{TM} , the different IF components are spaced apart to support high isolation and easy filtering to retrieve the multi-beam MIMO information, unlike the reported code-domain or frequency-domain multiplexing with a limited crossbeam isolation.

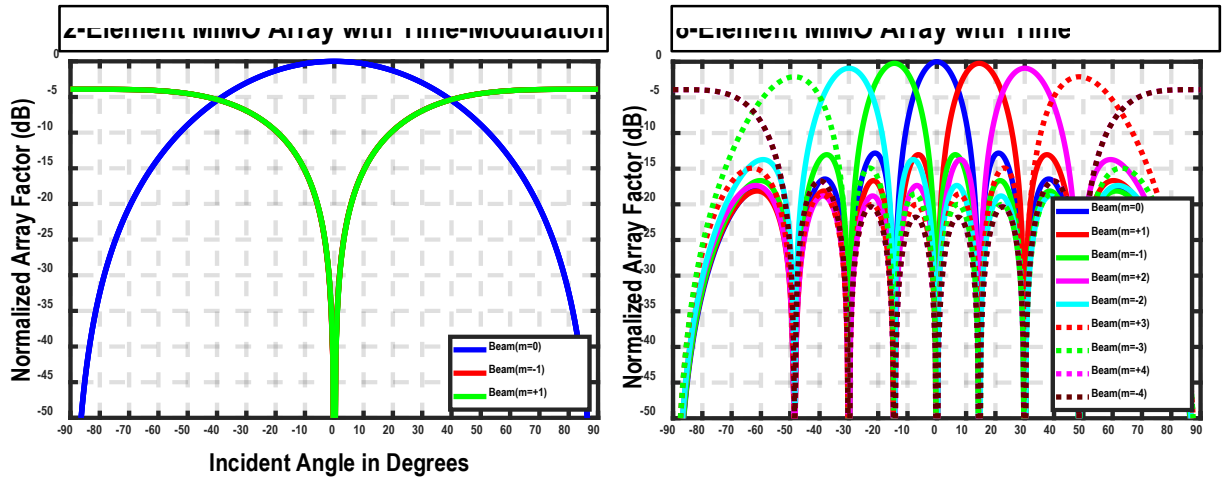


Figure 23 Theoretical Normalized Array Factor of the $N=2$ and 8 TMA for MB-MIMO Beamforming

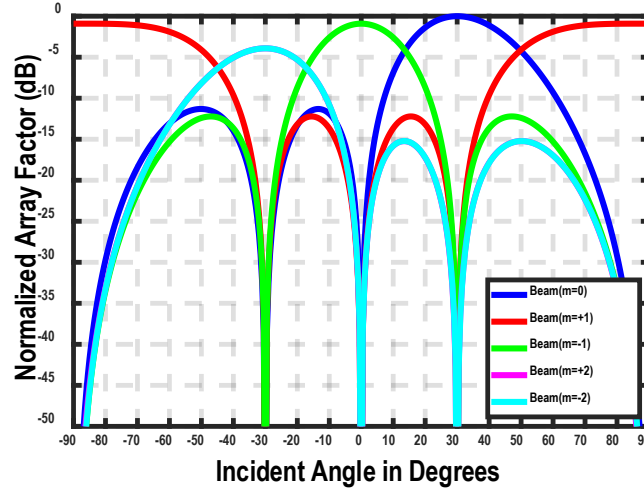


Figure 24 Simulated TM MB-MIMO RX Array with 30° Beam-steering

5.1.2 SNR Consideration in Time-Modulated MIMO RX

One key consideration on the TM RX array is to understand the SNR on each concurrent multi-beams and interference suppression versus conventional single-beam analog phased array. Further discussion is included in this subsection. In practice, time-modulation will affect the entire spectrum, including the received signal and noise. When the envelope of the time-modulation signal is applied to the received signal and noise, both of them are spread on the spectrum based on the Fourier transformation. The received signal and noise are down-converted to the baseband circuitry in an RX system. In the derivation, we first assume that the antenna bandwidth is limited from $F_C - 0.5F_{TM}$ to $F_C + 0.5F_{TM}$. If the antenna bandwidth is not limited in the derivation, the received noise spectrum will exhibit noise folding depending on the actual antenna bandwidth and the TM switch's sampling rate. For the simplicity of the derivation and to provide an intuitive understanding of SNR in the TM RX array (compared to the conventional phased array system), the limited antenna bandwidth is assumed. Also, the recently published microstrip patch antenna, which is widely used in 5G communication applications (e.g., 28GHz or 37GHz) and radar/sensing applications, commonly has small fractional bandwidth lower than 5% [55]-[58].

In a conventional phased-array RX, the SNR of the received signal at each antenna element can be expressed as:

$$SNR_{single} = \left(\frac{S_n}{V_n}\right)^2 \quad (26)$$

where $y_n = S_n e^{jknd \sin \theta}$ is the received signal with amplitude S_n and V_n is additive white Gaussian noise with N -element array. Assuming that the element spacing is half-wavelength, the array SNR can be expressed as:

$$SNR_{array} = \frac{\sum_{n=0}^{N-1} y_n^2}{\sum_{n=0}^{N-1} V_n^2} = \frac{(N \cdot S_n)^2}{N \cdot V_n^2} = N \times SNR_{single} \quad (27)$$

where N is the directivity gain.

In the TMA, both the received signal and noise are modulated by switching sequence and corresponding spectra are spread. Assuming that both signal and noise are not aliased, the TM received signals at fundamental and harmonic frequencies can be constructively combined on the spreading spectrum. Thus, the TMA SNR can be represented as:

$$SNR_{array}^m = Directivity_{single}^m \times SNR_{single} \quad (28)$$

where SNR_{array}^m is associated with m^{th} harmonic frequencies.

$$Directivity_{single}^m = \left| \sum_{n=0}^{N-1} |\beta_{n,m}| \right|^2 / \sum_{n=0}^{N-1} |\beta_{n,m}|^2 \quad (29)$$

where $\beta_{n,m}$ is the equivalent complex excitation shown in (23) for the n^{th} element with the m^{th} order harmonic frequency.

The SNR_{array}^m will be determined by $\beta_{n,m}$ with different selected TM sequences. In this work, we want to emphasize the potential of fast-scanning, so we use the periodic non-overlapping TM sequence for generating $N+1$ beams for covering full FoV. However, if the application is aimed at complex wireless communications with much unknown interference, the dedicated time-modulation sequence can be adjusted and leveraged.

5.1.3 Time-Modulated MB-MIMO RX with Beam-Steering

By leveraging the time modulation operation together with the beam steering capability using element-based phase shifters, the RX array can cover a full field-of-view (FoV) supporting steerable multi-beams using a single beamformer for fast beam-scanning over the FoV. The analysis of the TMA with beam steering can be carried out using the same methodology described in section-II.A. Assume the phase shifter in each element has a progressive phase shift φ , the array factor $AF(\theta, t)$ of (23) will be modified to $AF_{bs}(\theta, t)$ as:

$$AF_{bs}(\theta, t) = e^{j\omega_c t} \sum_{n=0}^{N-1} a_n e^{jkn d \sin \theta} e^{-jn\varphi}. \quad (30)$$

By maintaining the same time-modulation pulse sequence shown in Fig. 2, a_n will be still given by (19), (21), and (22). Accordingly, by assuming an element-to-element spacing $d = \lambda/2$, the array factor with beam steering $AF_{bs}(\theta, t)$ can be expanded as:

$$AF_{bs}(\theta, t) = \sum_{m=-\infty}^{\infty} e^{j(\omega + m\omega_{TM})t} e^{-\frac{j m \pi}{N}} \sum_{n=0}^{N-1} \frac{\sin\left(\frac{m\pi}{N}\right)}{m\pi} e^{j\pi n(\sin \theta - \frac{2m}{N} - \frac{\varphi}{\pi})} \quad (31)$$

Equation (31) reveals that with the presence of the progressive phase shift, the peaks of the array factor for different TM harmonic frequencies $m * F_{TM}$ will occur at $\theta = \sin^{-1}\left(\frac{2m}{N} + \frac{\varphi}{\pi}\right)$. Therefore, by choosing the appropriate φ , desirable multi-beam patterns can be synthesized. It is worth noting that since the two terms $\frac{2m}{N}$ and $\frac{\varphi}{\pi}$ are added inside the inverse sine function, each beam from the multi-beams at different harmonics will be steered with a different angle. In addition, the nulls of the beams will be steered with the same angles as the peaks of other beams, ensuring a high peak-to-null ratio for these concurrent beams.

5.2 Circuits Implementation

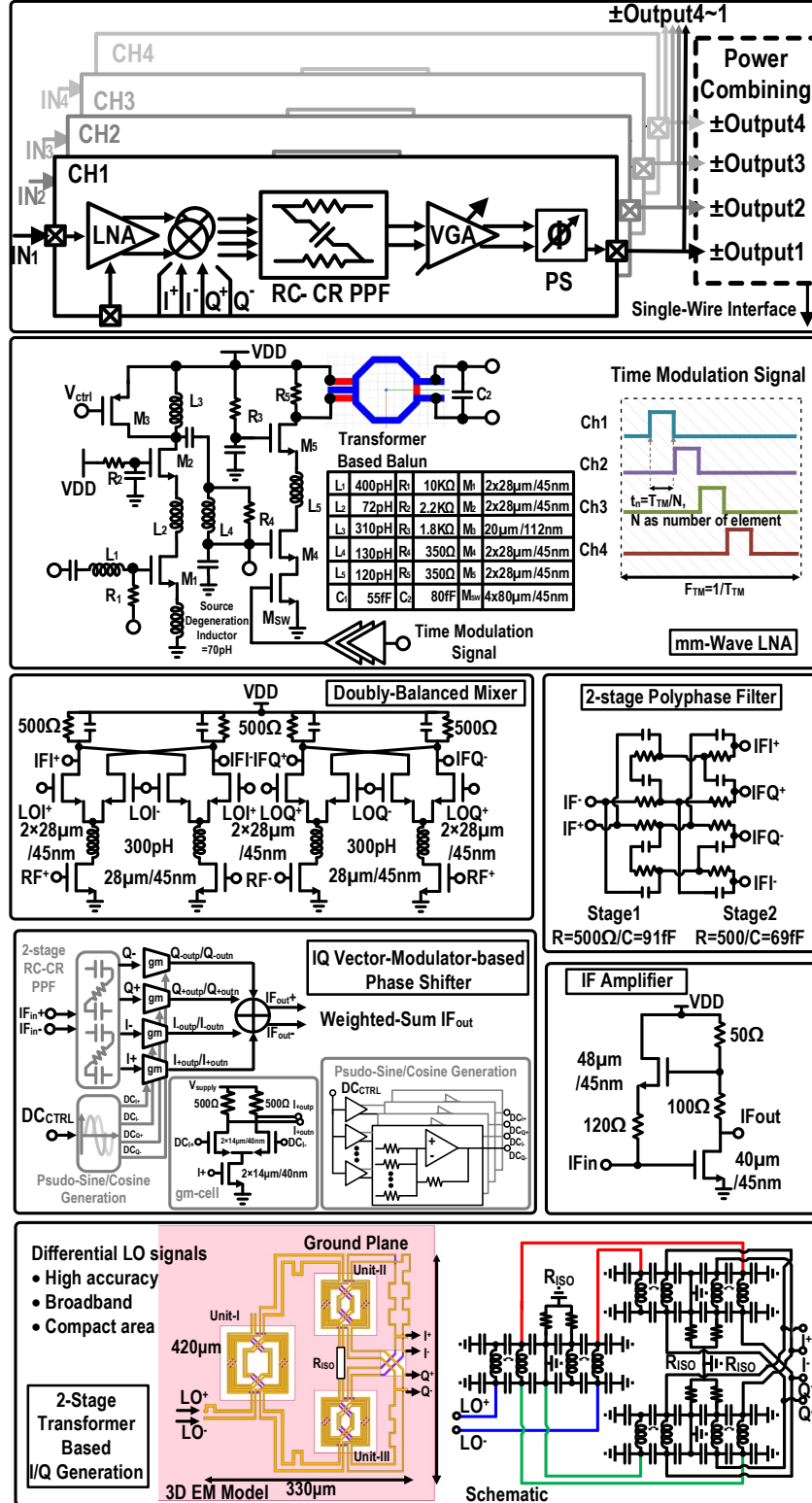


Figure 25 System Block Diagram and Detailed Schematic of the Proposed TM MIMO RX Array

The proposed TM MIMO RX is implemented as a 4-channel broadband mm-Wave image-rejection RX array (figure 26). Broadband mm-wave low noise amplifier (LNA) is designed with a source degeneration inductor to achieve input matching and low noise figure simultaneously. The Hartley image RX architecture with broadband LO I/Q generation and IF I/Q combining is chosen. High-accuracy transformer I/Q generation network achieves high-quality quadrature LO generation over 20-45GHz. An IF two-stage 2-5GHz RC-CR poly-phase filter is used for image rejection I/Q combining.

This achieves broadband image rejection without additional control or tuning circuits. A two-stage low noise amplifier (LNA) with wideband resonance loads is designed to provide broadband performance as shown in figure 26. The source degeneration technique is leveraged to optimize for both wideband noise and input matching. The two-stage LNA is designed with a different gain setting for different practical receiving scenarios with linearity consideration. The PMOS switch device M_3 is placed on the load at the 1st stage of LNA which is shown on the figure 26. The loading condition for the first stage of LNA will be determined by the parallel impedance of device M_3 and inductor L_3 . By properly changing the V_{ctrl} , the gain of the LNA will be varied accordingly to achieve receiver conversion gain tunability. An output transformer-based balun absorbs the loading effect from following the differential I/Q double-balanced mixers and serves as a balanced differential signal generation. The TM signals are digitally buffered on-chip and applied to the high-speed switches at the tail current source of the LNA second stage. This ensures negligible degradation of the RX noise figure and linearity, unlike using series switches in the RX signal path. The entire RX element (or most part of the RX element) can be completely switched off for better system efficiency when the corresponding RX path should be off. In this proof-of-concept design, we aim at the reliable demonstration of multi-beam MIMO receiving of the time-modulated array, so we choose to only switch on/off the second stage of LNA.

The active mixer is based on a standard double-balanced mixer topology (figure 26). The mixer is resistively loaded for wideband IF operation. The RF and LO transistor sizes and current density are simultaneously optimized to achieve the highest conversion gain and linearity but the benefit in linearity stays in conflict with a loss of conversion gain. Therefore, the inductor between the switching pair and the g_m stage is leveraged to improve the interstage matching between the g_m -stage and the switching pair. This additional effort results in an increased conversion gain that compensates for the gain reduction. The I/Q double-balanced mixers are followed by the IF variable-gain amplifier (VGA) and IF RC-CR poly-phase filter. Figure 26 shows the schematic of the IF VGA consisting of the feedback loop to broaden the operation bandwidth while having various gate biases for gain control. Next, a two-stage RC-CR poly-phase filter is utilized to complete the IR at the IF frequency.

The schematic of the utilized wideband I/Q voltage-controlled phase-shifter is shown in figure 26. It consists of a two-stage RC-CR poly-phase network and an analog multiplier with built-in dc pseudo sine/cosine generation as a vector-modulator phase-shifter. A quadrature splitter produces in-phase signal $I=\sin(\omega t)$ and quadrature-phase signal $Q=\cos(\omega t)$, where ω is the angular frequency of the input signal. Then the two signals are multiplied by DC coefficients

DC_I and DC_Q , respectively, such that $I_{out}=DC_I \cdot \sin(\omega t)$ and $Q_{out}=DC_Q \cdot \cos(\omega t)$. A pseudo-sine/cosine generator plays the role of a voltage-to-voltage translator from voltage DC_{CTRL} to voltage $\cos(DC_{CTRL})$ and $\sin(DC_{CTRL})$. Thus, the output $I_{out}=\sin(\omega t+DC_{CTRL})$ and phase of I_{out} should be proportional to control voltage DC_{CTRL} . The proposed I/Q phase shifter achieves wideband full-range continuous-tuning and only requires one analog control voltage system simplicity.

For the LO driving in the differential I/Q double-balanced mixer, an mm-Wave transformer-based I/Q network is designed to convert one differential LO input to two balanced well-matched differential I/Q LO outputs with compact size and low loss over an extremely wide bandwidth. The proposed transformer-based I/Q network is designed based on a two-stage cascaded self-similar 90° hybrid coupler as a one-inductor-footprint I/Q transformer. The phase/amplitude mismatch is highly suppressed by cascading multiple stages of transformer-based 90° hybrid coupler units and a proof-of-concept two-stage transformer-based I/Q is proposed to achieve high-accuracy I/Q generation over 20–45 GHz.

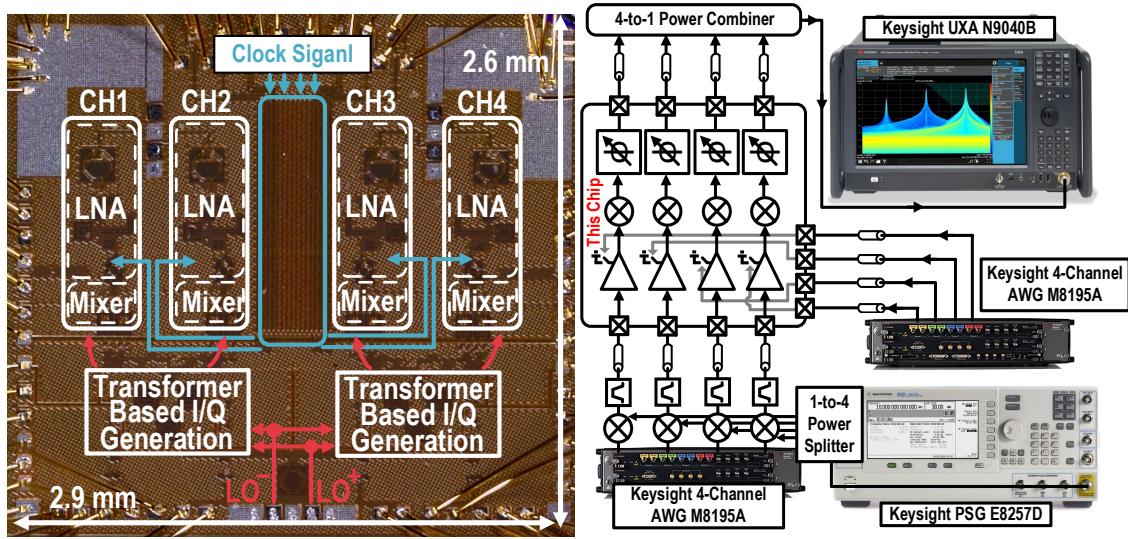


Figure 26 Chip Micrograph of the Proposed TM MIMO RX Array and Measurement Setup for the mm-Wave TM MIMO RX Array for Both CW and Modulated Signals

5.2.1 Experimental Results

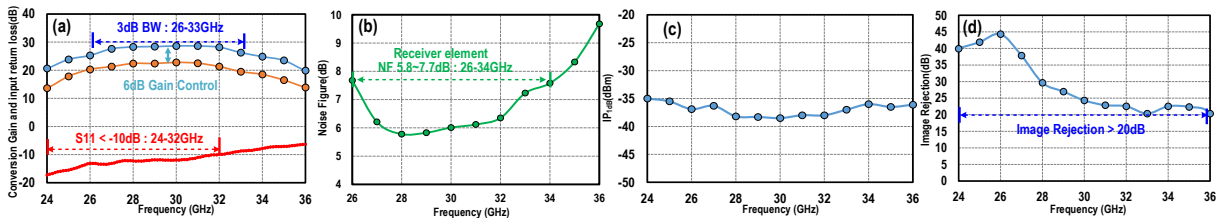


Figure 27 Measured Wideband RX Array Element Conversion Gain (CG), Input Matching S11, Noise Figure NF, Input-referred 1dB Compression Point IP1dB, and Image Rejection

As a proof of concept, we demonstrated an mm-Wave TM MIMO RX array with concurrent steerable multi-beams using one beamformer and single-wire interface. The proposed TM MIMO RX array is fabricated using a 45nm CMOS RF SOI process with a total chip size of 2.9mm×2.6mm (figure 27).

The measurement setup for the TM RX array is shown and described in figure 27. Four channel continuous-wave (CW) and modulated IF signals with variable phase and amplitude are synthesized by the Keysight arbitrary wave generator (AWG) 8195A to demonstrate the received signals with different incident angles. Then, the signals are up-converted to mm-Wave frequency using off-shelf mixers. A second AWG is applied to synthesize the responding ON-OFF control signals for the TM RX array. To characterize the CW and complex modulation results of the proposed TM RX array, Keysight spectrum analyzer UXA is used to capture the down-converted both CW and modulated signals. All the connected cables are used matched cables to minimize both amplitude and phase errors. Further amplitude and phase mismatches are also calibrated through AWG.

5.2.2 Single Path RX Performance Characterization

The proposed tm rx array demonstrates 26-to-33 ghz wideband operation. For the mm-wave performance characterization, the single-channel of the proposed rx is measured including both small-signal and large-signal performance and summarized in fig.8. The rx demonstrates wideband input and noise matching simultaneously with a measured input return loss s_{11} is <-10 db across 24~32 ghz.

in addition, it achieves a maximum conversion gain of 28db with a 3db bandwidth of 26~33 ghz. The single channel rx noise figure (nf) is verified by keysight uxa with noise source 346ck01 and the minimum nf is measured to be 5.78 db at 28 ghz. From 26 to 34 ghz, the measured nf is 5.78 to 7.7db. The linearity of the proposed rx is also tested with rx input-referred $ip1$ db of -38dbm at 30ghz. To further test the image rejection ratio of the proposed rx, both desired signal and image signal are sent to the tested rx channel simultaneously. For the frequency of interest from 24 to 36 ghz, the image rejection ratio is higher than 20db and shows a maximum rejection of 45db at 26 ghz. It is worth mentioning that no further tuning or switching element is used in these cw image rejection ratio measurements.

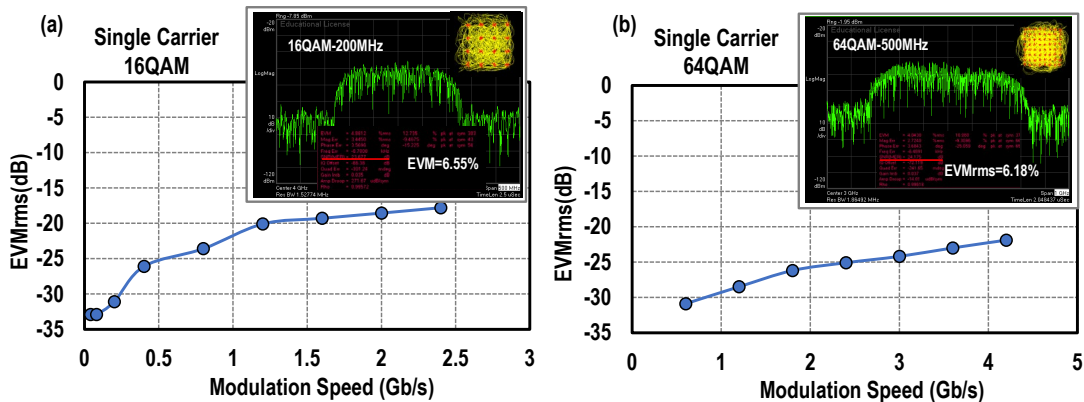


Figure 28 Measured Wideband Receiver With HIGH-Speed Complex Modulated Single Carrier Signal with Both 16-QAM and 64-QAM

The proposed rx is also verified through high-speed single-carrier 16-/64-qam modulation signals to validate the compatibility for a future mimo communication system. For the desired signal (mm-wave frequency = 30 ghz), it supports 2gb/s and 2.4gb/s 16-qam wideband modulation signal with -18.6db/-17.8db evmrms. Figure 29(a) demonstrates the tested modulation results summary using single carrier 16-qam modulation signals. With 16-qam 200mhz received modulation signal, the proposed rx shows 6.55% evmrms. Furthermore, the single carrier 64-qam modulation measurements are also verified. In figure 29(b), with 64-qam 500mhz received modulation signal, the proposed rx shows 6.18% evmrms. In summary, the designed rx supports 3.6 gb/s and 4.2gb/s 64-qam modulation signal with -23db/-21.98db evmrms.

5.2.3 Time-Modulated MIMO RX Array

Figure 30 summarizes the measurement results to validate the functionality of the proposed tm mimo rx array with a corresponding tm signal (tm frequency = f_{tm}). The detailed measurement setup is also described in figure 28. First awg is applied to generate four-channel receiving signals, and second awg is leveraged to synthesize four-channel tm clock signals. Phase and amplitude mismatches in each channel are calibrated in the measurements.

firstly, the received signals from awg are up-converted to mm-wave frequency 30ghz through an off-shelf mixer and sent to the proposed tm mimo rx. Then, the built-in tm switches of the tm rx start to modulate the received signals. Thus, the received signals from different incident directions are mapped to different harmonic frequencies $m \cdot f_{tm}$ following the tma theory. Next, the received signals are down-converted to if frequencies and combined through an off-shelf four-way power combiner. The output spectrum is captured through uxa. By distinguishing the output spectrum, we can specify the incident direction of the received signals. Further research can be extended to direction-finding techniques and phased array beam alignment applications.

the overall beam pattern is tested at the carrier frequency $f_c=30$ ghz with tm frequency $f_{tm}=100$ mhz. According to the tma concept, the normalized array factor is measured in the full field-of-view (fov) for different beam-steering cases. Spatial-spectral mapping of five concurrent beams by temporal modulation on a 4-element rx array is successfully achieved and is consistent with the theoretical simulations shown in figure 30. Furthermore, by using the built-in element vector-modulator phase shifters, the proposed rx array achieves beam-steering of the concurrent multi-beams by the time-modulation. It should be noted that with the concurrent multi-beams, the required phase shifting range to cover the full fov is highly reduced from $-90^\circ < \theta < 90^\circ$ to $-30^\circ < \theta < 30^\circ$, enabling fast array beam scanning. It should be noted that employing a large array will linearly increase the number of concurrent beams and further decrease the phase shift range and array scanning time. In this prototype design, we still leverage the built-in vector sum phase shifter to achieve beam scanning. Further tm switching sequences can be studied to achieve more efficient beam-scanning mechanisms.

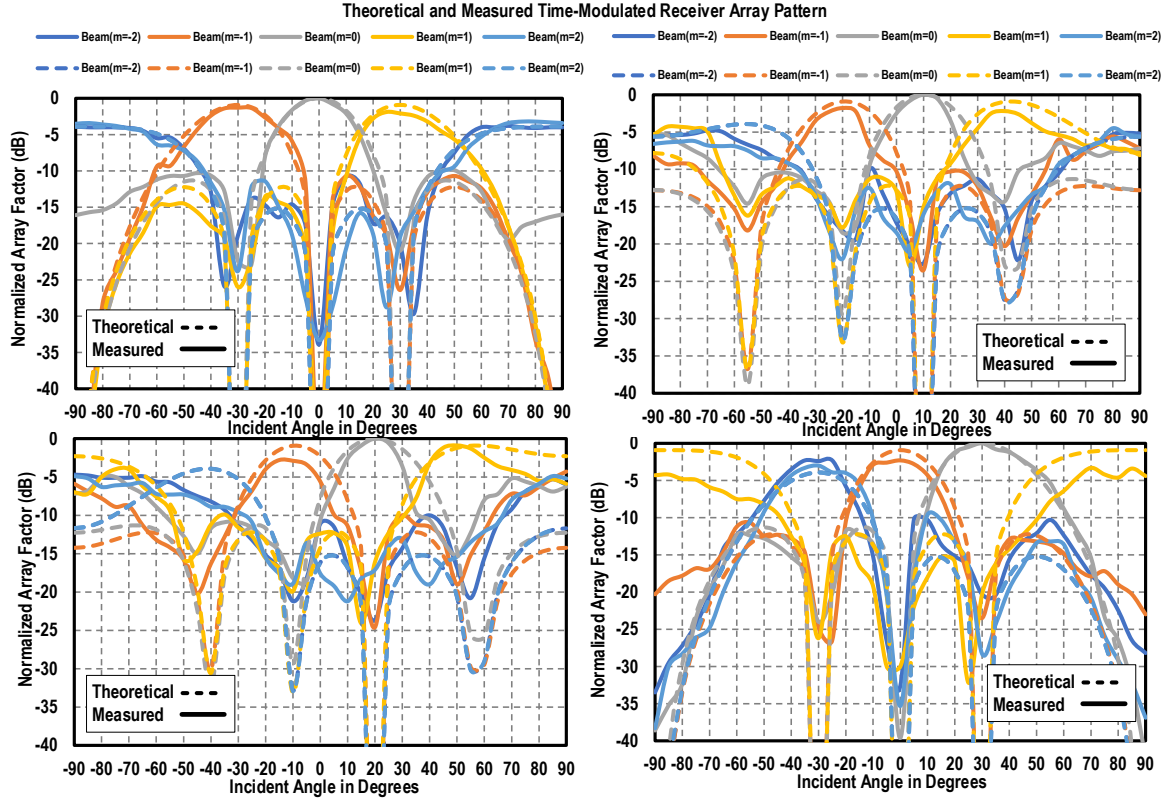


Figure 29 Measured Normalized Array Pattern of 4-element MIMO RX Array with Time Modulation to Achieve Concurrent Steerable 5-bands ($n = 0, \pm 1$, and ± 2), while the Full FoV can be Covered by RX Array Beam Steering with a Much-Reduced Phase Shifting Range ($-30^\circ < \theta < 30^\circ$), Enabling Fast Array Beam Scanning Over the Full FoV

5.2.4 Space Division Multiple Access Communication Using Time-Modulated MIMO Rx Array

In this subsection, the space division multiple access communication schemes by the proposed tm mimo array is discussed and demonstrated. Due to the intrinsic multi-beam spatial to spectral mapping characteristic of the tm rx array, the proposed rx can distinguish user-ends with the same carrier frequency from different incident angles by the harmonic frequency spectrum. By utilizing a tm sequence of $f_{tm}=200\text{mhz}$, the incident signals are firstly time-modulated and then mapped to various harmonic frequencies.

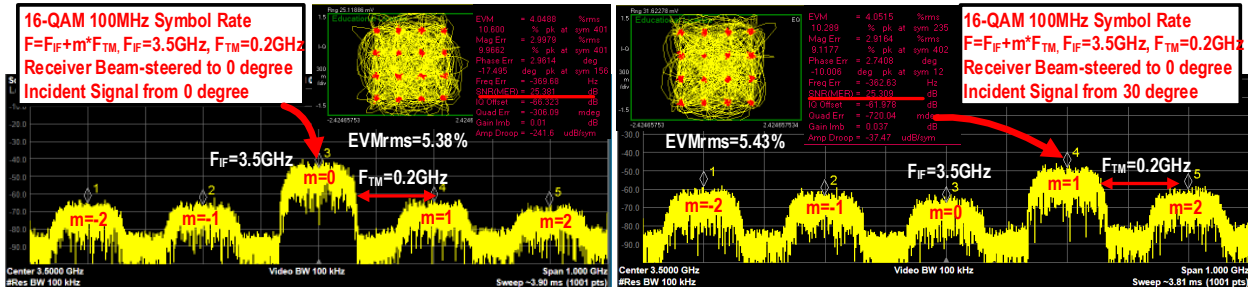


Figure 30 Measured Complex Modulation Performance of the 4-element MIMO RX Array with Time Modulated Spectral-spatial Mapping with Concurrent 5 Beams showing Incident Angles of 0° and 30° are Mapped to $0 \cdot F_{TM}$ (3.5GHz) and $1 \cdot F_{TM}$ (3.7GHz) IF Tones

For instance, in the 4-element tm rx array, if the incident signal of the user comes from $+30^\circ$ at f_c , the received signal will be firstly time-modulated to $f_c + 1 \times f_{tm}$ with preserved spatial information and then down-converted with f_{lo} to $f_1(\theta) = f_{if} + 1 \times f_{tm}$. Similarly, the incident signal from -30° follows the same intrinsic mapping behavior but it is mapped to $f_{-1}(\theta) = f_{if} + (-1) \times f_{tm}$. all the received signals passing through the four element channels are in-phase combined after calibration and sent to uxa for demodulation.

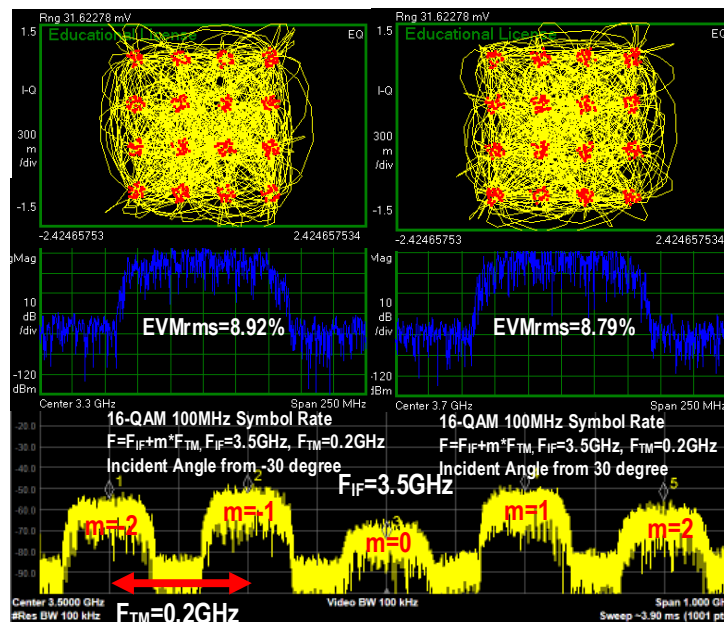


Figure 31 Measured Complex Modulation Performance of the 4-element MIMO RX Array with TM Spectral-spatial Mapping with Concurrent 5 Beams Showing Two Concurrently Received Signals with -30° and 30° Incident Angles are Mapped to $-1 \cdot F_{TM}$ (3.3GHz) and $+1 \cdot F_{TM}$ (3.7GHz) IF Tones

As an experiment with one receiving the signal, the incident modulated signal is at carrier frequency 30 ghz with single-carrier 16qam 100mhz symbol rate. With tm frequency $F_{TM}=200\text{mhz}$ and $F_{IF}=3.5\text{ghz}$, we demonstrate temporal spatial-spectral mapping of the two

different incident signals at 0° and 30° with a separation of 200mhz at the if frequency. Reading from the if spectrum (figure 31), the 0° incident signal is mapped to $FIF + 0 \times f_{tm} = 3.5\text{ghz}$ ($m=0$) and is successfully demodulated with $\text{evmrms}=5.38\%$. Also, the 30° incident signal is mapped to $FIF + 1 \times FTM = 3.7\text{GHZ}$ ($m=1$) with 5.43% demodulation evmrms .

In the second experiment, two concurrent modulated single carrier 16-qam incident signals at the same carrier frequency $F_c=30\text{ghz}$ with different incident angles $+30^\circ$ and -30° are synthesized by AWG. It is worth mentioning that the two concurrent receiving case in the TM RX array will require more accurate channel-to-channel calibration, including amplitude, phase, and switching clock. The system SNR is not only determined by noise but also the alias of the received signal from other directions. In figure 32, reading from the if spectrum shows that the two concurrent 16-QAM signals from incident angles $= -30^\circ$ and $+30^\circ$ are temporally mapped and down-converted to $FIF-1 \times FTM=3.3\text{ghz}$ (-30°) and $FIF+1 \times FTM = 3.7\text{ghz}$ ($+30^\circ$), respectively. The successfully demodulated evmrms for each one are 8.92% and 8.79%. Theoretically, an n -element TMA RX can communicate with $N-1$ users simultaneously with high channel-to-channel isolation. If the number of elements n increases, the TMA can ideally cover nearly full fov communication at the same time without requiring complicated and area-consuming on-chip beamformers for multi-beam generation. Furthermore, it's practically challenging to implement low-loss on-chip phase shifters with the compact area at these frequencies, so tmas are especially suitable for high mm-wave and even thz frequencies.

As shown in table. III, the proposed tm MB-MIMO RX demonstrates 26-to-33ghz wideband operation. The maximum conversion gain is 28db with a 3db-bandwidth of 26~33 ghz and the measured NF is 5.78 db at 28 ghz with RX input-referred ip1db of -38dbm. Also, the proposed RX can support both 16-/64 QAM wideband single carrier modulation.

By exploiting the intrinsic spatial-spectral mapping behavior of TMA, the proposed 4-element wideband MIMO RX array successfully demonstrates concurrent steerable MB-MIMO with one single-wire interface. With tm operation, received beams incident at different angles are mapped to different if spectral components and thus can be effectively offloaded to the digital backend demodulation. Moreover, SDMA communication scheme is also successfully verified with two concurrent signals from two different incident angles. Note that this technique only requires low hardware complexity or power overhead and can be easily scaled to a large array with increased concurrent multi-beams and fast full fov scanning.

TABLE. III Comparison with Recently Reported State-of-the-Art mm-Wave MIMO RXs

	This Work	Garg ISSCC 2020	Mondal ISSCC 2020	Johnson RFIC 2019	Pang ISSCC 2019	Dunworth ISSCC 2018	Sadhu JSSC 2017
Technology	45nm SOI CMOS	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	28nm CMOS	0.13 μm SiGe
Frequency (GHz)	26-33	28	28/37	29.2	26.5-29.5	25-30.5	28
Conversion Gain (dB)	28	>16	44/37	16	11	22	34
NF DSB,eq(dB) [§]	5.8-7.7	6-7.8	7.9/8.8	10	4.2-5.0	4.4-4.8	6
Beamforming Mode	Time-Modulated Array Operation and Phase-Shifter-Based	Frequency Domain Multiplexing	Multi-layer and Full- Duplex Beamforming	Code-Domain Multiplexing	Phase-Shifter Based	Phase-Shifter Based	Phase-Shifter Based
Spatial-to-Spectral Mapping	Yes	Yes	Yes	Yes	No	No	No
Modulation Scheme	4.2Gb/s 64-QAM	0.4Gb/s 16-QAM	1.5Gb/s 64-QAM	NA	6.4Gb/s 256-QAM	2.4Gb/s 64-QAM	5.16Gb/s 256-QAM
Power Consumption per Element (mW)	66	112.6	98.75	NA	112	42.6	207
Area (mm ²)	7.54	10.7	12.65	5.75	12	30	165.10

[§]NF DSB is defined as element RX noise figure.

6 A 26-32 GHZ DUAL-POLARIZATION RECEIVER FRONTEND WITH RAPID-RESPONSE MIXED-SIGNAL POLARIZATION ALIGNMENT FOR ULTRA-RELIABLE LOW LATENCY COMMUNICATIONS

6.1 System Overview

Exploiting mm-Wave bands, the next-generation wireless communication systems promise to deliver extreme data rates (multi-Gb/s) and ultra-reliable low latency communications (URLLC) [59]-[71]. To meet next-generation wireless communication systems' data-rate, low-latency, and spectrum efficiency requirements, polarization MIMOs are gaining attention because of their ability to use orthogonal polarizations to transmit two independent data streams simultaneously. For their compatibility with existing antennas and electronics platforms, linear vertical and horizontal polarizations are often used. However, any linear polarization misalignment between the transmitting and receiving antennas results in cross-polarization leakages between both signal streams as well as in polarization mismatch signal loss, which significantly degrades the signal-to-noise (SNR) ratio of the desired signal and limits for future 5G and URLLC applications. One of the most popular ways to correct the antenna misalignment is using backend digital signal processing (DSP). Backend DSP is sufficient for applications that operate in static or slowly varying environments and fixed wireless accesses, such as backhaul, customer premise equipment (CPE), and data center. For future mobile and URLLC applications which operate in highly dynamic and rapidly changing environments, e.g., drone-/vehicle-based mm-Wave communication and mobile satellite terminals, the backend processing time will cause a major penalty on link latency and response time. Therefore, real-time recurrent polarization realignments ($<1\text{ms}$) are required [1]. To address this challenge, we present a polarization MIMO receiver (RX) architecture that utilizes front-end mixed-domain feedback loops on signal polarizations; without any backend DSP computation, the RX achieves rapid autonomous polarization alignment within micro-seconds (μs) and enables future ultra-low latency and extreme-data-rate polarization MIMOs for highly dynamic and mobile URLLC applications. This work is an extension of the conference presentation in [68].

6.1.1 Analog/mixed-signal Computation Unit

Assuming that the desired vertical/horizontal signals are A and B, respectively, the received vertical channel signal RX_V and horizontal channel signal RX_H are cross-contaminated as shown in (32), due to misalignment angle (θ) between transmitting antenna and receiving antenna (figure 33).

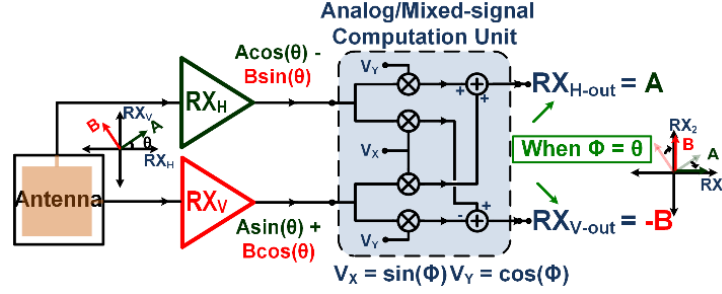


Figure 32 Signal Cross Contamination Due to TX/RX Antenna Misalignment and Proposed Low Latency Analog/Mixed-Signal Computation Unit

The autonomous polarization computation/ correction stage operates at the IF frequency and adds/subtracts the two received and polarization-misaligned signals RX_V and RX_H with weightings $V_X \propto \sin(\Phi)$ and $V_Y \propto \cos(\Phi)$ [72]. The results of addition/subtraction yield the final two RX output streams as shown in equation (2). When the control phase (Φ) is set to be equal to the incoming polarization misalignment angle (θ), the undesired cross-polarization terms are removed and the outputs are just the signals A and B.

$$\begin{cases} RX_H = A \cdot \cos(\theta) + B \cdot \sin(\theta) \\ RX_V = A \cdot \sin(\theta) - B \cdot \cos(\theta) \end{cases} \quad (32)$$

$$\begin{cases} RX_{H_{out}} = A \cdot \cos(\theta - \phi) + B \cdot \sin(\theta - \phi) \\ RX_{V_{out}} = A \cdot \sin(\theta - \phi) - B \cdot \cos(\theta - \phi) \end{cases} \quad (33)$$

6.1.2 Autonomous Control Voltage Generation

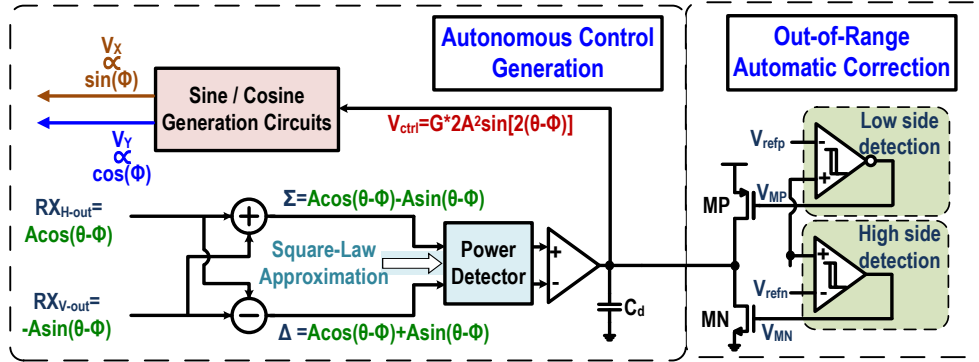


Figure 33 Autonomous Control Voltage Generation Block Diagram

The weighting signals V_X and V_Y (control phase Φ) are generated by an autonomous control voltage generation (Figure 34). Assuming only one of the signals (A or B) is presented, the control generation circuit works as follows. First, the outputs of the two receivers are added and subtracted to produce the sum and delta signals (Σ and Δ) as

$$\begin{cases} \Delta = A \cdot \cos(\theta - \phi) - A \cdot \sin(\theta - \phi) \\ \Sigma = A \cdot \cos(\theta - \phi) + A \cdot \sin(\theta - \phi) \end{cases} \quad (34)$$

Next, each of these signals separately undergoes squaring computations by a square-law CMOS power detector [73]. Then, the squared outputs are subtracted, amplified, and lowpass filtered yielding the control voltage signal V_{ctrl} below:

$$V_{ctrl} = G * 2A^2 * \sin(2[\theta - \phi]) \quad (35)$$

where G represents the total gain of the power detector and amplifier. V_{ctrl} is monotonically proportional to $\theta - \Phi$ (when less than 45°) and, hence, is suitable to form a negative feedback loop to automatically bring $\theta - \Phi$ to zero.

6.1.3 Feedback Loop Concept

The autonomous voltage control generation block and the analog/mixed-signal computation unit form a negative feedback loop. After applying the polarization calibration protocol, the control voltages (V_X & V_Y) are generated and held constant. The polarization calibration protocol operates as follows. First, only one of the two signals (A or B) is transmitted. It is then processed by the autonomous loop, which allows the generation of V_X and V_Y . The autonomous loop will drive Φ close to θ and eventually equal to θ . After that, control voltage V_X and V_Y is first saved and then held constant. Hence, the loop is opened, and the polarization calibration is completed. In this way, the receiver polarization orientation is properly tilted to match the incoming signals' polarization orientations, so that both streams A and B are received with reduced cross-polarization.

6.2 Circuits Implementation

Figure 35 shows the system block diagram of the implemented dual-polarization receiver front-end. The RX front-end design incorporates a common source LNA followed by a double-balanced active mixer. It achieves a RF S_{11} bandwidth of 26-32 GHz. Lastly, our autonomous polarization alignment stage is applied to correct the signal cross-contamination caused by antenna misalignment.

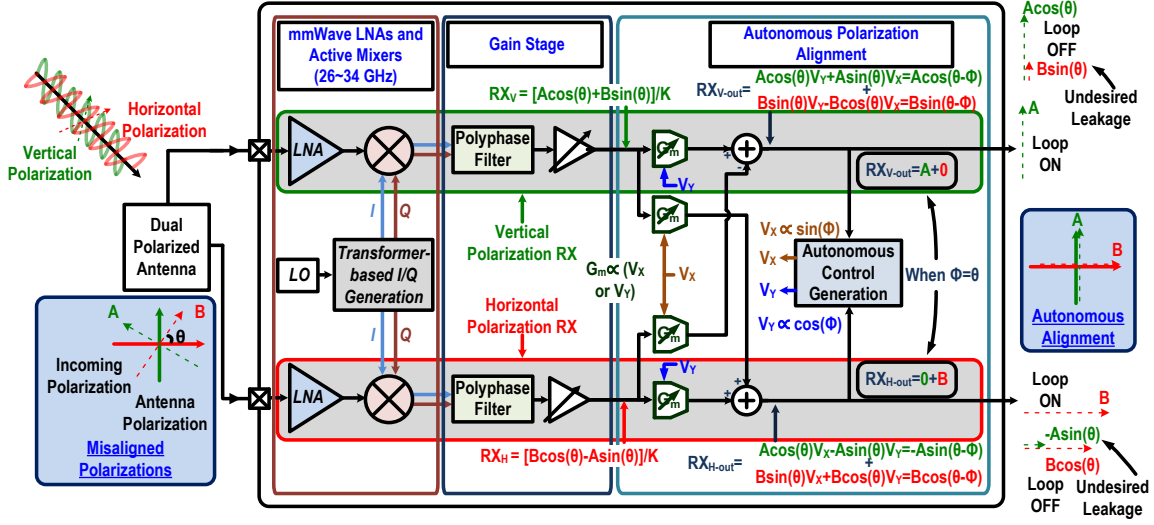


Figure 34 The Proposed mm-Wave Dual-Polarization Receiver RX Front Ends (RX_V and RX_H) with Autonomous Rapid Polarization Alignment

Figure 36 shows the detailed circuits implementation within the autonomous voltage generation block. Figures 36(a), 36(b) and 36(c) show the CMOS power detector, amplifier, and hysteresis comparator circuits respectively. Figure 36(d) shows the sine/cosine generation circuit. We adopt a mixed-signal approach. V_{ctrl} is first converted to a digital thermometer code using a 6-bit flash-ADC-like comparators and resistor ladder (figure 36(d)). Then, this code is converted back to the analog form using an op-amp feedback DAC structure with non-equal resistances. The resistance is given by equation (5.a) for sine generation circuits, and (36.b) for cosine generation circuits. A factor K_{AMP} , in (36.c) and (36.d), is used to account for the value of R_{FB} and the supply voltage of the comparators (logic “1”). This implementation will generate output voltages (V_X & V_Y) in a sine/cosine relationship with the input control signal V_{ctrl} as indicated in Figure 4(d). V_{ref-L} and V_{ref-H} are the flash ADC low and high reference voltages. The comparators have a save control signal, which is used to save the correct digital codes for the required Φ value. Then, there is a hold control signal to open the loop and hold the saved state to be used for receiving the dual-polarization signals.

$$R \cdot \sin(n) = \frac{R_{FB}}{V_X(n+1) - V_X(n)} \quad (36.a)$$

$$R \cdot \cos(n) = \frac{R_{FB}}{V_Y(n+1) - V_Y(n)} \quad (36.b)$$

$$V_X(n) = -K_{Amp} \cdot \sin(S) \quad (36.c)$$

$$V_Y(n) = -K_{Amp} \cdot \cos(S) \quad (36.d)$$

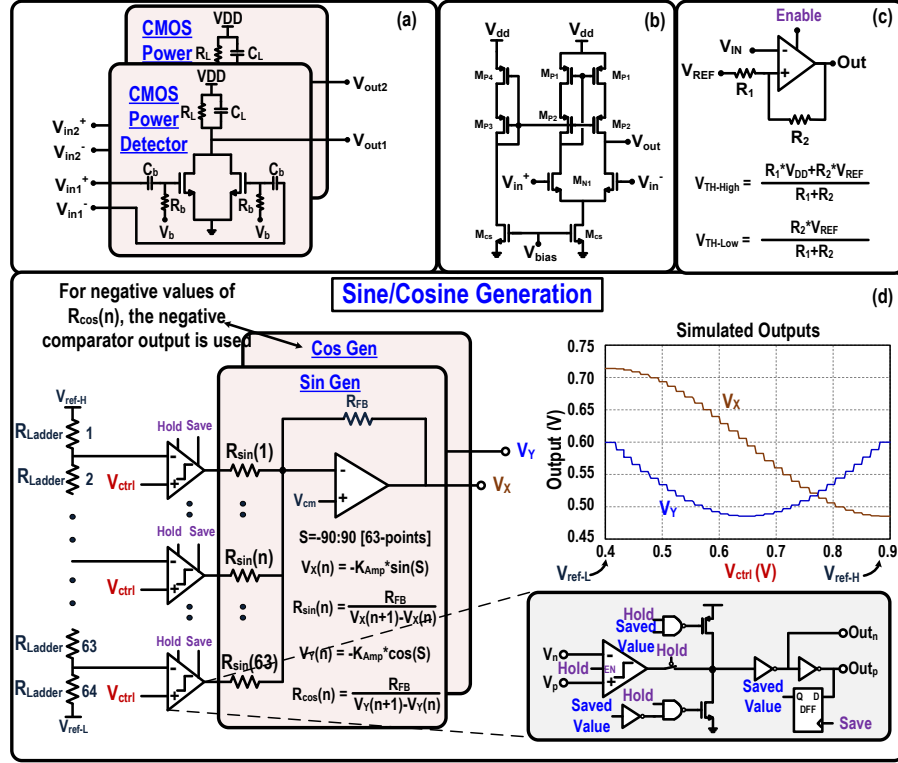


Figure 35 Circuit Details of (a) CMOS Power Detector Circuit (b) Op-amp (c) Hysteresis Comparator (d) Sine/Cosine Generation Circuit

However, if $|\theta - \Phi|$ is greater than 90° , the feedback loop will stay in the positive feedback region and V_{ctrl} will keep moving away from the stable point until it is clipped by either reference voltages. This can happen during system start-up or when θ changes by more than 90° . To solve this potential out-of-lock issue, we adopt an out-of-range automatic correction loop (figure 34). When V_{ctrl} moves out of the accepted range between V_{ref-L} and V_{ref-H} (flash ADC low and high reference voltages), it will trigger the hysteresis comparators (Figure 34(c)) to generate a flag. If $V_{ctrl} > V_{ref-H}$, a flag “high” is generated. The flag “high” will activate transistor MN to bring the V_{ctrl} back to the lower half of the voltage range. Alternatively, if $V_{ctrl} < V_{ref-L}$, a flag “low” will be generated. The flag “low” will activate transistor MP to bring V_{ctrl} back to the higher part of the voltage range. In either case, the main loop is brought back to either a negative feedback region or a “safe” positive feedback region where proper locking can be achieved and the hysteresis comparator, in turn, will be turned off. The hysteresis comparators are based on positive feedback Schmitt trigger amplifiers.

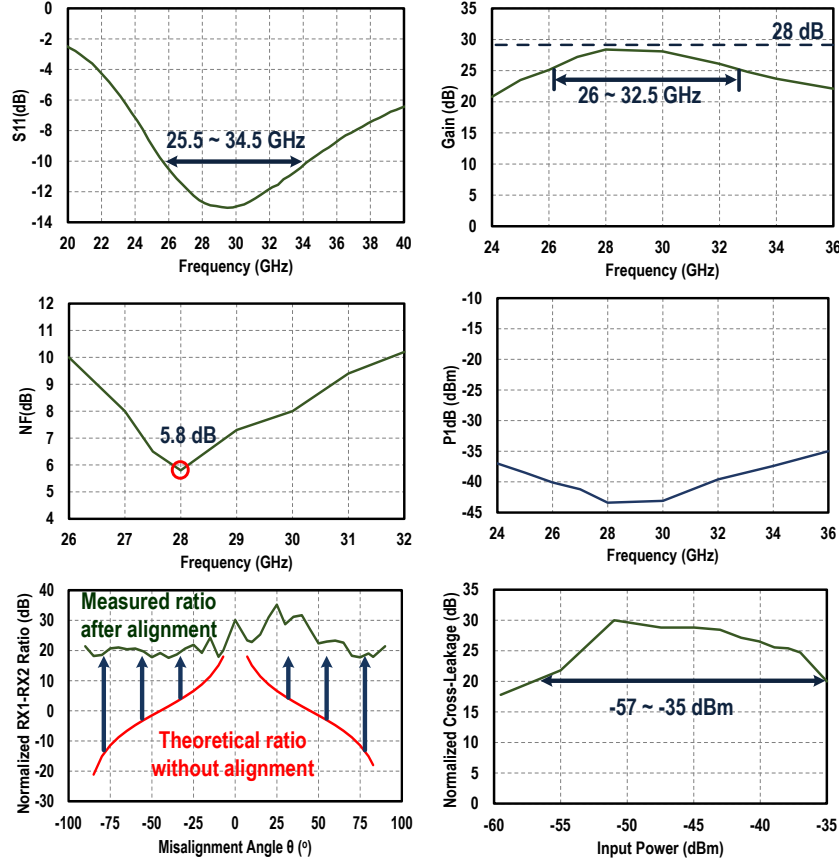


Figure 36 Measured RX S11, Gain, P1dB and NF Across Frequency Range, as well as the Measured Autonomous Polarization Alignment Performance Over the Entire -90° to $+90^\circ$ Polarization Mismatch Range

6.3 Experimental Results

The dual-polarization RX front-end is implemented in GlobalFoundries 45RFSOI CMOS process. All DC and biasing pads are wire-bonded to the PCB, and the RF/LO signals are probed. The measured S_{11} is <-10 dB across 25.5~34.5 GHz (Figure 37). The measured RX maximum gain is 28dB with a 3dB gain-bandwidth of 26~32.5 GHz. The measured NF is 5.8 dB at 28 GHz with RX input P_{1dB} of around -40 dBm. In addition, the autonomous polarization loop achieves 18~32 dB of cross-leakage suppression ratio. The implemented RX is measured using concurrent wideband modulated dual-polarized signals across θ as shown in figure 38. With implemented dual-polarization cancellation technique, the desired signals are successfully demodulated across θ with less than -20dB EVM (16QAM 1.2Gb/s), -21dB EVM (64QAM 1.2Gb/s), and -20dB EVM (64 QAM 1.8Gb/s).

This work presents a dual-polarization receiver front-end implementing an analog/mixed-signal autonomous polarization alignment technique. Table IV shows the comparison between implemented receiver front-end and state-of-art dual-polarization receiver front-ends with antenna misalignment correction functions. The implemented front-end shows the first dual-polarization receiver with $<9\mu s$ latency, 18-32dB misalignment suppression, and Gb/s data rate, which enables future URLLC applications.

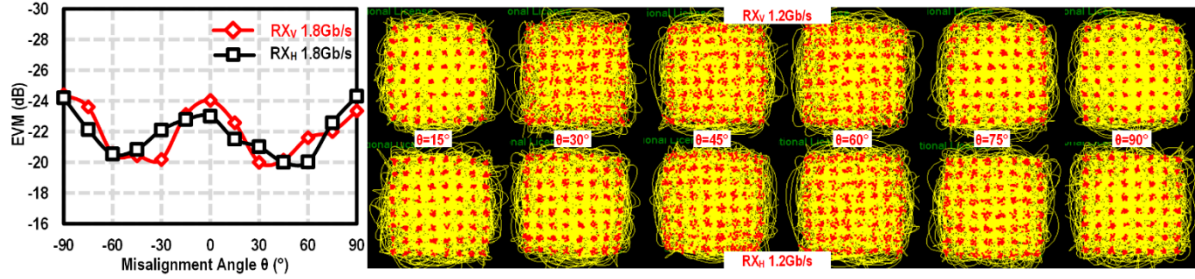


Figure 37 The Measured SNR(MER) for Outputs RXH and RXV with 1.8Gb/s 64QAM Modulation and the Measured Constellation of Outputs RXH and RXV with 1.8Gb/s 64QAM Modulation when Misalignment Angles θ vary from 15° to 90° .

TABLE. IV Comparison with recently reported state-of-the-art Designs

	This Work	Dasgupta [2] JSSC '18	Sadhu [3] JSSC '17	Chi [6] JSSC '18	Dinc [7] JSSC '16	Yao [8] RFIC '19
Technology	45nm SOI CMOS	28nm CMOS	130nm SiGe	45nm SOI CMOS	45nm SOI CMOS	180nm SiGe BiCMOS
Frequency (GHz)	28	60	28	63	59	62
Gain (dB)	28	34 ¹ (RX CG)	30 ¹	10.9	40	14 (LNA Gain)
Bandwidth (GHz)	26~32.5	N/R	27~28.5 ¹	60~75	NR	56~68
NF _{DSB} (dB)	5.8	7.6 ¹	6 (LNA + Switch)	4.8	4	7
Modulation	16QAM ³ : 1.2Gb/s (-20dB EVM) 64QAM ³ : 1.2Gb/s (-21dB EVM) 1.8Gb/s (-20dB EVM)	16QAM ² 27.8 Gb/s (-18 dB EVM)	N/R	16QAM ² 3 Gb/s (-19.8 dB EVM)	N/R	N/R
Dual-Pol Leakage Suppression (dB)	18 ~ 32	N/R	N/R	N/A	N/A	N/A
Response time	< 9 μ s	N/R	N/A	N/A	N/A	N/A
Power (mW) / RX Element	68	110 (RX+LO)	103	108	111 (RX+LO)	37.2 (LNA)
Pin1dB (dBm)	-40	N/R	-22.5	N/R	-40	N/R
Area (mm ²)	5.67	3.9 (Per Element)	166 (Overall)	7.29 (TRX+Ant.)	4.42 (TRX Chip)	9 (TRX+Ant.)
Function	Autonomous Polarization Alignment Without baseband computation	Dual-pol MIMO	Total 128TRX in package with dual pol	Multi-feed Antenna SIC	Full-duplex TRX with antenna and SIC	Polarization-Duplex STAR TRX Antenna IC

6.4 PUBLICATIONS SUMMARY

1. 7 conference papers:
 - a. 4 papers accepted for publication at the Government Microcircuit Applications and Critical Technology Conference (GOMACTech) in March 2019, March 2021 (2 papers), and March 2022;
 - b. 2 papers presented at the IEEE Custom Integrated Circuits Conference (CICC) in April 2021 and to appear in March 2020;
 - c. 1 paper presented at the IEEE Radio Frequency Integrated Circuits (RFIC) in June 2022.
2. 5 journal papers:

- a. 3 papers published in IEEE J. of Solid-State Circuits in March 2021, December 2019, and March 2021 (Best Student Paper Award finalist);
- b. 1 paper published in IEEE Solid-State Circuits Lett. in 2021;
- c. 1 paper published in IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers in February 2019.

The detailed list is the following:

[1] B. Lin, T.-Y. Huang, A. Ahmed, M. Huang, and H. Wang, “A 23-37GHz Autonomous Two-Dimensional MIMO Receiver Array with Rapid Full-FoV Spatial Filtering for Unknown Interference Suppression” has been accepted for publication at the IEEE CICC conference 2022. — **Best Student Paper Award finalist.**

[2] B. Lin, A. Ahmed, and H. Wang, “A 26-32 GHz Dual-Polarization Receiver Frontend with Rapid-Response Mixed-Signal Polarization Alignment for Ultra-Reliable Low Latency Communications,” IEEE Solid-State Circuits Lett., vol. 4, pp. 222-225, 2021.

[3] A. Ahmed, M. Huang, D. Munzer, and H. Wang, “A 43-97 GHz Mixer-First Front-End with Quadrature Input Matching and On-chip Image Rejection,” IEEE J. of Solid-State Circuits, vol. 56, no. 3, pp. 705 – 714, Mar. 2021.

[4] A. Ahmed, B. Lin, and H. Wang, “A Mm-Wave Wideband Dual-Polarization Receiver with Autonomous Rapid-Response Polarization Alignment in Highly Dynamic and Unknown Mobile Environments,” Proc. The Government Microcircuit Applications and Critical Technology Conference (**GOMACTech**), Mar. 2021.

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[7] A. Ahmed, M. Huang, H. Wang, “A Mixer-First Extremely Wideband 43-97 GHz RX Frontend with Broadband Quadrature Input Matching and Current Mode Transformer-Based Image Rejection for Massive MIMO Applications,” accepted and to appear in Proc. IEEE Custom Integrated Circuits Conference (**CICC**), Mar 2020. — **Best Student Paper Award finalist.**

[8] M. Huang and H. Wang, “A Wideband 27-41GHz N-Input-N-Output MIMO Receiver Using Scalable Cascadable Autonomous Array-Based High-Order Spatial Filters for Instinctual Full-FoV Multi-Blocker Suppression and Signal Beamforming,” Proc. The Government Microcircuit Applications and Critical Technology Conference (**GOMACTech**), Mar. 2019.

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7 CONCLUSION

In summary, throughout the duration the project, we designed and demonstrated multiple next generation wireless frontend array system architectures that can support wideband communication links and be robust in increasingly complex and dynamic EM environment. The demonstrated system can also support the wireless communication links with ‘smart’ front-end functionalities such as autonomous spatial filters and dynamic array operations. In total, we published 11 papers, including 7 conference papers and 5 journal papers.

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LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS

ACRONYM	DESCRIPTION
AB	Autonomous Beamformer
ADCs	Analog-to-Digital Converters
AoA	Angle-of-Arrival
AWG	Arbitrary Waveform Generator
CG	CONVERSION gain
CLC	Coupled-Line Coupler
CMOS	Complementary Metal Oxide Semiconductor
CPE	Customer Premise Equipment
CW	Continuous Wave
D2X	Drone-to-Everything
DLL	Delay-Lock-Loop
DSP	Digital Signal Processing
EM	Electromagnetic
FoV	Field-of-View
IF	Intermediate Frequency
IP3	Intermodulation Performance
ITS	Intelligent Transportation Systems
LNA	Low Noise Amplifiers
LO	Local Oscillator
MGTRs	Multi-Gated Transistors
MIMO	Multiple-Input and Multiple-Output
MISO	Multiple-Input Single-Output
RF	Radio Frequency
SATCOM	SATCOM-on-the-Move
SNR	Signal-to-Noise Ratio
TX	Transmitter
URLLC	Ultra-Reliable Low Latency Communications
V2X	Vehicle-to-Everything
VGA	Variable-Gain Amplifier