3DHI and the Coming Inflection Point in Microelectronics Manufacture

Mark Rosker, MTO Director

Briefing prepared for GOMACTech 2023

21 March 2023

CHIPS and chips


Forbes

BREAKING • BUSINESS

CHIPS Act Passes: House Approves $280 Billion Bill To Boost Microchip Production And Counter China

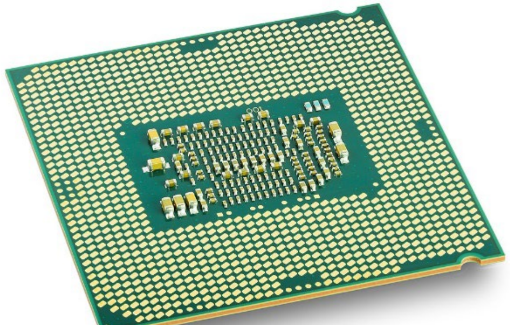
Brian Bushard Forbes Staff

I cover breaking news for Forbes

Jul 28, 2022, 03:26pm EDT

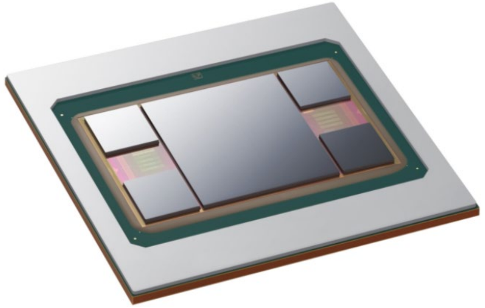
Source: Forbes

Source: CNET



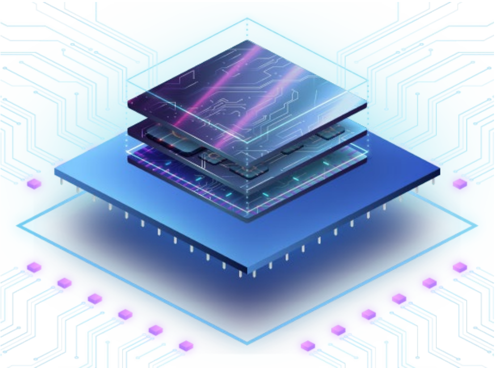
2D

Intel i7



2.5D

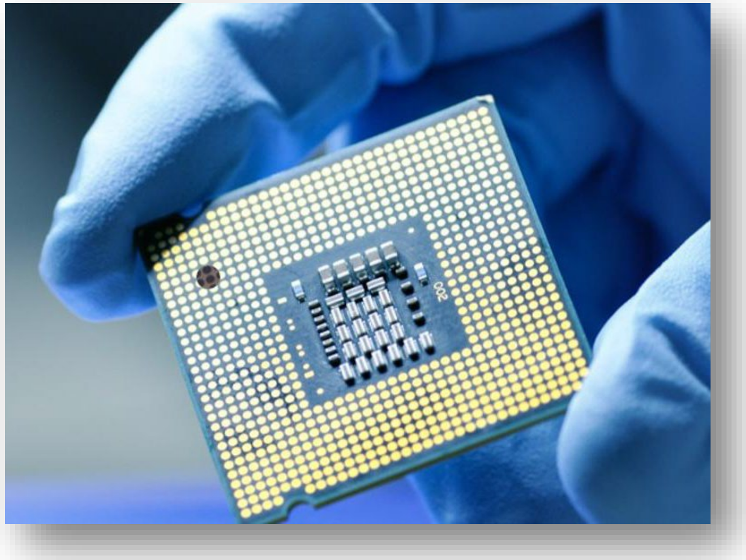
Samsung I-Cube4

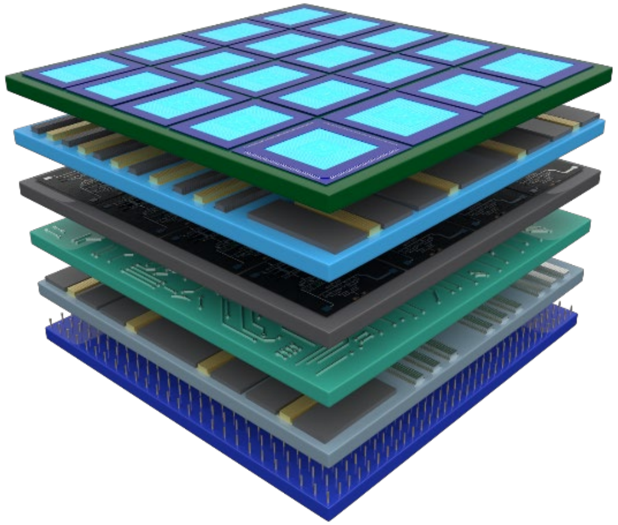


3D

Concept

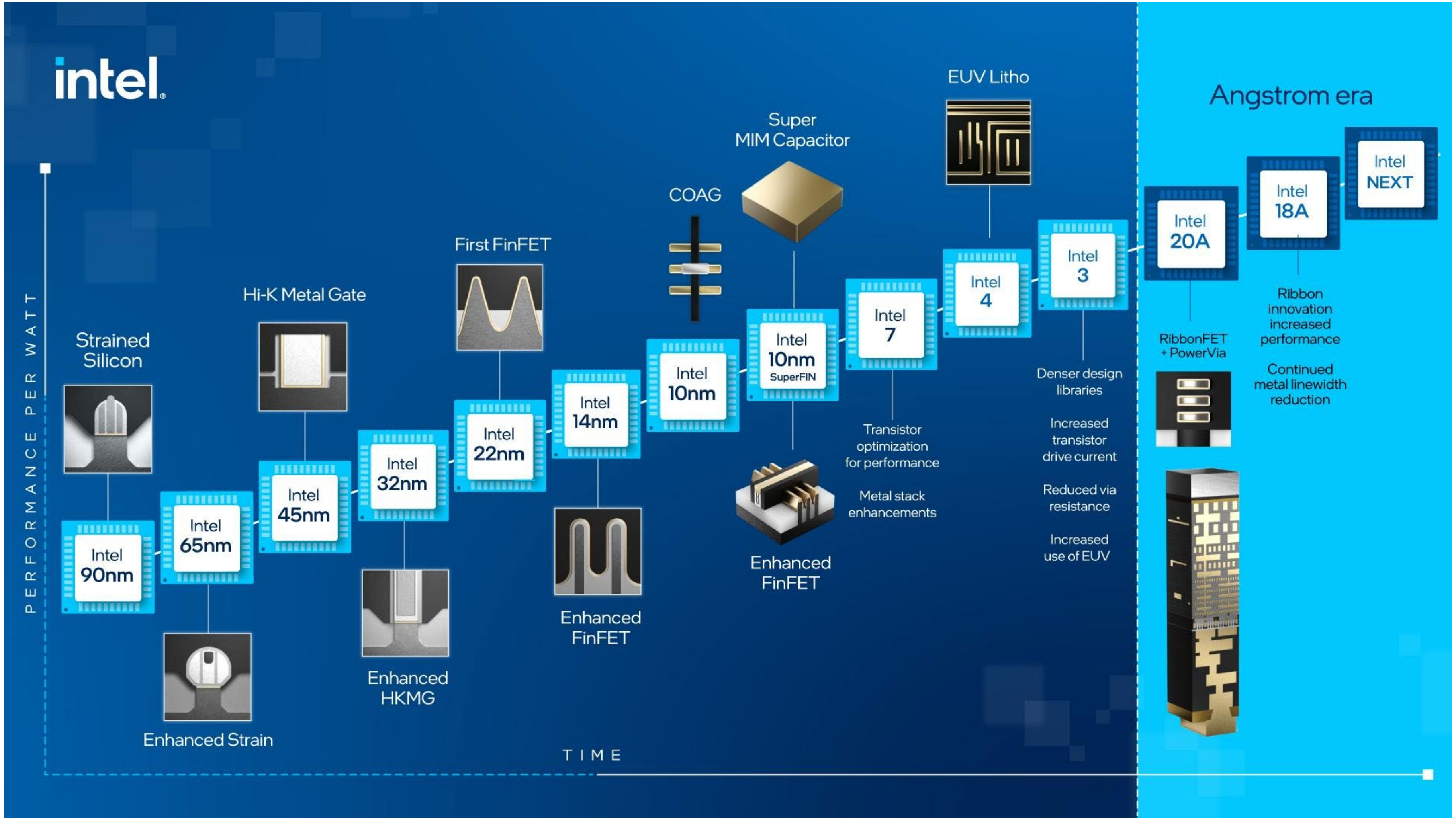
What are “chips”?



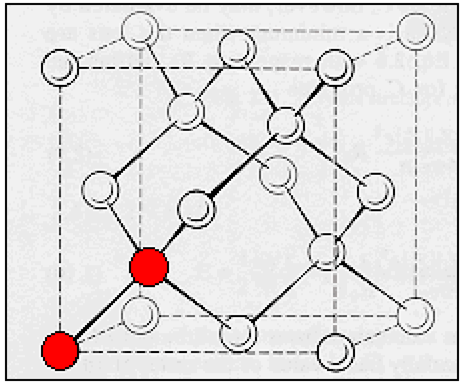


Today	Future
2D	3D with dense interconnects
Monolithic integration	Disaggregation
Silicon	Multi-process / multi-material
Packaged after fabrication	Packaging no longer distinct

Geometric scaling



Silicon



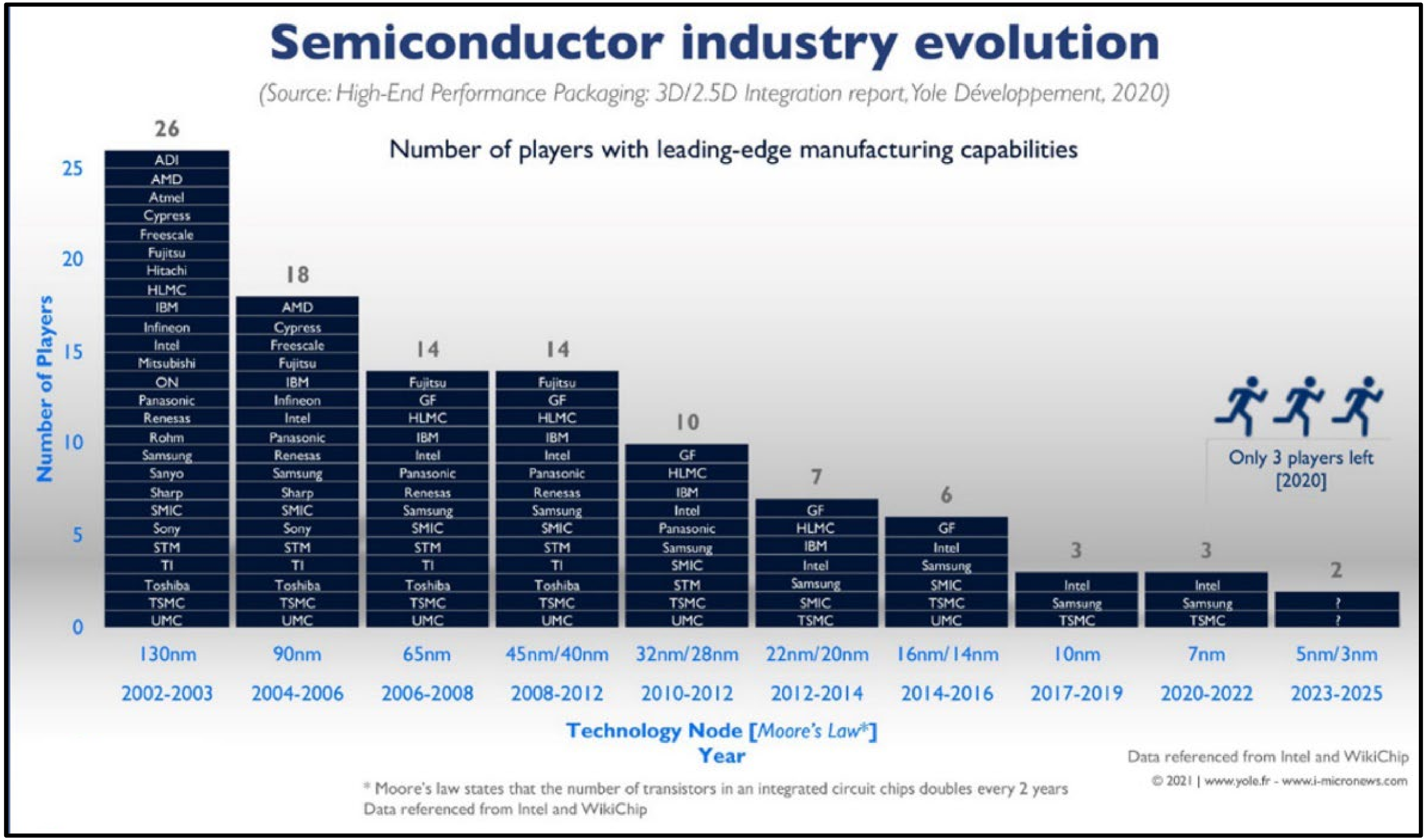
Source: Princeton

Nearest neighbor: 0.235 nm
Lattice parameter: 0.543 nm

Other scaling failure modes

- Leakage current increase
- Transistor turn-off / turn-on
- Oxide layers
- Barrier layers
- Contact quality
- Transistor area

Economic scaling



Semiconductor industry evolution

(Source: High-End Performance Packaging: 3D/2.5D Integration report, Yole Développement, 2020)

Number of players with leading-edge manufacturing capabilities

Data referenced from Intel and WikiChip

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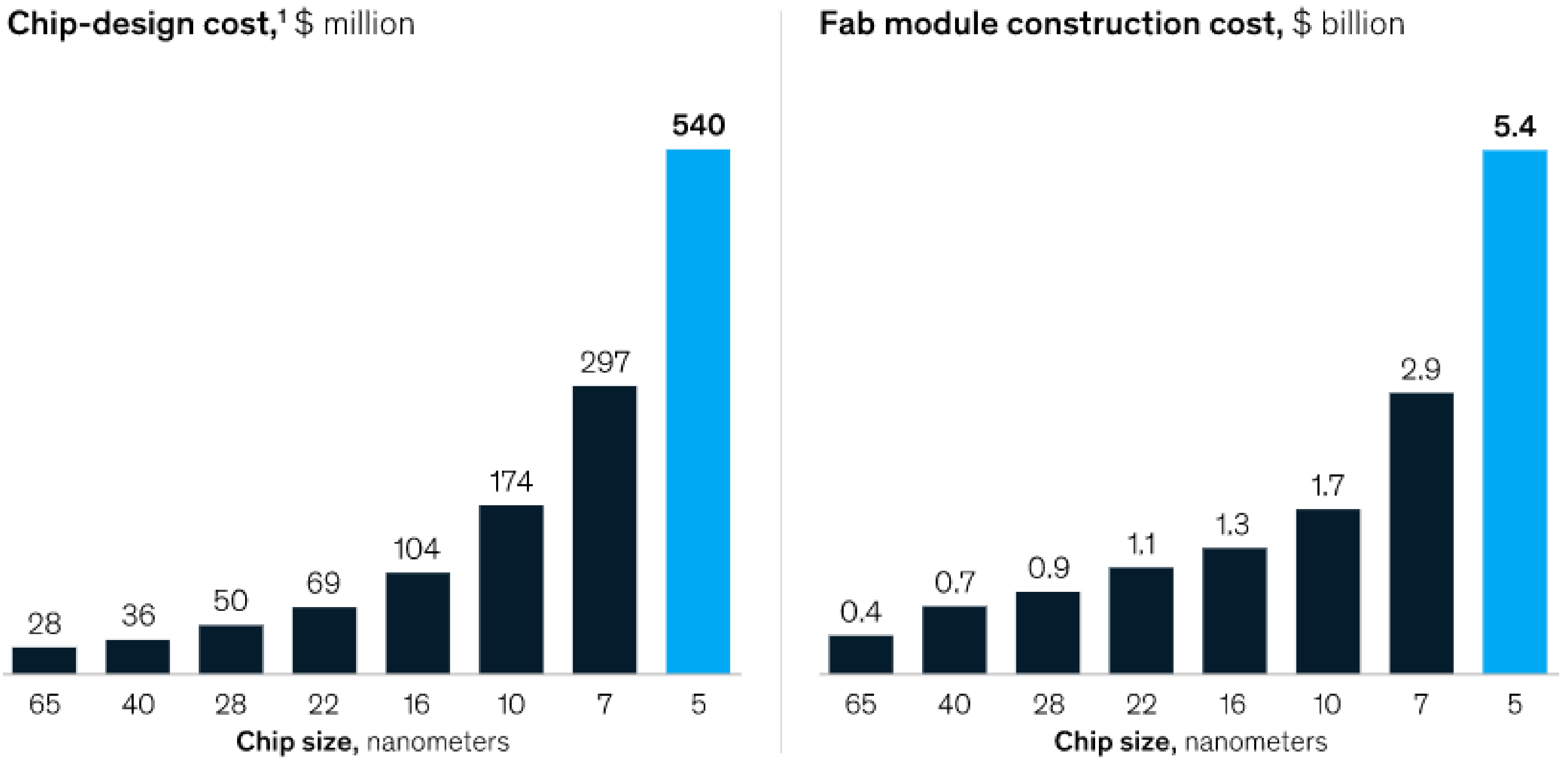
* Moore's law states that the number of transistors in an integrated circuit chips doubles every 2 years
Data referenced from Intel and WikiChip

Economies of scale in semiconductor manufacturing

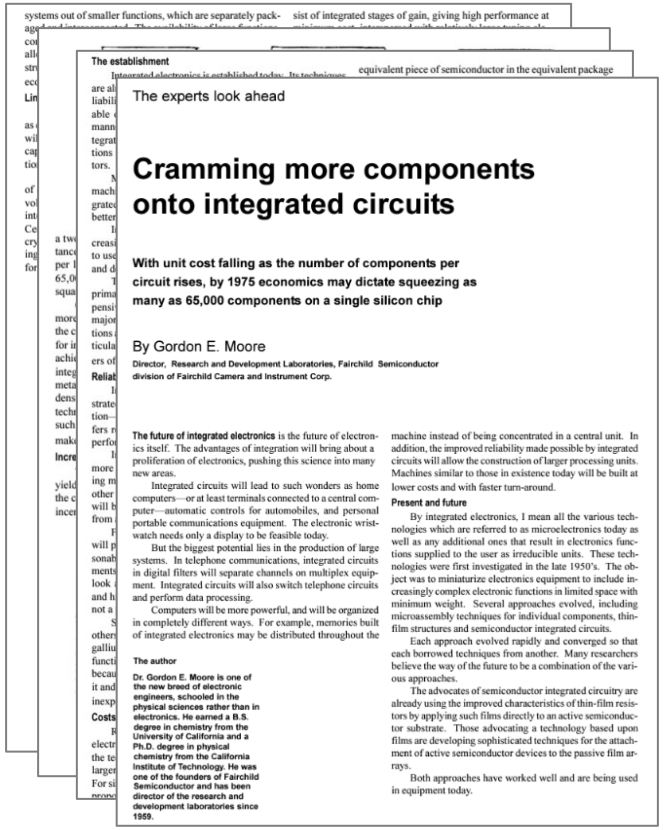
R&D for chips and fab module construction costs are soaring.



[1] Major components include IP qualification, architecture, verification, physical, software, prototyping, and validation.

Source: IBS/McKinsey, "Semiconductor design and manufacturing: Achieving leading-edge capabilities," McKinsey, 2020

Disaggregation*



The experts look ahead

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

Computers will be more powerful, and will be organized in completely different ways. For example, memories built of integrated electronics may be distributed throughout the machine instead of being concentrated in a central unit. In addition, the improved reliability made possible by integrated circuits will allow the construction of larger processing units. Machines similar to those in existence today will be built at lower costs and with faster turn-around.

Present and future

By integrated electronics, I mean all the various technologies which are referred to as microelectronics today as well as any additional ones that result in electronics functions supplied to the user as irreducible units. These technologies were first investigated in the late 1950's. The object was to miniaturize electronics equipment to include increasingly complex electronic functions in limited space with minimum weight. Several approaches evolved, including microassembly techniques for individual components, thin-film structures and semiconductor integrated circuits.

Each approach evolved rapidly and converged so that each borrowed techniques from another. Many researchers believe the way of the future to be a combination of the various approaches.

The advocates of semiconductor integrated circuitry are already using the improved characteristics of thin-film resistors by applying such films directly to an active semiconductor substrate. Those advocating a technology based upon films are developing sophisticated techniques for the attachment of active semiconductor devices to the passive film arrays.

Both approaches have worked well and are being used in equipment today.

The author

Dr. Gordon E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been director of the research and development laboratories since 1959.

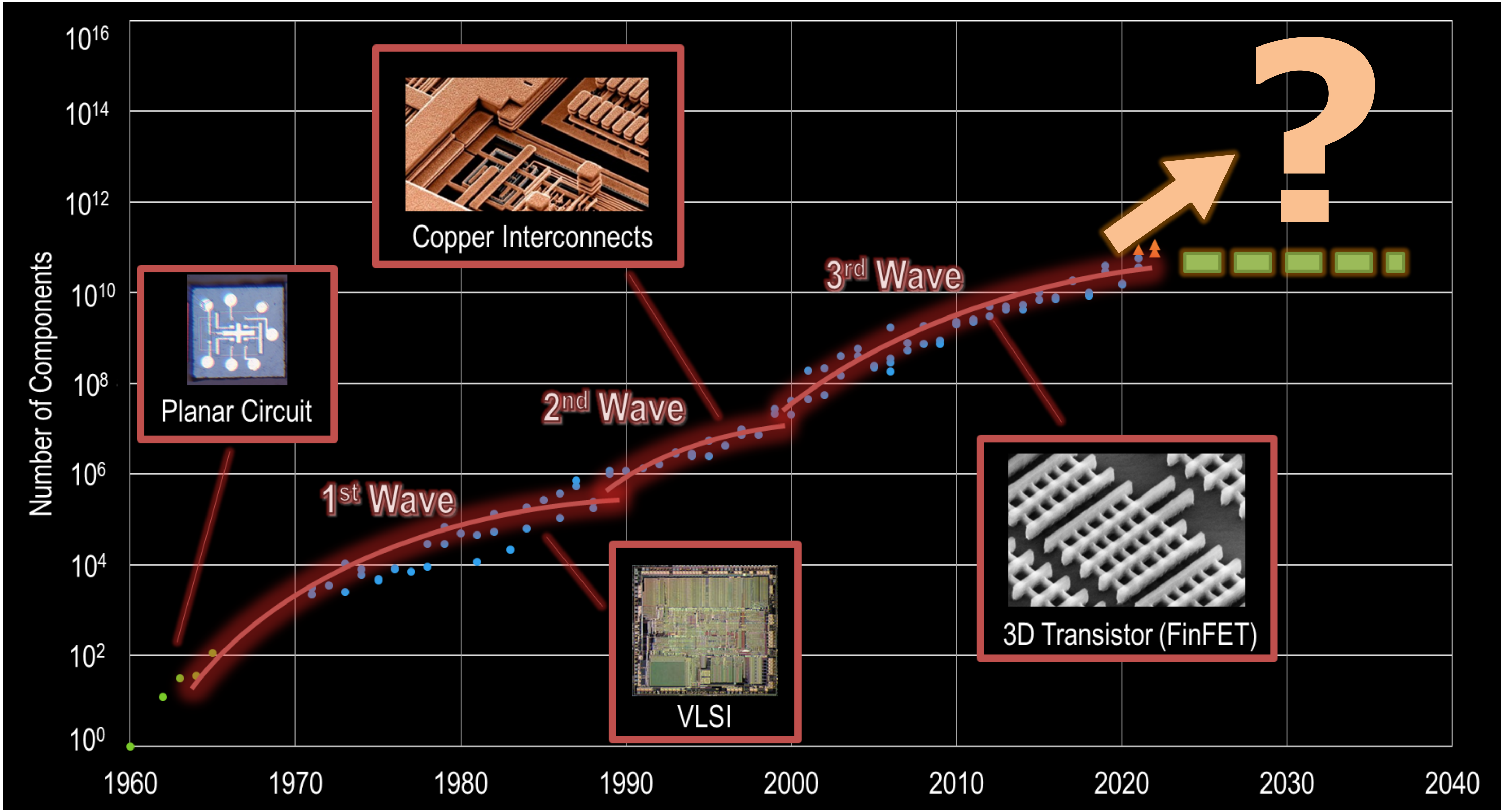
Source: Electronics, Volume 38, Number 8, April 19, 1965

> "It may prove more economical to **build large systems out of smaller functions, which are separately packaged and interconnected**. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically."
>
> – Gordon Moore

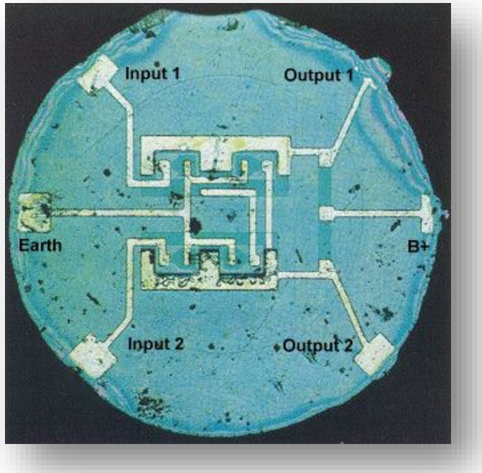
*a.k.a.

- *Polylithic*
- *Pseudo-lithic*
- *Chiplet-based*
- *3DHI*

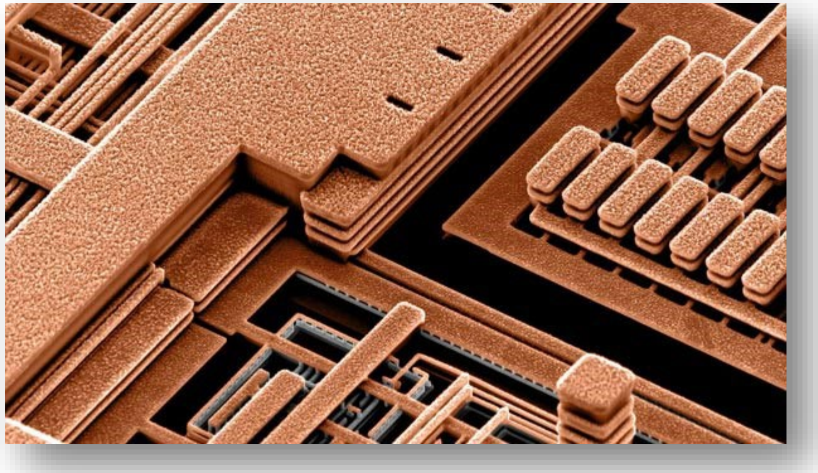
Progress in microelectronics



Monolithic integration – 1961-present



Monolithic Silicon Integrated Circuit (1961)
Source: Chiphistory.org



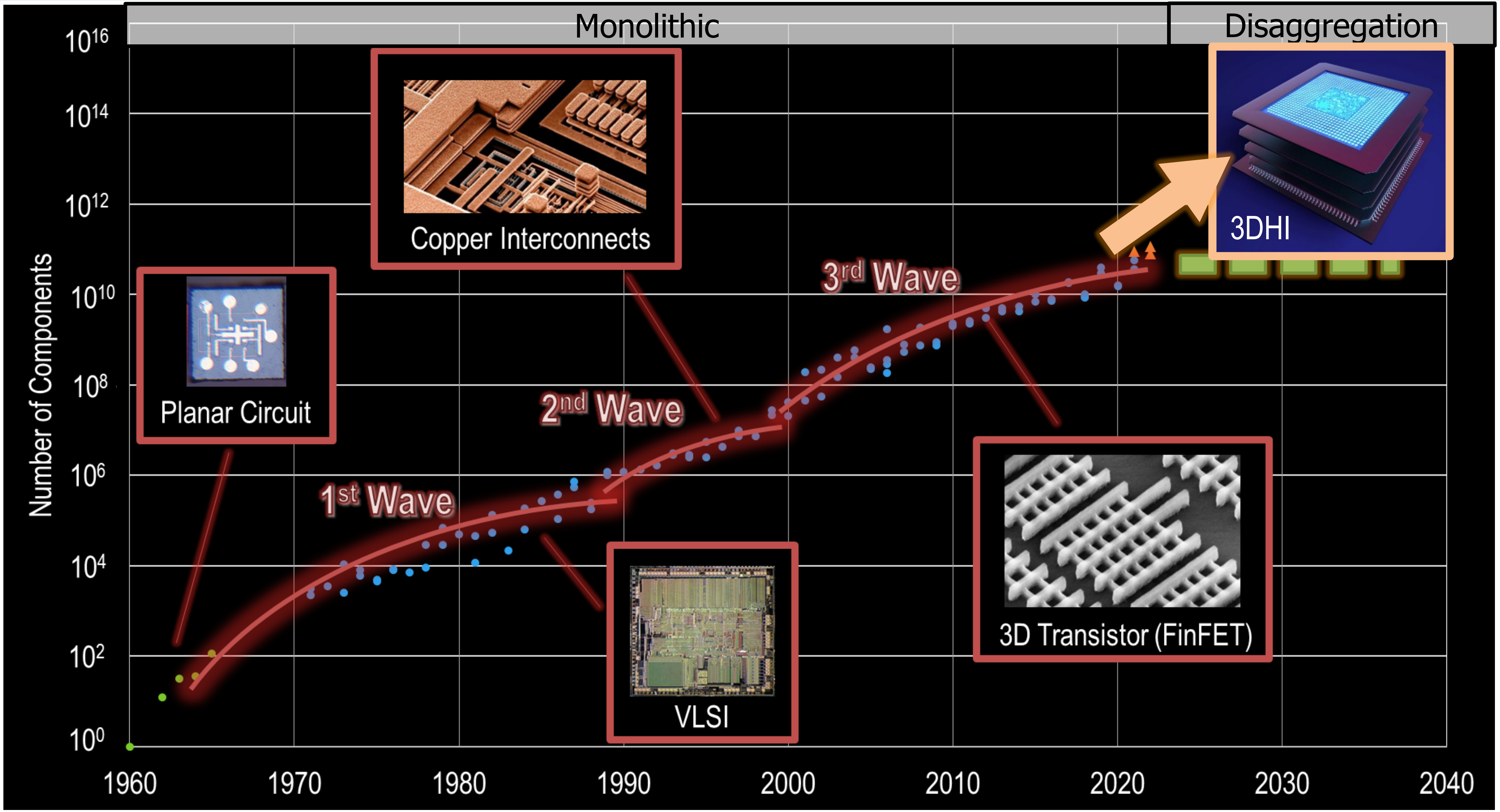
3D Copper Interconnect (1997)
Source: Chiphistory.org

Trillion Transistor Chip (2019)
Source: Spectrum.IEEE.org

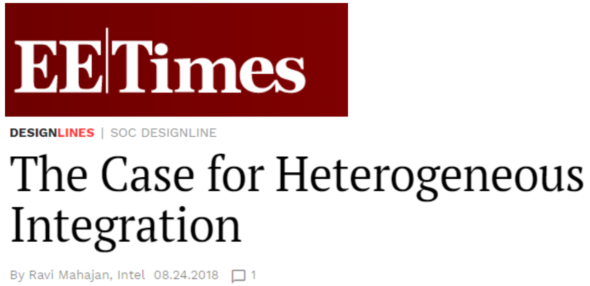
Source: TSMC

Monolithic integration characterized the first three waves

Progress in microelectronics

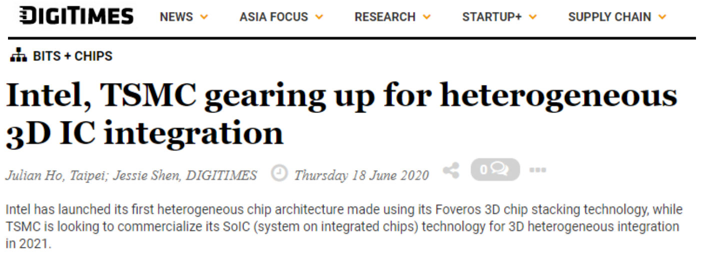


The next wave: 3DHI



The Case for Heterogeneous Integration

By Ravi Mahajan, Intel 08.24.2018 1



Intel, TSMC gearing up for heterogeneous 3D IC integration

Julian Ho, Taipei; Jessie Shen, DIGITIMES *Thursday 18 June 2020*

Intel has launched its first heterogeneous chip architecture made using its Foveros 3D chip stacking technology, while TSMC is looking to commercialize its SoIC (system on integrated chips) technology for 3D heterogeneous integration in 2021.

Heterogeneous integration of rigid, soft, and liquid materials for self-healable, recyclable, and reconfigurable wearable electronics

Chuanqian Shi[1,2,*], Zhanan Zou[2,*], Zepeng Lei[3], Pengcheng Zhu[2,4], Wei Zhang[3,†] and Jianliang Xiao[2,†]

+ See all authors and affiliations

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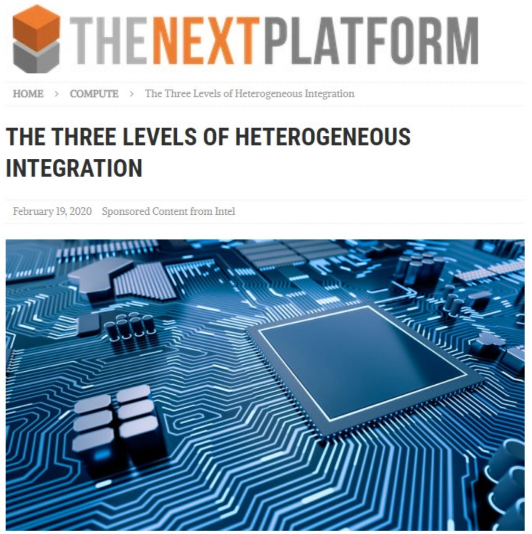
DOI: 10.1126/sciadv.abd0202

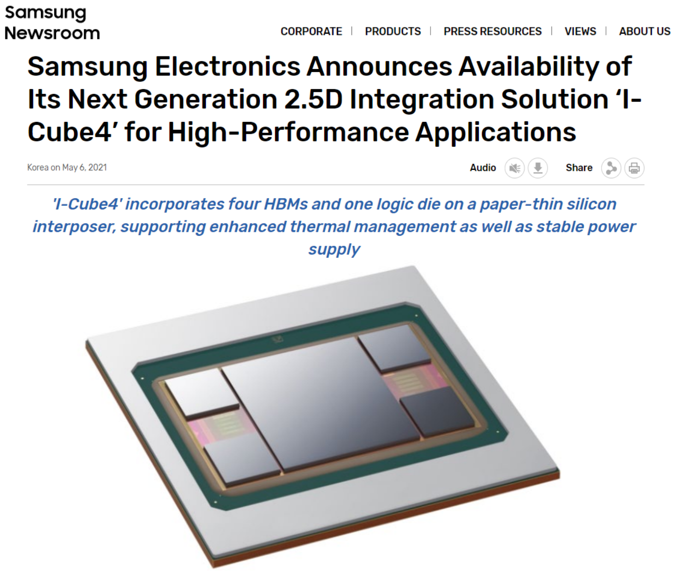
HETEROGENEOUS INTEGRATION ROADMAP

2019 Edition



THE THREE LEVELS OF HETEROGENEOUS INTEGRATION

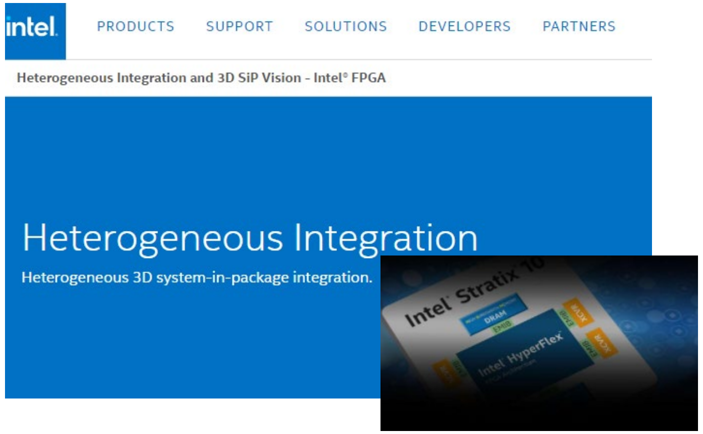
February 19, 2020 Sponsored Content from Intel



Samsung Electronics Announces Availability of Its Next Generation 2.5D Integration Solution 'I-Cube4' for High-Performance Applications

Korea on May 6, 2021

'I-Cube4' incorporates four HBMs and one logic die on a paper-thin silicon interposer, supporting enhanced thermal management as well as stable power supply



Heterogeneous Integration and 3D SiP Vision - Intel® FPGA

Heterogeneous Integration

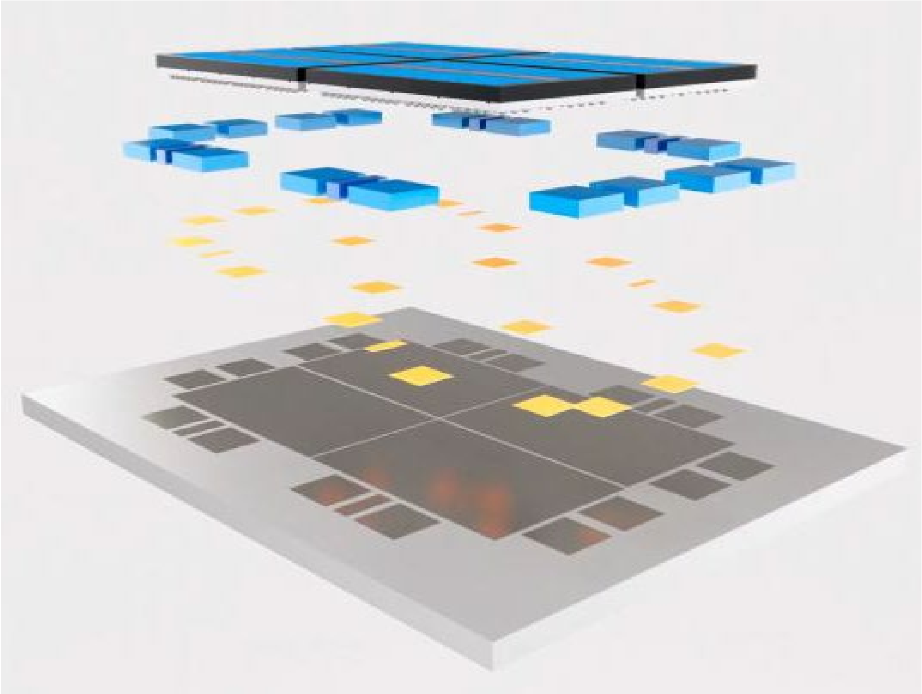
Heterogeneous 3D system-in-package integration.

RAYTHEON'S THREE-DIMENSIONAL HETEROGENEOUS INTEGRATION (3DHI) ELECTRONICS TECHNOLOGY

What is 3DHI?

3D

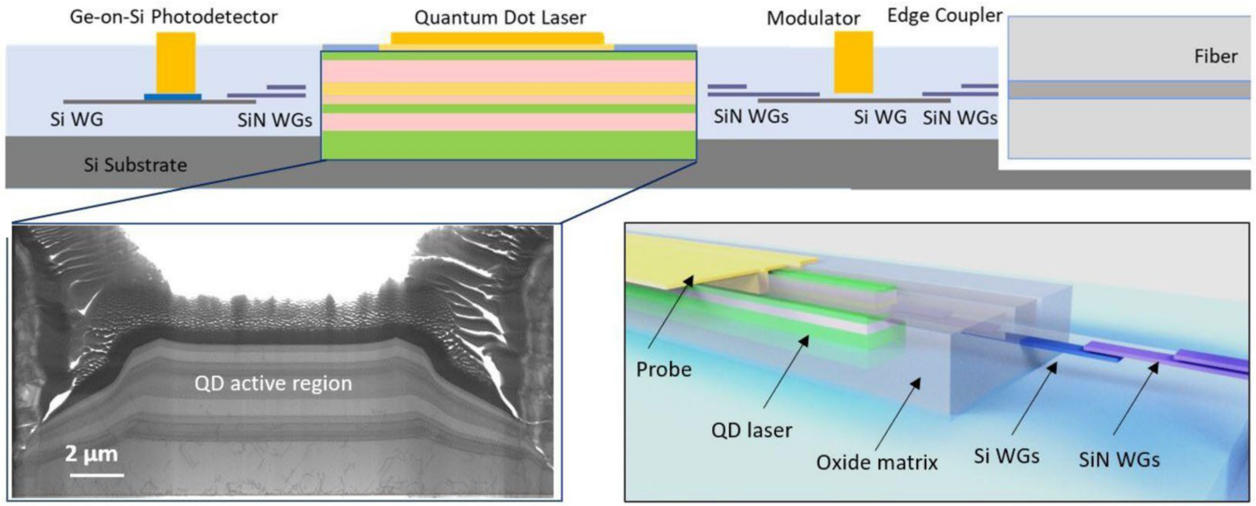
Intel 3D stacked packaging



Source: Intel

HI

High-performance lasers on a 300 mm silicon photonics wafer



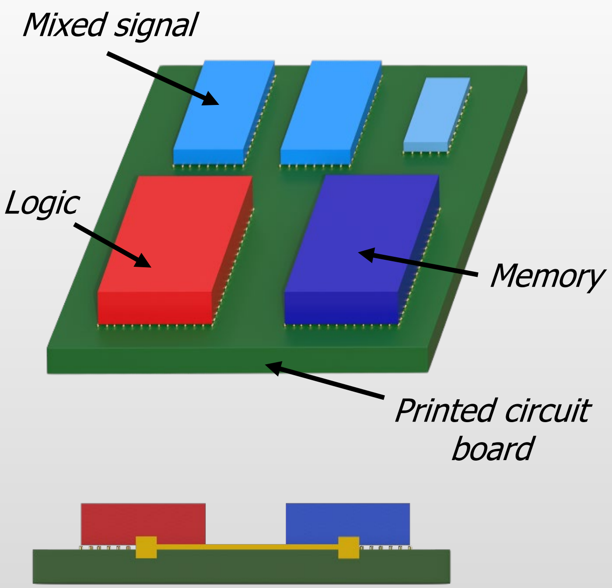
Source: RF-SUNY, IQE, UCSB

3DHI: Three-dimensional heterogeneous integration
Ge: Germanium
QD: Quantum dot

Si: Silicon
SiN: Silicon nitride
WGs: Waveguides

Three Dimensional (3D)

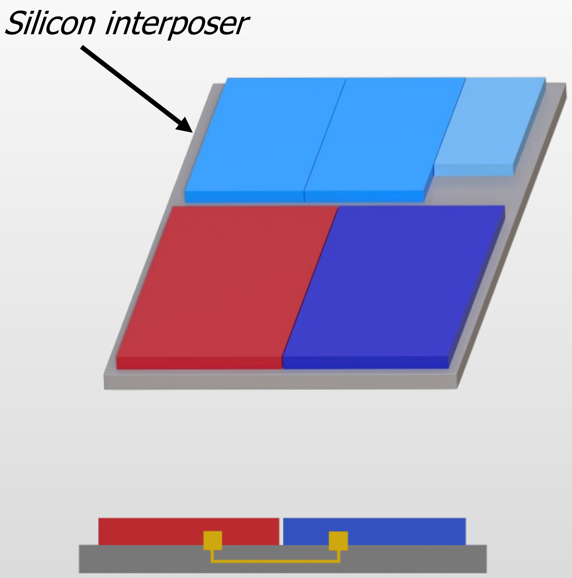
Traditional



Flip chip and wire bonds on printed circuit board

Package interconnect pitch ~ 125 μm

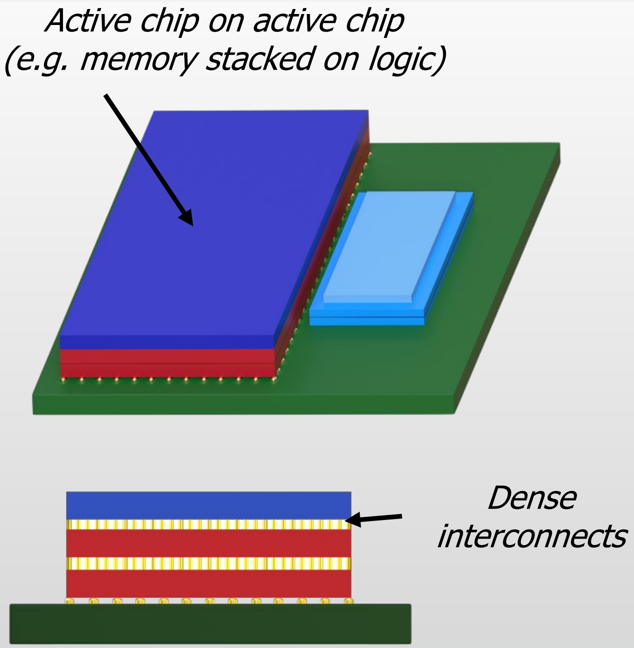
2.5D Interposer



Active chips connected through a passive interposer layer

Interconnect pitch shrinks 4x

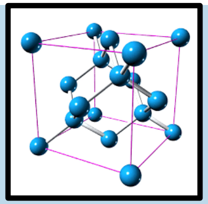
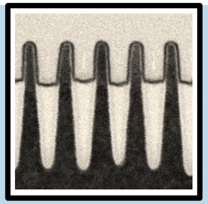
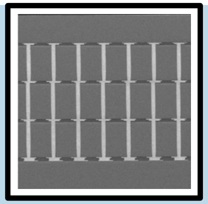
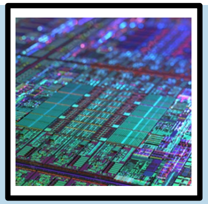
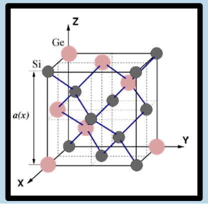
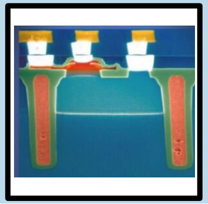
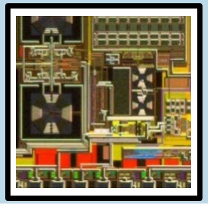
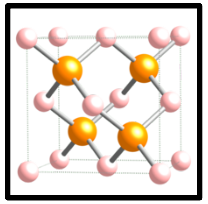
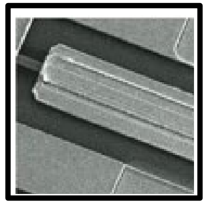
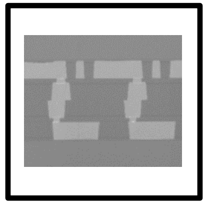
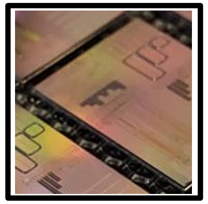
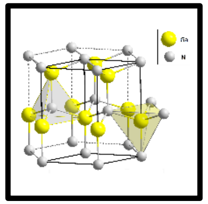
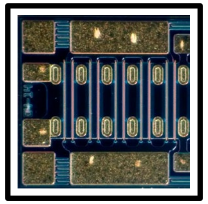
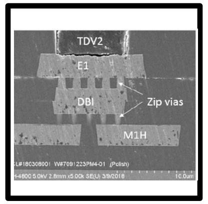
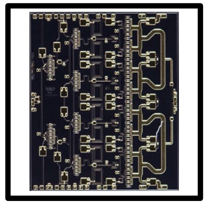
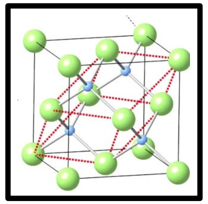
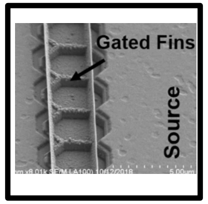
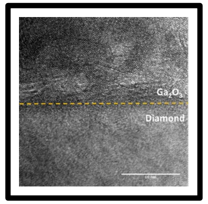
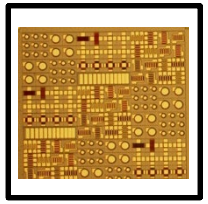
3D



Vertical stacking of active chips

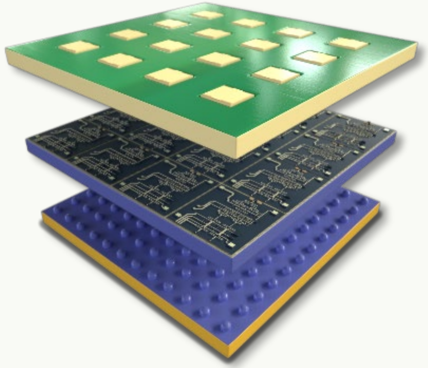
Interconnect pitch shrinks 10x-100x

Heterogeneous Integration (HI)

	Materials	Devices	Process	Function
Traditional Focus	 Silicon	 MOSFET, FinFET, GAAFET	 Bump, μ-Bump, TSV, Hybrid	 Logic, Memory
	 Silicon germanium	 Bi-CMOS, HBTs	 Bump, μ-Bump, TSV, Hybrid	 Analog, Mixed-Signal, RF
Emerging Opportunities	 III-V, II-VI (GaAs, InP, HgCdTe)	 Laser, LED, Detector	 Bump, μ-Bump, TSV, Hybrid	 Photonics, RF
	 Wide bandgap (GaN, SiC)	 HEMT, MESFET, JFET	 Bump, μ-Bump, TSV, Hybrid	 Photonics, RF, Power
	 Ultrawide bandgap (AlGaN, Diamond)	 HEMT, MESFET, JFET	 Bump, μ-Bump, TSV, Hybrid	 Photonics, Power

Why 3DHI?

Performance



Optimized devices

Security

Source: Adobe Stock

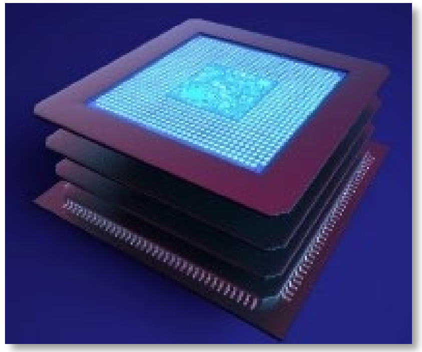
New approaches to incorporate 3D design and assembly

Supply chain

Source: National Association of Manufacturers

Domestic-based processes can be used for assembly

SWaP



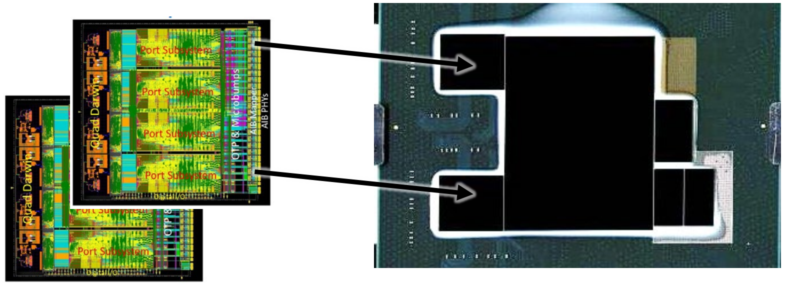
Minimum footprint with maximum efficiency

SWaP: Size, weight, and power

Disaggregation offers performance advantages

Surpasses monolithic designs in performance, cost, and time-to-market

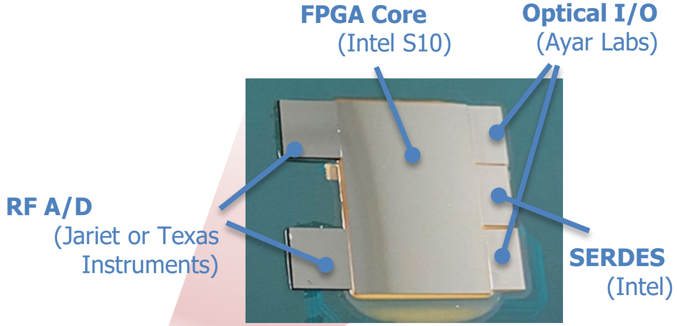
Standard interface (Intel’s AIB) enables modular chiplet ecosystem



Component-level IP with AIB interface…

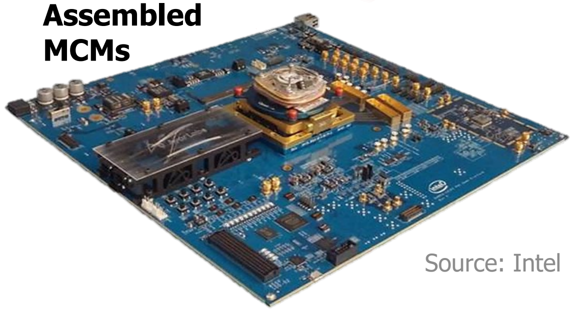
…integrated into high-performance System-in-a-Package (SiP)

Source: Intel

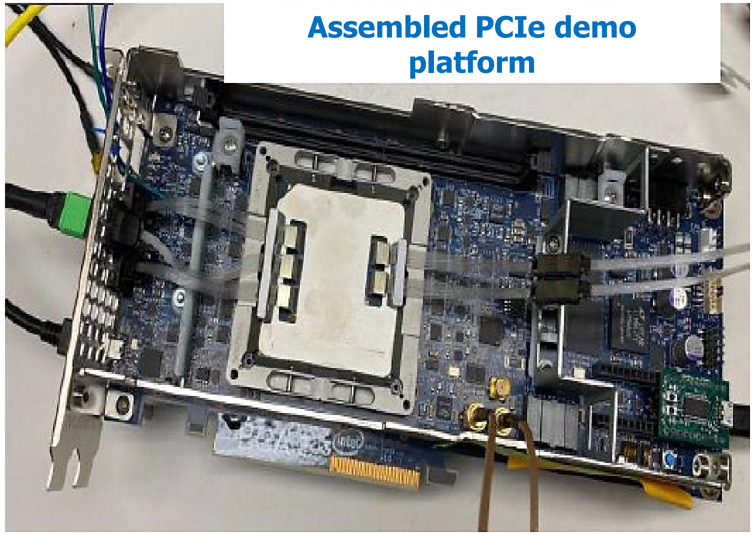


Integrated chiplets

Assembled MCMs



Source: Intel



Source: Intel / Ayar Labs

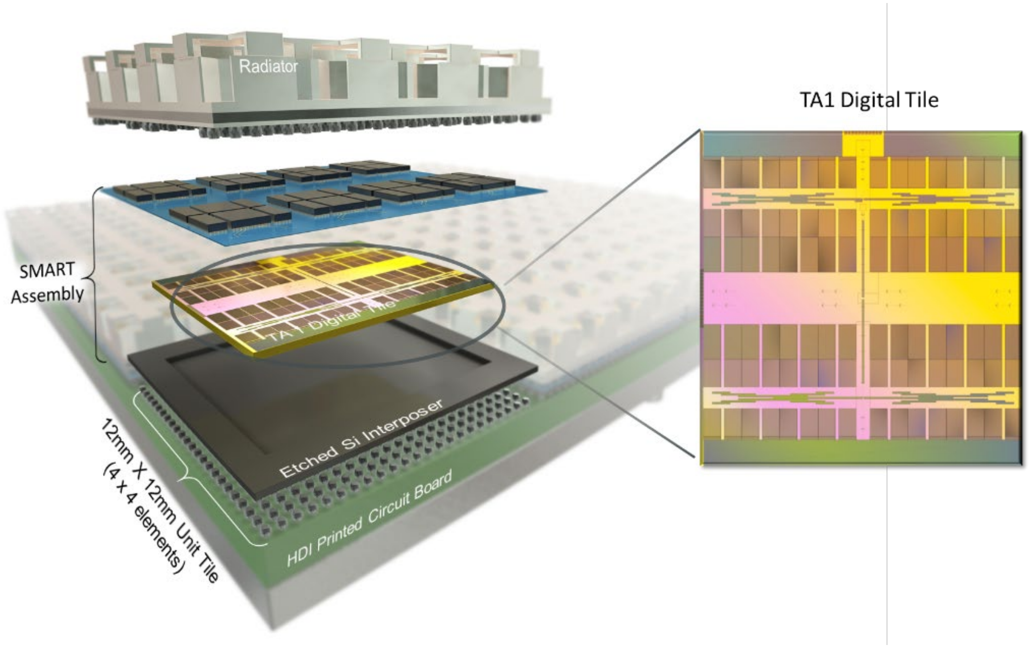
FPGA capable of over 1 Tbps and extendable to over 100 Tbps in total

Common Heterogeneous Integration and IP Reuse Strategies (CHIPS) program
Photonics in the Package for Extreme Scalability (PIPES) program

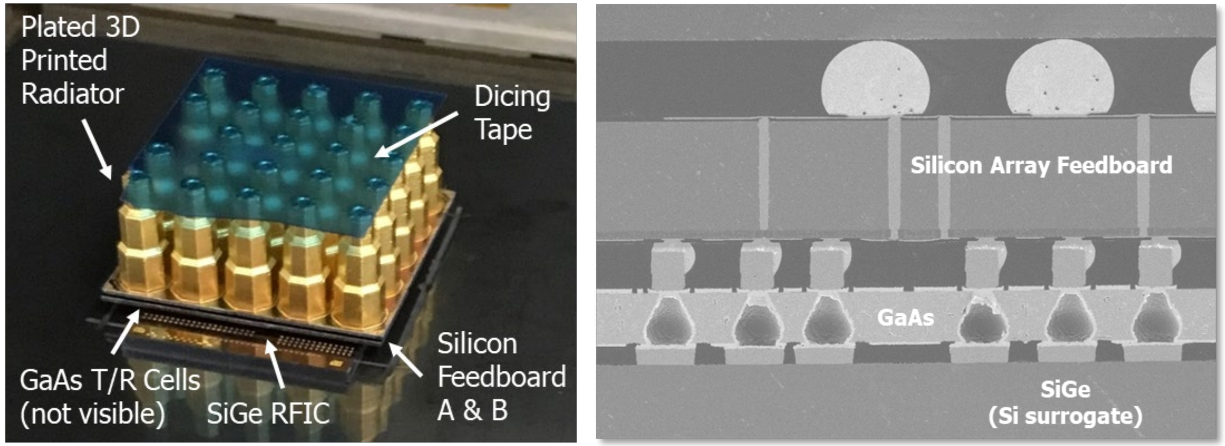
A/D: Analog / digital
AIB: Advanced interface bus
FPGA: Field-programmable gate array
I/O: Input / Output
IP: Intellectual Property
MCM: Multi-chip module
NRE: Non-recurring engineering
SERDES: Serializer / de-serializer

3DHI enables new applications

Demonstrated millimeter wave digital beam forming and integrated arrays from 18-50 GHz



Raytheon 16 element, dual polarized 18-50 GHz scalable tile building block



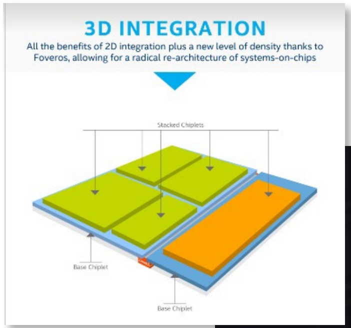
Heterogeneous integration of compound semiconductors and 3D printed notch antenna array (left) cross-section of array stack (right) by Northrop Grumman

Millimeter Wave Digital Arrays (MIDAS) program

CMOS: Complementary metal-oxide semiconductor
GHz: Gigahertz

Making 3DHI electronics real

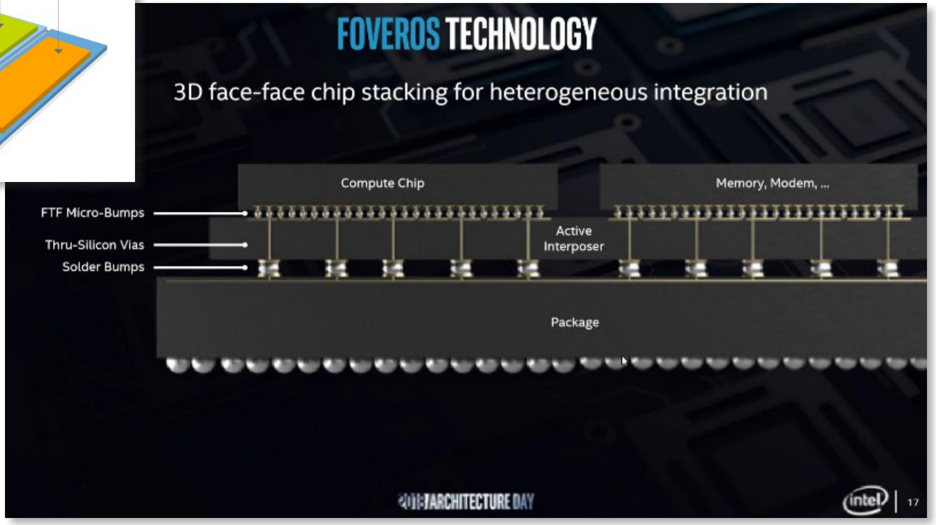
Today



3D INTEGRATION

All the benefits of 2D integration plus a new level of density thanks to Foveros, allowing for a radical re-architecture of systems-on-chips

Source: Intel



FOVEROS TECHNOLOGY

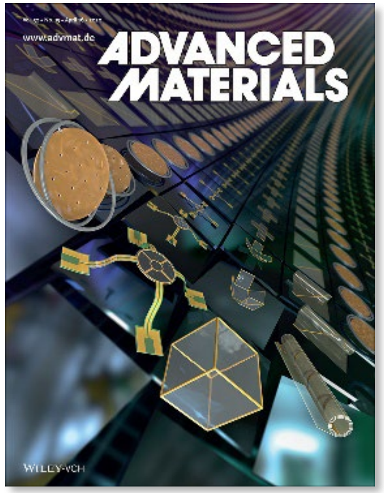
3D face-face chip stacking for heterogeneous integration

Source: Intel

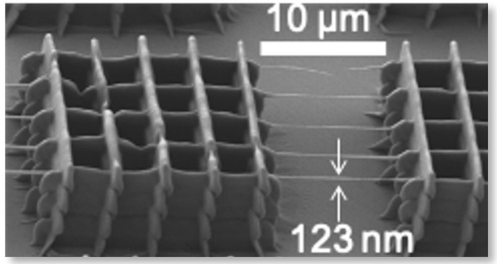
- Only low-power silicon chips
- No embedded thermal management

3DHI technical challenges

- Multi-chip, multi-technology assembly / packaging
- 3DHI interconnects
- Thermal and power
- Tools for design, simulation, and test
- "MOSIS-like" 3DHI prototyping services



3D Microelectronics: 3D Self-Assembled Microelectronic Devices: Concepts, Materials, Applications (Adv. Mater. 15/2020)

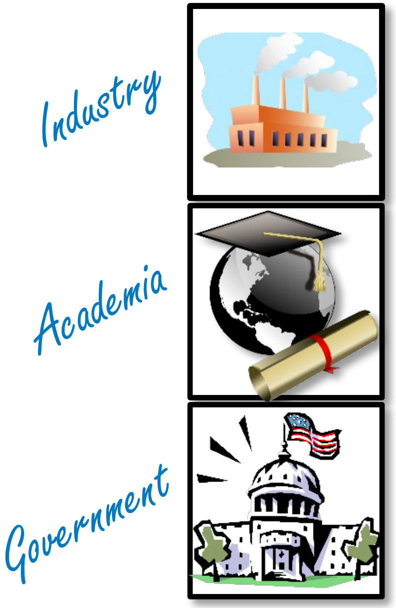


Saha et al., Science, Vol. 366, Issue 6461, pp. 105-109, 2019

Source: Gorodenkoff

Next-Generation Microelectronics Manufacturing (NGMM) program

Users

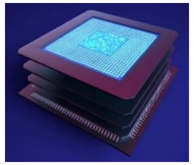


Source: Creative Commons

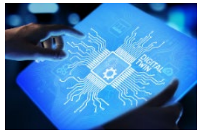
National capability

Source: Adobe Stock

Output



3DHI microsystem prototypes

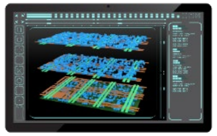


Source: Adobe Stock

Digital twin

Manufacturing process

Source: SUSS



3DHI assembly design kit

3DHI: Three-dimensional heterogeneous integration

NGMM objectives

Phase 0
Define baseline capability

- **Identify process modules and tooling needed**
- **Future customers' input defines baseline for solicitation**

BAA August 2022

Phases 1 and 2
Establish center and R&D services

Phase 1

- **Establish center**
- **Develop baseline process modules**
- **Qualify initial pilot-line processes**

Phase 2

- **Qualify final process modules**
- **Qualify packaging automation**
- **Implement R&D access model**

Future solicitation

DARPA has a long history of microelectronics manufacturing technology

THE MOSIS SERVICE

Source: themosisservice.com

- Initiated in 1981 at University of Southern California’s Information Sciences Institute with DARPA funding
- Facilitate fabrication services through multi-project wafers (MPWs) to U.S. Government, their contractors, and Academic Community

SEMATECH

Source: smtnet.com

- Initiated in 1987 with 14 U.S. semiconductor companies and DARPA matching funding
- Ten years of public-private partnership to maintain U.S. competitiveness in semiconductors

MNX

MEMS Foundry

www.mems-exchange.org

Source: memsnet.org

- Initiated in 1999 at the Corporation for National Research Initiatives (CNRI) with support from DARPA Microsystems Technology Office
- Provide MEMS fabrication resources to the academic, industrial, and government communities

MEMS: Micro-electromechanical systems

CHIPS and Science Act

Forbes

BREAKING • BUSINESS

CHIPS Act Passes: House Approves $280 Billion Bill To Boost Microchip Production And Counter China

Brian Bushard Forbes Staff

I cover breaking news for Forbes

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Jul 28, 2022, 03:26pm EDT

Source: Forbes

Source: CNET

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NEWS | SEMICONDUCTORS

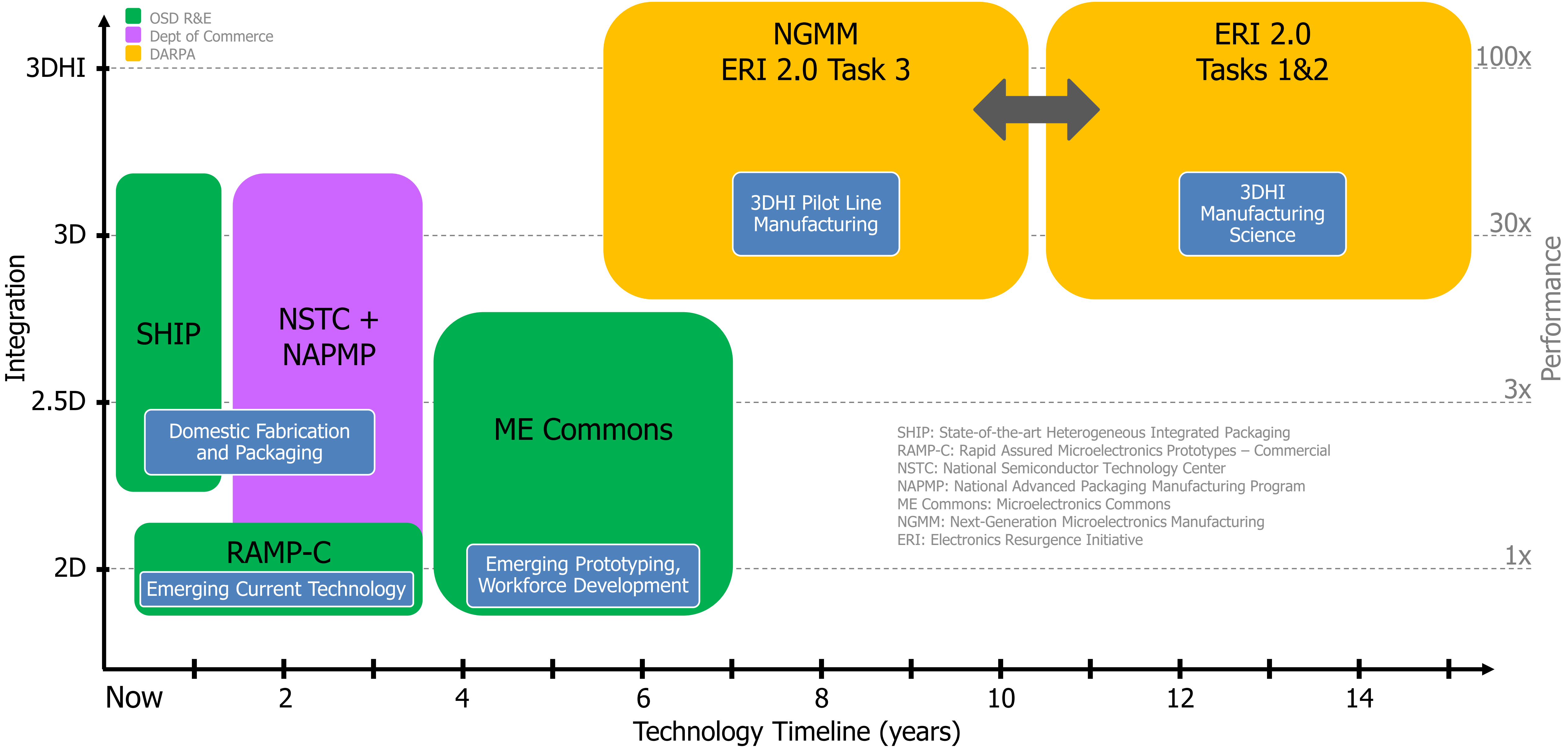
U.S. Passes Landmark Act to Fund Semiconductor Manufacturing › CHIPS and Science Act of 2022 provides billions for new fabs and other incentives

BY SAMUEL K. MOORE | 29 JUL 2022 | 3 MIN READ

Chip manufacturers are hoping their expansions will be less costly now. GETTY IMAGES

Source: IEEE

A long term vision for advanced microelectronics manufacturing

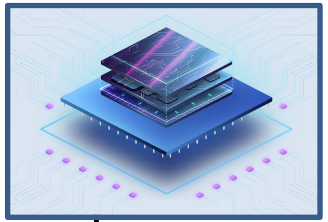


SHIP: State-of-the-art Heterogeneous Integrated Packaging
RAMP-C: Rapid Assured Microelectronics Prototypes – Commercial
NSTC: National Semiconductor Technology Center
NAPMP: National Advanced Packaging Manufacturing Program
ME Commons: Microelectronics Commons
NGMM: Next-Generation Microelectronics Manufacturing
ERI: Electronics Resurgence Initiative

Electronics Resurgence Initiative (ERI) 2.0 timeline

NGMM Phase 0 BAA
August 2022

ERI Summit 2023
August 22-24 / Seattle, WA

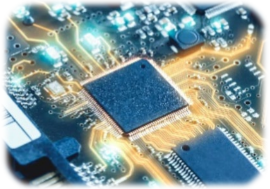


FY22 | FY23 | FY24 | FY25 | FY26 | FY27

Original ERI funding

ERI 2.0: Reinventing microsystems manufacturing for a new age

COMPUTE

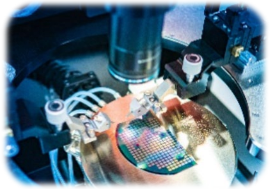


Increasing information processing efficiency at the edge

DECIDE

Accelerating innovation in AI hardware

BUILD



Manufacturing complex 3D microsystems

COMPOSE

Optimizing design and test for complex circuits

SECURE

Overcoming security threats across the entire hardware lifecycle

TALK

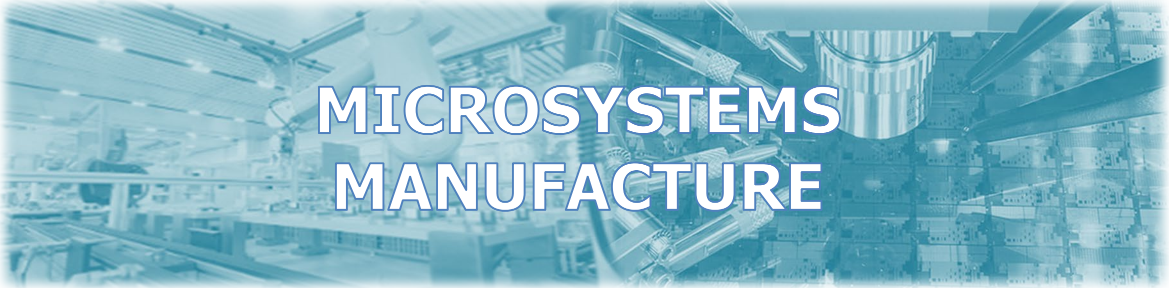
Securing communications

HARDEN

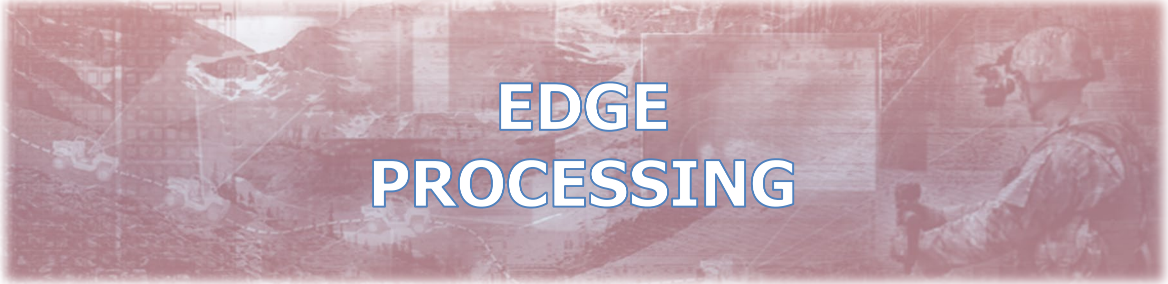
Developing electronics for extreme environments

NGMM: Next-Generation Microelectronics Manufacturing program

DISRUPTIVE
MICROSYSTEMS



MICROSYSTEMS
MANUFACTURE



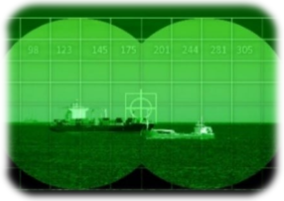
EDGE
PROCESSING

MTO thrust areas

Electronics Resurgence Initiative (ERI)

DISRUPTIVE MICROSYSTEMS

SEE



Gaining an advantage in sensing the physical world

TALK

Securing communications

ACT

Increasing the effectiveness of radiation on target

NAVIGATE

Embedding accurate positioning and timing

EDGE PROCESSING

COMPUTE

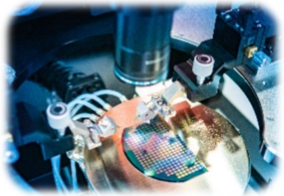
Increasing information processing efficiency at the edge

DECIDE

Accelerating innovation in AI hardware

MICROSYSTEMS MANUFACTURE

BUILD



Manufacturing complex 3D microsystems

COMPOSE

Optimizing design and test for complex circuits

SECURE

Overcoming security threats across the entire hardware lifecycle

HARDEN

Developing electronics for extreme environments

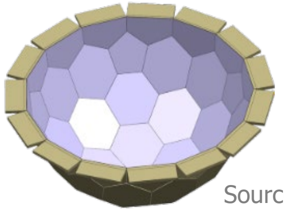
3D: Three-dimensional
AI: Artificial Intelligence

Problem: Flat focal plane arrays suffer from optical aberrations at array periphery, degrading illumination and resolution

Approach:

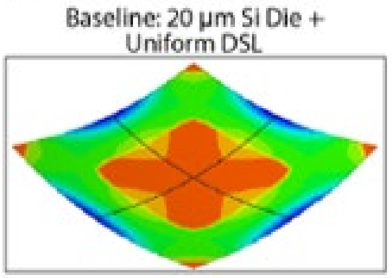
- Curve the focal array to reduce edge aberrations
- Develop structured readout integrated circuits that achieve hemispherical curvature to reduce size and weight of the imager

Mitigate stress of curving by structuring focal plane arrays with stress relief features

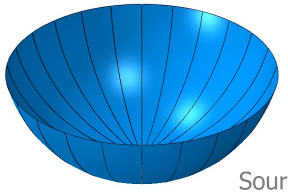


Source: Northrop Grumman

"The soccer ball"



Stress/strain engineering

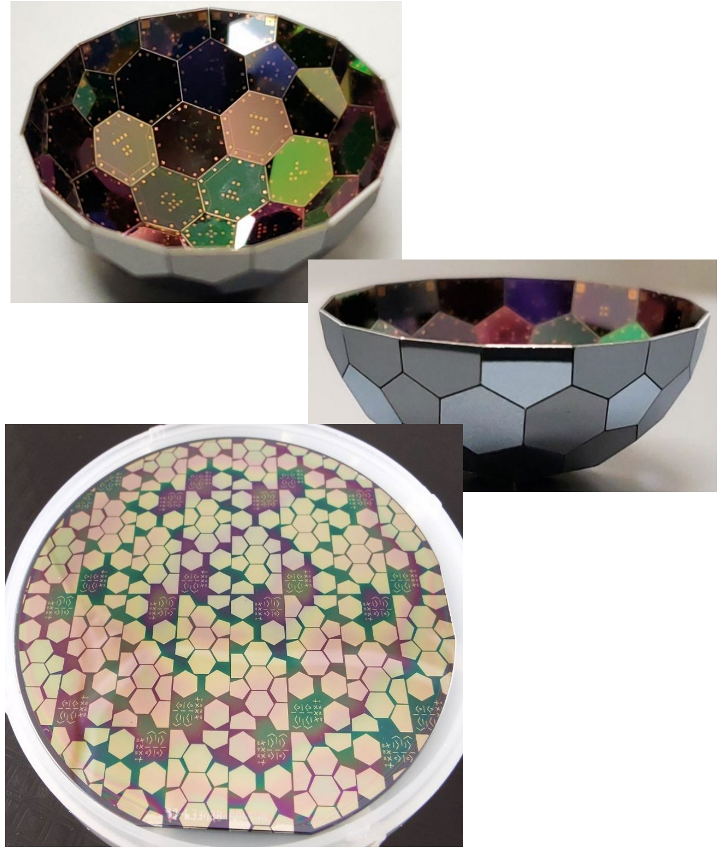


Source: HRL

"The daisy"

FOcal arrays for Curved Infrared Imagers (FOCII)

Successfully demonstrated curved focal plane array test structures

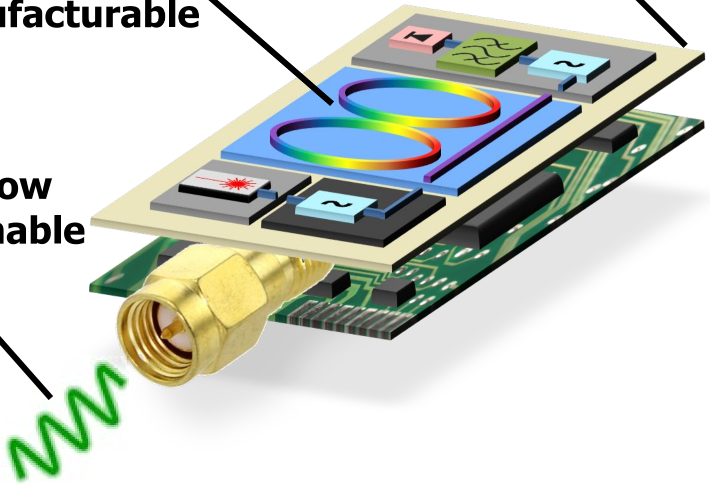


Source: Northrop Grumman

Problem: Precision microwave sources are too large, costly, and fragile to support C4ISR capabilities on SWaP-constrained platforms

Approach:

- Optical frequency division using stable chip-scale lasers and optical frequency combs to create a compact, tunable, low-noise microwave synthesizer

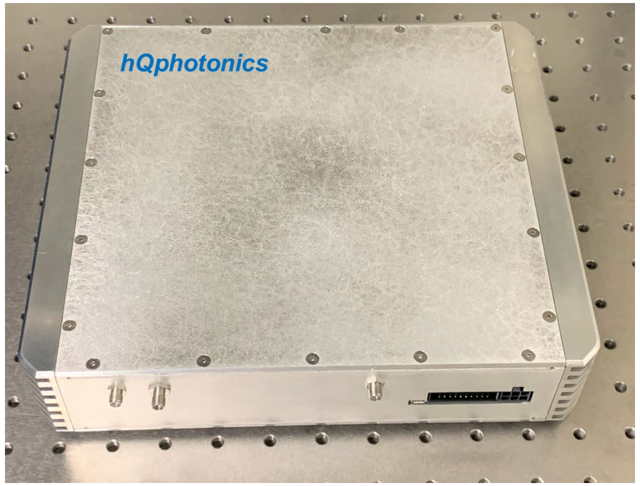


Environmentally robust

Compact and manufacturable

Extremely low noise and tunable

Created portable microwave oscillator product with the lowest phase noise to date



40 GHz oscillator achieves noise of only -156 dBc/Hz in 3 liter module

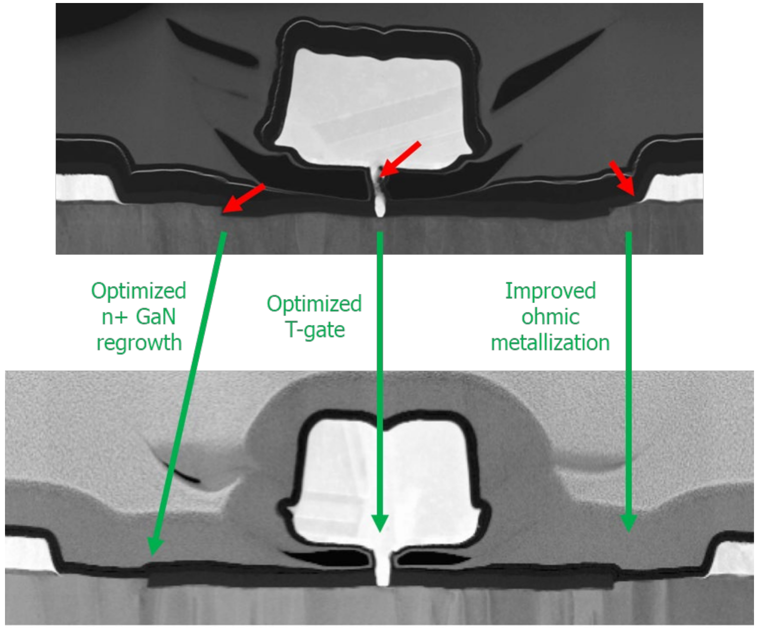
C4ISR: Command, Control, Communications, Computers (C4) Intelligence, Surveillance and Reconnaissance
dBc/Hz: Decibels from Carrier per Hertz; GHz :Gigahertz; SWaP: Size, Weight, and Power;

Generating RF with Photonic Oscillators for Low Noise (GRYPHON)

Problem: Current planar microwave power transistors lack speed, linearity, and power density at millimeter wave (mmW) frequencies

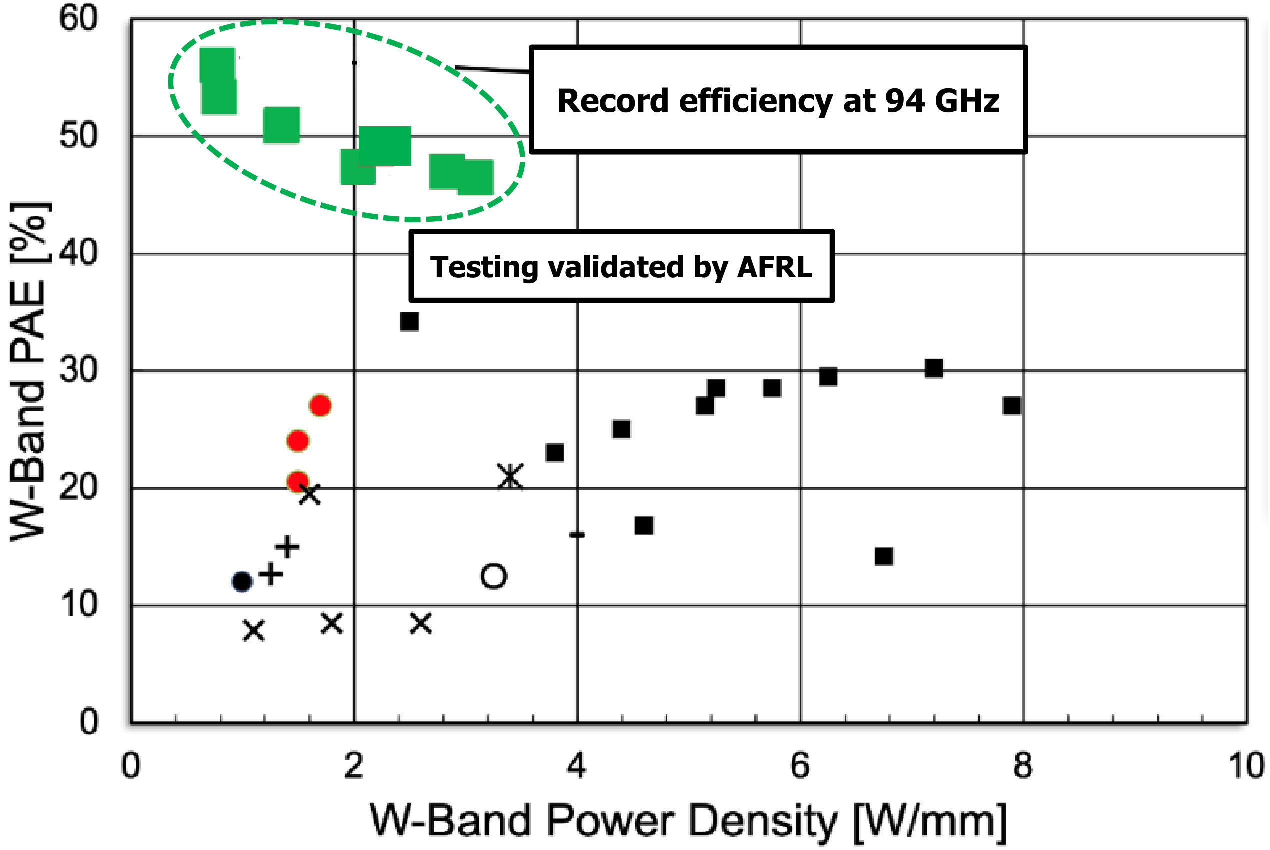
Approach:

- Explore new materials processing and devices to deliver 5x power density and 100x linearity at > 30 GHz



Source: Siddiqi et al., HRL Laboratories, CSMANTECH 2022

World record power added efficiency (PAE) for GaN transistor at W-band (94 GHz)



Record efficiency at 94 GHz

Testing validated by AFRL

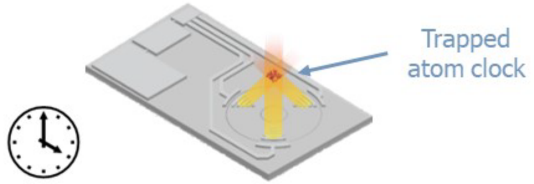
Millimeter Wave GaN Maturation (MGM)
Dynamic Range-enhanced Electronics and Materials (DREaM)

Problem: Timing alternatives to GPS are too complex and large for strategic uses and applications

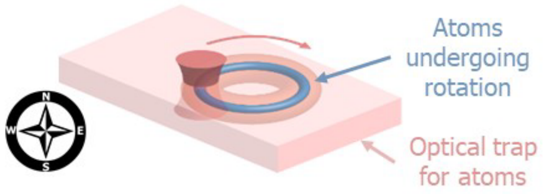
Approach:

- Develop photonic integrated circuit (PIC) architectures to realize highly-sensitive atomic clocks and gyroscopes

Integrating onto PIC will simplify complex optical geometry required for atomic clocks

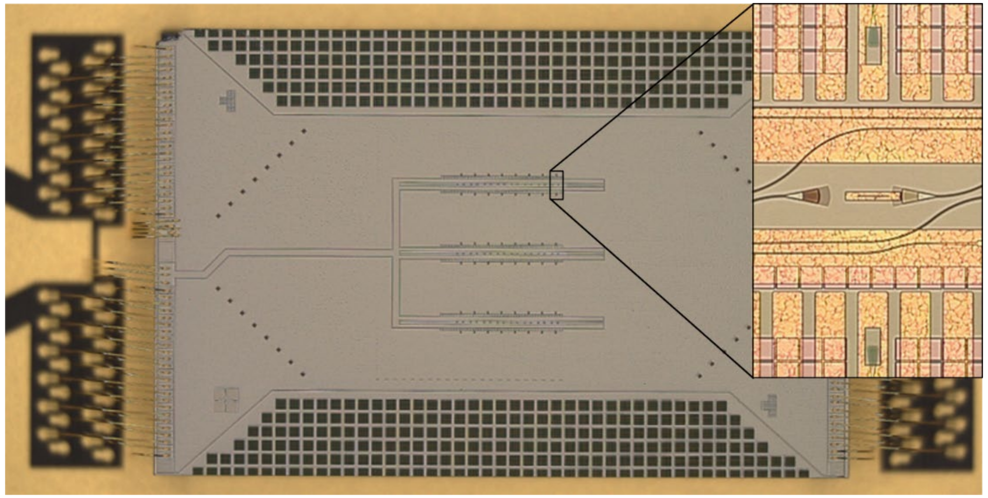


Using atomic traps will decouple acceleration from rotation



Source: DARPA

Developed microfabricated ion traps with directly integrated photonics used to deliver, control, and detect light for each atom



Source: Sandia National Laboratory

First-ever PIC that supports multiple ion traps

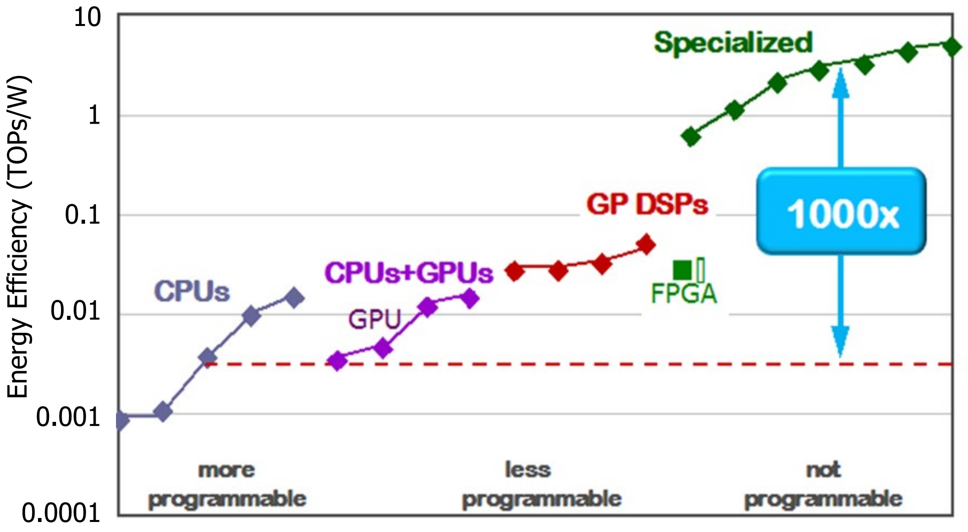
Atomic-Photonic Integration (A-PhI)

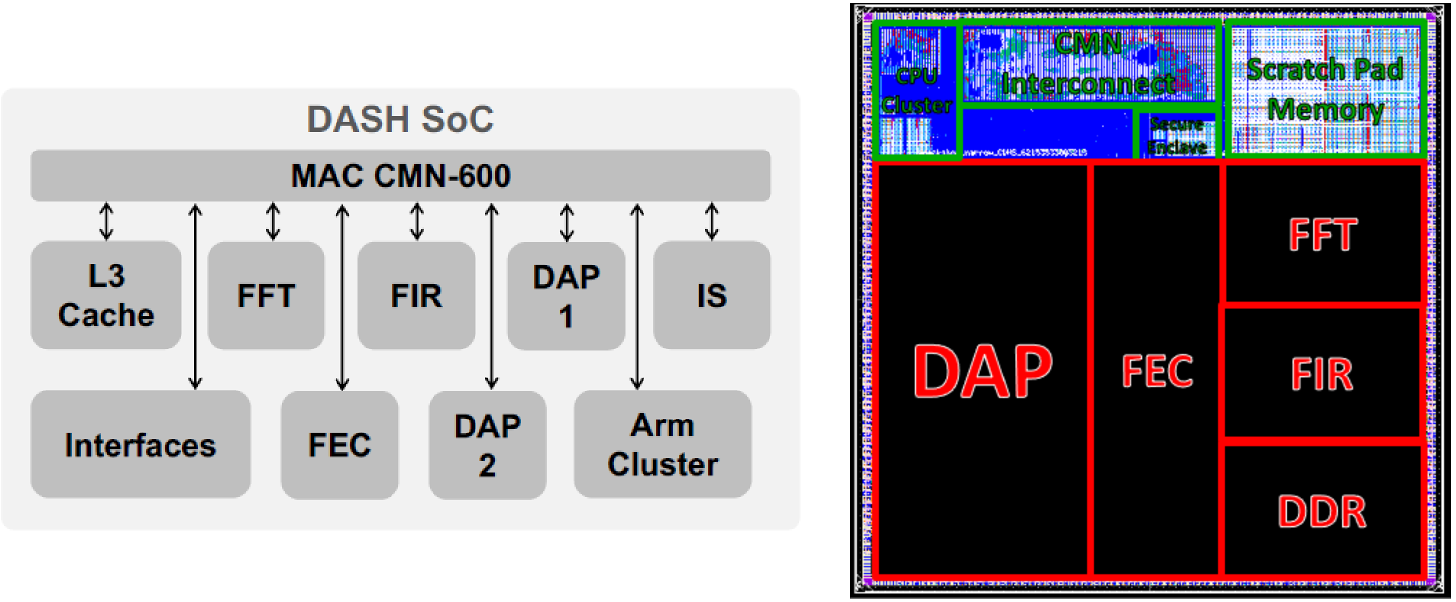
Problem: Achieving breakthrough performance in computation without excessive burden in time and cost associated with specialization

Approach:

- Automate analysis of code for kernels
- Identify Processing Elements (PEs)
- Automate scheduling of code on PEs

Developed programmable accelerator chip with 20x better processing efficiency (21 TOPs/W)





Arizona State's DASH-1 chip design and layout

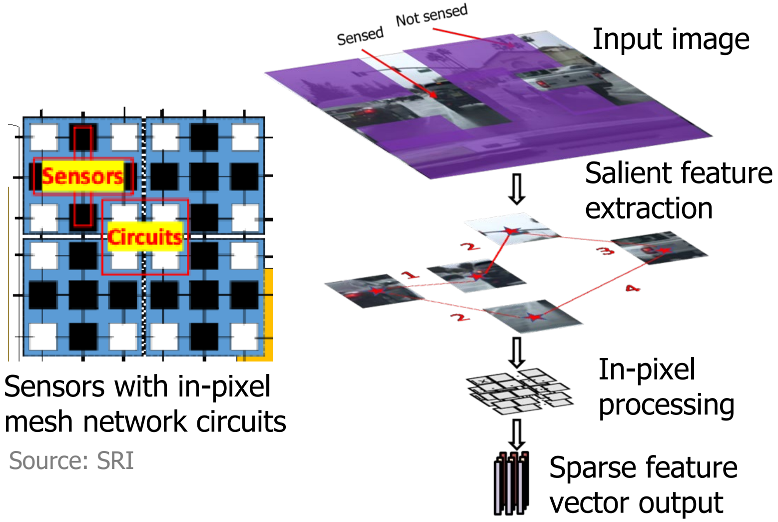
Domain-Specific System-on-Chip (DSSoC)

Problem: Latency constrained platforms at the edge cannot maintain image inferencing accuracy and functionality for deep neural networks (DNNs)

Approach: Bring intelligent processing to the pixel level

- Capture saliency and immediate data sparsity
- Reduce the complexity and latency of the back-end DNN

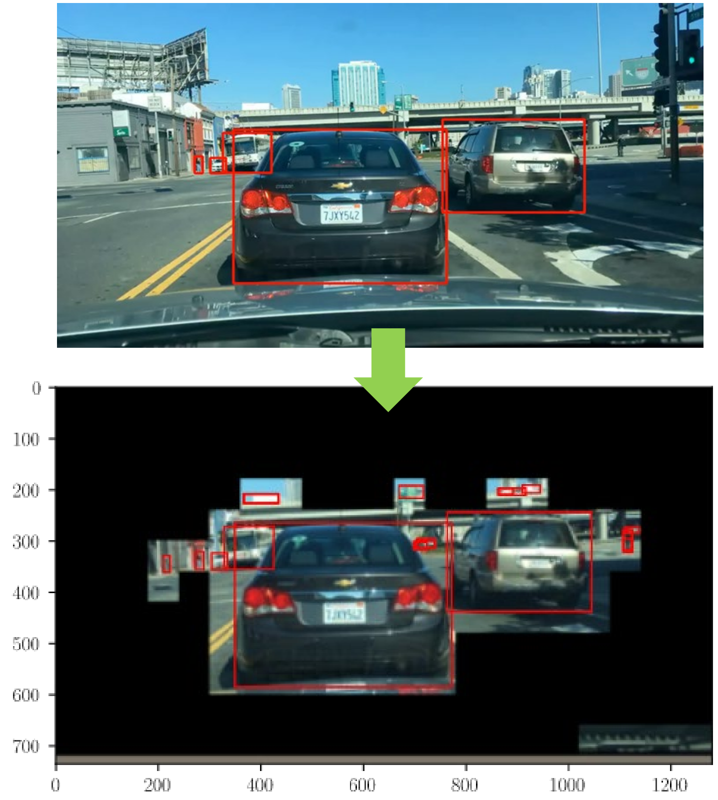
Maintained state-of-the-art accuracy with 10x reduced data bandwidth and dimensionality



Sensors with in-pixel mesh network circuits

Source: SRI

In-pixel saliency neural network circuit for dimensionality reduction



Source: Georgia Tech

Salient image feature patch extraction with dimensionality reduction

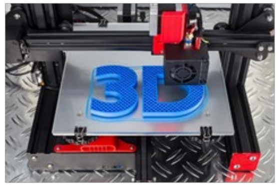
In-Pixel Intelligent Processing (IP2)

Problem: Domestic 3DHI R&D lacks an open-access, holistic approach and has long cycle-times for prototype manufacturing

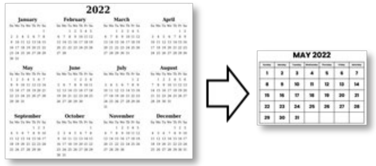
Approach:

- Establish a domestic capability to produce 3DHI prototypes
- Develop baseline processes in 3DHI facility for service offering
- Reduce manufacturing cycle-time through standardization and automation

Cost-effective

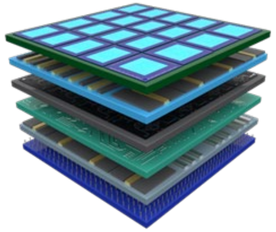


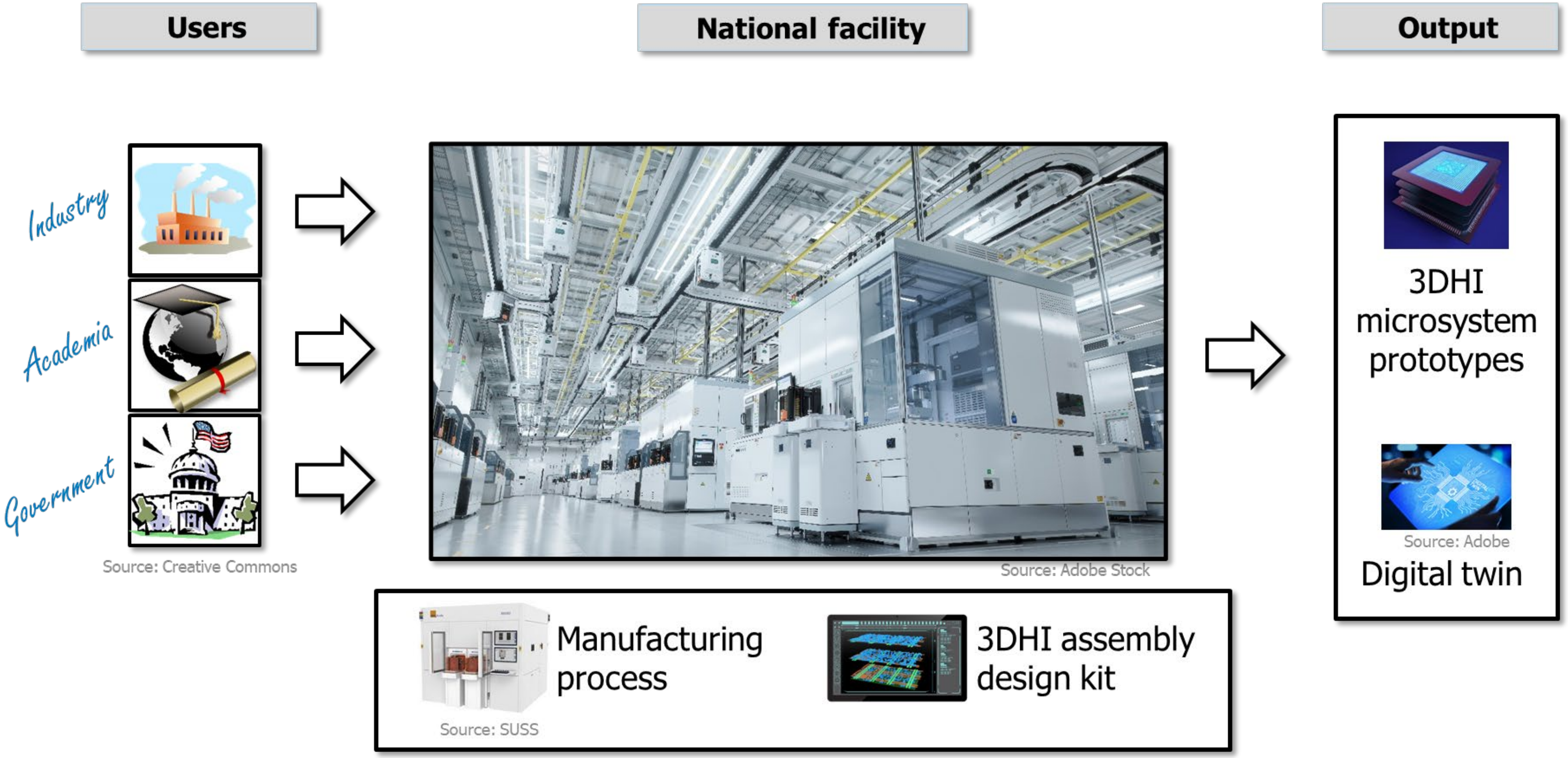
Fast prototyping



Secure access

High performance





Users

Industry
Academia
Government

Source: Creative Commons

National facility

Source: Adobe Stock

Manufacturing process

Source: SUSS

3DHI assembly design kit

Output

3DHI microsystem prototypes

Source: Adobe

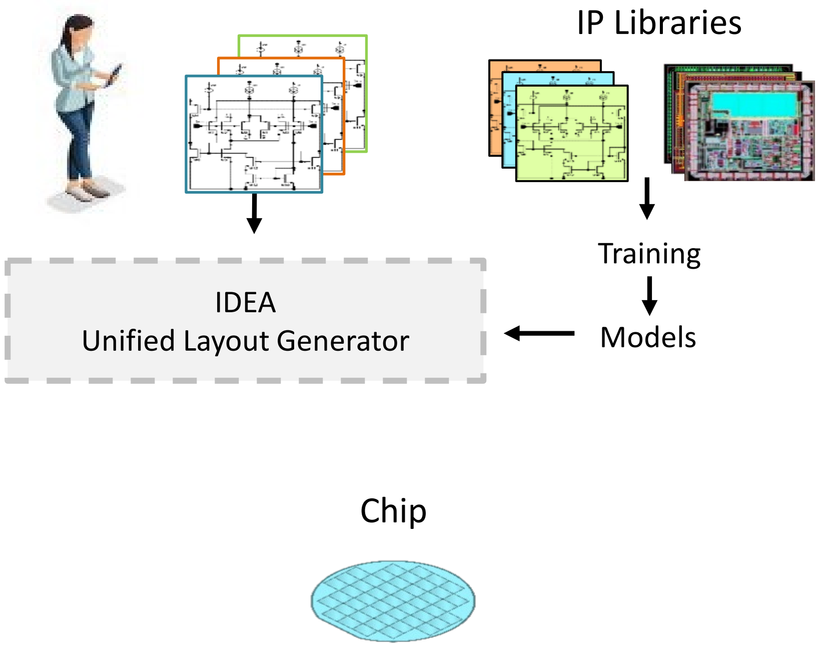
Digital twin

Next-Generation Microelectronics Manufacturing (NGMM)

Problem: System-on-Chip (SoC) development requires 12-36 months of manual, human-intensive design

Approach:

- Leverage machine learning advances to create a general purpose “silicon compiler” for systems-on-chip



IP Libraries

Training

Models

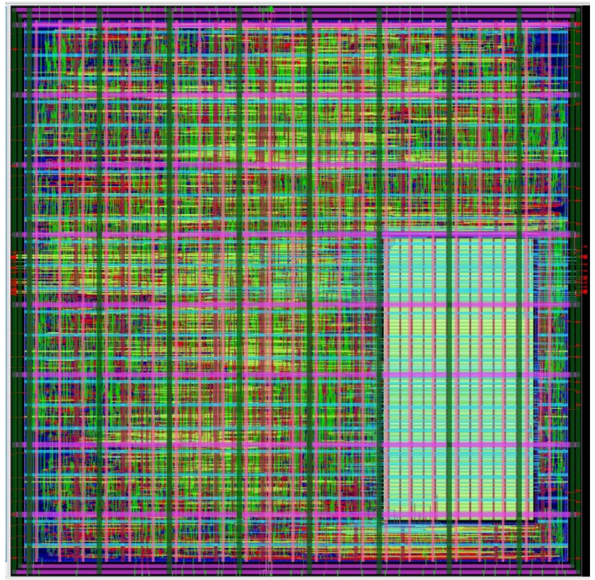
IDEA
Unified Layout Generator

Chip

No-Human-In-the-Loop

Intelligent Design of Electronic Assets (IDEA)

UCSD’s automatic layout tool used to tape-out an AI computing platform in hours with minimal designer effort

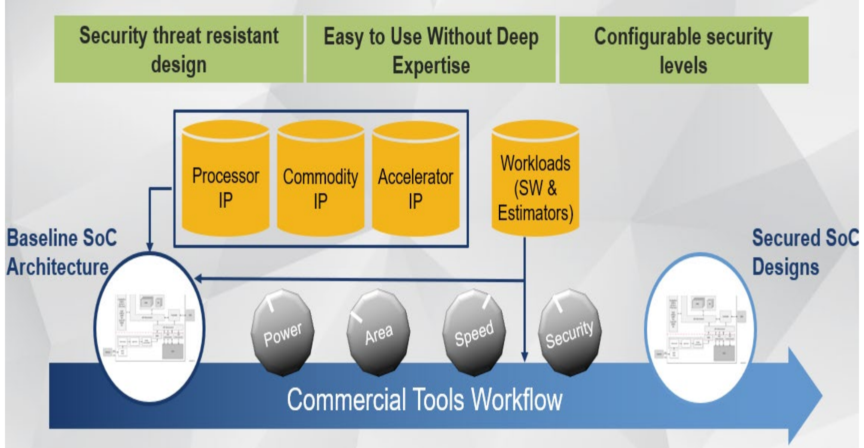


Army Research Laboratory AI chip
in Global Foundries’ 12nm process

Problem: Integrating security into all DoD system-on-chips (SoC) is prohibitive

Approach:

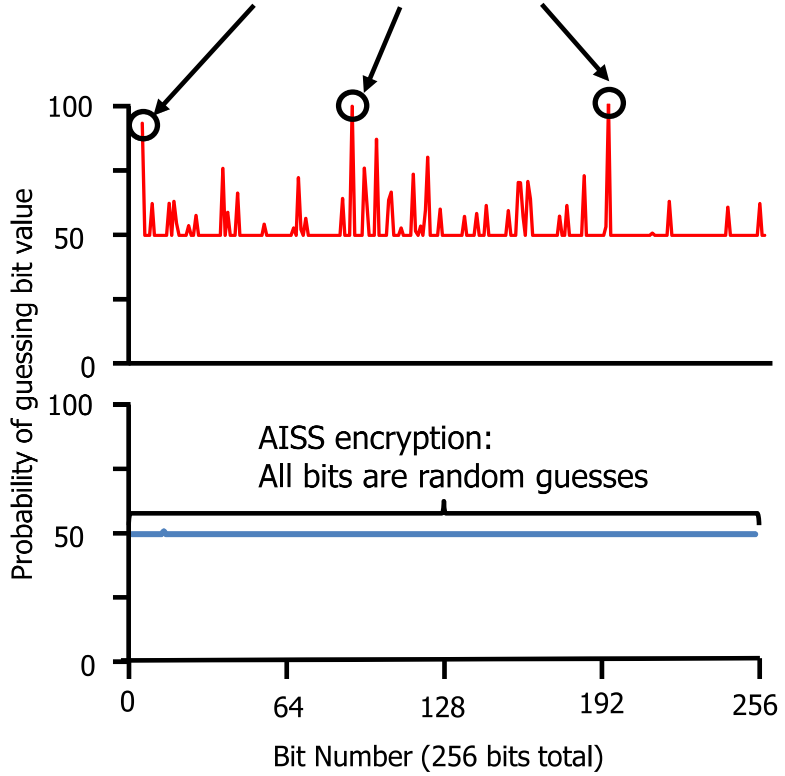
- EDA tools and algorithms to automatically add security to SoCs



- Users can tune power, area, speed, and security for each design
- Security suitable for small, medium and large SoCs

World’s first side-channel free encryption design in simulation

Traditional encryption:
High likelihood of guessing bit values



Source: Northrop Grumman

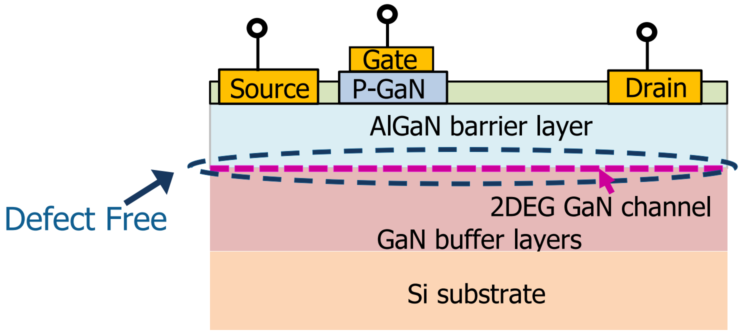
Automatic Implementation of Secure Silicon (AISS)

Problem: Space point-of-load (POL) converters have low efficiency, severely limiting the satellite available power, capabilities, and battery lifetime

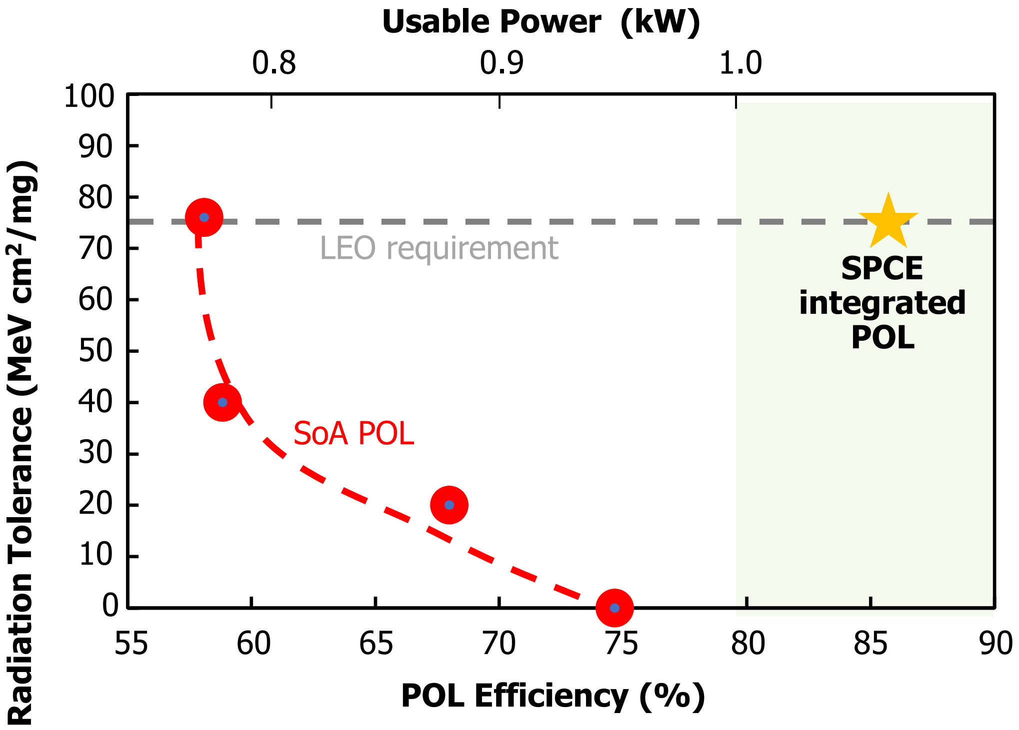
Approach:

- Exploit wide-bandgap semiconductor advance material synthesis
- Design novel device architectures
- Employ 3D heterogeneous integration technology

Radiation tolerant power electronics with breakthrough conversion efficiency for space systems



Reduced defects in high electric-field region improved radiation-tolerance and switching performance



Space Power Conversion Electronics (SPCE)

LEO: Low earth orbit
SoA: State of the art

MTO staff


Mark Rosker
MTO Director


Dev Palmer
MTO Deputy Director


Carl McCants
ERI Chief of Staff


Wendy Smith
MTO ADPM


Shannon Hurt
MTO PA

Adjunct PMs with MTO Programs

Whitney Mason, STO
Ted Senator, DSO
Matt Wilding, I2O
Howie Shrobe, I2O


David Abe
HPM/Vacuum Electronics


Todd Bauer
MEMS/Rad-Hard


John Davies
EW/Adv. Processing


Thomas Ehrenreich
Directed Energy


Ben Griffin
MEMS/High T materials


Jonathan Hoffman
Quantum/PNT


Bryan Jacobs
Algorithms


Yogendra Joshi
Thermal Management


Tom Kazior
Devices/Integration


Gordon Keeler
Photonics


Sung Kyu Lim
Electronic Design


Daniel Ridge
Hardware Security


Mike Sangillo
Additive Manufacturing


Anna Tauke-Pedretti
HW Security/Photonics


Trish Veeder
EO/IR


James Wilson
Integration


Jason Woo
CMOS/Processing

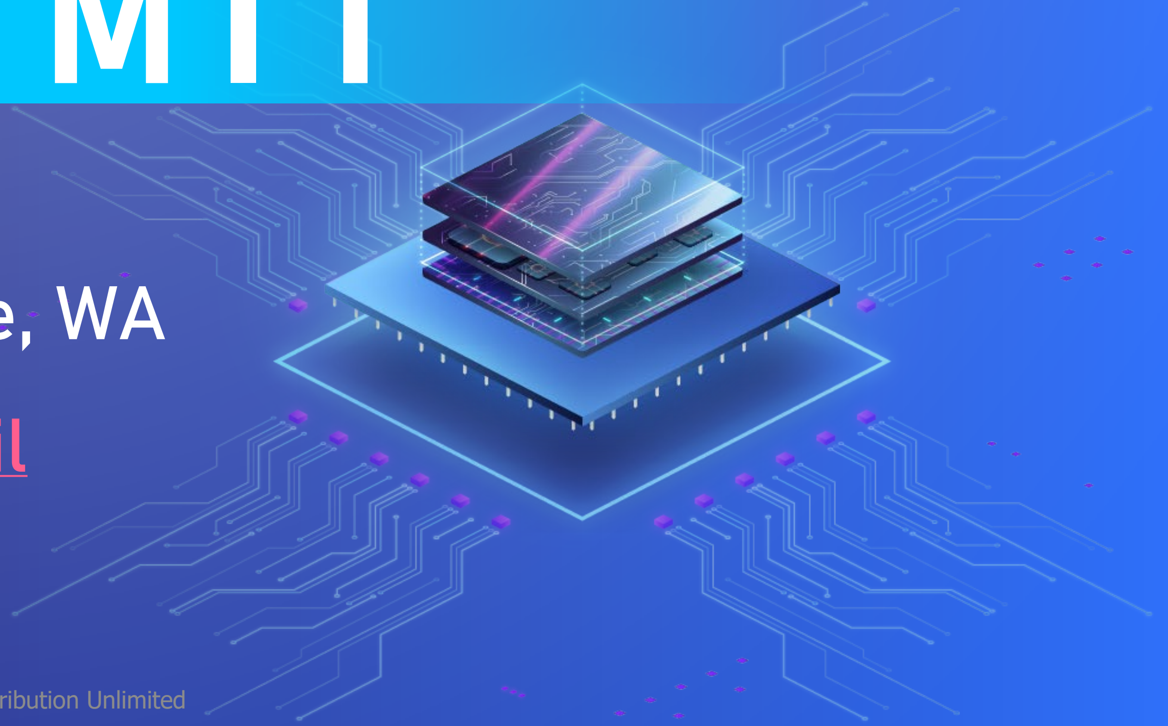

Lok Yan
Hardware Emulation

Join us in person as we focus on reinventing microelectronics manufacturing

ERI 2.0

ELECTRONICS
RESURGENCE
INITIATIVE

SUMMIT



August 22-24, 2023 | Seattle, WA

https://eri-summit.darpa.mil

Registration opens in May

DARPA

www.darpa.mil

Image credits for Heterogeneous Integration (HI) slide

Slide 14: (by row, L to R)

- Silicon, Materials: https://www.researchgate.net/figure/Unit-cell-of-the-silicon-cubic-crystal-with-edge-lengths-equal-to-the-lattice-parameter_fig13_309530722 [accessed Aug 10, 2022]
- Silicon, Devices: IBM, https://semiengineering.com/7nm-last-major-node/ [accessed Aug 10, 2022]
- Silicon, Process: Mirkaimi, Laura, Abul Nuruzzaman, "A new era of computing performance with hybrid bonding," Chip Scale Review, July 2021, pp. 14.
- Silicon, Function: Adobe, https://stock.adobe.com/images/technology-background-cpu-circuit-on-large-wafer-advanced-technology-concept-visualization-ai-processor-digital-data-transmission-process-3d-rendering/415894076 [accessed Aug 10, 2022]
- SiGe, Materials: https://www.iue.tuwien.ac.at/phd/wittmann/node9.html [accessed Aug 10, 2022]
- SiGe, Devices: Georgia Tech, https://cressler.ece.gatech.edu/research/SiGe.html [accessed Aug 10, 2022]
- SiGe, Process: Intel, Intel Accelerated Press Kit, July 26, 2021. https://www.intel.com/content/www/us/en/newsroom/resources/press-kit-accelerated-event-2021.html#gs.8u2la7
- SiGe, Function: IBM, https://www.ibm.com/ibm/history/ibm100/us/en/icons/siliconchip/ [accessed Aug 10, 2022]

Slide 14 (by row, L to R - duplicates, in blue, from above, not repeated)

- III-V, Materials: Wikipedia, public domain image, https://en.wikipedia.org/wiki/Indium_phosphide#/media/File:Boron-phosphide-unit-cell-1963-CM-3D-balls.png [accessed Aug 10, 2022]
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