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Combinational Logic in Soft, Conductive Mechanical Integrated Circuit Materials (POSTPRINT)

Christopher E. Tabor

AFRL/RXES

Charles El Helou, Benjamin Grossmann**,** Philip R. Buskohl, and Ryan L. Harne

Department of Mechanical Engineering, The Pennsylvania State University, University Park, PA

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Christopher E. Tabor – AFRL/RXES

Charles El Helou - Benjamin Grossmann - Philip R. Buskohl - Ryan L. Harne - Department of Mechanical Engineering, The Pennsylvania State University, University Park, PA

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14. ABSTRACT

Information processing is a key function of autonomous engineered materials, since the comparison and assessment of input signals is crucial to determine intelligent material responses. Recent research has developed emerging methods of mechanical computing to realize fundamental logic gates in soft matter. Here, we uncover a relation between Boolean mathematics and mechanically reconfigurable electrical circuits to realize the functioning of all combinational logic operations in soft, conductive mechanical materials.

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Combinational Logic in Soft, Conductive Mechanical Integrated Circuit Materials

Charles El Helou, Benjamin Grossmann, Christopher E. Tabor, Philip R. Buskohl, and Ryan L. Harne*

Department of Mechanical Engineering, The Pennsylvania State University, University Park, PA USA

** Corresponding author: ryanharne@psu.edu*

Abstract

Information processing is a key function of autonomous engineered materials, since the comparison and assessment of input signals is crucial to determine intelligent material responses. Recent research has developed emerging methods of mechanical computing to realize fundamental logic gates in soft matter. Here, we uncover a relation between Boolean mathematics and mechanically reconfigurable electrical circuits to realize the functioning of all combinational logic operations in soft, conductive mechanical materials. We establish an analytical framework that first minimizes the canonical functions of combinational logic by the Quine-McCluskey method, and secondly governs the mechanical design of reconfigurable integrated circuit switching networks in soft matter. The resulting materials may compute higher level arithmetic operations such as addition, subtraction, and multiplication, which are essential to process mechanical stress information applied to the material platform. We exemplify two methods to automate the design and fabrication of the materials, and show one way to arbitrarily increase the computational density of the materials by a layer-by-layer design approach. Because the framework established here leverages mathematics and kinematics for system design, the proposed approach of mechanical integrated circuit computing can be realized on any length scale and in a wide variety of physics.

Main Text

Recent developments in autonomous engineered matter introduce the ability for intelligent materials to process environmental stimuli and functionally adapt [1] [2] [3]. This emerging class of engineered living systems offers the future prospects for materials that independently monitor and restore aging civil infrastructure [4] [5], that capture and neutralize the threat of airborne pathogens [6], and that search and digest pollutants in water supplies [7], among other visions. To formulate a foundation for such new material paradigm, researchers have introduced sensing functionalities in soft matter to detect a variety of physical fields. These include photo- [8] and thermo- [9] responsive hydrogels and liquid crystal elastomers, strain-sensitive conductive silver thermoplastic polyurethane composites [10] [11], and thermo-mechanochromic monitoring of strain and thermal loads [12]. Electromechanical sensing is also integrated by means of unique substrate designs such as continuously deforming conductive mechanical metamaterials [13] [14] or digitized connections of liquid metal microchannels embedded in elastomeric metamaterials [15]. Actuation, another fundamental function of autonomy, is coupled with electrical signals through electro-active polymer gels [16] and ionic polymer–metal composites [17] to leverage soft material shape reconfiguration. Pneumatic [18], optical [19], and electrothermal [20] responses have also been exploited to govern the dynamic shape change of soft matter.

Information processing of sensory signals for sake of governing activated responses is the key functional element in the vision of engineering living systems that has been the focus of recent research. Unconventional techniques have been explored such as mechanical computing that abstract digital bits according to mechanism and material configurations [21] [22]. Logic operations are cultivated through unique architectures of elements with elastic instabilities found in origami [23] [24] [25], mechanical devices [26] [27], and metamaterials [28]. Soft matter realizations are also illustrated through stable propagation of digital signals in bifurcated chains that are mechanically [29] and pneumatically [30] controlled. Even though such embodiments develop innovative concepts for processing input signals, the approaches lack scalability to compute all of the advanced operations of traditional digital logic necessary in autonomous material responses.

Integrated circuits (ICs) are the conventional platform for computing digital electrical signals, which are prolific in modern electronics. Efforts are growing to embed mechanically strain gated switching elements in ICs for the development of logic operations in soft matter [31] [32]. By combining mechanical computing bit abstraction from discrete mechanical configurations with reconfigurable electrical networks, El Helou et al. [33] realized all of the universal logic gates in soft and conductive mechanical metamaterials. Yet individual logic gates cannot compute advanced operations such as arithmetic, which are essential to the intelligent behavior of soft matter. A method to develop combinational logic ICs in soft materials, that incorporate a multitude of logic gates, has yet to be established. The computing network is currently limited by the type and quantity of inputs that an output signal can drive in electromechanical IC assemblies [32] [33], and by the damping of the signal propagation in mechanical mechanisms [26] [29]. A design approach is required whereby scalable, higher-level computing operations are cultivated in soft, autonomous matter.

Inspired by the mathematical principles of switching theory for ICs [34], we introduce a robust strategy that is grounded in Boolean mathematics to guide the design of all combinational logic operations in soft, conductive mechanical materials. The approach builds upon the logic gate components fashioned in El Helou et al. [33]. In this work, we create a new IC-synthesis procedure whereby any arbitrary *combination* of logic gates used in a combinational logic process can be realized. This facilitates advanced information processing such as *n*-bit addition, subtraction, and multiplication. These materials are programmed through a design process that supports automation in both material design and fabrication. The computing networks realized by this approach are minimized via the set of canonical Boolean functions required to realize the combinational operation. Here, we demonstrate reconfigurable integrated circuit materials that sense and process mechanical stress to compute higher-level 2-bit arithmetic operations that could be used for intelligent response and actuation. Furthermore, we propose a layer-by-layer fabrication approach that permits arbitrarily large computational density in this concept of soft, conductive mechanical integrated circuit materials.

The integrated circuit synthesis strategy builds from the fundamental mechanical computing unit cell material cross-section shown in Figure 1(a). The unit cell is comprised of a beam column with one center square tile with two half-square tiles on the boundaries. In this research, we retain a geometric ratio ρ of 1.6 for the unit cell, which describes the ratio of the half column length b to the square tile side length a. When uniaxially compressed, a bifurcated kinematic collapse stage is reached with two possible compact configuration states that are controlled through left or right shear perturbations. Mechanical computing bit abstraction is exploited to represent the 1-bit mechanical shear input as '1' for the counterclockwise (left shear) rotational state and '0' for the clockwise (right shear) rotational state, respectively, Figure 1(a). A row of adjacent unit cells that are connected in parallel deform homogenously with the same digital input due to the mechanical disconnections between center square tiles. To develop an *n*-bit material system with 2^n unique configuration states, n unit cell rows must be serially connected. In other words, the rows are stacked vertically with respect to vertically directed loads or constraints. For instance, a 2-bit material is shown in Figure 1(a) with two mechanical input rows, A_1 and A_2.

Figure 1. Bit abstraction via switching elements and gates. (a) 1-bit unit cell geometry with the 1 (counterclockwise) and 0 (clockwise) mechanical configurations to reach the corresponding self-contact states. The 2-bit material is also shown with two mechanical input rows connected in series, A_1 and A_2. Schematic of the (b) Buffer and (c) NOT elementary switches on a 1-bit unit cell with respective conductive networks. Digital mechanical inputs are highlighted in green. Digital electrical

output terminals are highlighted in red and are powered by the cyan colored V_{cc} terminal. (d) Schematics and experimental images of the AND and OR logic gates designed on a 2-bit material structure with their respective switching circuitry. The (e) AND and (f) OR shown in the four possible mechanical configurations with the appropriate digital outputs for each.

Our embodiment of digital logic [33] fundamentally depends on the discrete mechanical behavior of a unit cell coupled with unique electrical network to develop two kinematic 1-bit switching elements. Shown in Figure 1(b), a Buffer switch conductive network contains an electrical power terminal V_{cc} shown in blue, and an output terminal Q_B shown in red. The corresponding network connects at the compact state to output an electrical digital signal Q_B of 1 when a mechanical input of 1 is applied, and an output Q_B of 0 for an input of 0. The second switch in Figure 1(c) is a NOT switch. The NOT is an inverted Buffer switch, so that the NOT outputs a Q_N of 0 when Q_N is 1, and vice versa.

With this 2-bit material and bit abstraction concept as shown in Figure 1(a), El Helou et al. [33] realized all the fundamental 2-bit logic gates, namely AND, NAND, OR, NOR, XOR, and XNOR. The gates are systematically programmed by placing the appropriate switches (Buffer or NOT) on the mechanical bit rows (A_1 or A_2) and electrically connecting the switches in series or parallel according to the appropriate switch network. Figure 1(d) demonstrates the AND gate that contains a Buffer switch on each of the A_1 and A_2 input rows that are electrically connected in series. Using a similar approach of switch assembly, the OR gate contains Buffer switches that are connected in parallel. Through the negation laws stated in De Morgan's theorem, the remainder of the 2-bit gates are designed, Supplementary Figure 5. The AND and OR are experimentally fabricated (see Supplementary Information) on a soft urethane rubber substrate with conductive surface channels containing silver thermoplastic polyurethane (Ag-TPU) composites. Figure 1(e)(f) validate the 4 possible configurations for the AND and OR gates, respectively. The electrical networks reconfigure to result in the digital outputs that correspond to the appropriate logic operation.

Through serial and parallel connections of the Buffer and NOT switching elements, it has been shown that all the 2-bit logic gates may be constructed [33]. Yet, higher-level combinational logic operations that contain multiple logic gate connections, such as the full adder in Figure 2(a), are the next significant step forward to yield a mechanical computing framework with scalable computing complexity.

Figure 2 illustrates the process created in this research of designing the mechanical materials and conductive networks to program any combinational logic sequence. The approach leverages the foundations of canonical Boolean functions and their algebraic combinations. A means to automate this design process is given in the Supplementary Information.

To exemplify the design strategy established here that constructs arbitrary combinational logic sequences, we use the full adder as a model logic combination. The full adder in Figure 2(a) includes three digital inputs A, B, and C_{in}. This logic operation adds the 1-bit numbers A and B, and allows for the C_{in} input as a carry bit that is conventionally passed along in a parallel binary adder circuitry. The full adder yields two independent digital outputs Q_{Sum} and Q_{Cout}, which correspond to the first- and second-bit digit

in the total binary number $(Q_{Cout}\ Q_{Sum})_2$, respectively. Each output is presumed as a separate logic path in the design strategy created here. Thus, distinct truth table outputs are obtained for a specific combinational logic process, Figure 2(b). The truth tables are then utilized to extract the canonical Standard Sum of Product (SSoP) Boolean functions for each output.

An SSoP is devised of minterms corresponding to each bit output in the truth table. Each minterm contains the product (&) of all the input Boolean terms. If the input is '0' in that specific configuration, the inverted term (~) is included in the product, and vice versa. All the minterms are added together (|) to form the SSoP form of the Boolean function. The SSoP functions for the Q_{Sum} and Q_{Cout} are described by Equations 1 and 2, respectively.

$$Q_{Sum}(A,B,C_{in}) = \sim A \& \sim B \& C_{in} \mid \sim A \& B \& \sim C_{in} \mid A \& \sim B \& \sim C_{in} \mid A \& B \& C_{in} \quad (1)$$

$$Q_{Cout}(A,B,C_{in}) = A \& B \& C_{in} \mid A \& B \& \sim C_{in} \mid \sim A \& B \& C_{in} \mid A \& \sim B \& C_{in} \quad (2)$$

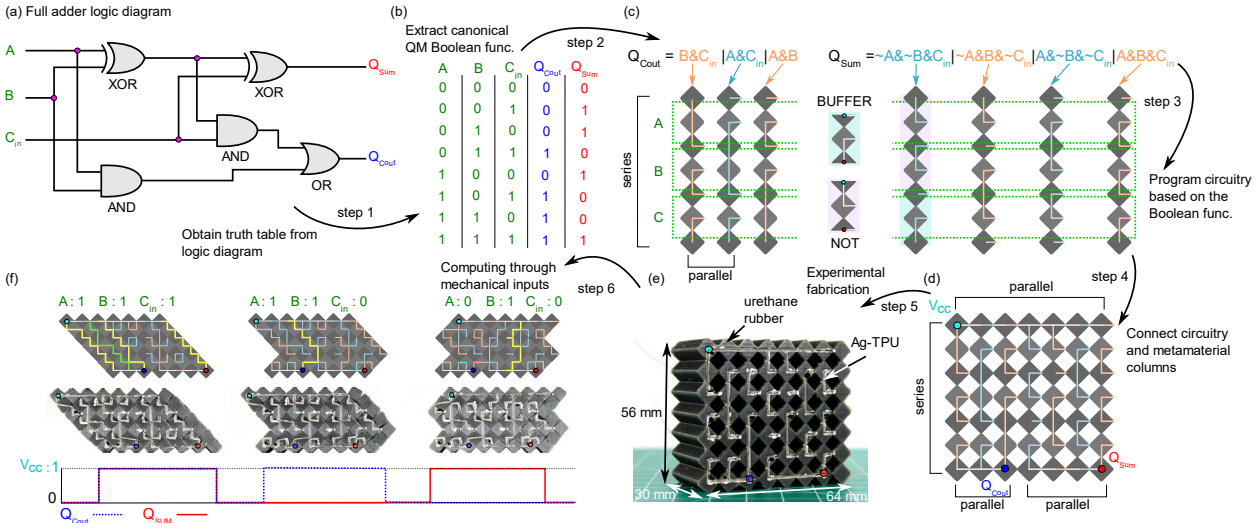

Figure 2. Combinational logic design synthesis. (a) The full adder logic diagram with the mechanical inputs (A, B, C_{in}) shown in green, and the electrical outputs (Q_{Sum}, Q_{Cout}) highlighted in red and blue, respectively. (b) The truth table corresponding to the full adder operation. (c) A schematic illustrating the relationship between the QMSoP Boolean function minterms, and the 3-bit material columns that contain either NOT or Buffer connected in series. (d) A schematic and (e) experimental image of the full adder material design that is constructed by connecting the material columns in parallel. (f) Experimental digital output results of three possible configurations with their respective experimental images and schematics of the reconfigured network. Connected paths that result in an output of 1 are highlighted in green or yellow. Electrical connections can only occur through switches in the same column.

As shown in Equation 1 and 2, both Q_{Sum} and Q_{Cout} in the SSoP contain four minterms with A, B, and C_{in}. Since each Boolean term corresponds to a switch in the circuit, minimizing the SSoP corresponds to a reduction in the quantity of switches and, as a result, the mechanical material size. Thus, the canonical function minimization Quine-McCluskey (QM) algorithm [35] is applied here to the SSoP and the modified Q_{Sum} and Q_{Cout} QMSoP functions are demonstrated in Equation 3 and 4, respectively.

$$Q_{Sum}(A,B,C_{in}) = \sim A \,\&\, \sim B \,\&\, C_{in} \mid \sim A \,\&\, B \,\&\, \sim C_{in} \mid A \,\&\, \sim B \,\&\, \sim C_{in} \mid A \,\&\, B \,\&\, C_{in} \quad (3)$$

$$Q_{Cout}(A,B,C_{in}) = B \,\&\, C_{in} \mid A \,\&\, C_{in} \mid A \,\&\, B \quad (4)$$

Using the Quine-McCluskey (QM) algorithm, the Q_{Sum} in Equation 1 is already in the optimized canonical form. On the other hand, the Q_{Cout} reduces significantly as shown in the Equation 4.

We then employ the symbolic representation of switching circuits presented by Shannon [34]. In this approach, we construct the conductive network by utilizing the QMSoP functions composed only using the two elementary switches, Buffer and NOT. As shown in Figure 2(c), each simplified minterm corresponds to a material column of three serially connected unit cells. An inverted term (~) corresponds to a NOT switch, and an ordinary term corresponds to a Buffer switch. For instance, the initial minterm in the Q_{Sum} function ($\sim A \,\&\, \sim B \,\&\, C_{in}$) contains two NOT switches on the A and B rows, and a Buffer switch on the C_{in} row that are serially connected. Such gate sequence is shown in the left column of Figure 2(c) for Q_{Cout} .

By this method, each simplified minterm is represented in a distinct material column, where the Buffer and NOT switches are used in exact agreement with the QMSoP functions for a given combinational logic process. Then the material columns are connected in parallel as shown in Figure 2(d) to form the integrated circuit material system. Both outputs are powered by the same V_{cc} (cyan) terminal, yet the output terminals are separated to the Q_{Sum} (red) and the Q_{Cout} (blue).

The mechanical integrated circuit material is then fabricated with the full adder logic operation programmed on the surface as shown in Figure 2(e). An additional column is included on the fabricated samples to improve electrical connections on the right boundary. This design is validated by the example addition arithmetic sequences shown in Figure 2(f). In each example, the appropriate digital output bits are obtained as those shown in the truth table, Figure 2(b). In practice, each layer undergoes a combination of shear and uniaxial compression to determine the digital input sequence (see Supplementary Information). The column networks that electrically conduct and output a value of '1' upon compaction are highlighted in yellow or green in Figure 2(f). Since the conductive Ag-TPU ink is practically confined by the substrate geometry, electrical connections are only allowed through the switches in the same column. All 8 addition computations possible for the full adder are exemplified in Supplementary Figure 1 via simulated and experimental results.

The design strategy introduced in this research enables the programing of any high-level combinational logic in the soft, mechanical integrated circuit materials. To illustrate such computing scalability, three fundamental 2-bit arithmetic operators are constructed with the QMSoP functions. These operators are the 2-bit adder, 2-bit subtractor, and 2-bit multiplier as shown in Figure 3. The operators are applied between the two 2-bit binary operands, A and B, that are mechanically applied on the 4-bit material in the row

order A_1, B_1, A_2, and B_2 from top to bottom. See the Supplementary Information for the logic diagrams and QMSoP functions for each arithmetic operator.

The 2-bit adder in Figure 3(a) contains 32 electrical switches and 44 material unit cells. This is accounted for via 11 material columns each including 4 unit cells stacked vertically in series. By comparison, a 2-bit adder designed with the SSoP functions requires 60 switches and 64 unit cells. The Boolean function minimization algorithm such as the QM allows for the same computing function with significantly reduced quantity of switches. For the specific material fabrications realized here, this corresponds to reduced substrate strain energy consumption per computing operation. Furthermore, a third method of designing combinational logic is created in this work termed the Substitution Method (SM) (see Supplementary Information). The 2-bit adder designed from the Substitution Method has 24 switches and 36 unit cells which is still less than the switches and unit cells via QMSoP. On the other hand, the Substitution Method does not derive the Boolean functions for sake of conductive network design. Consequently, the Substitution Method is dependent on a sequence of manipulations to the switching circuit and lends itself more so as a visual interface between the mechanical integrated circuit material design and the corresponding electrical logic gate counterpart. As a result, the Substitution Method is tedious to scale and automate compared to the QMSoP that exploits the canonical functions.

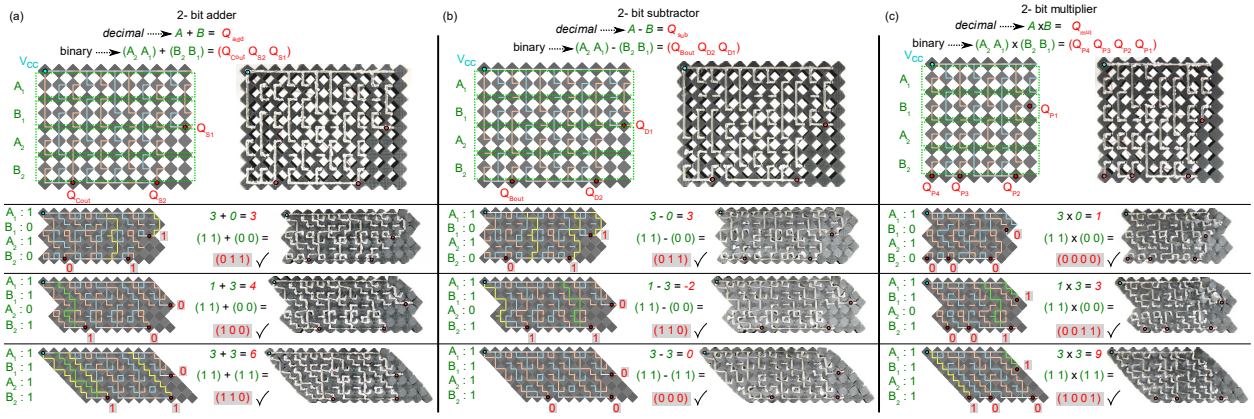

Figure 3. 2-bit arithmetic operators. A chart illustrating the schematic and experimental images of the 4-bit material and computing network design for a 2-bit (a) adder, (b) subtractor, and (c) multiplier. The operations are computed between two operands *A* $(A_2\ A_1)_2$ and *B* $(B_2\ B_1)_2$ that are mechanically entered (green) through the three representative material configurations. The binary digital outputs (red) for each configuration are compared to the decimal value for validation.

The QMSoP 2-bit subtractor shown in Figure 3(b) contains 32 switches and 44 unit cells, which is the same number as for the QMSoP 2-bit adder. This can be anticipated since the adder and subtractor logic diagrams differ only by NOT gates in the subtractor that replace particular Buffer gates in the adder. Previous findings by El Helou et. al [33] demonstrate that logic inversion does not result in the addition of switches, yet rather the replacement and reconnection of switches as likewise found here. Finally, the 2-bit multiplier shown in Figure 3(c) requires 24 switches and 32 unit cells. With increasing *n*-bits, the order of the computational complexity governs the IC network and material size.

These exemplary arithmetic operators are fabricated with urethane rubber substrates and Ag-TPU conductive networks as seen in Figure 3. The digital outputs are experimentally validated through representative arithmetic calculations seen in Figure 3. The 2-bit adder and subtractor result in three digital outputs corresponding to the binary numbers $(Q_{Cout}Q_{S2}Q_{S1})_2$ and $(Q_{Bout}Q_{D2}Q_{D1})_2$, respectively. It is important to note that the two's complement binary representation is utilized for the 2-bit subtractor output, and thus the Q_{Bout} binary digit corresponds to a decimal value of -4. The 2-bit multiplier results in four digital outputs that correspond to the binary number $(Q_{P4}Q_{P3}Q_{P2}Q_{P1})_2$. As shown in Figure 3, the binary outputs for the 3 representative mathematical calculations agree with the expected decimal operations. See the Supplementary Information for all 16 possible mathematical computations able to be determined by the 2-bit adder, subtractor, and multiplier.

We connect a 2-bit adder to LED panels, Figure 4, to demonstrate the sensing, information processing, and response functionalities of one such soft, mechanical integrated circuit material. According to the binary addition, the current flow from the V_{cc} (9 V) source connects and disconnects parallel LED panels that are each in series with an adder output. These LED panels subsequently light up a decimal calculation. The Q_{Cout}, Q_{S2}, and Q_{S1} are connected in series with the "4", "2", and "1" LED panels, respectively.

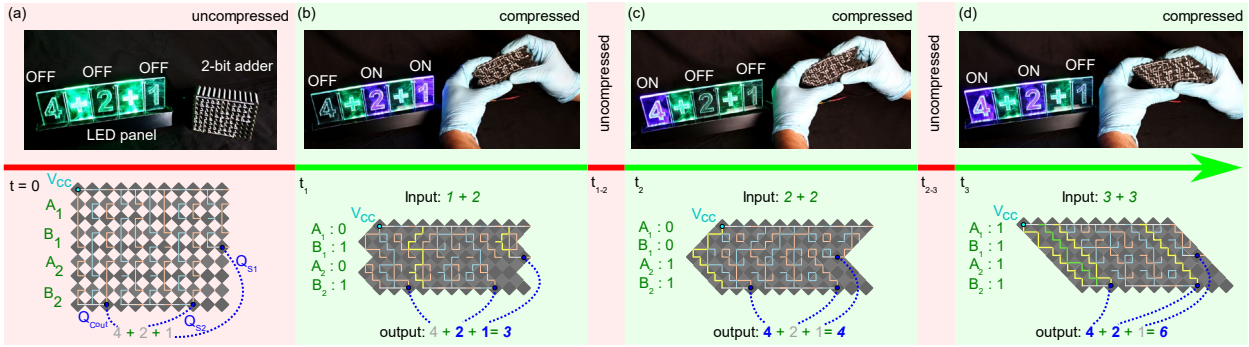

Figure 4. Demonstration of the sensing, computing, and actuating functionalities of a soft material-based 2-bit adder. (a) Image of 2-bit adder with bit value output 2^2 connected to a decimal "4" LED panel, with output 2^1 connected to a decimal "2" LED panel, and output 2^0 connected to a decimal "1" LED panel. Initially at t = 0 all the LEDs are OFF when the 2-bit adder has no digital input. Application of digital inputs to the 2-bit adder to enter the (b) $(0101)_2$, (c) $(0011)_2$, and (d) $(1111)_2$ arithmetic calculations show that the appropriate decimal LED displays are lit (ON) in blue on the LED panel. The corresponding schematic configurations and decimal calculations are shown in the lower row.

In Figure 4(a), the adder initially has no digital input and correspondingly has no output. By manually applying a combination of uniaxial and shear stress at time t_1, the $(0101)_2$ digital input sequence is applied to the vertically stacked input layers. This corresponds to the decimal operation $(2+1)_{10}$. As shown in Figure 4(b), the adder outputs the correct numerical value: 2 + 1 = 3. Since these computing materials have volatile memory, the bit information is lost at time t_{2-3} when the digital inputs are removed, which automatically resets the material. Further digital inputs of $(0011)_2$ and $(1111)_2$ are applied to the soft 2-bit adder as shown in Figure 4(c) and (d), respectively. These and all other 2-bit inputs are correctly summed

as seen via the appropriate decimal outputs in the LED panel display. See the Supplementary Video 1 and Supplementary Information for further demonstrations.

Since the digital outputs in a logic operation are independent of each other, it is possible to decouple such binary switching sequences. In our embodiment of mechanical computing, this corresponds to separate computing material layers that are then networked by stacked assembly. This is exemplified for the 2-bit adder in Figure 5(a). This technique also reduces the quantity of unit cells required in the system fabrication. Conductive traces through the depth of the material provide appropriate parallel interfaces for V_{cc} while the digital inputs act on all layers simultaneously. For instance, the QMSoP 2-bit adder reduces from 44 to 24 material unit cells, which is a 46% reduction in the 2D substrate area. The cross-sectional span of the material computing layers is governed by the largest output network. For the 2-bit adder, this is the layer that computes the Q_{S2} output. Furthermore, the thickness of the layers may be reduced to increase the computational density or bit-resolution of the integrated circuit to any arbitrary extent. Moreover, one may exploit this paradigm to layer *multiple arithmetic operations* in a single mechanical integrated circuit material, underscoring the capability to arbitrarily increase the computational density.

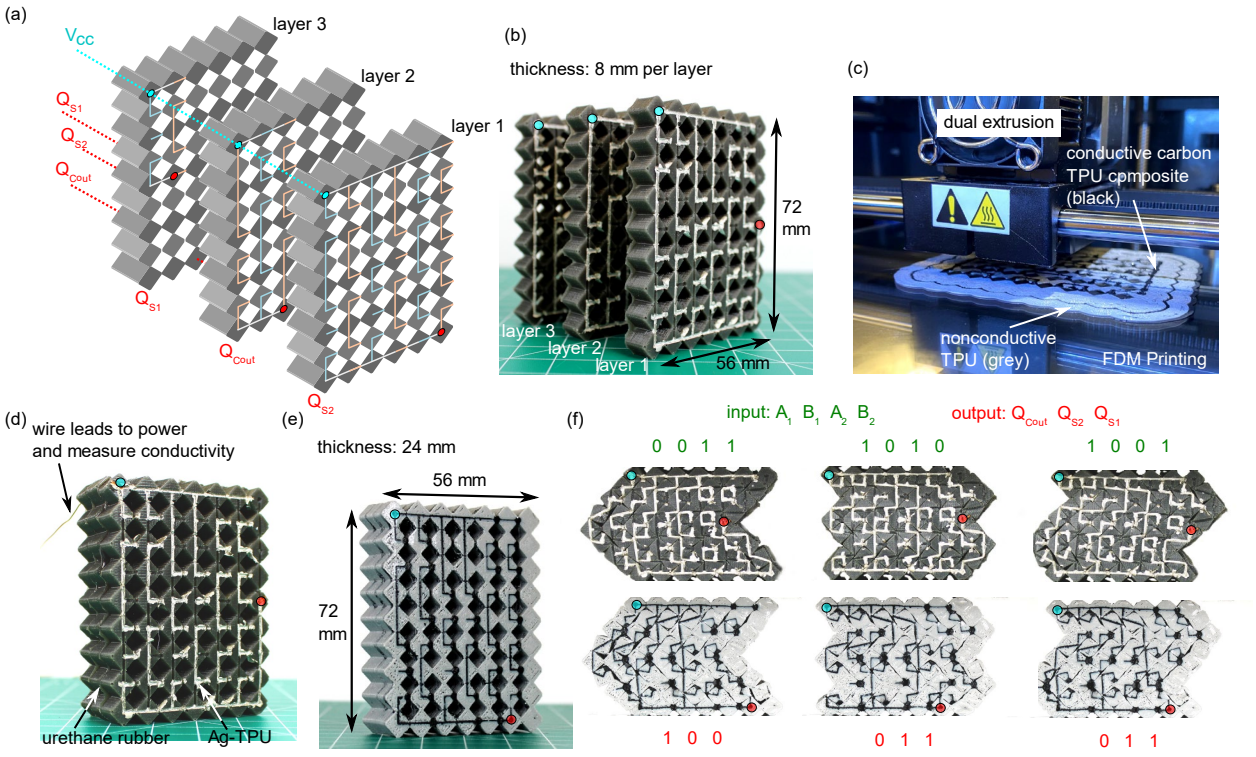

Figure 5. Layered, computing-dense mechanical integrated circuit material. (a) A schematic of a 2-bit adder with three stacked layers that contain the Q_{S2}, Q_{Cout} , and Q_{S1} on layers 1, 2 and 3, respectively. All layers are powered by the same Vcc terminal (cyan). (b) Experimental image showing the three layers made with cast urethane rubber substrates and Ag-TPU networks. (c) Image of commercial dual extrusion printer as it simultaneously prints the substrate and conductive network of a 2-bit adder by the layer-by-layer fabrication method. Photos of 2-bit adders as fabricated using the (d) casting

and (e) additive manufacturing techniques. (f) Experimental results showing three digital input and output combinations for the cast (top) and additive manufactured (bottom) samples.

To experimentally illustrate the layered mechanical integrated circuit materials, two fabrication techniques are proposed. The first technique utilizes the casting method that is used to fabricate the initial samples with urethane rubber and Ag-TPU conductive networks. As shown in Figure 5(b), three layers each with a unique 2-bit adder output network are initially molded and then bonded together with uncured urethane rubber. The second fabrication technique employs multi-material additive manufacturing (AM) to 3D print the 2-bit adder computing material in a layer-by-layer extrusion approach, Figure 5(c), with insulating material as the substrate and conducting material as the electrical network. See Supplementary information for further fabrication details. The casting and AM fabrication techniques both yield operational 2-bit adders as shown in Figure 5(d,e,f).

The formulation of combinational logic created here is grounded in Boolean mathematics [34] and kinematically reconfigurable geometric networks [36]. Consequently, similarly complex and scalable information processing could be achieved in other length scales and in other physics where such principles may be harnessed. Therefore, the sense of "touch" realized here could be augmented with a sense of "sight" via photo-response hydrogels [8] in the material system design process, or with a sense of "hearing" via discretized spectral signaling like that used in the cochlea [37]. Certainly, the soft computing framework formulated here does not compete with the speed and complexity of conventional semi-conductor-based microprocessors. Yet, the information processing cultivated here is sufficiently scalable and advanced to provision future engineered living materials with ample adaptability as they navigate the environment in pursuit of a programmed objective.

In this research, we introduce a robust strategy that exploits canonical Boolean functions and kinematically reconfigurable structures to program combinational logic into soft, mechanical integrated circuit materials. We demonstrate sensing, processing, and responding functions in a monolithic material platform that thinks about digitized mechanical stress via higher-level arithmetic calculations. Any arbitrary combinational logic process may be synthesized by this method and any degree of computational density may be achieved via the layer-by-layer fabrication approach. This foundation can be extended further by the formulation of analog-to-digital conversion layers that help the materials to interface between the analog mechanical loads natural to the environment and the requirement for digital sensory inputs. Nevertheless, as one embodiment of mechanical computing [21], our approach offers advanced decision-making functionality to the toolset of researchers pursuing engineered living systems across a wide range of length scales.

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