FINAL REPORT

Title: Research-to-Adoption of Structured Silicon Anode Technology (SSAT) for Enhanced Safety Fast Charging/Discharging Batteries

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Abstract
High energy density fast charging/discharging batteries will be transformational for military and commercial applications. In this Defense University Research-to-Adoption (DURA) initiative, the research team matured the SSAT battery technology via safety optimization through battery chemistry and modulation design, failure mode, effect and criticality analysis (FMECA), and battery thermal and power management to minimize the deleterious effects of heat on battery life and provide accurate state of health prognosis and early awareness of safety critical failures, thereby enabling broad adoptions of the technology by the defense and commercial sectors.

Key Accomplishments
Through the combined efforts of the team, the structured silicon anode technology was moved from being a basic research effort to a technology that is now under consideration by several large industry groups, including a major automotive manufacturer. Highlights of the team's specific accomplishments are outlined here.

Subproject 1: SSAT Optimization for Safety and Reliability
The structured Si anode (SSA), consisting of porous metal scaffold with thin coating layers of Si was proven to be an effective strategy to mitigate volume expansion related effects of silicon upon lithiation. To better understand the stress concentration during lithiation and to optimize SSA safety and reliability, we performed a series of computational simulations and experimental investigations.

We first used a multi-physics-based finite element (FE) model coupled with cohesive zone modeling technique to simulate the electrochemical process and crack generation during delithiation. On top of that, a Gaussian Processes (GP) based surrogate model is developed to assist the exploration of the crack patterns within the anode design space. By looking at the simulated crack patterns, it was found that with the increase of the Si layer thickness, the area of the Si island also increases. The changes of the areas of Si island are crucial to the reliability performances of Si anode: smaller Si island area indicates more cracks in the Si layer, which could introduce more sites for the formation of solid electrolyte interphase (SEI) and more intensive degradation of the anode. In addition, the influence of the curvatures of the substrate on the areas of Si islands are studied. It is found that, positive curvature leads to a reduction of the Si island area, suggesting an exacerbated fracture scenario; on the other hand, when the curvature is negative, larger area Si islands are observed, indicating that substrates with negative curvatures tend to resist the formation of cracks. The GP based surrogate model is further implemented to predict the Si island area within the design space. The coupling effects of different electrode design parameters, including fracture strength, Si layer thickness and curvature of the substrate, are explored. GP surrogate model is a powerful tool to efficiently explore the design space and assist further optimization design.

Though 3D structured porous electrodes are solutions to address the large volume change of the Si active material, uncertainty and non-uniformity inherited from the fabrication process is inevitably introduced as important considerations for the performances of the Si anode. Several simulation efforts were spent to characterize the effects of non-uniformity on Si anode performance. The multi-physics-based FE model is developed, where the geometric of the non-uniform structured anode is built based on experimental measurements. The stress distribution and deformation of the anode after full lithiation are predicted and compared with experimental results, as shown in **Fig. 1.** It is found that large tensile stress concentrations are shown on the surfaces of Si layers; meanwhile, compressive stress concentrations are mainly observed at the sharp edges of the positive Si layers (circled in red).

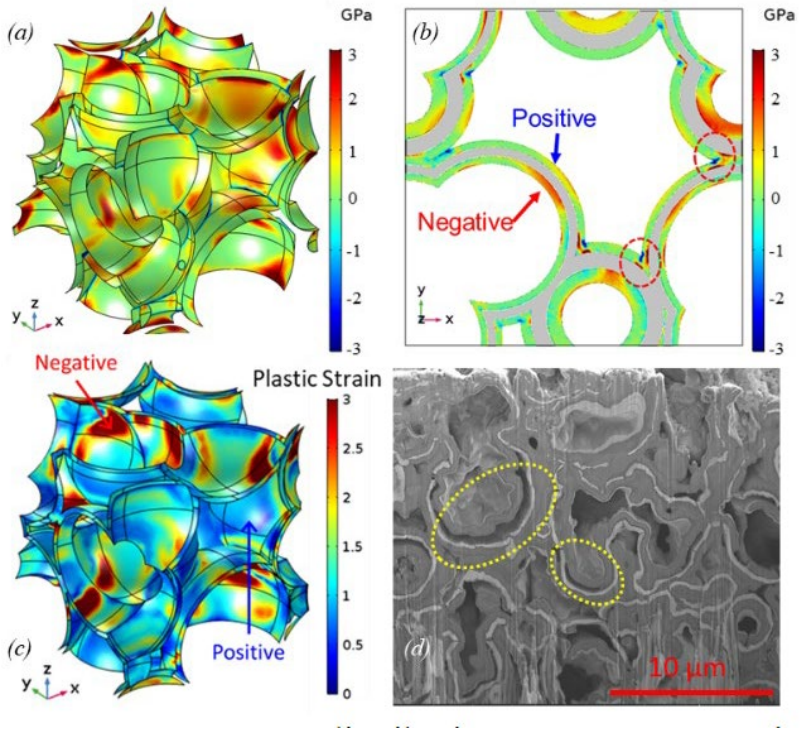


Fig. 1. (a) Stress distribution contours on Si-electrolyte surfaces of the nonuniform structured Si anode; (b) stress distribution on the Si layers, cross section view of the anode, where the gray phases are the scaffold; (c) plastic strain contour on the scaffold surfaces; (d) FIB-SEM image of the cross section of the structured Si anode after 30 charging-discharging cycles.

The high plastic strain spots are primarily on the negative-curvature surfaces (**Fig. 1 c**), which will potentially initiate the delamination between Si and scaffold during charging-discharging cycles. This is confirmed by experimental observation (**Fig. 2 d**). Furthermore, with the increase of scaffold non-uniformity, the stress concentration will also increase; a scaffold made of high modulus material is found to help mitigate the large stress on Si layer; sharp edges in the scaffold is another the critical factor that attributes to the large stress concentration. To further quantify the stress concentration, Gaussian Process (GP) based surrogate model was constructed using finite element (FE) simulation results as training data to mitigate the high computational cost. **Fig. 2** illustrates the predicted stress concentration surfaces using the GP based surrogate model with respect to two selected combinations of the input variables, including the Youngs's modulus E_{Ni} and yield strength of Ni σ_{y_Ni}, and the Young's modulus of lithiated Si E_{Si} and the non-uniformity of scaffold δs, respectively. As shown in **Fig. 2 b**, δs has a big impact on the stress concentration behavior: with the decrease of the non-uniformity of the structured nanoporous scaffold, the stress level on Si can be greatly reduced, because the curvature changes of the scaffold substrates from one pore to another is less significant, resulting in a more uniform distribution of lithiation-induced stress and less stress concentration spots on the Si layer. **Fig. 3** presents the histograms of stress concentration with respect to the change in distributions of t_{Si} or δs, and E_{Si}, E_{Ni} or σ_{y_Ni}, respectively. On one hand, with the decrease variation of t_{Si} or δs from 16% to 4%, the variation of stress concentration on the Si layer can be decreased from 0.43 to 0.32 GPa. On the other hand, the uncertainty of the system is not much affected by reducing the variation of E_{Si}, E_{Ni} or σ_{y_Ni}. Thus, to acquire a better design of the SSA with more stable performances and less uncertainty, the most effective approaches are to narrow the differences of the Si layer thickness, as well as the non-uniformity of the porous scaffold. Lastly, a physics-based FE model is developed to predict the capacity degradation of the thin film Si anode. Multiple potential failure modes, e.g., cracking of the Si material, delamination, and unstable growth of the solid electrolyte interface (SEI), and their coupling effects are included in the FE model. As shown in **Fig. 4 a**, the formation of cracks will be influenced by the thickness of the Si layer. The color legend represents the quality of the interfaces, where 0 indicates that the interface remains intact,

value between 0 and 1 means that the interface is degrading (cohesive strength) but keeps in contact with the adjacent one, and 1 suggests the completely de-bonded interfaces. It can be observed that, when the Si layer is ultra-thin, only 20 nm, neither cracking nor delamination will be initiated and the film could remain intact during charging and discharging cycles; in this scenario, the capacity degradation of the anode is only attributed to the growth of SEI. On the contrary, when the Si layer is thickened to 100 nm, cracks will be generated in the Si layer; the cracked Si island has a dimension of 1×1 μm^2. Consequently, new Si surfaces are created by the cracks and exposed to the electrolyte and become active sites for SEI growth; in addition, the Si layer may also experience delamination from the substrate, leading to electrical isolation and extra capacity loss. As a result, the corresponding capacity fade of the Si anodes with different thicknesses are estimated by the FE model, as illustrate in the **Fig. 4 b**. The FE model results show reasonably accurate prediction compared to experiments. With the increase of the Si layer thickness from 20 nm to 1 μm, the capacity degradation of the anode is largely increased.

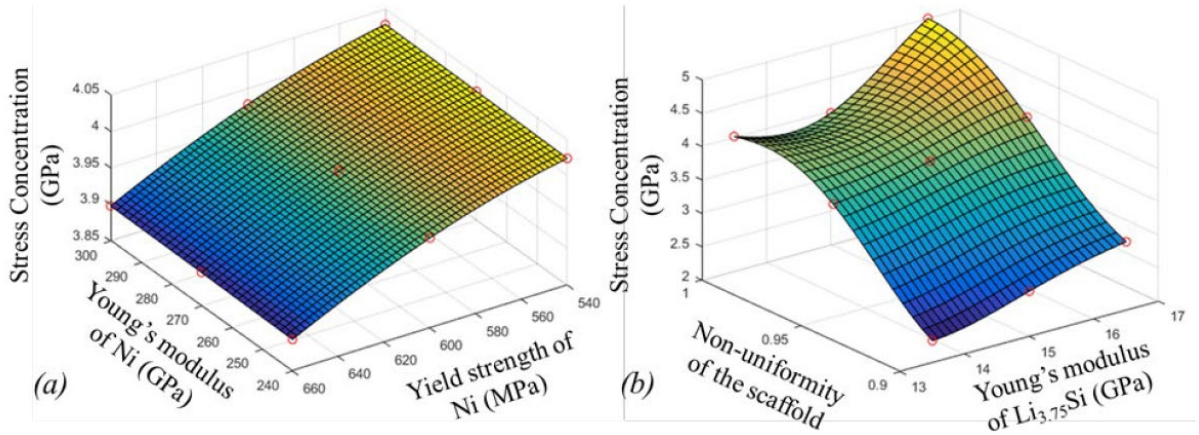


Fig. 2. Predicted stress concentration performance surfaces using the GP based surrogate model with respect to different combinations of input variables, including (a) Youngs's modulus and yield strength of Ni, and (b) Young's modulus of lithiated Si and non-uniformity of scaffold. The red scatters indicate the FE simulation results.

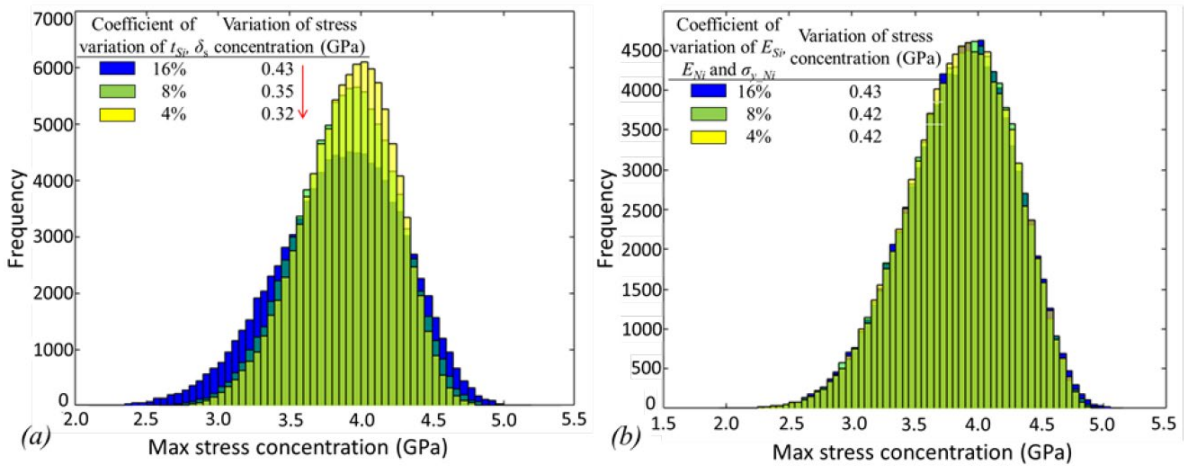


Fig. 3. Histogram of the stress concentration with the change of coefficient of variations of five input variables: (a) t_{Si} or δs, and (b) E_{Si}, E_{Ni} or σ_{y_Ni}.

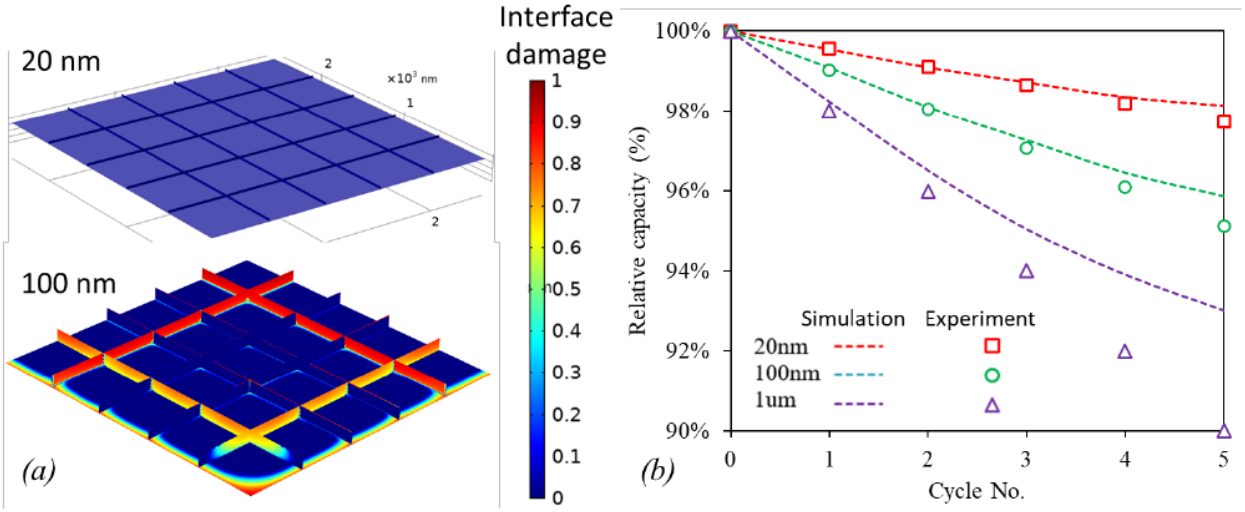


Fig. 4. (a) The simulated cracking patterns on the thin film anodes with different Si layer thicknesses; the color legend represents the interfacial damage, where 0 indicates that the interface remains intact and 1 suggests the completely damaged interface. (b) The corresponding capacity fade of the Si anodes as a function of cycle number considering the couplings among various failure modes.

A deep understanding of silicon chemistry and composition is required for optimizing safety and reliability. For the SSAT, silicon is deposited either via Chemical Vapor Deposition (CVD) or electrodeposition. The goal of this effort is to advance electrochemical routes for synthesis, as that pathway to Si growth is the most scalable. Materials-based development and analysis was completed on in-house deposition methods for the conformal growth of silicon on the nanostructured 3D bi-continuous scaffold. Solution-based electrodeposition was advanced through microelectrode analysis of bath compositions, control of pre- and post-processing conditions, and variation in precursor species. Additionally, high-vacuum static CVD was optimized to produce ultra-high-purity silicon for

baseline measurements of anode performance. The as-deposited material from each method (Electrodeposition and CVD respectively) was measured by CHN-analysis (0.1 wt% detection limit), inductively coupled plasma (ICP;1 ppb detection limit), and halide ion-selective electrode analysis (0.2 ppm detection limit), which report the weight-percent of samples that can be normalized to produce a full chemical composition of the test-material. The two materials exhibited distinct chemical compositions (**Table 1**).

Table 1. Measured and calculated elemental weight- and atomic-percent of elements in CVD and electrodeposited silicon.

	CVD Deposited		Electrodeposited	
Element	Weight %	Atomic %	Weight %	Atomic %
Carbon	0.1	-	0.4	1.4
Hydrogen	0.0	-	0.2	8.7
Nitrogen	0.1	-	0.1	-
Nickel	91.9	82.3	90.5	73.6
Silicon	7.2	13.5	7.2	12.3
Chlorine	0.1	0.1	0.7	0.9
Oxygen*	0.6	2.0	0.9	2.7

**Note: Oxygen is assumed for wt% to at% conversion as oxygen is not directly measured. Missing items are at or below the instrument detection limit.*

This detailed chemical characterization verified the purity of CVD silicon for use as a control and identified major compositional differences as a result of electrodeposition. The latter exhibits 10-fold chlorine content and significant inclusion of carbon and hydrogen as compared to the baseline. However, the origins of O and C measured in the EDEP-Si remain unclear. As will be discussed with electrochemical cycling, oxygen is believed to dominate the lithiation behavior of impurities. Due to the persistent and uniform presence of O throughout the layer, it is unlikely that surface oxidation alone is responsible. Instead, there are several other steps in the synthesis process where oxygen-containing species could be introduced, including trapped oxygen and trace contamination of water in the raw solvents used for the electrodeposition bath, during deposit rinsing and post processing, or exposure during transfer and handling of the samples. These must be systematically examined to identify the major sources of impurities and explore whether they can be mitigated or eliminated.

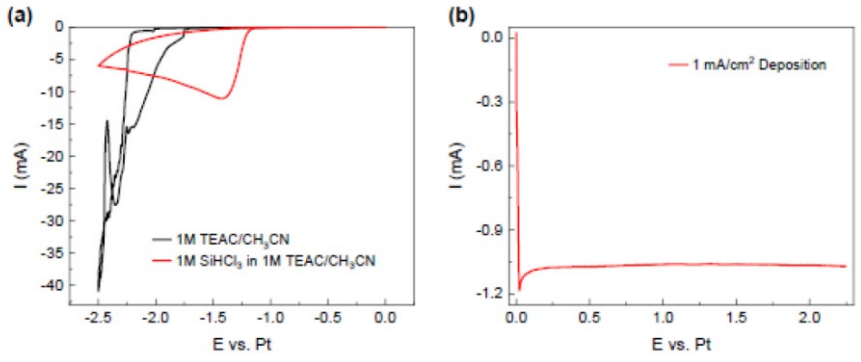


Fig. 5. (a) Cyclic voltammetry profiles of the electrodeposition bath with 1M SiHCl3 precursor (red line) and the acetonitrile solvent with 1M TEAC without precursor (black). Voltage limits are OCV to -2.5 V vs. Pt QRE. (b) Constant current electrodeposition profile of EDEP-Si at an applied current density of 1 mAh/cm^2 for 2.25 hrs.

The bath components used for EDEP-Si are trichlorosilane ($SiHCl_3$), tetraethylammonium chloride (TEAC, $C_8H_{20}ClN$), and propylene carbonate (PC, $C_4H_6O_3$). Of these, only PC contains bonded oxygen within its chemical formula. Confocal Raman spectroscopy revealed molecular structures of PC and TEAC in the deposit

despite apparent solvent stability evidenced by the stable electrochemical window CVs presented for PC baths. Thus, one likely source of O contamination is from the PC itself from full or partial inclusion during layer growth. A number of solvent systems with no bonded oxygen are compatible with trichlorosilane electroreduction, including acetonitrile (CH_3CN) and dichloromethane (CH_2Cl_2). Due to its lower boiling point (39.6 ˚C) and higher density (1.33 g/cm3), dichloromethane could limit the long-term stability of the bath over the deposition time (2.25 hrs), so anhydrous acetonitrile is selected as a logical alternative for PC. Solutions with each solvent were prepared and studied as presented below. It is worth noting that tetrahydrofuran (THF) was also attempted, but miscibility of the solution, stability against evaporation and significant nonuniformity of obtained deposits presented major challenges. Solutions of 1M trichlorosilane (> 98% Aldrich) with 1M TEAC (> 98.0%, TCI Chemicals) in acetonitrile (> 99.9%, anhydrous, Aldrich) were prepared and characterized via cyclic voltammetry (CV) as presented in **Fig. 5** As with the standard PC bath composition, the cathodic wave at -1.15 V vs. Pt is ascribed to the electroreduction of Si from $SiHCl_3$. This is confirmed by the absence of the same wave in a solution prepared without the precursor. The onset of background solvent and salt decomposition is -1.7 V vs. Pt for this system. This is ~300 mV higher than the PC-based solution, indicating a smaller overall voltage stability window. Additionally, CVs performed in the solution containing no precursor resulted in significant yellow discoloration from the decomposition of bath molecules. In full solutions with $SiHCl_3$, discoloration is not observed. Galvanostatic depositions were performed at 1 mA/cm^2 for 2.25 hours. Overall deposition behavior is similar to the PC system; after a sharp initial drop in potential, a plateau around –1.06 V is observed over the deposition (steady state conformal Si growth).

Rutherford backscattering spectrometry (RBS) was used to identify elemental composition and areal atomic density of planar EDEP-Si from different bath and CVD-Si samples. While this method does not provide the same resolution of elemental at% as STEM EDS or XPS, it is significantly more tractable for quick measurements to identify the presence of O via the peak ~750 keV. **Fig. 6** shows the RBS spectra and SIMNRA simulation fits of EDEP-Si grown from PC-based and acetonitrile-based baths. Though the oxygen peak is smaller in the acetonitrile case, it is not completely gone. This indicates O is still present throughout the layer. However, quantification of the spectra reveals a reduced content of oxygen (20-30 at%) compared to the deposit from a PC-based bath (~30-50 at%). This is accompanied by a slight increase in Si content of the acetonitrile deposition (~50 at%). Carbon is also increased to 20-30 at%. As mentioned before, the significant background of the Si wafer substrate obfuscates any clear carbon signal below ~20 at%. Nevertheless, the required concentration for accurate Si and O peak fitting falls within the experimental data. Overall, the acetonitrile-based deposit exhibits reduced oxygen and increased carbon and silicon compared to the PC-based deposit. This should be further verified with a complimentary compositional technique such as STEM EDS or depth profiling XPS to refine distributions of chemical species.

Confocal Raman spectroscopy was used to identify the nature and types of Si, C, and O bonding present in the EDEP-Si (**Fig. 7**). A complex chemical structure was found consisting of Si-Hx, Si-C, and Si-CHx type bonds in addition to the expected Si-Si network. The as deposited samples share characteristic features of Raman activity for Si–Hx bonding between 2000 cm^{-1} and 2300 cm^{-1} as well as the CHx-type bonding around 3000 cm^{-1}. There is very little activity correlated to Si bonding at low wavenumbers. For both elevated temperatures studied (~314 ˚C and ~ 336 ˚C) the high wavenumber signals are gone, and clear emergence of Si-Si coordination is observed around 500 cm^{-1}. These peaks are consistent with the TA, LA, LO, and LA vibrational modes of Si reported by Vichery et al. and observed for our CVD-Si, suggesting the onset of this transformation occurs below 400 ˚C. Additionally, pronounced Si–H bonding can be seen around 630 cm^{-1}. The presence of this signal implies that the hydrogen introduced through electrodeposition is not driven out of the layer at the temperatures studied. This coupled with the densification studied earlier suggests an overall rearrangement of the bonding network and stabilization of the Si bonding in the electrodeposit. Interestingly, these experiments represent annealing below and above the temperature associated with the thermal event observed in TGA, though no significant difference in Raman activity is measured.

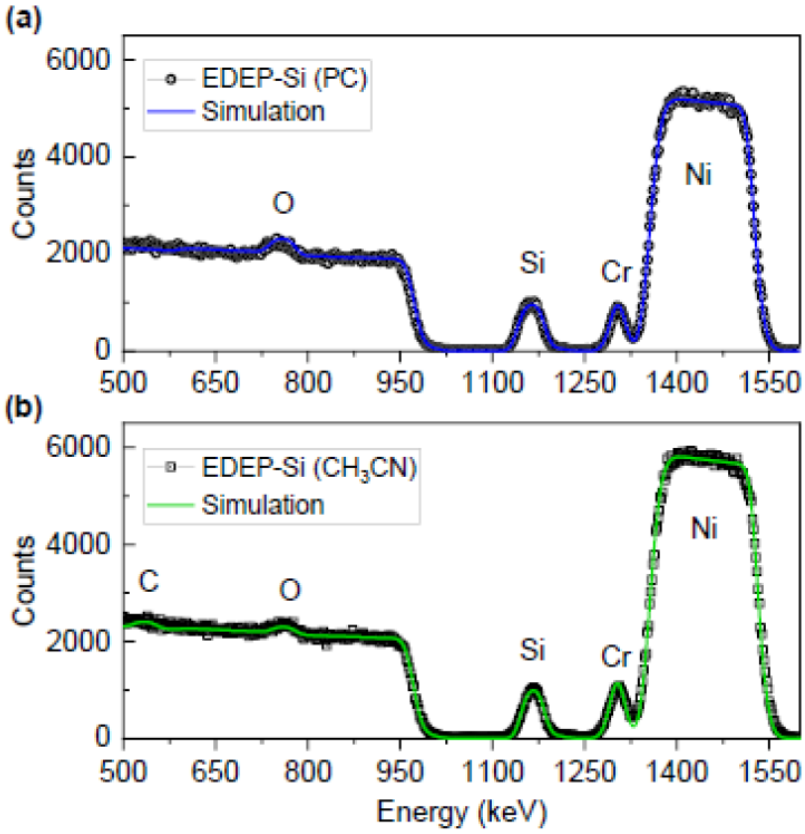


Fig. 6. RBS spectra of (a) PC-based and (b) acetonitrile-based EDEP-Si. Symbols represent experimental data, and the solid lines are the SIMNRA fits.

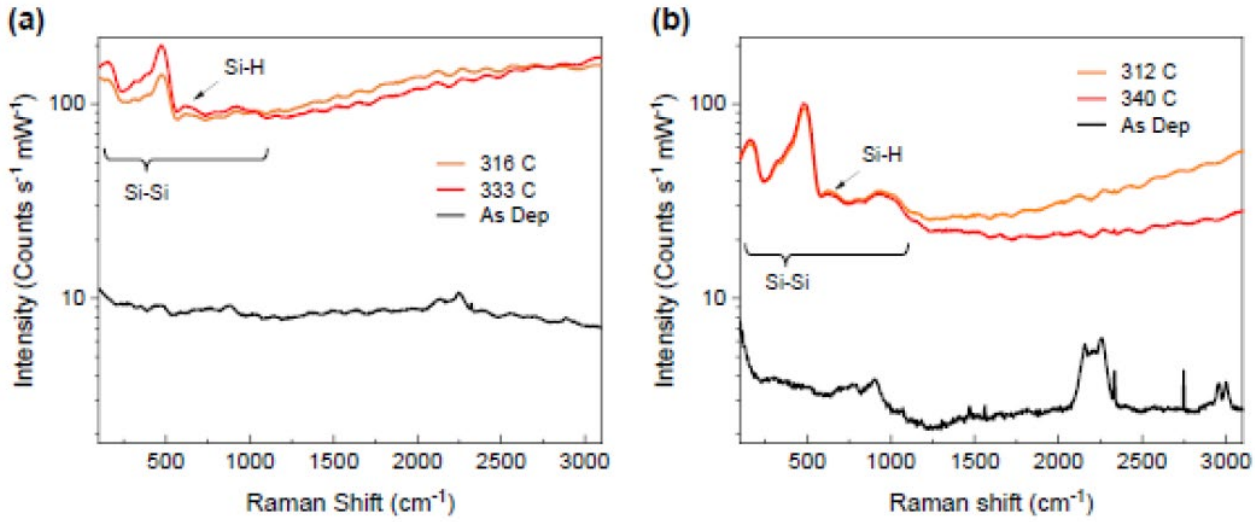


Fig. 7. Confocal Raman spectra (532 nm excitation) of EDEP-Si on (a) 3D Ni foams and (b) planar substrates after deposition and annealed to indicated surface temperatures.

To assess the electrochemical behavior of material grown from an acetonitrile-based bath with that grown from a PC-based solution EDEP-Si foams were assembled into Li half-cells. **Fig. 8** shows the galvanostatic charge-discharge behavior of assembled cells with associated differential capacity plots. Compared with previous results, the overall cycling behavior is like that of EDEP-Si plated from a PC-based bath. The discharge capacity normalized to the electrode area (geometric) is ~1.5 mAh/cm^2 with comparable voltage profiles. Additionally, the peak ~470 mV vs. Li is present, associated with conversion of oxygen within the deposit with lithium. Some noise is evident in the first cycle, but principle lithiation peaks of Si are clearly identifiable at ~211 mV vs. Li and ~74 mV vs. Li in the discharge (lithiation) of all cycles with complementary reverse changes during charge (delithiation). Given the moderate decrease in oxygen content measured by RBS, we could expect a minor improvement to the early cycle behavior. However, this is not distinguishable as evidenced in Figure 3 c by similar first cycle efficiency (FCE), 72 % compared to 73% for acetonitrile-based and PC-based deposits, respectively. Upon close inspection of the coulombic efficiency (CE) of each deposit over 50 cycles, both deposits exhibit overlapping cyclic reversibility for lithium storage. These results suggest the changing of solvent for deposition alone does not lead to large-scale changes in the lithiation behavior of the material. This is not surprising given the significant amount of O still measured in the material. Nevertheless, this speaks to the congruency of deposition solutions and flexibility of solvent-choice without major impacts on material performance.

As shown in **Fig. 9**, the impact of these bath inclusions on electrochemical performance is exhibited by a 13.6% lower first cycle efficiency (FCE) and reduced round trip efficiencies (RTE) for the first 15 cycles compared to CVD-Si. Thereafter the reversible specific capacity per gram of Si (~2700 mAh g^{-1}), coulombic efficiency (CE), and fade behavior match that of the CVD-grown baseline. As a practical implication for this work, the presence of EDEP-Si deposition inclusions may necessitate a pre-conditioning to compensate for initial Li reactions. However, the extended electrochemical performance of the Si within this material indicates high utilization of the deposited Si that exhibits good stability and low cyclic fade. Thus, we conclude that the chemical species introduced via electrodeposition do not limit high utilization of the underlying Si in LIB applications. This further supports adoption of this technique for deposition on complex battery electrode structures, increasing the viability for high loading Si-dominant anodes.

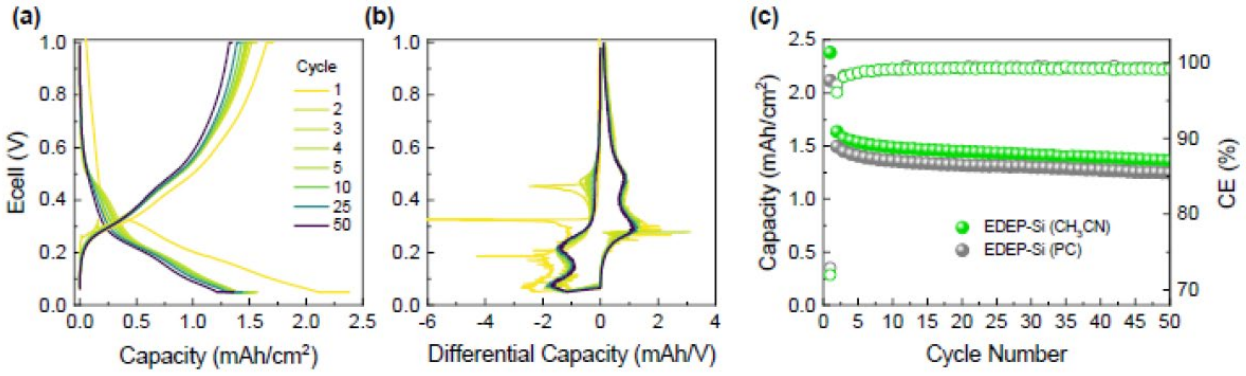


Fig. 8. Cycling performance of EDEP-Si from an acetonitrile-based solution on 3D Ni foam substrates, including (a) charge-discharge curves (b) corresponding differential capacity, and (c) cycling stability of discharge capacity for acetonitrile-based and PC-based coatings. Current rate is C/20 for the first cycle followed by C/5 for all subsequent cycles. Deposit mass loadings for electrode coatings from CH3CN and PC are 0.53 mg/cm^2 and 0.65 mg/cm^2, respectively

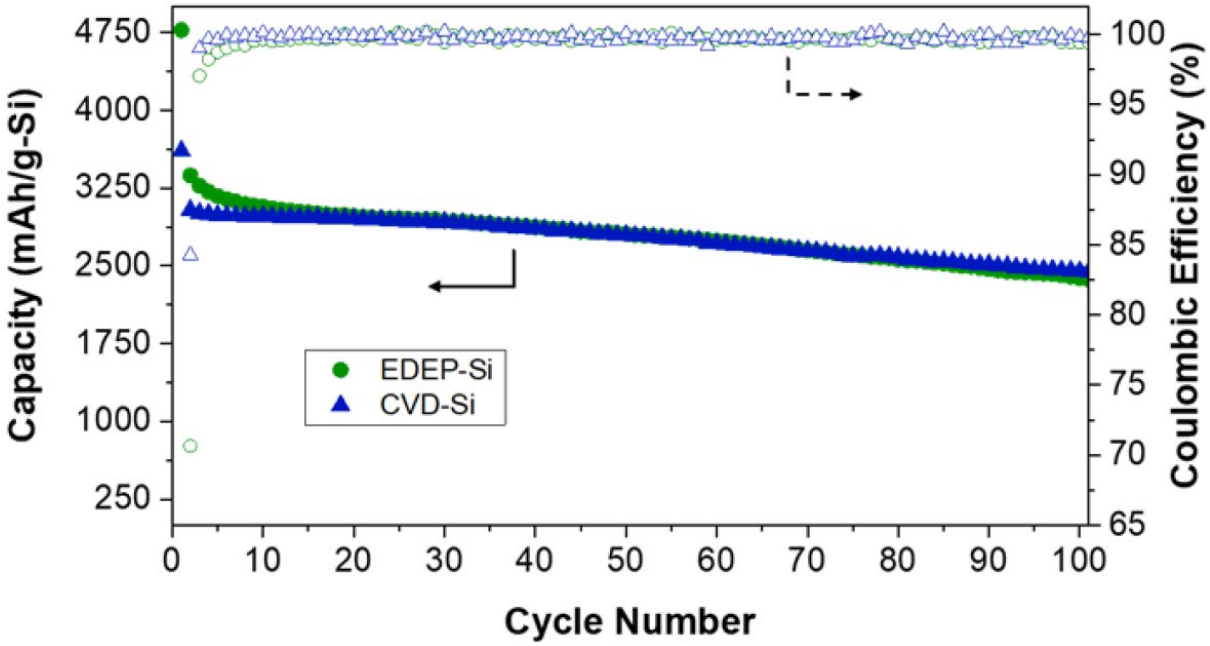


Fig. 9. Cycling performance of EDEP-Si porous Ni-foam anodes compared to CVD-Si coated baseline normalized to grams of Si.

Subproject 2: SSAT Failure Mode, Effect and Criticality Analysis

The key failure modes of the SSAT is cracking of the three dimensionally structured Ni foam which serves as the support for the silicon active material. Fatigue due to the expansion and contraction of silicon during lithiation/delithiation is perhaps the cause of cracking in the foam. To determine if this failure mode is the dominant factor, we performed thermal and electrical measurements of the foam to measure crack formation. We also accessed different factors that can contribute to SSA failure, for instance, solid electrolyte interphase (SEI) layer, faster lithiation/delithiation, stress evolution during cycling and so on.

Early efforts focused on thermal imaging of the scaffold during resistive (ohmic) heat generation.

However, the results were not promising. During resistive heating, heat transfer and current transfer become coupled. Scaffold breakage reduces current flow; thus, less heat is generated. Scaffold breakage also reduces heat flow, and the two effects largely cancel each other out, making determination of the effects of scaffold cracking difficult (perhaps possible using time resolved imaging, but that also has challenges). We thus chose a purely thermal based method using a spot heater which would allow us to clearly isolate the impact of change in the local thermal conductivity. Here, the heater rods are allowed to heat until a steady state is reached. Then using IR thermography, an image of the temperature field in the scaffold is captured. This temperature field is then compared with the extensive simulation results that were performed for the exact setup. Through minimization of R2 deviation and interpolation, we then arrive at the conductivity of the scaffold (**Fig. 10** and **Fig. 11**).

As established, accurate simulations are important for extracting the thermal conductivity results from the experimental data. To that end, a full 3-D simulation was developed in ANSYS Icepak (**Fig. 10 b**). The experimental geometry is modelled as is, in a room of ambient air to model natural convection. The scaffold is simplified as a solid conducting foam with effective properties for conductivity and density. Results from the simulation show variations in the temperature field which are very much in line with IR thermal imaging results. Extensive simulations were performed to further fine tune the setup. Based on the simulations a sensitivity matrix was built, which tabulates the trends (**Fig. 12**). Finally, based on the experimental data so far, conductivity for bare Nickel scaffold was concluded to be close to 15 W/m-K (**Fig. 11**), which matches that expected for effective media theory.

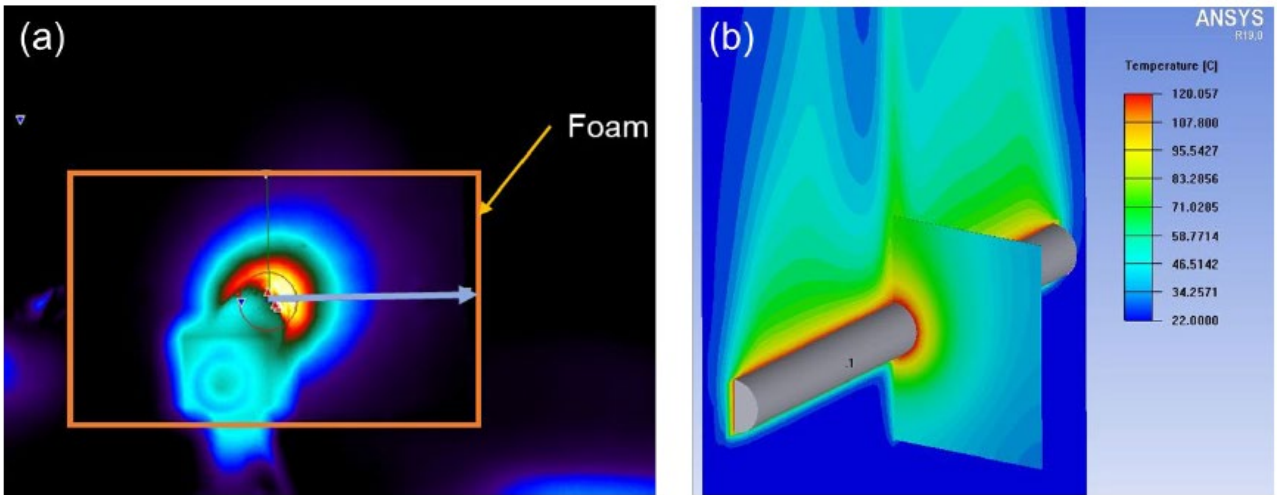


Fig. 10. Temperature fields as obtained from (a) experiments, (b) simulations

Experimental measurements of the thermal and mechanical properties of the silicon anodes are of crucial importance and are difficult to achieve high accuracy. Very fast instruments are required to track the heat flow and acoustic waves in <100 nm-thick films, because in most materials acoustic waves travel a few nanometers in a picosecond and heat flows about a hundred nanometers in a nanosecond. Time-domain thermoreflectance (TDTR) is one of the ultrafast laser systems by which the thermal and mechanical properties of thin film material can be measured. During the measurement, an optical pulse is focused onto an absorbing material and creates a localized increase in the temperature. A thermal stress is then generated by thermal expansion of the material. Once the material is heated up, the change in the reflectance of the surface can be utilized to derive the thermal properties, and the acoustic echoes detected can be used to measure the velocity of sound and elastic constant of the materials. We have utilized TDTR to measure the thermal conductivity, speed of sound,

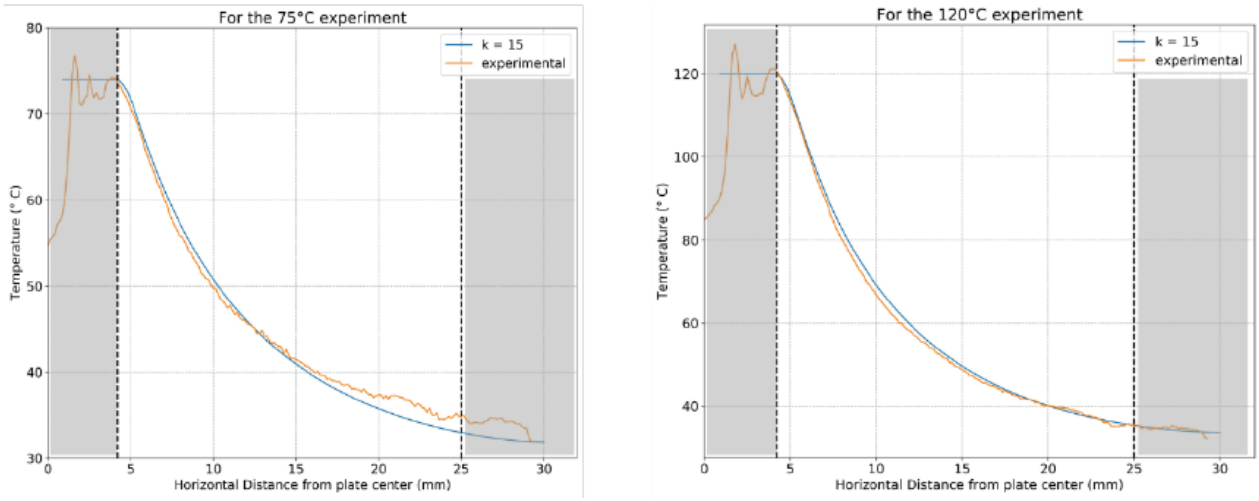


Fig. 11. Experimental vs Simulated data for different spot temperatures.

"Free" Parameters	Thermal conductivity (k)	Natural Convection HTC (h)	Heater Temperature (T)	Scaffold thickness (t)	Radiation (Q_{rad})
Thermal conductivity (k)		Become independent for our useful range of k values	Independent	k·t = constant Accurate scaffold thickness needed	Independent
Natural Convection HTC (h)	average h tends to 7.5 W/m²K with increase in k		Full 3D simulation necessary to capture h, cannot use a constant average value	Independent	Radiation cannot be ignored, needs to be accounted for in simulation
Heater Temperature (T)	NA (Both are inputs)	local and average h both increase with increase in T		Independent	Power law obeyed, simulation takes care of this automatically
Scaffold thickness (t)	Increasing k and decreasing t has the same effect	average h does not change on doubling t, local h changes insignificantly	NA (Both are inputs)		Internal radiation negligible as compared to external
Radiation (Q_{rad})	NA	a new radiative HTC (h_{rad}) added $h_{total} = h + h_{rad}$	Q_{rad} increases as T increases	No effect	

Fig. 12. Sensitivity matrix for impact of different parameters.

and elastic constant of silicon thin films deposited by chemical vapor deposition and electrodeposition methods. As shown in **Fig. 13**, the thermal conductivity of CVD-Si has been determined to be k≈1.28 W/mK, which is close to the value of amorphous silicon dioxide. The thermal conductivity of electrodeposited silicon layer is much lower, which is only k≈0.18 W/mK. This result indicates that the electrodeposited silicon behaves more like a polymer film that contains silicon instead of a dense silicon layer. The speed of sound and elastic constant values of these two materials also support our conclusion. The speed of sound of CVD Si is about 6.0 nm/ps, corresponds to a C_11≈67.3 GPa, while the speed of sound of the EEDEP Si is only 1.8 nm/ps, showing a polymer like elastic constant C_11≈5.9 GPa. Work is ongoing to characterize the EDEP-Si material after cycling with TDTR. These physical characteristics (especially after cycling) are important input parameters for all multi-physics simulations. Additionally, they grant insight into the fundamental heat transport characteristics of the silicon layer which underpin heat transport in the system overall.

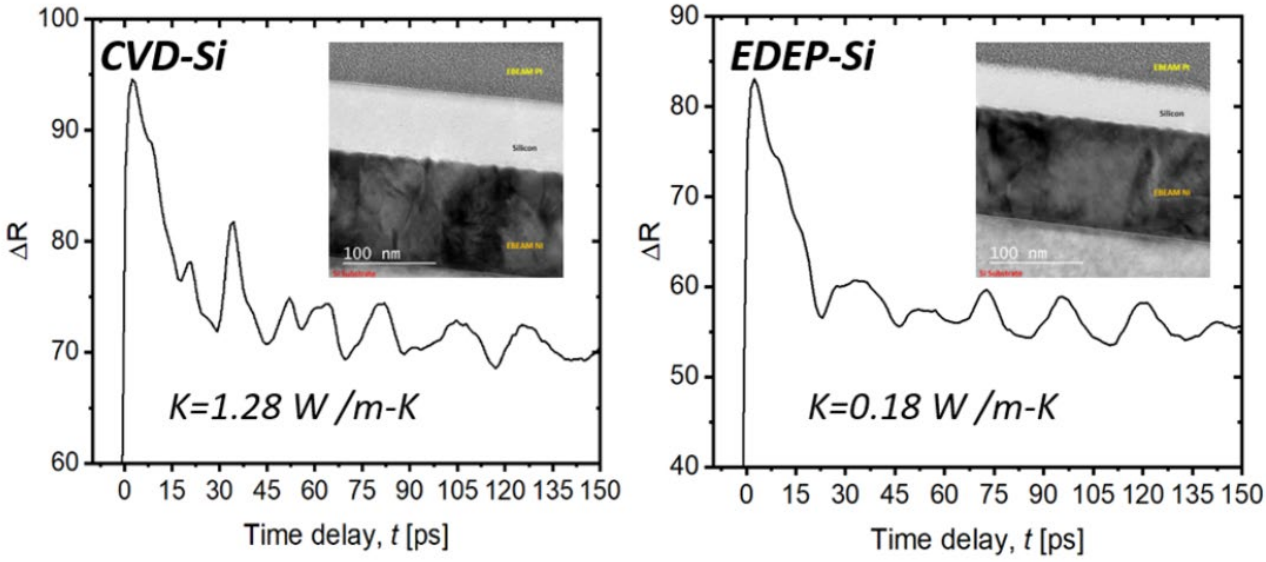


Fig. 13. TDTR results for CVD-Si and EDEP-Si. Insets: TEM cross sections used for thickness measurements and speed of sound calculations.

Electrochemical measurements of SSA were performed to access the SSA stability and failure mode. Galvanostatic charge-discharge curves with corresponding differential capacity plots are shown in **Fig. 14**. The plateaus in charge-discharge profiles can be correlated to phase transformations in the material at specific voltages and Li concentrations. This is used to track material evolution and assign transferred charge to specific electrochemical reactions through cycling. In the first lithiation of the CVD-Si foam, only three peaks are observed (**Fig. 14 c-d**). Peak 1 at 73 mV and Peak 2 at 235 mV vs. Li+/Li, are ascribed to the principal lithiation phases of a-Si, corresponding to approximate alloy compositions of ~Li_7Si_2 and ~Li_2Si, respectively. Unequivocal attribution of Peak 3 at 263 mV vs. Li+/Li is challenging as discussed in the literature. In this potential range given the high baseline composition of Si, this process could be ascribed to the reduction of the native SiOx, Li trapping due to dangling bonds at the electrode surface, and formation of SEI on the exposed Si. These irreversible processes all occur at higher potentials than the principal lithiation of a-Si and are usually most pronounced for the first discharge of the electrode, where any SiO_2 has yet to reduce, dangling bonds have not been passivated, and the largest area of fresh Si is exposed to the electrolyte. Thereafter, considerably less charge is transferred in this same potential region. For CVD-Si, Peak 3 is significantly reduced in the second cycle, existing only as a shoulder around 337mV vs. Li+/Li (inset of **Fig. 14 d**). The persistence of this signal might be explained by the continual cracking and reforming of the SEI layer as the Si expands and contracts upon continued lithiation and delithiation. Four peaks are observed for the EDEP-Si foam during the first lithiation in the voltage window of 1 V to 50 mV vs. Li+/Li. As with CVD-Si, Peak 1 and Peak 2 at 60 mV and 177 mV vs. Li+/Li, respectively, are attributed to the same principal alloying phases of Si arising from specified concentrations of Li. Peak 3 is quite pronounced in the first discharge but is undiscernible in cycle 2, as shown in the inset of **Fig. 14 b** at ~343 mV. Therefore, this can also be attributed to one or more of the first cycle processes described for the CVD-Si foam above. However, Peak 4 observed at ~430 mV vs. Li+/Li is unique to EDEP-Si and consistently decays over the first 10-20 charge-discharge cycles before fading away. The integrated charge transferred in this potential region corresponds to electrochemical reactions that are distinct from the reversible lithiation of underlying Si found at Peak 1 and Peak 2.

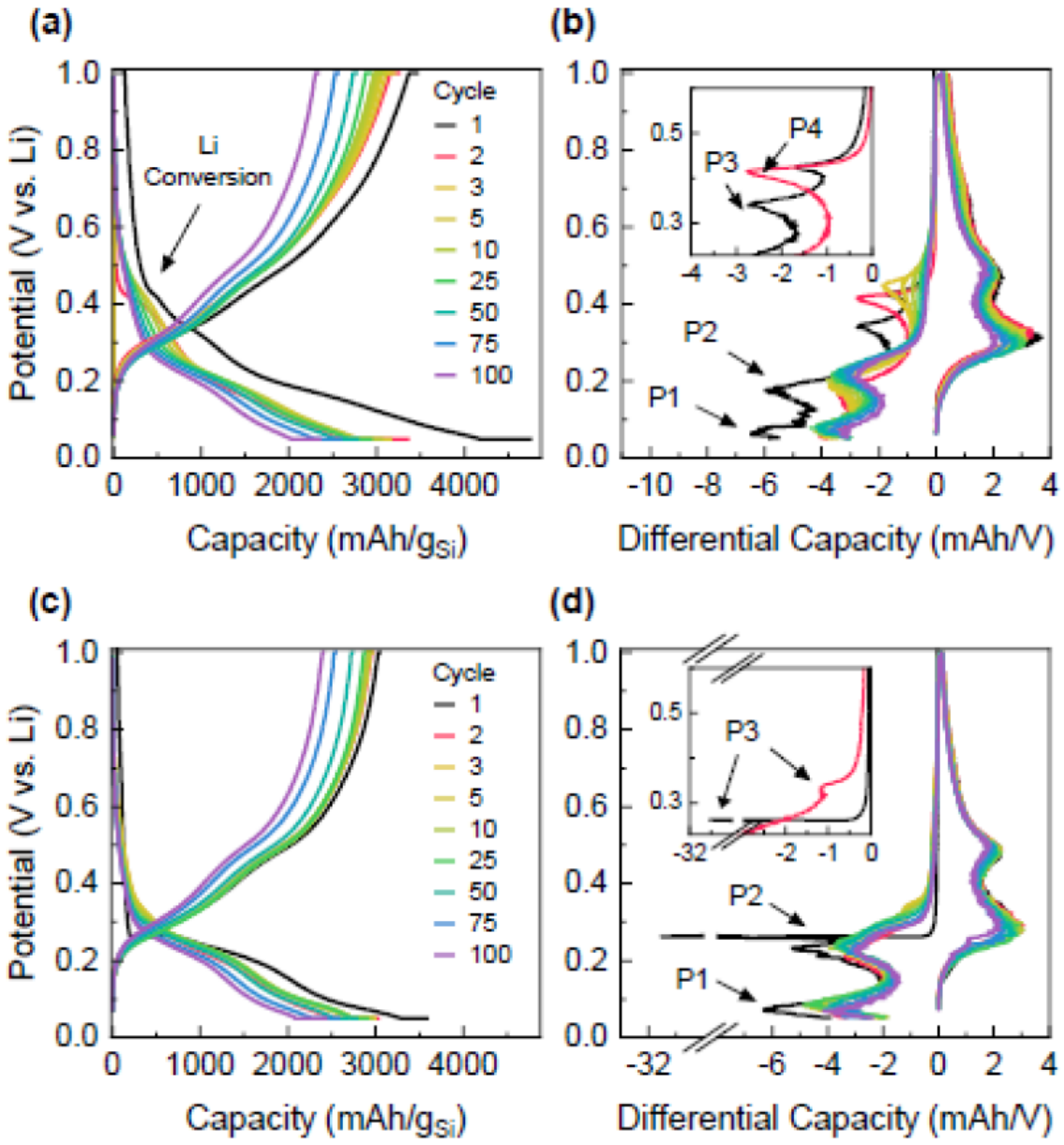


Fig. 14. Selected galvanostatic charge/discharge curves and differential capacity plots with magnified insets around Peak 3 and 4 for (a,b) EDEP-Si and (c,d) CVD-Si. After formation, cells were cycled between 50 mV to 1 V vs. Li at C/5. Calculated Si loadings for the EDEP-Si and CVD-Si are 0.44 mg/cm^2 and 0.6 mg/cm^2, respectively.

To investigate changes in the morphology of cycled electrodes, ion-polished cross section SEM images of 3D structured EDEP-Si and CVD-Si anodes are presented in **Fig. 15**. as prepared after deposition, formation, 5 cycles, and 30 cycles. Both surface roughness and bulk layer thickness change significantly with increasing cycle number, so materials will be discussed in turn. For the EDEP-Si (**Fig. 15 a-d**) the surface of the fresh deposit is smooth and conformal as expected. As pointed out in earlier sections, the nodules inherent to the bare foam are not a product of deposition. After the first cycle, a slight increase in roughness presents as small bumps on the layer surface, which continue to grow and roughen slightly after 5 cycles. After 30 cycles obvious cracks are visible in the coating which has formed rough interconnected islands. Nodules and outgrowths are also present across the surface, which are distinct from those inherent to the foam substrate. This morphology is correlated to increased delithiated Si layer thickness outlined in Table 1. From a starting thickness of 56 +/- 7 nm, the EDEP-Si swells to 93 +/- 11 nm after formation and maintains a 91 +/- 10 nm thickness after 5 cycles. Despite this significant jump in thickness, the layer remains continuous and adherent to the scaffold. However, after 30 cycles the layer is 170 +/- 30 nm thick and exhibits widespread cracking. The CVD-Si undergoes similar evolution as shown in **Fig. 15 e-h**, though this material exhibits accelerated deformation compared to EDEP-Si. The as-deposited surface is smooth and conformal with a film thickness of 43 +/- 6 nm. After formation, the delithiated layer is 59 +/- 8 nm, and the surface shows roughness similar to the EDEP-Si after 5 cycles. After 5 cycles, the CVD-Si layer has bimodal thicknesses of 56 +/- 8 nm along continuous sections and 83 +/- 16 nm islands. The layer has become quite rough and nonuniform with cracks visible along the coating cross section. This deformation is significantly more pronounced after 30 cycles, where only island structures are present with an average thickness of 158 +/- 58 nm separated by widespread deep cracks. The wrinkling and cracking of the layer is likely due to the extensive mechanical deformation upon cyclic expansion of the material as shown extensively in literature for Si. The EDEP-Si exhibits a thicker Si layer in the delithiated state. Moreover, it contains a lower atomic fraction of Si compared to CVD-Si, so it is reasonable to conclude the EDEP-Si expands less per cycle than CVD-Si. This could help to explain the observed trends in morphology.

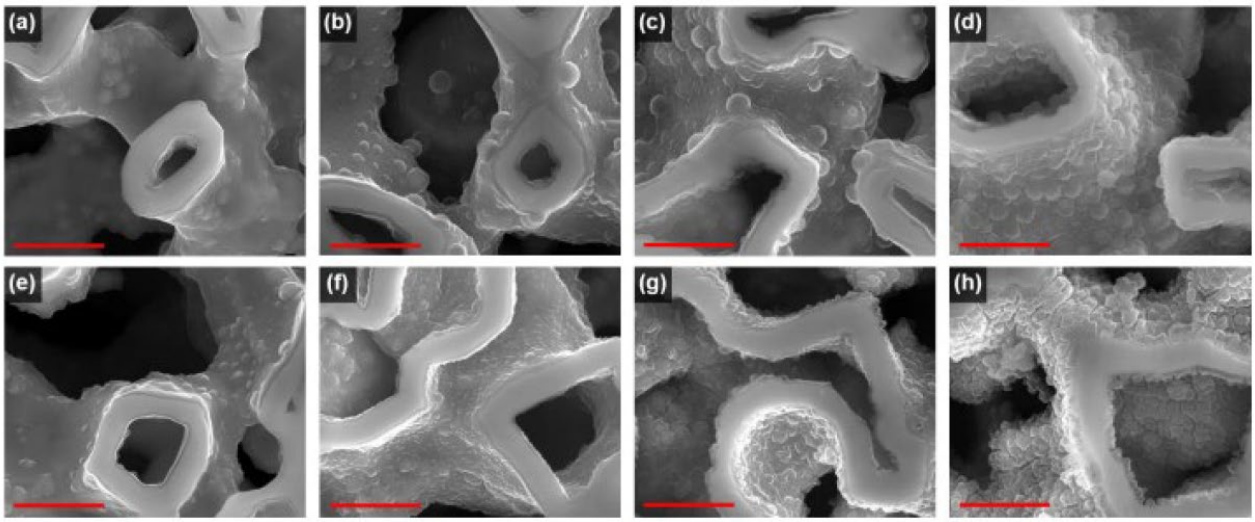


Fig. 15. SEM cross-section of (a-d) EDEP-Si and (e-h) CVD-Si 3D foam anodes (a,e) as deposited and after (b,f) formation, (c,g) 5 cycles, and (d,h) 30 cycles at C/5. Scale bar for all images is 2 μm.

Continual growth of the solid electrolyte interphase (SEI) is one of the most dominant failure modes of the silicon-anode system. Long term stability and integrity of the SEI especially important for high surface area electrode designs like the SSAT. Using both RD810 and LHCE electrolytes, postmortem analysis was conducted on cycled cells at various cycle intervals. As shown in **Fig. 16**, even after 240 cycles the SEI layer formed in the LHCE electrolyte remains conformal, uniform and in-tact after 240 cycles. However, the RD810 system shows clear signs of unstable SEI formation after only 130 cycles. The silicon layer appears to delaminate, and the underlying Ni foam undergoes significant mechanical deformation and crack formation. Additionally, a multi-physics-based FE model was developed that couples an electrochemical module, lithium diffusion module and solid mechanics module to calculate capacity degradation caused by SEI growth. Two main assumptions of the simulation were that capacity degradation is solely attributed to the growth of SEI, and parasitic reactions which form the layer consist of two terms: 1) the continuous growth of SEI on the original surface and 2) the instable growth on new surfaces due to SEI cracking, Experimentally, the simulation results were validated using SSAT half-cells with very low loading of silicon. **Fig. 17** shows the comparison of the capacity degradation of the Si anode from the simulation model and experiments at different discharging C-rates. In general, relatively good predictions of the capacity at various C-rates are obtained. Higher C-rate could lead to a larger lithiation induced stress concentration and strain level (cracking) on the Si surfaces, resulting in a wilder growth of SEI and a higher capacity loss.

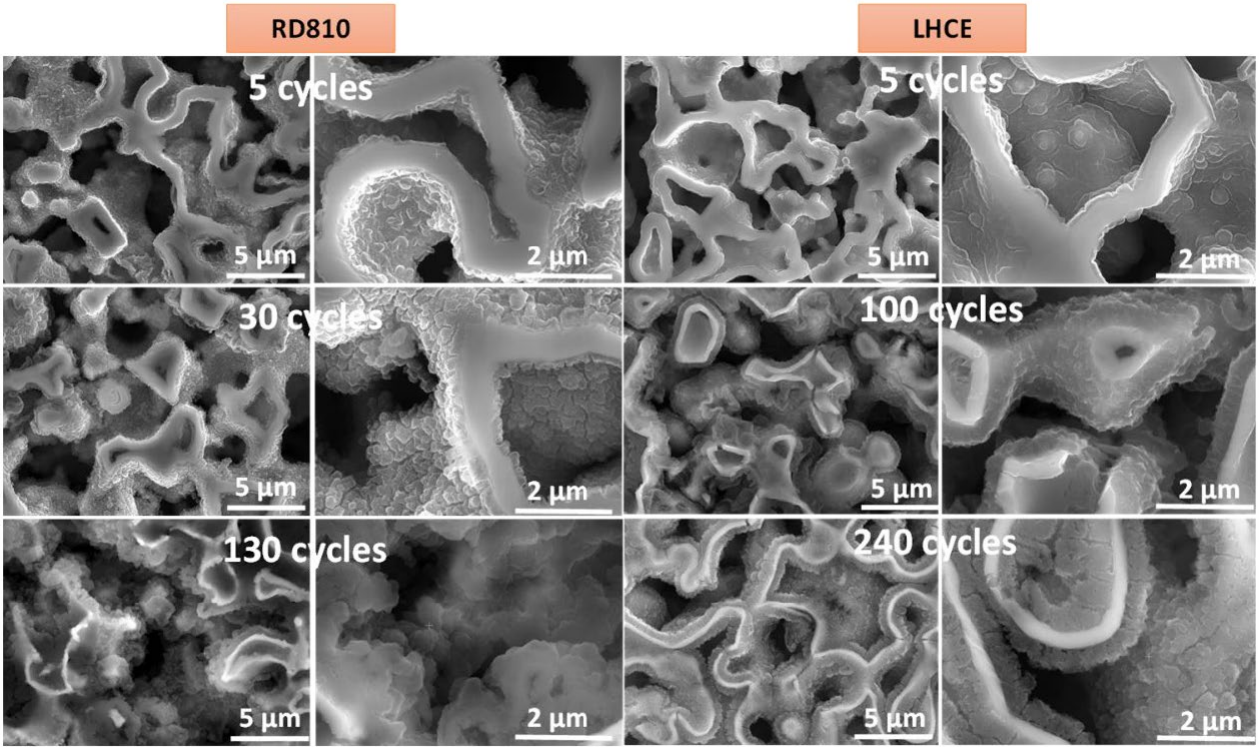


Fig. 16. Post-mortem SEM images of cycled SSAT anodes.

To obtain a fundamental understandings on the influences of the lithiation-induced deformation on the electrochemical performances and energy dissipation phenomena of Si, an electrochemical-mechanical-thermal coupled finite element (FE) model and experimental approaches are employed to investigate the energy dissipation of the thin film Si anode and quantify the effects of several critical design parameters, e.g., lithiation C-rate, Si layer thickness and depth of lithiation, and the energy losses due to various mechanisms, including mechanical dissipation, polarization loss and joule

heating, are discussed.

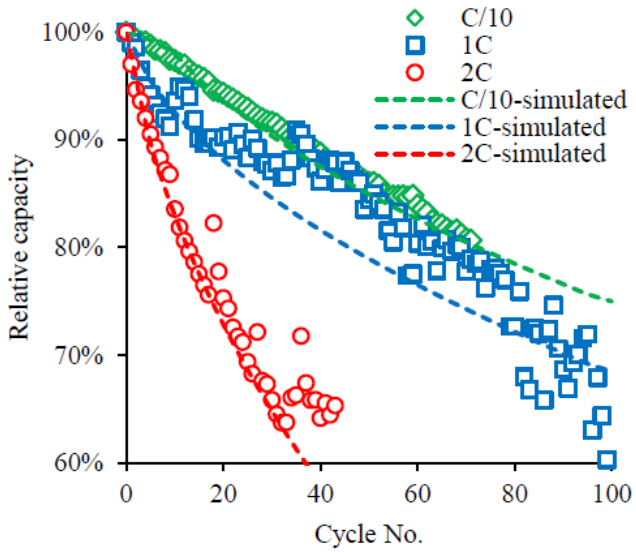


Fig. 17. Comparison of the relative capacity degradation of the Si anode from simulation model and experiments under different discharging C rates.

Fig. 18 illustrates simulated cycling curves of the Si anode half-cells with respect to the state of charge (SoC) under constant current (CC) protocol with different lithiation C-rates from C/3 to 2C. The Si film has a thickness of 250 nm, which is consistent with experiments. The cycling window is determined based on the cell potential ranging from 50 mV to 1V, consistent with experimental setup. Note that, the Si anode is assumed to be fully lithiated when reaching 50 mV, i.e., SoC = 1; the SoC during the cycling process can then be calculated accordingly. The cycling processes start from the first lithiation of the brand-new cells, followed by the first delithiation up to 1 V and the second lithiation process till 50 mV. The simulation results are further compared with experiments; as can be seen, the FE model can rather accurately estimate the electrochemical responses of the Si anodes. The first and second lithiation curves almost coincide, because no significant side reaction or material degradation are involved yet, suggesting that the energy dissipations, both simulated and experimentally measured, should be attributed to the material properties of the anodes rather than any other battery failure mechanisms. Besides, with the increase of C-rates, the potential differences of the anodes between lithiation and delithiation process are largely extended: for C/3, the potential difference, ΔV, at SoC = 0.6 is about 0.21 V, whereas for 2C case, the ΔV becomes 0.64 V, almost three times high. Moreover, higher C-rate is found to obstruct the lithium storage capacity of Si anode and lower the reversible energy; for example, at C/3, the delithiation process stops at SoC $\approx$ 0.04 when reaching the cutoff voltage of 1 V, indicating that most of the stored energy during lithiation can be eventually released and the lithium residue in Si is minimal; on the other hand, when using 2C condition, the cutoff SoC is as high as 0.2, suggesting a large portion of irreversible capacity and low energy efficiency. This is because the high C-rate could result in an increased overpotential at the electrode-electrolyte surfaces, causing the exaggerated polarization effect, along with the reduction of coulombic efficiency and the shrinkage of cycling SoC window of the battery.

Fig. 19 illustrates the estimated stress evolutions of the Si anodes as a function of SoC with various C-rates. The stress curves start from the very first delithiation process at SoC = 1, followed by the second lithiation process. Note that, since the cycling potential window of the anode is predetermined and higher C-rate condition could generate larger polarization effect, the ending SoC points of delithiation curves are different. The stress evolution process consists of four stages. Firstly, at the initial delithiation stage, Si experiences elastic deformation from compressive to tensile states; it is worth mentioning that since the Si-Li alloy is hardened upon delithiation, the stress curves are not entirely linear, and the slopes of the curves change gradually. Besides, higher C-rate is found to have a slightly stronger hardening effect, where the stress in the Si film is larger and the Si material reaches

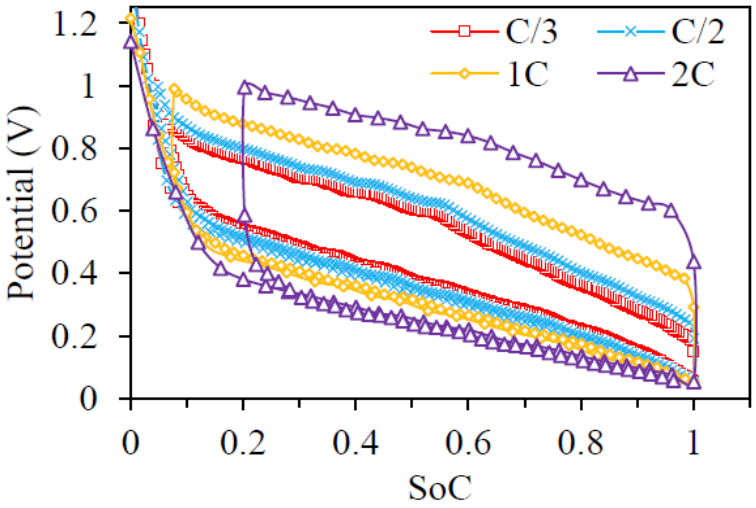


Fig. 18. The simulated cycling curves of the Si anode half-cells with respect to SoC under different CC lithiation C-rates. The scatters are experimental results for comparison.

the yielding strength sooner. Then, when Si reaches the yield strength of 1.5 GPa, the stress will no longer evolve with the volume shrinkage process due to the assumed perfect plasticity of Si material. Afterwards, at the beginning of lithiation, Si deforms elastically again, where Young's modulus of Si is relatively high so that the slopes of the stress curves are large. Finally, when reaching -1.5 GPa, Si deforms with perfect plasticity and its stress remain constant. The overall deformation of Si material after one full lithiation-delithiation cycle is 0, meaning the lithium residue in Si is neglectable (< 2%). From the above results, we can see that, on one hand, C-rate is found to have no significant impact on the stress level of the Si anode and the trends of stress propagation are similar; this is because the Si anode has a uniform lithium concentration and homogeneous deformation upon cycling due to the short lithium diffusion path along the thin film and the relatively high lithium diffusivity. On the other hand, Si bears great plastic flow during cycling, resulting in the huge irreversible mechanical energy dissipation. Therefore, it is essential to further evaluate the mechanical energy dissipation and to figure out possible mitigation approaches.

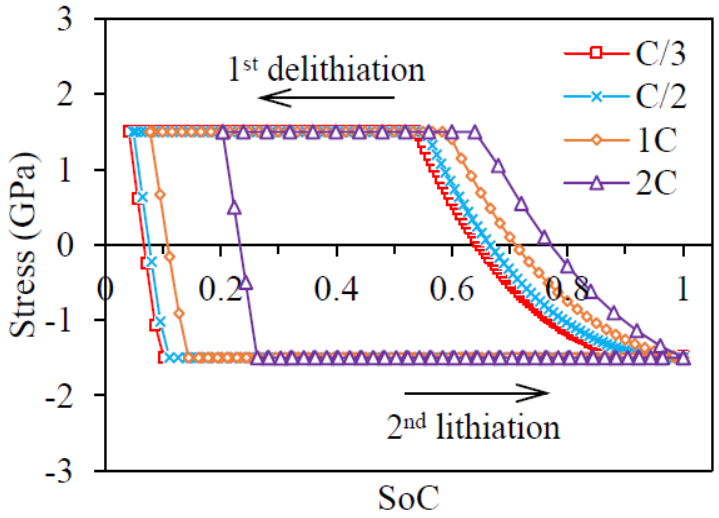


Fig. 19. The simulated stress evolutions of the Si anodes as a function of SoC with various Crates.

On the basis of previous results, the overall energy dissipation, along with the energy losses from various sources, e.g., mechanical energy, joule heating and polarization loss, can be obtained. **Table 2** and **Fig. 20** summarize the energy dissipation of the 250 nm thick Si film anode with different C-rates, where the simulation results are compared with experimental measurements. The D and L in the horizontal axis of **Fig. 20** denote the delithiation and lithiation processes, respectively. The experimental data are based on five independent measurements and the error bars are labelled to show the deviations. Note that, the simulated energy values are based on the modeling RVE with the size of 1000 nm (l) × 1000 nm (w); therefore, to have a fair comparison, these values are normalized depending on the theoretical capacities of the practical LIB cells. It can be observed from the results that, firstly, the developed FE model can rather accurately predict the overall energy dissipation behaviors of the Si anode upon delithiation and lithiation, where the average prediction error is lower

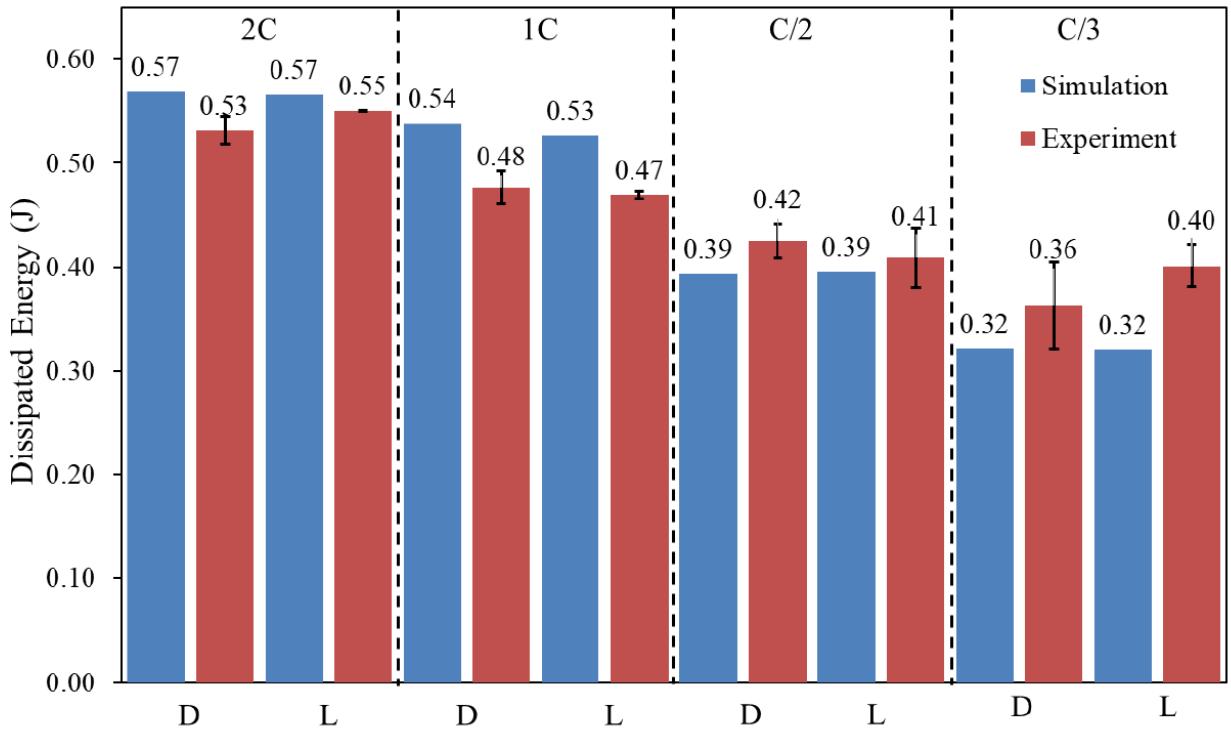


Fig. 20. Comparison of the simulation results and experimental measurements of the total energy dissipation of the Si anode during delithiation and lithiation processes with different Crates. D and L in the x axis denote the delithiation and lithiation periods, respectively. The simulation results are normalized depending on the theoretical capacities of the assembled LIB cells.

than 9%, demonstrating the model can serve as a powerful tool to capture the Multiphysics phenomena of the LIB electrode materials and to explore the underlying mechanisms. Later in the study, the model has been further employed to investigate the influences of other critical battery design and operation variables. Secondly, the energy dissipation during delithiation is found to be comparable with that during lithiation. This is because, as listed in **Table 2**, the polarization losses, Wp, which are the dominating factor to the energy dissipation, are equal for the lithiation and delithiation processes, as mentioned in the method section. Similarly, the calculated Wh and Wm between lithiation and delithiation show the same magnitude, as well. More importantly, the energy dissipation is highly related with the C-rate. It can be observed that, the polarization-effect-induced energy loss Wp is largely exaggerated by the high lithiation current and is almost on the same level as or even greater than the available electrochemical energy, Wec. This implies nearly half of the energy that has been infused into the Si anode upon lithiation will be wasted by polarization at last; there is a large room for the improvement of the Si anode design. In addition, the energy loss directly attributed to joule heating, Wh, is nearly linearly increasing with the increase of lithiation C-rate; nevertheless, since the applied operating powers on the thin film anodes are generally low, Wh is actually small and neglectable compared to other sources. On the contrary, Wm is generally not much influenced by C-rate, where the slightly reduced Wm at higher C-rate is caused by the smaller cycling SoC window, as shown in **Fig. 20**. The lithium is uniformly distributed along the Si thin film because of the fast lithium diffusivity and short lithiation path, so that the stress in the film is uniform and barely influenced by the lithiation rate. Moreover, the plastic deformation of the Si film is solely driven by the lithiation process; even though the plastic strain rate is changing with the lithiation C-rate, the overall plastic strain, as well as the integral of strain rate over time, will be the same since

the cutoff voltage bounds keep unchanged at different C-rates. As a result, the Wm is calculated to be almost a constant. Last but definitely not least, the resulting Wec, especially during lithiation, is rather sensitive to the applied current and has an inverse linear correlation with C-rate: increasing lithiation rate could result in a significant reduction of the available electrochemical energy, e.g., Wec at 2C is only half of that at 1C. This means that for the LIBs with Si based anodes, the amount of energy that can eventually be released during battery discharging will be strictly limited by their practical operation conditions; better Si anode design considering the large energy dissipation phenomena needs to be explored.

Table 2. Summary of the simulated and experimentally measured energy dissipation of the 250 nm Si thin film from various sources

		W_{ec} (J)	W_h (J)	W_m (J)	W_p (J)	W_{tot} [1] (J)	W_{dis} [2] (J)	*Normalized* W_{dis} (J)	W_{dis} *from exp.* (J)
2C	Delithiation	5.85E-09	6.63E-13	3.25E-10	1.96E-09	3.67E-09	2.17E-09	0.59	0.57
	Lithiation	1.51E-09	6.33E-13	3.32E-10	1.96E-09	3.67E-09	2.16E-09	0.59	0.55
1C	Delithiation	6.93E-09	4.60E-13	3.33E-10	1.72E-09	4.87E-09	2.06E-09	0.56	0.48
	Lithiation	2.86E-09	4.46E-13	3.36E-10	1.72E-09	4.87E-09	2.01E-09	0.55	0.50
C/2	Delithiation	6.70E-09	2.55E-13	3.40E-10	1.16E-09	5.2E-09	1.5E-09	0.41	0.42
	Lithiation	3.69E-09	2.46E-13	3.46E-10	1.16E-09	5.2E-09	1.51E-09	0.41	0.45
C/3	Delithiation	6.51E-09	1.76E-13	3.43E-10	8.84E-10	5.28E-09	1.23E-09	0.33	0.42
	Lithiation	4.05E-09	1.68E-13	3.42E-10	8.84E-10	5.28E-09	1.23E-09	0.33	0.41

[1] W_{tot} denotes the total stored energy in the anode, where $W_{tot} = W_{ec} - W_h - W_m - W_p$ during delithiation, and $W_{tot} = W_{ec} + W_h + W_m + W_p$ during lithiation, according to Eq. (11-12).

[2] $W_{dis} = W_h + W_m + W_p$ denotes then overall energy dissipation, which is then normalized based on the theoretical capacities of the LIB cells for comparison.

Furthermore, the influences of the depth of lithiation, i.e., cutoff potential window, are explored. Table 3 lists the details of the energy terms from various sources with the changed lower bounds from 50 to 150 mV. The Si anodes are 250 nm thick and cycled at 1C rate, where the upper bound is fixed at 1 V. Similar to the effects of Si layer thickness, although narrowing the cycling window may cause a slight reduction of the available Wec, it could effectively promote the energy efficiency of the Si anode, where its energy efficiency and depth of lithiation are linearly correlated. Compared to the 50 mV scenario, by lifting the lower bound to 150 mV, the energy efficiency is increased by 1.2 times while the available energy is decreased by 26.6%. Additionally, both Wm and Wp show inverse linear relations with the lower bound value, meanwhile the fraction of Wm still keeps almost as a constant. However, the underlying mechanisms for the reduction of the two energies are slightly different. For Wm, it is rooted by the fact that the plastic deformation of the Si film is largely limited by narrowing the voltage bound; whereas since Wp is the integral of polarization effect over time, although the applied lithiation current and the magnitude of the resulting polarization effect are the same, the total lithiation time is obviously decreased, resulting in the weakened Wp. After all, combining above two terms, Wdis becomes smaller as the depth of lithiation is higher. This demonstrates that, depending on the requirements of the specific applications, the trade-off between energy efficiency and practical available energy can be effectively addressed through adjusting the depth of lithiation.

Table 3. Summary of the energy dissipation of the Si thin film anodes with changed depth of lithiation

		W_{ec} (J)	W_h (J)	W_m (J)	W_p (J)	W_{tot} (J)	W_{dis} (J)
50 mV	Delithiation	6.93E-09	4.60E-13	3.33E-10	1.72E-09	4.87E-09	2.06E-09
	Lithiation	2.86E-09	4.46E-13	2.86E-10	1.72E-09	4.87E-09	2.01E-09
100 mV	Delithiation	5.38E-09	3.36E-13	2.63E-10	1.16E-09	3.96E-09	1.39E-09
	Lithiation	2.57E-09	3.36E-13	2.30E-10	1.16E-09	3.96E-09	1.42E-09
150 mV	Delithiation	3.98E-09	2.33E-13	1.76E-10	7.79E-10	3.02E-09	9.55E-10
	Lithiation	2.10E-09	2.33E-13	1.39E-10	7.79E-10	3.02E-09	9.18E-10

Subproject 3: SSAT-Optimized Battery Thermal and Power Management System

An important step towards engineering a SSAT-optimized battery thermal and power management system is developing a deep understanding of the performance of the SSA's under different charge, discharge, and thermal conditions. The team has implemented accelerated life testing of its SSAT batteries with an aim to reveal product failure modes in a matter of days or weeks, as compared to what could take months or years with traditional testing. It is desired to obtain enough failure data at high stress levels to accurately project reliability at normal use stress conditions based on an acceleration model developed by UIUC. To this end, the team developed and implemented a test plan for ALT that consisted of the following: 1. Three key stressors that accelerate the failure mechanism under investigation (**Table 4**): charging rate, temperature, and depth of discharge. Each combination of stressor levels constitutes a different "stress cell." 2. Verification that the stress levels used were not too high (e.g., temperature elevated beyond 60 °C introduces additional failure modes which are not of interest). 3. Randomization of the nuisance factors associated with each SSA (e.g., variation in active loading, first cycle efficiency, etc.) via a random selection of samples in each stress cell.

Following these established guidelines has led to the solidification of stressor levels for this project, as outlined in **Table 5**. Notably, the team has switched from half-cell testing to full-cell testing which has altered the depth of discharge criterion by modifying the full-cell voltage window instead of changing the lithiation cut-off voltage in half-cell. Moreover, the high and low levels for the temperature stressor have been changed to 55 °C and 5 °C. This is to avoid the unwanted decomposition of LiPF6-based electrolyte at elevated temperature (i.e., an additional failure mode), and to offer an alternative mode to SSA failure at low temperature via restricted mass transport and kinetics.

Table 4. Summary of different failure types for Si anode. Stressors under investigation are bolded.

Anode Failure Type		Failure Feature
Internal Factor	Pulverization	Irreversible SEI growth & therefore Li consumption
	Structural deformation	Volume change, fracture, delamination/electrical isolation
	Dendrite growth	Li plating/separator puncture/cell shorting
	Li-ion trapping	Li trapped in defect sites (manifested as capacity loss)
External Factor	**Temperature**	**Side reactions & dense SEI growth (high temp.); restricted mass transport, poor SEI re-growth, Li-ion trapping (low temp.)**
	Ageing	Current collector corrosion & other physical/chemical damages
	Depth of discharge (DOD)	**Pulverization and structural deformation**
	Charge/discharge rate	**Structural deformation**
	Pressure	Restricted volume change, particle cracking

Table 5. Stress factors and their respective levels for accelerated life testing.

			Level		
		Control	**0**	**1**	**2**
Factor A	Rate	C/3	C/2	1C	2C
Factor B	Temperature	20 °C	5 °C	45 °C	55 °C
Factor C	Volt. Window	2.80 - 4.15	2.80 - 4.00	2.50 - 4.10	4.25 - 2.25

The accelerated life testing protocol for SSA has been effectively implemented based on the above guidelines. Fig. 21 displays both the experimental design table of treatments and a selected data set from stress cells commonly exposed to 55 °C, but to different charge rates and depth of discharge. Each stress cell (with at least one replicate) exhibited a linear trend in capacity fade before reaching end-of-life (EOL), which is designated as the cycle number at which the cell capacity falls below 80% of its initial capacity. This linear fading trend is a good indicator that an acceleration model will be readily applied to the data set without any confounding parameters. Further EOL assessment is planned to verify the failure mechanism of each stress cell, in addition to completing ALT of the remaining stress cells.

a)

The 3^3 Design - Table of Treatments				
		Factor A		
Factor B	Factor C	0	1	2
0	0	000	100	200
0	1	001	101	201
0	2	002	102	202
1	0	010	110	210
1	1	011	111	211
1	2	012	112	212
2	0	020	120	220
2	1	021	121	221
2	2	022	122	222

b)

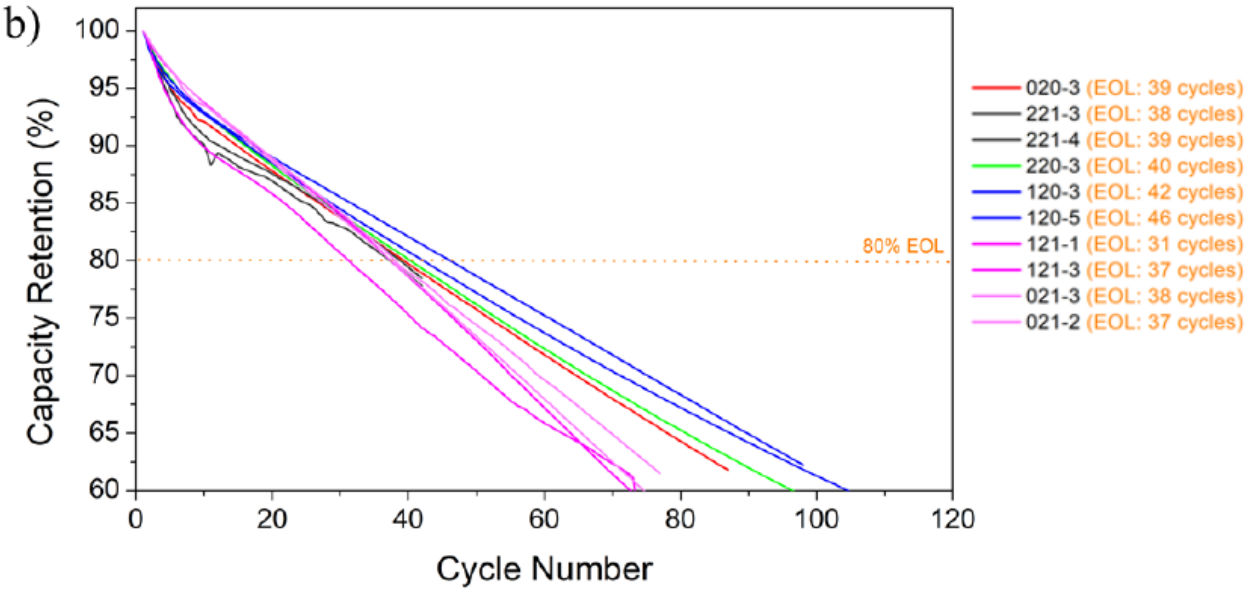
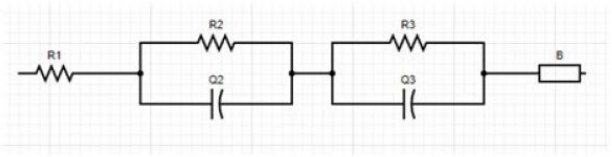


Fig. 21. The 3^3 full-factorial design table of treatments (a). The first set of accelerated life testing data collected using the updated stressor factors in Table 5 (b).

To address pouch-scale performance and management of the SSAT, Xerion Advanced Battery Corporation (XABC) leveraged the information gained from accelerated life testing, performed in Periods 1 and 2, to update the design space for critical parameters as outlined in **Table 2**. Experimental results gathered thus far suggest reliable operation can be achieved through (i) elevated temperature (ca. 45 °C) formation over 3-5 cycles and (ii) limiting silicon thickness to ca. 100 nm within a (iii) 1-2 μm pore regime. Having also optimized cell parameters to reliably test single-layer pouch (SLP) test articles, XABC expects to produce 5-10 SLPs for demonstration purposes by the end of Period 3. Toward making full use of the accelerated life testing data, XABC also developed an equivalent circuit model to correlate failure modes and aging mechanisms with applied stressors (**Fig. 15**). The data suggest that the SSAT was mass transport limited, hence the modification to silicon layer thickness in **Table 2**. It was also apparent from these analyses that NMC was limiting the rate performance of full-cells.

Table 6. Design space outlining parameters found critical to SSAT performance.

Symbol	Physical Meaning	Starting Range (options)	Optimized Range (options)
T	Cell construction parameter	Coin, pouch, prismatic, spiral	Coin and single-layer pouch
t	Silicon layer thickness	10-250 nm	Under optimization
V	Silicon electrodeposition voltage	~1.6 V vs. Ag/Ag^+	Switched to electrodeposition current: - 1 mA/cm^2
P	Conductive support characteristic dimension	0.5 – 2.0 μm	1.5 – 2.0 μm
ff	Conductive Support Filling Fraction	5-20%	17-18%
F	Formation Cycles	1-10	Under optimization
E	Electrolyte Additives	FEC, VC, PS, SN	FEC, PS
C	Cathode Selection	LMO, NCA, NMC, LCO	LCO, LFP



R (Ω)	Ageing Mechanism	Root Cause(s)
R_i	Particle uniformity/ consistency, contact loss, Conductivity Loss	• Increasing anode resistance with cycling • Dendrite formation • Contact loss between cell components • Electrical conductivity of bulk Silicon
R_1 and R_2	Loss of Lithium, and SEI depletion	• SEI formation and build-up • SEI decomposition and precipitation • Particle cracking, pore clogging & particle disconnection
B/M/W and R_3	Slowing down of lithium ion (de)insertion kinetics, random mass diffusion into scaffold (rather than 1-D, 2-D, or 3-D)	• Solvent co-intercalation (& resulting side reactions) – manifests as negative resistance and capacitance • Transition metal dissolution & dendrite formation • Structural disordering within scaffold

Fig. 22. Relationship between equivalent circuit model and ageing mechanisms for SSAT.

Publications

This project resulted in 13 publications[1-13] with several additional publications anticipated.

1. Zheng, Z. Y.; Chen, B.; Fritz, N.; Gurumukhi, Y.; Cook, J.; Ates, M. N.; Miljkovic, N.; Braun, P. V.; Wang, P. F., Lithiation Induced Stress Concentration for 3D Metal Scaffold Structured Silicon Anodes. *Journal of the Electrochemical Society* **2019,** *166* (10), A2083-A2090.
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4. Zheng, Z. Y.; Chen, B.; Fritz, N.; Gurumukhi, Y.; Cook, J.; Ates, M. N.; Miljkovic, N.; Braun, P. V.; Wang, P. F., The Impact of Non-uniform Metal Scaffolds on the Performance of 3D Structured Silicon Anodes. *Journal of Energy Storage* **2020,** *30*.
5. Ham, Y.; Fritz, N. J.; Hyun, G.; Lee, Y. B.; Nam, J. S.; Kim, I. D.; Braun, P. V.; Jeon, S., 3D periodic polyimide nano-networks for ultrahigh-rate and sustainable energy storage. *Energy & Environmental Science* **2021,** *14* (11), 5894-5902.
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8. Zheng, Z. Y.; Liu, Z.; Wang, P. F.; Li, Y. M., Numerical modeling on the delamination-induced capacity degradation of silicon anode. *Journal of Energy Storage* **2021,** *43*.
9. Zheng, Z. Y.; Xu, Y. W.; Wang, P. F., Uncertainty Quantification Analysis on Mechanical Properties of the Structured Silicon Anode via Surrogate Models. *Journal of the Electrochemical Society* **2021,** *168* (4).
10. Kohtz, S.; Xu, Y. W.; Zheng, Z. Y.; Wang, P. F., Physics-informed machine learning model for battery state of health prognostics using partial charging segments. *Mechanical Systems and Signal Processing* **2022,** *172*.
11. Ma, J. C.; Zheng, Z. Y.; Hoque, M. J.; Li, L. N.; Rabbi, K. F.; Ho, J. Y.; Braun, P. V.; Wang, P. F.; Miljkovic, N., A Lipid-Inspired Highly Adhesive Interface for Durable Superhydrophobicity in Wet Environments and Stable Jumping Droplet Condensation. *Acs Nano* **2022,** *16* (3), 4251-4262.
12. Rabbi, K. F.; Ho, J. Y.; Yan, X.; Ma, J. C.; Hoque, M. J.; Sett, S.; Miljkovic, N., Polydimethylsiloxane-Silane Synergy enables Dropwise Condensation of Low Surface Tension Liquids. *Advanced Functional Materials* **2022,** *32* (19).
13. Zheng, Z. Y.; Wang, P. F., Uncertainty Quantification Analysis on Silicon Electrodeposition Process Via Numerical Simulation Methods. *Asce-Asme Journal of Risk and Uncertainty in Engineering Systems Part B-Mechanical Engineering* **2022,** *8* (1).