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DESIGN AND IMPLEMENTATION OF A DATA ACQUISITION SYSTEM WITH IN-SITU PICOAMMETER FOR AUTOMATED RELIABILITY TESTING

by

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March 2023

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In recent years, the military has been exploring the use of wide bandgap semiconductors (WBGS) such as gallium nitride (GaN) and silicon carbide (SiC) due to their promising material properties, as compared to silicon (Si). Understanding the reliability of these high-performance WBGS devices is paramount to their implementation in military systems. However, it remains to be tested because good-quality reliability data is needed, but it is difficult and expensive to produce. This thesis looks at the design and implementation of a modular reliability testing subsystem in the form of a novel data acquisition system. First, a system was designed to perform automated, in-situ leakage current measurements of up to four devices under test (DUT) with sub-nA resolution. Next, a wide sample of devices consisting of a resistor, two Zener diodes, a power diode, two GaN diodes, and a field effect transistor (FET) were subjected to various voltage sweep and reverse-bias tests that were recorded by the system. Finally, the results of those validation tests were processed and analyzed. The system achieved leakage current resolutions below 100 pA, demonstrating its ability to measure various devices.

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DESIGN AND IMPLEMENTATION OF A DATA ACQUISITION SYSTEM WITH IN-SITU PICOAMMETER FOR AUTOMATED RELIABILITY TESTING

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In recent years, the military has been exploring the use of wide bandgap semiconductors (WBGS) such as gallium nitride (GaN) and silicon carbide (SiC) due to their promising material properties, as compared to silicon (Si). Understanding the reliability of these high-performance WBGS devices is paramount to their implementation in military systems. However, it remains to be tested because good-quality reliability data is needed, but it is difficult and expensive to produce. This thesis looks at the design and implementation of a modular reliability testing subsystem in the form of a novel data acquisition system. First, a system was designed to perform automated, in-situ leakage current measurements of up to four devices under test (DUT) with sub-nA resolution. Next, a wide sample of devices consisting of a resistor, two Zener diodes, a power diode, two GaN diodes, and a field effect transistor (FET) were subjected to various voltage sweep and reverse-bias tests that were recorded by the system. Finally, the results of those validation tests were processed and analyzed. The system achieved leakage current resolutions below 100 pA, demonstrating its ability to measure various devices.

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LIST OF ACRONYMS AND ABBREVIATIONS

AI	artificial intelligence
BFOM	Baliga Figure of Merit
DAQ	data acquisition
dc	direct current
DIP	dual in-line package
DUT	device under test
EDA	electronic design automation
EMI	electromagnetic interference
EMP	electromagnetic pulse
FET	field effect transistor
GaN	gallium nitride
HTOL	high temperature operating life
HTRB	high temperature reverse bias
HV	high voltage
IDE	integrated development environment
IO	input-output
I-V	current-voltage
I-V-T	current, voltage, temperature
I^2C	Inter-Integrated Circuit
JFET	junction field effect transistor
JLTV	Joint Light Tactical Vehicle
LMB	leakage measurement board
LoSPRaDC	Low Side Picoammeter for Reliability and Device Characterization
LPF	low-pass filter
LSB	least significant bit
MFB	multi feedback
MOSFET	metal oxide semiconductor field effect transistor

MPSMU	medium power source measurement unit
NBW	noise bandwidth
NPLC	number of power-line-cycles
PCB	printed circuit board
PDF	probability density function
PSD	power spectral density
PTFE	polytetrafluoroethylene
Re/GaN	Rhenium/GaN
RMS	root-mean-square
RTOS	real-time operating system
Si	silicon
SiC	silicon carbide
SIGINT	signals intelligence
SMS	stress-measure-stress
SMT	surface mount
SOIC-8	small outline integrated circuit 8-pin
SPI	serial port interface
SPS	samples per second
TIA	transimpedance amplifier
USMC	United States Marine Corps
USNA	United States Naval Academy
USB	universal serial bus
UPS	uninterrupted power supply
VI	virtual instrument
WBGS	Wide Bandgap Semiconductor

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I. INTRODUCTION

A. MOTIVATION

The United States Marine Corps (USMC) is currently navigating through a large-scale institutional modernization. At the forefront of this modernization is the adoption and implementation of multiple advanced electronic technologies, from AI (artificial intelligence) at the edge, capable of rapidly processing collected signals intelligence (SIGINT) on the front lines, to autonomous Joint-Light Tactical Vehicles (JLTV) equipped with area-denial weapon systems, shown in Figure 1 [1]. While the USMC seeks to adopt state-of-the-art electronic systems, these systems must be able to meet the harsh and demanding expeditionary requirements inherent to the mission of the USMC. When designing these advanced electronic systems that will support distributed operations in a contested maritime environment, particular care must be taken to optimize their performance against their energy efficiency and size.

Figure 1. Navy Marine Expeditionary Ship Interdiction System Source: [2].

The greatest challenge to the implementation of these advanced systems are limited power resources; these resource limitations are created by existing power generation equipment, bulky power electronic distribution systems, and low energy density storage technology [3]. These systems all share one thing in common, they are beholden to the limitations of their primary semiconductor material, silicon (Si). These systems based on Si semiconductor power devices have simply reached the upper thresholds of performance and efficiency per unit area, as governed by the nature of their intrinsic material properties with respect to the modern demands of electronic systems [4]. Therefore, more research into new power semiconductor materials is needed to overcome these limitations.

In recent years, the military has been exploring the use of wide bandgap semiconductors (WBGS) such as gallium nitride (GaN) and silicon carbide (SiC) in power electronic devices due to their promising material properties, as compared to Si, as shown in Figure 2 [5]. GaN and SiC offer several advantages over Si for power applications, such as higher temperature operation thresholds, which allows for the design of electronic devices with smaller form factors; higher critical electric field and electron mobility, which allows for greater current densities and increased protection against electromagnetic pulse (EMP) events; resistance to radiation effects, which limits the durability of traditional Si devices in space; and higher frequency operation, which improves the performance of radar systems [6], [7].

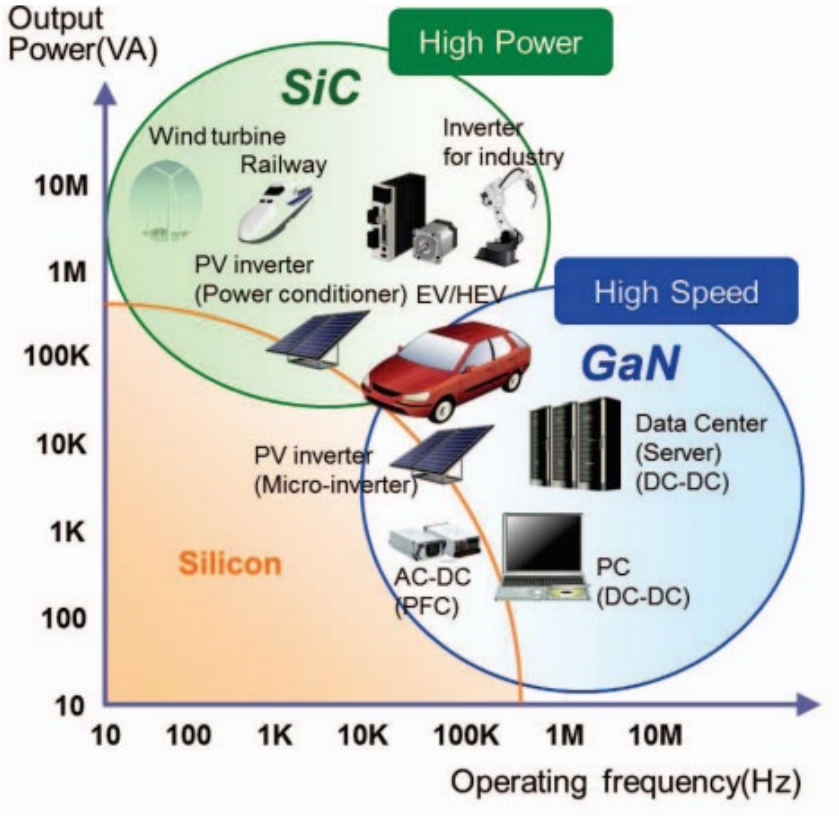

Figure 2. Applications of GaN and SiC vs. Si. Source: [8].

Given these improved performance characteristics, WBGS are one of the most promising technologies for next generation solid-state power devices. This research directly pushes the USMC closer to meeting its expeditionary requirements for advanced electronic systems capable of higher performance while becoming more physically compact, energy efficient, and reliable. While determining the physical dimensionality and energy efficiency of a system is relatively simple, determining the reliability of WBGS devices is not. Understanding the reliability of these high performance WBGS devices is paramount to their implementation in military systems but remains untested because good quality reliability data is needed, but it is difficult and expensive to produce. To understand device reliability, systems capable of accurately measuring device characteristics are needed.

B. PROBLEM STATEMENT AND RESEARCH OBJECTIVES

A modular and affordable system capable of automatically measuring, and constantly monitoring, the amount of leakage current generated by multiple devices-under-test (DUTs) while they are being electrically stressed in parallel during reliability tests is needed for ongoing testing of the reliability of WBGS at the Naval Postgraduate School (NPS). Historically, semiconductor reliability testing at NPS has been done primarily using the high temperature operating life (HTOL) method; there is a distinct need at NPS for a low-cost system to perform automated high temperature reverse bias (HTRB) testing.

HTOL is a semiconductor reliability testing method during which a DUT is subjected to operation at a constant current over a fixed interval of time while also being held at a fixed temperature. Such a test can be automated via a stress-measure-stress (SMS) modification: between each measurement period, the current, voltage, and temperature (I-V-T) characteristics of the device are recorded to identify changes, which are indicative of potential failure mechanisms. HTRB is like HTOL, except that it holds a device at a fixed voltage over a fixed time interval to evaluate time-dependent breakdown characteristics. With previous prototype HTRB systems developed at NPS, DUTs could only be characterized between stress cycles; DUT leakage currents during stressing could not be adequately monitored. The lack of this capability resulted in the destruction of numerous DUTs during electrical stress cycles due to the inability of the system to monitor leakage currents and disconnect DUTs which were approaching nominal failure conditions. As such, researchers were not able to conduct deterministic failure analysis on these devices.

This thesis examines the research, development, and implementation of a novel in-situ low-side automatic leakage current measurement system capable of picoampere-resolution, from 1 nA to 400 μA, that can be integrated with high voltage (HV) HTRB reliability tests. This system, referred to as the Low Side Picoammeter for Reliability and Device Characterization (LoSPRaDC), is specifically designed to be implemented as a sub-system within an upgraded SMS system for a future combined HTRB/HTOL system design. This upgraded system is being designed to support HV HTRB testing up to 5 kV and high current HTOL testing up to 30 A. Ultimately, the overall system is intended to be used by various students, such as those at NPS and the United States Naval Academy

(USNA), and researchers, such as those at the Naval Research Lab (NRL), for reliability research and testing of high-power and WBGS devices.

After developing the LoSPRaDC, the performance of the system was examined through the extraction of measurement data for the leakage current and voltage (I-V) characterization of several example DUTs. This was done by comparing the leakage current data produced by the LoSPRaDC against the data extracted from the Keysight B1505A Power Device Analyzer / Curve Tracer medium power source measurement unit (MPSMU) module used to electrically stress a selection of DUTs. The DUTs used to perform this validation testing consist of one Re/GaN diode manufactured at Pennsylvania State University, as well as commercially available devices such as one vertical GaN PN diode, two Si Zener diodes, one Si power diode, one resistor, and one field-effect transistor (FET).

C. RELATED WORK

In 2019, Clemmer conducted a reliability study on Pd-GaN diodes using the original SMS HTOL system at NPS [9]. His research showed the ability of an HTOL system to collect in-situ I-V-T measurements during the period between electrical stress tests. This study recommended updates to the HTOL system for conducting better reliability tests and minimizing noise in the data [9].

In 2021, O'Neal conducted reliability study using a student developed HTOL/ HTRB system at NPS [10]. During his research, he tested Pd-GaN devices under HTOL and HTRB conditions. His research showed that such an adaptable and modular testing system was relatively simple to implement which made it ideal for educational institutions to perform reliability research using a cost-effective system. In his paper, he also spoke about future work related to the need for testing three-terminal devices [10].

In 2022, Kavanaugh upgraded the existing HTOL system by increasing the magnitude of current and temperature stress that could be generated by the system [11]. He also implemented a spectrometer to measure the electroluminescence of the DUT. His research showed that electroluminescence spectral analysis could be used to monitor the health of direct bandgap semiconductors over time [11].

D. THESIS ORGANIZATION

This thesis is organized as follows. Chapter II provides background information on WBGS and operational amplifier (op-amp) theory, including the implementation of reverse-feedback current amplifiers designed using a transimpedance amplifier configuration and the benefits of this current sensing method over a shunt resistor. Specifically, TIA stability considerations and the effects of various noise interference is presented. In Chapter III, the system design of LoSPRaDC along with the system testing and validation methodologies is covered. In Chapter IV, the system testing and validation testing results are presented. Finally, Chapter V presents the conclusions of the validation testing, along with recommendations on future work relating to the overall testing system

II. BACKGROUND

This chapter discusses the motivation and background necessary to understand the design and operation of the LoSPRaDC system developed in this thesis. This chapter first motivates the need for a picoampere-capable measurement system in WBGS device reliability testing by discussing the properties of WBGS materials. Then, an introduction to op-amps provides the background needed to understand the effects of noise and stability in an amplifier designed to measure the low leakage currents generated by WBGS devices.

A. MATERIAL PROPERTIES OF WBGS

Si has remained dominant as the material of choice for the power semiconductor industry due to its abundant availability, low-cost, and relative ease of manufacturing into substrates for integrated circuits (IC); however, its intrinsic material properties limit its performance in high-speed power switching devices, HV protection, and high temperature applications [12]. This is mostly due to the tradeoff that exists between breakdown voltage and on-state resistance, limiting the minimum charge per unit cross-sectional area, or current density, that Si can withstand [13]. Because of the intrinsic material properties of WBGS, higher electron mobility and lower on-state resistance, they are the materials of choice to replace Si for high-frequency and high-power applications, such as power electronics, radar, and solid-state lighting.

GaN and SiC are classified as WBGS because they have an energy gap between their valence and conduction bands, or bandgap, that is greater than 2.2 eV [9]. A comparison of the material properties of GaN and SiC to Si is shown in Table 1.

Table 1. Material and Electrical Properties of Semiconductors. Source: [14].

Parameter	Symbol	Unit	Si	SiC	GaN
Bandgap	E_c	eV	1.12	3.2	3.43
Relative Dielectric Constant	ϵ_s	-	11.9	10	9.5
Electron Mobility	μ_n	$cm^2/(V.s)$	1500	700	2000
Peak Electron Velocity	v_{peak}	$10^7 \cdot cm/s$	1	2	2.5
Critical Electric Field	E_c	MV/cm	0.3	3.0	3.3
Baliga Figure of Merit	$\epsilon_s \mu_n E_c^2$	W/cm^2	1	392*	1416*
* Normalized to Si					

1. Baliga's Figure of Merit

Baliga's Figure of Merit (BFOM) is a widely accepted metric used to compare the suitability of a semiconductor material for use in power device applications through the examination of materials by their potential for minimizing on-state loss in a power semiconductor device design. It comes from the denominator of (1), which is used to determine the specific on-state resistance of the ideal drift region ($R_{on,sp}$) based on the breakdown voltage (V_{br}), dielectric constant (ε_s), electron mobility (μ_n), and critical field strength (E_{crit}) of the given material [12], [15].

$$R_{on,\,sp} = \frac{4V_{br}^2}{\varepsilon_s \mu_n E^3_{\,crit}} \tag{1}$$

The BFOM, defined in (2), defines the material parameters which minimize the $R_{on,sp}$ of a power semiconductor drift layer for a desired V_{br}. Figure 3 provides an example of the BFOM limits for Si, GaN, and SiC, which demonstrate an improvement of over four orders of magnitude offered by the utilization of GaN over Si for power applications.

$$BFOM = \varepsilon_s \mu_n E^3_{\,crit} \tag{2}$$

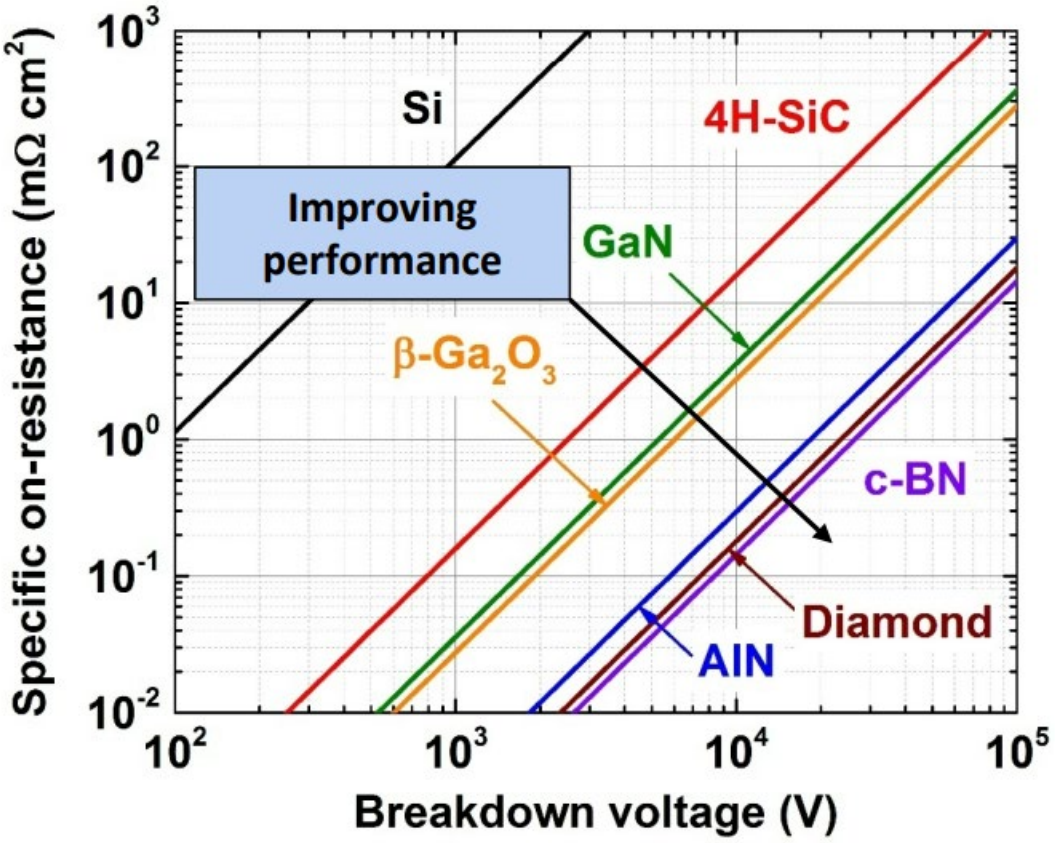

Figure 3. $R_{on,sp}$ vs. V_{br} of Other Materials. Source: [3].

2. PN Diode Leakage Current

Another material property that must be discussed takes place at the PN junction formed between p-type and n-type semiconductors. This interface between acceptor and donor doped semiconductors forms a barrier potential caused by the change of Fermi levels between each material in an area known as the depletion region. This depletion region grows under reverse-bias and limits current flow. The I-V function for an ideal diode is shown in (3), where I_D is the diode current, I_s is the saturation current, q is the elementary charge, V is the potential across the device, k is the Boltzmann constant, and T is the temperature in degrees Kelvin.

$$I_D = I_S(e^{qV/kT} - 1) \tag{3}$$

When a p^+-n device is reverse biased, the ideal saturation current is represented by (4), where A is the area of the device, n_i is the intrinsic carrier concentration, N_D is the donor concentration, D_P is hole diffusion coefficient, and τ is the carrier lifetime [16].

$$I_S = -qAn_i^2\left(\frac{1}{N_D}\right)\sqrt{\frac{D_P}{\tau}} \tag{4}$$

The intrinsic carrier concentration is defined in (5), where N_C and N_V are the density of states in the conduction and valence bands. The intrinsic carrier concentration is exponentially related to the bandgap energy; therefore, it can be concluded that a larger bandgap, as found in WBGS, is directly correlated to an exponentially low intrinsic carrier concentration [16].

$$n_i = \sqrt{N_C N_V}\cdot e^{-(E_g/2kT)} \tag{5}$$

The further reduction of this already small intrinsic carrier concentration to the reverse saturation current, shown in (4), is what explains the low leakage currents characteristic of WBGS devices based on PN junctions. These low reverse leakage current values are what motivates the need for picoampere-capable measurements during the HTRB reliability testing of WBGS devices.

B. OPERATIONAL AMPLIFIERS

An op-amp is a type of electronic amplifier that is widely used in a variety of circuit applications, including amplifiers, filters, oscillators, and comparators. Op-amps are designed to have a high gain and a high input impedance, making them ideal for amplifying small signals from sensors or other sources. They typically have two input terminals, labeled as the inverting input and the non-inverting input, two power supply input terminals, labeled as the positive and negative power supplies, and a single output terminal. These are commonly presented as shown in Figure 4.

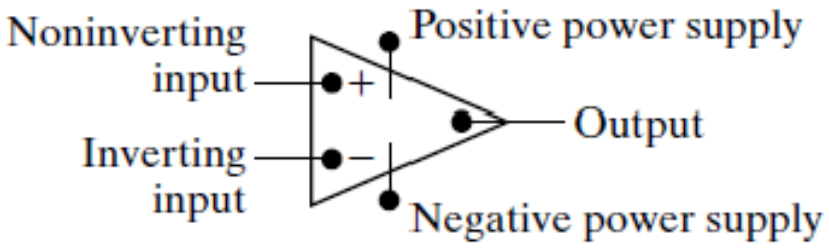

Figure 4. Circuit Symbol for an Op-amp. Source: [17].

The output voltage of the op-amp is proportional to the difference in voltage between its two inputs, this output can be positive or negative. This relationship is defined in (6), where V_{out} is the output voltage, V^+ is the non-inverting input voltage, V^- is the inverting input voltage, and A_{ol} is the open-loop gain.

$$V_{out} = A_{ol}(V^+ - V^-) \tag{6}$$

Ideal op-amps have infinite gain and bandwidth, meaning they can amplify signals of any frequency with the same amount of gain; however, op-amps are almost never used in the open-loop configuration. This is because the limit of the gain of an op-amps is determined by the saturation range set by the positive and negative power supplies to the circuit, which limits the maximum signal which can be applied between V+ and V-. To mitigate this, op-amps are almost always implemented with a feedback mechanism, referred to as a closed-loop configuration, which is either positive or negative [18].

1. Ideal Closed-Loop Gain (Inverting and Non-inverting)

When a connection is made between either of the input terminals and the output terminal of an op-amp, it is said to be configured in a closed-loop configuration. Figure 5 shows a resistor, R_2, connected from the output terminal to the inverting terminal; thus, this op-amp is said to be in an inverting configuration.

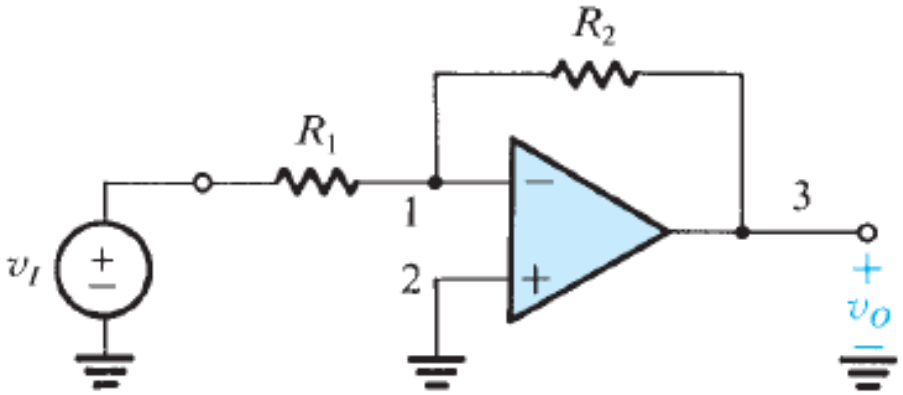

Figure 5. Inverting Closed-Loop Configuration. Source: [18].

Since the non-inverting terminal is tied to ground, it will have a value very close to zero. This op-amp has a voltage source connected to its non-inverting terminal across a resistor, but because an op-amp will output the difference between its input terminals, the voltage at the non-inverting terminal will also be essentially zero. This results from the op-amp producing a negative output that will feedback to the non-inverting terminal to equalize it with the value of the inverting terminal; the mechanism of this action is referred to as a virtual short, or virtual ground, as in Figure 5, because an op-amp with negative feedback will always drive the potential between its input terminals to zero. The closed-loop gain, G, output voltage, V_{out}, and input impedance, Z_{in}, of this configuration are defined in (7), (8), and (9).

$$G = Gain = \frac{V_{out}}{V_{in}} \tag{7}$$

$$V_{out} = -V_{in}\left(\frac{R_2}{R_1}\right) \rightarrow \frac{V_{out}}{V_{in}} = -\left(\frac{R_2}{R_1}\right) \tag{8}$$

$$Z_{in} = R_1 \tag{9}$$

Figure 6 shows a voltage source connected to the non-inverting input and the inverting input attached to a resistor, R_1, that is connected to ground. The same principles apply in this case, except that the virtual ground is now equal to V_{in}. In this case, the input impedance, Z_{in}, is equal to infinity, but in the non-ideal case it would be equal to the impedance of the op-amp itself.

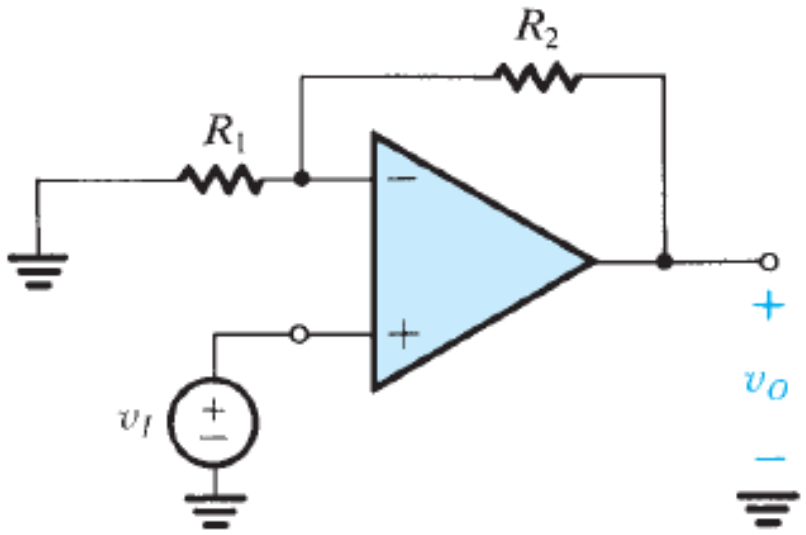

Figure 6. Non-Inverting Closed-Loop Configuration. Source: [18].

$$V_{out} = V_{in}\left(1+\frac{R_2}{R_1}\right) \rightarrow \frac{V_{out}}{V_{in}} = \left(1+\frac{R_2}{R_1}\right) \tag{10}$$

$$Z_{in} = \infty \tag{11}$$

2. Non-ideal Op-amp Model

Figure 7 shows the non-ideal model of the op-amp in a non-inverting configuration. Here, the previously infinite input-impedance is replaced with the finite input-impedance R_i, the zero-output impedance is replaced with the non-zero-output impedance R_o, and the open-loop gain, A, is now finite. While V^+ is still tied to ground, the value of V^- is no longer equal to V^+ due to the small voltage drop across R_i. Because of these non-ideal factors, the previous equations from the ideal model are no longer true and must be re-calculated by setting up new equations for V_{in} and V_{out}, as shown in (12) [17].

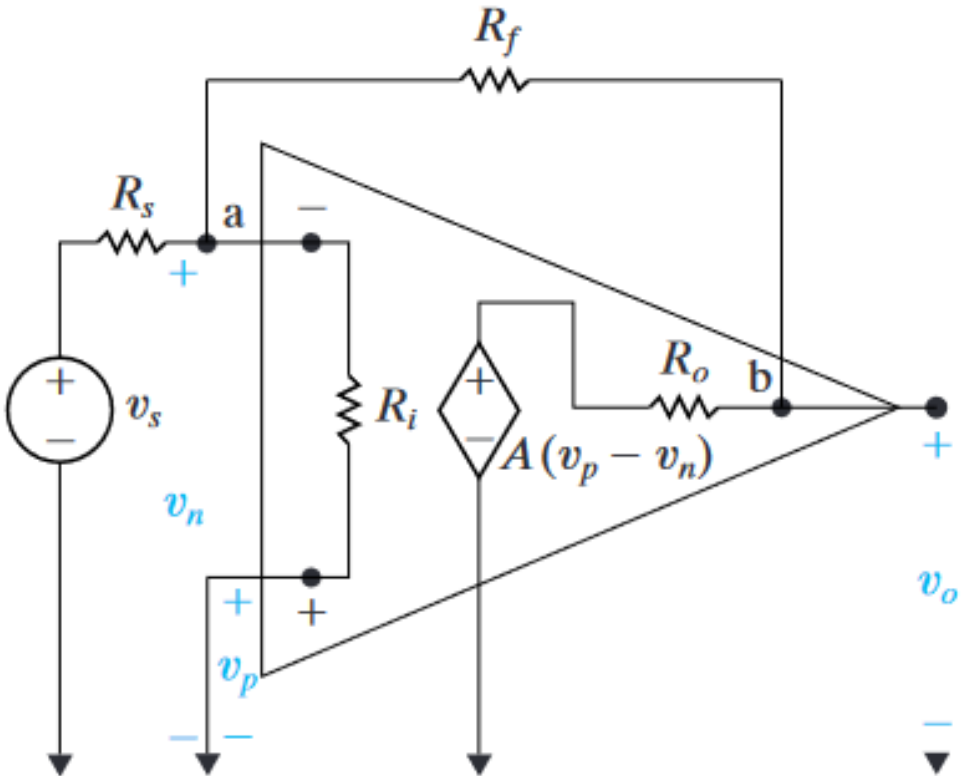

Figure 7. Non-ideal Inverting Op-amp Model. Source: [17].

$$\text{Equation 1: } \frac{V^- - V_{in}}{R_s} + \frac{V^- - V^+}{R_i} + \frac{V^- - V_{out}}{R_f} = 0$$

$$\text{Equation 2: } \frac{V_{out} - V^-}{R_f} + \frac{V_{out} - A(V^+ - V^-)}{R_o} = 0 \qquad (12)$$

Setting V^+ to zero and solving each equation in terms of V_{in} and V_{out} simplifies to,

$$\left(\frac{1}{R_s}+\frac{1}{R_i}+\frac{1}{R_f}\right)V^- - \frac{1}{R_f}V_{out} = \frac{1}{R_s}V_{in}$$
$$\left(\frac{A}{R_o}-\frac{1}{R_f}\right)V^- + \left(\frac{1}{R_f}+\frac{1}{R_o}\right)V_{out} = 0 \ , \tag{13}$$

where combining both equations and solving for V_{out} yields,

$$V_{out} = \frac{-A+\left(R_o \middle/ R_f\right)}{\frac{R_s}{R_f}\left(1+A+\frac{R_o}{R_i}\right)+\left(1+\frac{R_s}{R_i}\right)+\frac{R_o}{R_f}}V_{in} . \tag{14}$$

Equation (14) is the transfer function of the non-ideal inverting op-amp configuration in Figure 7. From here, the closed-loop gain, A_{cl}, can be calculated by simply dividing by V_{in}. This demonstrates the effect that a finite-input impedance and open-loop gain has on the performance of an op-amp and why a very high input-impedance and open-loop gain are needed to maintain the conditions for a virtual short [17].

3. Frequency Response and Bandwidth

One of the most limiting factors to the performance of any non-ideal op-amp is the frequency response. In the case of the ideal op-amp, the frequency response is constant across an infinite bandwidth range. In the case of the non-ideal op-amp, however, the bandwidth of the op-amp is finite and determined by the internal parasitic capacitances of the device. For this reason, many op-amps are internally compensated, which means they are built with a known value capacitor to control their operational stability and which gives the op-amp frequency response a dominant real pole at low frequency [18].

The use of this capacitor to ensure the stability of an op-amp over a particular operational frequency range is known as frequency compensation [18]. Figure 8 shows an example of the frequency response for a generic, internally compensated, op-amp with a corner frequency at 10 Hz and a gain roll-off of -20 dB/decade through the unity-gain

bandwidth at 0 dB and 10^6 Hz, or 10 MHz, which equals the open-loop bandwidth of this device. This point where the open-loop gain curve crosses 0 dB is indicative of the finite nature of a non-ideal op-amps bandwidth [18].

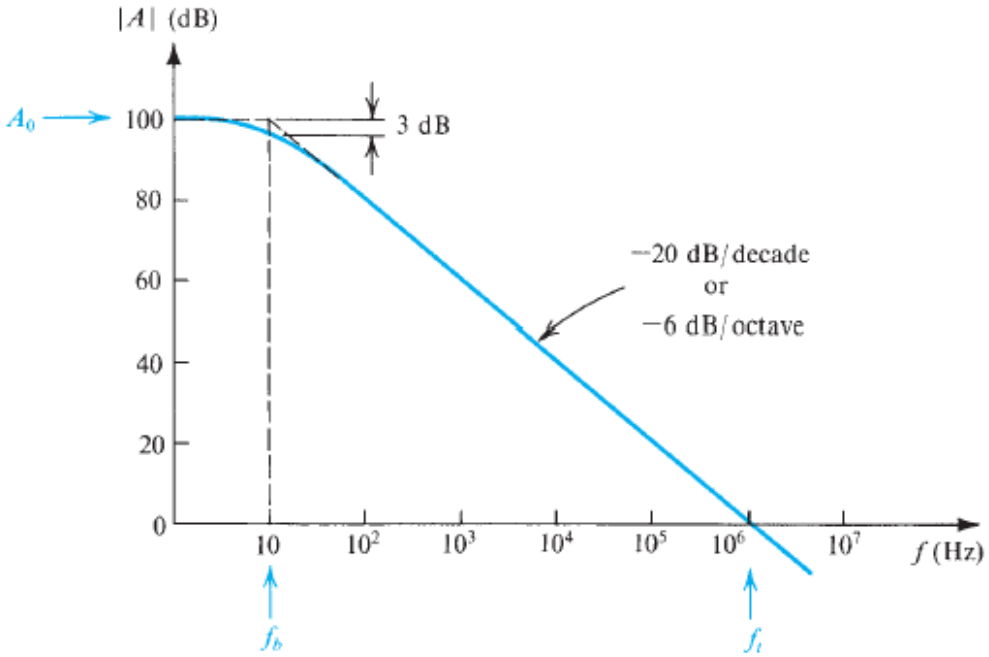

Figure 8. Open-Loop Gain of Non-ideal Op-Amp. Source: [18].

4. Closed Loop Op-amp Circuit Stability

The previous section introduced the idea of stability in an op-amp over its open-loop bandwidth, and some of the mechanisms by which to ensure said stability. This section will primarily focus on the closed-loop bandwidth, how it is related to the open-loop bandwidth, and the concept of phase margin as well as how it can be used to quickly identify whether a closed-loop op-amp circuit will be stable.

The closed-loop behavior of an op-amp with feedback can be modeled by a block diagram, as shown in Figure 9. In Figure 9, A represents the open loop op-amp gain, or A_{ol}, β represents the feedback factor [18], and x_i, x_o, and x_f represent V_{in}, V_{out}, and V_{fb}, respectively.

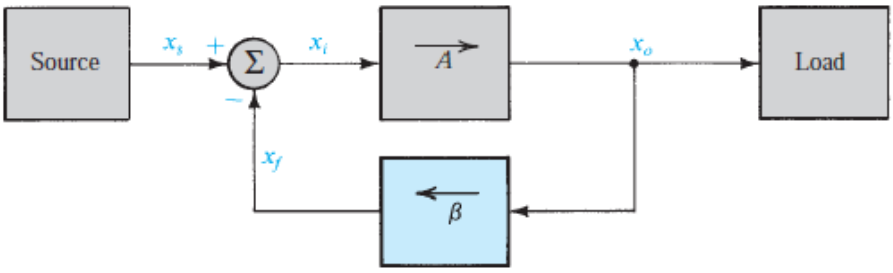

Figure 9. Block Diagram Model of Closed-Loop Gain. Source: [18].

With these terms defined, a few relationships and equations relating to the gain can now be derived,

$$\beta = \text{Feedback Factor} = \frac{V_{fb}}{V_{out}} \tag{15}$$

$$A_{cl} = \text{Closed-Loop Gain} = \frac{A_{ol}}{(1 + A_{ol}\beta)} \tag{16}$$

$$\text{Loop Gain} = A_{ol}\beta \tag{17}$$

$$A_{cl} = \lim_{A_{ol} \to \infty} \left(\frac{A_{ol}}{1 + A_{ol}\beta} \right) = \frac{1}{\beta} \tag{18}$$

Equation (16) shows that the model in Figure 9 becomes unstable when loop gain, (17), is equal to -1, because this is when the denominator of closed-loop gain, shown in (16), is equal to 0, causing A_{cl} to equal infinity. This may not seem possible because the lowest value for loop gain magnitude is 0 dB. However, the loop gain can become negative due to the phase shift of the gain. When the system experiences a phase shift of -180°, there is an inversion of the gain, so when loop gain is 0 dB and there is a -180° phase shift, the value of loop gain, shown in (17), becomes -1, therefore, the system becomes unstable.

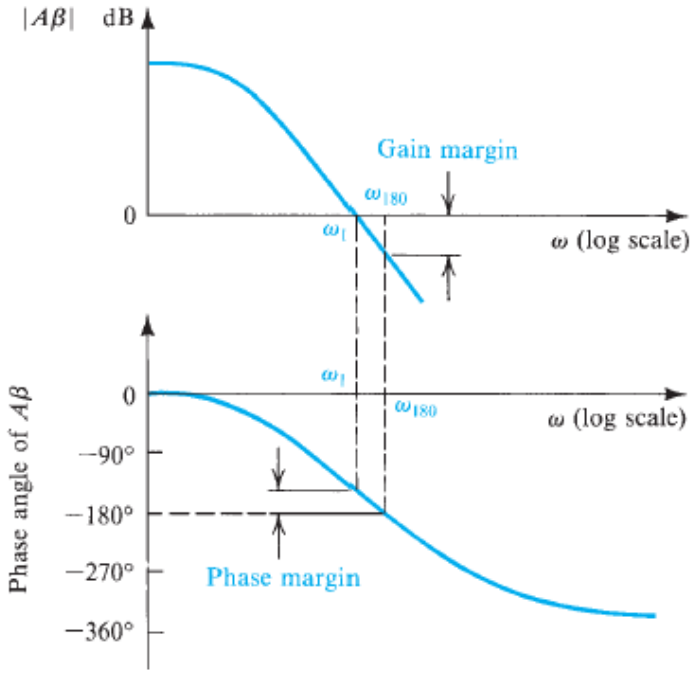

Figure 10. Illustration of Gain Margin and Phase Margin. Source: [18].

The margin of stability between loop gain and a -180° phase shift is known as the phase margin [18]. Phase margin, visually depicted in Figure 10, is defined as the difference between the loop gain phase angle and -180°, at the point where loop gain magnitude equals 0 dB. If the phase angle is greater than -180° when the loop gain equals 0 dB, then the circuit is stable. When designing an op-amp circuit with closed-loop feedback, or a feedback amplifier, the phase margin can be used to quickly determine the degree of its stability. For this reason, feedback amplifiers are typically designed to have a phase margin greater than 45° [18].

Using Figure 11 as an example, (15) through (18) would be used to define the following equations:

$$\beta = \frac{V_{fb}}{V_{out}} = \frac{R_1}{R_1 + R_2} \tag{19}$$

$$\therefore A_{cl} = \frac{A_{ol}}{\left(1 + A_{ol}\left(\frac{R_1}{R_1 + R_2}\right)\right)} \tag{20}$$

$$\therefore A_{cl} = \lim_{A_{ol} \to \infty} \left(\frac{A_{ol}}{1 + A_{ol}\left(\frac{R_1}{R_1 + R_2}\right)} \right) = \frac{1}{\left(\frac{R_1}{R_1 + R_2}\right)} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1} \tag{21}$$

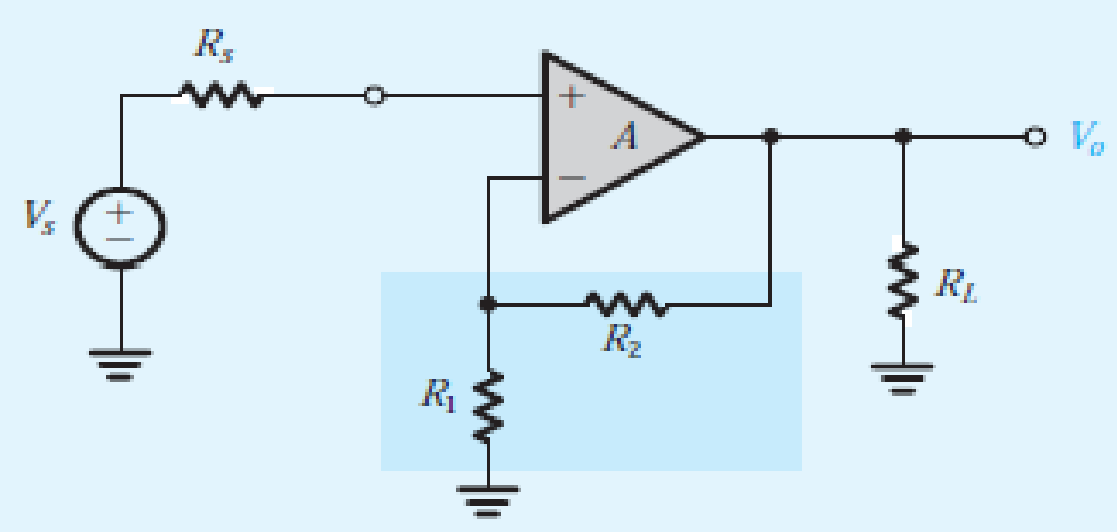

Figure 11. Example of Non-inverting Feedback Amplifier. Source: [18].

Equations (19) and (21) show that loop gain is the product of β and A_{ol}. If the open-loop gain is real and constant, then the circuit will be stable at all frequency values as the phase of the loop gain remains zero at all frequencies [18].

C. TRANSIMPEDANCE AMPLIFIER CONFIGURATION

The transimpedance amplifier (TIA) op-amp configuration, also referred to as a current to voltage converter or current feedback amplifier, is one of the methods most frequently used by designers to amplify the low-level currents produced by various types of sensors into a useful output voltage that can be measured by an analog-to-digital converter (ADC). A TIA schematic is typically referenced with a photodiode with its

cathode connected to ground and anode connected to the inverting input terminal of an op-amp, as in Figure 12.

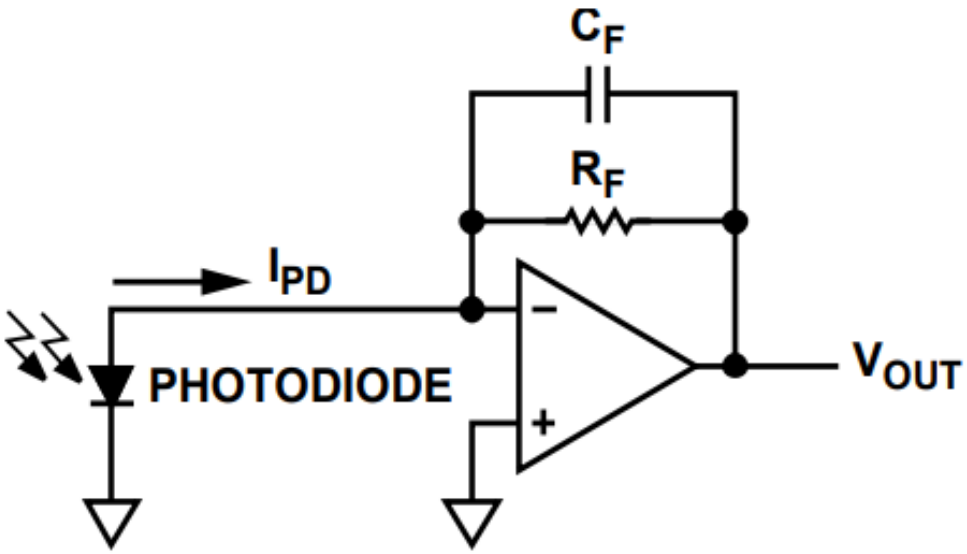

Figure 12. TIA with Photodiode. Source: [19].

In Figure 12, C_F and R_F refer to the feedback capacitor, which includes any resistive capacitance, and the feedback resistor, I_{PD} refers to the photocurrent and dark current generated by the photodiode, and V_{OUT} represents the output voltage.

Figure 13 shows another common representation of a TIA circuit where the photodiode is modeled by a current source in parallel with a capacitor and resistor, connected between the inverting input and ground. C_{SHUNT} represents the junction capacitance of the photodiode and R_{SHUNT} represents the equivalent input resistance of the photodiode as seen by the op-amp. Conveniently, this model is also representative of many types of devices, with I_{PD} used to model the low-level leakage current of the device. Given this similarity, equations derived for this model can be applied to predict performance of the TIA circuit for DUT current sensing applications.

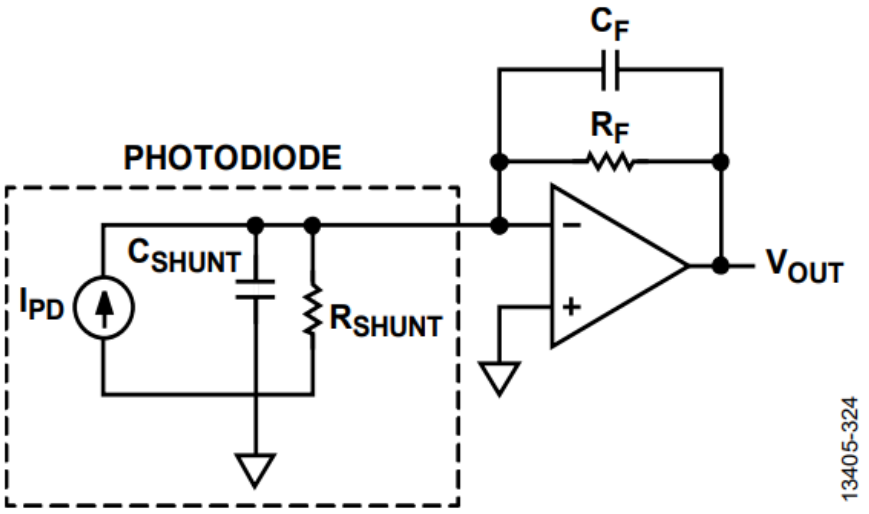

Figure 13. TIA with Equivalent Photodiode Model. Source: [19].

1. TIA Stability Analysis

To derive the transfer function for the TIA, new parameters must first be defined, based on (15) through (18). For these derivations, R_{SHUNT} will be represented by R_i, for input resistance; C_{SHUNT} will be represented by C_i, for input capacitance; I_{PD} will be represented by I_{in}, for input current, and V^- and V^+ will represent the inverting and non-inverting input terminals, respectively.

Z_f and Z_i, (22) and (23), represent the feedback and input impedances corresponding to the parallel combinations of C_f with R_f and C_i with R_i.

$$Z_f = \frac{R_f}{1 + sR_fC_f} \tag{22}$$

$$Z_i = \frac{R_i}{1 + sR_iC_i} \tag{23}$$

The transfer function derivation begins with setting up the current equation at V^-,

$$\frac{V^- - V_{out}}{Z_f} + \frac{V^-}{Z_i} - I_{in} = 0 \tag{24}$$

then, proceeding to solve for V^- in terms of I_{in} and V_{out} yields,

$$I_{in} = \frac{V^- - V_{out}}{Z_f} + \frac{V^-}{Z_i}$$

$$I_{in} = \frac{V^-}{Z_f} - \frac{V_{out}}{Z_f} + \frac{V^-}{Z_i}$$

$$I_{in} + \frac{V_{out}}{Z_f} = V^- \left(\frac{1}{Z_f} + \frac{1}{Z_i} \right)$$

$$I_{in} + \frac{V_{out}}{Z_f} = V^- \left(\frac{Z_f + Z_i}{Z_f Z_i} \right)$$

$$V^- = \left(I_{in} + \frac{V_{out}}{Z_f} \right) \left(\frac{Z_f Z_i}{Z_f + Z_i} \right)$$

$$V^- = \left(\frac{Z_f Z_i}{Z_f + Z_i} \right) I_{in} + \left(\frac{Z_i}{Z_f + Z_i} \right) V_{out} . \tag{25}$$

Finally, simplifying the impedances in (25) yields,

$$\left(\frac{Z_i}{Z_f + Z_i} \right) \rightarrow \beta$$

$$\left(\frac{Z_f Z_i}{Z_f + Z_i} \right) \rightarrow \left[Z_f \parallel Z_i \right]$$

$$V^- = \left[Z_f \parallel Z_i \right] I_{in} + \beta V_{out} . \tag{26}$$

Thus, defining V_{out} and using (26) for V^- yields,

$$V_{out} = A_{ol}(V^+ - V^-) = -A_{ol} V^-$$

$$\therefore V_{out} = -A_{ol} \left(\left[Z_f \parallel Z_i \right] I_{in} + \beta V_{out} \right), \tag{27}$$

and finally, by solving for V_{out},

$$V_{out}\left(1+A_{ol}\beta\right)=-I_{in}\left[Z_f \parallel Z_i\right]A_{ol}$$

$$\therefore V_{out}=-I_{in}\left[Z_f \parallel Z_i\right]\frac{A_{ol}}{1+A_{ol}\beta} \quad . \tag{28}$$

The frequency dependence of the TIA assuming an ideal op-amp can be found by taking the limit of A_{ol} in (28). From (18), taking the limit of A_{cl} as $A_{ol}\rightarrow\infty$ yields the following,

$$V_{out}=-I_{in}\left[Z_f \parallel Z_i\right]\lim_{A_{ol}\rightarrow\infty}\left(\frac{A_{ol}}{1+A_{ol}\beta}\right)$$

$$\therefore V_{out}=-I_{in}\left[Z_f \parallel Z_i\right]\frac{1}{\beta} \tag{29}$$

Finally, expanding and simplifying (29) yields the TIA transfer function,

$$V_{out}=-I_{in}\frac{Z_f \cancel{Z_i}}{\cancel{Z_f+Z_i}}\frac{\cancel{Z_f+Z_i}}{\cancel{Z_i}}$$

$$\therefore V_{out}=-I_{in}Z_f=-I_{in}\frac{R_f}{1+sR_fC_f} \tag{30}$$

Noise gain (NG) is the inverse of the feedback factor, shown in (15). The NG transfer function, shown in (31), is derived by placing a noise source in series with V^+ of the TIA and solving for the closed-loop gain. This is important because noise incident at V^+ is amplified by the closed-loop gain, which can cause oscillations that lead to instability. From (29), when A_{ol} is large, the TIA transfer function is dominated by the contribution of NG.

$$\frac{1}{\beta}=\text{Noise Gain}=\frac{Z_f+Z_i}{Z_i} \tag{31}$$

Solving the NG transfer function at all frequencies can be done by combining (22), (23) and (31) as follows,

$$NG(f) = \frac{1}{\beta} = \frac{Z_f + Z_i}{Z_i} = \left(\frac{R_f + R_i}{R_i}\right)\left(\frac{1 + s\frac{R_f R_i}{R_f + R_i}\left(C_f + C_i\right)}{1 + sC_f R_f}\right). \quad (32)$$

Equation (32) shows that NG has a constant contribution at low frequency direct current (dc) governed by R_f and R_i. It also has a single zero, whose frequency can be represented by f_z, from (22), and a single pole, whose frequency can be represented by f_p, from (23). Since NG is the inverse of feedback factor, the zeros and poles of the feedback factor becomes the poles and zeros of the NG. The location of f_z is governed by C_i and compensated by C_f. This concept will be covered in further detail later in the thesis.

$$f_z = \frac{1}{2\pi\left[R_f \parallel R_i\right]\left(C_f + C_i\right)}$$
$$Given\ \mathrm{R}_i >> R_f, \left[R_f \parallel R_i\right] \cong R_f$$
$$\therefore f_z = \frac{1}{2\pi R_f\left(C_f + C_i\right)} \quad (33)$$

$$f_p = \frac{1}{2\pi R_f C_f} \quad (34)$$

Substituting for s and redefining the dc NG contribution in (32) yields,

$$NG(0) = \mathrm{DC\ NG} = \left(\frac{R_f + R_i}{R_i}\right)$$
$$NG(f) = NG(0)\left[\frac{1 + j\frac{f}{f_z}}{1 + j\frac{f}{f_p}}\right]. \quad (35)$$

Therefore, at low frequencies, NG is dominated by the input and feedback resistances. Since the input resistance is based on the effective resistance across a zero-biased PN diode, the value of R_i is typically greater than 10^9 Ω, or 10 GΩ. The full-

spectrum behavior of NG can be understood by again revisiting (32) to derive the high frequency contribution of NG,

$$NG(\infty)=\frac{1}{\beta}=\frac{Z_f+Z_i}{Z_i}=\left(\frac{R_f+R_i}{R_i}\right)\left(\frac{1+s\dfrac{R_fR_i}{R_f+R_i}\left(C_f+C_i\right)}{1+sC_fR_f}\right). \tag{36}$$

Next, taking the limit as s approaches infinity yields,

$$\lim_{s\to\infty}\frac{1}{\beta}=\frac{Z_f+Z_i}{Z_i}=\left(\frac{R_f+R_i}{R_i}\right)\left(\frac{1+s\dfrac{R_fR_i}{R_f+R_i}\left(C_f+C_i\right)}{1+sC_fR_f}\right)$$

$$=\left(\frac{\cancel{R_f+R_i}}{\cancel{R_i}}\right)\left(\frac{\dfrac{\cancel{R_f}\ \cancel{R_i}}{\cancel{R_f+R_i}}\left(C_f+C_i\right)}{C_f\cancel{R_f}}\right)$$

$$\therefore\lim_{s\to\infty}\frac{1}{\beta}=\frac{C_f+C_i}{C_f} \quad . \tag{37}$$

Therefore, at high frequencies, the contribution of NG is dominated by C_i, which cannot be controlled, and C_f which can. Figure 14 provides a visual illustration of how the selection of C_f, or lack thereof, affects the behavior of NG in relation to A_{ol}. The corner frequency, f_c, on the A_{ol} curve is typically set by the internal design of the op-amp and sets a smooth -20 dB/decade roll-off and induces a phase shift of -90°; the zero frequency, f_z, on the NG curve is defined by (33); the pole frequency, f_p, on the NG curve is defined by (34); and the gain-bandwidth product (GBWP) frequency, f_{GBW}, is defined by the point where A_{ol} crosses unity-gain (0 dB). Since the NG is the inverse of the feedback factor, the presence of the zero f_z leads to an overall phase shift in the loop gain of 180° which can lead to instability.

The frequency at the point where NG intersects A_{ol} is what determines both the closed-loop bandwidth, or f_i and the 0 dB frequency of the loop gain. The GBWP is the product of f_i and A_{cl}. Since NG approaches A_{ol} at +20 dB/decade as A_{ol} rolls-off at -20 dB/decade, a generalized equation for the crossover frequency of the NG and A_{ol} can be derived by taking the geometric mean of f_z and f_{GBW} [20], as shown in (38). Equation (38) can be used to derive an equation to solve for the value of C_f needed to create the NG pole (and thus zero in the feedback factor) at f_{p2} in Figure 14 in terms of f_{GBW} and C_i, as shown in (39), ensuring at least 45° of PM in the loop gain and moderate stability.

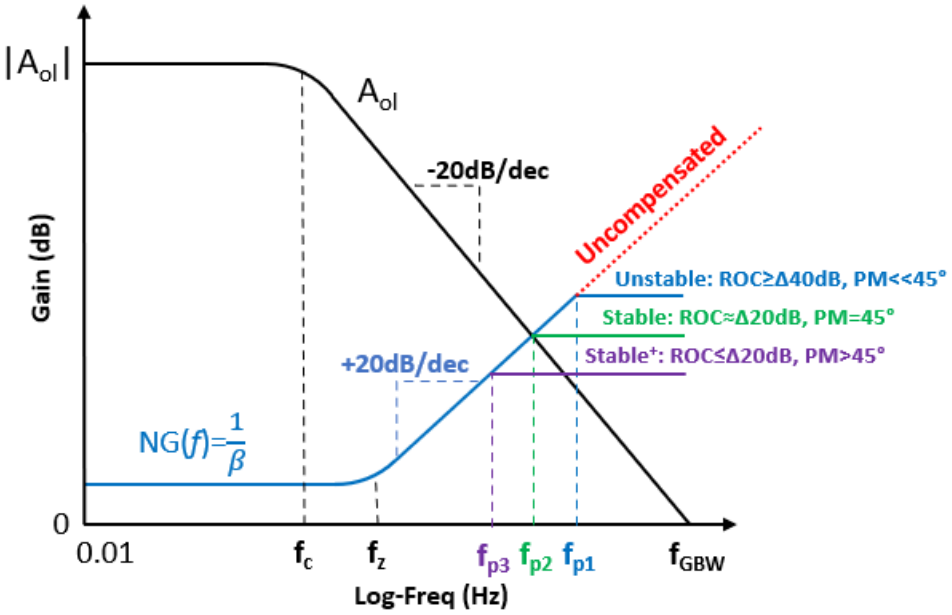

Figure 14. Effects of C_f on A_{ol} vs. NG Crossover Stability

$$f_i = \sqrt{f_z f_{GBW}} \tag{38}$$

Combining (33), (34), and (38), then squaring both sides and solving the resulting quadratic equation for C_f yields the following,

$$f_i = \sqrt{\frac{f_{GBW}}{2\pi R_f (C_f + C_i)}}$$

$$\left(\frac{1}{2\pi R_f C_f}\right)^2 = \frac{f_{GBW}}{2\pi R_f (C_f + C_i)}$$

$$\therefore C_f = \frac{1}{4\pi R_f f_{GBW}}\left(1 + \sqrt{1 + 8\pi R_f C_i f_{GBW}}\right). \tag{39}$$

When designing a TIA, using (39) allows for the quick determination of the C_f needed to ensure stability at the intersection of A_{ol} and NG. Another simple method of visually analyzing the stability of a TIA, or any feedback amplifier, is to note the rate of closure (ROC) between A_{ol} and NG. The uncompensated case in Figure 14 refers to a TIA configuration without a feedback capacitor. The presence of C_i will create a low-frequency zero in the NG transfer function, initiating a +20 dB/decade rise. Without compensation in the form of a feedback capacitor, NG will continue to rise until it intersects with A_{ol}, which has at least -20 dB/decade of roll off [20]. Since every 20 dB/decade of slope in the ROC corresponds to a 90° overall phase shift in the loop gain, this Δ40 dB/decade ROC at the intersect produces a 180° phase shift while A_{ol} is equal to NG, shown in (40), causing A_{cl} to become unstable.

$$\therefore A_{ol}\beta = 1\angle 180° = -1 \tag{40}$$

Table 2 provides a quick reference for troubleshooting the stability of a TIA by analyzing the ROC. Generally, a larger value of C_f leads to a NG pole at a lower frequency, preventing the uncompensated or unstable case from occurring.

Table 2. A_{ol} vs. NG Stability Factors. Adapted from [21].

f_p	Slope of A_{ol}	Slope of NG	ROC	PM	Stability	ΔC_f
f_{p1}	-20dB/decade	+20dB/decade	≥Δ40dB/ decade	<45°	Unstable	Increase
f_{p2}	-20dB/decade	~0dB/decade	~Δ20dB/ decade	~45°	Stable	Increase/Hold
f_{p3}	-20dB/decade	+0dB/decade	≤Δ20dB/ decade	>45°	Stable^{+}	Decrease/Hold

2. TIA Noise Analysis

For a TIA to maximize the resolution of current sensing, noise generated by the TIA circuit must be minimized in the circuit design. There are multiple internal and external noise contributing sources that should be considered when conducting a noise analysis for a TIA, shown in Figure 15. These can be simplified into three contributions, each modeled as a separate noise source: DUT noise, R_f noise, and op-amp noise. The noise contributions from each of these sources can be geometrically combined to compute the total output noise voltage. Each of these noise sources is uncorrelated and random, with a normal probability density function (PDF); therefore, the individual contribution they make to the output noise can be added as the root sum of their squares to give the total output noise. Moreover, these noise sources are presented as spectral densities whose units are V/√Hz for thermal and voltage noise, and A/√Hz for current noise.

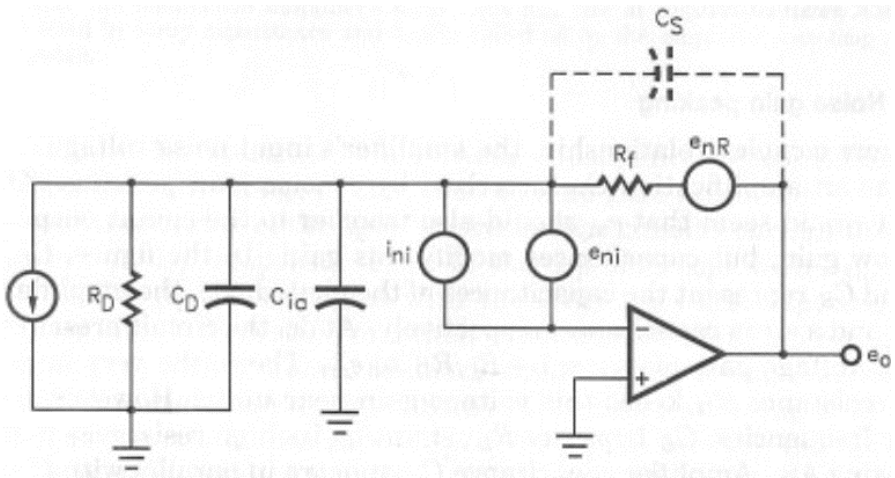

Figure 15. TIA Noise Model. Source: [20].

As such, to convert these values from spectral density to root-mean-square (RMS), their power spectral density (PSD) must first be integrated over their relevant bandwidth.

$$\sqrt{\int_{f_L}^{f_H} e_n^{\,2} df} = E_{rms} \tag{41}$$

From (41), because E_{rms} has a normal PDF, its value can be converted to a peak-to-peak value, E_{pp}, by multiplying E_{rms} by 6. This accounts for six standard deviations, representing the probability of 99.7% of the peak-to-peak values [22],[23].

$$6 \times E_{rms} = E_{pp} \tag{42}$$

a. DUT Noise Contribution

The noise contribution of the DUT is a combination of the input-referred thermal noise current, I_D, caused by the DUT resistance, R_D, and the input-referred shot noise due to the flow of current from the DUT caused by light, I_{sL}, or the lack thereof, I_{sD}, referred to as the dark current or leakage current. Equation (43) through (45) show the input-referred noise current spectral density calculations for each of these contributions and (46) shows the total DUT input-referred noise current spectral density contribution. In the equations

below, k is the Boltzmann constant, T is the temperature in Kelvin, and q is the elementary charge.

$$i_{D,in} = \sqrt{\frac{4kT}{R_D}} \tag{43}$$

$$i_{sL,in} = \sqrt{2qI_{sL}} \tag{44}$$

$$i_{sD,in} = \sqrt{2qI_{sD}} \tag{45}$$

$$i_{nDUT,in} = \sqrt{{i_{D,in}}^2 + {i_{sD,in}}^2 + {i_{sL,in}}^2} \tag{46}$$

b. R_f Noise Contribution

The noise contribution of the feedback resistor, R_f, is defined as the output-referred thermal noise voltage spectral density, $e_{nRf,out}$, defined in (47).

$$e_{nR_f,out} = \sqrt{4kTR_f} \tag{47}$$

c. Op-amp Noise Contribution

The noise calculations for the op-amp are more complex because of the two different noise sources intrinsic to the op-amp. The first is the input-referred noise current spectral density, $i_{nOPA,in}$, and the second is the input-referred noise voltage spectral density, $e_{nv,in}$. Both values are provided in the datasheet of op-amps where they are typically referred to as current noise density, I_n, and voltage noise density, e_n.

(1) Calculating the Input-Referred Noise Voltage Contribution of the Op-Amp

The total input-referred noise voltage spectral density is difficult to calculate because NG is a function of frequency, shown in (35), whose magnitude varies throughout the unity-gain crossover bandwidth of the op-amp, as shown in Figure 16. This calculation can be simplified by splitting the NG function into regions of constant slope, whose bandwidths can be marked by the previously derived pole and zero frequencies, then

normalizing each region by the broadband voltage noise spectral density, e_{nBB}, which represents the noise floor [20].

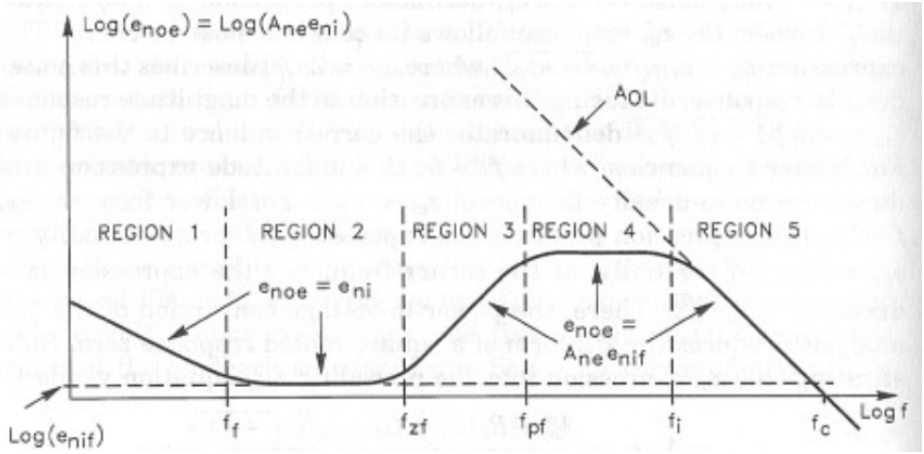

Figure 16. Frequency Response of $e_{nv,in}$ by Region. Source: [20].

The RMS output noise voltage due to $e_{nv,in}$ of the op-amp can then be calculated for each region using (48) through (52). Where f_L represents the lowest frequency in the datasheet, f_f represents the frequency of the 1/f corner, f_z represents the zero-frequency calculated in (33), f_p represents the pole-frequency calculated in (34), f_i represents the frequency calculated in (38), and f_{GBW} represents the unity-gain crossover frequency of the op-amp.

$$E_{nvR1,out} = e_{nBB}\sqrt{f_f \ln\left(\frac{f_f}{f_L}\right)} \tag{48}$$

$$E_{nvR2,out} = e_{nBB}\sqrt{f_z - f_f} \tag{49}$$

$$E_{nvR3,out} = e_{nBB}\sqrt{\frac{f_p^{\,3} - f_z^{\,3}}{3f_z^{\,2}}} \tag{50}$$

$$E_{nvR4,out} = e_{nBB}\left(\frac{C_f + C_i}{C_f}\right)\sqrt{f_i - f_p} \tag{51}$$

$$E_{nvR5,out} = e_{nBB}\sqrt{\frac{{f_{GBW}}^2}{f_i}} \tag{52}$$

Finally, the total RMS output-referred noise voltage, $E_{nv,out}$, due to $e_{nv,in}$, can be calculated by taking the root sum of the squares of the previous equations, as shown in (53).

$$E_{nv,out} = \sqrt{E_{nvR1,out}^2 + E_{nvR2,out}^2 + E_{nvR3,out}^2 + E_{nvR4,out}^2 + E_{nvR5,out}^2} \tag{53}$$

3. Calculating the Total RMS Noise Voltage

The total RMS output-referred noise voltage due to the input-referred noise current sources, $E_{ni,out}$, can be calculated by first calculating the total input-referred noise current densities of the DUT, $i_{nDUT,in}$, (46), and op-amp, as shown in (54).

$$i_{n,in} = \sqrt{i_{nDUT,in}^2 + i_{nOPA,in}^2} \tag{54}$$

Next, $i_{n,in}$ can be converted to the total output-referred noise voltage density due to the noise current sources of the DUT and op-amp, $e_{ni,out}$, by multiplying (54) by the feedback resistor, R_f, as shown in (55).

$$e_{ni,out} = R_f\sqrt{i_{nDUT,in}^2 + i_{nOPA,in}^2} \tag{55}$$

Then, $E_{ni,out}$, can be calculated by multiplying (55) by the square root of the noise bandwidth (NBW), represented by f_i multiplied by the brick-wall correction factor [22], K_n, as shown in (56),

$$\begin{aligned} NBW &= f_i \times K_n \\ \therefore E_{ni,out} &= e_{ni,out}\sqrt{NBW}\ . \end{aligned} \tag{56}$$

Similarly, $E_{nRf,out}$, can be calculated by multiplying (47) by the root of NBW, shown in (57).

$$E_{nR_f,out} = e_{nR_f,out}\sqrt{NBW} \tag{57}$$

Finally, the total output RMS noise voltage, $E_{n,out}$, can be calculated by taking the root sum of the squares of (53), (56), and (57), as shown in (58) [20].

$$E_{n,out} = \sqrt{E_{nv,out}^2 + E_{ni,out}^2 + E_{nR_f,out}^2} \tag{58}$$

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III. SYSTEM DESIGN

A. SYSTEM OVERVIEW

The LoSPRaDC, Figure 17, was designed as part of a greater effort to upgrade the legacy HTOL system created by Clemmer in 2019 [9]. The original system could measure the I-V characteristics of a single DUT at a time, and only between stress intervals. The subsystem designed in this thesis increases the reliability testing capabilities available at NPS by allowing for greater testing capacity, the ability to test three-terminal devices, and the ability to sense, and respond to, DUT failure under stressing conditions. The data acquisition (DAQ) board was designed to power and monitor the leakage measurement boards (LMB), while also controlling and communicating with future subsystem integrations, such as humidity or fan controllers, via two Inter-Integrated Circuit (I^2C) busses, as well as the ability to control a switch-matrix using up to eight digital input-output (IO) ports. These features are all controlled by a single Mbed LPC1768, 32-bit ARM based microcontroller running the Mbed OS real-time operating system (RTOS) which utilizes the C/C++ programming language.

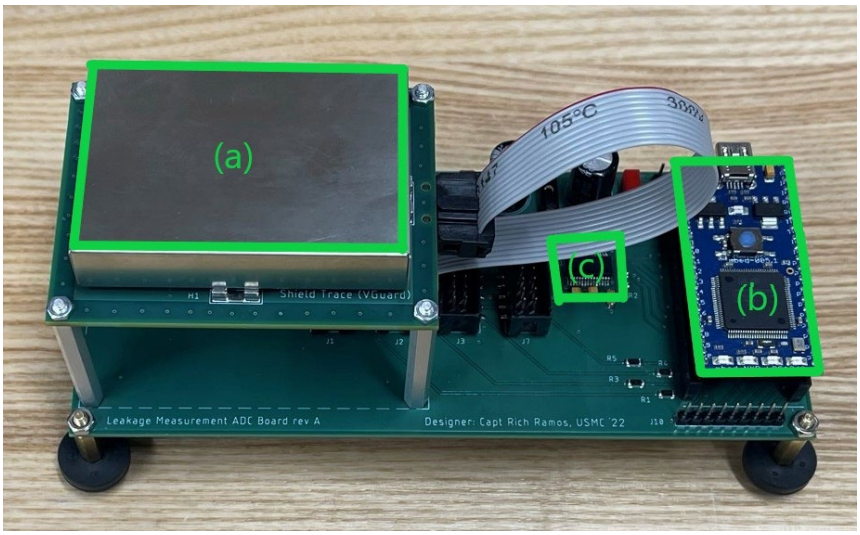

Figure 17. LoSPRaDC: (a) LMB, (b) Mbed, (c) DAQ Board

B. DESIGN OF LEAKAGE MEASUREMENT BOARD

1. TIA Component Selection

Given the picoampere levels of leakage current generated by reverse biased WBGS [24], all components used in the analog front-end of the measurement system must be carefully selected. The common theme across all resources governing low-level current measurement designs was the type of input stage employed by the op-amp that would be used [25]. Traditionally, the input stage of choice for low-level current measurements was a differential pair of junction field-effect transistors (JFET) due to their low input bias currents, on the order of 100s of fA to 10s of pA; high input impedance, on the order of 10s of GΩ; and their relatively low cost. More recently, TIA focused op-amp designs have started using differential metal-oxide silicon field-effect transistors (MOSFET) due to their lower input bias currents, on the order of 10s of fA; higher input impedance, on the order of 100s of TΩ; and much lower input capacitances, due to their metal-oxide layer. Besides the previously mentioned characteristics for ideal TIA op-amps, other key factors are low voltage and current noise densities, on the order of 10s of nV/√Hz and sub-fA/√Hz, respectively. For these reasons, the ADA4530-1, a femtoampere input bias current electrometer amplifier, was chosen. It has a guaranteed bias current of ±250 fA across its entire operating range, a low e_n of 14 nV/√Hz and i_n of 0.07 fA/√Hz, as well as a differential pair of MOSFETs for its input stage [19]. Utilizing this op-amp allows for the construction of a modular TIA circuit capable of sub-pA leakage measurements.

Since the design parameters required the measurement of leakage currents across multiple decades, there needed to be an implementation of ranging in this system. Ranging had to be handled carefully due to the stability and A_{cl} of the TIA being predominantly driven by the poles/zeros created by R_f, C_f, and C_i. Given the modular design requirement, the measurement subsystem needed to be capable of testing a wide variety of devices and interfacing with various testing systems. To facilitate this, the system was designed for a worst-case scenario C_i value of 100 pF with a PM of almost 90°. Choosing the value of R_f for the first range was based on a desired current resolution of 0.4 mV/nA, when used to drive a 16-bit ADC with a 4 V reference, with a voltage resolution of 61 µV per quantized value, which left around seven quantized values worth of headroom. This was

accomplished with R_{fl} and C_{fl} values of 400 kΩ and 33 pF, respectively. Any value of C_i lower than this would only contribute to a flatter NG curve, still maintaining a ROC of 20 dB/decade. This feedback combination maintains a stable PM > 45° up to a C_i of 8 nF. Circuit simulations using LTSpice were used to verify the frequency performance of the design using a SPICE model of the ADA4530-1 and the chosen component values. The simulated circuit NG, op-amp OL gain and loop gain for the two component ranges are shown in Figure 18 and Figure 19.

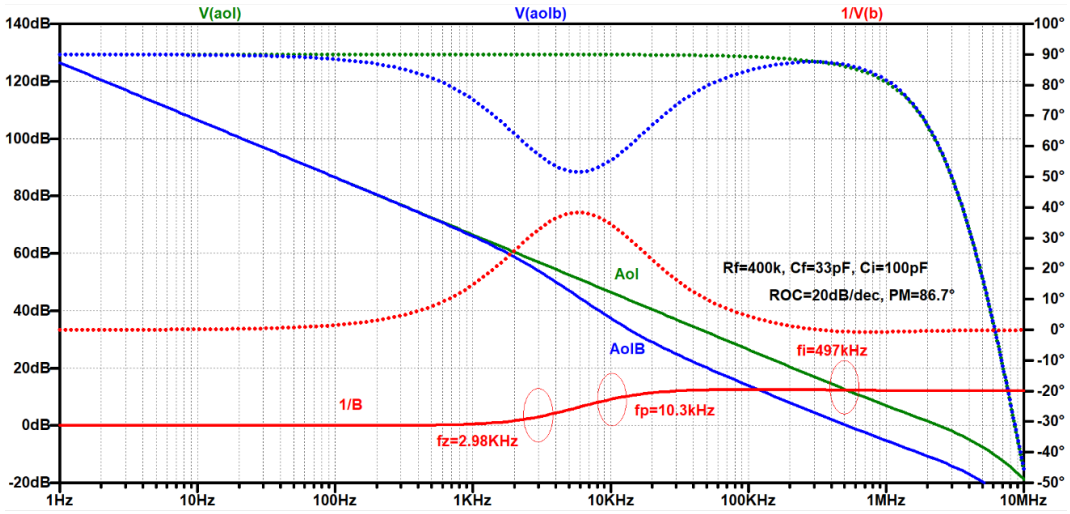

Figure 18. LTSpice Stability plot for Range 1, C_i=100 pF

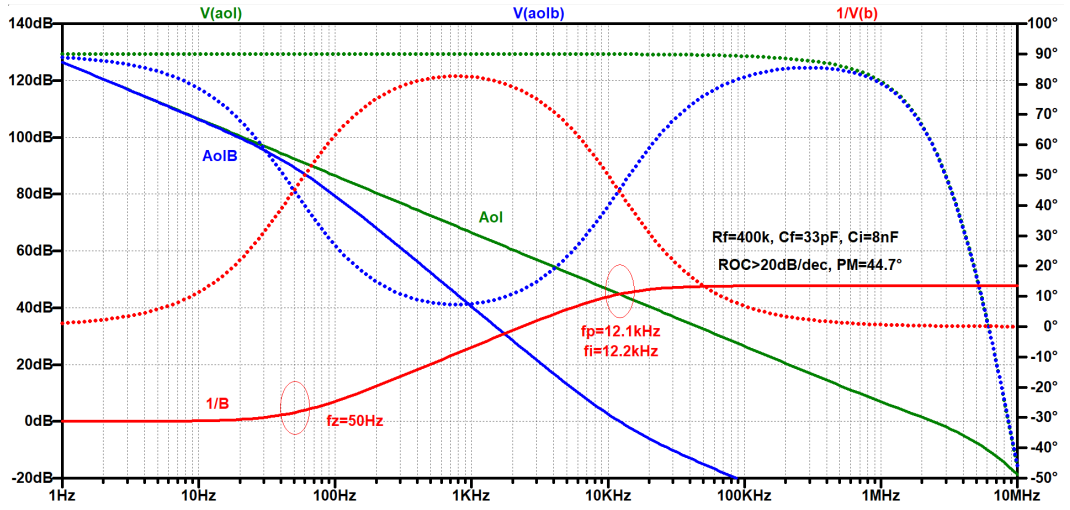

Figure 19. LTSpice Stability Plot for Range 1, C_i=8 nF

Choosing the value of R_f for the first range was based on a desired current resolution of 1 mV/µA. This was accomplished with equivalent R_{f2} and C_{f2} values of 10 kΩ and 200 pF, respectively. Any value of C_i lower than this would only contribute to a flatter NG curve, still maintaining a ROC of 20 dB/decade. This feedback combination also maintains a stable PM > 45° up to a C_i of 8 nF, stability plots of both cases are shown in Figure 20 and Figure 21. Figure 22 shows the circuit configuration in LTSpice for these plots.

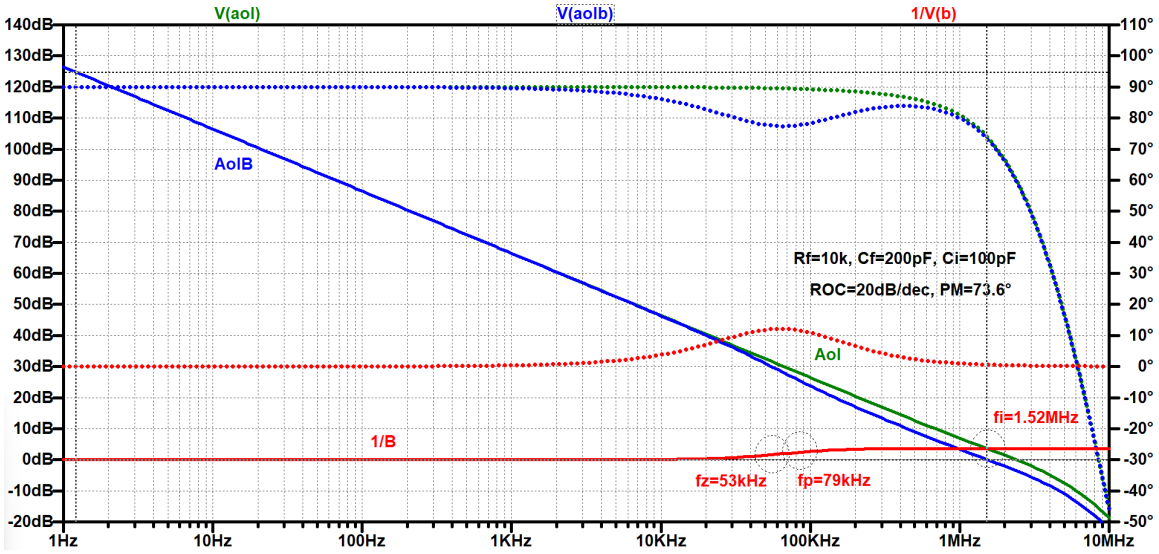

Figure 20. LTSpice Stability Plot for Range 2, C_i=100 pF

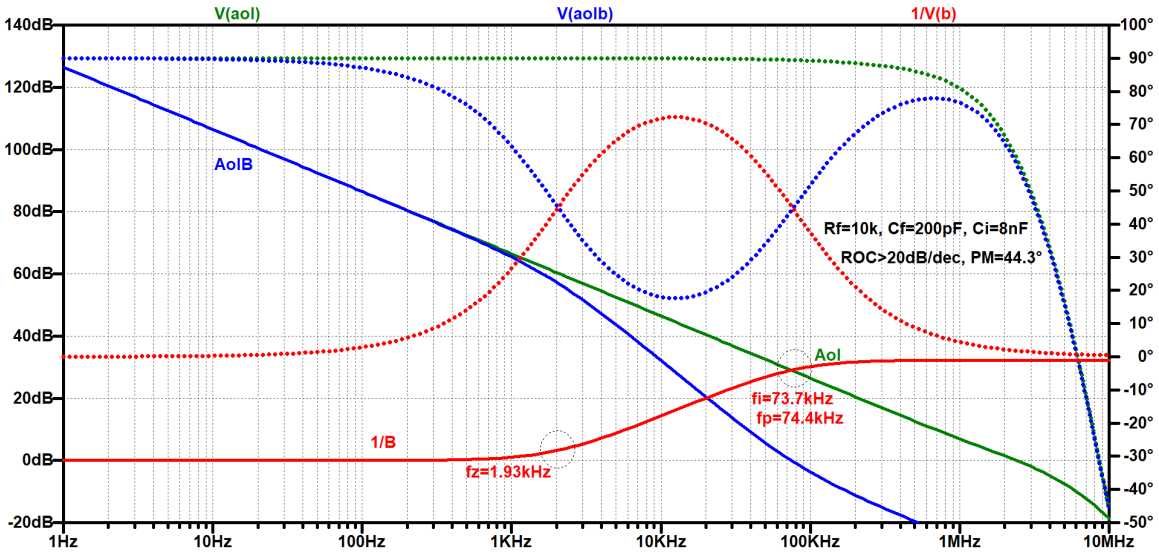

Figure 21. LTSpice Stability Plot for Range 2, C_i=8 nF

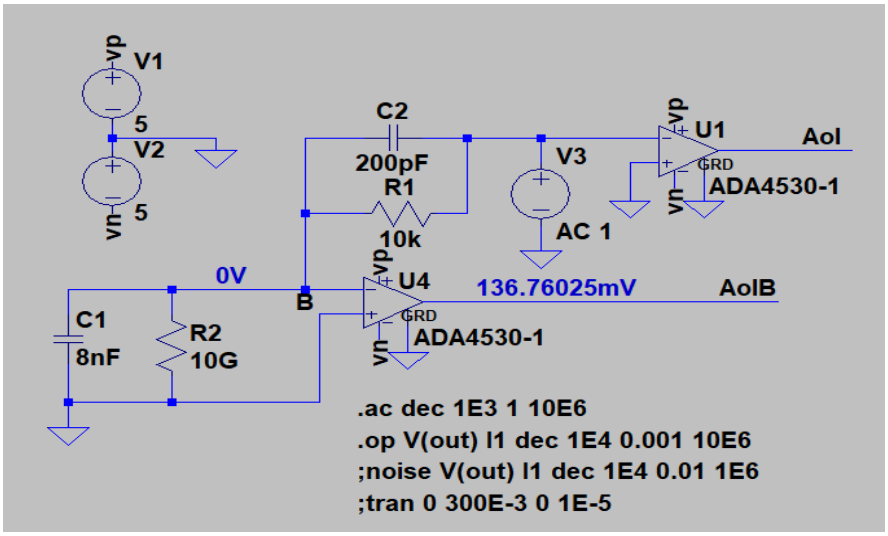

Figure 22. LTSpice Circuit for Plotting A_{ol}, $A_{ol}\beta$, and β^{-1}

Ranging was done by switching R_{f2} and C_{f2} in parallel with R_{f1} and C_{f1}. The actual values of R_{f2} and C_{f2} were implemented using a 10 kΩ and 256 Ω resistor in series, and a 180 pF capacitor, yielding a 10 kΩ equivalent resistor and a 213 pF equivalent capacitor in range two. The switching of these components was done using a Coto 9002–05-11 reed relay, with a built-in transient suppression diode and shield, which was chosen for its fast-operating times, minimum TΩ insulation resistance, and low contact resistance [26].

2. Noise Analysis and Reduction

Noise analysis of the LMB design was done using LTSpice. Figure 23 and Figure 24 represent the LTSpice schematics used to test the noise of both amplifier stages and ranges. The first stage represents the TIA and the given range setting it is configured for, either one for the nA range or two for the µA range. The second stage in each range consists of an inverting Multiple Feedback (MFB) LPF, configured for unity gain, with a cut-off frequency of 1 kHz. The MBF LPF configuration was chosen as the ADC driver due to its ease of implementation and stop-band rejection performance.

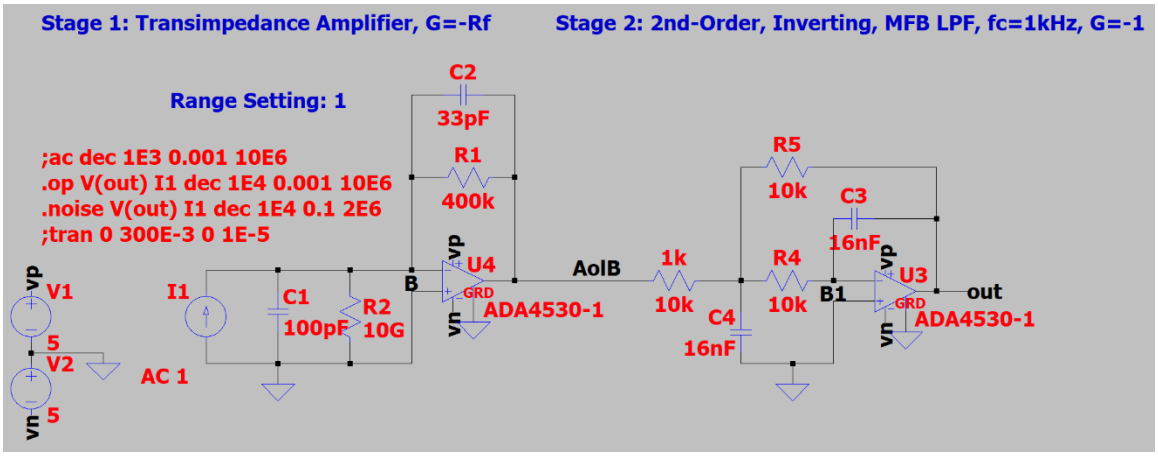

Figure 23. LTSpice Noise Model for Stages 1 and 2 of Range 1

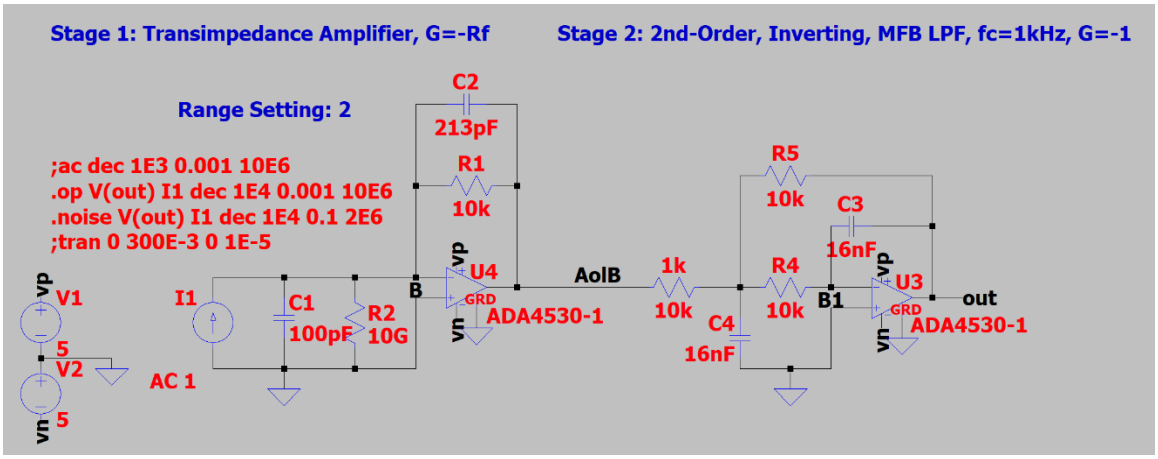

Figure 24. LTSpice Noise Model for Stages 1 and 2 of Range 2

Figure 25 is a visual representation of each region of the output voltage noise due to the ADA4530-1 itself, without any contribution from thermal resistance or input current. This output is equivalent to the output generated by using the pole and zero frequencies calculated below, with the e_{nBB} values from the datasheet for the ADA4530-1, in (53). Using the values from the datasheet, and the frequency values listed in Figure 25, yielded an output of 60.079 µV RMS.

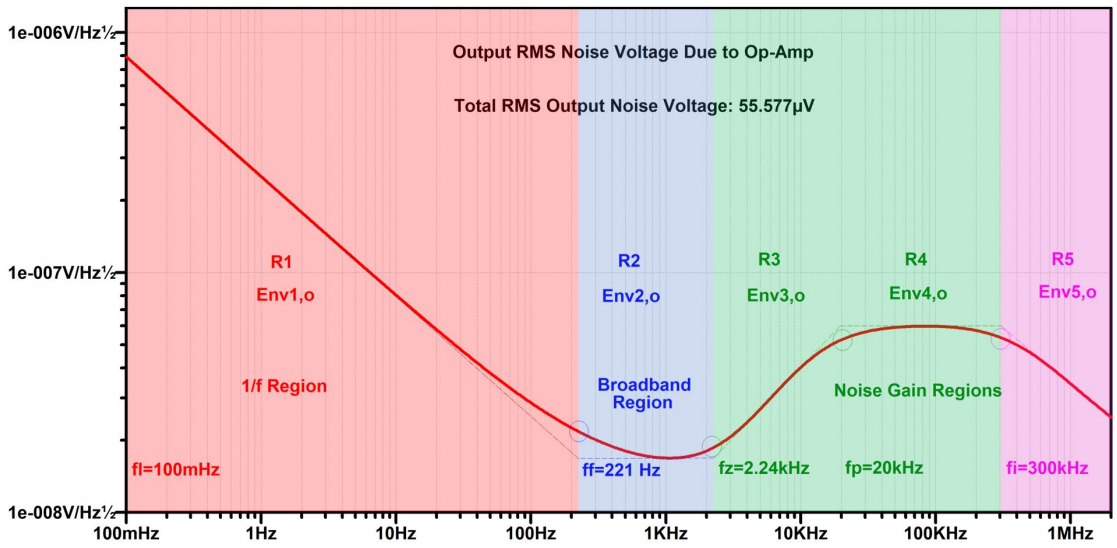

Figure 25. LTSpice E_{nvR} Regions of ADA4530-1

Noise analysis of each stage was accomplished using LTSpice. Figure 26 shows the total output noise of stage one, whereas Figure 27 shows the total output noise of both the first and second stages. The total output voltage noise (RMS) was decreased by 59.4% with the addition of the second stage, this is due to the MBF LPF attenuating the noise contributions at higher frequency. Converting each of total RMS noise outputs from Figure 26 and Figure 27 using (42) gives 340.134 μV_{pp} for the first stage and 138.948 μV_{pp} for the entire circuit. Comparing these results to the 61 µV resolution of the 16-bit ADC shows that the second stage filter provides almost two extra bits of resolution, which equates to 610 pA lower resolution.

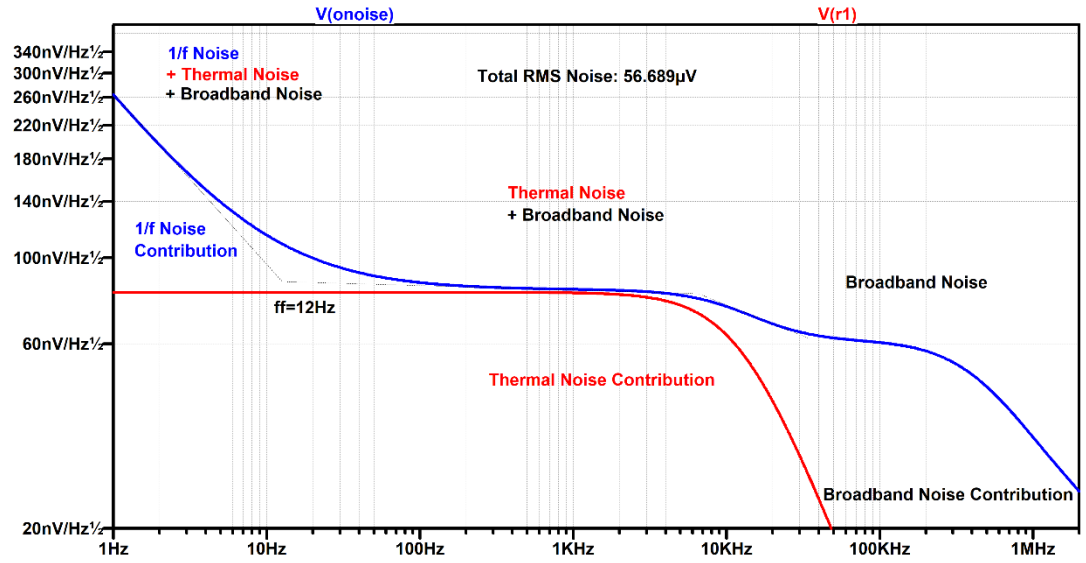

Figure 26. LTSpice Noise Analysis of Stage 1 TIA, Range 1, C_i=100 pF

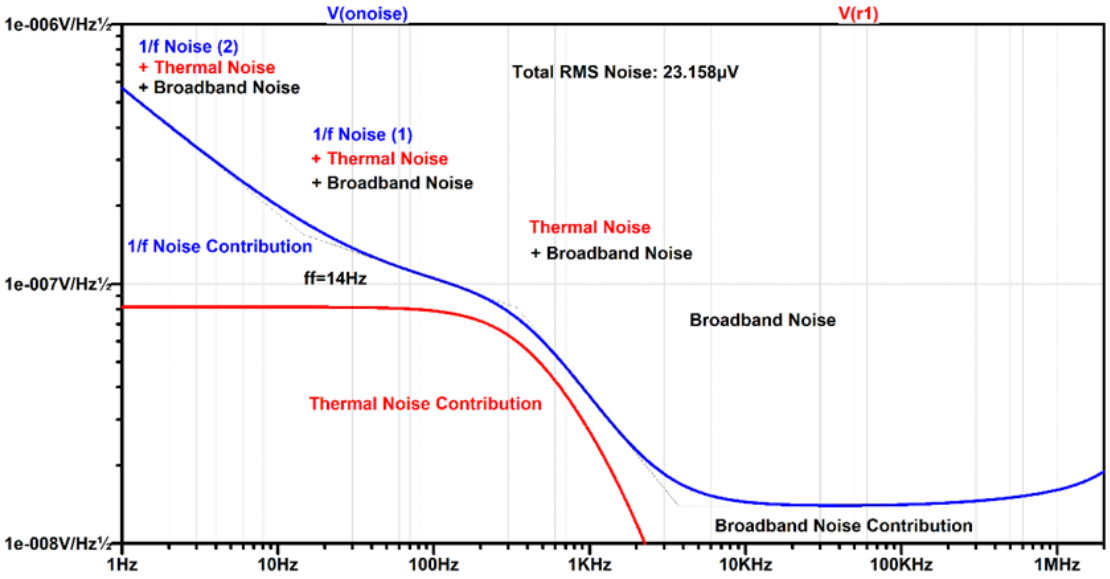

Figure 27. LTSpice Noise Analysis of Stages 1 and 2 MBF, Range 1, C_i=100 pF

Figure 28 and Figure 29 show the total noise voltage output analysis of range two. The total output voltage noise (RMS) was decreased by 36.4% with the addition of the

second stage, again due to the MBF LPF attenuating the noise contributions at higher frequency. Converting each of total RMS noise outputs using (39) shows almost one extra bit of resolution, or 152 pA.

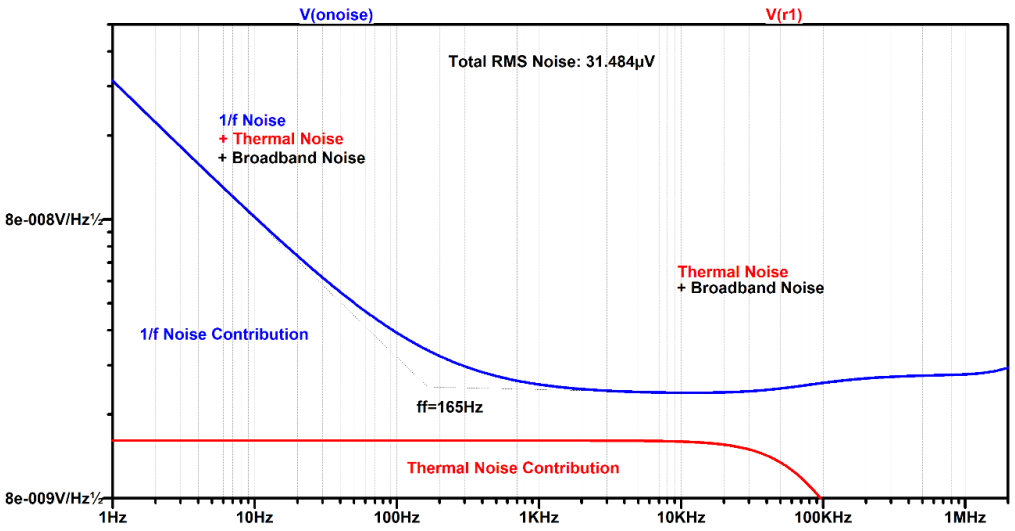

Figure 28. LTSpice Noise Analysis of Stage 1 TIA, Range 2, C_i=100 pF

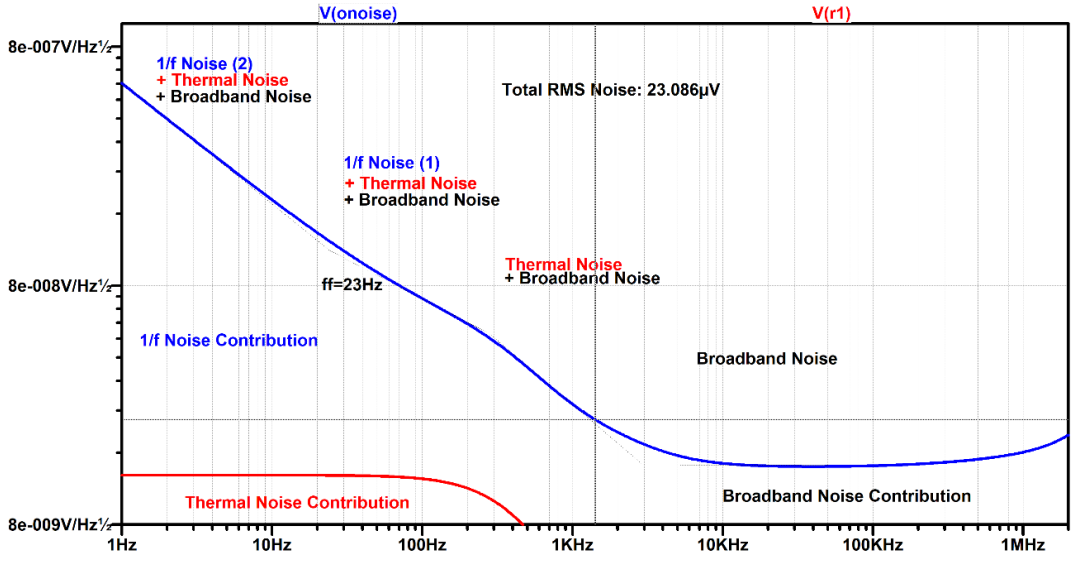

Figure 29. LTSpice Noise Analysis of Stages 1 and 2 MBF, Range 2, C_i=100 pF

3. Circuit Design Prototyping and PCB Design

a. Circuit Design Prototyping

Design prototyping was accomplished by using an 8-lead small-outline integrated circuit (SOIC-8) to dual in-line package (DIP) PCB to interface the surface mounted (SMT) ADA4530-1 packages with a breadboard, shown in Figure 30.

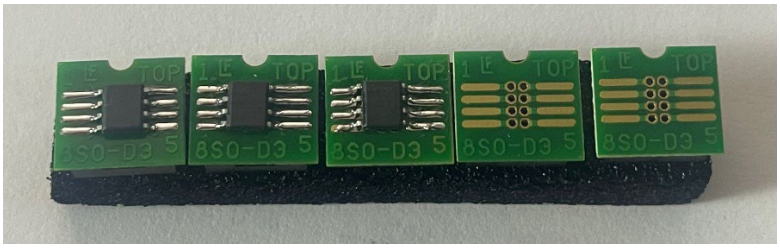

Figure 30. SOIC-8 SMT to DIP PCB with ADA4530-1

Following the conversion of the ADA4530-1 to a DIP package, a breadboard circuit was constructed to test the performance of the circuit design of Figure 23 and Figure 24. A manual push-button switch was used to control ranging. The prototype circuit is shown in Figure 31. To test the dc operation, the stage one input terminals were tied in parallel with large value series resistance, capacitance, and a voltage source in series with a 10 MΩ resistor to act as an effective current source.

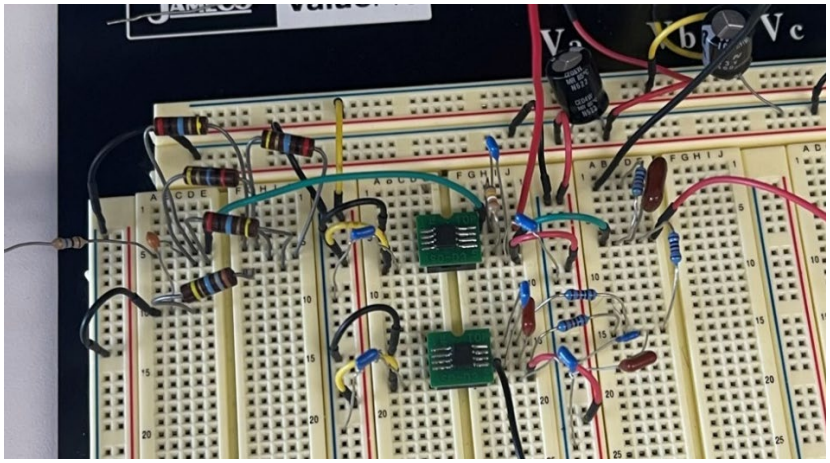

Figure 31. Prototype of LMB

Stage one was tested individually by putting 1 V across the 10 MΩ resistor to create a 1 nA current using the 6 V output of an Agilent E3631A triple power supply. The voltage output from the stage 1 TIA was measured using a Fluke 8846A. The output of -39.797 mV, shown in Figure 32, confirmed the 0.4 mV/nA design specification of the TIA. Following this, the dc operation of both stages was tested by putting 1 mV across the 10 MΩ to create a 100 pA current using a BK Precision 9130B. The measured output of 42 μV, confirmed the sub-nA performance of the circuit under non-ideal conditions.

Figure 32. Stage 1 dc Operation Validation Test

Following the dc tests, a transient stability analysis was performed on the circuit. This was done using an Agilent 33220A to generate a pulse through the measurement circuit and a Keysight DSOX3014T Oscilloscope to monitor the input and output response. Figure 33 and Figure 34, demonstrate a stable response with a 2.5 ms settling time.

Figure 33. Single Pulse Transient Response of Prototype Circuit

Figure 34. Multi Pulse Transient Response of Prototype Circuit

Finally, a frequency analysis was done using an HP3585B to verify the BW and filter performance at each stage and range. A LabView program was designed to control and extract data from the HP3585B, shown in Figure 35, Figure 36, Figure 37, and Figure

38. These results showed BW and filter behavior that was close to the designed performance at each stage and range combination, as shown in the figures.

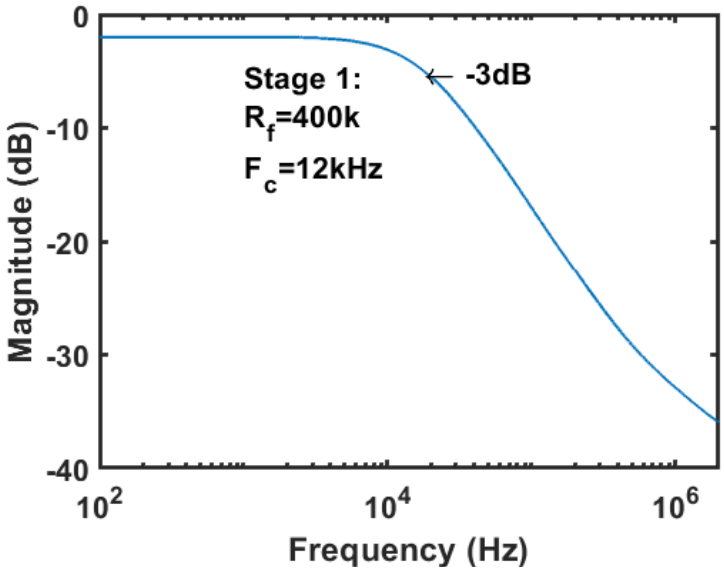

Figure 35. HP3585B Bode Plot of Measurement Circuit: Stage 1, Range 1

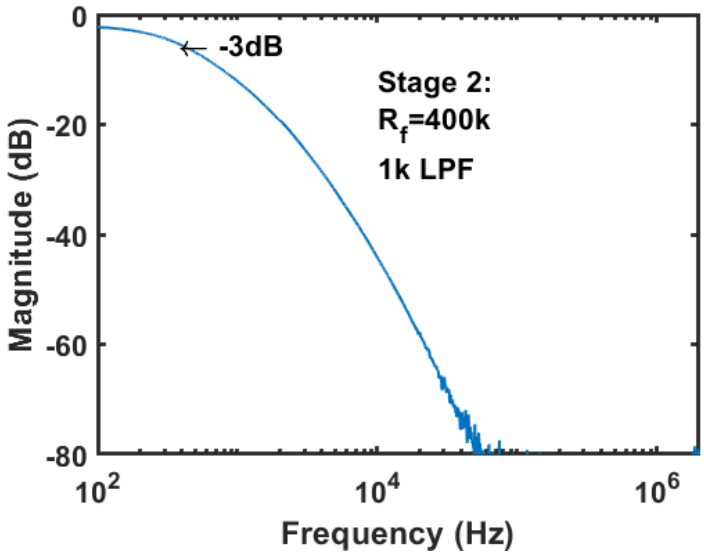

Figure 36. HP3585B Bode Plot of Measurement Circuit: Stage 2, Range 1

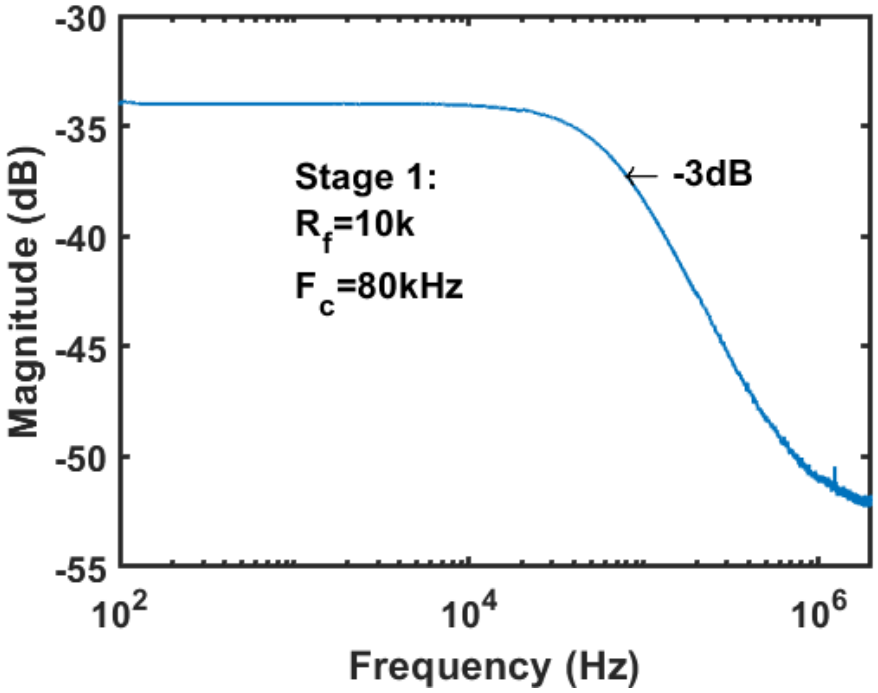

Figure 37. HP3585B Bode Plot of Measurement Circuit: Stage 1, Range 2

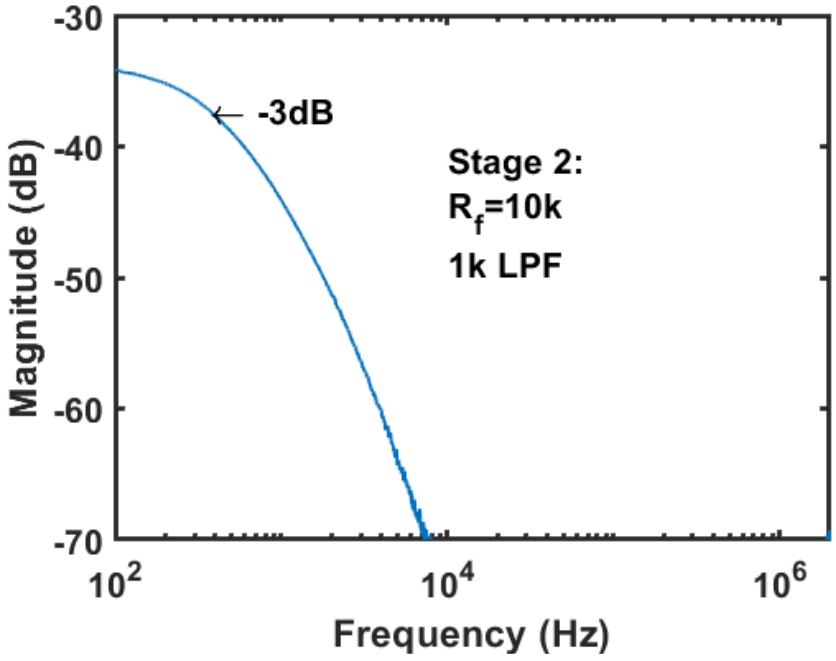

Figure 38. HP3585B Bode Plot of Measurement Circuit: Stage 2, Range 2

b. LMB Board Layout and PCB Design

Because modularity was one of the most important requirements for this subsystem, the PCB was designed to take advantage of as much of the operational range of the ADA4530-1 as possible. The design incorporates numerous ultra-low leakage mitigation techniques and best practices which are inspired by those found in various electrometer and other sensitive high input impedance designs, as well as those mentioned in its data sheet [19], [25], [27]. The PCB was designed using the EAGLE electronic design automation (EDA) software, Figure 39 and Figure 40 show the overall EAGLE schematic and PCB layout.

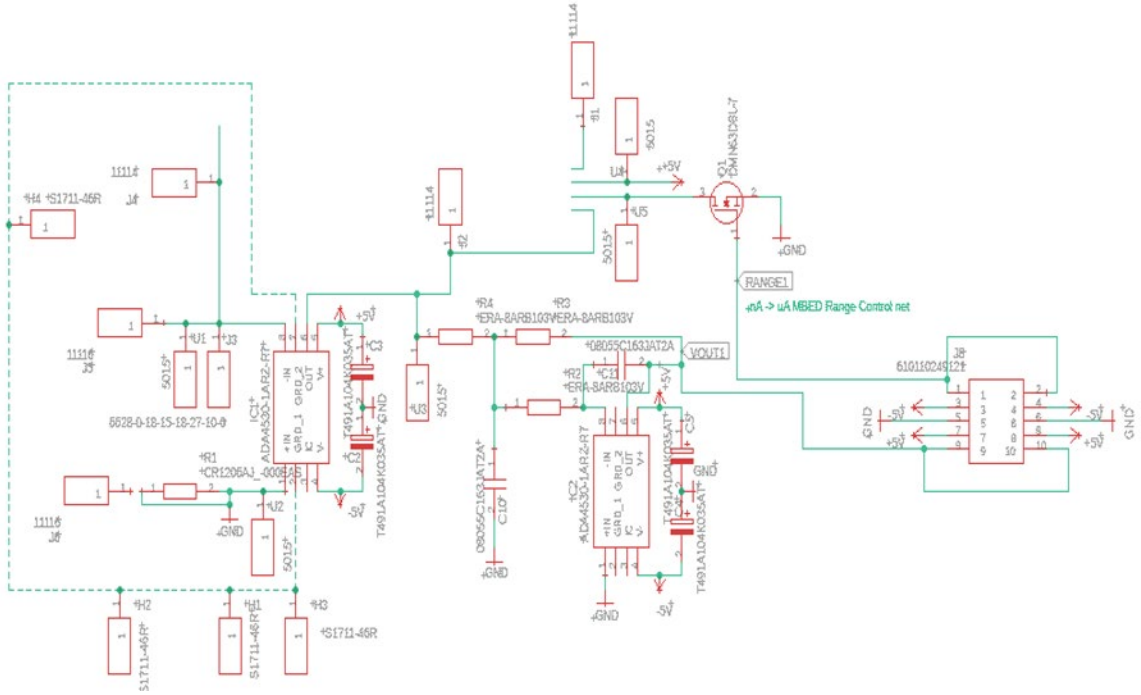

Figure 39. EAGLE LMB Schematic

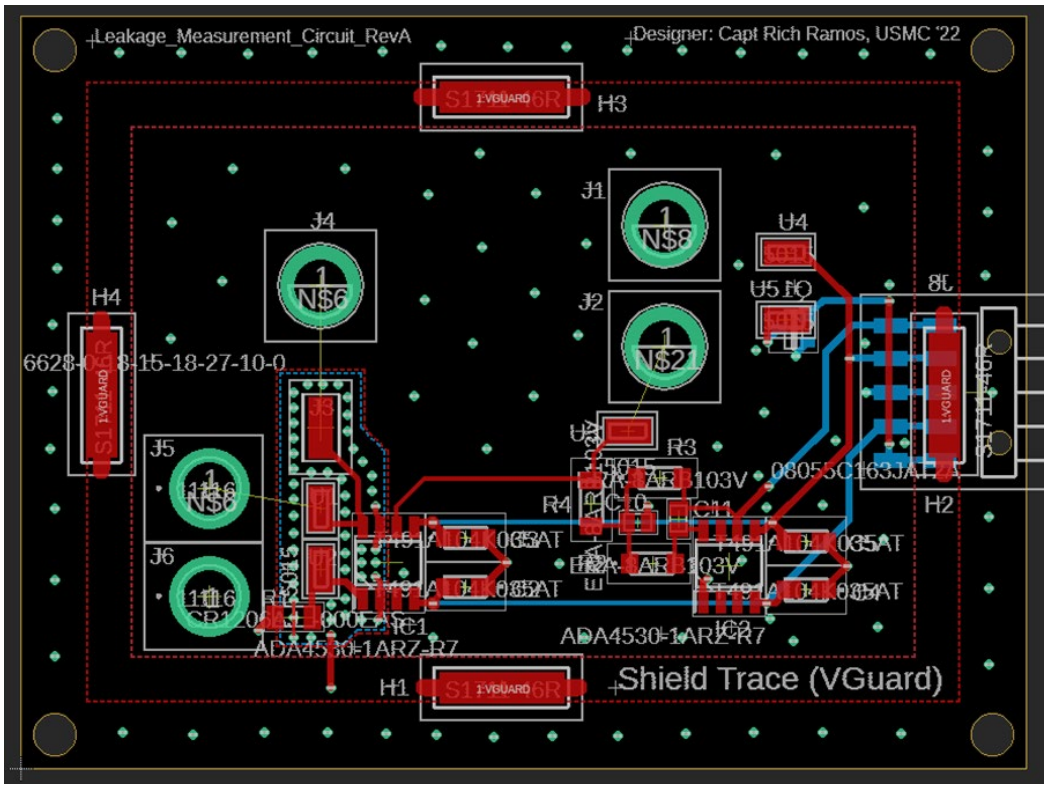

Figure 40. EAGLE LMB Layout

The LMB PCB consists of a four-layer design with key features such as: a four-layer isolated guard plane, surrounded by a fence of vias connected to each layer which minimize lateral leakage through the board; a guard trace, connected to the guard plane, that drives an aluminum electromagnetic interference (EMI) shield to the same potential as the input; multiple polytetrafluoroethylene (PTFE) insulated terminals, used to isolate the sensitive high impedance components from potential leakage paths; and stitched ground vias that provide short return paths to reduce large inductive ground loops.

The first layer, Figure 41, contains a ground plane, isolated guard plane, shield trace, and routed signals and power. Layers two and three, Figure 42, are simply identical dedicated ground planes which provide uncoupled return paths for the electric fields on the top and bottom of the board. Layer four, Figure 43, consists of a ground plane, routed signals and power, and the connector used to interface with the DAQ board.

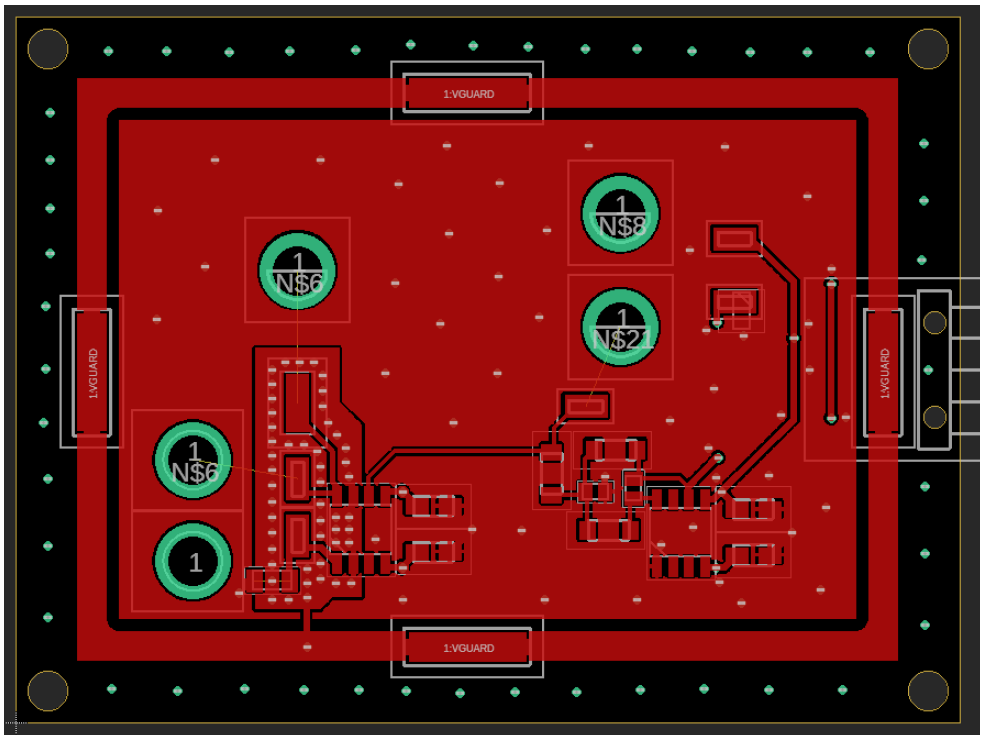

Figure 41. Layer 1 of LMB

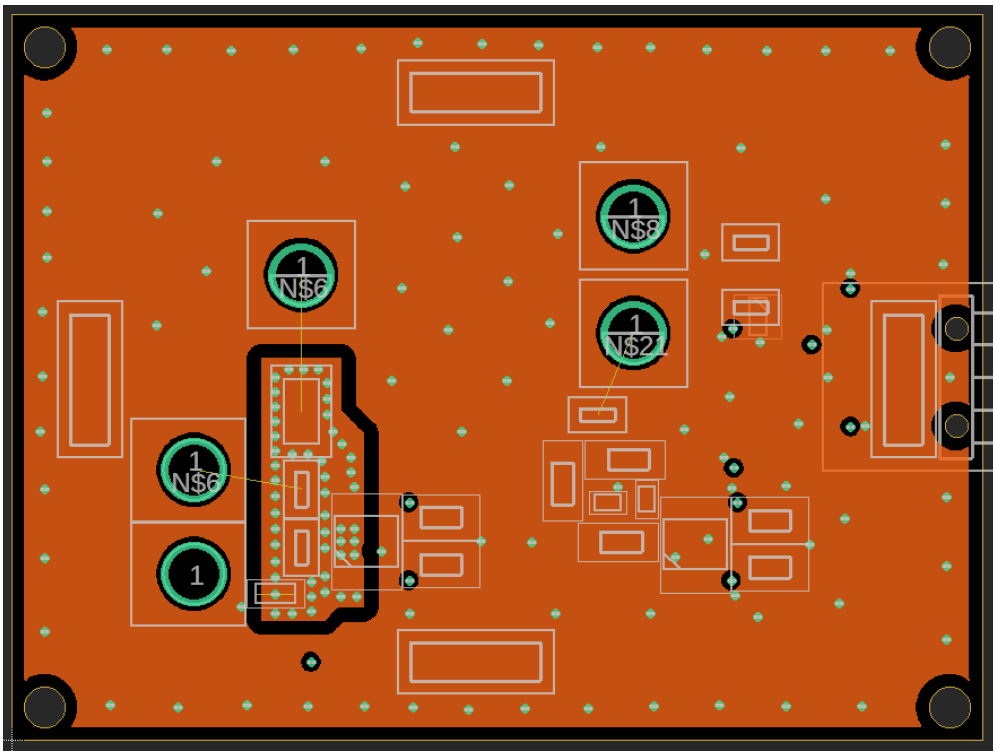

Figure 42. Layer 3 of LMB

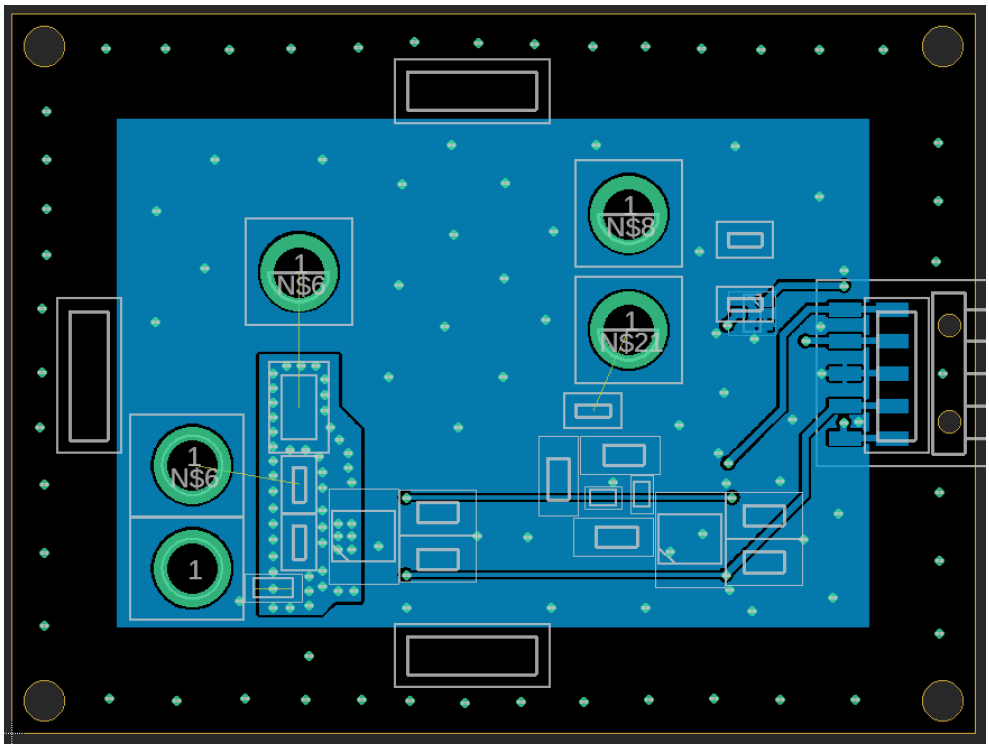

Figure 43. Layer 4 of LMB

Finally, Figure 44 shows the final LMB PCB with each of the key components highlighted. The first ADA4530-1, configured as an inverting TIA, is represented by (a.1) where (b) and (c) correspond to both feedback impedance ranges, which is controlled by (d). The second ADA4530-1, configured as an inverting MFB LPF, is represented by (a.2). The PTFE turrets to the left of (a.1) act as the input terminals which extend to the underside of the board, allowing for an isolated connection from the DUT to the TIA. The guard plane and via-fence are used to protect these sensitive input terminals and isolate the input and output terminals of the TIA. The other PTFE turrets are located on each side of the feedback components, allowing them to be air-wired above the board, further minimizing leakage paths. Finally, surrounding the board is a guard trace that is connected to each of the four shield clips which drives the aluminum EMI shield to the same potential.

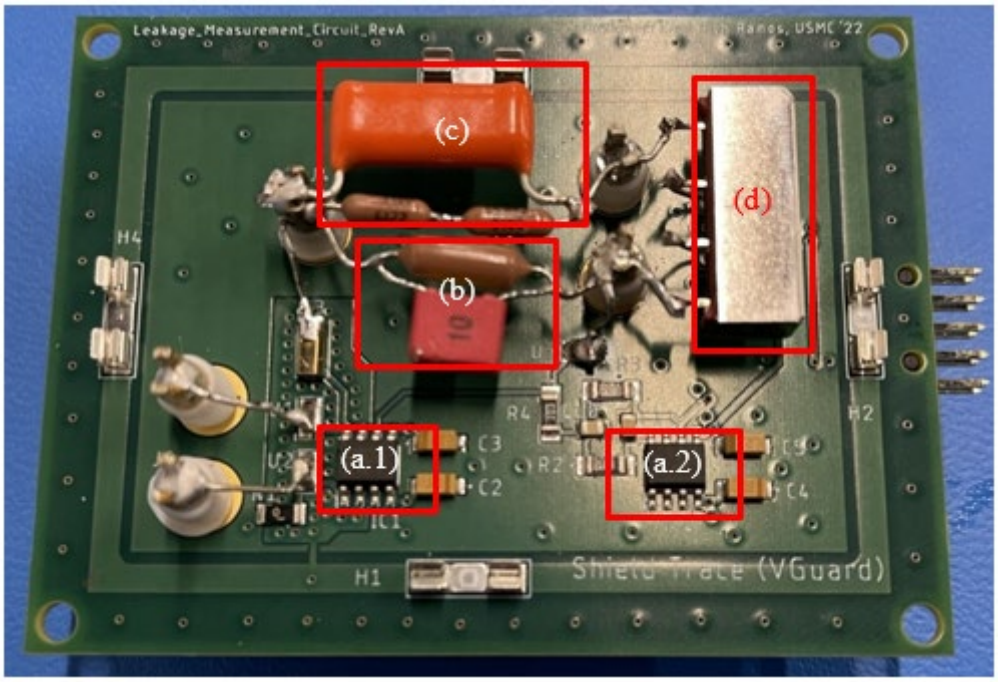

Figure 44. LMB: (a.1) TIA, (a.2) LPF, (b) $C_{f1}||R_{f1}$, (c) $C_{f2}||R_{f2}$, (d) Relay

C. DESIGN OF DAQ BOARD

1. Component Selection

The DAQ board was designed around the AD974, a 4-channel, 16-bit, 200 kSPS ADC [28]. This device was chosen due to its modularity, primarily related to the variety of internal features and input ranges that it supports, shown in Figure 45. An ADC was needed that could quickly control and sample up to four DUTs at a time, while still maintaining enough bandwidth to support rapid data acquisition. The 200 kSPS of the AD974 supports the bandwidth needed to average the data of four separate DUTs, while still maintaining a high level of fidelity.

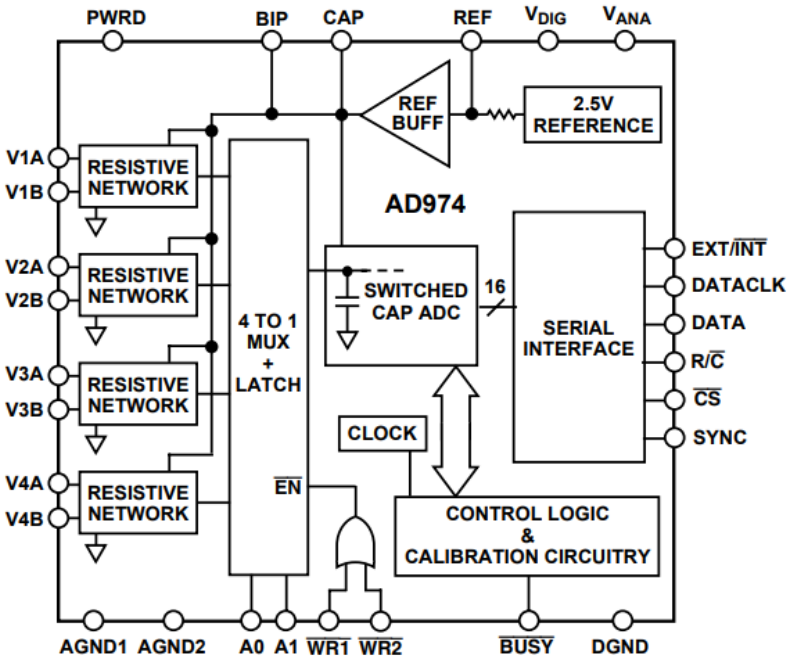

Figure 45. Functional Block Diagram of AD974. Source: [28].

2. Configuration and Control of ADC

The ADC was configured to operate on the 4 V input range, allowing for the highest resolution per quantization level of the 16-bit ADC. Data communication occurs using an external clock signal provided by the Mbed to the DATACLK pin via a Serial-Peripheral-Interface (SPI) connection. EXT/INT is held high, indicating that an external clock is being referenced. With the multiplexer write inputs WR1 and WR2 tied low, the multiplexer becomes transparent, all channel selection is controlled by A1 and A0, whose truth table is shown in Figure 46.

A1	A0	Data Available from Channel
0	0	AIN 1
0	1	AIN 2
1	0	AIN 3
1	1	AIN 4

Figure 46. AD974, A1 and A0 Truth Table

With the chip select input CS tied low, a falling edge on the read/convert input R/C starts a data conversion. A falling edge on R/C also sets the BUSY output low until the data conversion is complete, preventing the initiation of any other data conversions. The timing diagram for this configuration of the AD974 is shown in Figure 47.

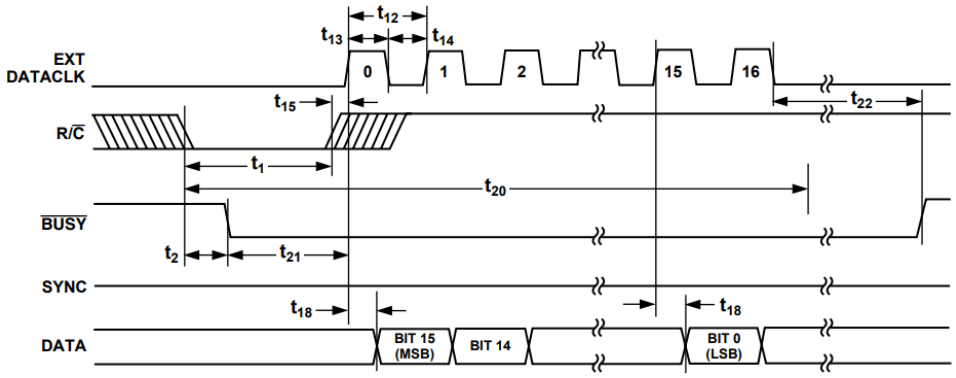

Figure 47. AD974 Timing Diagram for Data Conversion. Source: [28].

3. DAQ PCB Layout and PCB Design

The DAQ PCB was also designed with modularity and flexibility in mind. The primary design requirements of the DAQ Board called for the ability to power, control, and measure up to four LMBs. This design was able to achieve that using four surface mounted connectors and a mezzanine style board system which stacked the LMBs atop one another. The DAQ board also houses the Mbed which provides control and measurement of both the AD974 and LMBs via channel and range selection, respectively. The DAQ Board also features two 4-pin I^2C connectors above the Mbed, for future integrations, and an 8-pin digital IO interface below the Mbed for future switch matrix integration. The EAGLE schematic of the DAQ Board is shown in Figure 48.

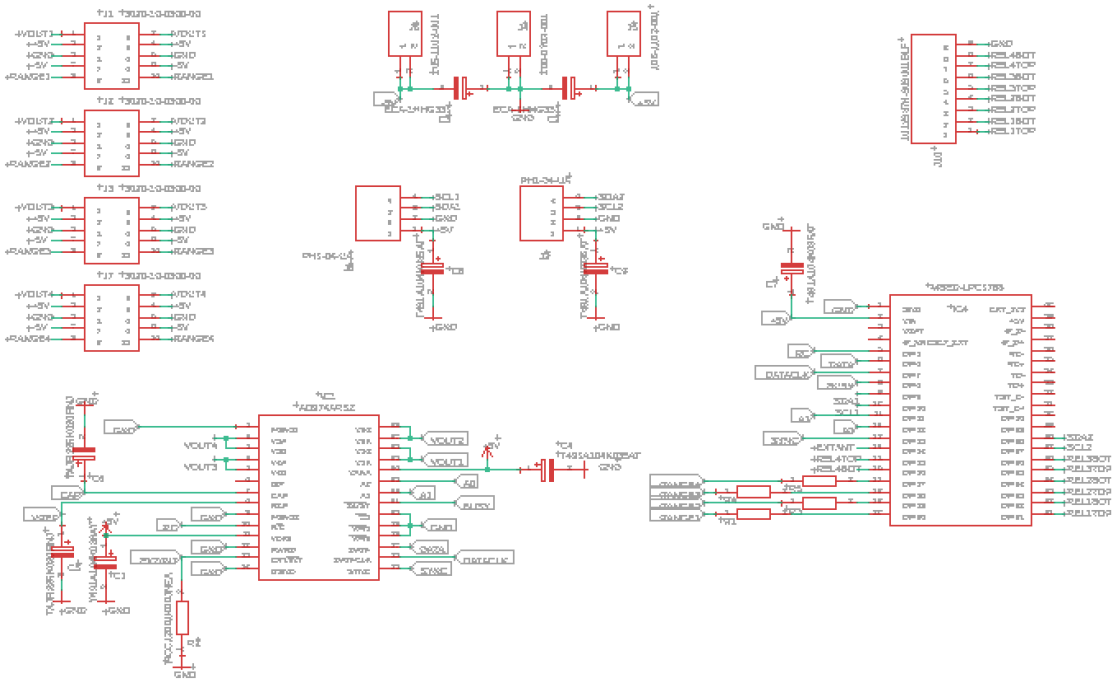

Figure 48. EAGLE DAQ PCB Schematic

The DAQ PCB, Figure 49, consists of a simple two-layer design utilizing ground planes and routed power, signal, and data traces. Bulk filtering capacitors are used at the power rails and various bypass capacitors are used close to the IC to filter high frequency transitions and provide local charge storage. Less ground stitching was utilized in this design, simply to prevent cross talk between traces and minimize inductive ground loops.

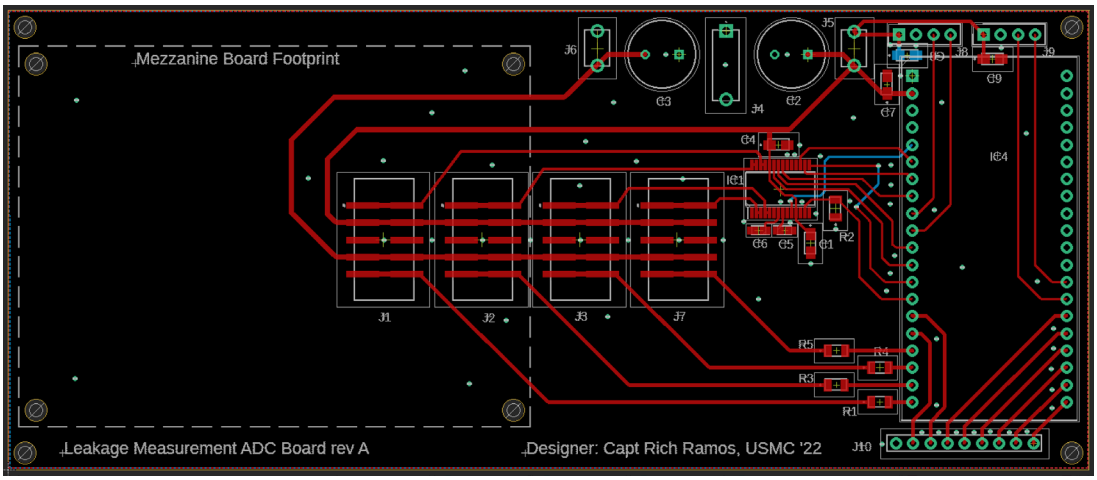

Figure 49. EAGLE DAQ PCB Layout

D. MBED MICROCONTROLLER

The Mbed LPC1768 Microcontroller was chosen due to its availability and reliable performance in each of the previous HTOL system designs. Its C/C++ based RTOS, multithreading capability, and multitude of communication interfaces is ideal for controlling multiple sub-systems, while also performing on-board data processing.

1. SPI Interface with AD974

A modified SPI interface was established between the AD974 and Mbed using pins 5–7, shown in Figure 50. Pin 5 was connected to RC, which controlled the reading and conversion of data from the AD974. Pin 8 was used to monitor the BUSY output from the AD974. Pins 11 and 12 were used to control the channel selection, as defined in Figure 46. Finally, pin 14, connected to EXT/INT communicated the chosen clock to the AD974. The SPI connection was configured in a 16-bit, mode 3, format with a 10 MHz clock.

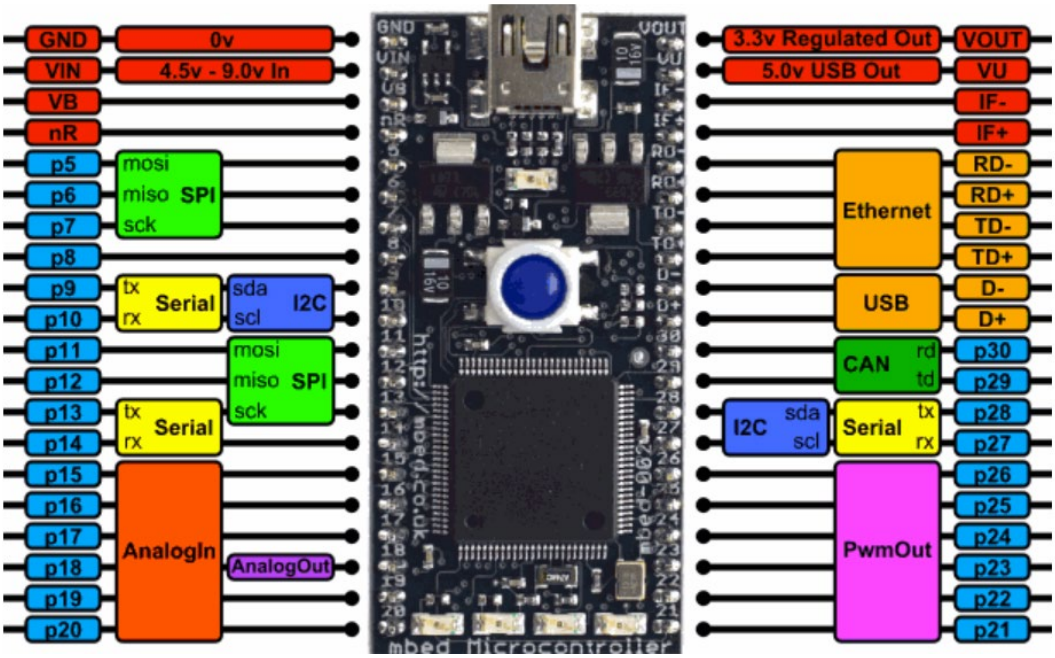

Figure 50. Mbed LPC1768 Pinout Diagram. Source: [29].

2. Programming of Microcontroller

The Mbed LPC1768 was programmed using the Mbed Studio integrated development environment (IDE) program which supports the proprietary Mbed OS 6 RTOS. It is connected to a computer via a Micro Universal Serial Bus (USB) connection. The Mbed program, shown in Appendix A, establishes a serial terminal connection with a LabVIEW Virtual Instrument (VI) program, shown in Appendix B, running on a computer, at a baud rate of 115.2 kbps. The Mbed also performs a nontrivial amount of onboard data-processing via the conversion of quantized values to their associated current value and sample averaging, to include sampling by an adjustable number of power line cycles (NPLC) to filter the zero-mean 60 Hz power line noise from the data.

IV. SYSTEM TESTING AND DATA ANALYSIS

A. SYSTEM TESTING

Testing and validation of the LoSPRaDC system was accomplished by using a B1505A semiconductor parameter analyzer with pA current resolution to generate a fixed-interval voltage sweep across a device while the LoSPRaDC measured the current at the low side. A LabView VI was designed to control the voltage output of the MPSMU module on the B1505A, while also recording its output voltage and current; control the LoSPRaDC, while also recording its measured current; and create a data output with each of the three recorded parameters, while also displaying the I-V plots within the VI. This data was used to create an overlay of I-V plots using the recorded measurements from the B1505A and the LoSPRaDC. This data was then used as a reference to determine the performance of the LoSPRaDC and calibrate it as needed. Figure 51 and Figure 52 show the block diagram and the test system setup it, respectively, where the power supply represents the HP E3631A, which was used to provide the ±5 V power rails needed to run the LoSPRaDC, as well as the third channel needed to test three-terminal devices; the module selector represents the Keysight N1258A, which was used to select the various modules on the B1505A; and the uninterrupted power supply (UPS) represents the common power and ground points for the entire testing system.

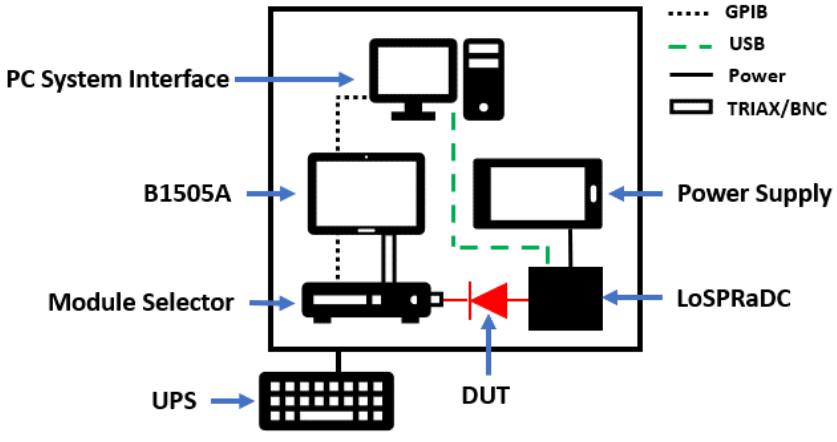

Figure 51. Block Diagram of LoSPRaDC Testing System

The PC System Interface was obscured by (a) in Figure 52. The PC interface consisted of a Lenovo P52S workstation that was used to run the LabView VI and save the testing data.

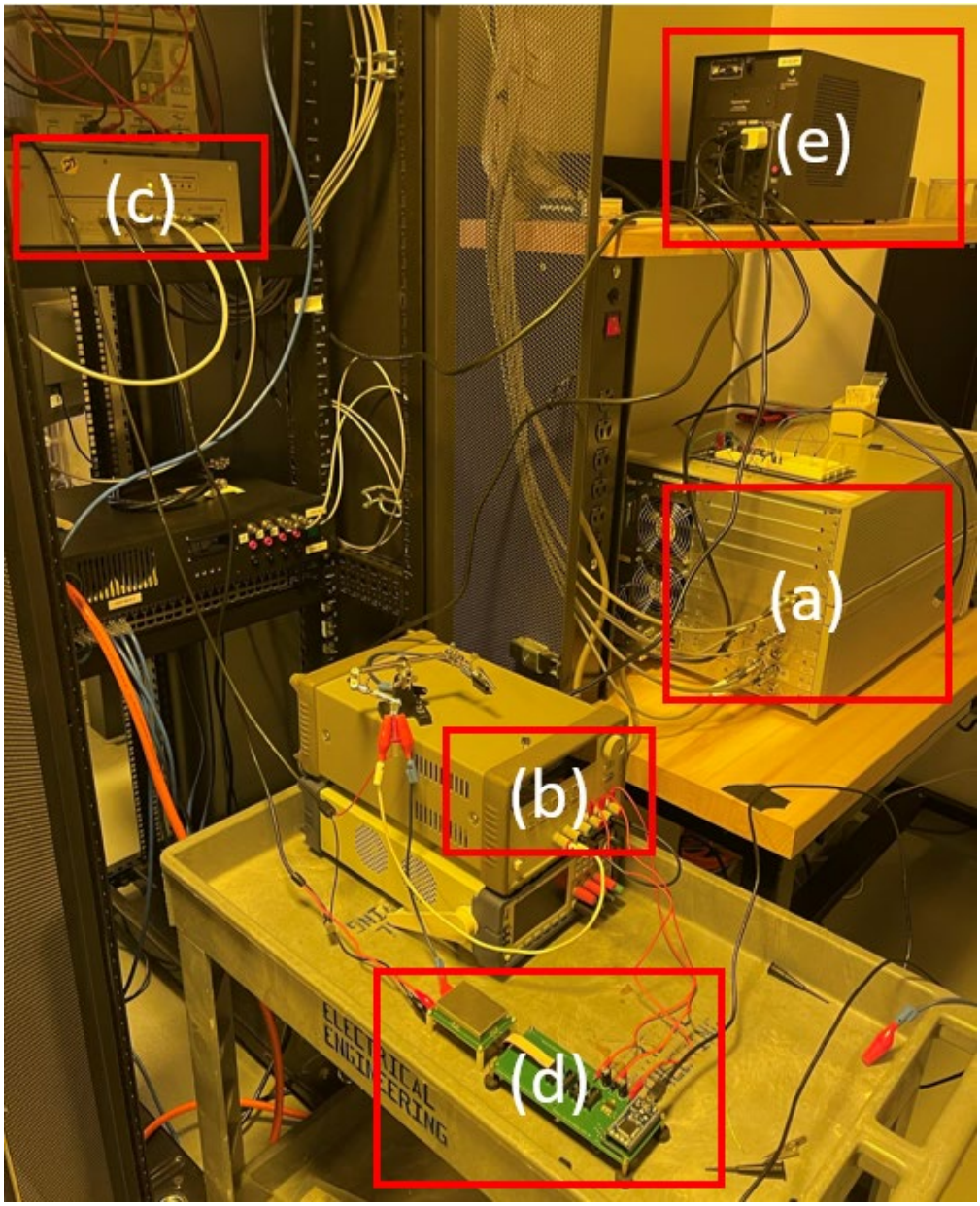

Figure 52. Test System Setup: (a) B1505A, (b) Power Supply, (c) Module Selector, (d) LoSPRaDC, (e) UPS

B. SYSTEM CALIBRATION

The primary parameters targeted for the calibration of the LoSPRaDC system were the offset current error and the error in the assume feedback resistance values. All LoSPRaDC system calibrations were handled programmatically. This was done by adjusting calibration parameters in the Mbed OS software program used to control the system. The initial calibration focused on correcting the offset current through the open-circuit output offset of the system until a zero-mean output was achieved. Next, the system was supplied a constant current and offsets were adjusted iteratively until the next digit of precision was found. This process yielded a maximum raw current resolution of ±300 pA, which corresponded to an error of one least significant bit (LSB). Next, averaging was implemented as a function of samples and NPLCs. After optimizing, calibrations were re-done for the remaining sampling rate and NPLC combinations. This process yielded an optimized resolution of ±20 pA when using 3000 or 6000 samples-per-second (SPS) and two NPLCs, shown in Figure 53.

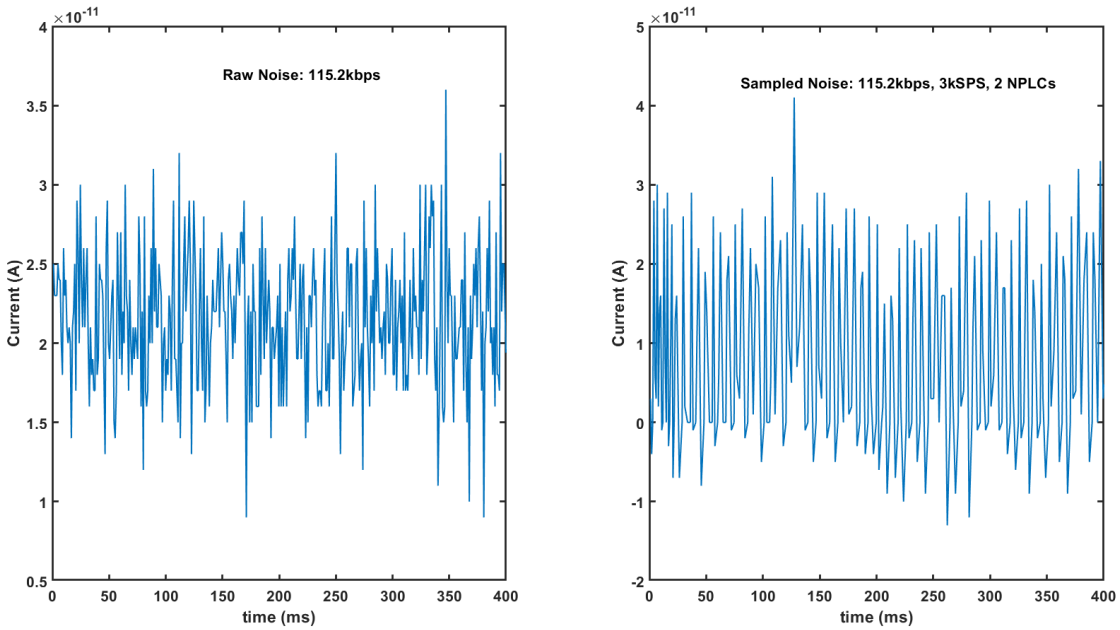

Figure 53. Noise Samples Collected from LoSPRaDC

Four sampling rates were chosen for final calibrations prior to device testing, 2 through 4 kSPS, and 6 kSPS. Calibration of the programmed feedback resistance, R_f, values used to estimate current within the microcontroller program was done by analyzing the linear I-V plots of a resistor, measured simultaneously by the LoSPRaDC and the B1505A, an example of which is shown in Figure 54.

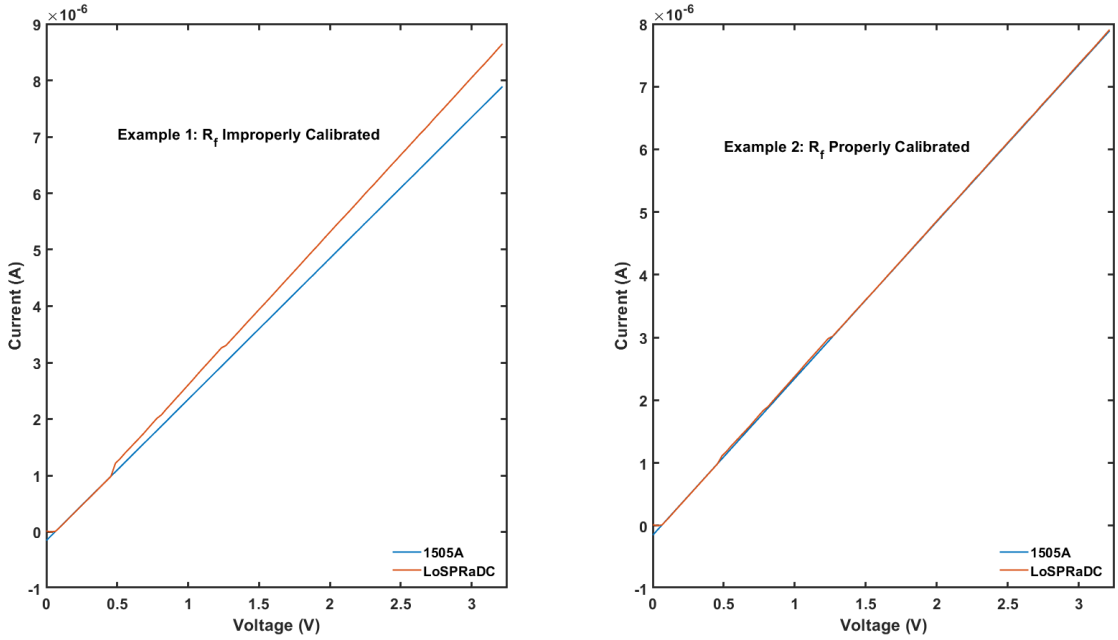

Figure 54. R_f Calibration Example

C. SYSTEM VALIDATION

The methodology for system validation was to begin by testing the I-V characteristics of devices that produced small currents, or leakage currents, at a low-voltage bias. Validation testing then expanded to I-V testing of devices of increasing complexity, voltage ratings, and variable leakage current magnitude. The validation testing was also repeated for multiple system sampling and averaging rates to allow for more comparison of results and varying performance levels. The following sections provide the validation data produced from each of the various device tests, presented in the order they were tested.

1. Resistor Tests

The first validation test was done on a 400 kΩ, 0.1% precision resistor, identical to the one being used for R_f in stage one. Because of the simplicity of this device, only two sampling rates were fully tested, shown in Figure 55 and Figure 56. Figure 57 shows a comparison of the full voltage sweeps for each of the sampling rates. Each of the tests consisted of three voltage sweeps across consecutive ranges along with a single cumulative voltage sweep across the entire range at once.

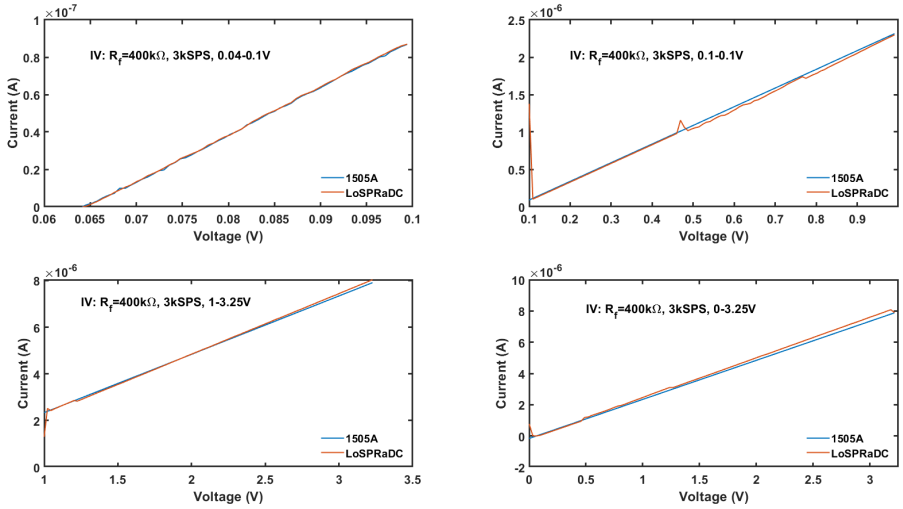

Figure 55. 400 kΩ Resistor IV Plots, 3 kSPS

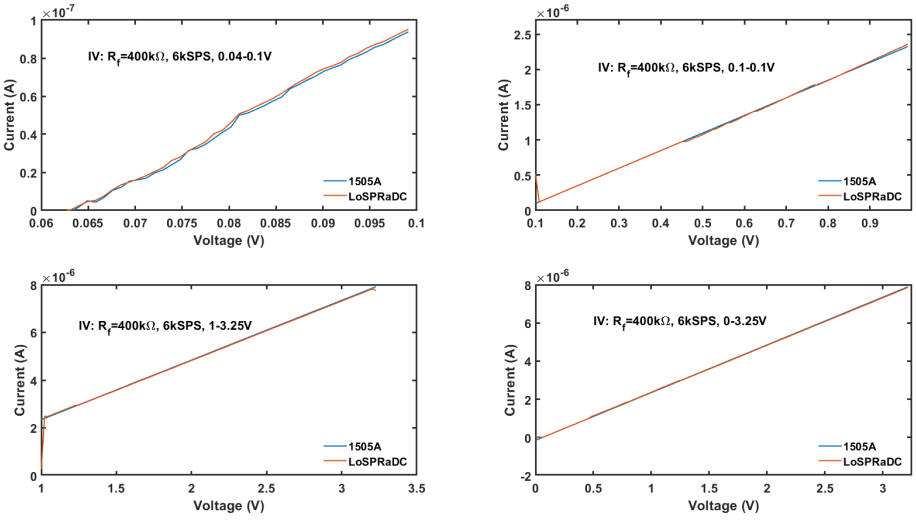

Figure 56. 400 kΩ Resistor IV Plots, 6 kSPS

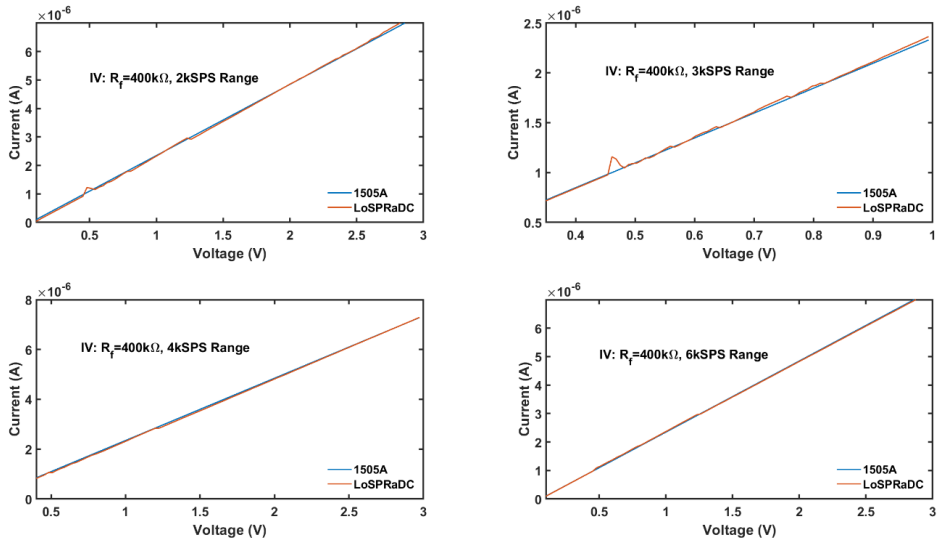

Figure 57. Full 400 kΩ Resistor IV Plots of All Sampling Ranges

Resistor validation tests were conducted with 0 V to 3 V sweeps across all ranges. Maximum deviation was ±2 nA in range one and ±200 nA in range two, these results confirm the calibrations at each sampling range were successful. Higher sampling rates resulted in marginally decreasing error between the B1505A and the LoSPRaDC measurements.

2. Zener Diode Tests

Validation testing was then done on two Zener diodes with 8.7 V and 28 V Zener voltages. These devices were chosen to validate the ability of the LoSPRaDC to measure a device experiencing a breakdown voltage. These devices were specifically chosen for their breakdown voltages below the voltage limitations of the B1505A MPSMU. The devices were tested across four sampling ranges, with four voltage sweeps in each.

a. 1N5238B-T 8.7V 0.5W

The anode of the 1N5238B-T was attached to the input terminal of the LoSPRaDC, its cathode was attached to the B1505 force high terminal, and the B1505 force low terminal was attached to the ground input of the LOSPRaDC. Multiple reverse-bias voltage sweeps were performed from 0 V to 3 V, 3 V to 7 V, 7 V to 9 V, and 0 V to 9 V across

each of the four sampling ranges. The results of these tests are shown in Figure 58, Figure 59, Figure 60, and Figure 61.

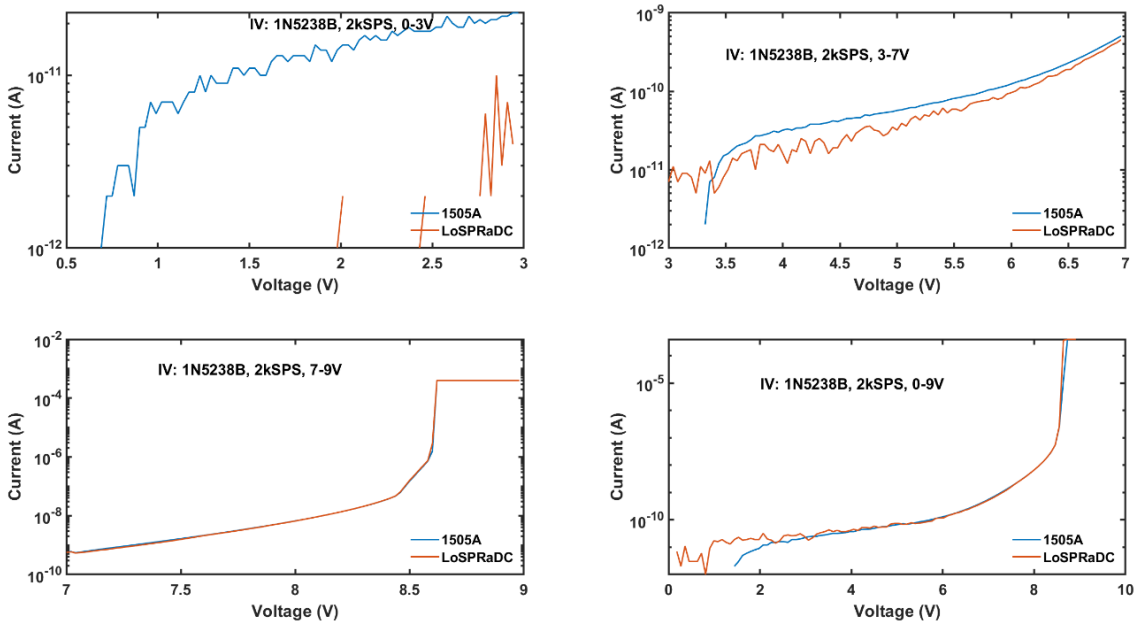

Figure 58. 1N5238B Zener IV Plots, 2 kSPS

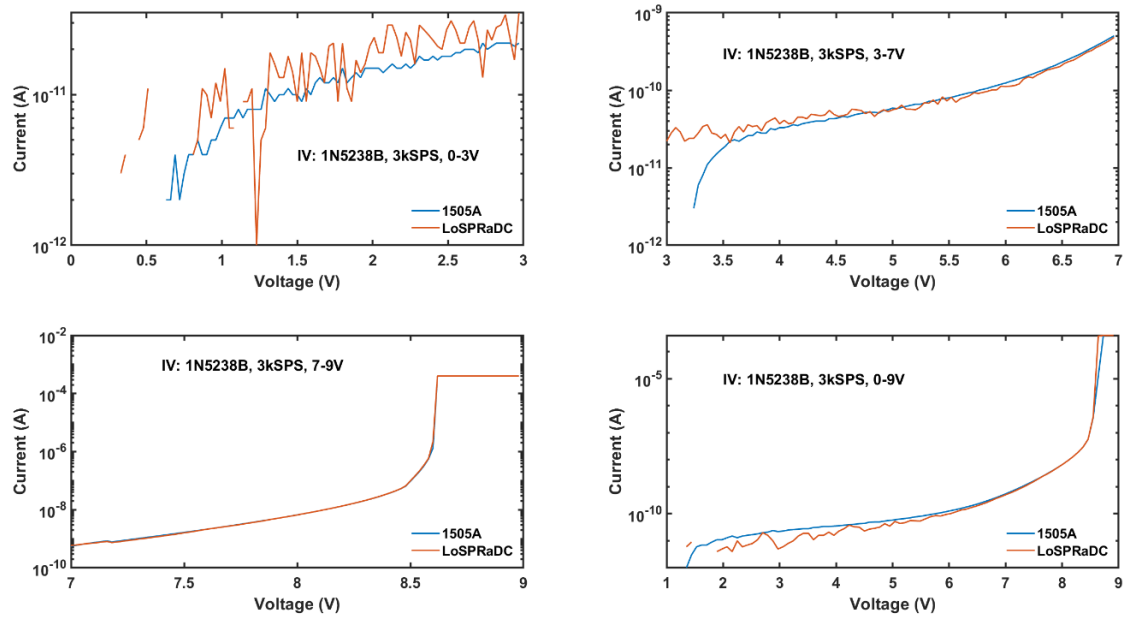

Figure 59. 1N5238B Zener IV Plots, 3 kSPS

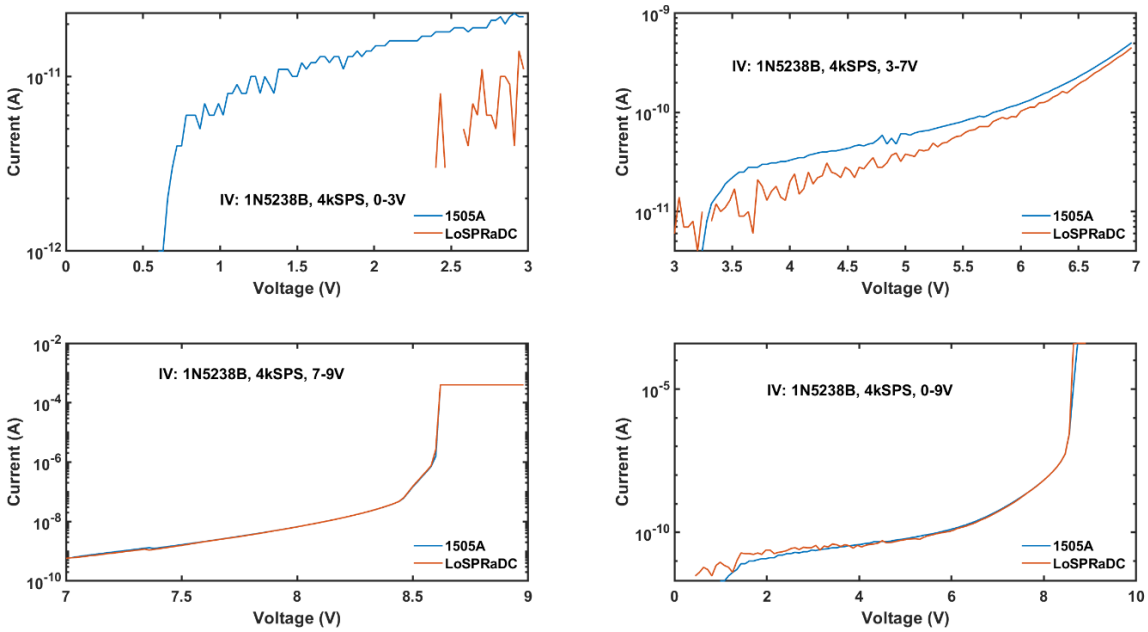

Figure 60. 1N5238B Zener IV Plots, 4kSPS

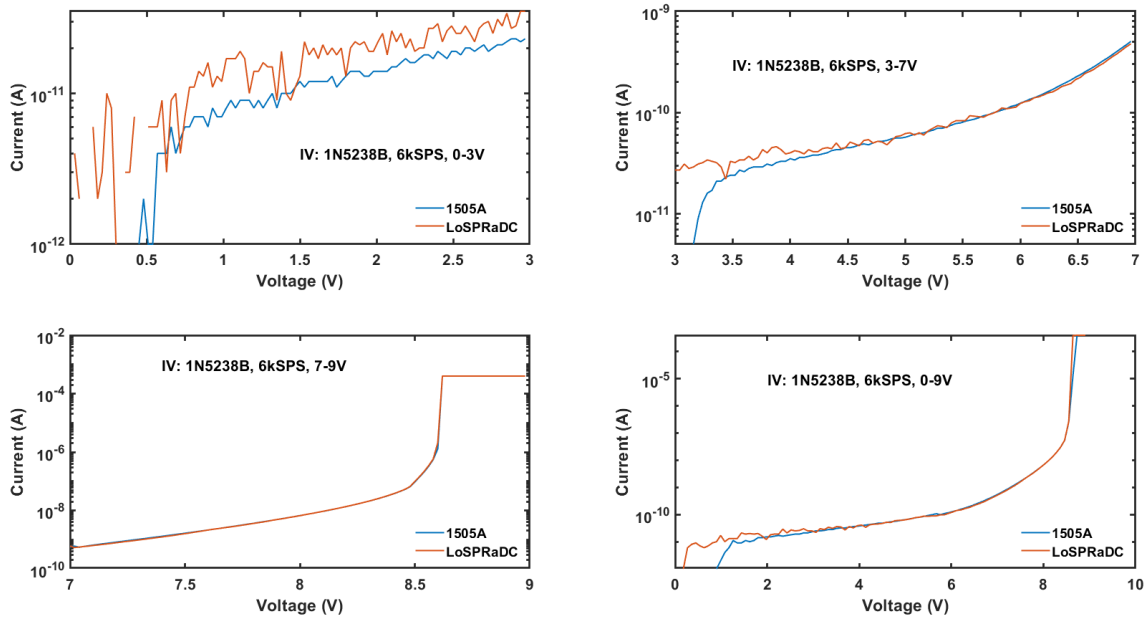

Figure 61. 1N5238B Zener IV Plots, 6 kSPS

During these reverse-bias sweeps, leakage currents were measured from 1 pA at 0.4 V to 400 µA at 9 V in Figure 61. The lowest leakage current measured was 1 pA at 6 kSPS, shown in the 0 V to 0.1 V and 0 V to 9 V plots in Figure 61. In the pA to µA range,

the average measurement error between the B1505A and LoSPRaDC was approximately 20 pA across all sampling ranges. Above 1 µA, only one useful datapoint exists between the switching point and the compliance limit; therefore, an adequate conclusion cannot be drawn on current error in this range. Figure 61 show the effectiveness of higher sampling when the measurements at lower current are compared with those of the lower sampling rates. Higher sampling increases the probability that the final averaged current value will be greater than zero.

b. 1N5255B 28V 0.5W

An 1N5255B Zener diode was attached to the LoSPRaDC and multiple reverse-bias voltage sweeps were performed from 0 V to 10 V, 10 V to 25 V, 25 V to 30 V, and 0 V to 29 V, for each sampling range. The results of these tests are shown in Figure 62, Figure 63, Figure 64, and Figure 65.

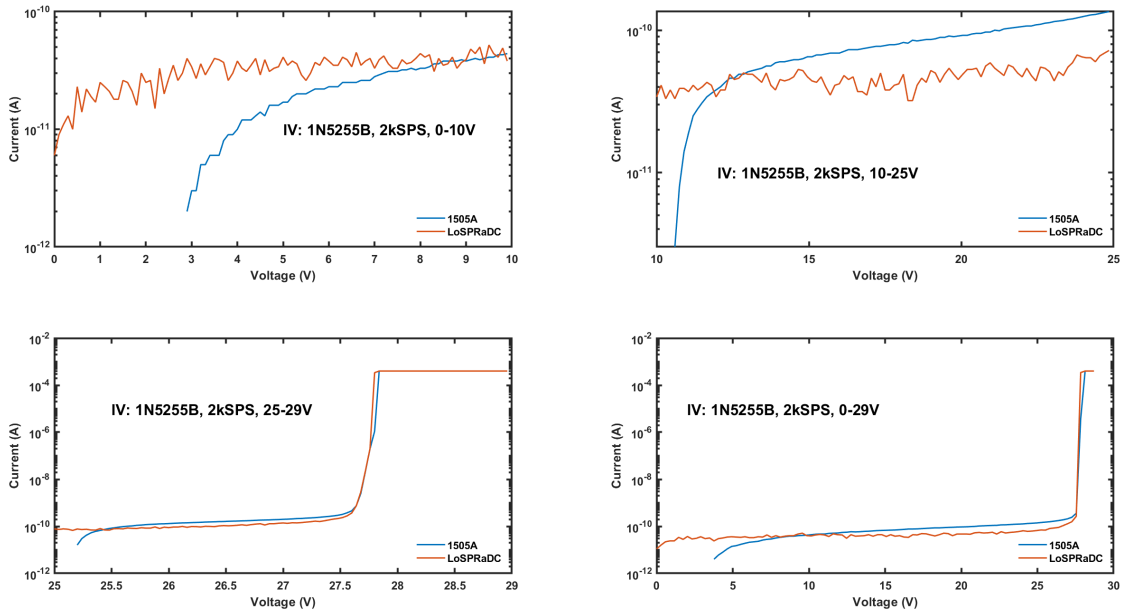

Figure 62. 1N5255B Zener IV Plots, 2 kSPS

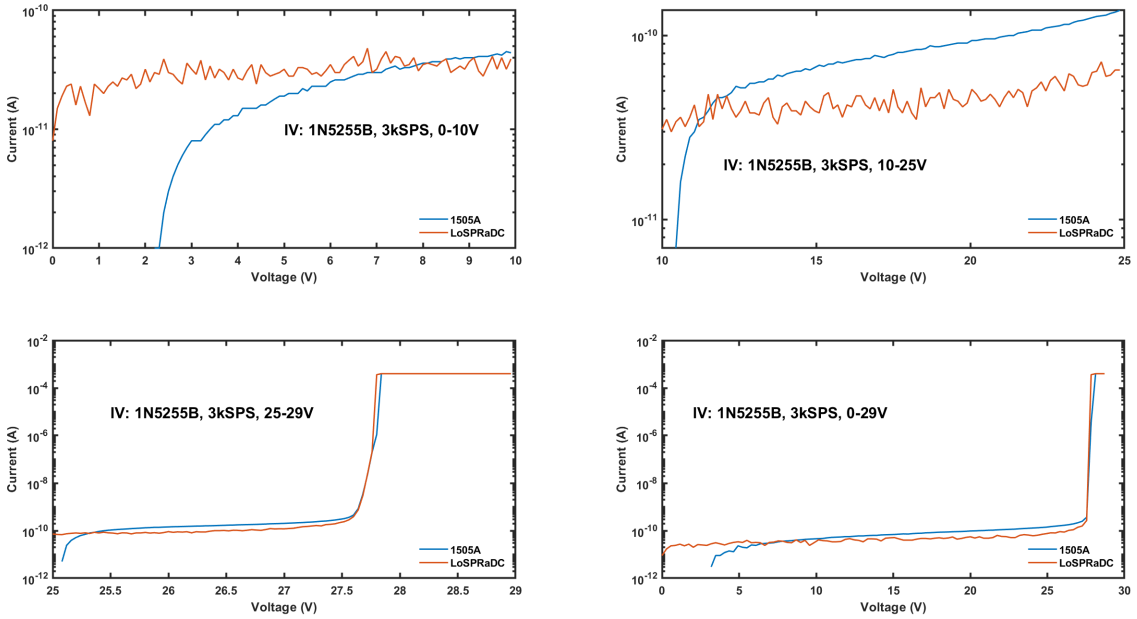

Figure 63. 1N5255B Zener IV Plots, 3 kSPS

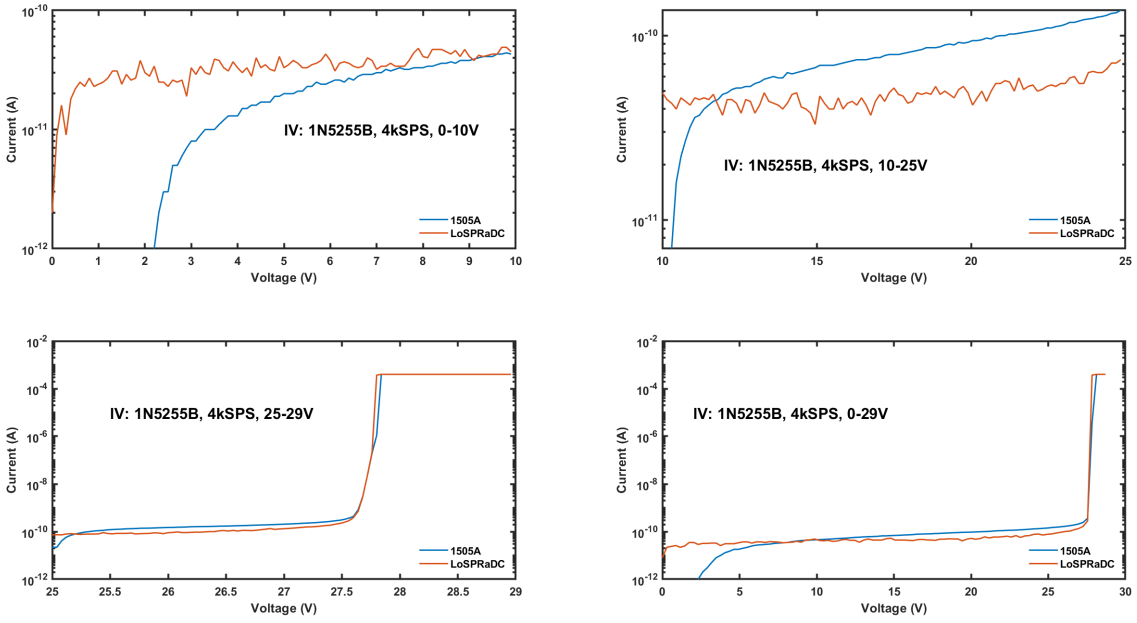

Figure 64. 1N5255B Zener IV Plots, 4 kSPS

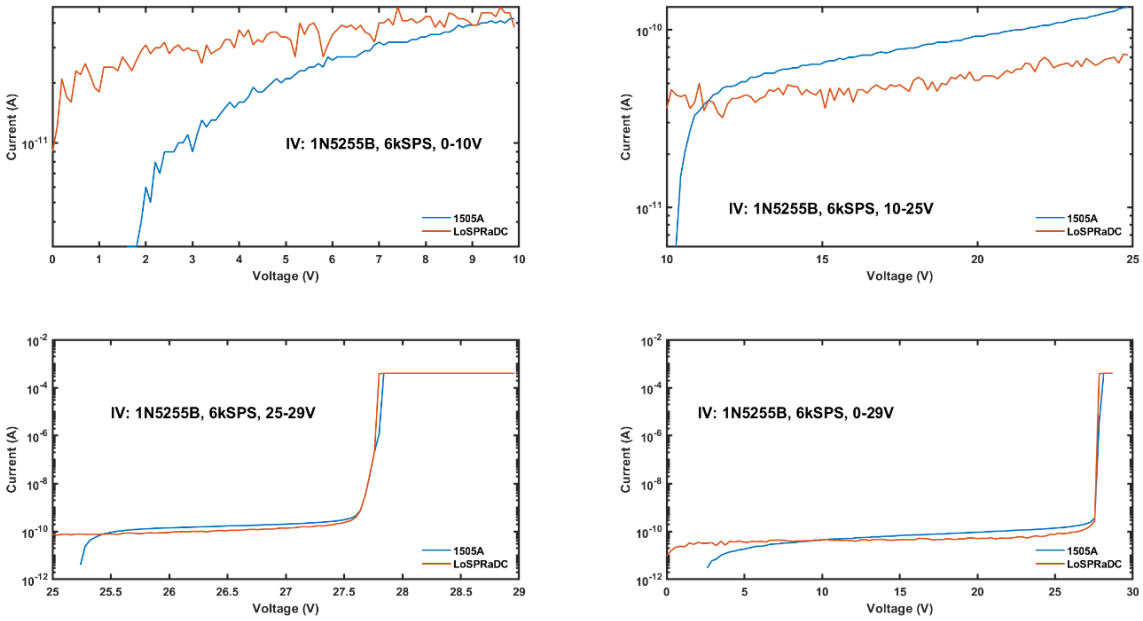

Figure 65. 1N5255B Zener IV Plots, 6 kSPS

The results of these tests validated the ability of the LoSPRaDC to measure the leakage current of a device up to its breakdown voltage. Figure 65 shows that the system was able to resolve 10s of pA. This is well below the range the LoSPRaDC was designed to measure. Figure 58, Figure 59, Figure 60, and Figure 61 show that some data was removed during post-processing due to negative current values that could not be plotted logarithmically, this was the case for both the B1505 and the LoSPRaDC. Like the first device, resolution improved marginally with increasing sampling rates. Comparing the differences in measurement error between 2 kSPS and 6 kSPS showed that higher sampling contributed to an error average reduction of approximately 6 pA.

3. Si Power Diode Test

Next, validation testing was done on a DSEP60-12AR Si power diode with a rated breakdown voltage of 1.2 kV. This device was chosen because it allowed for reverse-bias testing to be safely conducted across the full voltage range of the MPSMU. The DSEP60-12AR was attached to the LoSPRaDC and multiple reverse-bias voltage sweeps were performed from 0 V to 1 V, 1 V to 40 V, 40 V to 100 V, and 0 V to 100 V, across each

sampling range. The results of these tests are shown in Figure 66, Figure 67, and Figure 68.

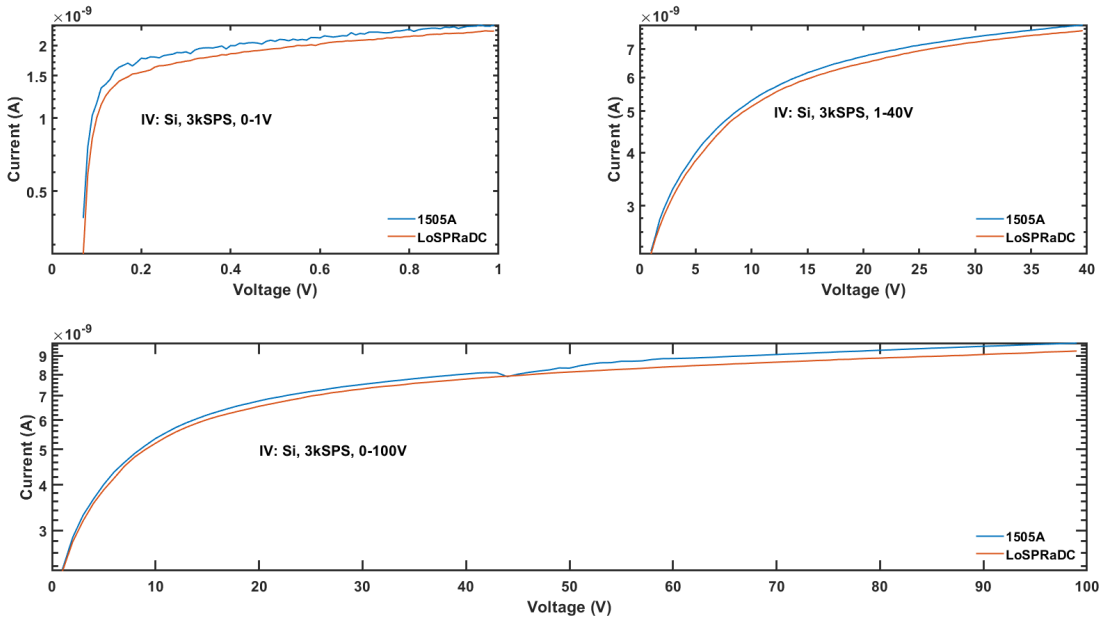

Figure 66. Si IV Plots, 3 kSPS

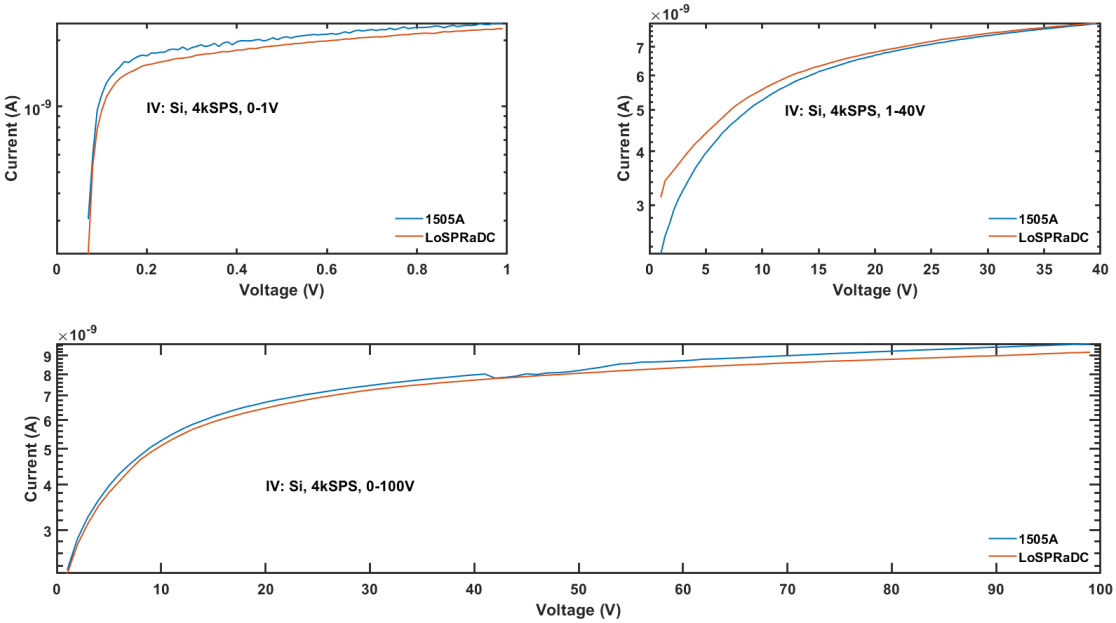

Figure 67. Si IV Plots, 4 kSPS

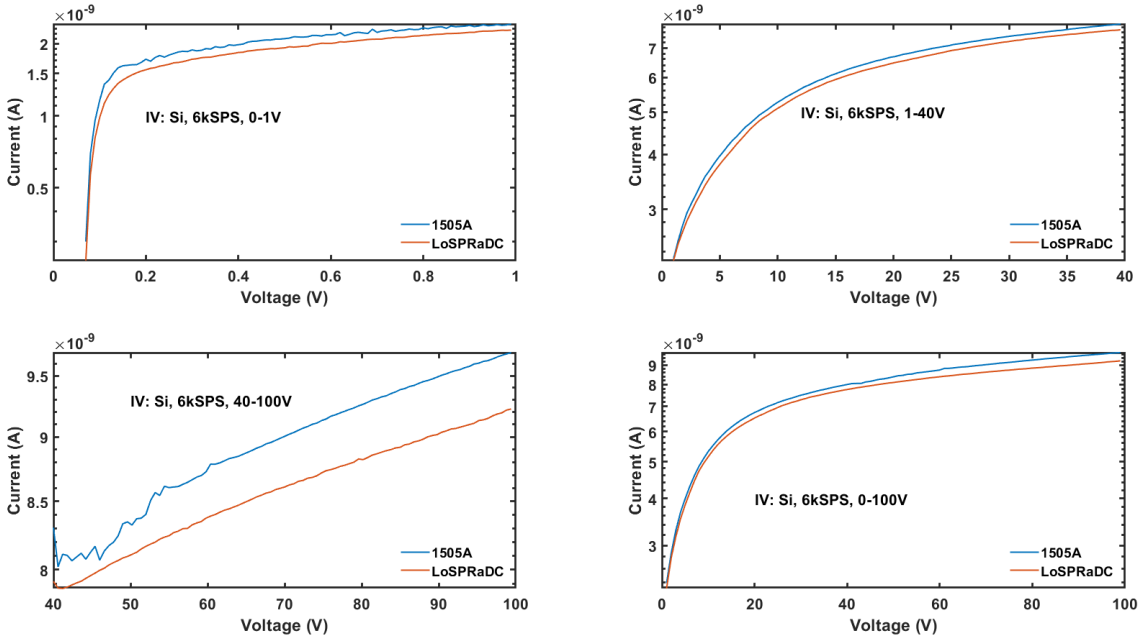

Figure 68. Si IV Plots, 6 kSPS

The results of these tests validated the ability of the LoSPRaDC to measure the leakage current of a power device prior to its rated breakdown voltage. The error was within approximately 300 pA of the B1505A in this range, demonstrating the accuracy and precision of the system. It is worth noting that the LoSPRaDC was calibrated with a -350 pA offset. The 40 V to 100 V plots in Figure 65 and Figure 66 were omitted due to data corruption.

4. GaN Diode Tests

Finally, validation testing was performed on two WBGS devices. One is a commercial GaN PN diode and the other is a Re/GaN Schottky diode produced at Penn State. These devices are used to validate the ability of the LoSPRaDC to measure the leakage current of a reverse biased WBGS.

a. PN-GaN Diode

The commercial GaN diode was attached to the LoSPRaDC and multiple reverse-bias voltage sweeps were performed by the B1505A from 0 V to 0.1 V, 0.1 V to 1 V, 1 V

to 35 V, 35 V to 100 V, and 0 V to 100 V, for each sampling range. The results of these tests are shown in Figure 69, Figure 70, Figure 71, and Figure 72.

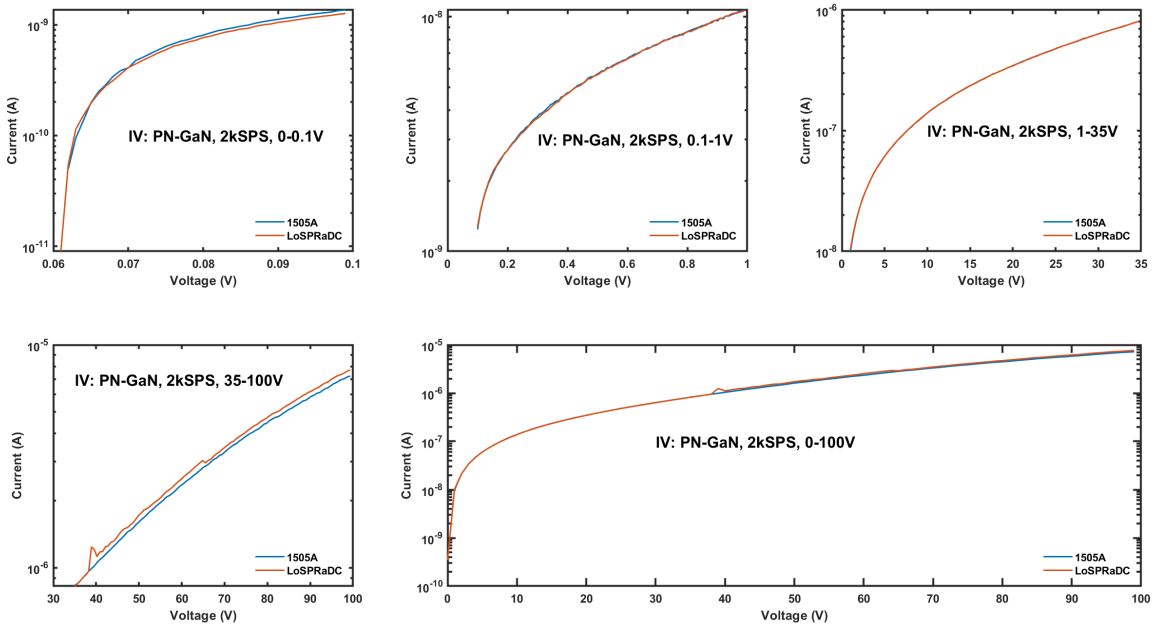

Figure 69. PN-GaN IV Plots, 2 kSPS

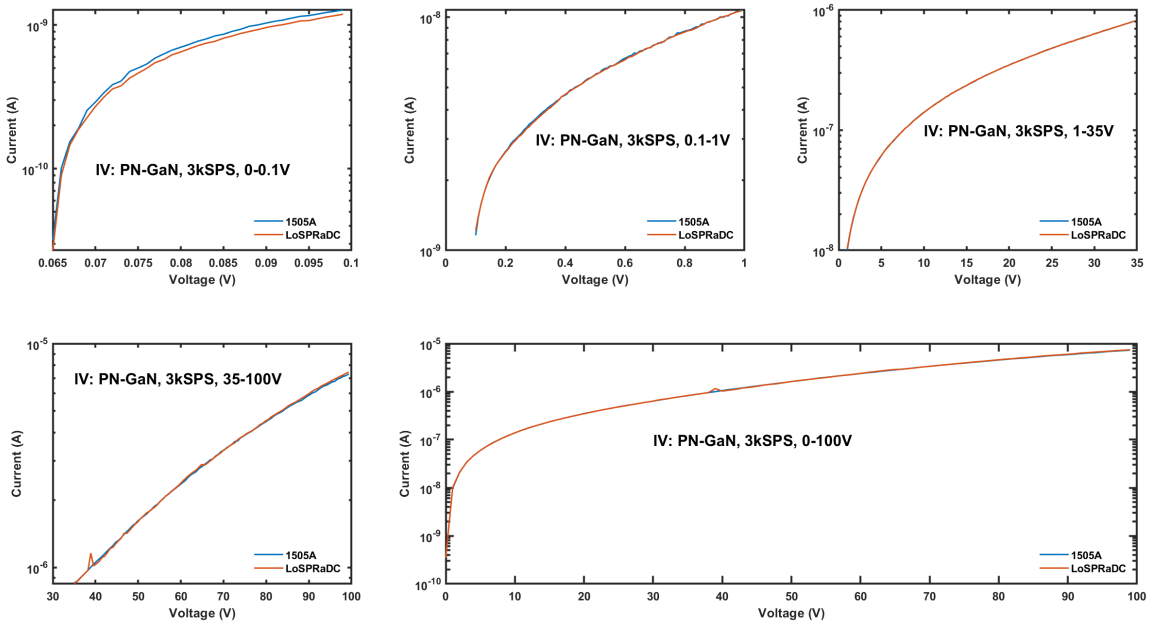

Figure 70. PN-GaN IV Plots, 3 kSPS

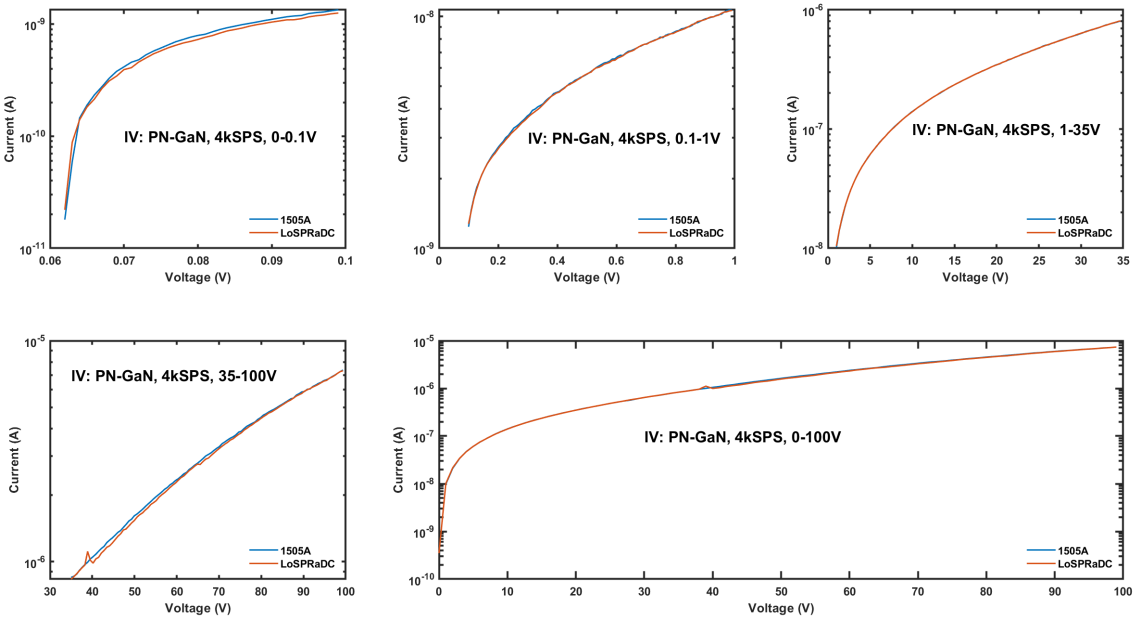

Figure 71. PN-GaN IV Plots, 4 kSPS

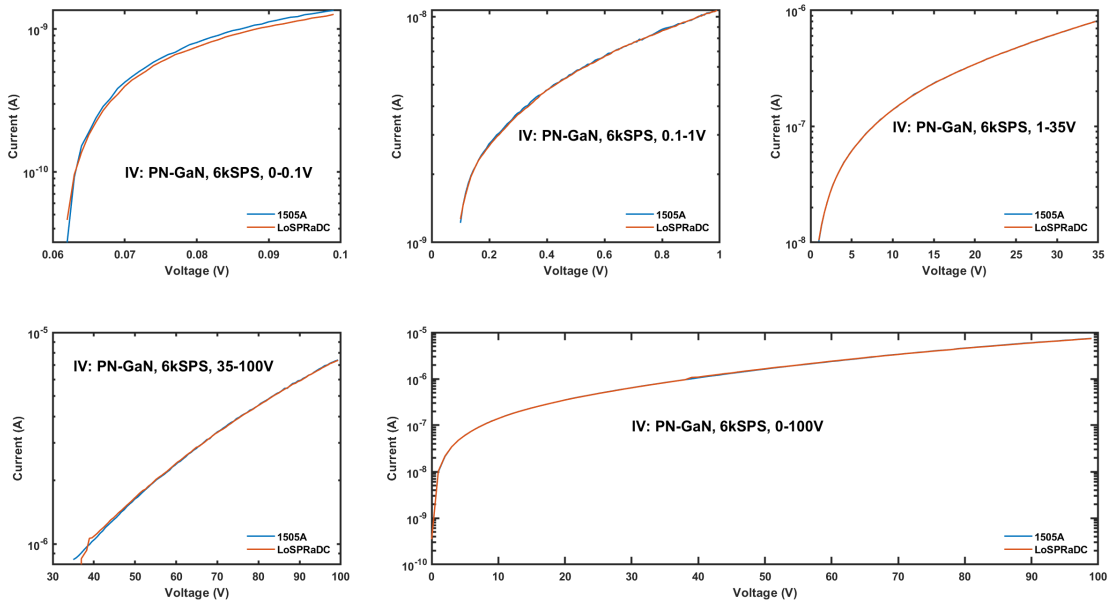

Figure 72. PN-GaN IV Plots, 6 kSPS

The results of the PN-GaN validation tests were remarkable across all sampling ranges. The lowest leakage current measured was 9 pA at 2 kSPS, shown in the 0 V to 0.1 V plot in Figure 69. In the pA to µA range, the average measurement error between the

B1505A and LoSPRaDC was approximately 40 pA across all sampling ranges. Above 1 µA, the average measurement error was approximately 1.2 nA across all sampling ranges.

b. Re/GaN Schottky Diode

The Penn State fabricated Re/GaN Schottky package consists of a five DUT array with a common ground pad at the cathode and five individual pads at the anode, all of which are coated in a nonconductive epoxy. This allows for the fabrication of multiple devices on the same substrate and subsequent placement in a single package for testing. For these tests, only a single device from this array was used. Therefore, only a single Re/GaN Schottky diode was attached to the LoSPRaDC and multiple reverse-bias voltage sweeps were performed by the B1505A from 0 V to 4 V, 4 V to 30 V, and 0 V to 30 V, for each sampling range. The results of these tests are shown in Figure 73, Figure 74, Figure 75, and Figure 76.

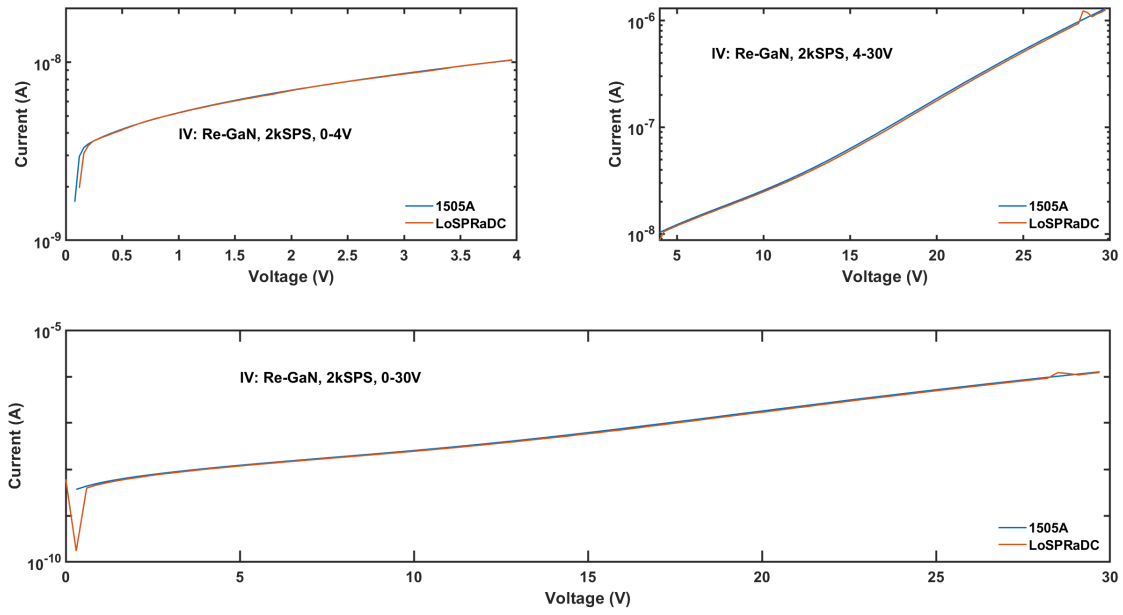

Figure 73. Re/GaN IV Plots, 2 kSPS

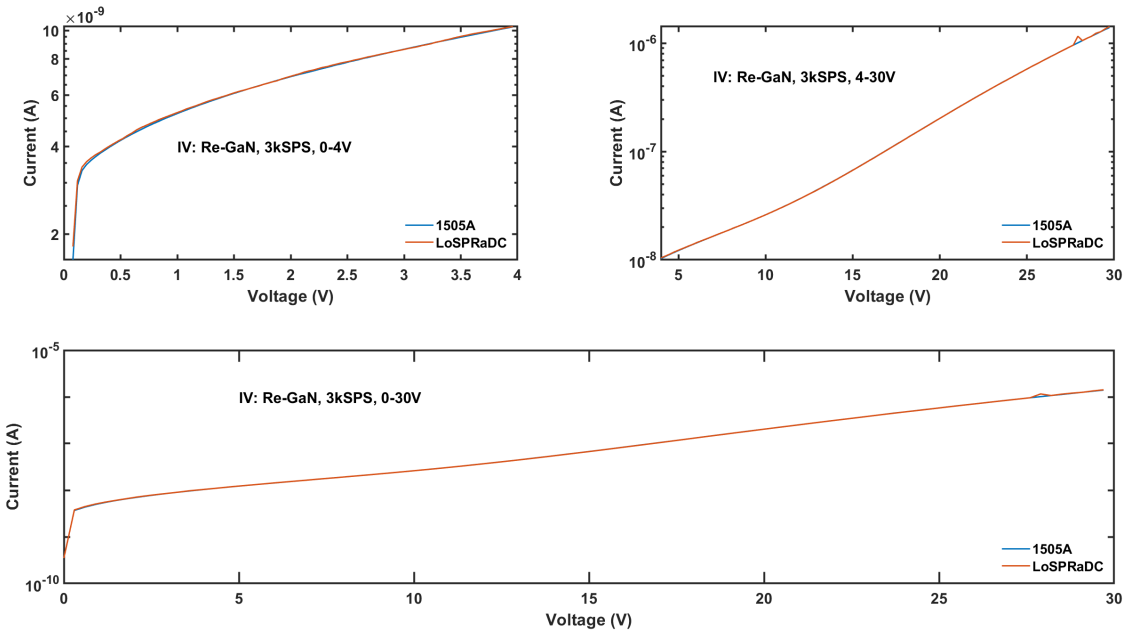

Figure 74. Re/GaN IV Plots, 3 kSPS

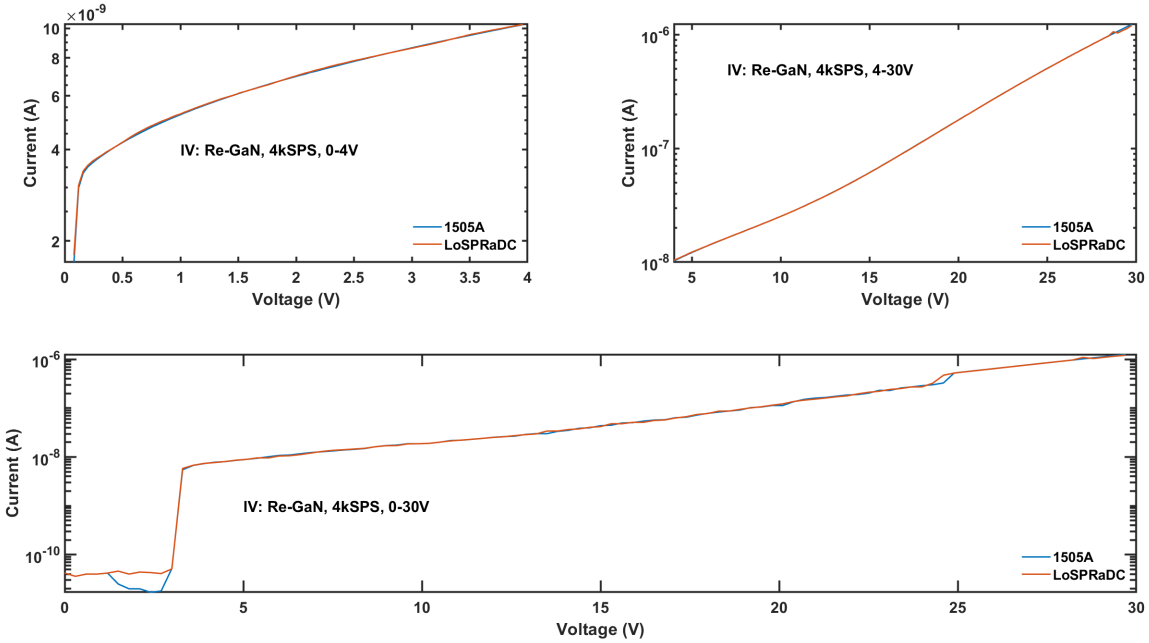

Figure 75. Re/GaN IV Plots, 4 kSPS

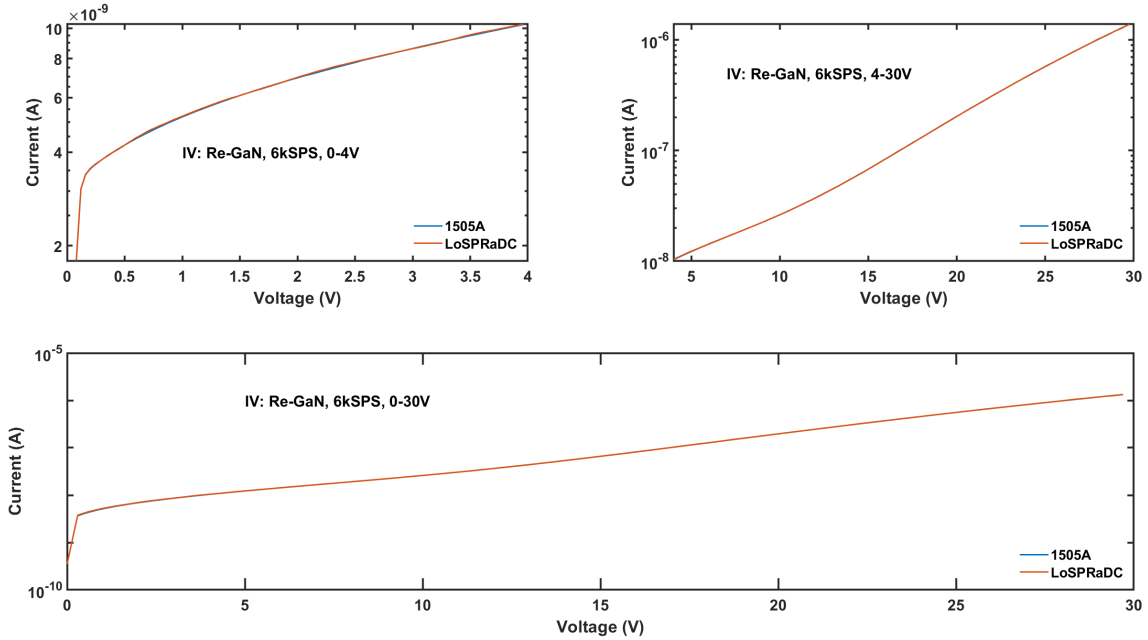

Figure 76. Re/GaN IV Plots, 6 kSPS

From the results of the PN-GaN validation tests, the largest leakage current measurement error was 4 nA at 2 kSPS, shown in the 4 V to 30 V plot in Figure 73. However, the smallest measurement error was 8 pA at 6 kSPS, shown in the 0 V to 100 V plot in Figure 76. This low error is what makes it seem as if the B1505A measurement data is not present in some of the figures. In the nA to µA range, the average measurement error between the B1505A and LoSPRaDC was approximately 50 pA. Above 1 µA, the average measurement error varied from 30 nA at 2 kSPS to 5 nA at 6 kSPS, in Figure 73 and Figure 76, respectively. Overall, results of the two GaN diode tests validated the ability of the LoSPRaDC to measure reverse-bias leakage currents of WBGS with a high degree of precision and accuracy.

5. IRF540Z Power FET Test

The final validation test was performed on an IRF540Z MOSFET. This device was chosen to validate the ability of the LoSPRaDC to test a three-terminal device. The gate of the device was biased by the triple power supply, the drain was swept by the B1505A from 0 V to 20 V, and the source was connected to the input of the LoSPRaDC. Figure 77, Figure

78. Figure 79, and Figure 80 show the IV curves produced by both systems. Finally, Figure 81 shows an overlay of all the IV curves measured by the LoSPRaDC at 6 kSPS.

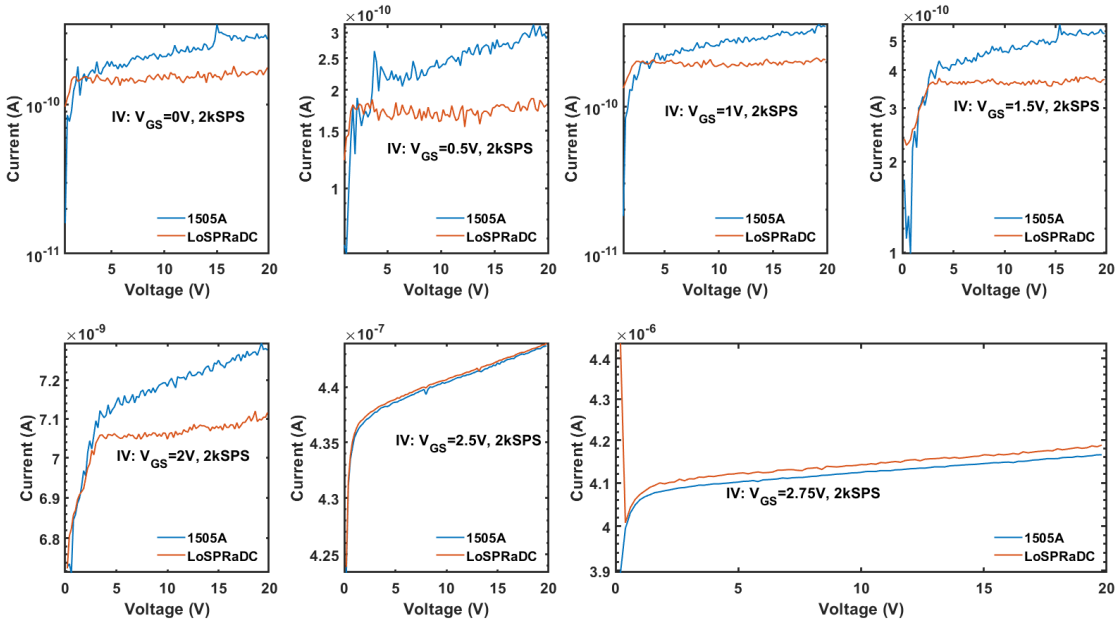

Figure 77. FET IV Plots, 2 kSPS

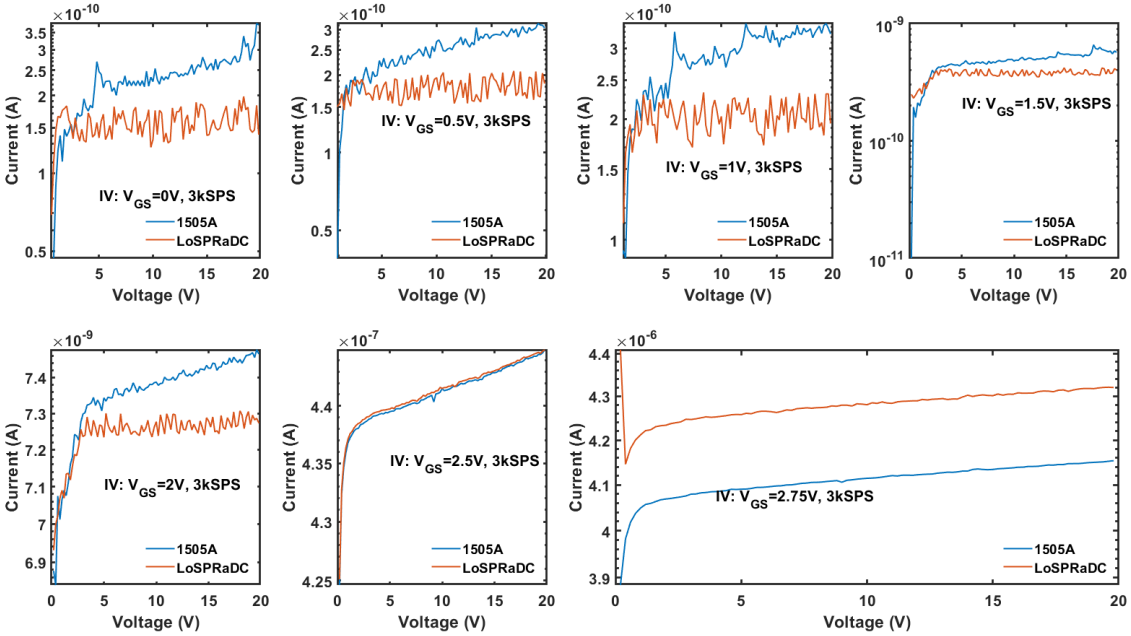

Figure 78. FET IV Plots, 3 kSPS

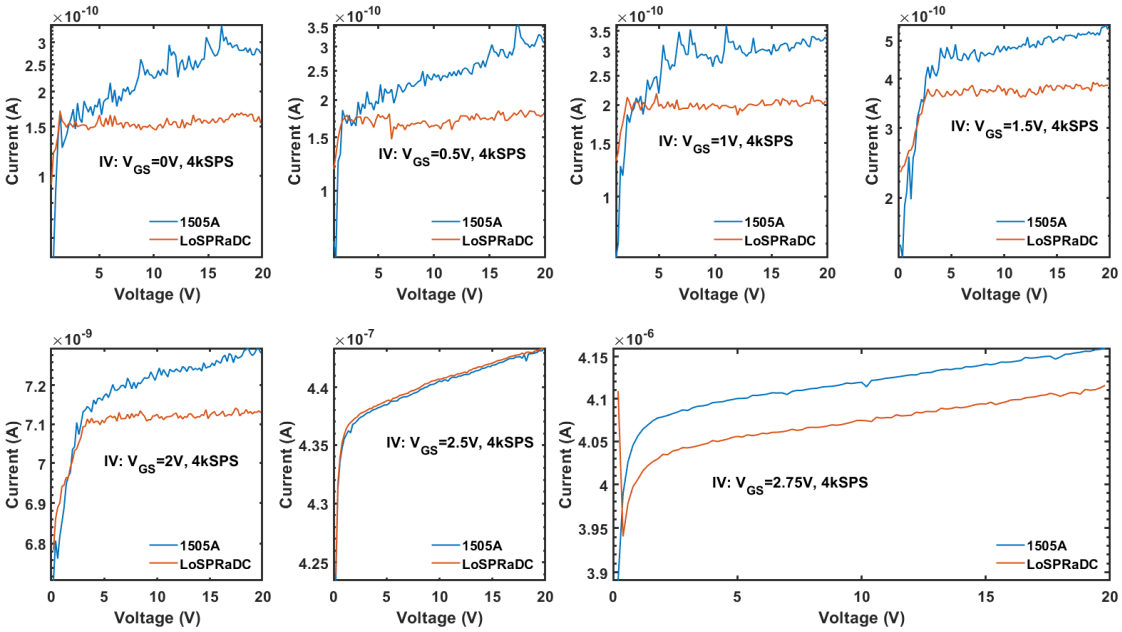

Figure 79. FET IV Plots, 4 kSPS

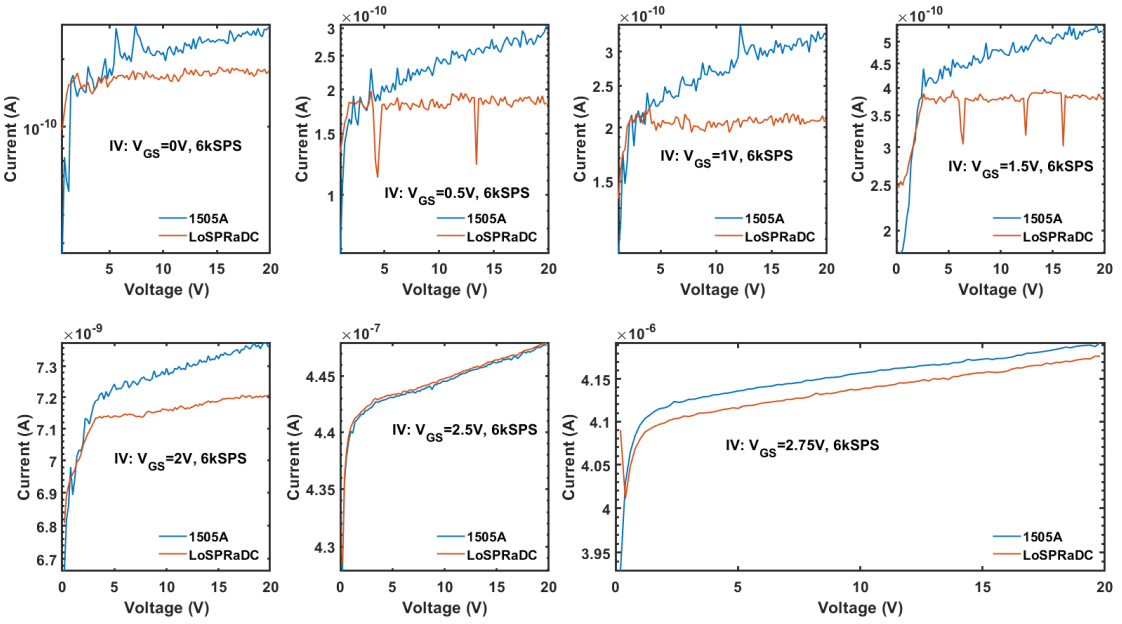

Figure 80. FET IV Plots, 6 kSPS

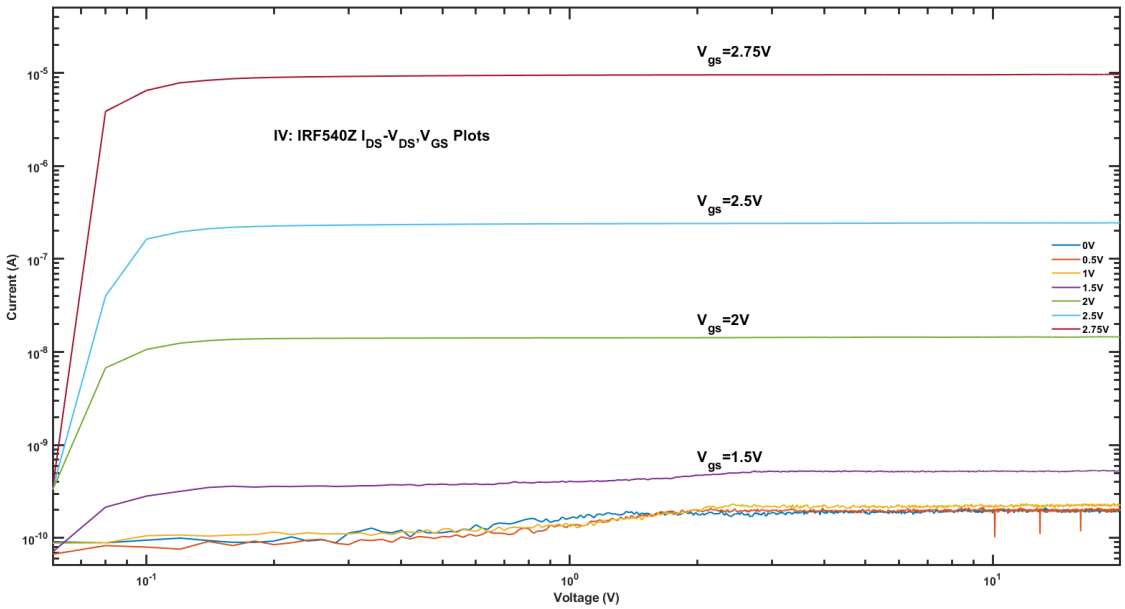

Figure 81. MOSFET Output Characteristic Curve

The results of Figure 77, Figure 78, Figure 79, and Figure 80, validate the ability of the system to measure the leakage current of a three-terminal device. The 0 V to 2 V V_{GS} plots in each of these figures show a current deviation between the LoSPRaDC and the B1505A at lower leakage current values. This deviation is due to the LoSPRaDC only measuring the I_S source current, whereas the B1505A is measuring the total leakage current through the drain I_D, which is the sum of both I_S and the gate leakage I_G. The 2.5 V V_{GS} plots in each of these figures show an offset error of approximately 300 pA. The measurement error in the 2.75 V V_{GS} plots of these figures is due to varying calibration error of the range two R_f value for each sampling range. Finally, Figure 81 demonstrates the ability of the LoSPRaDC to characterize a three-terminal device.

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V. CONCLUSION AND FUTURE WORK

A. CONCLUSION

The primary goal of this thesis was to design, build, and test a modular, automated data acquisition system that could measure low leakage currents generated by various types of DUTs under an active electrical stress. A circuit was designed to measure sub-nA reverse-leakage currents using an inverting TIA op-amp configuration. Stability analysis was performed on this circuit using LTSpice, ensuring a PM greater than 45° up to an input capacitance of 8 nF. A noise analysis was then done which led to the implementation of a second stage LPF to reduce noise by almost 60% in the first measurement range and 34% in the second. Focus then shifted to the design of an ultra-low leakage PCB and a DAQ board built around a 16-bit ADC. The manufacturing of the two PCBs marked the end of the design phase.

The build phase began with the physical completion of the board, which included the installation of low-leakage PTFE terminals and the feedback components on the LMB and all the components on the DAQ board. The build then continued with the programming of the Mbed used to control the LoSPRaDC, allowing it to communicate externally, and the LabView program used to interface the LoSPRaDC and the B1505A with a PC system interface. Calibration of the system was done programmatically, first adjusting the noise floor offset, then implementing an averaging scheme based on samples and NPLCs. Calibrating the range resistors marked the end of the build phase.

Finally, the testing phase consisted of performing various validation tests on an array of devices. Devices were chosen to demonstrate the flexibility of the system, eventually culminating with validation testing done using two WBGS devices and a three-terminal device. The results validated the design requirements, showing that the LoSPRaDC could measure sub-nA leakage currents, even when not configured with a feedback resistance value typically expected for those sorts of measurement ranges. Averaging and sampling made this possible, lowering the 16-bit resolution of the system from 152 pA to on the order of 10 pA.

The validation of this system expands the WBGS reliability testing capabilities available to all students and researchers. Expanding access to reliability testing systems also increases the overall testing volume, giving researchers quicker turn-around times on the performance characteristics of the devices they fabricate. This effectively shortens the research and development timeline for WBGS devices, increasing the rate at which these devices are implemented into advanced electronic systems needed by the USMC today.

B. FUTURE WORK

Recommendations for future work include the utilization of the two I^2C interfaces and that eight digital IO ports that are already configured on the DAQ board. These interfaces are ideally suited for integration with a high voltage switch matrix. This would expand the ability of the system to perform automated testing, allowing for the configuration of leakage current thresholds that can be used to control the switching of DUTs out of the stress condition. This allows for non-destructive reliability testing, giving researchers the opportunity to analyze devices for potential indicators that might help improve fabrication or packaging methods. The I^2C connections can be used to integrate various sensors needed for HTRB testing, like humidity sensors, fan controllers, wireless modules for isolated control, and even external LED screens for visualizing performance or output data.

Board level recommendations include implementing a coaxial connection to the input of the LMB, vice the PTFE standoffs that are used now. This would allow for greater shielding of the inputs from EMI, which is critical when performing sub-pA current measurements. Other options include choosing a different ADC with more than four channels to increase the testing volume by simply constructing more LMBs.

Finally, the current measurement range can be extended by configuring multiple LMBs with different range resistance values in parallel and switching them into the circuit as needed. Given the design of the LoSPRaDC, up to four LMBs could be configured with eight different resistance values per DAQ board and an updated Mbed program could control the switching of the individual range resistors, as well as the different boards.

APPENDIX A. ADC CONTROL BOARD MBED PROGRAM

The Mbed control program made for this thesis is only preliminary; moreover, given the intended functionality of the ADC board, it would need to be expanded upon for future design iterations.

```
#include “mbed.h”

using namespace std;

BufferedSerial pc(USBTX,USBRX);
SPI spi(NC,p6, p7); // mosi, miso, sclk
DigitalOut rc(p5); // R/C, controls conversion
DigitalIn busy(p8); // busy signal from the ADC
DigitalOut a1(p11); // A1 pin of the ADC
DigitalOut a0(p12); // A0 pin of the ADC
DigitalIn sync(p13); // sync signal from the ADC
DigitalOut ext_int(p14); // EXT/INT pin of the microcontroller
DigitalOut range1(p20); // RANGE1 pin of the microcontroller

// Convert the ADC value to a current in amperes
float convertToAmps(uint16_t adc_value, float resistor) {
 if (adc_value > 65535 || resistor == 0) {
     return -1; // handle out-of-range error
 }
 float current = (float)adc_value * (4.0 / 65536.0) / resistor;
 return current;
}
// Compute the average of uA samples
float computeAvgSamples(float uA_sum,int samples) {
 float uA_avg = uA_sum / samples;
 return uA_avg;
}// Offset measurement
float measurement(int samples,int nplc) {
 bool measure_current = true;
 int sample_count = 0;
 float resistor = 400000.0; // resistor value for current calculation
 Timer timer; // create a timer to measure sampling time
 float uA_sum = 0.0; // sum value of uA
 float uA_avg = 0.0;
 uint16_t adc_value;
 float current;
```

```
float uA;
timer.start();
while (measure_current) {
    // Wait for ADC to be ready
    while (busy == 1) {
        // Hold the analog input signal internally
        rc = 0;
        wait_ns(60);
        // Enable the transmission of the conversion result
        rc = 1;
    }
    while (busy == 0) {         // Wait for busy to go low
        wait_ns(100);
    }
    adc_value = spi.write(0x0000); // Send command to ADC to read data
    // Convert the ADC value to a current
    current = convertToAmps(adc_value,resistor);
    if (current == -1) {
        // handle out-of-range error
        continue;
    }
    uA = current * 1000000.0; // Convert the current to microamps (uA)
    // Check if the current exceeds 1 uA,
    // if it does then switch in parallel resistor
    if ((uA > 1.0) && (resistor == 400000)){
        range1=1;
        resistor = 10500;
        uA=uA-0.03;
        wait_us(350); // typical operate time of Reed Relay
    }
    // Check if the current is under 0.2 uA,
    // if it is then switch out the parallel resistor
    else if ((uA < 0.2) && (resistor == 10500)){
        range1=0;
        resistor = 400000;
        wait_us(10); // typical release time of Reed Relay
    }
    uA_sum += uA-350e-6;         // add the uA sample to the sum
    sample_count++;         // increment the sample counter by 1
    // Check if sample count is reached
    if (sample_count >= samples) { // Stop measuring current
        measure_current = false;   // compute the average
        uA_avg = computeAvgSamples(uA_sum, samples);
        // reset the sum and sample count
```

```
            uA_sum = 0.0;
            sample_count = 0;
        }
        // wait until 1/60/nsamples of a second has passed
        while (timer.elapsed_time().count() < nplc/60.0/samples) { // do
nothing
        }
        // reset the timer
        timer.reset();
    }
    return uA_avg; // returns the value of uA_avg
}
int main() {
    // Set Digital Output Parameters
    rc = 1; // Set R/C to start high
    a1 = 0;  // Set A1 to LOW
    a0 = 0;  // Set A0 to LOW
    ext_int = 1;  // Set EXT/INT to HIGH
    range1 = 0;  // Set RANGE1 to LOW
    // Set up serial communication and SPI
    pc.set_baud(115200);  // Set baud rate for serial communication
    spi.format(16, 3); // 16-bit data, mode 0
    spi.frequency(10000000); // 10 MHz clock frequency
    int samples=6000; // number of samples we are taking
    float resistor = 400000.0; // resistor value for current calculation
    bool measure_current = false; // flag to indicate whether to measure the
current
    Timer timer; // create a timer to measure sampling time
    float uA_avg = 0.0; // sum value of uA
    int nplc=2.0;
    char cmd=0;
    int len=0;
    while (1) {
        if (pc.readable()) {
            pc.read(&cmd,1);
            if (cmd==‘s’) {
                uA_avg=measurement(samples,nplc);
                printf(“%.6f\n”,uA_avg);
            }
        }
    }
}
```

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APPENDIX B. LABVIEW PROGRAMS

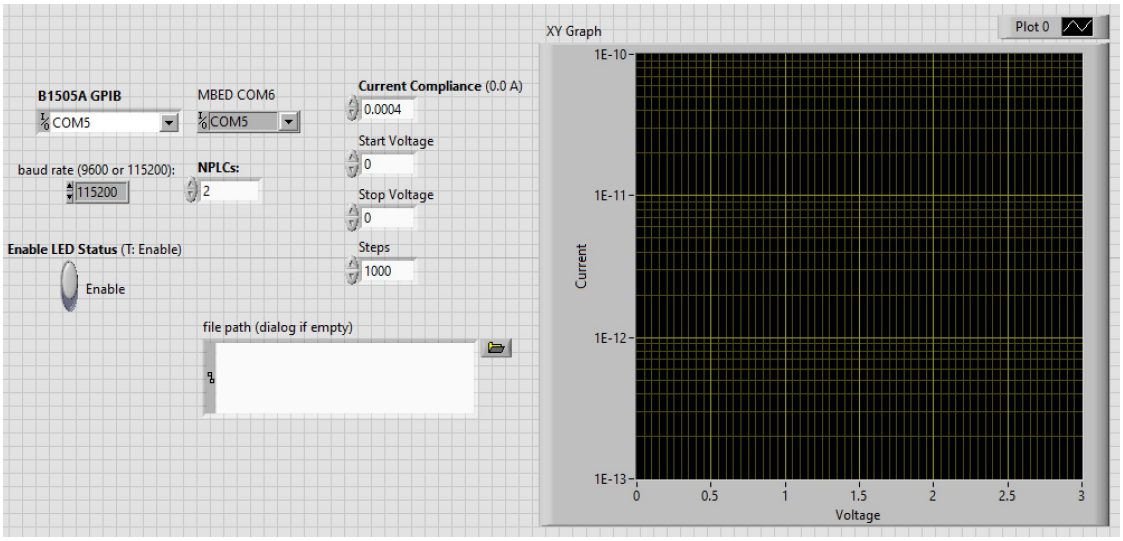

Figure 82. Front Control Panel of LoSPRaDC LabVIEW VI

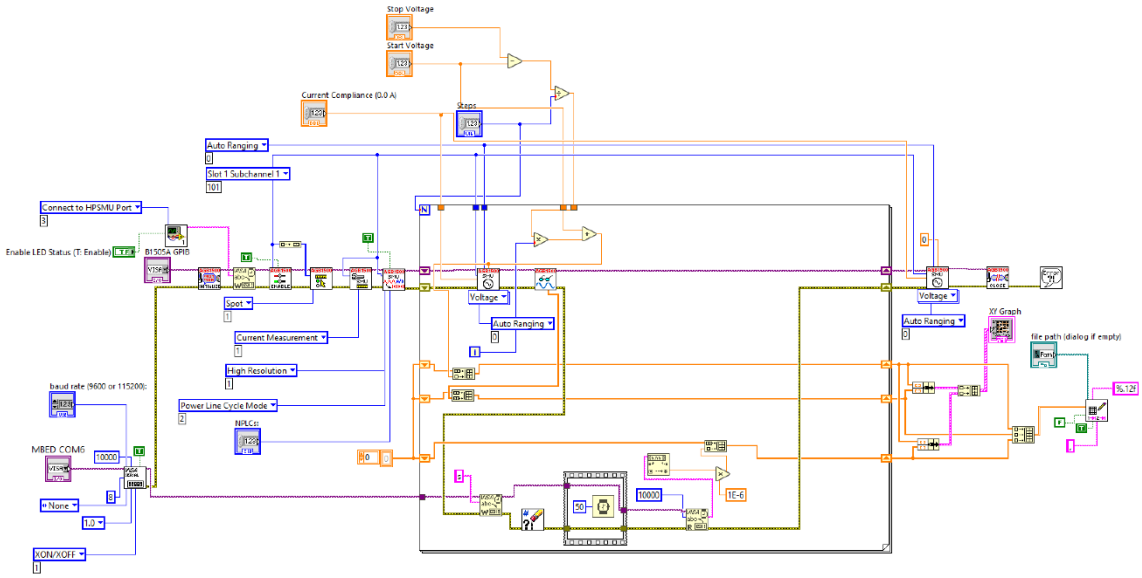

Figure 83. Block Diagram of LoSPRaDC LabVIEW VI

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